North Atlantic Industries

Excellence in ALL we do

Model **64RS2**

Twelve (12) Synchronous/Asynchronous RS-232C, RS-422, RS-485 Channels

VMEbus CONTROL

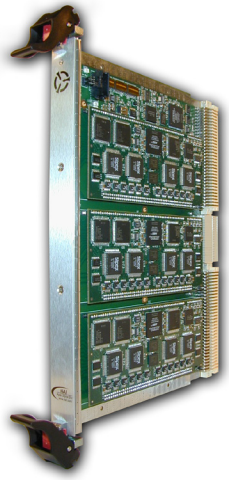
SERIAL COMMUNICATION CARD

TWELVE, EIGHT, or FOUR INDEPENDENT & PROGRAMMABLE

RS-232C, RS-422, RS-485

SYNCHRONOUS or ASYNCHRONOUS

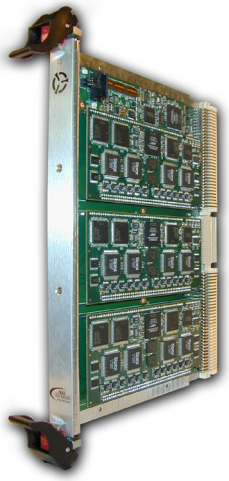
For Commercial or Military Applications



Typical Configuration

FEATURES

- Independent full-duplex synchronous or asynchronous channels
- High Data Rate (8 Mbps synchronous, 800 Kbps asynchronous)
- Programmable for RS-232C, RS-422, RS-485
- Hardware data transfers minimize data latency
- Power-on loop-back self-test
- Watchdog timer and soft reset
- I/O via front panel, P2 or both
- Part Number, S/N, Date Code, & Revision in non-volatile memory
- Conforms to ANSI/VITA 1.1-1997 VME64 extension
- Conforms to VITA 1-1994
- VxWorks Library and Driver Available



Typical Configuration

DESCRIPTION

This sophisticated, high-speed, DSP-based card incorporates up to twelve (12) intelligent, full duplex communications channels that can be individually software configured for RS-232C, RS-422 or RS-485 Synchronous or Asynchronous Communication. The architecture **avoids latency problems** because all data transfer is done in hardware and not in software. DSP runs at 160 MHz and only handles background tasks such as interrupt generation. Any incoming data, no matter how many channels are active, in whatever mode, can be immediately extracted. A BREAK sequence capability is also incorporated. Bus Data is transferred within 300 ns. **A layer of software isolates the user from UART idiosyncrasies thus simplifying programming and usage.**

An **Internal Loop Back Self Test** is performed when power is applied and results are stored in registers. During Loop Back test, the outputs are disconnected. Each channel can be programmed into a **Loop Back mode** that internally wraps the transmitter to the receiver without the need of external wiring. Output short circuit capability is continuous and bullet proof. If the card is not powered, neither the inputs nor outputs will load down the lines. Inputs and outputs can withstand ±15 volts under any condition. All serial lines are transient protected to IEC1000 4-2, 4-4, & 4-5.

Serial Data Transmit Enhancement: An additional asynchronous mode to support "Immediate Transmit" operation has been incorporated. This mode immediately transmits serial data anytime the transmit buffer is not empty. There is no requirement to set the "TX Initiate" bit after each byte where VME traffic and overhead can be simplified since only the actual data byte being transmitted needs be sent to the transmit buffer. Each channel has its own 64kbyte Transmit and Receive buffer.

While in Asynchronous mode, the upper byte of each received word provides status information for that word.

Receiver Enable/Disable: A Receiver Enable/Disable function allows the user to turn selected receivers ON/OFF. When a receiver is disabled, no data will be placed in the buffer. (Card is shipped with all receivers enabled).

DSR capability is available for channels 1-6 via P2 & P0, and for channels 1-12 from front panel connectors.

CRC code generation and detection is also available for message integrity when used in Synchronous, HDLC and Asynchronous PPP modes.

This serial card can operate in an **Interrupt Driven Environment** to provide notification of all events to the system. It supports hardware flow control (CTS/RTS and/or DCD/DTR) as well as software flow control (XON, XOFF). When a flow control mode is selected, the serial card does the operation automatically with minimal system intervention.

A Parity Error Interrupt is provided for each single byte throughout the communications data stream.

Multi-Drop Link Mode: The transmitter and receivers of up to 32 cards can be tied together in either Half or Full Duplex mode. While in Multi-Drop Link Mode, the transmit line for each channel will automatically change from tri-state to enable to transmit any data as soon as it is placed in the transmit buffer. Once transmission is completed, the transmit line is automatically changes back to tri-state mode.

For **redundant applications**, this card can be paralleled with another card to offer redundancy. User provided software control is required to drive one output ON at time during data transmission. No two or more cards in parallel should transmit simultaneously. Output levels are in “tri-state” while transmission is inactive.

Geographical addressing can be implemented

A **watchdog timer** is provided to monitor processor activity.

To simplify logistics, Part number, Serial number, Date code and Rev Level are stored in non-volatile memory locations.

A VxWorks Software Communications Driver & Library is available from our WEB site http://www.naii.com.

A current, updated soft copy of this manual is also available at our web site.

SPECIFICATIONS

Number of channels:	Twelve (12) fully programmable
Data rate:	8 Mbits/s per channel in Synchronous/HDLC mode 800kbits/s per channel in Asynchronous mode (RS-422 & RS-485) Data can be read 4µs after receipt in UART. These data rates are verified with **all** channels running simultaneously.

Asynchronous and synchronous (internal clock) Bit Rate Generation limitation(s):

Bit rate generation is based on a primary clock divided by an integer value.

Programmed bit versus actual bit rate will have greater resolution at lower bit rates (<115 KHz). When specifying internal clock, the card generates and transmits the actual bit rate as close (rounding off) to the programmed bit rate based on the following formula:

Actual bit rates available:

25 MHz / N	(synchronous)
1.5625 MHz / N	(asynchronous)
	(N = integer)

Asynchronous examples:

Programmed Bit Rate (b/s)	(Integer Divisor)	Actual Bit Rate
381 (minimum)	4096	381.5
600	2604	600
2400	651	2400
9600	163	9586
57600	27	57870
115200	14	111607
300000	5	312500
600000	3	520883
800000 (maximum)	2	781250

Note: Bit generation formulas may differ between product models.

VME Data transfer:	**Data transfers within 300 ns.**
Receive/Transmit buffers:	64 Kbytes for each Receive and Transmit buffer. Accessed in 16 bit mode only.
Interrupts:	1 vector per channel
Power:	+5 VDC, 1A per module (Mode dependant: RS232 has lower power req’ts, RS422 more)
Temperature, operating:	C" 0°C to +70°C, "E" -40°C to +85°C (See part number)
Storage temperature:	-40°C to +105°C.
Base address:	Geographical addressing can be implemented. Otherwise, board dip switches are activated for setting base address.
Size:	(9.2") H, 4HP (0.8") W. 233.4 x 20.3 x 160 mm deep
Weight:	22 oz.

I/O CONFIGURATION:

The VME bus interface will respond to A32:D16, A24:D16 and A16:D16 DTB cycles.

A32 mode: Unit responds to address modifiers 0A, 0D, 0E and 09. Base address can be set anywhere in the 4 Gigabyte address space on 512 byte boundaries.
A24 mode: Responds to address modifiers 3A, 3D, 3E and 39. Base address can be set anywhere in the 16 Megabyte address space on 512 byte boundaries.
A16 mode: Responds to address modifiers 2A, 2D, 2E and 29. Base address can be set anywhere in the 64 K byte address space on 512 byte boundaries.

Note: Address switch A8, A9 & A10 must be set to "ON" for 2048 byte boundaries (SW1.1, SW1.2, & SW1.3)

Enable Geographical Addressing by removing jumper from JP2. Disable by adding jumper to JP2.

GEOGRAPHICAL ADDRESSING

Geographical Addressing may be implemented implemented. This card will respond to address modifier 2Fh for A24 Address mode, where the 5 Msb's of the A24 address are the 5 bits defined by the slot in VME back plane. The Card can optionally be interrogated at 2Fh to determine resource requirements and available functionally. Using the address modifier 2Fh, the following need to be written to the card:

1) The base address the card should respond to
2) The address modifier (A16, A24, A32)
3) Then enable the card.

For example: If the card is in slot # 10 the 5 Msb's are 01010 so the address of the CSR registers are:
0101 0 111 1111 1111 xxxx xxxx or 57FFxx h (xx is CSR register offset)

Write to address 57FF63 h, the A31 – A24 base address bits, for example 01h
Write to address 57FF67 h, the A23 – A16 base address bits, for example 02h
Write to address 57FF6B h, the A15 – A8 base address bits, for example 04h
Write to address 57FF6F h, the address modifier you wish to respond to shifted up 2 bits, ex. 28h(0A<< 2)

then write to address 57FFFBh, 10h to enable the card.

The card will now respond to the base address (010204 in the example) and address modifier (0A in example) programmed. The base address and address modifier can be changed at any time.

PRODUCT CONFIGURATION AND MEMORY MAP

This card is populated with up to 3 modules of 4 Serial Communication Channels. As such, the card can be configured as a 4, 8 or 12 channel card. The memory map of each module counts from, or is superimposed over, its respective module offset (1 through 3).

Address = Base + Module Offset + Register Offset.

For example: Address = Base + Module 2 offset 200 + MRS2 register 00C = Base + 20C hex.

MEMORY MAP

000	Module 1 Register…	200	Module 2 Register…	400	Module 3 Register…
002		202		402	
004		204		404	
006		206		406	
008		208		408	
.		.		.	
.	Module 1 Offset 000	.	Module 2 Offset 200	.	Module 3 Offset 400
.		.		.	
1FC	Channels 1-4	3FC	Channels 5-8	5FC	Channels 9-12
1FE		3FE		5FF	

The memory map of the 4 channel Serial Communications module is described hereafter:

MODULE MEMORY MAP – 4 CHANNEL SERIAL COMMUNICATIONS (P1)

000	Tx Buffer Chan 1	W	074	Channel Control Low Chan 3	R/W	0F0	Termination Character Chan 1	R/W
002	Tx Buffer Chan 2	W	076	Channel Control High Chan 3	R/W	0F2	Termination Character Chan 2	R/W
004	Tx Buffer Chan 3	W	078	Channel Control Low Chan 4	R/W	0F4	Termination Character Chan 3	R/W
006	Tx Buffer Chan 4	W	07A	Channel Control High Chan 4	R/W	0F6	Termination Character Chan 4	R/W
00C	Rx Buffer Chan 1	R	084	Data Configuration Chan 1	R/W	0FC	XON Character Chan 1	R/W
00E	Rx Buffer Chan 2	R	086	Data Configuration Chan 2	R/W	0FE	XON Character Chan 2	R/W
010	Rx Buffer Chan 3	R	088	Data Configuration Chan 3	R/W	100	XON Character Chan 3	R/W
012	Rx Buffer Chan 4	R	08A	Data Configuration Chan 4	R/W	102	XON Character Chan 4	R/W
018	Number Of Words Tx Buffer Chan 1	R	090	Baud Rate Low Chan 1	R/W	108	XOFF Character Chan 1	R/W
01A	Number Of Words Tx Buffer Chan 2	R	092	Baud Rate High Chan 1	R/W	10A	XOFF Character Chan 2	R/W
01C	Number Of Words Tx Buffer Chan 3	R	094	Baud Rate Low Chan 2	R/W	10C	XOFF Character Chan 3	R/W
01E	Number Of Words Tx Buffer Chan 4	R	096	Baud Rate High Chan 2	R/W	10E	XOFF Character Chan 4	R/W
024	Number Of Words Rx Buffer Chan 1	R	098	Baud Rate Low Chan 3	R/W	114	FIFO Status Chan 1	R
026	Number Of Words Rx Buffer Chan 2	R	09A	Baud Rate High Chan 3	R/W	116	FIFO Status Chan 2	R
028	Number Of Words Rx Buffer Chan 3	R	09C	Baud Rate Low Chan 4	R/W	118	FIFO Status Chan 3	R
02A	Number Of Words Rx Buffer Chan 4	R	09E	Baud Rate High Chan 4	R/W	11A	FIFO Status Chan 4	R
030	Protocol Chan 1	W	0A8	Preamble Chan 1	R/W	120	Time Out Value Chan 1	R/W
032	Protocol Chan 2	W	0AA	Preamble Chan 2	R/W	122	Time Out Value Chan 2	R/W
034	Protocol Chan 3	W	0AC	Preamble Chan 3	R/W	124	Time Out Value Chan 3	R/W
036	Protocol Chan 4	W	0AE	Preamble Chan 4	R/W	126	Time Out Value Chan 4	R/W
03C	Clock Mode Chan 1	W	0B4	Tx Buffer Almost Empty Chan 1	R/W	180	Interrupt Enable Chan 1	R/W
03E	Clock Mode Chan 2	W	0B6	Tx Buffer Almost Empty Chan 2	R/W	182	Interrupt Enable Chan 2	R/W
040	Clock Mode Chan 3	W	0B8	Tx Buffer Almost Empty Chan 3	R/W	184	Interrupt Enable Chan 3	R/W
042	Clock Mode Chan 4	W	0BA	Tx Buffer Almost Empty Chan 4	R/W	186	Interrupt Enable Chan 4	R/W
048	Interface Levels Chan 1	W	0C0	Rx Buffer Almost Full Chan 1	R/W	18C	Interrupt Status Chan 1	R/W
04A	Interface Levels Chan 2	W	0C2	Rx Buffer Almost Full Chan 2	R/W	18E	Interrupt Status Chan 2	R/W
04C	Interface Levels Chan 3	W	0C4	Rx Buffer Almost Full Chan 3	R/W	190	Interrupt Status Chan 3	R/W
04E	Interface Levels Chan 4	W	0C6	Rx Buffer Almost Full Chan 4	R/W	192	Interrupt Status Chan 4	R/W
054	Tx-Rx Configuration Low Chan 1	R/W	0CC	Rx Buffer High Watermark Chan 1	R/W	198	Interrupt Vector Chan 1	R/W
056	Tx-Rx Configuration High Chan 1	R/W	0CE	Rx Buffer High Watermark Chan 2	R/W	19A	Interrupt Vector Chan 2	R/W
058	Tx-Rx Configuration Low Chan 2	R/W	0D0	Rx Buffer High Watermark Chan 3	R/W	19C	Interrupt Vector Chan 3	R/W
05A	Tx-Rx Configuration High Chan 2	R/W	0D2	Rx Buffer High Watermark Chan 4	R/W	19E	Interrupt Vector Chan 4	R/W
05C	Tx-Rx Configuration Low Chan 3	R/W	0D8	Rx Buffer Low Watermark Chan 1	R/W	1A4	Channel Status 1	R
05E	Tx-Rx Configuration High Chan 3	R/W	0DA	Rx Buffer Low Watermark Chan 2	R/W	1A6	Channel Status 2	R
060	Tx-Rx Configuration Low Chan 4	R/W	0DC	Rx Buffer Low Watermark Chan 3	R/W	1A8	Channel Status 3	R
062	Tx-Rx Configuration High Chan 4	R/W	0DE	Rx Buffer Low Watermark Chan 4	R/W	1AA	Channel Status 4	R
06C	Channel Control Low Chan 1	R/W	0E4	HDLC Address/Sync Char Chan 1	R/W	1F8	Module ID	R
06E	Channel Control High Chan 1	R/W	0E6	HDLC Address/Sync Char Chan 2	R/W	1FC	FPGA Version	R
070	Channel Control Low Chan 2	R/W	0E8	HDLC Address/Sync Char Chan 3	R/W	1FE	DSP Version	R
072	Channel Control High Chan 2	R/W	0EA	HDLC Address/Sync Char Chan 4	R/W			

Serial Communications Module register programming and its associated Bit Map is as follows:

MODULE REGISTER DEFINITIONS

Transmit Buffer

Address: 000h, 002h, 004h, 006h (Chan.1-4)
Type: unsigned character word
Range: 00h or FFh (low byte)
Read/Write: W
Initialized Value: Not Applicable

This register is the transmit data buffer. Data intended to be transmitted must be placed here prior to transmission. Data words are 8-bit and occupy the register's lowest significant bits (lsbs), or low byte. See bit map below:

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
TRANSMIT BUFFER	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	X=DON'T CARE, D=DATA BIT

Receive Buffer

Address: 00Ch, 00Eh, 010h, 012h (Chan.1-4)
Type: unsigned integer word.
Range: 00h or FFh (for low byte and for high byte)
Read/Write: R
Initialized Value: Not Applicable

This register is the receive data buffer. Data is received in the low byte as unsigned integer. The high byte is used for status.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
RECEIVE BUFFER	S	S	S	S	S	S	S	S	D	D	D	D	D	D	D	D	S=STATUS BIT, D=DATA BIT
Asynchronous	PE	FE	X	X	X	X	EOF	P	D	D	D	D	D	D	D	D	EOF only if Termination Char is used
Bi/Mono Synchronous	X	X	X	X	X	X	EOF	X	D	D	D	D	D	D	D	D	
HDLC Mode	X	X	X	X	X	X	EOF	X	VFR	RDO	CRC	RAB	X	X	C/R	X	Last Word is Status Word

PE = Parity Error — '1' Calculated parity does not match the received parity bit
FE = Framing Error — '1' A character framing error was detected.
EOF = End Of Frame — '1' Indicates End of Frame. Useful to identify multiple frames in large buffer
P = Parity Bit — This bit carries the parity bit of the last received character
VFR = Valid Frame — '0' Received fame is invalid
RDO = Receive Data Overflow — '0' No data overflow has occurred — '1' Overflow
CRC = CRC Compare/Check — '0' Fail; Received frame contains errors — '1' Pass; No CRC errors in received frame.
RAB = Receive msg Aborted — '0' No abort condition detected — '1' Receive frame was aborted.
C/R = Command/Response — Only significant for 2 byte address mode.

Number of Words Tx Buffer

Address: 018h, 01Ah, 01Ch, 01Eh (Chan.1-4)
Type: unsigned integer word
Range: 0 to 65535
Read/Write: R
Initialized Value: 0

This register contains the number of words to be transmitted.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
NUM WORDS TX BUFFER	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Number of Words Rx Buffer

Address: 024h, 026h, 028h, 02Ah (Chan.1-4)
Type: unsigned integer word
Range: 0 to 65535
Read/Write: R
Initialized Value: 0

This register contains the number of words to be received.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
NUM WORDS RX BUFFER	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Protocol

Address: 030h, 032h, 034h, 036h (Chan.1-4)
Type: unsigned integer word
Range: 0 to 5
Read/Write: W
Initialized Value: 0, Asynchronous

This register is used to configure the associated channel for either asynchronous, mono-synchronous, bi-synchronous, or HDLC, PPP-asynchronous, Extended Transparent communications mode.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
PROTOCOL	0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**0**	**0**	ASYNC
	0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**0**	**1**	MONO-SYNC
	0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**1**	**0**	BI-SYNC
	0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**1**	**1**	HDLC
	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	**0**	**0**	PPP-ASYNC
	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	**0**	**1**	EXTENDED TRANSPARENT

Clock Mode

Address: 03Ch, 03Eh, 040h, 042h (Chan.1-4)
Type: unsigned integer word
Range: 0 to 5
Read/Write: W
Initialized Value: 0

This register configures for internal or external transmit/receive clocks. To transmit or output clock signal on channel clock pin, program TXCLK VISIBLE (0x8000).

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
CLOCK MODE	0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**0**	**0**	TX-INTERNAL , RX-INTERNAL
	0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**0**	**1**	TX-CLKA , RX-INTERNAL
	0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**1**	**0**	TX-INTERNAL , RX-CLKB
	0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**1**	**1**	TX-CLKA , RX-CLKA
	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	**0**	**0**	TX-CLKB , RX-CLKB
	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	**0**	**1**	TX-CLKA , RX-CLKB
	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TX-CLK VISIBLE

Interface Levels

Address: 048h, 04Ah, 04Ch, 04Eh (Chan.1-4)
Type: unsigned integer word
Range: 0 to 4
Read/Write: W
Initialized Value: 5

This register is used to configure the interface level (RS232, RS422, RS485, Loop Back, or Tri-State) for the associated channel. Loop Back selection connects the channel's transmit and receive line internally. To implement, user must send data and look at Receive FIFO to verify that the sent data. Loop Back is usually used for test.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
INTERFACE LEVELS	0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**0**	**0**	RS232
	0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**0**	**1**	RESERVED
	0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**1**	**0**	RS422
	0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**1**	**1**	RS485
	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	**0**	**0**	MANUAL LOOP BACK
	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	**0**	**1**	TRI-STATE

Tx-Rx Configuration Low

Address: 054h, 058h, 05Ch, 060h (Chan.1-4)
Type: binary word
Range: not applicable
Read/Write: R/W
Initialized Value: 0

This register is used to set the transmit/receive configuration for the associated channel. Functions depend upon programmed protocol (see *Protocol Register*).

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Tx-Rx CONFIG LO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	"1" = RTS/CTS FLOW CONTROL
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	"1" = DTR/DSR FLOW CONTROL
	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	"1" = AUTO TRANSMIT MODE ENABLED
	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	RTS FUNCTION "0" = WATERMARK "1" = TxDATA AVAIL
	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	"1" = CARRIER DETECT FLOW CONTROL
	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	CARRIER DETECT PIN POLARITY "1" = ACTIVE LOW "0" = ACTIVE HIGH
	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	"1" = ADDRESS RECOGNITION (HDLC ONLY)
	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	ADDRESS LENGTH (HDLC ONLY) "1" = 16 "0" = 8 BITS
	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	"1" = HIGH BYTE RECOGNITION (HDLC ONLY)
	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	ADDRESS AS DATA (HDLC ONLY) "0" = STRIPPED "1" = KEPT
	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	SYNC CHAR LENGTH "0" = (6) MONO,(12) Bi-Sync "1" = (8)MONO,(16) Bi-Sync
	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	SYNC CHAR AS DATA "0" = STRIPPED "1" = KEPT
	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	"1" = TERMINATION CHAR DETECTION
	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	"1" = XON/XOFF FLOW CONTROL
	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	XON/XOFF CHAR AS DATA "0" = STRIPPED "1" = KEPT
	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	"1" = TIME OUT DETECTION

Tx-Rx Configuration High

Address: 056h, 05Ah, 05Eh, 062h (Chan.1-4)
Type: binary word
Range: not applicable
Read/Write: R/W
Initialized Value: 0

This register is used to configure CRC function and OPEN and IDLE flags. In HDLC mode, error protection is done by CRC generation and checking. The frame sequence at the end of each frame consisted of two or four bytes of CRC checksum. 32-bit or CCITT algorithms can be selected.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Tx-Rx CONFIG HI	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	CRC RESET VALUE (HDLC ONLY) "1" = 0000 or 00000000 "0" = FFFF or FFFFFFFF
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	CRC SELECT HDLC : "1" = 32BIT CRC "0" = 16BIT CRC-CCITT SYNC : 1" = 16BIT CRC-CCITT "0" = 16BIT CRC
	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	"1" = APPEND CRC TO TxDATA
	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	RxCRC AS DATA (HDLC ONLY) "0" = STRIPPED "1" = KEPT
	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	"1" = SHARED FLAGS TRANSMISSION (HDLC ONLY)
	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	"1" = IDLE FLAGS TRANSMISSION
	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	DATA INVERSION "0" = NORMAL "1" = INVERTED

Channel Control Low

Address: 06Ch, 070h, 074h, 078h (Chan.1-4)
Type: binary word
Range: not applicable
Read/Write: R/W
Initialized Value: 0

This register is used to for channel control configuration.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
CONTROL LO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	RTS/GPIO 1[1]
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	CTS/GPIO 2[1]
	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	DTR/GPIO 3[1]
	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	DSR/GPIO 4[1]
	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	DCD/GPIO 5[1]
	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	Tx INITIATE[2]
	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	Tx ALWAYS (ASYNC ONLY)
	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	RESERVED
	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	TRISTATE TRANSMIT LINE
	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	ENABLE RECEIVER
	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	SET/RELEASE BREAK
	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	ENTER HUNT MODE
	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	TIMEOUT ENABLE
	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	RESET CHANNEL FIFOs & UART[2]
	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLEAR Rx FIFO[2]
	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CLEAR Tx FIFO[2]

Notes: 1. Disable D0 through D4 to enter GPIO control.
RTS/CTS as GPIO when RTS/CTS Flow Control disabled.
DTR/DSR as GPIO when DTR/DSR Flow Control disabled.
2. Firmware will clear bit when done.

Channel Control High

Address: 06Eh, 072h, 076h, 07Ah (Chan.1-4)
Type: binary word
Range: not applicable
Read/Write: R/W
Initialized Value: 0

This register is reserved for future use.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
CONTROL HI	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	

Data Configuration

Address: 084h, 086h, 088h, 08Ah (Chan.1-4)
Type: binary word
Range: not applicable
Read/Write: R/W
Initialized Value: 0000 0000 0101 0011 binary (53h)

This register is used for channel data configuration.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
DATA CONFIG	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**0**	8 DATA BITS
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0**	**1**	7 DATA BITS
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	**0**	6 DATA BITS
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	**1**	5 DATA BITS
	0	0	0	0	0	0	0	0	0	0	0	**0**	**0**	**0**	0	0	NO PARITY
	0	0	0	0	0	0	0	0	0	0	0	**0**	**0**	**1**	0	0	SPACE PARITY
	0	0	0	0	0	0	0	0	0	0	0	**0**	**1**	**1**	0	0	ODD PARITY
	0	0	0	0	0	0	0	0	0	0	0	**1**	**0**	**1**	0	0	EVEN PARITY
	0	0	0	0	0	0	0	0	0	0	0	**1**	**1**	**1**	0	0	MARK PARITY
	0	0	0	0	0	0	0	0	0	**0**	**0**	0	0	0	0	0	1 STOP BIT
	0	0	0	0	0	0	0	0	0	**0**	**1**	0	0	0	0	0	2 STOP BITS
	0	0	0	0	0	0	**0**	**0**	**1**	0	0	0	0	0	0	0	NRZ DATA ENCODING
	0	0	0	0	0	0	**0**	**1**	**0**	0	0	0	0	0	0	0	NRZI DATA ENCODING
	0	0	0	0	0	0	**1**	**0**	**0**	0	0	0	0	0	0	0	FM0 DATA ENCODING
	0	0	0	0	0	0	**1**	**0**	**1**	0	0	0	0	0	0	0	FM1 DATA ENCODING
	0	0	0	0	0	0	**1**	**1**	**0**	0	0	0	0	0	0	0	MANCHESTER DATA ENCODING

Baud Rate

Baud Rate High + Low Address: 092+090h, 096+094h, 09A+098h, 09B+09Ch (Chan.1-4)
Type: 24-bit unsigned integer
Range: 300 to 8Mbps, Baud Rate High & Low Registers combined
Read/Write: R/W
Initialized Value: 9600 Baud

Both the *Baud Rate High Register* and *Baud Rate Low Register* combined together determine the communications baud rate. Enter desired baud (bit) rate directly as 24-bit unsigned integer. Use external clock to transmit data as low as necessary (ex 2Hz).

BAUD RATE HIGH REGISTER																BAUD RATE LOW REGISTER													
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
300 Baud = 00 012C hex								0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0
9600 Baud = 00 2580 hex								0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	0	0	0	0
4000000 Baud = 3D 0900 hex								0	0	1	1	1	1	0	1	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0

Asynchronous and synchronous (internal clock) Bit Rate Generation limitation(s):

Bit rate generation is based on a primary clock divided by an integer value.
Programmed bit versus actual bit rate will have greater resolution at lower bit rates (<115 KHz). When specifying internal clock, the card generates and transmits the actual bit rate as close (rounding off) to the programmed bit rate based on the following formula:

Actual bit rates available: 25 MHz / N (synchronous)
1.5625 MHz / N (asynchronous)
(N = integer)

Asynchronous examples:

Programmed Bit Rate (b/s)	(Integer Divisor)	Actual Bit Rate
381 (minimum)	4096	381.5
600	2604	600
2400	651	2400
9600	163	9586
57600	27	57870
115200	14	111607
300000	5	312500
600000	3	520883
800000 (maximum)	2	781250

Note: Bit generation formulas may differ between product models.

Preamble

Address: 0A8h, 0AAh, 0ACh, 0AEh (Chan.1-4)
Type: binary word
Range: High word 80h, A0h, C0h, or E0h; Low word 00h to FFh
Read/Write: R/W
Initialized Value: 0
Modes Affected: HDLC, Bi-Sync

This register determines both the number of preambles and the preamble pattern sent out during preamble transmission. The high byte decodes 1, 2, 4 or 8 preambles. The low byte describes the preamble pattern. Preamble transmission applies to both the HDLC and Sync modes. In HDLC-mode, zero-bit insertion is disabled during preamble transmission.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
PREAMBLE	1	0	0	0	0	0	0	0	D	D	D	D	D	D	D	D	1 PREAMBLE (VALUE 0xNN)
	1	0	1	0	0	0	0	0	D	D	D	D	D	D	D	D	2 PREAMBLES (VALUE 0xNN)
	1	1	0	0	0	0	0	0	D	D	D	D	D	D	D	D	4 PREAMBLES (VALUE 0xNN)
	1	1	1	0	0	0	0	0	D	D	D	D	D	D	D	D	8 PREAMBLES (VALUE 0xNN)

Tx Buffer Almost Empty

Address: 0B4h, 0B6h, 0B8h, 0BAh (Chan.1-4)
Type: unsigned integer
Range: 0 to 65535
Read/Write: R/W
Initialized Value: 100 decimal (64h)

This register specifies the minimum size, in bytes, of the transmit buffer before the TxFIFO Almost Empty Status bit D1 in the FIFO Status register is flagged (High True). If the interrupt is enabled (see Interrupt Enable register), a VME interrupt will be generated.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Tx BUFFER AE VALUE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Rx Buffer Almost Full

Address: 0C0h, 0C2h, 0C4h, 0C6h (Chan.1-4)
Type: unsigned integer
Range: 0 to 65535
Read/Write: R/W
Initialized Value: 65435 (0xFF9B)

This register specifies the maximum size, in bytes, of the receive buffer before the RxFIFO Almost Full Status bit D0 in the FIFO Status register is flagged (High True). If the interrupt is enabled (see Interrupt Enable register), a VME interrupt will be generated.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
Rx BUFFER AF VALUE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Rx Buffer High Watermark

Address: 0CCh, 0CEh, 0D0h, 0D2h (Chan.1-4)
Type: binary word
Range: *Low Watermark* < *High Watermark* < 65535
Read/Write: R/W
Initialized Value: 64535 decimal (FC17h)

This register defines the *Receive Buffer High Watermark* value. When Rx Buffer size equals the High Watermark value, FIFO Status bit D3 is flagged and;

If XON/XOFF is enabled, XOFF is sent, **and/or**
If RTS/CTS is enabled, RTS goes inactive.

The Watermark registers are used for XON/XOFF and/or RTS/CTS flow control. The *Receive Buffer High Watermark* register value controls when the XOFF character is sent when using software flow control and controls when the RTS signal would be negated when using hardware flow control. For software flow control operation, the XOFF character would be sent once when the number of bytes in the RX FIFO equals the value in the *Receive Buffer High Watermark* register. Once the XOFF has been sent, it cannot be sent again until the XON character has been sent. The valid state transitions to sending the XOFF character can be either no previous XON/XOFF character sent or a previous XON character sent. There is also a *High Watermark Reached* interrupt enable/disable bit in the Interrupt Enable Register and a *High Watermark Reached* bit in the ISR, (Interrupt Status Register). When the *High Watermark Reached*, and interrupt request will be generated.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
HI WATERMARK VALUE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Rx Buffer Low Watermark

Address: 0D8h, 0DAh, 0DCh, 0DEh (Chan.1-4)
Type: binary word
Range: 0 < *Low Watermark* < *High Watermark* < 65535
Read/Write: R/W
Initialized Value: 1000 decimal (3E8h)

This register defines the *Receive Buffer Low Watermark* value. When the Rx Buffer size is less than the Low Watermark value, FIFO Status bit D3 is flagged and;

If XON/XOFF is enabled, XON is sent, **and/or**
If RTS/CTS is enabled, RTS goes active.

The Watermark registers are used for XON/XOFF and/or RTS/CTS flow control. The *Receive Buffer Low Watermark* register value controls when the XON character is sent when using software flow control and controls when the RTS signal would be asserted when using hardware flow control. For software flow control operation, the XON character would be sent once when the number of bytes in the Rx FIFO equals the value in the *Receive Buffer Low Watermark* register AND an XOFF character has be sent prior to this XON character. The valid state transition to sending the XON character can only be from the state of a previous XOFF character that has been sent. There is a *Low Watermark Reached* interrupt enable/disable bit in the Interrupt Enable Register and a *Low Watermark Reached* bit in the ISR, (Interrupt Status Register). When the *Low Watermark Reached*, an interrupt request will be generated.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
LO WATERMARK VALUE	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

HDLC Address/Sync Character

Address: 0E4h, 0E6h, 0E8h, 0EAh (Chan.1-4)
Type: unsigned character word
Range: not applicable
Read/Write: R/W
Initialized Value: A5h
Modes Affected: HDLC and Synchronous

This register is mode dependant. If using HDLC mode, this value is compared to the address is received message and if it's equal, the message is stored in the receive buffer. If using Mono/Bi-Synchronous mode, this value is considered the "Sync Character" and is used for communication synchronization. The receiver searches incoming data for the Sync Character, once found, communication is synchronized and additional data is valid.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
HDLC/SYNC CHAR	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

Termination Character

Address: 0F0h, 0F2h, 0F4h, 0F6h (Chan.1-4)
Type: unsigned character (usually a member of the ASCII data set)
Range: not applicable
Read/Write: R/W
Initialized Value: 3h
Modes Affected: Async and Bi-Sync

This register contains the termination character used for termination detection. When using the Asynchronous or Bi-Synchronous modes, the receive data stream is monitored for the occurrence of the termination character. When this character is detected, an interrupt (unless masked,) is generated.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
TERMINATION CHAR	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

XON Character

Address: 0FCh, 0FEh, 100h, 102h (Chan.1-4)
Type: unsigned character (usually a member of the ASCII data set)
Range: not applicable
Read/Write: R/W
Initialized Value: 11h
Modes Affected: Async

This register bit field specifies the XON character for in-band flow control in Async mode.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
XON CHAR	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

XOFF Character

Address: 108h, 10Ah, 10Ch, 10Eh (Chan.1-4)
Type: unsigned character (usually a member of the ASCII data set)
Range: not applicable
Read/Write: R/W
Initialized Value: 13h
Modes Affected: Async

This register bit field specifies the XOFF character for in-band flow control in Async mode.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
XOFF CHAR	X	X	X	X	X	X	X	X	D	D	D	D	D	D	D	D	D=DATA BIT

FIFO Status

Address: 114h, 116h, 118h, 11Ah (Chan.1-4)
Type: binary word
Range: not applicable
Read/Write: R
Initialized Value: not applicable

This register describes current FIFO Status. See Rx Almost Full, Tx Almost Empty, Rx High Watermark and Rx Low Watermark specific registers for function description and programming.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
FIFO STATUS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	RxFIFO ALMOST FULL
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	TxFIFO ALMOST EMPTY
	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	HIGH WATERMARK REACHED
	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	LOW WATERMARK REACHED
	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	Rx EMPTY
	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	Tx FULL

Time Out Value

Address: 120h, 122h, 124h, 126h (Chan.1-4)
Type: unsigned integer
Range: 0 to 65535
Read/Write: R/W
Initialized Value: 9C40h (1 second)
Modes Affected: Async

This register bit field determines the time out period. If there is no receive line activity for the configured period of time, a time out is indicated in the Interrupt Status Register, bit D10. Lsb is 25µs.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
TIME OUT VALUE	D	D	D	D	D	D	D	D	D	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Interrupt Enable

Address: 180h, 182h, 184h, 186h (Chan.1-4)
Type: binary word
Range: not applicable
Read/Write: R/W
Initialized Value: not applicable

This register provides for Interrupt Enabling. Set bit high True to enable interrupts. Status will still be reported in status registers. See specific registers for function description and programming

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
INTERRUPT ENABLE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	PARITY ERROR
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	Rx BUFFER ALMOST FULL
	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	CRC ERROR (sync & hdlc only)
	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	Rx COMPLETE / ETX RECEIVED
	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	Rx DATA AVAILABLE
	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	Rx OVERRUN
	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	HIGH WATERMARK REACHED
	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	LOW WATERMARK REACHED
	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	Tx BUFFER ALMOST EMPTY
	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	Tx COMPLETE
	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	TIME OUT OCCURRED
	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	BREAK / ABORT
	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	SYNC CHAR DETECTED
	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	N/A
	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	N/A
	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	N/A

Interrupt Status

Address: 18Ch, 18Eh, 190h, 192h (Chan.1-4)
Type: binary word
Range: not applicable
Read/Write: R/W
Initialized Value: not applicable

This register describes the status of 13 different events. These events are latched and not cleared until read by the host. See specific registers for function description and programming

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
INTERRUPT STATUS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	PARITY ERROR
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	Rx BUFFER ALMOST FULL
	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	CRC ERROR (sync & hdlc only)
	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	Rx COMPLETE / ETX RECEIVED
	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	Rx DATA AVAILABLE
	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	Rx OVERRUN
	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	HIGH WATERMARK REACHED
	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	LOW WATERMARK REACHED
	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	Tx BUFFER ALMOST EMPTY
	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	Tx COMPLETE
	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	TIME OUT OCCURRED
	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	BREAK / ABORT
	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	SYNC CHAR DETECTED
	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	N/A
	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	N/A
	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	N/A

Interrupt Vector

Address: 198h, 19Ah, 19Ch, 19Eh (Chan.1-4)
Type: unsigned character
Range: not applicable
Read/Write: R/W
Initialized Value: not applicable

This register contains the interrupt vector, or address to the interrupt service routine.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
INTERRUPT VECTOR	X	X	X	X	X	X	X	X	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT

Channel Status

Address: 1A4h, 1A6h, 1A8h, 1AAh (Chan. 1-4)
Type: binary word
Range: not applicable
Read/Write: R/W
Initialized Value: not applicable

This register describes the status of 13 different events. These events are NOT latched. They are dynamic. Use this register to read current or real-time status. See specific registers for function description and programming

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
CHANNEL STATUS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	PARITY ERROR
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	Rx BUFFER ALMOST FULL
	0	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	CRC ERROR (sync & hdlc only)
	0	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	Rx COMPLETE / ETX RECEIVED
	0	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	Rx DATA AVAILABLE
	0	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	Rx OVERRUN
	0	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	HIGH WATERMARK REACHED
	0	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	LOW WATERMARK REACHED
	0	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	Tx BUFFER ALMOST EMPTY
	0	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	Tx COMPLETE
	0	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	TIME OUT OCCURRED
	0	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	BREAK / ABORT
	0	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	SYNC CHAR DETECTED
	0	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	N/A
	0	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	N/A
	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	N/A

Module ID

Address: 1F8h
Type: ASCII character (in each upper and lower byte)
Range: 0 to 65535
Read/Write: R
Initialized Value: 5031h

Read register to determine Module ID “P1” in ASCII. Find ASCII “P” in upper byte and ASCII “1” in lower byte, together 5031h.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE ID	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	**D**	D=DATA BIT
	ASCII “P”								**ASCII “1”**								

FPGA Version

Address: 1FCh
Type: unsigned integer word
Range: 0 to 65535
Read/Write: R
Initialized Value: not applicable

This register contains the FPGA version number.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
FPGA VERSION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

DSP Version

Address: 1FEh
Type: unsigned integer word
Range: 0 to 65535
Read/Write: R
Initialized Value: not applicable

This register contains the DSP firmware version number.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
DSP VERSION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT

GENERAL USE MEMORY MAP

7D8	Platform	R	7EA	Watchdog Timer	R/W
7DA	Model	R	7EC	Soft Reset	W
7DC	Generation	R	7EE	Part Number	R
7DE	Special Spec	R	7F0	Serial Number	R
7E0	Interrupt Level	R/W	7F2	Date Code	R
7E2	Test Enable	R/W	7F4	Rev Level PCB	R
7E4	Module Test Status	R	7F6	Rev Level Master FPGA	R
7E6	Module Test Status	R	7F8	Rev Level Master DSP	R
7E8	Module Test Status	R	7FA	Board Ready	R

GENERAL USE REGISTER DEFINITIONS

Platform

Address: 7D8h
Type: ASCII character (in each upper and lower byte)
Range: not applicable
Read/Write: R
Initialized Value: 3624h

The register holds the VME platform code "64" in ASCII. ASCII "6" is in upper byte and ASCII "4" is in lower byte.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
PLATFORM	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "6"								ASCII "4"								

Model

Address: 7DAh
Type: ASCII character (in each upper and lower byte)
Range: not applicable
Read/Write: R
Initialized Value: 5253h

This register holds product model code "RS" in ASCII. ASCII "R" is in upper byte and ASCII "S" is in lower byte.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODEL	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII "R"								ASCII "S"								

Generation

Address: 7DCh
Type: ASCII character (in each upper and lower byte)
Range: not applicable
Read/Write: R
Initialized Value: 2032h

This register holds product generation code "2" in ASCII. ASCII "space" is in upper byte and ASCII "2" is in lower byte.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
GENERATION	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII " "								ASCII "2"								

Special Spec

Address: 7DEh
Type: ASCII character (in each upper and lower byte)
Range: not applicable
Read/Write: R
Initialized Value: 2020h

This register holds product special code in ASCII. ASCII "spaces" are used for none where ASCII "space is in upper byte and ASCII "space" is in lower byte.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
SPECIAL SPEC	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D=DATA BIT
	ASCII " "								ASCII " "								

Interrupt Level

Address: 7E0h
Type: unsigned integer
Range: 0 to 7
Read/Write: R
Initialized Value: 0h

This register is used to define the Interrupt Priority Level. Enter 0 to disable interrupts. Enter in priority level 0 through 7 otherwise.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
FPGA VERSION	X	X	X	X	X	X	X	X	X	X	X	X	X	D	D	D	D=DATA BIT

Test Enable

Address: 7E2h
Type: binary word
Range: not applicable
Read/Write: R
Initialized Value: 0h

This register is used to enable the Loopback Test D0. The D0 test transmits 65580 characters from each channel FIFO buffer which is looped it back to the receive FIFO buffer where it is checked for validity. Test checks and verifies internal hardware for proper operation. Card implements D0 as Power-On-Self-Test or (POST). POST cannot be disabled.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
TEST ENABLE	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	D0	D=DATA BIT

Module Test Status

Address: 7E4h, 7E6h, 7E8h
Type: binary word
Range: 0000h to FFFFh
Read/Write: R
Initialized Value: not applicable

This register reports the D0 Loopback Test Status for each module channel. D0 reports status for channel 1, D1 for channel 2, etc. Channel Status Data bit (Chn, where n is 1, 2, 3, 4, 5 or 6) is fail, high true, and indicates channel is not operating spec compliant. Status is latched. Status is unlatched when read.

REGISTER	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
MODULE TEST STATUS	X	X	X	X	X	X	X	X	X	X	X	X	Ch4	Ch3	Ch2	Ch1	MODULE CHANNEL STATUS BIT

Watchdog Timer

Address: 7EAh
Type: binary word
Range: not applicable
Read/Write: R
Initialized Value: 0h

This register implements a *Watchdog timer*. When it detects that a value, or word, has been written to it, that word will be inverted within 50 µSec. The inverted word remains until replaced by a new word. User, after 50 µSec. looks for the inverted word to confirm that the processor is operating.

Soft Reset

Address: 7ECh
Type: unsigned integer
Range: 0 to 1
Read/Write: R
Initialized Value: 0

Level sensitive. Writing a "1" initiates and holds software in reset state. Then, writing "0" initiates reboot (depending upon configuration, takes up to 10 seconds). This function is equivalent to a power-on reset.

Part Number

Address: 7EEh
Type: unsigned integer word
Range: 0000h to FFFFh
Read/Write: R
Initialized Value: not applicable

This register contains the product part number. A unique 16-bit code is assigned to each part number.

Serial Number

Address: 7F0h
Type: unsigned integer word
Range: 0000h to FFFFh
Read/Write: R
Initialized Value: not applicable

This register contains the board serial number.

Date Code

Address: 7F2h
Type: unsigned integer word
Range: 0000h to FFFFh
Read/Write: R
Initialized Value: not applicable

This register contains the date of manufacture. It is read as a four digit decimal number, where four digits represent YYWW (Year, Year, Week, Week). For example, 0126 converts to the 26th week of 2001.

Revision Level, PCB

Address: 7F4h
Type: unsigned integer word
Range: not applicable
Read/Write: R
Initialized Value: not applicable

This register contains the PCB revision level.

Revision Level, Master FPGA

Address: 7F6h
Type: unsigned integer word
Range: not applicable
Read/Write: R
Initialized Value: not applicable

This register contains the Master FPGA firmware revision level.

Revision Level, Master DSP

Address: 7F8h
Type: unsigned integer word
Range: not applicable
Read/Write: R
Initialized Value: not applicable

This register contains the Master DSP firmware revision level.

Board Ready

Address: 7FAh
Type: binary word
Range: not applicable
Read/Write: R
Initialized Value: not applicable

This register can be polled to determine if the card is ready for configuration or any register read or write access. When board initialization is completed after as much as 10 seconds, the board is ready for access and the *Board Ready* register is set to AA55h.

GLOSSARY

CTS
Clear to Send

CTS/RTS
If enabled, the operation of these bits is automatic. Both CTS/RTS & DTR/DSR can be enabled at the same time. If CTS/RTS is disabled, CTS & RTS can be used as I/O ports.

DCD
Data Carrier Detect

DCD/DTR
If enabled, operation is automatic. Both CTS/RTS & DSR/DTR can be enabled at the same time.

DSR
Data Set Ready

DTR
Data Terminal Ready

RS232
– is output; + is not used

RS422
+ is non-inverted; – is inverted and is internally terminated with 120Ω.

RS485
+ is non-inverted; – is inverted. No internal termination. Generally used for multi-drop (Party) lines, and terminated at far end.

Full duplex (4 wire)
Use RXD & TXD

Half-duplex (2 wire)
Use RXD+ tied to TXD+ and RXD- tied to RXD-

RTS
Request to Send

RXD
Receive Data.

TXD
Transmit Data (The transmit word is 8 bits)

SERIAL COMMUNICATIONS SPECIFICATIONS

Serial Communications Specifications	RS232	RS422	RS485
Mode of Operation	Single Ended	Differential	Differential
Total Number of Drivers and Receivers on One Line	1 Driver 1 Receiver	1 Driver 1 Receiver	1 Driver 32 Receiver
Maximum Data Rate	120 kb/s	10Mb/s	10Mb/s
Driver Output Signal Level (Min Loaded)	±5V @3kΩ load	±2.0V@100Ω load	±1.5V@54Ω load
Driver Load Impedance (Ohms)	3k min	100	54
Max Driver Current in High Z State (Power On)	N/A	N/A	±100uA
Max Driver Current in High Z State (Power Off)	±6mA@±2V	±100uA	±100uA
Receiver Input Voltage Range	±15V	-10V to +10V	-7V to +12V
Receiver Input Sensitivity	±3V	±200mV	±200mV
Receiver Input Resistance (Ohms)	3k to 7k	120	10k

FACTORY DEFAULTS:

Address recognition:	Off
Baud rate:	9600
CTS/RTS:	Disabled
Clock select:	Internal
DCD/DTR:	Disabled
HDLC/SDLC address (sync char):	0x00A5
Interrupt level:	0
Interrupt vector	0x00
Lower limit:	100
Mode:	Tri-State, Asynchronous
Number of data bits:	8
Parity:	Disabled
Receivers:	Enabled
RX buffer, almost full:	65435
Stop bits:	1
TX buffer, almost empty:	100
Upper limit:	64535
XON:	0x11
XOFF:	0x13
XON/XOFF:	Disabled

Note: See function descriptions for specific default values

CONNECTORS

Front panel Connectors J1, J2 & J3

J1: AMP 748483-5 Mate: AMP 748368-1

Pin		Pin		Pin		Pin		Pin		Pin		Pin	
1	Chassis	13	CTS 02+	25	DSR 04+	37	CTS 01-	49	CLKA I/O03+	61	DTR 04-	73	CLKAI/O02-
2	DCD 04+	14	TXD 02+	26	DCD 03-	38	TXD 01-	50	DSR 02-	62	CLKB IN 04-	74	Ground
3	CTS 04+	15	RXD 02+	27	CTS 03-	39	RXD 01-	51	RTS 02+	63	CLKA I/O04-	75	RTS 01-
4	TXD 04+	16	DSR 01+	28	TXD 03-	40	Chassis	52	DTR 02+	64	DSR 04-	76	DTR 01-
5	RXD 04+	17	DCD 01+	29	RXD 03-	41	RTS 04+	53	CLKB IN 02+	65	RTS 03-	77	CLKBIN 01-
6	DSR 03+	18	CTS 01+	30	Ground	42	DTR 04+	54	CLKA I/O02+	66	DTR 03-	78	CLKAI/O01-
7	DCD 03+	19	TXD 01+	31	DCD 02-	43	CLKBIN04+	55	DSR 01-	67	CLKB IN 03-		
8	CTS 03+	20	RXD 01+	32	CTS 02-	44	CLKAI/O04+	56	RTS 01+	68	CLKA I/O03-		
9	TXD 03+	21	DCD 04-	33	TXD 02-	45	DSR 03-	57	DTR 01+	69	Ground		
10	RXD 03+	22	CTS 04-	34	RXD 02-	46	RTS 03+	58	CLKB IN 01+	70	RTS 02-		
11	DSR 02+	23	TXD 04-	35	Ground	47	DTR 03+	59	CLKA I/O01+	71	DTR 02-		
12	DCD 02+	24	RXD 04-	36	DCD 01-	48	CLKBIN 3+	60	RTS 04-	72	CLKB IN 02-		

J2: AMP 748483-5 Mate: AMP 748368-1

Pin		Pin		Pin		Pin		Pin		Pin		Pin	
1	Chassis	13	CTS 06+	25	DSR 08+	37	CTS 05-	49	CLKA I/O07+	61	DTR 08-	73	CLKAI/O06-
2	DCD 08+	14	TXD 06+	26	DCD 07-	38	TXD 05-	50	DSR 06-	62	CLKB IN 08-	74	Ground
3	CTS 08+	15	RXD 06+	27	CTS 07-	39	RXD 05-	51	RTS 06+	63	CLKA I/O08-	75	RTS 05-
4	TXD 08+	16	DSR 05+	28	TXD 07-	40	Chassis	52	DTR 06+	64	DSR 08-	76	DTR 05-
5	RXD 08+	17	DCD 05+	29	RXD 07-	41	RTS 08+	53	CLKB IN 06+	65	RTS 07-	77	CLKBIN 05-
6	DSR 07+	18	CTS 05+	30	Ground	42	DTR 08+	54	CLKA I/O06+	66	DTR 07-	78	CLKAI/O05-
7	DCD 07+	19	TXD 05+	31	DCD 06-	43	CLKBIN 08+	55	DSR 05-	67	CLKB IN 07-		
8	CTS 07+	20	RXD 05+	32	CTS 06-	44	CLKAI/O 08+	56	RTS 05+	68	CLKA I/O07-		
9	TXD 07+	21	DCD 08-	33	TXD 06-	45	DSR 07-	57	DTR 05+	69	Ground		
10	RXD 07+	22	CTS 08-	34	RXD 06-	46	RTS 07+	58	CLKB IN 05+	70	RTS 06-		
11	DSR 06+	23	TXD 08-	35	Ground	47	DTR 07+	59	CLKA I/O05+	71	DTR 06-		
12	DCD 06+	24	RXD 08-	36	DCD 05-	48	CLKBIN 07+	60	RTS 08-	72	CLKB IN 06-		

J3: AMP 748483-5 Mate: AMP 748368-1

Pin		Pin		Pin		Pin		Pin		Pin		Pin	
1	Chassis	13	CTS 10+	25	DSR 12+	37	CTS 09-	49	CLKAI/O 11+	61	DTR 12-	73	CLKA I/O 10-
2	DCD 12+	14	TXD 10+	26	DCD 11-	38	TXD 09-	50	DSR 10-	62	CLKB IN 12-	74	Ground
3	CTS 12+	15	RXD 10+	27	CTS 11-	39	RXD 09-	51	RTS 10+	63	CLKA I/O 12-	75	RTS 09-
4	TXD 12+	16	DSR 09+	28	TXD 11-	40	Chassis	52	DTR 10+	64	DSR 12-	76	DTR 09-
5	RXD 12+	17	DCD 09+	29	RXD 11-	41	RTS 12+	53	CLKB IN 10+	65	RTS 11 -	77	CLKB IN 09-
6	DSR 11+	18	CTS 09+	30	Ground	42	DTR 12+	54	CLKA I/O 10+	66	DTR 11-	78	CLKA I/O 09-
7	DCD 11+	19	TXD 09+	31	DCD 10-	43	CLKB IN	55	DSR 09-	67	CLKB IN 11-		
8	CTS 11+	20	RXD 09+	32	CTS 10-	44	CLKA I/O	56	RTS 09+	68	CLKA I/O 11-		
9	TXD 11+	21	DCD 12-	33	TXD 10-	45	DSR 11-	57	DTR 09+	69	Ground		
10	RXD 11+	22	CTS 12-	34	RXD 10-	46	RTS 11+	58	CLKB IN 09+	70	RTS 10-		
11	DSR 10+	23	TXD 12-	35	Ground	47	DTR 11+	59	CLKA I/O 09+	71	DTR 10-		
12	DCD 10+	24	RXD 12-	36	DCD 09-	48	CLKB IN 11+	60	RTS 12-	72	CLKB IN 10-		

Rear Panel Connectors P2 & P0

P2 Connector: 160 pin DIN connector

Pin		Pin		Pin		Pin		Pin		Pin		Pin	
1a	RXD 01+	15a	CTS 02+	31a	TXD 03+	11c	DTR 04+	21c	RXD 06+	30c	RTS 07+	17z	DTR 08+
2a	RXD 01-	16a	CTS 02-	32a	TXD 03-	11d	DTR 04-	21d	RXD 06-	30d	RTS 07-	19z	DTR 08-
3a	CTS 01+	17a	DCD 02+	1c	RTS 03+	13c	CTS 05+	22c	DCD 06+	31c	TXD 07+	21z	CLKAI/O1 +
4a	CTS 01-	18a	DCD 02-	2c	RTS 03-	13d	CTS 05-	22d	DCD 06-	31z	TXD 07-	23z	CLKAI/O1 -
5a	DCD 01+	19a	TXD 02+	3c	DTR 03+	14c	RXD 05+	23c	RTS 06+	32c	DTR 07+	25z	CLKAI/O2 +
6a	DCD 01-	20a	TXD 02-	4c	DTR 03-	14d	RXD 05-	23d	RTS 06-	29z	DTR 07-	27z	CLKAI/O2 -
7a	TXD 01+	21a	RTS 02+	6c	CTS 04+	15c	DCD 05+	24c	TXD 06+	3d	RXD 08+	5c	CLKAI/O3 +
8a	TXD 01-	22a	RTS 02-	6d	CTS 04-	15d	DCD 05-	24d	TXD 06-	4d	RXD 08-	5d	CLKAI/O3 -
9a	RTS 01+	23a	DTR 02+	7c	RXD 04+	16c	RTS 05+	25c	DTR 06+	1z	CTS 08+	12c	CLKAI/O4 +
10a	RTS 01-	24a	DTR 02-	7d	RXD 04-	16d	RTS 05-	25d	DTR 06-	3z	CTS 08-	12d	CLKAI/O4 -
11a	DTR 01+	25a	RXD 03+	8c	DCD 04+	17c	TXD 05+	27c	CTS 07+	5z	DCD 08+	19c	CLKAI/O5 +
12a	DTR 01-	26a	RXD 03-	8d	DCD 04-	17d	TXD 05-	27d	CTS 07-	7z	DCD 08-	19d	CLKAI/O5 -
1d	DSR 01+	27a	CTS 03+	9c	RTS 04+	18c	DTR 05+	28c	RXD 07+	9z	TXD 08+	26c	CLKAI/O6 +
2d	DSR 01-	28a	CTS 03-	9d	RTS 04-	18d	DTR 05-	28d	RXD 07-	11z	TXD 08-	26d	CLKAI/O6 -
13a	RXD 02+	29a	DCD 03+	10c	TXD 04+	20c	CTS 06+	29c	DCD 07+	13z	RTS 08+		
14a	RXD 02-	30a	DCD 03-	10d	TXD 04-	20d	CTS 06-	29d	DCD 07-	15z	RTS 08-		

P0 Connector

1e	DSR 02+	17e	CLKBIN 05 +	14d	RTS 09+	11c	RXD 11+	8b	DCD 12+	5a	CLKBIN 09 +
2e	DSR 02-	18e	CLKBIN 05 –	15d	RTS 09-	12c	RXD 11-	9b	DCD 12-	6a	CLKBIN 09 –
3e	DSR 03+	19e	CLKBIN 06 +	16d	DTR 09+	13c	CTS 11+	10b	TXD 12+	7a	CLKBIN 10 +
4e	DSR 03-	1d	CLKBIN 06 –	17d	DTR 09-	14c	CTS 11-	11b	TXD 12-	8a	CLKBIN 10 –
5e	CLKAI/O7+	2d	CLKBIN 07 +	18d	RXD 10+	15c	DCD 11+	12b	RTS 12+	9a	CLKBIN 11 +
6e	CLKAI/O7–	3d	CLKBIN 07 –	19d	RXD 10-	16c	DCD 11-	13b	RTS 12-	10a	CLKBIN 11 –
7e	CLKAI/O8 +	4d	CLKBIN 08 +	1c	CTS 10+	17c	TXD 11+	14b	DTR 12+	11a	CLKBIN 12 +
8e	CLKAI/O8 –	5d	CLKBIN 08 –	2c	CTS 10-	18c	TXD 11-	15b	DTR 12-	12a	CLKBIN 12 –
9e	CLKBIN 01 +	6d	RXD 09+	3c	DCD 10+	19c	RTS 11+	16b	CLKAI/O9+	13a	DSR 04+
10e	CLKBIN 01 –	7d	RXD 09-	4c	DCD 10-	1b	RTS 11-	17b	CLKAI/O9 -	14a	DSR 04-
11e	CLKBIN 02 +	8d	CTS 09+	5c	TXD 10+	2b	DTR 11+	18b	CLKAI/O10 +	15a	DSR 05+
12e	CLKBIN 02 –	9d	CTS 09-	6c	TXD 10-	3b	DTR 11-	19b	CLKAI/O10 -	16a	DSR 05-
13e	CLKBIN 03 +	10d	DCD 09+	7c	RTS 10+	4b	RXD 12+	1a	CLKAI/O11 +	17a	DSR 06+
14e	CLKBIN 03 –	11d	DCD 09-	8c	RTS 10-	5b	RXD 12-	2a	CLKAI/O11 -	18a	DSR 06-
15e	CLKBIN 04 +	12d	TXD 09+	9c	DTR 10+	6b	CTS 12+	3a	CLKAI/O12 +		
16e	CLKBIN 04 –	13d	TXD 09-	10c	DTR 10-	7b	CTS 12-	4a	CLKAI/O12-		

The board contains three green LED's (LED1, LED2 & LED3) that are for factory use only. LED2 & LED3 will be ON during normal operation.

Miniature test connector, JP1 is used to download programming data and JP4 is a ground. Do not interface to these two connectors unless factory instructed to be used for field modification.

PART NUMBER DESIGNATION

64RS2 - XX X X X X - XX

Number of Channels
12 = 12 channels
08 = 08 channels
04 = 04 channels

ENVIRONMENTAL
C = 0°C to +70°C
E = -40°C to +85°C
H = E With Removable Conformal Coating
K = C With Removable Conformal Coating

MECHANICAL
F = Front Panel I/O and P2 & P0 I/O
S = Front Panel I/O and P2 I/O (No P0)
P = P2 & P0 I/O only
G = P2 I/O only (No P0)
W = P With Wedgelocks
A = VME64 with Blank Front Panel and P2 & P0 I/O only
B = VME64 Front Panel unshielded***
with Front Panel, P2 & P0I/O
T = VME64 Front Panel unshielded***
with Front Panel & P2 I/O (No P0)
D = VME64 with Blank Front Panel,
Low profile extractors and P2 & P0I/O only

P0 CONNECTOR
1 = P0 Connector installed
2 = P0 Connector not installed

OPTIONS
0 = none
9 = custom (see separate spec)

SPECIAL OPTION CODE (OR LEAVE BLANK)

NOTE:
*** Unshielded to accommodate for mating 78 pin connector.

Revision Page

Revision	Description of Change	Engineer	Date
1	Initial Release	GS	7/2/02
1.1	Channel Status is reg 1A4-A. Desc: There is no requirement to set the “TX Initiate” bit after each byte where VME traffic and overhead can be simplified since only the actual data byte being transmitted needs be sent to the transmit buffer. Protocol has 5 options. Clock mode has 5 options.Rx Buffer Almost Full initialized value is 65435. Corrected Module Test Status reg – one for each module. Watchdog timer is 2x25=50us. Board is Ready in ~10s	GS	11/19/2
1.2	Added Special Option code to Part Number	GS	12/12/2
1.3	LSB is for Ch1 in Module Test Status Register	GS	1/23/03
1.4	Enter baud rate directly into Baud Rate Register	GS	02/11/03
1.5	Added TIME OUT ENABLE to Channel Control Lo Register. Moved AUTO TRANSMIT MODE ENABLE from Channel Control Low to Tx-Rx Configuration Low register	GS	7/1/3
1.6	The board contains three green LED’s (LED1, LED2 & LED3) that are for factory use only. LED2 & LED3 will be ON during normal operation. Edits Baud Rate Hi/Lo register programming	GS	1/23/4
1.7	FOR COMMERCIAL AND MILITARY APPLICATIONS. To transmit or output clock signal on channel clock pin, program TXCLK VISIBLE (0x8000).	GS	4/6/4
1.8	RS422 is terminated with 120ç. (not 10k)	GS	11/4/4
1.9	Timeout Value defaults to 1 second (9C40h)	GS	7/8/5
1.10	New Address	KL	04/24/07
2.0	Added clarification to internal clock bit rate generation and available bit rates. Clarified TxRx Config Low/High register bit actions. Corrected minor typos.	AS	01/03/08
2.1	Corrected Channel Status Register	SB/JG	12/12/08