cPCI-3510 Series

Performance 3U CompactPCI® PlusIO
Intel® Core™ i7/i5 Processor Blade

User's Manual

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Revision History

Revision	Release Date	Description of Change(s)
2.00	26/03/2014	Initial release
2.01	17/11/2014	Correct Block Diagram SATA device support

Preface

Disclaimer

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ADLINK is committed to fulfill its social responsibility to global environmental preservation through compliance with the European Union's Restriction of Hazardous Substances (RoHS) directive and Waste Electrical and Electronic Equipment (WEEE) directive. Environmental protection is a top priority for ADLINK. We have enforced measures to ensure that our products, manufacturing processes, components, and raw materials have as little impact on the environment as possible. When products are at their end of life, our customers are encouraged to dispose of them in accordance with the product disposal and/or recovery programs prescribed by their nation or company.

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Using this Manual

Audience and Scope

The cPCI-3510 User's Manual is intended for hardware technicians and systems operators with knowledge of installing, configuring and operating industrial grade single board computers.

Manual Organization

This manual is organized as follows:

Chapter 1, Introduction: Introduces the cPCI-3510, its features, block diagrams, and package contents.

Chapter 2, Specifications: Presents detailed specification information, power consumption, and technical drawings.

Chapter 3, Functional Description: Describes the cPCI-3510 main functions.

Chapter 4, Board Interfaces: Describes the cPCI-3510 board interfaces.

Chapter 5, Getting Started: Describes the installation of components to the cPCI-3510 and rear transition modules.

Chapter 6, Driver Installation: Provides information on how to install the cPCI-3510 device drivers under Windows 7.

Chapter 7, Watchdog Timer: Describes the watchdog timer of the cPCI-3510.

Chapter 8, BIOS Setup Utility: Describes basic navigation for the AMI EFI BIOS setup utility.

Chapter 9, IPMI User Guide: Provides information on the baseboard management controller (BMC) of the Intelligent Platform Management Interface (IPMI).

Important Safety Instructions: Presents safety instructions all users must follow for the proper setup, installation and usage of equipment and/or software.

Getting Service: Contact information for ADLINK's worldwide offices.

Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.


NOTE:

Additional information, aids, and tips that help users perform tasks.


CAUTION:

Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.


WARNING:

Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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Table of Contents

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List of Figures

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List of Tables

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1 Introduction

1.1 Overview

The ADLINK cPCI-3510 Series is a 3U CompactPCI® PlusIO compatible processor blade with soldered DDR3L-1600 ECC memory up to 8GB. The ADLINK cPCI-3510 features an Intel® Core™ i7 processor with Mobile Intel® QM87 Express Chipset.

The cPCI-3510 Series is a 3U CompactPCI blade available in single-slot (4HP), dual-slot (8HP) or triple-slot (12HP) width form factors with various daughter boards to provide a broad range of I/O requirements. Front panel I/O in the single-slot (4HP) version includes 1x DVI-I, 2x GbE and 1x USB 3.0 port (these I/O are common to all versions). Front panel I/O in the dual-slot (8HP) version includes additional 2x USB 2.0, 1x COM, 1x KB/MS and Line-in/Line-out on the cPCI-3510D or additional 2x DisplayPorts, 1x COM in RJ-45 connector, 1x KB/MS and 1x additional USB2.0 port on the cPCI-3510G. Two more dual-slot options are the cPCI-3510L with additional 2x GbE, 1x COM and 2x USB and the cPCI-3510M with one 100-pin high density connector supporting additional 2x DVI-I/DP, 2x USB 2.0, 2x COM, 2x KB/MS and Line-in/Line-out ports.

Graphics support is integrated on the CPU and allows 3 independent displays on the front panel by selecting the cPCI-3510G with additional 2x DisplayPorts. Storage includes a CFast slot or a 32GB SSD (optional) and 2.5" SATA HDD on the layer 2 riser card (cPCI-3510D/P/L/M). One optional PCI 32-bit/66 MHz PMC site or PCIe x1 XMC site is available on the 8HP or 12HP versions (cPCI-3510S or cPCI-3510P/T).

Rear I/O signals to J2 include 4x PCIe x1, 3x SATA 3 Gb/s, and 3x USB 2.0. GPIO and SMBus signals are also routed to the J2 connector. The optional Rear Transition Module (RTM) provides 3x SATA, 2x GbE, 2x USB, 1x COM (Tx/Rx) and 1x VGA port.

The cPCI-3510 is a high performance solution for factory automation and other industrial applications that require superior data transfer capability and advanced computing power. The ADLINK cPCI-3510 provides high manageability, supports Satellite mode operation as a standalone blade in peripheral slots, and IPMI for

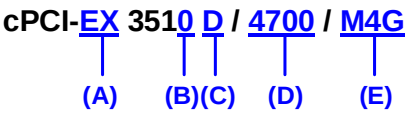
system health monitoring. A GbE port on the faceplate supports Intel® AMT 9.0 for remote monitoring.

1.2 Features

- 3U CompactPCI blade in 4HP, 8HP or 12HP width form factor
- Intel® Core™ i7-4700EQ Processor (4 cores, 8 threads, 6M cache, 2.4 GHz)
- Graphics and memory controllers integrated in processor
- Compatible with PICMG 2.30 PlusIO (3x SATA, 4x PCIe x1, 3x USB, 2x GbE to J2)
- Dual channel DDR3L-1600 soldered SDRAM with ECC, up to 8GB
- 32bit/ 33, 66MHz CompactPCI Interface based on PCI specifications, universal V(I/O)
- Supports Satellite mode operation as a standalone blade in peripheral slots
- Optional 32-bit/66MHz PMC or PCIe x1 XMC site
- Supports IPMI for system health monitoring
- DVI-I port on front with VGA switchable to rear I/O by BIOS setting
- Additional two DisplayPorts on 8HP daughter board (cPCI-3510G)
- Supports 3 independent displays with DirectX 11.1, OpenGL 3.2
- Two PCIe Gigabit Ethernet egress ports, one supporting Intel iAMT 9.0
- Two additional PCIe Gigabit Ethernet Controllers routed to RTM (cPCI-R3P00)
- Additional two Gigabit Ethernet ports on 80mm RTM (cPCI-R3P00T)
- Line-in and Line-out ports on front panel (cPCI-3510D)
- CFast socket for SATA interface storage
- Optional onboard SSD for SATA interface storage (shares space with CFast socket)
- 2.5" SATA drive onboard on 8HP/12HP versions at 6 Gb/s (cPCI-3510/D/G/M/L)

1.3 Model Number Decoder

Blades



(A) Operating Temperature Code

- **Blank** = -20°C to +70°C
- **ET** = -40°C to +85°C (for CPUs with TDP below 37W only)

(B) J2 Connector Type Code

- **0** = HM connector
- **1** = UHM connector (PICMG 2.30 PlusIO compliant)

(C) Configuration Code

- **Blank** = Single slot width with CFast socket, 1x DVI-I, 1x USB 3.0, 2x GbE
- **D** = Dual slot width with CFast socket, 1x DVI-I, 1x USB 3.0, 2x GbE on layer 1; 2x USB, COM (RS-232/422/485), PS/2 KB/MS, Line-in, Line-out ports and 2.5" SATA drive space on layer 2 DB-3610L2
- **G** = Dual slot width with CFast socket, 1x DVI-I, 1x USB 3.0, 2x GbE on layer 1; 2x DisplayPort, RJ-45 COM (RS-232/422/485), PS/2 KB/MS, USB ports, onboard SATA connector and 2.5" SATA drive space on layer 2 DB-3970L2
- **L** = Dual slot width with CFast socket, 1x DVI-I, 1x USB 3.0, 2x GbE on layer 1; 2x GbE, 1x DB-9 COM (RS-232/422/485), 1x USB2.0 at front panel, 1x onboard USB port and 2.5" SATA drive space on layer 2 DB-LAN2-S
- **M** = Dual slot width with CFast socket, 1x DVI-I, 1x USB 3.0, 2x GbE on layer 1; 1x 100-pin high density connector supports 2xDVI/DP, 2x USB2.0, 2x COM (RS-232/422/485), 1x KB/MS, audio and 2.5" SATA drive space on layer 2 DB-Max
- **S** = Dual slot width with CFast socket, 1x DVI-I, 1x USB 3.0, 2x GbE on layer 1; PMC/XMC site on layer2 DB-3UMC

- **P** =Triple slot width with CFast socket, 1x DVI-I, 1x USB 3.0, 2x GbE on layer 1; 2x USB, COM (RS-232/422/485), PS/2 KB/MS, Line-in, Line-out ports and 2.5" SATA drive space on layer 2 DB-3610L2; PMC/XMC site in layer 3 DB-3UMC
- **T** = Triple slot width with CFast socket, 1x DVI-I, 1x USB 3.0, 2x GbE on layer 1; 2x DisplayPort, RJ-45 COM, PS/2 KB/MS, USB ports, onboard SATA connector and 2.5" SATA drive space on layer 2 DB-3970L2; PMC/XMC site on layer 3 DB-3UMC
- Other = ODM/OEM project code

(D) CPU Code

- **4700EQ** = Quad Core Intel® i7-4700EQ processor

(E) Memory Size Code

- M4G = 2x 2GB DDR3L-1600 soldered SDRAM
- M8G = 2x 4GB DDR3L-1600 soldered SDRAM

RTMs

(A) Model Code

- Blank = dual slot width, 50mm depth 3U RTM with 2x COM, 2x USB, 3x SATA, VGA, 2x GbE (switched from front CPU blade)
- T = dual slot width, 80mm depth 3U RTM with 2x COM, 2x USB, 3x SATA, VGA, 2x GbE (independent from front CPU blade)

1.4 Package Contents

The cPCI-3510 is packaged with the following components. If any of the following items are missing or damaged, retain the shipping carton and packing material and contact the dealer for inspection. Please obtain authorization before returning any product to ADLINK. The packing contents of cPCI-3510 Series non-standard configurations will vary depending on customer requests.

CPU module

- The cPCI-3510 Series Processor Blade
  - CPU and memory specifications will differ depending on options selected
  - Thermal module is assembled on the board
- Y-cable for PS/2 combo port (8HP/12HP version only)
- 2.5" HDD accessory pack (8HP/12HP version only)
- RJ-45 to DB-9 COM adapter cable (cPCI-3510G version only)
- RS-422/485 DB-9-to-DB-9 dongle (cPCI-3510G version only)
- DisplayPort to DVI adapter cable (cPCI-3510G version only)
- ADLINK All-in-One DVD
- User's manual

No I/O cables are included with the cPCI-3510M version.

Rear Transition Module

- cPCI-R3P00 or cPCI-R3P00T RTM
- RS-422/485 DB-9-to-DB-9 dongle

Optional Accessories

- DB-3SSD adapter for onboard SSD 32GB
  - DB-3SSD/B/NTPM (P/N 30-37581-300E)
  - DB-3SSD/B (P/N 30-37581-200E)
  - DB-3SSD/NTPM (P/N 30-37581-100E)
    (B: "coin cell battery", NTPM: "no TPM")
- DisplayPort to DVI adapter cable (P/N 30-01120-0000)
- DisplayPort to VGA adapter cable (P/N 30-01119-0000)
- DisplayPort to HDMI adapter cable (P/N 30-01121-0000)


NOTE:

The contents of non-standard cPCI-3510 configurations may vary depending on the customer's requirements.


CAUTION:

This product must be protected from static discharge and physical shock. Never remove any of the components except at a static-free workstation. Use the anti-static bag shipped with the product when putting the board on a surface. Wear an anti-static wrist strap properly grounded on one of the system's ESD ground jacks when installing or servicing system components.

2 Specifications

2.1 cPCI-3510 Processor Blade Specifications

CompactPCI® Standards	• PICMG® 2.0 CompactPCI® Rev. 3.0 • PICMG® 2.1 Hot Swap Specification Rev. 2.0 • PICMG® 2.9 System Management Rev. 1.0 • PICMG® 2.30 CompactPCI® PlusIO
Mechanical	• Standard 3U CompactPCI® • Board size: 100mm x 160mm • Single slot (4HP, 20.32mm); Dual slot (8HP, 40.64mm); Triple-slot (12HP, 60.96 mm) • CompactPCI® with HM type J1 connector, UHM type J2 connector
Processor	• Intel® Core™ i7-4700EQ Processor, 2.4 GHz, 6MB LLC cache, TDP 45W • Passive heatsink
Chipset	• Mobile Intel® QM87 Express Chipset
Memory	• Dual channel DDR3L-1600 ECC soldered memory • Up to 8GB
CompactPCI Bus	• PCI 32bit/ 33MHz; 3.3V, 5V universal V I/O • Supports operation in system slot as master or in peripheral slot as standalone blade without connectivity to CompactPCI bus (Satellite mode)
Gigabit Ethernet	• One PCIe x1 Intel® I217 GbE PHY and three PCIe x1 Intel® I210 Gigabit Ethernet controllers • Two egress 10/100/1000BASE-T ports on front panel, one supporting Intel® AMT 9.0 by I217 controller • Two egress 10/100/1000BASE-T ports routed to rear transition module
Graphics	• Integrated on Intel® Core™ processor • DVI-I port on front panel, VGA switchable to J2 (RTM) by BIOS setting • Analog monitor support up to QXGA 2048x1536 @75Hz, 32-bit • Two DisplayPorts on front panel with resolution up to 2560x1600 @60Hz (cPCI-3510G only) • Up to three independent display
USB	• Up to three USB front panel ports

Table 2-1: cPCI-3510 Processor Blade Specifications

Serial Ports	• Up to four serial ports • One RS-232/422/485 serial port on 8HP front panel (cPCI-3510D/G/L) • Additional RS-232 10-pin header on layer-2 board (cPCI-3510G only) • Up to two RS-232/422/485 COM port (cPCI-3510M only)
PMC/XMC	• One 32-bit/66MHz PMC site or PCIe x1 XMC site if DB-3UMC daughter board is installed
Audio	• Line-in/Line-out on front panel by Realtek ALC262 High Definition Audio codec (cPCI-3510D only) • Line-in/Line-out on front panel by 100-pin connector (cPCI-3510M only)
TPM	Atmel AT97SC3204 TPM (upon request) supporting: • Over/Under voltage detection • Low/High frequency sensor/filter • Reset filter • Memory encryption/decryption
Storage Interfaces[1]	• CFast socket on daughter board • Optional onboard SSD on daughter board • One SATA 6Gb/s direct connector for 2.5" onboard HDD/SDD (8HP/12HP version only)
BIOS	• AMI® EFI BIOS, 64Mbit SPI flash memory
OS Compatibility	• Microsoft Windows 7 32/64-bit • Microsoft Windows 8 32/64-bit • Red Hat Enterprise Linux 6.4, 64-bit • Fedora 14, 32-bit • VxWorks 6.9 • Real Time RTX (MSI) • Other OS support upon request
Environmental	• Operating Temperature (with forced air flow)[2]: Standard: -20°C to 70°C Extreme temperature: -40°C to +85°C (for Intel® Core™ i5 and Intel® Core™ i7-4700EQ processor with cTDP down and forced air flow) • Storage Temperature: -50°C to 100°C • Humidity: 95% @60°C non-condensing • Shock: 20G peak-to-peak, 11ms duration, non-operating • Vibration[3]: 2Grms, 5-500Hz, each axis, operating (w/o hard drive)
EMI	• CE EN55022 • FCC Class A

Table 2-1: cPCI-3510 Processor Blade Specifications

Faceplate I/O	**4HP (cPCI-3510)** • 1x USB 3.0 ports • 2x 10/100/1000BASE-T Ethernet ports • 1x DVI-I port **8HP (cPCI-3510D)** • 1x USB 3.0 ports • 2x 10/100/1000BASE-T Ethernet ports • 1x DVI-I port • 2x USB 2.0 ports • DB-9 RS-232/422/485/485+ port • PS/2 Keyboard/Mouse combo port • Line-in and Line-out port **8HP (cPCI-3510G)** • 1x USB 3.0 ports • 2x 10/100/1000BASE-T Ethernet ports • 1x DVI-I port • 2x DisplayPort • 1x USB 2.0 ports • RJ-45 RS-232/422/485 port[3] • PS/2 Keyboard/ Mouse combo port **8HP (cPCI-3510L)** • 1x USB 3.0 ports • 1x DVI-I port • 4x 10/100/1000BASE-T Ethernet ports • 1x USB 2.0 ports • DB-9 RS-232/422/485 port **8HP (cPCI-3510M)** • 1x USB 3.0 ports • 1x DVI-I port • 2x 10/100/1000BASE-T Ethernet ports • 1x 100-pin connector supports 2x DVI/DP, Line-in/Line-out, 2x USB 2.0, 2x RS-232/422/485 COM, 1x KB/MS **8HP (cPCI-3510S)** • 1x USB 3.0 ports • 2x 10/100/1000BASE-T Ethernet ports • 1x DVI-I port • PMC/XMC site

Table 2-1: cPCI-3510 Processor Blade Specifications

Faceplate I/O	**12HP (cPCI-3510P)** • 1x USB 3.0 ports • 2x 10/100/1000BASE-T Ethernet ports • 1x DVI-I port • 2x USB 2.0 ports • DB-9 RS-232/422/485/485+ port • PS/2 Keyboard/Mouse combo port • Line-in and Line-out port • PMC/XMC site **12HP (cPCI-3510T)** • 1x USB 3.0 ports • 2x 10/100/1000BASE-T Ethernet ports • 1x DVI-I port • 2x DisplayPort • 1x USB 2.0 ports • RJ-45 RS-232/422/485 port1 • PS/2 Keyboard/ Mouse combo port • PMC/XMC site

Table 2-1: cPCI-3510 Processor Blade Specifications

1. The storage device limits the operational vibration tolerance. When the application requires higher specification for anti-vibration, it is recommended to use a flash storage device.
2. ADLINK-certified thermal design. The thermal performance is dependent on the chassis cooling design. Sufficient forced air-flow is required. Temperature limits of optional mass storage devices may also affect the thermal specification.
3. A DB-9-to-DB-9 dongle to convert the cPCI-3510G RS-422/485 pin definitions to common pin definitions is included in the package (“cPCI-3510G/T Serial Ports” on page 47).

2.2 cPCI-R3P00(T) RTM Specifications

Mechanical	Board Size • cPCI-R3P00: 100mm x 50mm • cPCI-R3P00T: 100mm x 80mm Dual-slot (8HP, 40.64mm) (optional single slot upon request)
Gigabit Ethernet	• cPCI-R3P00: Two GbE ports switched from cPCI-3510 2x independent controller i210 • cPCI-R3P00T: Two GbE ports from independent Intel 82580DB GbE controller[1]
Serial Ports	• Two serial ports on I/O panel from pin header • One port converted from USB supporting RS-232/422/485[1] • One port provides Tx, Rx signals only
Storage Interfaces	• Three 7-pin Serial ATA ports
Faceplate I/O	• 2x USB 2.0 ports • 2x 10/100/1000BASE-T Ethernet ports • Analog DB-15 VGA port • 2x COM ports

Table 2-2: cPCI-R3P00(T) RTM Specifications

1. A DB-9-to-DB-9 dongle to convert the cPCI-R3P00 RS-422/485 pin definitions to common pin definitions is included in the package (“COM5 Connector (DB-9)” on page 50).

Specifications are subject to change without prior notice.

2.3 Block Diagrams

cPCI-3510 Blade

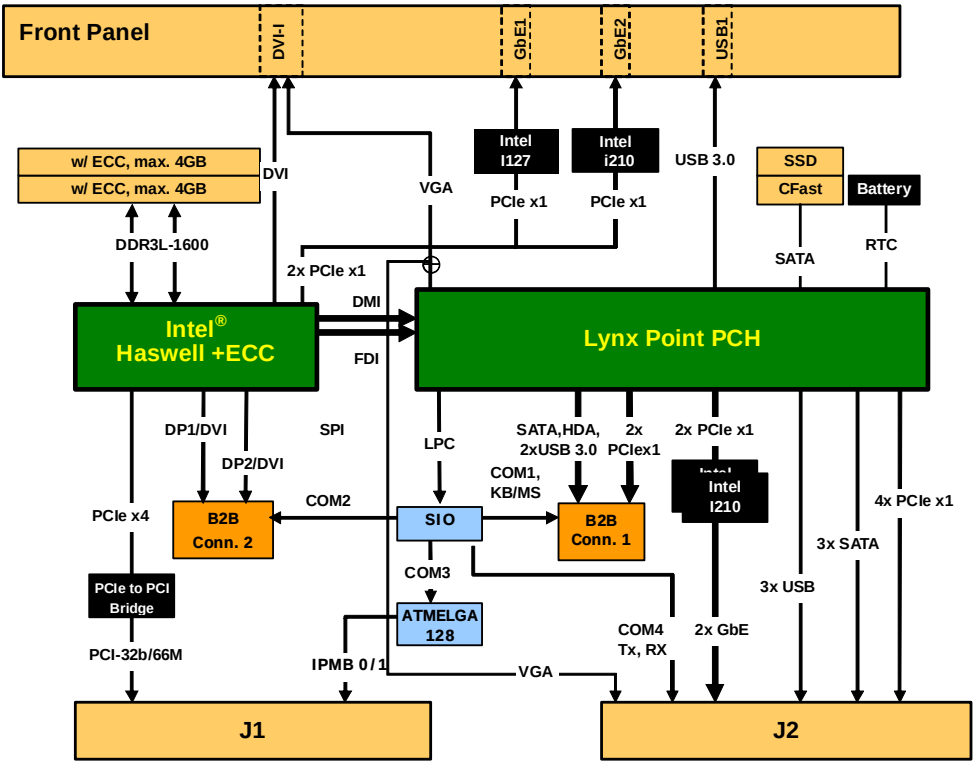


Figure 2-1: cPCI-3510 Blade Functional Block Diagram

DB-3610L2 Daughter Board

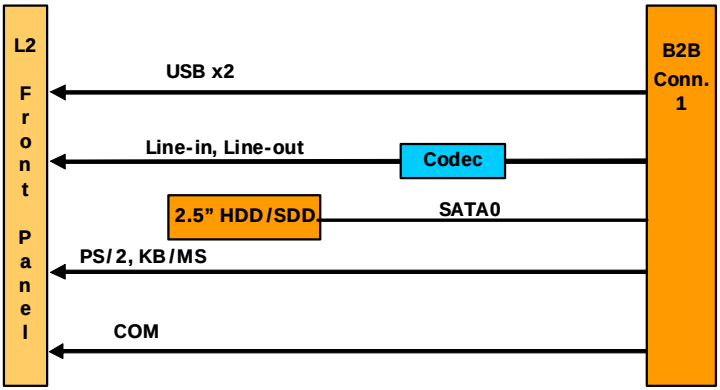


Figure 2-2: DB-3610L2 Daughter Board Functional Block Diagram

DB-3970L2 Daughter Board

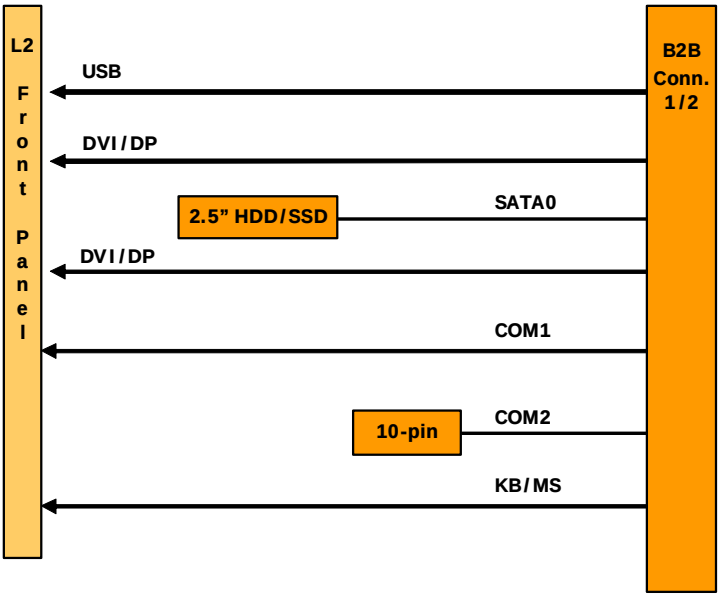


Figure 2-3: DB-3970L2 Daughter Board Functional Block Diagram

DB-LANL2-S Daughter Board

(cPCI-3510L versions)

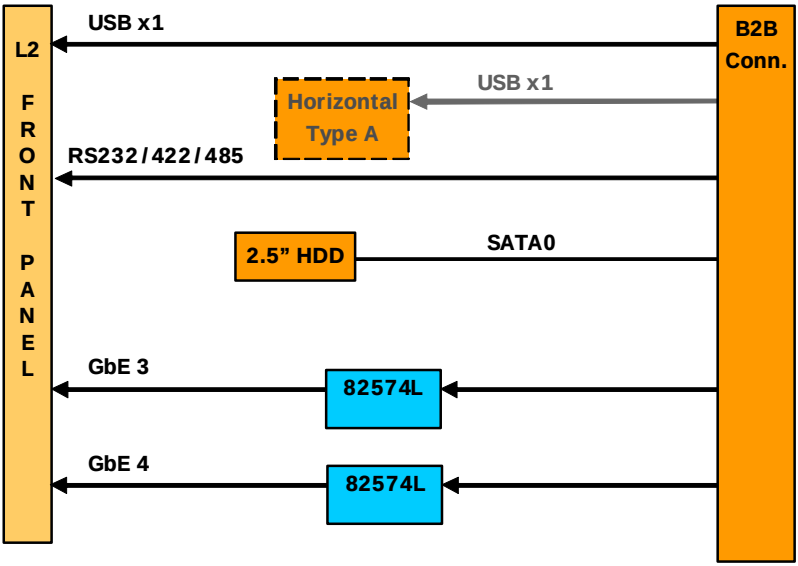


Figure 2-4: DB-LANL2-S Daughter Board Functional Block Diagram

DB-Max Daughter Board

(cPCI-3510M versions)

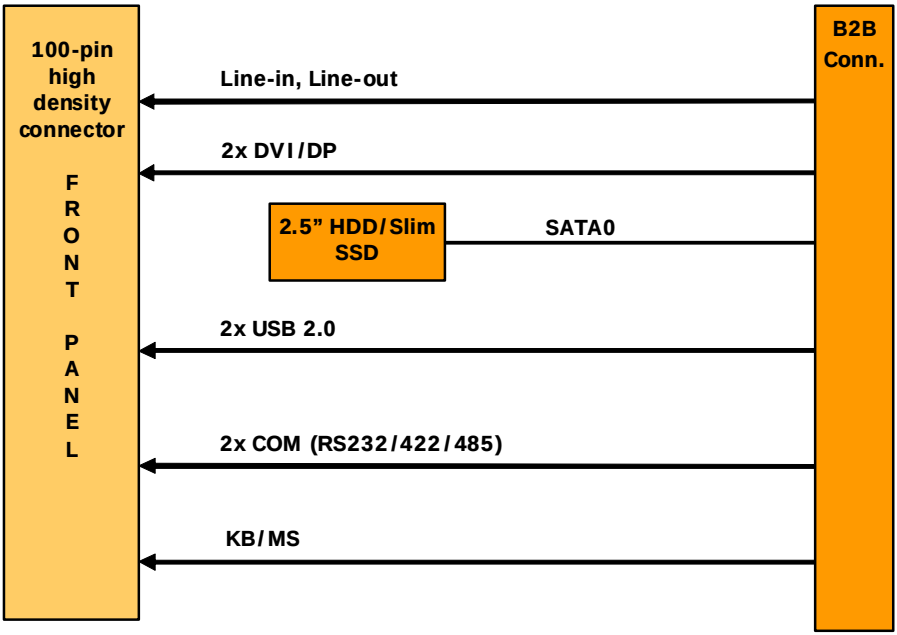


Figure 2-5: DB-Max Daughter Board Functional Block Diagram

cPCI-R3P00 RTM

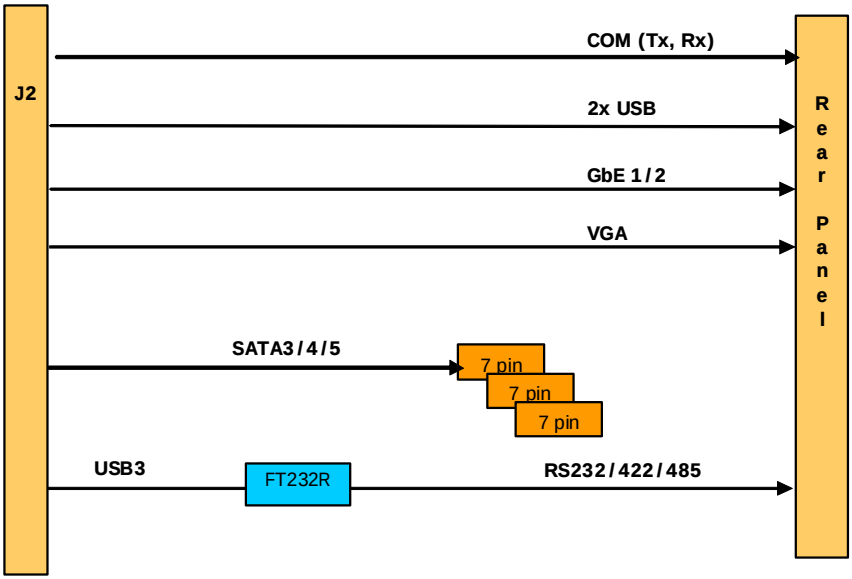


Figure 2-6: cPCI-R3P00 RTM Functional Block Diagram

cPCI-R3P00T RTM

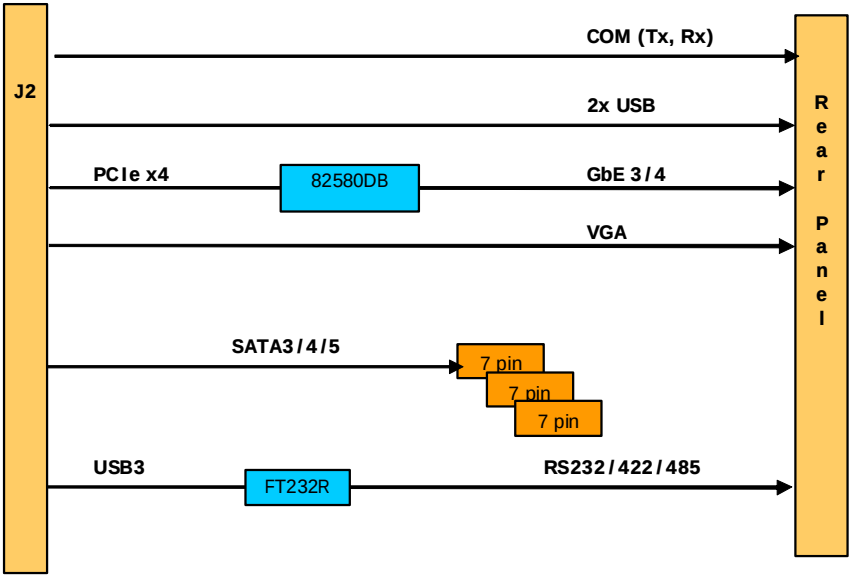


Figure 2-7: cPCI-R3P00T RTM Functional Block Diagram

2.4 I/O Connectivity Table

Function	cPCI-3510 (4HP)		cPCI-3510D (8HP)		cPCI-3510G (8HP)	
	Faceplate	Onboard	Faceplate	Onboard	Faceplate	Onboard
Gigabit Ethernet	Y x2		Y x2		Y x2	
COM			Y (DB-9)		Y (RJ-45)	Y (10-pin)
USB 3.0	Yx1		Yx1		Yx1	
USB 2.0			Y x2		Y x1	
DVI-I	Y		Y		Y	
VGA						
DisplayPort					Y x2	
Serial ATA				Y (for 2.5” drive)		Y (for 2.5” drive)
CFast		Y		Y		Y
PS/2 KB/MS			Y		Y	
Line-in/out			Y			
System LEDs	Y x5		Y x5		Y x5	
Reset Button	Y		Y		Y	

Table 2-3: cPCI-3510 I/O Connectivity

Function	cPCI-3510L (8HP)		cPCI-3510M (8HP)		R3P00(T) (RTM)	
	Faceplate	Onboard	Faceplate	Onboard	Faceplate	Onboard
Gigabit Ethernet	Yx4		Yx2		Y x2[1]	
COM	Y (DB-9)		Yx2		Y x2	
USB 3.0	Yx1		Yx1			
USB 2.0	Yx1		Y2x		Y x2	
DVI-I	Y		Y			
VGA					Y[2]	
DisplayPort						
Serial ATA		Y (for 2.5” drive)		Y (for 2.5” drive)		Y x3 (7-pin)
CFast		Y		Y		
PS/2 KB/MS			Y			
Line-in/out			Y			
System LEDs	Y x5		Y x5			
Reset Button	Y		Y			

Table 2-3: cPCI-3510 I/O Connectivity (cont’d)

1. Routed from CPU blade front ports for cPCI-R3P00, ports independent from front panel for cPCI-R3P00T.
2. VGA switched from front panel.

2.5 Power Requirements

In order to guarantee a stable functionality of the system, it is recommended to provide more power than the system requires. **An industrial power supply unit should be able to provide at least twice as much power as the entire system requires of each voltage**. An ATX power supply unit should be able to provide at least three times as much power as the entire system requires of each voltage.

The tolerance of the voltage lines described in the CompactPCI specification (PICMG 2.0 R3.0) is +5%/-3% for 5, 3.3 V and ±5% for ±12V. This specification is for power delivered to each slot and it includes both the power supply and the backplane tolerance.

Voltage	Nominal Value	Tolerance	Max. Ripple (P - P)
5V	+5.0 VDC	+5% / -3%	50 mV
3.3V	+3.3 VDC	+5% / -3%	50 mV
+12V	+12 VDC	+5% / -5%	240 mV
-12V	-12 VDC	+5% / -5%	240 mV
V I/O (PCI I/O Buffer Voltage)	+3.3 VDC or +5 VDC	+5% / -3%	50 mV
GND			

Power Consumption

This section provides information on the power consumption of cPCI-3510 Series when using the Intel® Core™ i7 processors with 4GB DDR3L-1600 ECC soldered memory and onboard 64GB SATA flash disk. The cPCI-3510 is powered by 5V and 3.3V. Power consumption at 100% CPU usage was measured using the Intel Thermal Analysis Tool (TAT).

Intel® Core™i7-4700EQ			
OS/Mode	**Current 5V**	**Current 3.3V**	**Total Power**
DOS/Idle mode	3.79 A	0.73 A	21.4 W
Windows XP/Idle mode	3.56 A	0.71 A	20.1 W
Windows® XP, CPU 100% Usage	6.97 A	0.71 A	37.2 W

3 Functional Description

The following sections describe the cPCI-3510 Series features and functions.

3.1 Processors

The Mobile 4th Generation Intel® Core™ Processor Family are state of the art, 64-bit, multi-core mobile processor built on 22 nanometer process technology. Based on a new micro-architecture, the processor is designed for a two-chip platform. The two-chip platform consists of a processor and Platform Controller Hub (PCH). The platform enables higher performance, lower cost, easier validation, and improved x-y footprint. The processor includes an Integrated Display Engine, Processor Graphics and Integrated Memory Controller.

The cPCI-3510 Series supports Intel® Core™ i7/i5 processors. The table below lists the general specifications and power ratings of the CPUs supported by the cPCI-3510 Series.

Features	Core™ i7-4700EQ	Core™ i5-I5-4400E	Core™ i5-4402E
Clock	2.4GHz	2.7GHz	1.6 GHz
Max. Single Core Turbo Freq.	3.4GHz	-	-
Last Level Cache	6MB	3MB	3MB
No. of Core(s)	4/8	2/4	2/4
Max. Power (TDP[1])	47W	37W	25W
DMI	5 GT/s	5 GT/s	5 GT/s
$T_{junction, MAX}$[2]	100°C	100°C	100°C

1. The highest expected sustainable power while running known power intensive applications. TDP is not the maximum power that the processor can dissipate.
2. The maximum supported operating temperature.

Supported Technologies

Features	Core™ i7-4700EQ	Core™ i5-I5-4400E	Core™ i5-4402E
Intel® Virtualization Technology for Directed I/O (Intel® VT-d)	Yes	Yes	Yes
Intel® Virtualization Technology (Intel® VT-x)	Yes	Yes	Yes
Intel® VT-x with Extended Page Tables (EPT)	Yes	—	—
Intel® Hyper-Threading Technology	Yes	Yes	Yes
Intel® 64 Architecture	Yes	Yes	Yes
Execute Disable Bit	Yes	Yes	Yes
Intel® Turbo Boost Technology	2.0	Yes	Yes
Intel® vPro Technology	Yes	Yes	Yes
Enhanced Intel SpeedStep® Technology	Yes	Yes	Yes
Thermal Monitoring Technologies	Yes	Yes	Yes
Intel® Identity Protection Technology	Yes	—	—

Interfaces

- Two channels of DDR3L-1333/1600 memory
- DDR3 memory data transfer rates of 1333 MT/s and 1600 MT/s
- 64-bit wide channels
- DDR3L I/O voltage of 1.35V
- 2Gb and 4Gb DDR3 DRAM technologies are supported for x8 and x16 devices (using 4Gb device technologies, the largest memory capacity possible is 8 GB, assuming dual-channel mode with x8, dual-ranked ECC SDRAM)
- PCI Express ports are fully-compliant with the PCI Express Base Specification, Revision 2.0.
- 5 GT/s point-to-point DMI interface to PCH is supported

3.2 Platform Controller Hub

The Mobile Intel® QM87 Express Chipset provides extensive I/O support. Functions and capabilities include:

- The QM87 PCH provides extensive I/O support, functions and capabilities including:
- PCI Express Base Specification, Revision 2.0 support for up to eight ports with transfers up to 5 GT/s
- ACPI Power Management Logic Support, Revision 4.0a
- Enhanced DMA controller, interrupt controller, and timer functions
- Integrated Serial ATA host controllers with independent DMA operation on up to six ports
- USB host interface with two EHCI high-speed USB 2.0 Host controllers and two rate matching hubs provide support for up to fourteen USB 2.0 ports
- Integrated 10/100/1000 Gigabit Ethernet MAC with System Defense
- System Management Bus (SMBus) Specification, Version 2.0 with additional support for I2C devices
- Supports Intel® High Definition Audio
- Supports Intel® Rapid Storage Technology
- Supports Intel® Virtualization Technology for Directed I/O
- Integrated Clock Controller
- Analog and Digital Display ports
- Low Pin Count (LPC) interface
- Firmware Hub (FWH) interface support
- Serial Peripheral Interface (SPI) support

3.3 PMC/XMC

The cPCI-3510P/S/T models support one PMC or XMC site for front panel I/O expansion. The PMC site provides a maximum 32-bit/66MHz PCI bus link using a Pericom PI7C9X130 PCI-Express-to-PCI bridge and PCI-Express x1 link. The PMC site supports +3.3V signaling only. The XMC site provides a PCI Express x1 lane.

3.4 Intel® Turbo Boost Technology

Intel® Turbo Boost Technology is a feature that allows the processor to opportunistically and automatically run faster than its rated operating core and/or render clock frequency when there is sufficient power headroom, and the product is within specified temperature and current limits. The Intel Turbo Boost Technology feature is designed to increase performance of both multi-threaded and single-threaded workloads. The processor supports a Turbo mode where the processor can use the thermal capacity associated with package and **run at power levels higher than TDP power for short durations**. This improves the system responsiveness for short, bursty usage conditions.

Turbo Mode availability is independent of the number of active cores; however, the Turbo Mode frequency is dynamic and dependent on the instantaneous application power load, the number of active cores, user configurable settings, operating environment, and system design. If the power, current, or thermal limit is reached, the processor will automatically reduce the frequency to stay with its TDP limit.

3.5 Intel® Hyper-Threading Technology

Intel® Hyper-Threading Technology allows an execution core to function as two logical processors. While some execution resources (such as caches, execution units, and buses) are shared, each logical processor has its own architectural state with its own set of general-purpose registers and control registers. This feature must be enabled using the BIOS and requires operating system support. Intel recommends enabling Hyper-Threading Technology with Microsoft Windows 7, Vista, and XP, and disabling Hyper-Threading Technology using the BIOS for all previous versions of Windows operating systems.

3.6 Trusted Platform Module

The cPCI-6530 is optionally equipped with an Atmel AT97SC3204 Trusted Platform Module (TPM). The TPM is a secure controller with added cryptographic functionality to provide users a secure environment in e-commerce transactions and Internet communications.

The key features Trusted Platform Module (TPM) offers are:

- Fully compliant to the Trusted Computing Group (TCG) Trusted Platform Module (TPM) version 1.2 specification
- Hardware hash accelerator for SHA-1 algorithm
- Advanced Crypto Engine (ACE) for asymmetric key operations(up to 2048-bit key length) to make hardware protection.
- Tick counter to extend the time required to decipher the key
- In addition to encryption key created by user. it also provide some security features to protect the integrated circuit itself:
- Over/Under-voltage detection to monitor the system stability. If the voltage fluctuates dramatically, this function can block the data transfer and lock the chip.
- Low/High frequency sensor to detect the IC clock frequency. If the frequency fluctuates dramatically, this function can block the data transfer and lock the chip.
- Reset filter to filter reset signal in order to break the time set by tick counter is received
- Memory encryption to protect memory
- Physical shield in the IC to protect the die from intruding or hacking by matching the data transferred on the 2 layer metal shield on the IC. If the data is not matched, the IC may be blocked.

3.7 Battery

The cPCI-3510 is equipped with a 3.0V "coin cell" lithium battery for the Real Time Clock (RTC). The battery socket is equipped on the DB-3CFAST daughter board. The lithium battery must be replaced with an identical battery or a battery type recommended by the manufacturer. A Rayovac BR2032 is equipped on board by default, and can be optionally equipped with a Gold Capacitor (Panasonic EECS5R5H105).

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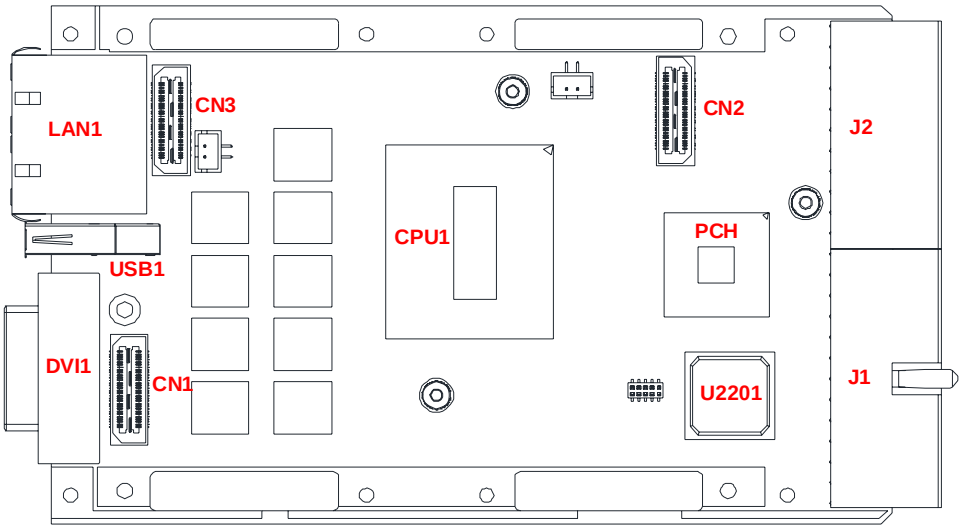
4 Board Interfaces

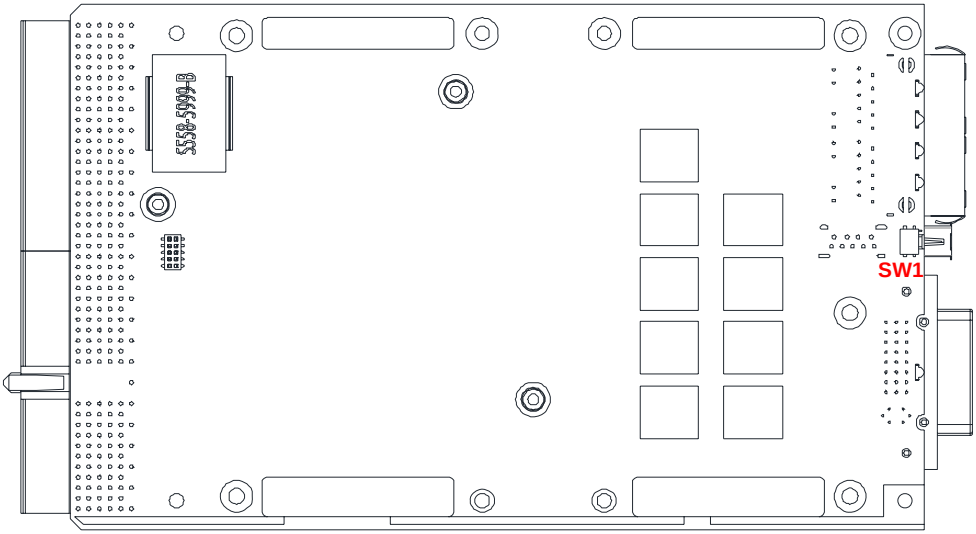
This chapter illustrates the board layout, connector pin assignments, and jumper settings to familiarize users with the cPCI-3510 Series.

4.1 cPCI-3510 Series Board Layout



CPU	Intel® Core™ Processor	**J1**	CompactPCI Connector J1
PCH	Intel® QM87 PCH	**J2**	cPCI J2 (UHM/HM)
CN4/5	Stacked SO-CDIMM socket	**LAN1**	Dual Ethernet connectors
CN1	DB-3610L2/DB-3970L2 connector	**DVI1**	DVI connector
CN2	DB-3CFAST connector	**USB1**	USB port
CN3	DB-3970L2 connector	**U2201**	Pericom PI7C9X130

Figure 4-1: cPCI-3510 Series Board Layout (component side)



SW1	Reset Button

Figure 4-2: cPCI-3510 Series Board Layout (solder side)

4.2 cPCI-3510 Blade Assembly Layout

This section describes the final assembly layout of the single slot cPCI-3510 Blade.

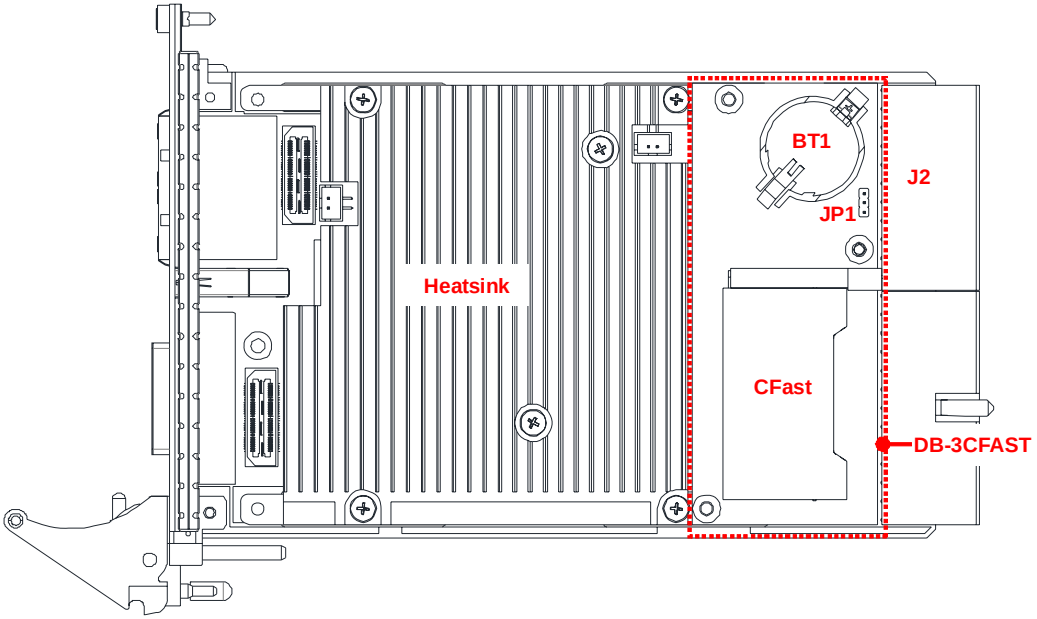
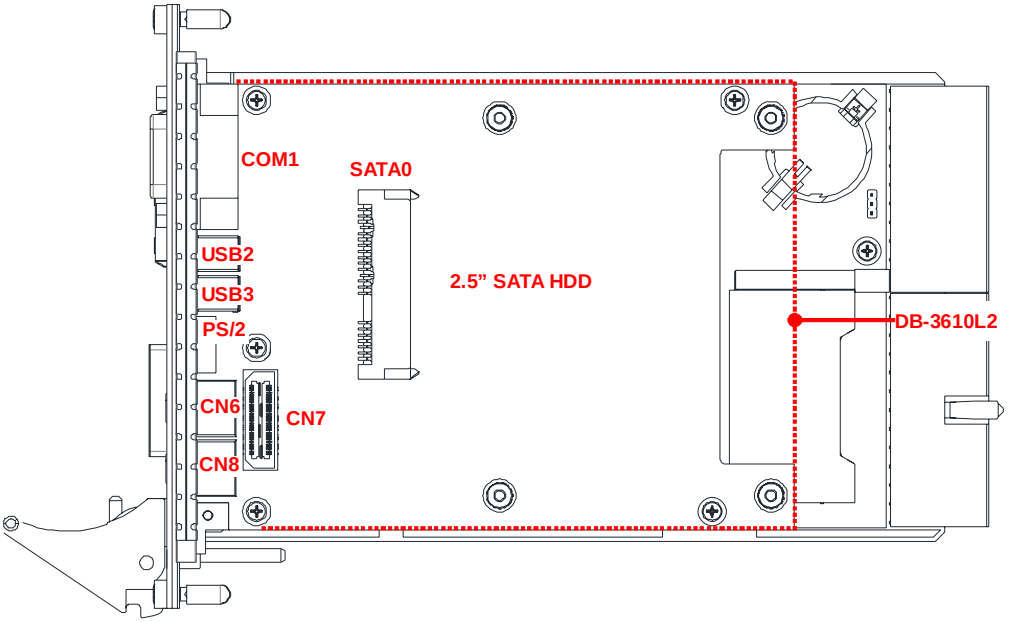


Figure 4-3: cPCI-3510 Blade Assembly Layout

BT1	Battery	**CFast**	CFast socket
JP1	Clear CMOS Jumper	**J2**	cPCI J2 (UHM/HM)

4.3 cPCI-3510D Blade Assembly Layout

The dual-slot width cPCI-3510D Blade is comprised of the cPCI-3510 single-slot main board and the DB-3610L2 riser card to expand I/O connectivity with PS/2, COM, 2x USB ports, Line-in, and Line-out ports .

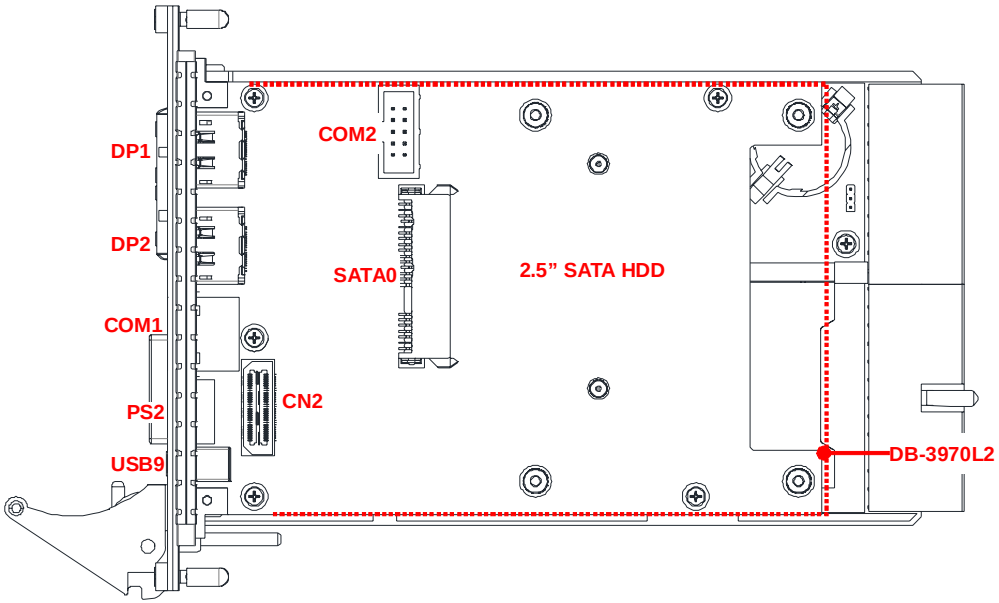


COM1	DB-9 COM port	**CN7**	DB-3UMC connector
USB2/3	USB connectors	**CN6**	Line-in port
PS2	PS/2 KB/Ms Combo port	**CN8**	Line-out port
SATA0	22-pin SATA connector		

Figure 4-4: cPCI-3510D Blade Assembly Layout

4.4 cPCI-3510G Blade Assembly Layout

The dual-slot width cPCI-3510G Blade is comprised of the cPCI-3510 single-slot main board and the DB-3970L2 riser card to expand I/O connectivity with PS/2, COM, USB ports, and 2x DisplayPorts.

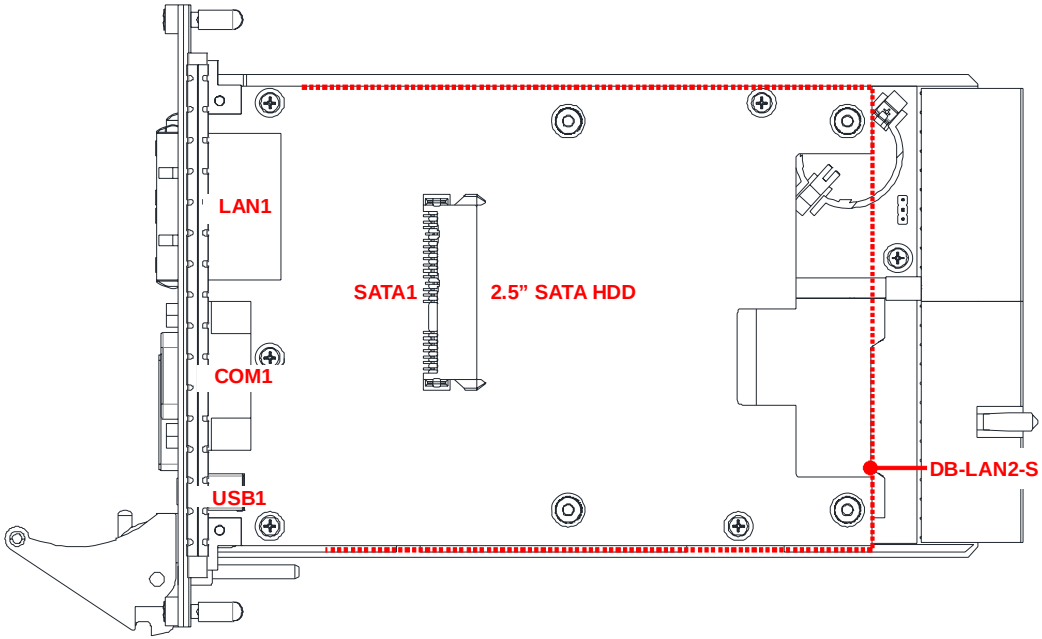


COM1	RJ-45 COM port	**CN2**	DB-3UMC connector
COM2	10-pin COM port	**DP1/2**	DisplayPort connectors
USB9	USB connector	**PS2**	PS/2 KB/MS Combo port
SATA0	22-pin SATA connector		

Figure 4-5: cPCI-3510G Blade Assembly Layout

4.5 cPCI-3510L Blade Assembly Layout

The dual-slot width cPCI-3510L Blade is comprised of the cPCI-3510 single-slot main board and the DB-LAN2-S daughter board, expanding I/O connectivity with 2x LAN, COM, USB.

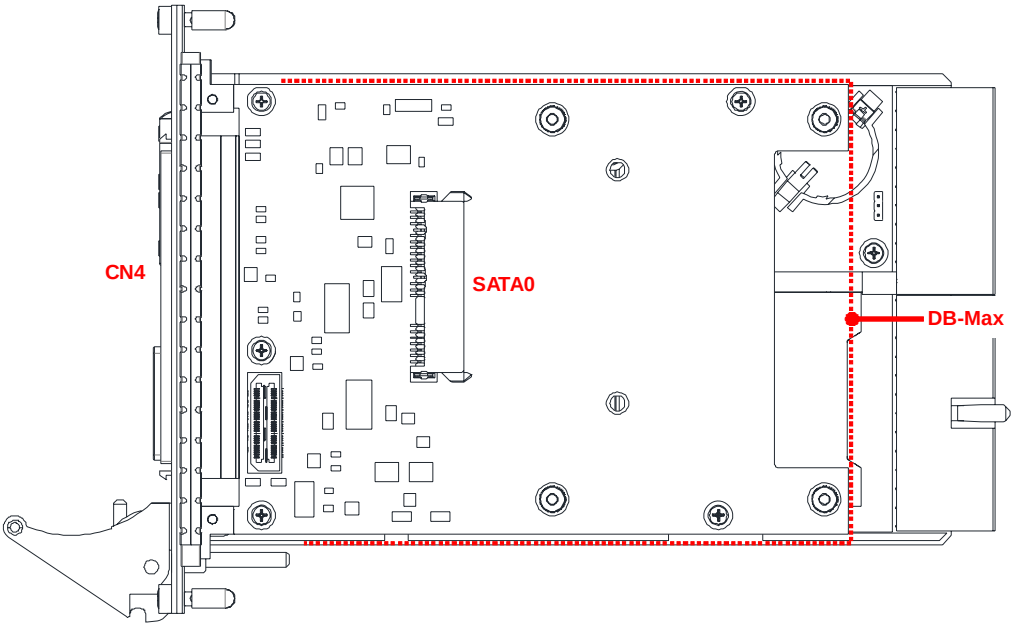


LAN1	GbE RJ-45 ports	**USB1**	USB connector
COM1	DB-9 COM port	**SATA1**	22-pin SATA connector

Figure 4-6: cPCI-3510L Blade Assembly Layout

4.6 cPCI-3510M Blade Assembly Layout

The dual-slot width cPCI-3510M Blade is comprised of the cPCI-3510 single-slot main board and the DB-Max daughter board, expanding I/O connectivity with a 100-pin high density connector.

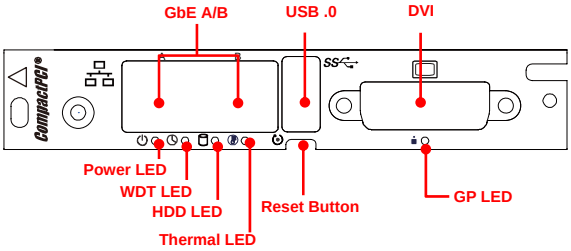


CN4	100-pin high density connector	**SATA0**	22-pin SATA connector

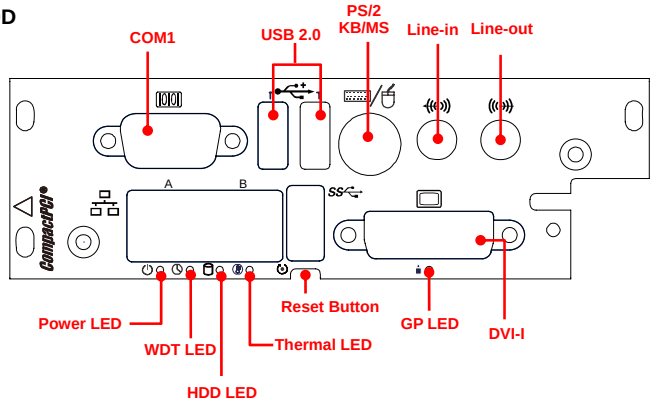
Figure 4-7: cPCI-3510M Blade Assembly Layout

4.7 cPCI-3510, cPCI-3510D, cPCI-3510G Faceplate

cPCI-3510



cPCI-3510D



cPCI-3510G

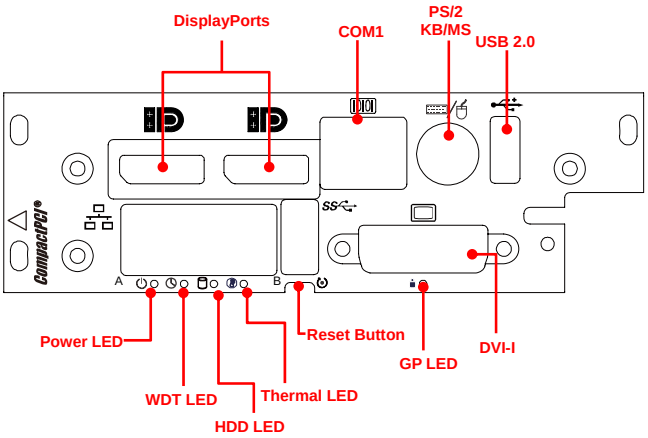
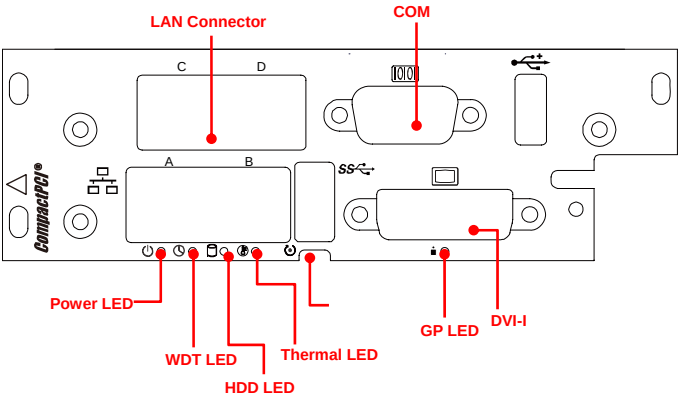


Figure 4-8: cPCI-3510, cPCI-3510D, cPCI-3510G Front Panel Layout

4.8 cPCI-3510L, cPCI-3510M Front Panel

cPCI-3510L



cPCI-3510M

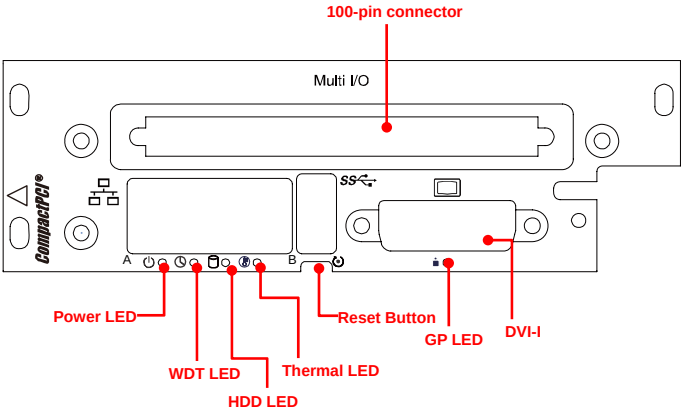


Figure 4-9: cPCI-3510L, cPCI-3510M Front Panel Layout

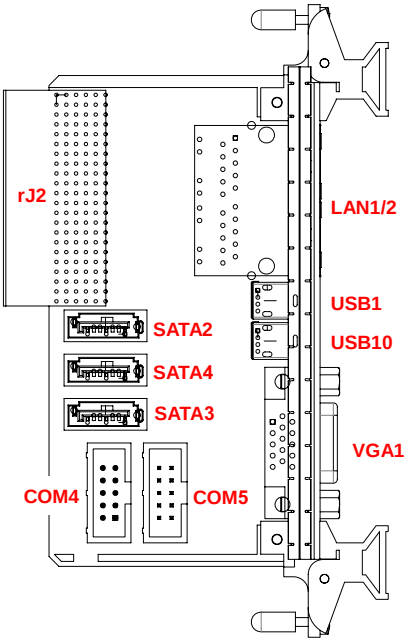
System LEDs

LED	Color	Condition	Indication
Power[1] 	Green/ Red	OFF	System is off
		Red	System Power ready (PWGD)
		Green	Post OK
WDT[1] 	Orange	OFF	No Watchdog event
		Blinking	Watchdog event alert
HDD 	Blue	OFF	No CFast/SATA HDD activity
		Blinking	Data read/write in process for CF/CFast/ SATA HDD
Overheat[1] 	Red	OFF	CPU $T_{junction}$ temperature is under 100ºC
		ON	CPU $T_{junction}$ temperature exceeds 100ºC
GP (General Purpose)[1] 	Yellow	OFF	No activity
		ON/Blinking	Defined by user

Table 4-1: cPCI-3510 Front Panel System LED Descriptions

1. Power, WDT, Overheat, GP LEDs are connected to GPIO pins of IPMC. The Power, WDT, Thermal LEDs can be programmed by the user as general purpose LEDs.

4.9 cPCI-R3P00(T) RTM Board Layout



COM5*	RS-232/422/485 port (converted from USB)	**LAN1/2**	Dual Ethernet ports
COM4	RS-232 port (Tx, Rx only)	**VGA1**	VGA port
SATA2/3/4	SATA ports	**USB1/10**	USB ports
rJ2	CompactPCI connector		

(cPCI-R3P00 is 50mm deep and cPCI-R3P00T is 80mm deep)

Figure 4-10: cPCI-R3P00(T) RTM Board Layout

NOTE:

*COM5 is incorrectly labeled COM3 on the A1 vers. PCB silkscreen.

4.10 cPCI-R3P00(T) RTM Faceplate

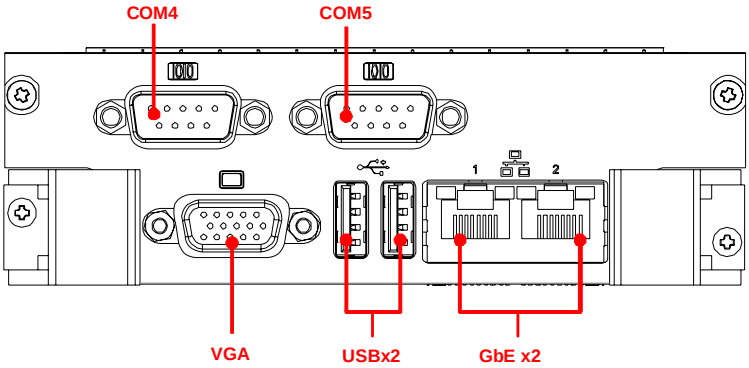


Figure 4-11: cPCI-R3P00(T) RTM Front Panel

4.11 Connector Pin Assignments

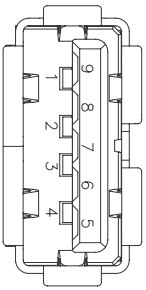
USB 2.0 Connectors

Pin #	Signal Name
1	Vcc
2	UV0-
3	UV0+
4	GND

Table 4-2: USB 2.0 Pin Definition

USB 3.0 Connectors

Pin #	Signal Name
1	USB3.0_P5VA
2	USB2_CMAN
3	USB2_CMAP
4	GND
5	USB3A_CMRXN
6	USB3A_CMRXP
7	GND
8	USB3A_CMTXN
9	USB3A_CMTXP



DB-15 VGA Connector

Signal Name	Pin #	Pin #	Signal Name
Red	1	2	Green
Blue	3	4	N.C.
GND	5	6	GND
GND	7	8	GND
+5V.	9	10	GND
N.C.	11	12	CRTDATA
HSYNC	13	14	VSYNC
CRTCLK	15		

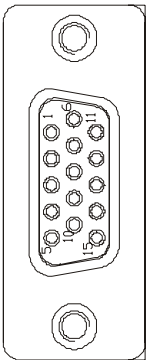


Table 4-3: VGA Pin Definition

DisplayPort Connectors

Pin #	Signal	Pin #	Signal
1	CN_DP0_P	2	Ground
3	CN_DP0_N	4	CN_DP1_P
5	Ground	6	CN_DP1_N
7	CN_DP2_P	8	Ground
9	CN_DP2_N	10	CN_DP3_P
11	Ground	12	CN_DP3_N
13	CN_CAD-L	14	CN_CEC
15	CN_AUX_P	16	Ground
17	CN_AUX_N	18	DDP_HPD
19	Ground	20	P3V3

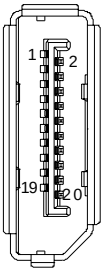
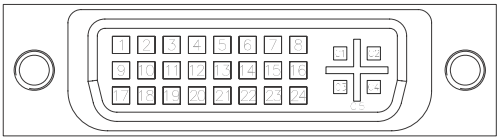


Table 4-4: DisplayPort Pin Definition

DVI-I Connector



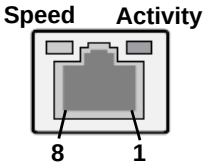
Pin #	Signal	Pin #	Signal
1	TMDS Data2-	16	Hot Plug Detect
2	TMDS Data2+	17	TMDS Data0-
3	GND	18	TMDSData0+
4	NC	19	GND
5	NC	20	NC
6	DDC Clock [SCL]	21	NC
7	DDC Data [SDA]	22	GND
8	Analog vertical sync	23	TMDS Clock +
9	TMDS Data1-	24	TMDS Clock -
10	TMDS Data1+	C1	Analog Red
11	GND	C2	Analog Green
12	NC	C3	Analog Blue
13	NC	C4	Analog Horizontal Sync
14	+5 V Power	C5	Analog GND Return
15	GND		

Table 4-5: DVI-I Connector Pin Definition

RJ-45 Gigabit Ethernet Connectors

Pin #	10BASE-T/ 100BASE-TX	1000BASE-T
1	TX+	LAN_TX0+
2	TX-	LAN_TX0-
3	RX+	LAN_TX1+
4	—	LAN_TX2+
5	—	LAN_TX2-
6	RX-	LAN_TX1-
7	—	LAN_TX3+
8	—	LAN_TX3-

Table 4-6: RJ-45 GbE Pin Definitions



Status		Speed LED (Green/Orange)	Activity LED (Yellow)
Network link is not established or system powered off		OFF	OFF
10 Mbps	Link	OFF	ON
	Active	OFF	Blinking
100 Mbps	Link	Green	ON
	Active	Green	Blinking
1000 Mbps	Link	Orange	ON
	Active	Orange	Blinking

Table 4-7: LAN LED Status Definitions

NOTE:

The cPCI-R3P00 RTM LAN LED signals are not passed through from the main board and are not displayed on the front panel LAN LEDs.

PS/2 Keyboard/Mouse Connector

Pin #	Signal	Function
1	KBDATA	Keyboard Data
2	MSDATA	Mouse Data
3	GND	Ground
4	+5V	Power
5	KBCLK	Keyboard Clock
6	MSCLK	Mouse Clock

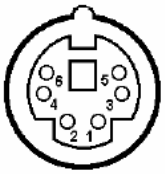


Table 4-8: PS/2 Keyboard/Mouse Pin Definition

cPCI-3510D/P Serial Ports

COM1 Connector (DB-9)

Pin #	RS-232	RS-422	RS-485(+)
1	DCD-L	TXD-	TXD-
2	RXD	TXD+	TXD+
3	TXD	RXD+	—
4	DTR-L	RXD-	—
5	GND	GND	GND
6	DSR-L	—	—
7	RTS-L	—	—
8	CTS-L	—	—
9	RI-L	—	—

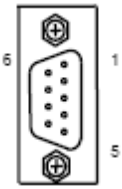


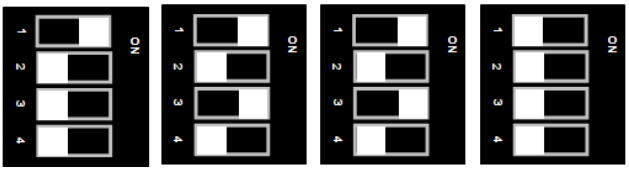
Table 4-9: cPCI-3510D/P COM1 (DB-9) Pin Definition

NOTE:

The COM mode setting for cPCI-3510D/P models is set using SW1~SW4. See *"COM1 Mode Selection Switches (SW1~SW4)" on page 46*.

COM1 Mode Selection Switches (SW1~SW4)

These switches set the cPCI-3510D/P COM1 to RS-232 full modem, RS-422, RS-485, or RS-485+ half-duplex mode. Switches SW1~SW4 are located on the top edge of the DB-3610L2 board. RS-232 full modem is set by default.



SW1 **SW2** **SW3** **SW4**

Mode	Pin	SW1	SW2	SW3	SW4
RS-232	1	ON	ON	ON	OFF
	2	OFF	OFF	OFF	OFF
	3	OFF	ON	ON	OFF
	4	OFF	OFF	OFF	OFF
RS-422	1	OFF	OFF	OFF	ON
	2	ON	ON	ON	OFF
	3	OFF	OFF	OFF	ON
	4	OFF	ON	ON	OFF
RS-485	1	OFF	OFF	OFF	ON
	2	OFF	ON	ON	OFF
	3	ON	OFF	OFF	ON
	4	OFF	ON	ON	OFF
RS-485+	1	OFF	OFF	OFF	OFF
	2	OFF	ON	ON	ON
	3	ON	OFF	OFF	OFF
	4	OFF	ON	ON	ON

Table 4-10: cPCI-3510D/P COM1 Mode Selection Switch Settings

NOTE:

The COM mode setting for cPCI-3510D/P models must be set using the SW1~SW4 DIP switches above. The *cPCI-3510G/T COM1/2 Output* BIOS setting is only used for cPCI-3510G/T models.

cPCI-3510G/T Serial Ports

COM1 Connector (RJ-45)

Pin #	RS-232	RS-422	RS-485
1	DCD-L	—	—
2	RTS-L	TXD+	TXD+
3	DSR-L	—	—
4	TXD	TXD-	TXD-
5	RXD	RXD-	—
6	Ground	—	—
7	CTS-L	RXD+	—
8	DTR-L	—	—
9	RI-L	—	—

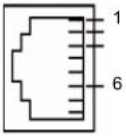


Table 4-11: cPCI-3510G/T COM1 (RJ-45) Pin Definition

NOTE:

The COM mode settings for cPCI-3510G/T models are set in the BIOS: see *"Output (cPCI-3510G/T COM1/2)" on page 104*.

COM1 Connector with DB-9 Adapter

An RJ-45 to DB-9 adapter cable is provided to breakout the COM1 signals.

Pin #	RS-232	RS-422	RS-485
1	DCD-L	—	—
2	RXD	RXD-	—
3	TXD	TXD-	TXD-
4	DSR-L	—	—
5	Ground	—	—
6	DSR-L	—	—
7	RTS-L	TXD+	TXD+
8	CTS-L	RXD+	—
9	—	—	—

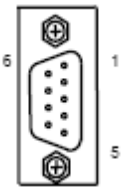


Table 4-12: cPCI-3510G/T COM1 (DB-9 adapter) Pin Definition

NOTE:

The cPCI-3510G/T COM1 RS-422/485 pin definitions are different from the common DB-9 pin definitions. An RS-422/485 DB-9 male-female adapter dongle is provided to allow compatibility with common RS-422/485 pin definitions.

RS-422/485 Adapter Dongle for cPCI-3510G/T

A DB-9 male-female adapter dongle is provided to allow compatibility with common RS-422/485 pin definitions

DB-9 (Female) Signal Name	Pin #	DB-9 (Male) Signal Name
NC	1	TXD-
RXD-	2	TXD+
TXD-	3	RXD+
NC	4	RXD-
NC	5	NC
NC	6	NC
TXD+	7	NC
RXD+	8	NC
NC	9	NC

Table 4-13: RS-422/485 Adapter Dongle Pin Definition

COM1 with RS-422/485 Dongle (DB-9)

Pin #	RS-422	RS-485
1	TXD-	TXD-
2	TXD+	TXD+
3	RXD+	—
4	RXD-	—
5	—	—
6	—	—
7	—	—
8	—	—
9	—	—

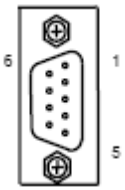


Table 4-14: cPCI-3510G/T COM1 with RS-422/485 Dongle Pin Definition

COM2 Pin Header

Pin #	RS-232	RS-422	RS-485
1	DCD-L	—	—
2	DSR-L	—	—
3	RXD	RXD-	—
4	RTS-L	TXD+	TXD+
5	TXD	TXD-	TXD-
6	CTS-L	RXD+	—
7	DTR-L	—	—
8	RI-L	—	—
9	Ground	—	—
10	NC	—	—

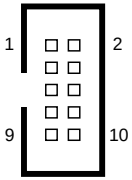


Table 4-15: cPCI-3510G/T COM2 Pin Header Definition

NOTE:

The COM mode settings for cPCI-3510G/T models are set in the BIOS: see *"Output (cPCI-3510G/T COM1/2)" on page 104*.

cPCI-R3P00(T) RTM Serial Ports

COM4 Connector (DB-9))

Pin #	RS-232
1	—
2	RXD
3	TXD
4	—
5	GND
6	—
7	—
8	—
9	—

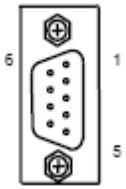


Table 4-16: cPCI-R3P00 RTM COM4 Pin Definition

COM5 Connector (DB-9)

NOTE:

The cPCI-R3P00(T) RTM COM5 RS-422/485 pin definitions are different from the common DB-9 pin definitions. An RS-422/485 DB-9 male-female adapter dongle is provided to allow compatibility with common RS-422/485 pin definitions. See “RS-422/485 Adapter Dongle for cPCI-3510G/T” on page 48

Pin #	RS-232	RS-422	RS-485
1	DCD-L	—	—
2	RXD	RXD-	—
3	TXD	TXD-	TXD-
4	DTR-L	—	—
5	GND	—	—
6	DSR-L	—	—
7	RTS-L	TXD+	TXD+
8	CTS-L	RXD+	—
9	RI-L	—	—

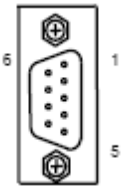


Table 4-17: cPCI-R3P00(T) RTM COM5 Pin Definition

COM5 with RS-422/485 Dongle (DB-9)

Pin #	RS-422	RS-485
1	TXD-	TXD-
2	TXD+	TXD+
3	RXD+	—
4	RXD-	—
5	—	—
6	—	—
7	—	—
8	—	—
9	—	—

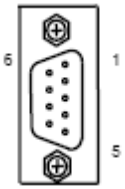


Table 4-18: cPCI-R3P00(T) RTM COM5 with RS-422/485 Dongle Pin Def’n

cPCI-3510M 100-pin I/O Connector (CN4)

Pin #	Signal	Pin #	Signal
1	GND	2	USB9_CN-N
3	USB9_CN-P	4	GND
5	USB1_CN-N	6	USB1_CN-P
7	GND	8	GND
9	TMDS_I2C_DATA	10	TMDS_I2C_CLK
11	GND	12	TMDSB_DATA2B
13	TMDSB_DATA2	14	GND
15	TMDSB_DATA1B	16	TMDSB_DATA1
17	GND	18	TMDSB_DATA0B
19	TMDSB_DATA0	20	GND
21	TMDSB_CLKB	22	TMDSB_CLK
23	GND	24	P5V_DVI1
25	TMDSB_HPD	26	GND
27	NC	28	NC
29	GND	30	TMDS_I2C_DATA
31	TMDS_I2C_CLK	32	GND
33	TMDSB_DATA2B	34	TMDSB_DATA2
35	GND	36	TMDSB_DATA1B
37	TMDSB_DATA1	38	GND
39	TMDSB_DATA0B	40	TMDSB_DATA0
41	GND	42	TMDSB_CLKB
43	TMDSB_CLK	44	GND
45	P5V_DVI2	46	TMDSB_HPD
47	GND	48	NC
49	NC	50	GND
51	P5V_USB_1_9	52	P5V_USB_1_9
53	P5V_USB_1_9	54	P5V_USB_1_9
55	GND	56	GND
57	GND	58	P5V_KBMS
59	MSCLK_CN	60	MSDATA_CN

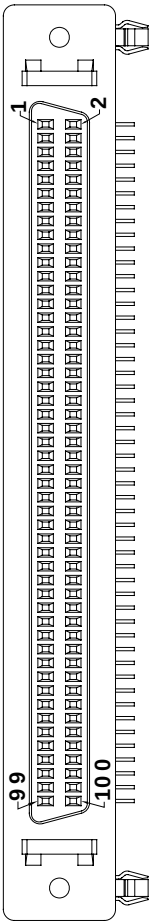


Table 4-19: cPCI-3510M 100-pin I/O Connector Pin Definition

Pin #	Signal	Pin #	Signal
61	KBCLK_CN	62	KBDATA_CN
63	GND	64	GND
65	COM1_RXD_CN	66	COM1_CTS-L_CN
67	GND	68	COM1_TXD_CN
69	COM1_RTS-L_CN	70	GND
71	COM1_DTR-L_CN	72	COM1_DSR-L_CN
73	COM1_DCD-L_CN	74	GND
75	COM2_RXD_CN	76	COM2_CTS-L_CN
77	GND	78	COM2_TXD_CN
79	COM2_RTS-L_CN	80	GND
81	COM2_DTR-L_CN	82	COM2_DSR-L_CN
83	COM2_DCD-L_CN	84	AGND_AU
85	NC	86	NC
87	NC	88	NC
89	NC	90	NC
91	NC	92	AGND_AU
93	L_IN_R	94	L_IN_L
95	L_IN_JD	96	AGND_AU
97	HP_R	98	HP_L
99	HP_JD	100	AGND_AU

Table 4-19: cPCI-3510M 100-pin I/O Connector Pin Definition

Serial ATA Connectors on RTM (CN4-R, CN5-R)

Pin #	Signal
1	GND
2	TX+
3	TX-
4	GND
5	RX-
6	RX+
7	GND

Table 4-20: Serial ATA Connector on RTM

Serial ATA Connector on DB-3610L2/3970L2

Pin #	Signal
S1	GND
S2	TX+
S3	TX-
S4	GND
S5	RX-
S6	RX+
S7	GND
P1	NC
P2	NC
P3	NC
P4	GND
P5	GND
P6	GND
P7	5V
P8	5V
P9	5V
P10	GND
P11	NC
P12	GND
P13~P15	NC

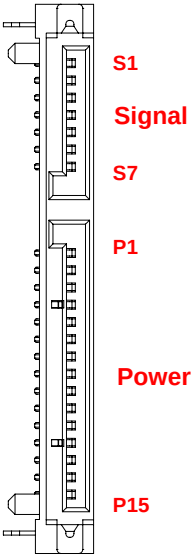


Table 4-21: Serial ATA Connector on DB-3610L2/3970L2 Pin Definition

CFast Socket (on DB-3CFAST)

Pin #	Signal Name
Ground	S1
SATA_TX-P	S2
SATA_TX-N	S3
Ground	S4
SATA_RX-N	S5
SATA_RX-P	S6
Ground	S7
CFast_CDI	P1
Ground	P2
NC	P3
NC	P4
NC	P5
NC	P6
Ground	P7
CFast_LED1	P8
CFast_LED2	P9
NC	P10
NC	P11
NC	P12
P3V3	P13
P3V3	P14
Ground	P15
Ground	P16
CFast_CDO	P17

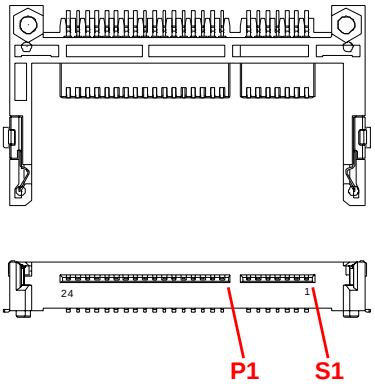


Table 4-22: CFast Socket Pin Definition

DB-3610L2 Connector (CN1)

Signal Name	Pin #	Pin #	Signal Name
USB2-N	1	2	-12V
USB2-P	3	4	+12
GND	5	6	GND
USB3-N	7	8	HDA_SDIN0
USB3-P	9	10	HDA_R_SDOUT
GND	11	12	GND
SATA_ICH_RX-N0	13	14	HDA_R_SYNC
SATA_ICH_RX-P0	15	16	HDA_R_BIT_CLK
GND	17	18	GND
SATA_TX-P0	19	20	CK_L2_PCIE1-P
SATA_TX-N0	21	22	CK_L2_PCIE1-N
GND	23	24	GND
PCIE_TXN5	25	26	CK_L2_PCIE2-P
PCIE_TXP5	27	28	CK_L2_PCIE2-N
GND	29	30	GND
PCIE_RXN5	31	32	HDA_R_RST-L
PCIE_RXP5	33	34	SPKR
GND	35	36	L2_PCIE_RST-L
PCIE_RXN4	37	38	NC
PCIE_RXP4	39	40	USB_2_3_OC-L
GND	41	42	COM1_DCD-L
PCIE_TXN4	43	44	COM1_RI-L
PCIE_TXP4	45	46	COM1_CTS-L
GND	47	48	COM1_DTR-L
MSCLK	49	50	COM1_RTS-L
MSDATA	51	52	COM1_DSR-L
KBCLK	53	54	COM1_SOUT
KBCDATA	55	56	COM1_SIN
P5V	57	58	+3.3V
P5V	59	60	+3.3V

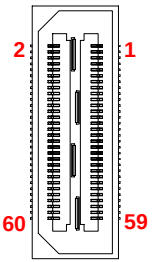


Table 4-23: DB-3610L2 Connector Pin Definition

DB-3CFAST Connector (CN2)

Signal Name	Pin #	Pin #	Signal Name
PCH_SPKR	1	2	CLK33_TPM
SIO_SPKR	3	4	LPC_FRAME-L
GND	5	6	TPM_RST-L
CN_VCC_RTC	7	8	LPC_AD3
GND	9	10	LPC_AD2
NC	11	12	LPC_AD1
NC	13	14	LPC_AD0
NC	15	16	TPM_LPCPD
NC	17	18	PCH_SERIRQ
NC	19	20	TPM_CLKRUN
NC	21	22	TPM_GPIO
NC	23	24	NC
NC	25	26	NC
NC	27	28	NC
NC	29	30	NC
NC	31	32	NC
NC	33	34	NC
NC	35	36	NC
GND	37	38	NC
SATA_PCH_RX-N0	39	40	NC
SATA_PCH_RX-P0	41	42	NC
GND	43	44	NC
SATA_PCH_TX-N0	45	46	NC
SATA_PCH_TX-P0	47	48	NC
GND	49	50	NC
CFast_CDI	51	52	NC
CFast_CDO	53	54	NC
GND	55	56	NC
P5V	57	58	P3V3
P5V	59	60	P3V3

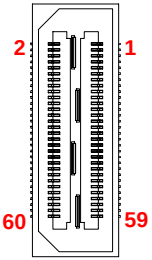


Table 4-24: DB-3CFAST Connector Pin Definition

DB-3970L2 Connector (CN3)

Signal Name	Pin #	Pin #	Signal Name
NC	1	2	RS232_COM2_SEL-L
NC	3	4	COM2_DCD-L
NC	5	6	COM2_RI-L
NC	7	8	COM2_CTS-L
NC	9	10	COM2_DTR-L
NC	11	12	COM2_RTS-L
NC	13	14	COM2_DSR-L
NC	15	16	COM2_SOUT
NC	17	18	COM2_SIN
NC	19	20	NC
NC	21	22	NC
GND	23	24	GND
PCH_DDPD_AUXN	25	26	PCH_DDPC_AUXN
PCH_DDPD_AUXP	27	28	PCH_DDPC_AUXP
GND	29	30	GND
PCH_DDPD_0N	31	32	PCH_DDPC_0N
PCH_DDPD_0P	33	34	PCH_DDPC_0P
GND	35	36	GND
PCH_DDPD_1N	37	38	PCH_DDPC_1N
PCH_DDPD_1P	39	40	PCH_DDPC_1P
GND	41	42	GND
PCH_DDPD_2N	43	44	PCH_DDPC_2N
PCH_DDPD_2P	45	46	PCH_DDPC_2P
GND	47	48	GND
PCH_DDPD_3N	49	50	PCH_DDPC_3N
PCH_DDPD_3P	51	52	PCH_DDPC_3P
GND	53	54	GND
DDPD_CTRLCLK	55	56	DDPC_CTRLCLK
DDPD_CTRLDATA	57	58	DDPC_CTRLDATA
DDPD_HPD	59	60	DDPC_HPD

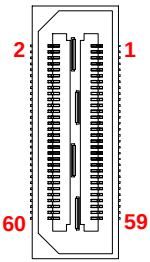


Table 4-25: DB-3970L2 Connector Pin Definition

DB-3UMC Connector on DB-3610L2/3970L2

Signal Name	Pin #	Pin #	Signal Name
NC	1	2	-12V
NC	3	4	+12V
GND	5	6	GND
NC	7	8	NC
NC	9	10	NC
GND	11	12	GND
NC	13	14	NC
NC	15	16	NC
GND	17	18	GND
NC	19	20	CK_PCIE1_P
NC	21	22	CK_PCIE1_N
GND	23	24	GND
PCIE_TXN2	25	26	CK_PCIE2_P
PCIE_TXP2	27	28	CK_PCIE2_N
GND	29	30	GND
PCIE_R_RXN2	31	32	NC
PCIE_R_RXP2	33	34	NC
GND	35	36	PCIE_RST#
PCIE_R_RXN1	37	38	NC
PCIE_R_RXP1	39	40	NC
GND	41	42	NC
PCIE_TXN4	43	44	NC
PCIE_TXP4	45	46	NC
GND	47	48	NC
NC	49	50	NC
NC	51	52	NC
NC	53	54	NC
NC	55	56	NC
+5V	57	58	+3.3V
+5V	59	60	+3.3V

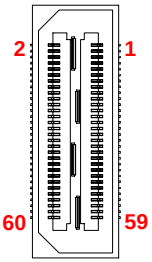


Table 4-26: DB-3UMC Connector Pin Definition

PMC Connector on DB-3UMC (JN1/2)

Pin#	JN1 Signal	JN2 Signal
1	PMC_TCK	P12V
2	N12V	PMC_TRST-L
3	GND	PMC_TMS
4	PCIX_INTA-L	NC (PMC_TDO)
5	PCIX_INTB-L	PMC_TDI
6	PCIX_INTC-L	GND
7	PMC_MOD-L1	GND
8	P5V	NC
9	PCIX_INTD-L	NC
10	NC	NC
11	GND	PMC_MOD-L2
12	P3V3_PMCAUX	P3V3
13	CLK66_PCIX_PMC	PMC_RST-L
14	GND	PMC_MOD-L3
15	GND	P3V3
16	PCIX_GNT-L0	PMC_MOD-L4
17	PCIX_REQ-L0	PMC_PME-L
18	P5V	GND
19	PMC_VIO	PCIX_AD30
20	PCIX_AD31	PCIX_AD29
21	PCIX_AD28	GND
22	PCIX_AD27	PCIX_AD26
23	PCIX_AD25	PCIX_AD24
24	GND	PCIX_AD23
25	GND	PMC_IDSEL
26	PCIX_CBE-L3	PCIX_AD23
27	PCIX_AD22	P3V3
28	PCIX_AD21	PCIX_AD20
29	PCIX_AD19	PCIX_AD18
30	P5V	GND
31	PCIX_FRAME-L	PCIX_AD16
32	PCIX_AD17	PCIX_CBE-L2

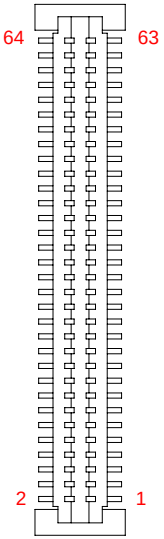
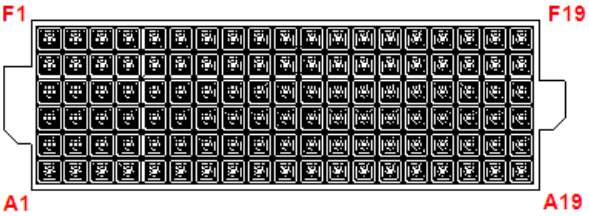


Table 4-27: PMC Connector Pin Definitions

Pin#	JN1 Signal	JN2 Signal
33	PCIX_FRAME-L	GND
34	GND	NC
35	GND	PCIX_TRDY-L
36	PCIX_IRDY-L	P3V3
37	PCIX_DEVSEL-L	GND
38	P5V	PCIX_STOP-L
39	PCIX_PCIXCAP	PCIX_PERR-L
40	PCIX_LOCK-L	GND
41	NC	P3V3
42	NC	PCIX_SERR-L
43	PCIX_PAR	PCIX_CBE-L1
44	GND	GND
45	PMC_VIO	PCIX_AD14
46	PCIX_AD15	PCIX_AD13
47	PCIX_AD12	PCIX_M66EN
48	PCIX_AD11	PCIX_AD10
49	PCIX_AD9	PCIX_AD8
50	P5V	P3V3
51	GND	PCIX_AD7
52	PCIX_CBE-L0	NC
53	PCIX_AD6	P3V3
54	PCIX_AD5	NC
55	PCIX_AD4	NC
56	GND	GND
57	PMC_VIO	NC
58	PCIX_AD3	NC
59	PCIX_AD2	GND
60	PCIX_AD1	NC
61	PCIX_AD0	PCIX_ACK64-L
62	P5V	P3V3
63	GND	GND
64	PCIX_REQ64-L	NC

Table 4-27: PMC Connector Pin Definitions (cont'd)

XMC Connector on DB-3UMC (JN3)



Pin#	A	B	C	D	E	F
1	RXP	RXN	3.3V	NC	NC	VPWR
2	GND	GND	Not used	GND	GND	PCIE_RST-L
3	NC	NC	3.3V	NC	NC	VPWR
4	GND	GND	Not used	GND	GND	Not used
5	NC	NC	3.3V	NC	NC	VPWR
6	GND	GND	Not used	GND	GND	+12V
7	NC	NC	3.3V	NC	NC	VPWR
8	GND	GND	Not used	GND	GND	-12V
9	NC	NC	Not used	NC	NC	VPWR
10	GND	GND	Not used	GND	GND	GA0
11	TXP	TXN	Not used	NC	NC	VPWR
12	GND	GND	GA1	GND	GND	Not used
13	NC	NC	3.3V	NC	NC	VPWR
14	GND	GND	GA2	GND	GND	Not used
15	NC	NC	Not used	NC	NC	VPWR
16	GND	GND	Not used	GND	GND	Not used
17	NC	NC	Not used	NC	NC	NC
18	GND	GND	Not used	GND	GND	Not used
19	CK-P	CK-N	Not used	Not used	Not used	Not used

Table 4-28: XMC Connector Pin Definition

CompactPCI J1 Connector

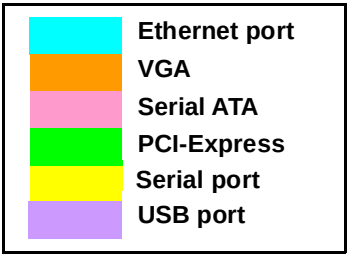
Pin	Z	A	B	C	D	E	F
25	GND	+5V	REQ64#	ENUM#	+3.3V	+5V	GND
24	GND	CPCI_AD1	+5V	CPCI_VIO	CPCI_AD0	ACK64#	GND
23	GND	P3V3	CPCI_AD4	CPCI_AD3	P5V	CPCI_AD2	GND
22	GND	CPCI_AD7	GND	P3V3	CPCI_AD6	CPCI_AD5	GND
21	GND	P3V3	CPCI_AD9	CPCI_AD8	CPCI_M66EN	CPCI_CBE-L0	GND
20	GND	CPCI_AD12	GND	VIO	CPCI_AD11	CPCI_AD10	GND
19	GND	P3V3	CPCI_AD15	CPCI_AD14	GND	CPCI_AD13	GND
18	GND	CPCI_SERR-L	GND	P3V3	CPCI_PAR	CPCI_CBE-L1	GND
17	GND	P3V3	NC	NC	GND	CPCI_PERR-L	GND
16	GND	CPCI_DEVSEL-L	CPCI_PCIXCAP	VIO	CPCI_STOP-L	CPCI_LOCK-L	GND
15	GND	P3V3	CPCI_FRAME-L	CPCI_IRDY-L	NC	CPCI_TRDY-L	GND
12-14	Key						
11	GND	CPCI_AD18	CPCI_AD17	CPCI_AD16	GND	CPCI_CBE-L2	GND
10	GND	CPCI_AD21	GND	P3V3	CPCI_AD20	CPCI_AD19	GND
9	GND	CPCI_CBE-L3	NC	CPCI_AD23	GND	CPCI_AD22	GND
8	GND	CPCI_AD26	GND	VIO	CPCI_AD25	CPCI_AD24	GND
7	GND	CPCI_AD30	CPCI_AD29	CPCI_AD28	GND	CPCI_AD27	GND
6	GND	CPCI_REQ-L0	GND	P3V3	CPCI_CLK0	CPCI_AD31	GND
5	GND	NC	NC	CPCI_RESET-L	GND	CPCI_GNT-L0	GND
4	GND	NC	CPCI_HEALTHY-L	VIO	NC	NC	GND
3	GND	CPCI_IRQA-L	CPCI_IRQB-L	CPCI_IRQC-L	P5V	CPCI_IRQD-L	GND
2	GND	cPCI_TCK-L	P5V	cPCI_TMS-L	NC	cPCI_TDI-L	GND
1	GND	P5V	NC	cPCI_TRST-L	P12V	P5V	GND

Table 4-29: CompactPCI J1 Connector Pin Definition

CompactPCI J2 Connector

Pin	Z	A	B	C	D	E	F
22	GND	GA4	GA3	GA2	GA1	GA0	GND
21	GND	PCI_CLK6	GND	LAN2_TXDP1	LAN1_TXDP3	LAN1_TXDP1	GND
20	GND	PCI_CLK5	GND	LAN2_TXDN1	LAN1_TXDN3	LAN1_TXDN1	GND
19	GND	GND	GND	LAN2_TXDP0	LAN1_TXDP2	LAN1_TXDP0	GND
18	GND	LAN2_TXDP3	LAN2_TXDP2	LAN2_TXDN0	LAN1_TXDN2	LAN1_TXDN0	GND
17	GND	LAN2_TXDN3	LAN2_TXDN2	J2_RSTJ	CPCI_REQ_L6	CPCI_GNT_L6	GND
16	GND	CLK_PCIE8_N	CLK_PCIE6_P	DEGJ	GND	+5V	GND
15	GND	CLK_PCIE8_P	CLK_PCIE6_N	FALJ	CPCI_REQ_L5	CPCI_GNT_L5	GND
14	GND	CLK_PCIE7_N	CLK_PCIE5_P	PCIE_RST-L	DDC_DAT	+5V	GND
13	GND	CLK_PCIE7_P	CLK_PCIE5_N	PCIE_RST-L	VGA_HSY	DDC_CLK	GND
12	GND	PCIE8_RX_P	PCIE_RST-L	PCIE_RST-L	VGA_VSY	SATA_RX-P2	GND
11	GND	PCIE8_RX_N	PCIE_TXP8	COM4_TX	SATA_TX-P2	SATA_RX-N2	GND
10	GND	PCIE7_RX_P	PCIE_TXN8	COM4_RX	SATA_TX-N2	SATA_RX-P3	GND
9	GND	PCIE7_RX_N	PCIE_TXP7	USB_0P	SATA_TX-P3	SATA_RX-N3	GND
8	GND	PCIE6_RX_P	PCIE_TXN7	USB_0N	SATA_TX-N3	SATA_RX-P4	GND
7	GND	PCIE6_RX_N	PCIE_TXP6	USB_3P	SATA_TX-P4	SATA_RX-N4	GND
6	GND	PCIE5_RX_P	PCIE5_RX_P	USB_3N	SATA_TX-N4	RGB_RED	GND
5	GND	PCIE5_RX_N	PCIE_TXP5	USB_10P	RS232_COM5_SEL-L	RGB_GREEN	GND
4	GND	VIO	PCIE_TXN5	USB_10N	USB_OC0	RGB_BLUE	GND
3	GND	CLK4	GND	GNT3#	REQ4#	GNT4#	GND
2	GND	CLK2	CLK3	SYSEN#	GNT2#	REQ3#	GND
1	GND	CLK1	GND	REQ1#	GNT1#	REQ2#	GND

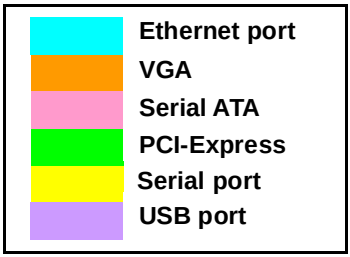
Table 4-30: CompactPCI J2 Connector Pin Definition



cPCI-R3P00 rJ2 Connector

Pin	Z	A	B	C	D	E	F
22	GND	NC	NC	NC	NC	NC	GND
21	GND	NC	GND	2_ETH_B+	1_ETH_D+	1_ETH_B+	GND
20	GND	NC	GND	2_ETH_B-	1_ETH_D-	1_ETH_B-	GND
19	GND	GND	GND	2_ETH_A+	1_ETH_C+	1_ETH_A+	GND
18	GND	2_ETH_D+	2_ETH_C+	2_ETH_A-	1_ETH_C-	1_ETH_A-	GND
17	GND	2_ETH_D-	2_ETH_C-	NC	NC	NC	GND
16	GND	NC	NC	NC	GND	+5V	GND
15	GND	NC	NC	NC	NC	NC	GND
14	GND	NC	NC	NC	DDC_DAT	+5V	GND
13	GND	NC	NC	NC	VGA_HSY	DDC_CLK	GND
12	GND	NC	NC	NC	VGA_VSY	2_SATA_RX+	GND
11	GND	NC	NC	COM4_TX	2_SATA_TX+	2_SATA_RX-	GND
10	GND	NC	NC	COM4_RX	2_SATA_TX-	3_SATA_RX+	GND
9	GND	NC	NC	0_USB+	3_SATA_TX+	3_SATA_RX-	GND
8	GND	NC	NC	0_USB-	3_SATA_TX-	4_SATA_RX+	GND
7	GND	NC	NC	1_USB+	4_SATA_TX+	4_SATA_RX-	GND
6	GND	NC	NC	1_USB-	4_SATA_TX-	RGB_RED	GND
5	GND	NC	NC	10_USB+	RS232_COM5_SEL-L	RGB_GREEN	GND
4	GND	NC	NC	10_USB-	USB1_10_OC	RGB_BLUE	GND
3	GND	NC	GND	NC	NC	NC	GND
2	GND	NC	NC	NC	NC	NC	GND
1	GND	NC	GND	NC	NC	NC	GND

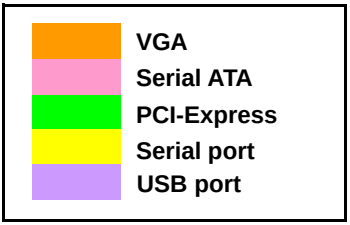
Table 4-31: cPCI-R3P00 rJ2 Connector Pin Definition



cPCI-R3P00T rJ2 Connector

Pin	Z	A	B	C	D	E	F
22	GND	NC	NC	NC	NC	NC	GND
21	GND	NC	GND	NC	NC	NC	GND
20	GND	NC	GND	NC	NC	NC	GND
19	GND	GND	GND	NC	NC	NC	GND
18	GND	NC	NC	NC	NC	NC	GND
17	GND	NC	NC	NC	NC	NC	GND
16	GND	4PE_CLK-	2_PE_CLK+	NC	GND	+5V	GND
15	GND	4PE_CLK+	2_PE_CLK-	NC	NC	NC	GND
14	GND	3PE_CLK+	1_PE_CLK+	4_PE_CLKE#	DDC_DAT	+5V	GND
13	GND	3PE_CLK-	1_PE_CLK-	3_PE_CLKE#	VGA_HSY	DDC_CLK	GND
12	GND	4PE_RX00+	1_PE_CLKE#	2_PE_CLKE#	VGA_VSY	2_SATA_RX+	GND
11	GND	4PE_RX00-	4PE_TX00+	COM4_TX	2_SATA_TX+	2_SATA_RX-	GND
10	GND	3PE_RX00+	4PE_TX00-	COM4_RX	2_SATA_TX-	3_SATA_RX+	GND
9	GND	3PE_RX00-	3PE_TX00+	0_USB+	3_SATA_TX+	3_SATA_RX-	GND
8	GND	2PE_RX00+	3PE_TX00-	0_USB-	3_SATA_TX-	4_SATA_RX+	GND
7	GND	2PE_RX00-	2PE_TX00+	1_USB+	4_SATA_TX+	4_SATA_RX-	GND
6	GND	1PE_RX00+	2PE_TX00-	1_USB-	4_SATA_TX-	RGB_RED	GND
5	GND	1PE_RX00-	1PE_TX00+	10_USB+	RS232_COM5_SEL-L	RGB_GREEN	GND
4	GND	NC	1PE_TX00-	10_USB-	USB1_10_OC	RGB_BLUE	GND
3	GND	NC	GND	NC	NC	NC	GND
2	GND	NC	NC	NC	NC	NC	GND
1	GND	NC	GND	NC	NC	NC	GND

Table 4-32: cPCI-R3P00T rJ2 Connector Pin Definition



4.12 Jumper Settings

Load BIOS Default Jumper (JP1)

The cPCI-3510 Load BIOS Default Jumper is located on the DB-3CF/CFast daughter board. To load the default BIOS settings, short pins 2-3 on JP1, then reinstall the jumper cap to pins 1-2.

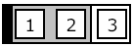
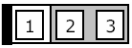
BIOS Setting	Connection	JP1
Normal	1 – 2	
Load default BIOS	2 – 3	

Table 4-33: Load BIOS Default Jumper Settings

XMC VPWR Select Jumper on DB-3UMC (JPX1)

This jumper is located on the DB-3UMC board near JN1/2 and selects the XMC VPWR setting. 5V is set by default.

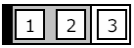
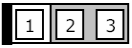
Mode	Connection	JPX1
+5V (Default)	1 – 2	
+12V	2 – 3	

Table 4-34: XMC VPWR Select Jumper Settings

PMC V(I/O) Select Jumper on DB-3UMC (JPX2)

This jumper is located on the DB-3UMC board near JN1/2 and selects the PMC V(I/O) setting. 3.3V is set by default.

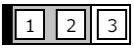
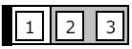
Mode	Connection	JPX2
+5V	1 – 2	
+3.3V (Default)	2 – 3	

Table 4-35: PMC V(I/O) Select Jumper Settings

5 Getting Started

This chapter describes the following installation procedures for the cPCI-3510 and rear transition module:

- CPU and Heatsink
- 2.5" SATA storage drive
- CFast card
- PCI Mezzanine Card
- Processor blade installation to chassis
- RTM installation to chassis

5.1 CPU and Heatsink

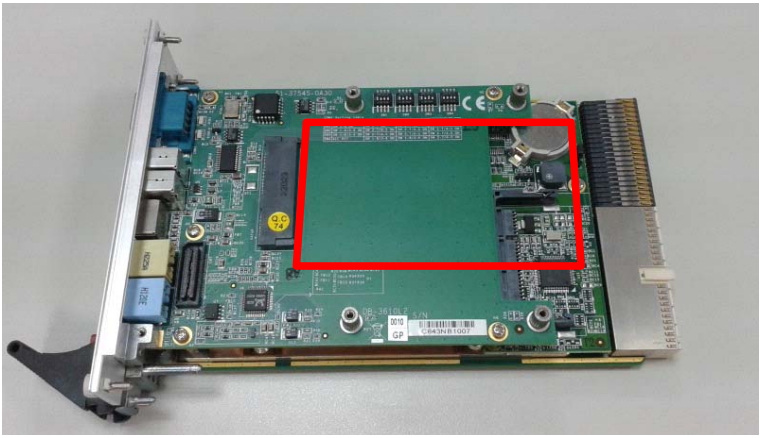
The cPCI-3510 Series come with CPU and heatsink pre-installed. Removal of heatsink/CPU by users is not recommended. Please contact your ADLINK service representative for assistance.

5.2 SATA Drive Installation

The cPCI-3510D/P/L/M 2/3-slot versions provide space to install a slim type 2.5" Serial-ATA storage drive.

Installing a SATA Drive - cPCI-3510D/G/P/L/M

1. A 2.5" SATA drive can be assembled in the location marked as below.

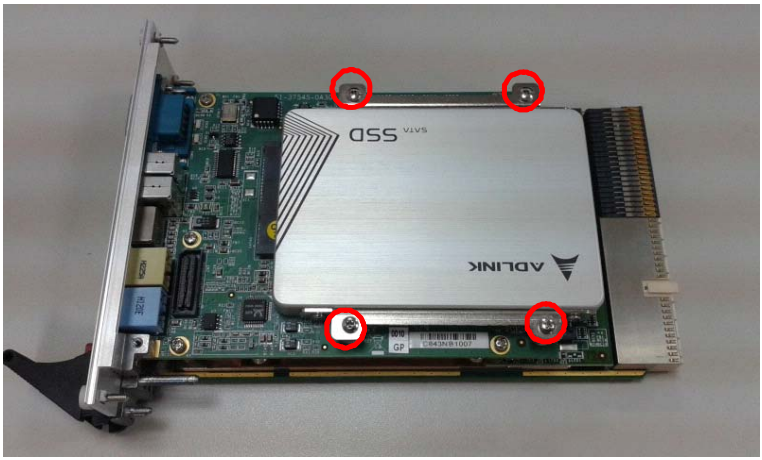


2. 2.Prepare a 2.5" SATA drive and locate the brackets and screws in the accessory kit.

3. Screw the brackets to the 2.5" SATA drive.

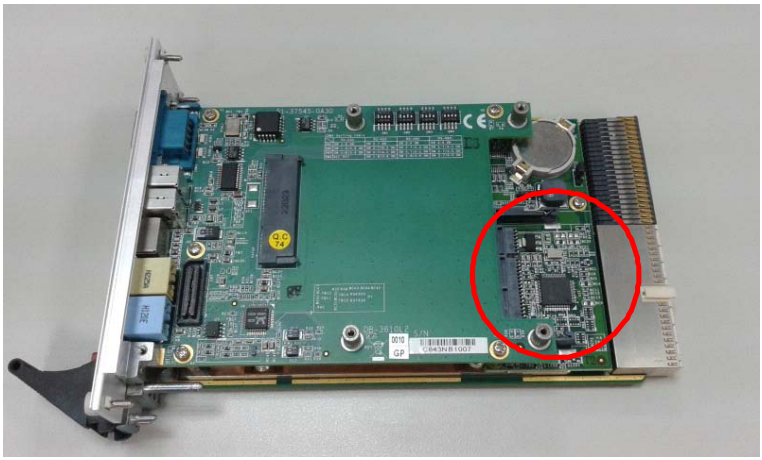
4. Align the drive assembly with the cPCI-3510 and insert it into the onboard SATA connector until it is properly seated.

5. Secure the hard drive assembly to the cPCI-3510 with four M2.5 screws provided.



5.3 Installing a CFast Card

To install a CFast card, locate the CFast connector on the DB-3CFAST daughter board and insert the card until it is properlly seated.



5.4 Installing the cPCI-3510 to the Chassis

The cPCI-3510 may be installed in a system or peripheral slot of a 3U CompactPCI chassis. These instructions are for reference only. Refer to the user guide that comes with the chassis for more information.

1. Be sure to select the correct slot depending on the operational purpose of the module. The system power may now be powered on or off.
2. Remove the blank face cover from the selected slot, if necessary.
3. Press down on the release catches of the cPCI-3510 ejector handles.
4. **Remove the black plastic caps securing the mounting screws to the front panel.**
5. Align the module's top and bottom edges to the chassis card guides, and then carefully slide the module into the chassis. A slight resistance may be felt when inserting the module. If the resistance it too strong, check if there are bent pins on the backplane or if the board's connector pins are not properly aligned with connectors on the backplane. Then push the board until it is completely flush with the chassis.
6. Push the ejector handles outwards to secure the module in place, and then fasten the screws on the module front panel.
7. Connect the cables and peripherals to the board, and then turn the chassis on if necessary.

5.5 RTM Installation - cPCI-R3P00(T)

The installation and removal procedures for a RTM are the same as those for CompactPCI boards. Because they are shorter than front boards, pay careful attention when inserting or removing RTMs.

Refer to previous sections for peripheral connectivity of all I/O ports on the RTM. When installing the cPCI-3510 Series and related RTMs, make sure the RTM is the correct matching model.


NOTE:

You must install the correct RTM to enable functions (I/O interfaces) on the rear panel. Installation of non-compatible RTMs may damage the system board and/or other RTMs.

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6 Driver Installation

The cPCI-3510 drivers are available from the ADLINK All-In-One DVD at **X:\cPCI\cPCI-3510**, or from the ADLINK website (**http://www.adlinktech.com/PD/web/PD_detail.php?cKind=&pid=1291**). ADLINK provides validated drivers for Windows 7 64-bit. We recommend using these drivers to ensure compatibility. The VxWorks BSP can be downloaded from the cPCI-3510 product page on the ADLINK website

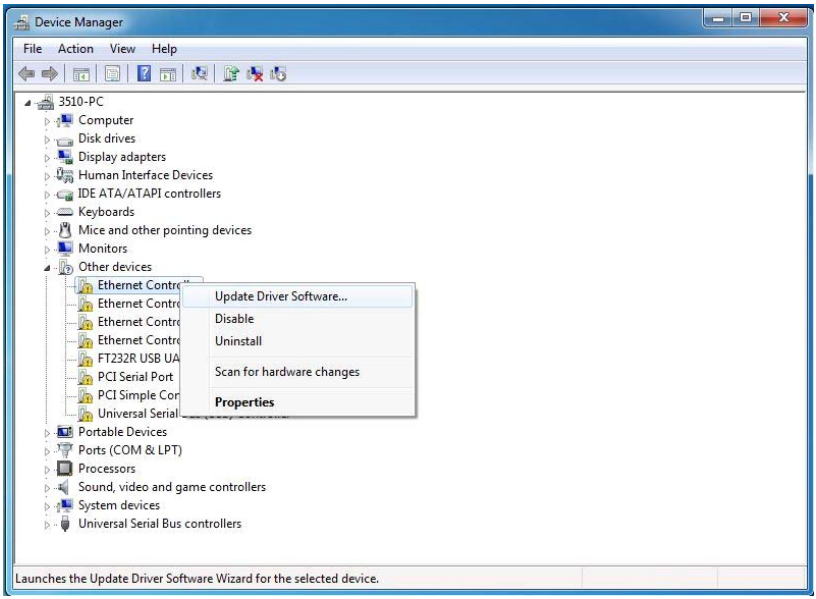
6.1 cPCI-3510 Drivers

The following describes the cPCI-3510 driver installation procedures for Windows 7 64-bit. Install the Windows operating system before installing any driver. Most standard I/O device drivers are installed during Windows installation.

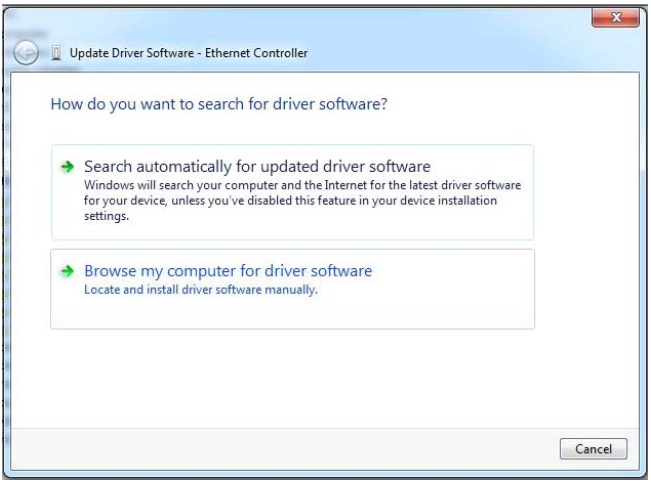
1. Before beginning Windows installation, save the AHCI driver to a USB flash drive. During Windows installation, install the AHCI driver from the USB flash drive when prompted.
2. Install the **chipset driver** by extracting and running the program in **...\Chipset\Intel Chipset Device Software_All OS_9.4.0.1017.zip**.
3. Install the **graphics driver** and utilities by extracting and running the program in **...\Graphics\Intel® HD Graphics 4600_Win7_64bit_9.18.10.3220.zip**.
4. Install the **Ethernet Controller driver** by following the steps described in "6.2 Ethernet Controller Driver" on page 76.
5. Install the **Management Engine (ME) driver** and utilities by extracting and running the program in **...\Chipset\Intel Management Engine Interface 9.0.0.1209.zip**.
6. Install the **TPM driver** by extracting and running the program in **…\TPM\Infineon_Trusted_Platform_Module_2.1.1.0.zip**.
7. Install the **audio driver** and utilities by extracting and running the program in **…\Audio\Realtek_High Definition Audio_Win7_8_64_6.0.1.6873.zip**.

6.2 Ethernet Controller Driver

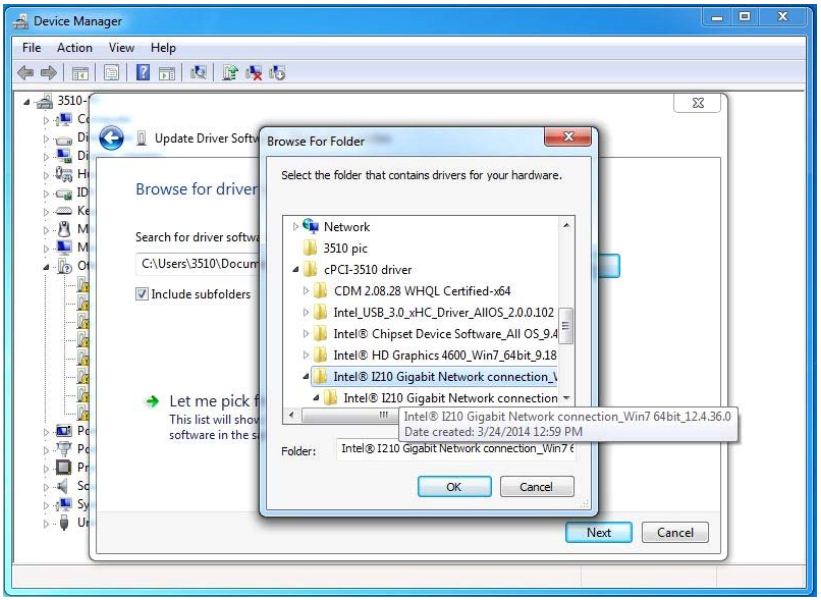
1. Extract the contents of **…\LAN\Intel® I210 Gigabit Network connection_Win7 64bit_12.7.28.0.zip**.
2. Open the *Device Manager* and go to *Other Devices.* You will see a "question mark" next to *Ethernet Controller* R-click on *Ethernet Controller* and choose "Update Driver Software…".



3. Click “Browse my computer for driver software”.



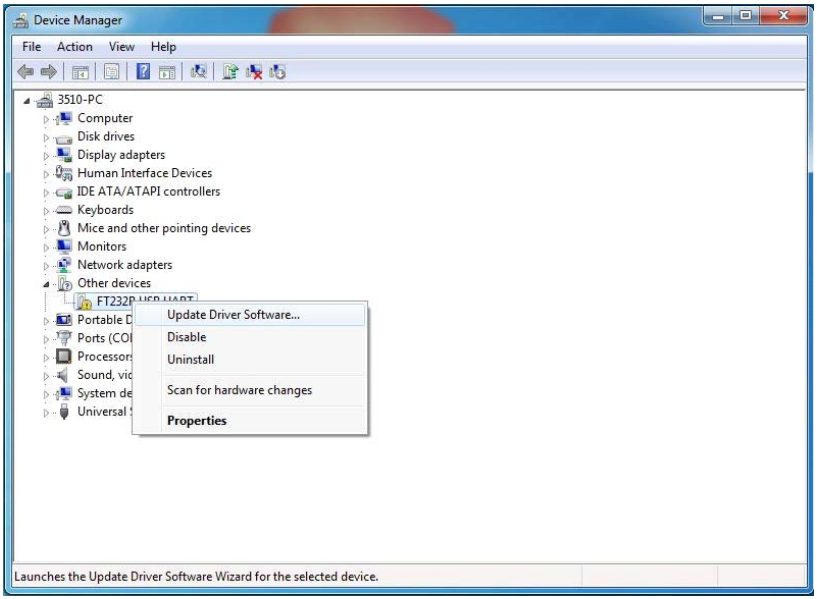
4. Navigate to the folder where you extracted the contents of the zip file and click “OK”. Click “Next” to install the driver.



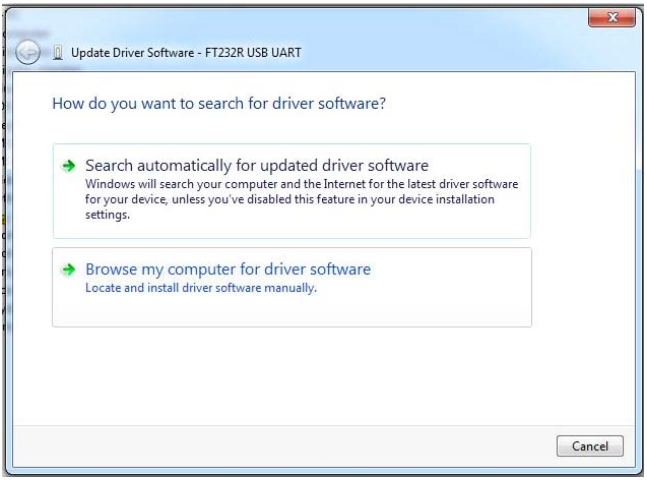
6.3 USB-to-Serial Converter Driver (RTM)

The COM5 serial port on the cPCI-R3P00(T) is converted from the USB3 port by a USB-to-serial converter (see " cPCI-R3P00 RTM" on page 17). To install the driver for the converter, follow the procedure below.

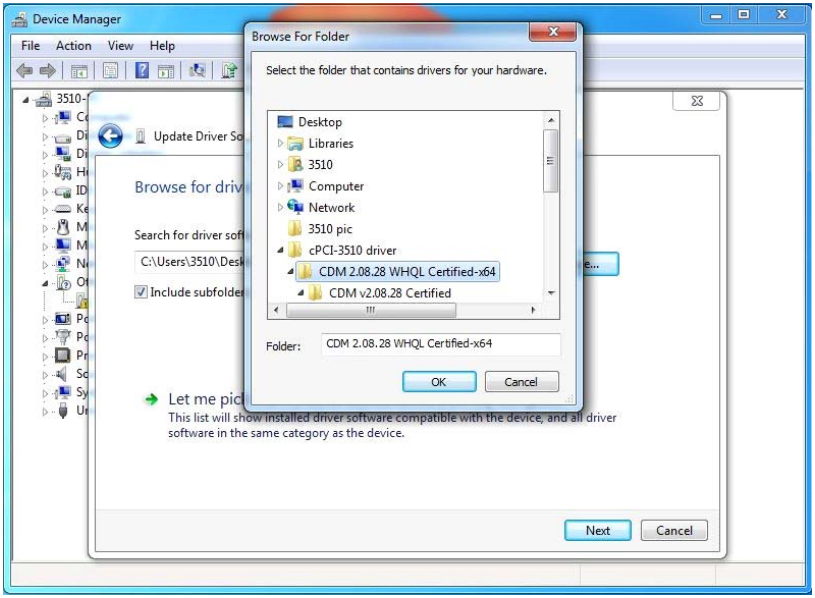
1. Extract the contents of **…\cPCI-3510\COM\CDM 2.08.28 WHQL Certified-x64.zip**.
2. Open the *Device Manager* and go to *Other Devices.* You will see a "question mark" next to *FT2332R USB UART.* R-click on *FT2332R USB UART* and choose "Update Driver Software…".



3. Click “Browse my computer for driver software”.



4. Navigate to the folder where you extracted the contents of the zip file and click “OK”. Click “Next” to install the driver



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7 Watchdog Timer

This section describes the operation of the cPCI-3510's watchdog timer (WDT). The primary function of the WDT is to monitor the cPCI-3510's operation and to reset the system if a software application fails to function as programmed. The following WDT functions may be controlled using a software application:

- enabling and disabling
- set and get current configuration
- reloading timeout value

The cPCI-3510 custom WDT functionality is implemented using an Intelligent Platform Management Controller (IPMC) and controlled using Intelligent Platform Management Interface (IPMI) commands.

7.1 Setting the Watchdog by IPMI Commands

The following section describes how to set the WDT functions using IPMI commands. For more detailed information about IPMI commands, please refer to IPMI specification: *Intelligent Platform Management Interface Specification Second Generation v2.0*.

WDT Commands

These commands enable the watchdog function, set the countdown period, and reload the timeout value periodically to keep it from resetting the system. If the timer countdown value is not reloaded, the watchdog resets the system hardware after the counter reaches zero.

Command	NetFn Code	Cmd Code
Reset Watchdog Timer	App (18h)	22h
Set Watchdog Timer	App (18h)	24h
Get Watchdog Timer	App (18h)	25h

Reset Watchdog Timer

This command is used to reload the WDT.

Action	Byte	Value	Description
Request	0	18h	NetFn/LUN
	1	22h	Defined command
Response	0	Complete Code	00h means OK

Set Watchdog Timer

This command is used to start and restart the Watchdog Timer using the specified countdown value.

Action	Byte	Value	Description
Request	0	18h	NetFn/LUN
	1	24h	Defined command
	2	[7] - 1b = don't log [6] - 1b = don't stop timer* [5:3] - reserved [2:0] - timer use 000b = reserved 001b = BIOS FRB2 010b = BIOS/POST 011b = OS Load 100b = SMS/OS 101b = OEM 110b -111b = reserved	Timer Use
	3	[7] - reserved [6:4] - pre-timeout interrupt 000b = none 001b = SMI (optional) 010b = NMI / Diagnostic Interrupt (optional) 011b = Messaging Interrupt 100b,111b = reserved [3] - reserved [2:0] - timeout action 000b = no action 001b = Hard Reset 010b = Power Down 011b = Power Cycle 100b,111b = reserved	Timer Actions

Action	Byte	Value	Description
Request	4	1h~ffh ('1h' based.)	Pre-timeout interval in seconds.
	5	[7] - reserved [6] - reserved [5] - OEM [4] - SMS/OS [3] - OS Load [2] - BIOS/POST [1] - BIOS FRB2 [0] - reserved 0b = leave alone 1b = clear timer use expiration bit	Timer Use Expiration flags clear
	6	00h~ffh ,LS byte (100 ms/ count)	Initial countdown value
	7	00h~ffh ,MS byte (100 ms/ count)	Initial countdown value
Response	0	Complete Code	00h means OK

***Note: don't stop timer:** If the WDT is already running, the countdown value will get set to the specified value and countdown will continue from that point. If timer is already stopped, it will remain stopped. If the pre-timeout interrupt bit is set, it will get cleared.

Get Watchdog Timer

This command is used to get the current WDT configuration.

Action	Byte	Value	Description
Request	0	18h	NetFn/LUN
	1	25h	Defined command
Response	0	Complete Code	00h means OK
	1	[7] - 1b = don't log [6] - 1b = don't stop timer [5:3] - reserved [2:0] - timer use 000b = reserved 001b = BIOS FRB2 010b = BIOS/POST 011b = OS Load 100b = SMS/OS 101b = OEM 110b -111b = reserved	Timer Use

Action	Byte	Value	Description
Response	2	[7] - reserved [6:4] - pre-timeout interrupt 000b = none 001b = SMI (optional) 010b = NMI / Diagnostic Interrupt (optional) 011b = Messaging Interrupt 100b,111b = reserved [3] - reserved [2:0] - timeout action 000b = no action 001b = Hard Reset 010b = Power Down 011b = Power Cycle 100b,111b = reserved	Timer Actions
	3	1h~ffh ('1h' based.)	Pre-timeout interval in seconds.
	4	[7] - reserved [6] - reserved [5] - OEM [4] - SMS/OS [3] - OS Load [2] - BIOS/POST [1] - BIOS FRB2 [0] - reserved 0b = leave alone 1b = clear timer use expiration bit	Timer Use Expiration flags clear
	5	00h~ffh ,LS byte (100 ms/ count)	Initial countdown value
	6	00h~ffh ,MS byte (100 ms/ count)	Initial countdown value
	7	00h~ffh ,LS byte (100 ms/ count)	Present countdown value
	8	00h~ffh ,MS byte (100 ms/ count)	Present countdown value

Example WDT Programming Procedure

Configuration of the watchdog timer is via serial interface. A detailed description of the WDT IPMI commands can be found above. The following example shows the procedure for configuring the WDT works over a serial console. See “Communications with IPMC” on page 129. for more information.

```
[18 00 24 43 01 01 08 50 00]          => Step 1: Set parameters to WDT
[1C 00 24 00]                         => Step 1: Response of setting OK.


[18 00 22]                            => Step 2: Trigger WDT
[1C 00 22 00]                         => Step 2: Response of trigger OK.


[18 00 25]                            => Get current configuration
[1C 00 25 00 43 01 01 00 50 00 28 00] => Response during WDT countdown

<A>: BMC Watchdog expired
<A>: Reset alert


[18 00 25]                            => Get current configuration
[1C 00 25 00 03 01 01 08 50 00 00 00 ] => Response after Reset
```

Figure 7-1: Example procedure for configuring the WDT over serial console

1. **Configure the WDT** by using the raw IPMI command "Set Watchdog Timer" described above.

```
"Set Watchdog Timer" Command:
[18 00 24 43 01 01 08 50 00]
Description:
0x18: Net function. Defined in IPMI specification
0x00: Bus ID. Usually "0x00".
0x24: Command. Defined in IPMI specification.
0x43: Set "Don’t stop timer" and "OS Load".
0x01: Hard Reset.
0x01: Pre-timeout interval in seconds.
0x08: Timer Use Expiration flags cleared by OS Load.
0x50: Initial countdown value. Sets the interval
   before watchdog timer expires.
   80 count: 100ms * 80 = 8000 ms = 8 seconds
Successful response to command:
[1C 00 24 00]
```

2. **Reload the WDT counter** by using the raw IPMI command "Reset Watchdog Timer".

"Reset Watchdog Timer" Command:
[18 00 22]
Successful response to Command:
[1C 00 22 00]

3. **Get the WDT configuration** by using the "Get Watchdog Timer" command.

"Get Watchdog Timer" Command:
[18 00 25]
Successful response to Command:
[1C 00 25 00 43 01 01 00 50 00 28 00]
0x18: Net function. Defined in IPMI specification
0x00: Bus ID. Usually "0x00".
0x25: Command. Defined in IPMI specification.
0x43: Get timer operation status and "OS Load".
The first nibble is "4". This means the timer is running. If the first nibble is "0", then the watchdog timer has timed out and stopped. The second nibble is "Timer Use". A value of "3" means the option is set to "OS Load".
0x01: Hard Reset.
0x01: Pre-timeout interval in seconds.
0x00: Timer Use Expiration flags clear.
0x50: Initial countdown value. The current interval before the watchdog timer expires.
80 count. 100ms * 80 = 8000ms = 8 seconds.
0x10: Present countdown value. How much time is left before timer expires.
16 count: 100ms * 16 = 1600ms = 1.6 seconds

8 BIOS Setup Utility

The following chapter describes basic navigation for the AMI EFI BIOS setup utility.

8.1 Starting the BIOS

To enter the setup screen, follow these steps:

1. Power on the motherboard
2. Press the < Delete > key on your keyboard when you see the following text prompt:
   < Press DEL to run Setup >
3. After you press the < Delete > key, the main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu.

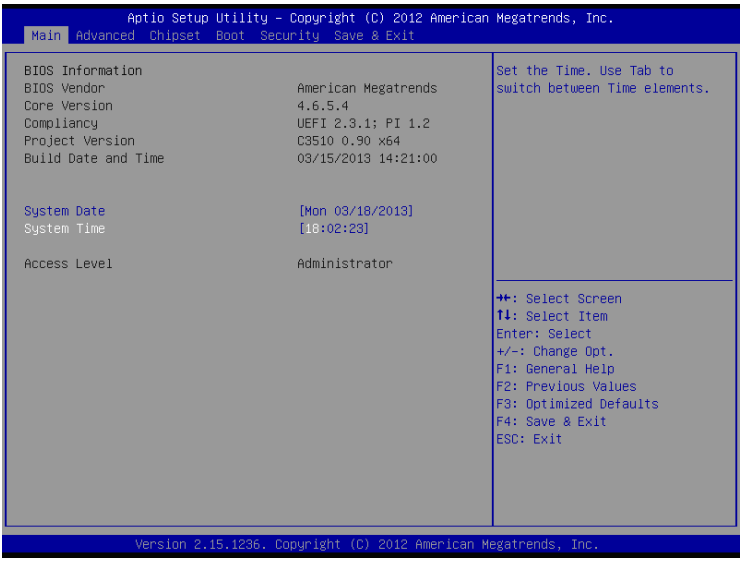
Note: In most cases, the < Delete > key is used to invoke the setup screen. There are several cases that use other keys, such as < F1 >, < F2 >, and so on.

Setup Menu

The main BIOS setup menu is the first screen that you can navigate. Each main BIOS setup menu option is described in this user's guide.

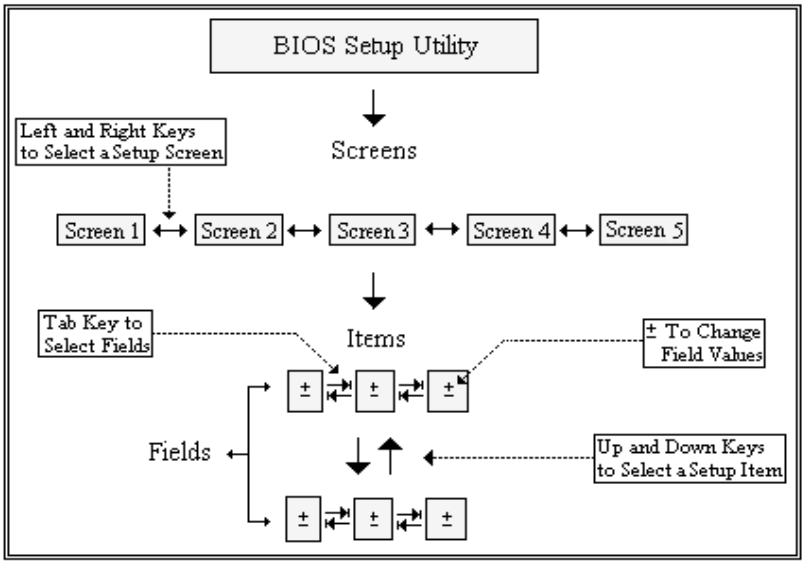
The Main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed" options cannot be configured, "Blue" options can be.

The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.



Navigation

The BIOS setup/utility uses a key-based navigation system called hot keys. Most of the BIOS setup utility hot keys can be used at any time during the setup navigation process.



NOTE:

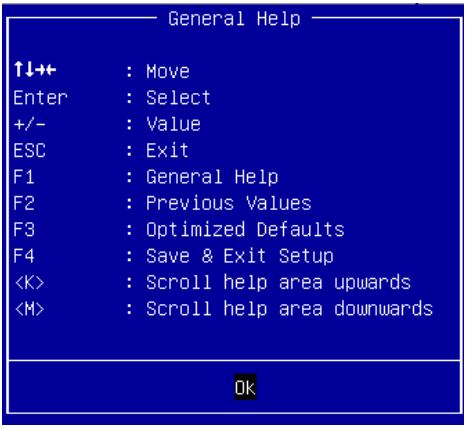
There is a hot key legend located in the right frame on most setup screens.

The < F8 > key on your keyboard is the Fail-Safe key. It is not displayed on the key legend by default. To set the Fail-Safe settings of the BIOS, press the < F8 > key on your keyboard. It is located on the upper row of a standard 101 keyboard. The Fail-Safe settings allow the motherboard to boot up with the least amount of options set. This can lessen the probability of conflicting settings.

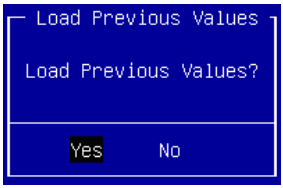
Hotkey Descriptions

Enter The < Enter > key allows you to display or change the setup option listed for a particular setup item. The < Enter > key can also allow you to display the setup sub-screens.

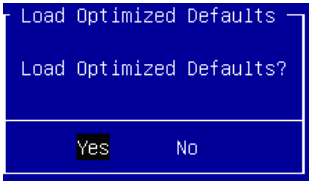
F1 The < F1 > key allows you to display the General Help screen. Press the < F1 > key to open the General Help screen.



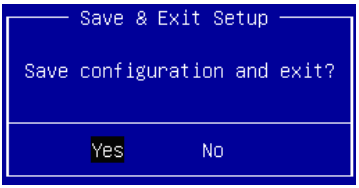
F2 The < F2 > key on your keyboard is the previous values key. It is not displayed on the key legend by default. To set the previous values settings of the BIOS, press the < F2 > key on your keyboard. It is located on the upper row of a standard 101 keyboard. The previous values settings allow the motherboard to boot up with the least amount of options set. This can lessen the probability of conflicting settings.



F3 The < F3 > key on your keyboard is the optimized defaults key. To set the optimized defaults settings of the BIOS, press the < F3 > key on your keyboard. It is located on the upper row of a standard 101 keyboard. The optimized defaults settings allow the motherboard to boot up with the optimized defaults of options set. This can lessen the probability of conflicting settings.

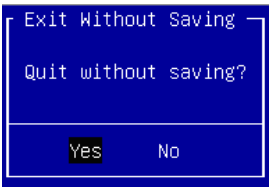


F4 The < F4 > key allows you to save any changes you have made and exit Setup. Press the < F10 > key to save your changes. The following screen will appear:



Press the < Enter > key to save the configuration and exit. You can also use the < Arrow > key to select Cancel and then press the < Enter > key to abort this function and return to the previous screen.

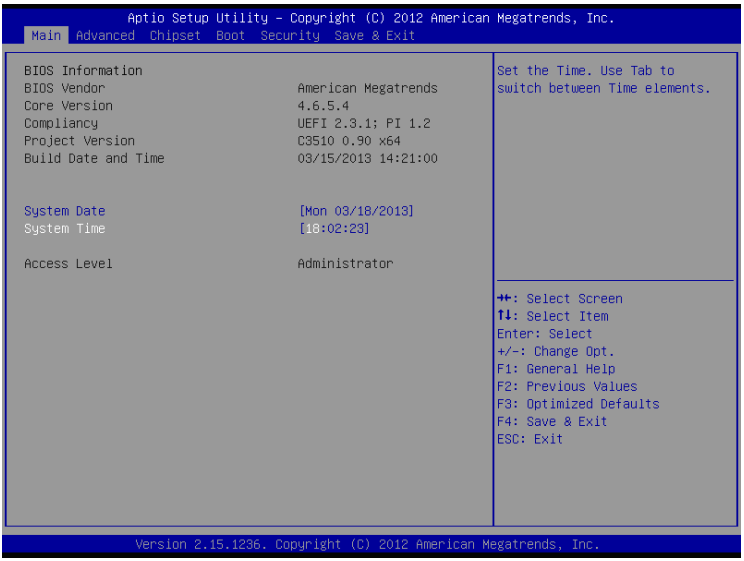
ESC The < Esc > key allows you to discard any changes you have made and exit the Setup. Press the < Esc > key to exit the setup without saving your changes. The following screen will appear:



Press the < Enter > key to discard changes and exit. You can also use the < Arrow > key to select Cancel and then press the < Enter > key to abort this function and return to the previous screen.

8.2 Main Setup

When you first enter the Setup Utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.



System & Board Info

The Main BIOS setup screen reports BIOS and Board version information.

System Time/System Date

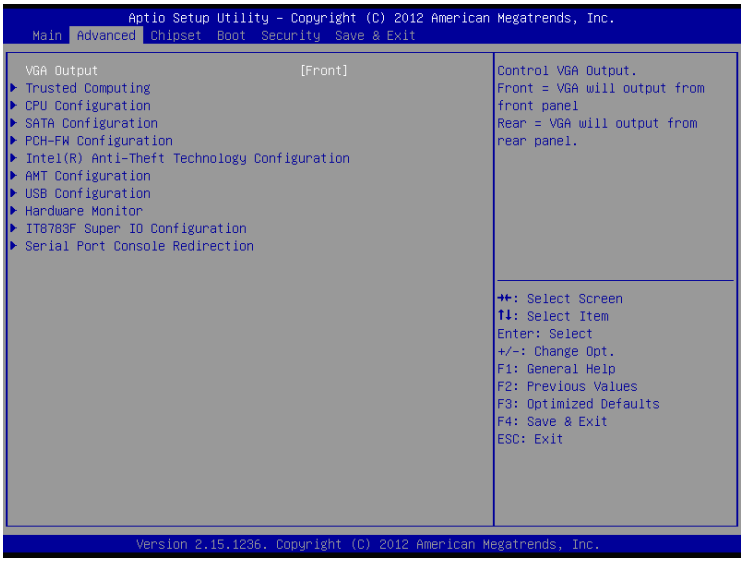
Use this option to change the system time and date. Highlight System Time or System Date using the < Arrow > keys. Enter new values using the keyboard. Press the < Tab > key or the < Arrow > keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

NOTE: The time is in 24-hour format. For example, 5:30 A.M. appears as 05:30:00, and 5:30 P.M. as 17:30:00.

8.3 Advanced BIOS Setup

Select the Advanced tab from the setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as SuperIO Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the < Arrow > keys. The Advanced BIOS Setup screen is shown below.

The sub menus are described on the following pages.



8.3.1 ACPI Settings

You can use this screen to select options for the ACPI Advanced Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on this page. The screen is shown below.

ACPI Sleep State

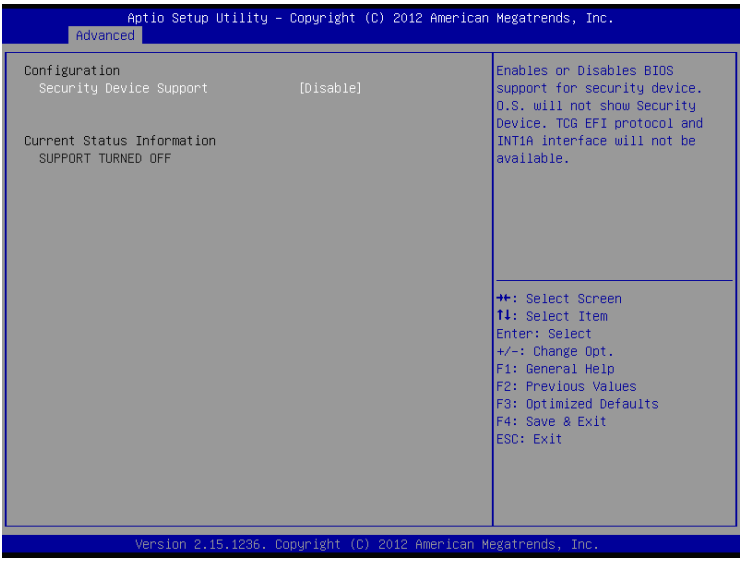
Select the highest ACPI sleep state the system will enter, when the SUSPEND button is pressed. Set this value to S1 only, Suspend Disable.

S1 only (CPU Stop Clock)

Power On Suspend - Under this setting the CPU is not executing instructions, all power resources that supply system level reference of S0 are off, system memory context is maintained, devices that reference power resources that are on are on, and devices that can wake-up the system can cause the CPU to continue to execute from where it left off.

8.3.2 Trusted Computing

Trusted Computing is an industry standard to make personal computers more secure through a dedicated hardware chip, called a Trusted Platform Module (TPM). This option allows you to enable or disable the TPM support.



Security Device Support

OS will not show TPM. Reset of platform is required. Set this value to Enabled/Disabled.

TPM State

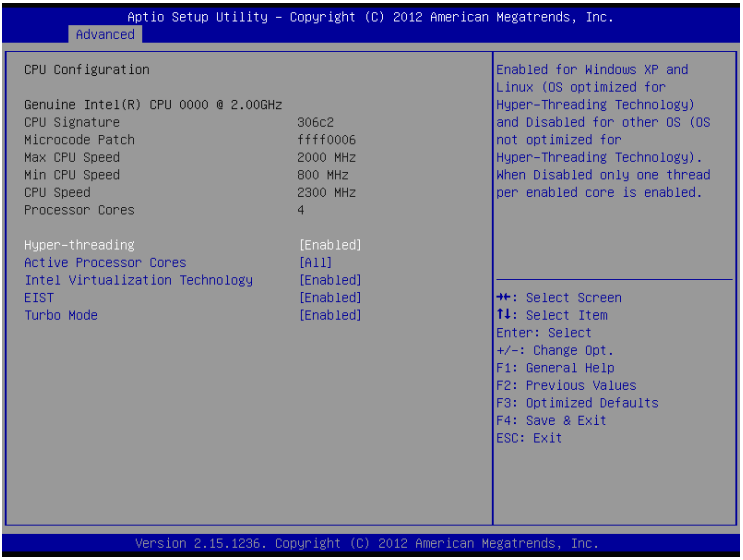
Determine whether TPM state change requires Password Authentication. Set this value to Enabled/Disabled.

Pending TPM operation

Schedule TPM operation. The settings for this value are Enable, Disable and Clear.

8.3.3 CPU Configuration

You can use this screen to select options for the CPU Configuration Settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option. A description of the selected item appears on the right side of the screen. The settings are described on the following pages. An example of the CPU Configuration screen is shown below.



Hyper-Threading

- **Enabled:** for Windows and Linux (OS optimized for Hyper-Threading Technology).
- **Disabled:** for other OS (OS not optimized for Hyper-Threading Technology).

Intel Virtualization Tech

When enabled, a VMM can utilize the additional hardware capability provided by Vanderpool Technology. Set this value to Enabled/Disabled.

EIST

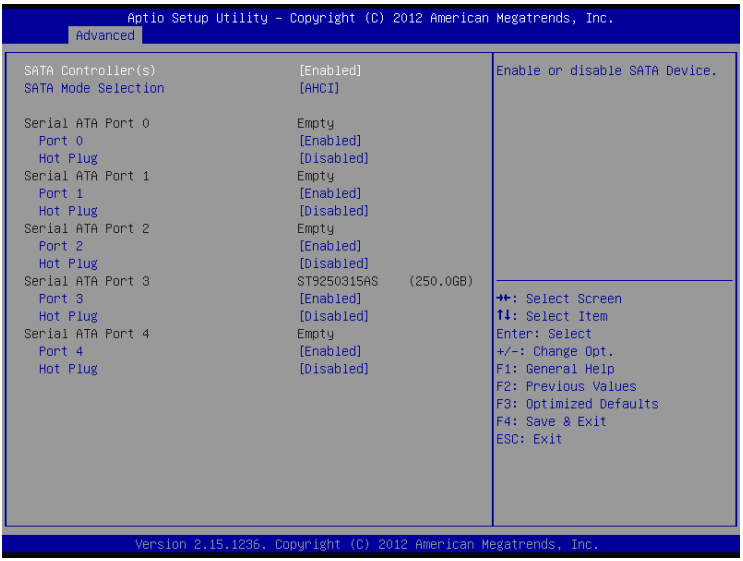
Set this value to Enabled/Disabled.

Turbo Mode

Set this value to Enabled/Disabled.

8.3.4 SATA Configuration

You can use this screen to select options for the SATA Configuration Settings. An example of the SATA Configuration screen is shown below.



SATA Controller(s)

Enable or disable SATA device.

SATA Mode Selection

The SATA can be configured as a legacy IDE, RAID and AHCI mode.

SATA Port 0~4

Display SATA device name string. Set this value to Enabled/Disabled.

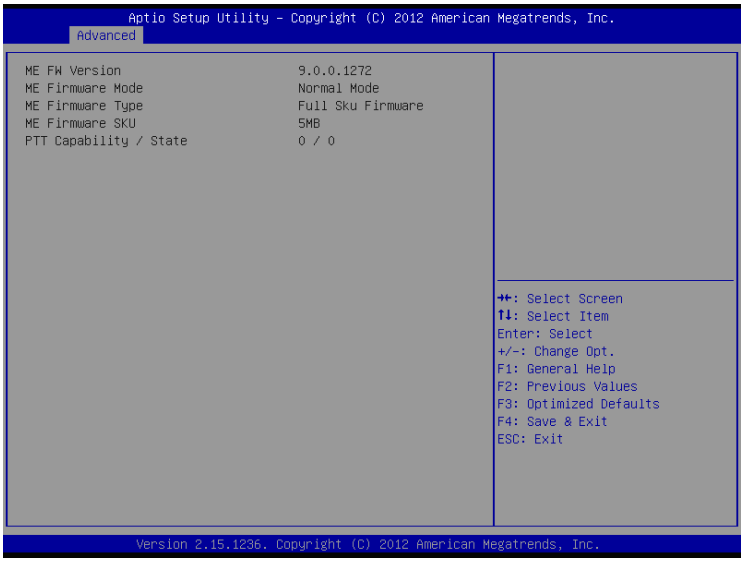
Hot Plug

Appears when SATA mode is AHCI. SATA port Hot Plug support. Set this value to Enabled/Disabled.

8.3.5 PCH-FW Configuration

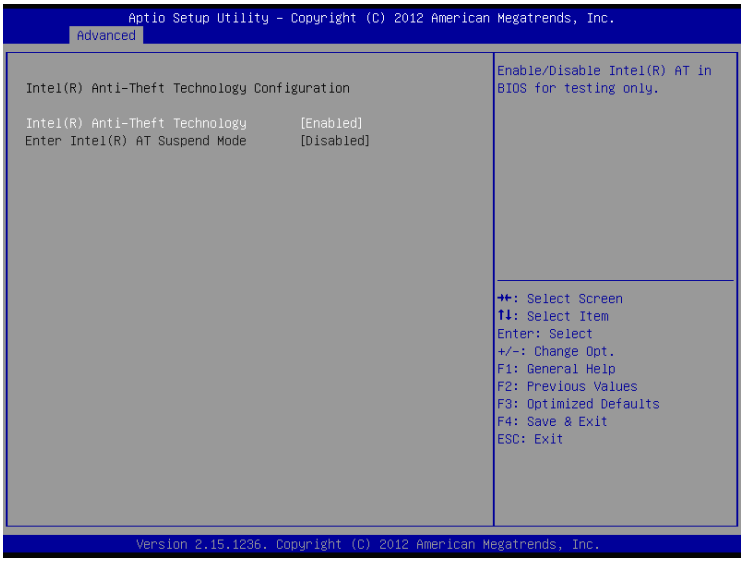
Intel TXT(LT) Configuration

You can use this screen to view ME related information. For example, ME FW Version, ME Firmware Mode, ME Firmware Type, ME Firmware SKU..etc. An example of the ME screen is shown below.



8.3.6 Intel ® Anti-Theft Technology Configuration

You can use this screen to select options for the Intel AT Configuration Settings. An example of the Intel AT Configuration screen is shown below.

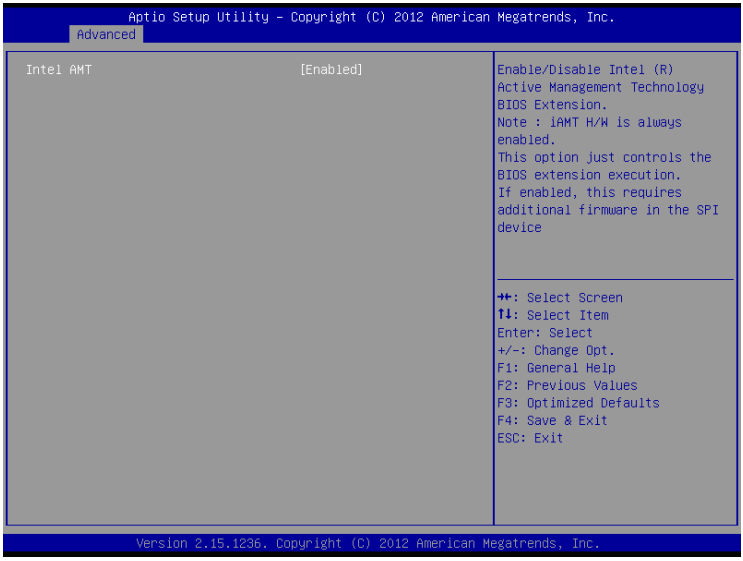


Intel® Anti-Theft Support

Set this value is Enable/Disable.

8.3.7 AMT Configuration

You can use this screen to select options for the AMT settings. Use the up and down < Arrow > keys to select an item. Use the < + > and < - > keys to change the value of the selected option.

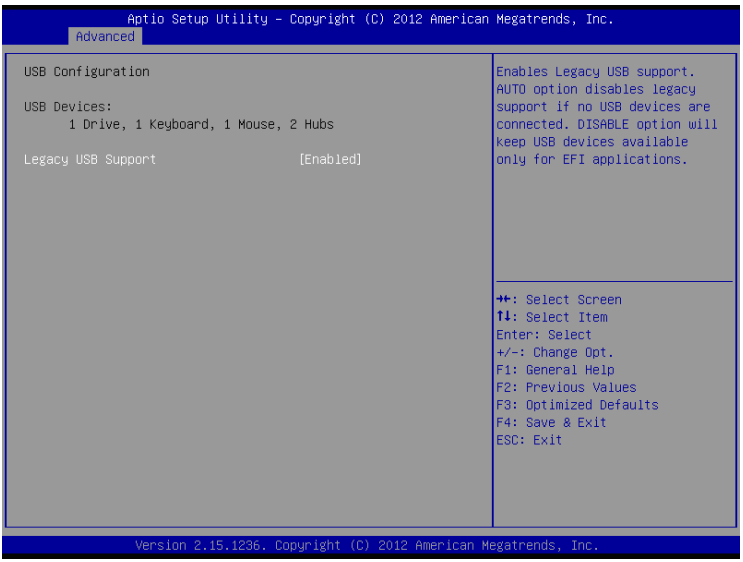


Intel AMT

Intel AMT feature. Set this value to Enabled/Disabled.

8.3.8 USB Configuration

You can use this screen to select options for the USB Configuration. Use the up and down < Arrow > keys to select an item. The screen is shown below.

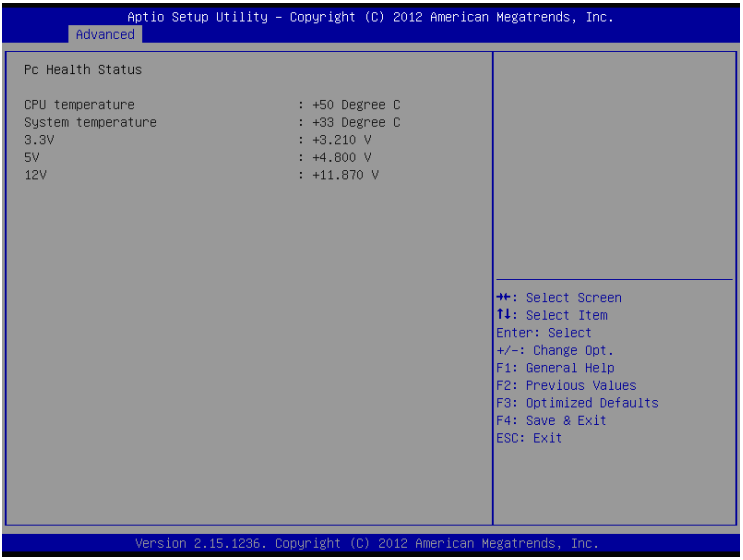


Legacy USB Support

Enables legacy USB support. Auto option disables legacy support if no USB devices are connected. Disable option will keep USB devices available only for EFI applications. Set this value to Enabled/Disabled/Auto.

8.3.9 Hardware Monitor

This option displays the current status of all of the monitored hardware devices/components such as voltages and temperatures.



CPU Temperature

Displays current CPU temperature.

System Temperature

Displays current system temperature.

3.3V

Displays current system 3.3V voltage.

5V

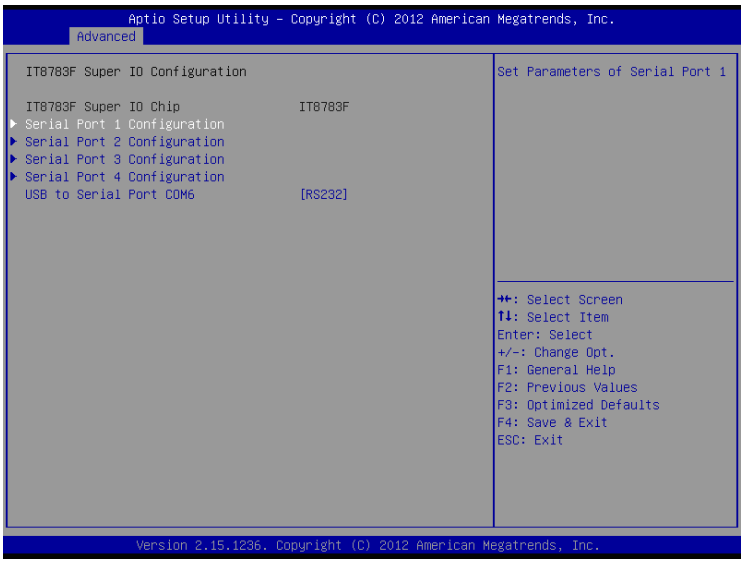
Displays current system 5V voltage.

12V

Displays current system 12V voltage.

8.3.10 Super IO Configuration

You can use this screen to select options for the Super IO Configuration settings.



Serial Port 1,2,3,4 Configuration

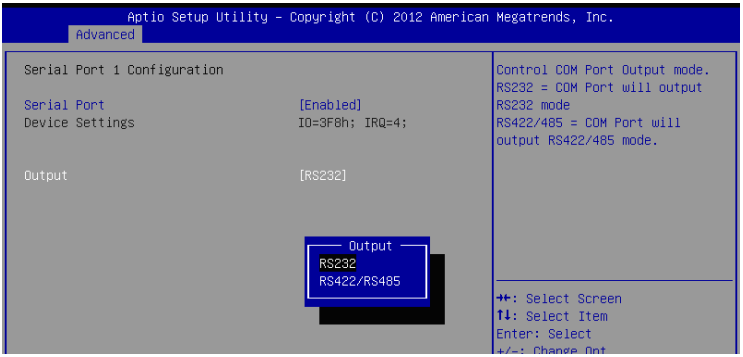
Set Parameters of Serial Port 1,2,3,4 (COM 1,2,3,4).
COM1/2: front panel; COM3: IPMI interface; COM4: RTM.

Serial Port

Enable/Disable serial port 1,2,3,4 (COM1,2,3,4). Set this value to Enable or Disable.

Output (cPCI-3510G/T COM1/2)

Set the mode of serial port 1,2,(COM1,2). Set this value to RS232 or RS422/RS485..



NOTE:

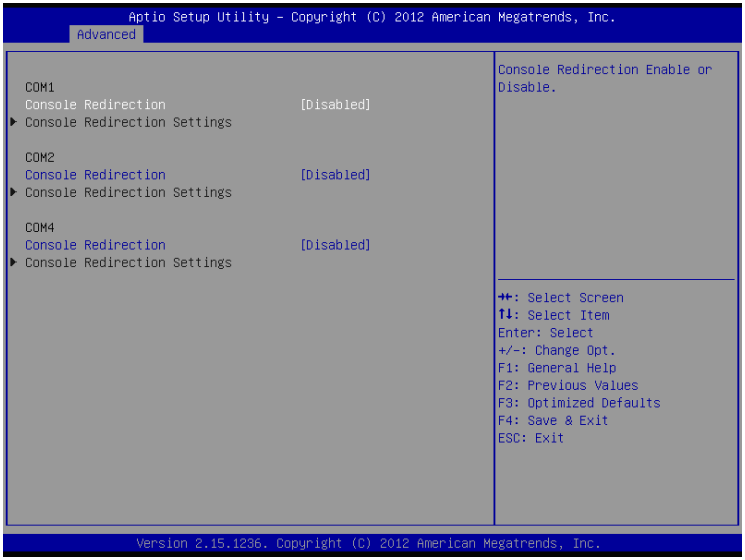
The cPCI-3510G/T COM1/2 Output BIOS setting is only used for cPCI-3510G/T models. The COM mode setting for cPCI-3510D/P models must be set using the *"COM1 Mode Selection Switches (SW1~SW4)" on page 43.*

USB to Serial Port

Set the mode of COM5 on the cPCI-R3P00(T) RTM. Options: RS232 and RS422/RS485 ("COM6" will be corrected to "COM5" in the next BIOS revision).

8.3.11 Console Redirection

You can use this screen to select options for the serial port console redirection settings. An example of the Serial Port Console Redirection screen is shown below.

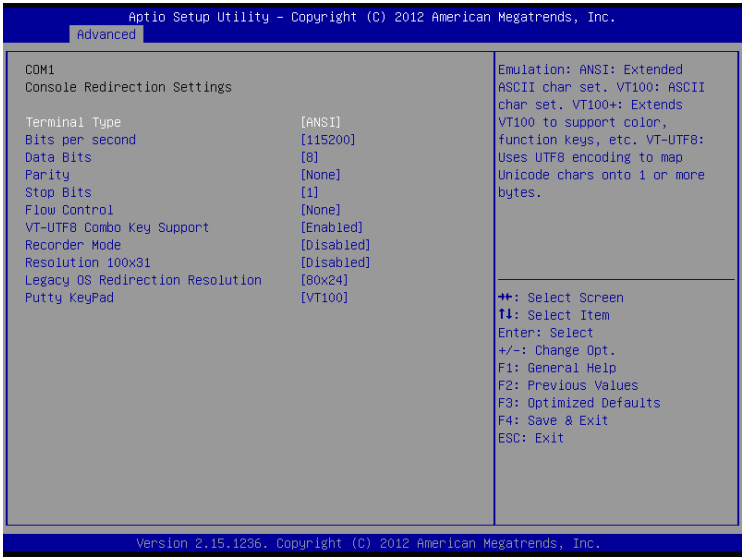


Console Redirection

Set this value to Enabled/Disabled.

Console Redirection Settings

The settings specify how the host computer and the remote computer will exchange data. Both computers should have the same or compatible settings. The screen is shown below.



Terminal Type

VT100+ is the preferred terminal type for out-of-band management. Configuration options: VT100, VT100+, VT-UTF8, ANSI.

Bits per second

Select the bits per second you want the serial port to use for console redirection. The options are 115200, 57600, 38400, 19200, 9600.

Data Bits

Select the data bits you want the serial port to use for console redirection. Set this value to 7, 8.

Parity

Set this option to select Parity for console redirection. The settings for this value are None, Even, Odd, Mark, Space.

Stop Bits

Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning). The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit. Set this value to 1 and 2.

Flow Control

Set this option to select Flow Control for console redirection. The settings for this value are None, Hardware RTS/CTS.

VT-UTF8 Combo Key Support

Enables VT-UTF8 combination key support for ANSI/VT100 terminals.Set this value to Enabled/Disabled.

Recorder Mode

When this mode is enabled, only text will be sent. This is to capture terminal data. Set this value to Enabled/Disabled.

Resolution 100x31

Set this option to extended terminal resolution. Set this value to Enabled/Disabled.

Legacy OS Redirection

On legacy OS, the number of rows and columns supported for redirection. Set this value to 80x24, 80x25.

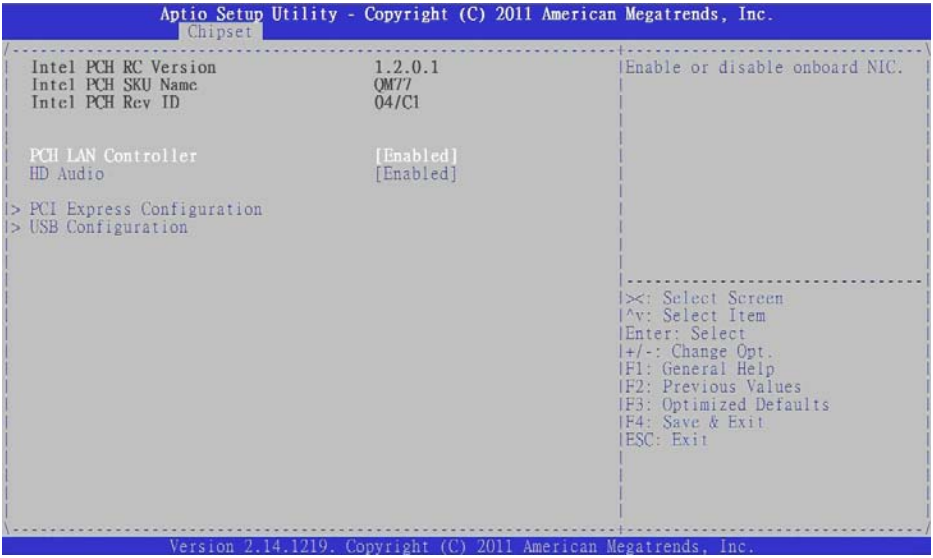
Putty Key Pad

Select FunctionKey and KeyPad on Putty. Set this value to VT100, LINUX, XTERMR6, SCO, ESCN, VT400.

8.4 Chipset Setup

Select the Chipset tab from the setup screen to enter the Chipset BIOS Setup screen. You can select any of Chipset BIOS Setup options by highlighting it using the < Arrow > keys. The Chipset BIOS Setup screen is shown below.

8.4.1 PCH-IO Configuration



PCH LAN Controller

Enable or disable onchip NIC. Set this value to Enabled/Disabled

HD Audio

Enable or disable the onboard HDA controller. Set this value to Enabled/Disabled.

PCI Express Configuration

PCI Express Clock Gating

Enable or disable XHCI Pre-Boot Driver support. Set this value to Enabled/Disabled.

DMI Link ASPM Control

Mode of operation of xHCI controller. Set this value to Enabled/Disabled.

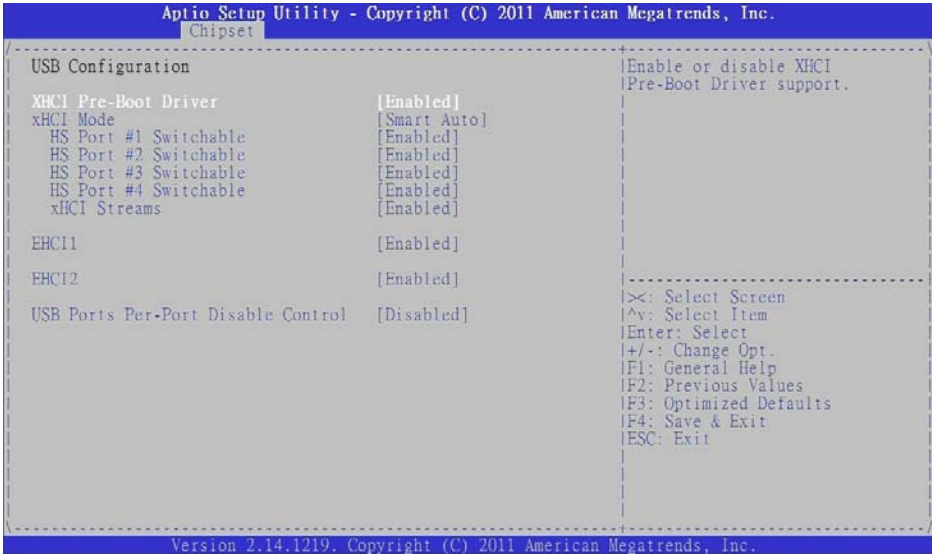
Subtractive Decode

Mode of operation of xHCI controller. Set this value to Enabled/Disabled.

PCI Express Root Port 2~5

Control the PCI Express Root Ports 2~5

USB Configuration



XHCI Pre-Boot Driver

Enable or disable XHCI Pre-Boot Driver support. Set this value to Enabled/Disabled.

XHCI Mode

Mode of operation of xHCI controller. Set this value to Enabled/Disabled.

HS Port #1/2/3/4 Switchable

Allows for HS port switching between xHCI and EHCI. If disabled, port is routed to EHCI. If HS port is routed to xHCI, the corresponding SS port is enabled. Set this value to Enabled/Disabled.

xHCI Stream

Enable or disable xHCI Maximum Primary Stream Array Size. Set this value to Enabled/Disabled.

EHCI1/2

Control the USB EHCI (USB 2.0) functions. One EHCI controller must always be enabled. Set this value to Enabled/Disabled.

USB Ports Per-Port Disable Control

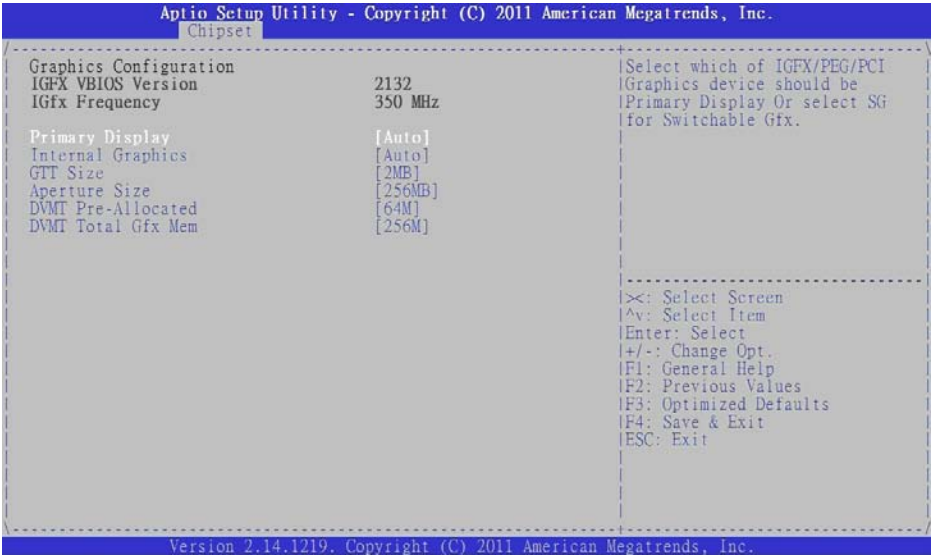
Control the per-port disabling of USB ports 0~13. Set this value to Enabled/Disabled.

8.4.2 System Agent (SA) Configuration

VT-d

The Intel Virtualization Technology for Directed I/O. Set this value to Enabled/Disabled.

Graphics Configuration



Primary Display

Select which graphics device should be the primary display. Set this value to Auto, IGFX, PCI.

Internal Graphics

Keep IGD enabled based on the setup options. Set this value to Auto, Enabled, Disabled.

GTT Size

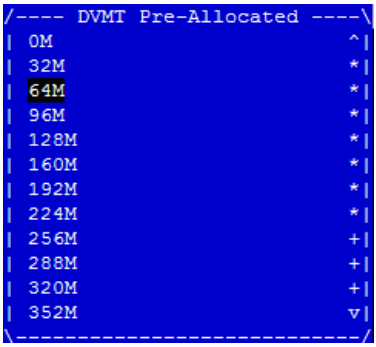
Select the GTT size. Set this value to 1MB, 2MB.

Aperture Size

Select the aperture size. Set this value to 128MB, 256MB, 512MB.

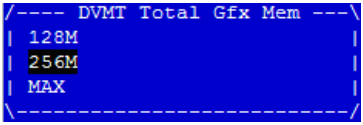
DVMT Pre-Allocated

Select DVMT 5.0 Pre-Allocated (fixed) graphics memory size used by the internal graphics device. Configuration options as below:

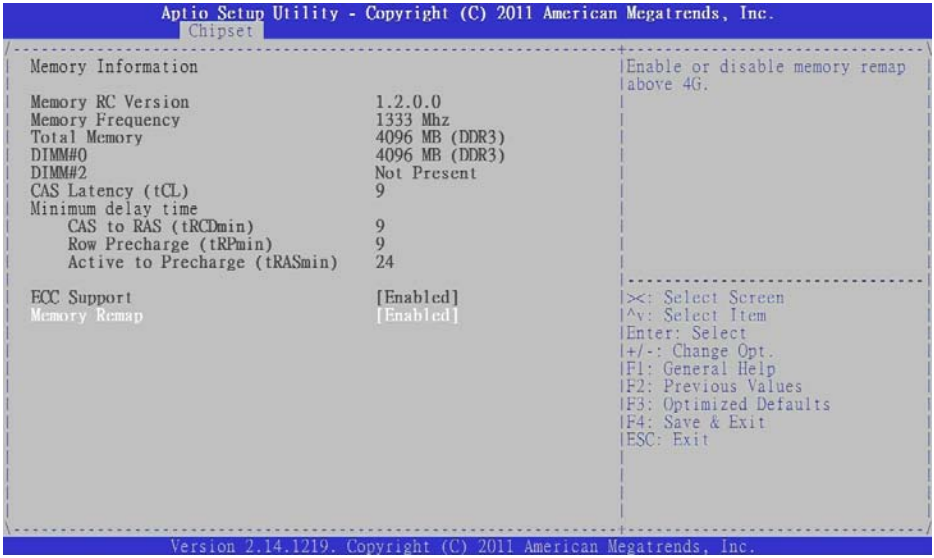


DVMT Total Gfx Memory

Select DVMT 5.0 total graphic memory size used by the internal graphics device. Configuration options as below:



Memory Configuration

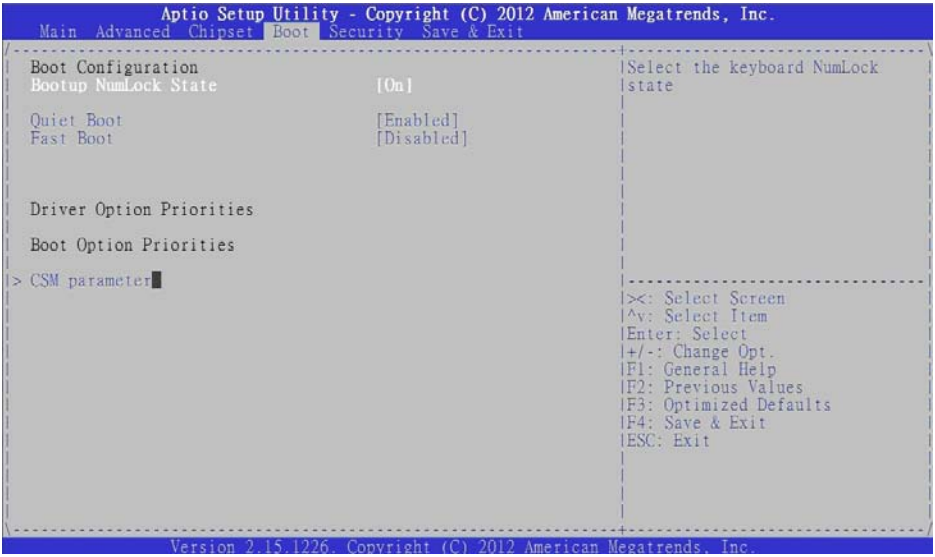


Memory Remap

Enable or disable memory remap above 4G. Set this value to Enabled/Disabled.

8.5 Boot Settings

Select the Boot tab from the setup screen to enter the Boot BIOS Setup screen. You can select any of the items in the left frame of the screen, such as Boot Device Priority, to go to the sub menu for that item. You can display a Boot BIOS Setup option by highlighting it using the < Arrow > keys. The Boot Settings screen is shown below:



Quiet Boot

- **Disabled** - Set this value to allow the computer system to display the POST messages.
- **Enabled** - Set this value to allow the computer system to display the OEM logo.

Fast Boot

Enables or disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options. Set this value to Enabled/Disabled.

Set Boot Priority

Set Boot Option #1 ~2 boot priority.

Hard Disk Drive BBS Priorities

Specifies the boot device priority sequence from available hard drives.

8.5.1 CSM Parameter

OpROM execution, boot option filter, etc.

Launch CSM

This option controls if CSM will be launched. Set this value to Always, Never.

Boot option filter

This option controls what devices system can boot to. Set this value to UEFI and Legacy, Legacy only, UEFI only.

Launch PXE OpROM policy

This option controls the execution of UEFI and Legacy PXE OpROM. Set this value to Do not launch, Legacy only.

Launch Storage OpROM policy

This option controls the execution of UEFI and Legacy Storage OpROM. Set this value to Do not launch, UEFI only, Legacy only.

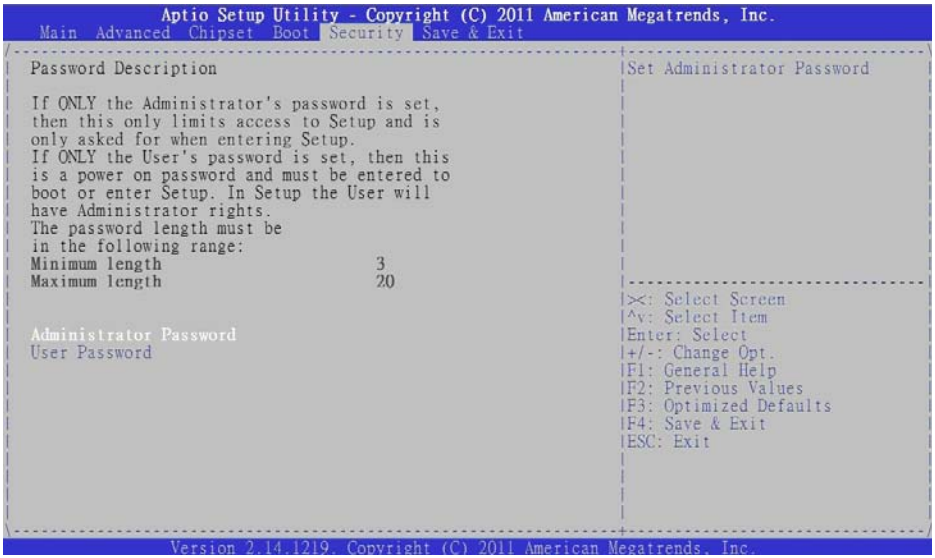
Launch Video OpROM policy

This option controls the execution of UEFI and Legacy Video OpROM. Set this value to Do not launch, UEFI only, Legacy only.

Other PCI device ROM priority

For PCI devices other than Network, Mass storage or Video defines which OpROM to launch. Set this value to UEFI OpROM, Legacy OpROM.

8.6 Security Setup



Administrator, User Password

If only the administrator's password is set, then this only limits access to setup and is only asked for when entering setup.

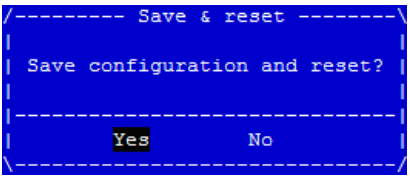
If only the user's password is set, then this is a power on password and must be entered to boot or enter setup. In setup the user will have administrator rights.

8.7 Save & Exit Menu

Select the Save & Exit tab from the setup screen to enter the Save & Exit BIOS Setup screen. You can display an Exit BIOS Setup option by highlighting it using the < Arrow > keys. The Save & Exit BIOS Setup screen is shown below.

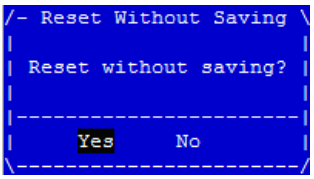
Save Changes and Reset

Reset the system after saving the changes.



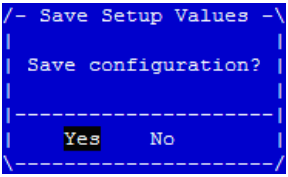
Discard Changes and Reset

Reset system setup without saving any changes.



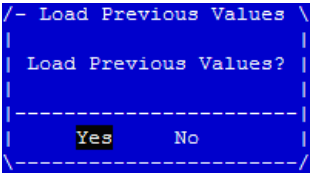
Save Changes

Save changes done so far to any of the setup options.



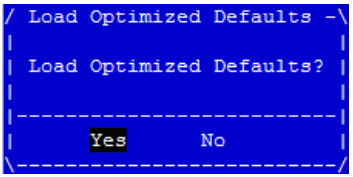
Discard Changes

Discard changes done so far to any of the setup options.



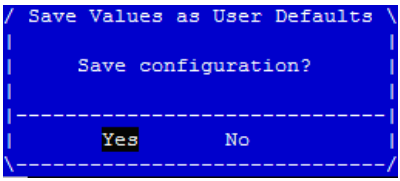
Restore Changes

Restore/Load Defaults values for all the setup options.



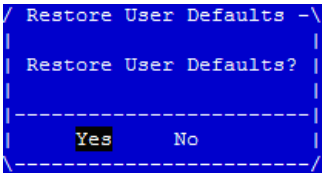
Save as User Defaults

Save the changes done so far as user defaults..



Restore User Defaults

Save changes done so far to any of the setup options.



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9 IPMI User Guide

9.1 Introduction

This chapter is written for those who already have a basic understanding of the newest implementation of the baseboard management controller (BMC) of the Intelligent Platform Management Interface (IPMI) specification rev. 1.5. It also describes the OEM extension IPMI command usages which are not listed in the IPMI specification.

9.2 Summary of Commands Supported by BMR-AVR-cPCI

The table below lists all the commands supported by the BMR-AVR-cPCI. The rightmost column indicates if the command is required by PICMG 3.0/ PICMG 2.9, or is optional.

Command	IPMI Spec	NetFn	CMD	IPM Controller Req (PICMG 2.9)
IPM Device "Global" Commands				
Get Device ID	17.1	App	01h	Mandatory
Cold Reset	17.2	App	02h	Optional
Warm Reset	17.3	App	03h	Optional
Get Self Test Results	17.4	App	04h	Mandatory
Get Device GUID	17.8	App	08h	Optional
Broadcast "Get Device ID"	17.9	App	01h	Mandatory
IPMI Messaging Support Commands				
Send Message	18.7	App	34h	Optional
BMC Watchdog Timer				
Reset Watchdog Timer	21.5	App	22h	Optional
Set Watchdog Timer	21.6	App	24h	Optional
Get Watchdog Timer	21.7	App	25h	Optional
Event Commands				
Set Event Receiver	23.1	S/E	00h	Optional
Get Event Receiver	23.2	S/E	01h	Optional

Command	IPMI Spec	NetFn	CMD	IPM Controller Req (PICMG 2.9)
Platform Event (a.k.a. “Event Message”)	23.3	S/E	02h	Optional
Sensor Device Commands				
Get Device SDR Info	29.2	S/E	20h	Optional
Get Device SDR	29.3	S/E	21h	Optional
Reserve Device SDR Repository	29.4	S/E	22h	Optional
Set Sensor Hysteresis	29.6	S/E	24h	Optional
Get Sensor Hysteresis	29.7	S/E	25h	Optional
Set Sensor Threshold	29.8	S/E	26h	Optional
Get Sensor Threshold	29.9	S/E	27h	Optional
Set Sensor Event Enable	29.10	S/E	28h	Optional
Get Sensor Event Enable	29.11	S/E	29h	Optional
Get Sensor Event Status	29.13	S/E	2Bh	Optional
Get Sensor Reading	29.14	S/E	2Dh	Optional
Get Sensor Type	29.16	S/E	2Fh	Optional
FRU Device Commands				
Get FRU Inventory Area Info	28.1	Storage	10h	Optional
Read FRU Data	28.2	Storage	11h	Optional
Write FRU Data	28.3	Storage	12h	Optional

9.3 OEM Commands Summary Table

Command	NetFn Code	Cmd Code
OemShowRevision	OEM (C0h)	12h
OemRescanGaInput	OEM (C0h)	22h
OemTestFunction	OEM (C0h)	30h
OemReportGeoAddress	OEM (C0h)	F0h
OemEnableSmbus	OEM (C0h)	F2h
OemDisableSmbus	OEM (C0h)	F3h
OemDispDebugVariable	OEM (C0h)	F4h
OemResetHost	OEM (C0h)	F5h
OemPowerOff	OEM (C0h)	F6h
OemPowerOn	OEM (C0h)	F7h

OemShowRevision

This command is used to show the current information of the firmware including the firmware revision, the product ID, and additional features.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	12h	OEM defined command
Response	0	Complete Code	00h means OK
	1	A5h	Internal check byte. Always A5h
	2	Firmware Rev	‘V’ in ASCII code for verification
	3	Firmware Rev	Revision info high byte
	4	Firmware Rev	Revision info low byte
	5	Product ID	‘P’ in ASCII code for verification
	6	Product ID	Product info high byte
	7	Product ID	Product info low byte
	8	Special info	‘S’ in ASCII code for verification
	9	Special info	Addition info byte
	10	5Ah	Internal check byte. Always 5Ah

OemRescanGaInput

This command is used to rescan the geo-address input pins and reset the IPMB address according to the input value.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	22h	OEM defined command
Response	0	Complete Code	00h means OK
	1	New IPMB address	New IPMB address value

OemTestFunction

Internal test purposes only.

OemReportGeoAddress

This command can report the IPMB address, the GA pin input status, and the event forwarding control value.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F0h	OEM defined command
Response	0	Complete Code	00h means OK
	1	IPMB address	IPMB address value
	2	GA value	GA pin input status
	3	Control value	Current control value of event forwarding

OemEnableSmbus

This command is used to turn on the I2C bus when it is off during boot up process. Usually BIOS will perform this command after booting in boards with ServerWorks chipset.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F2h	OEM defined command
Response	0	Complete Code	00h means OK

OemDisableSmbus

This command is used to shut down I2C bus access.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F3h	OEM defined command
Response	0	Complete Code	00h means OK

OemDispDebugVariable

This command can report up to 5 interval values for debug purposes. For developers only.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F4h	OEM defined command
Response	0	Complete Code	00h means OK
	1	*Debug variable 1	
	2	*Debug variable 2	
	3	*Debug variable 3	
	4	*Debug variable 4	
	5	*Debug variable 5	


NOTE:

*Reserved for customized IPMI debugging purposes. Contact your ADLINK representative for details.

OemResetHost

This command is implemented to control the system's status if rebooting is required. Operators can control the system remotely.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F5h	OEM defined command
Response	0	Complete Code	00h means OK

OemPowerOff

This command is implemented to control the system's status if power-off is required. Operators can control the system remotely.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F6h	OEM defined command
Response	0	Complete Code	00h means OK

OemPowerOn

This command is implemented to control the system's status if power-on is required. Operators can control the system remotely.

Action	Byte	Value	Description
Request	0	C0h	NetFn/LUN for OEM
	1	F7h	OEM defined command
Response	0	Complete Code	00h means OK

9.4 CompactPCI Address Map

Since more than one system may be installed in a single chassis, we allocate each IPMB address based on GA input as peripheral cards. The CompactPCI Peripheral Address Mapping Table is given below.

CompactPCI Peripheral Address Mapping			
Geo. Addr.	**IPMB Addr.**	**Geo. Addr.**	**IPMB Addr.**
0	**Disabled**	16	D0h
1	B0h	17	D2h
2	B2h	18	D4h
3	B4h	19	D6h
4	B6h	20	D8h
5	B8h	21	DAh
6	Bah	22	DCh

CompactPCI Peripheral Address Mapping			
Geo. Addr.	**IPMB Addr.**	**Geo. Addr.**	**IPMB Addr.**
7	BCh	23	DEh
8	BEh	24	E0h
9	Coh	25	E2h
10	C4h	26	E4h
11	C6h	27	E6h
12	C8h	28	E8h
13	CAh	29	EAh
14	CCh	30	ECh
15	CEh	**31**	**Disabled**

9.5 Communications with IPMC

Operating systems need to use a serial port to communicate with the IPMC. The resource setting of the serial port must be IO: 0x2E0 and IRQ:7. The communication setting of the serial port must be BaudRate: 9600, DataBit: 8, ParityCheck: None, StopBit: 1, and FlowControl: None. In Windows XP, use “COM3” to communicate with the IPMC.

9.6 IPMI Sensors List

Sensor Number	Sensor name	Normal Reading	Remark
00h	BMC Watchdog		
01h	3.3V	3.3 V	
02h	5V	5 V	
03h	12V	12 V	
04h	CPU Temp	40°C	
05h	System Temp	25°C	
06h	P_CPU_VCORE	1.8 V	
07h	P_CPU_VTT	1.5 V	
08h	P_CPU_VSA	1.5 V	

Sensor Number	Sensor name	Normal Reading	Remark
09h	P_CPU_VDD	1.5 V	
0ah	P1V8_BG	1.8 V	
0bh	P1V5_SSB	1.5 V	
0ch	P1V1_SSB	1.1 V	

9.7 Relevant Documents

Document Title	Revision	Source
Intelligent Platform Management Interface Specification v1.5	Document Revision 1.1 February 20, 2002	Intel Corp. http://www.intel.com/design/servers/ipmi/license_ipmi.htm
PICMG 2.9 D1.0 CompactPCI System Management Specification	January 21, 2000	
Intelligent Platform Management Bus Communications Protocol Specification v0.9	Document Revision 0.15 June 24, 1997	Intel Corp. http://www.intel.com/design/servers/ipmi/license_ipmi.htm

Important Safety Instructions

For user safety, please read and follow all **instructions**, **WARNINGS**, **CAUTIONS,** and **NOTES** marked in this manual and on the associated equipment before handling/operating the equipment.

- Read these safety instructions carefully.
- Keep this user's manual for future reference.
- Read the specifications section of this manual for detailed information on the operating environment of this equipment.
- When installing/mounting or uninstalling/removing equipment:
  - Turn off power and unplug any power cords/cables.
- To avoid electrical shock and/or damage to equipment:
  - Keep equipment away from water or liquid sources;
  - Keep equipment away from high heat or high humidity;
  - Keep equipment properly ventilated (do not block or cover ventilation openings);
  - Make sure to use recommended voltage and power source settings;
  - Always install and operate equipment near an easily accessible electrical socket-outlet;
  - Secure the power cord (do not place any object on/over the power cord);
  - Only install/attach and operate equipment on stable surfaces and/or recommended mountings; and,
  - If the equipment will not be used for long periods of time, turn off and unplug the equipment from its power source.

- Never attempt to fix the equipment. Equipment should only be serviced by qualified personnel.

A Lithium-type battery may be provided for uninterrupted, backup or emergency power.

Risk of explosion if battery is replaced with one of an incorrect type. Dispose of used batteries appropriately.

- Equipment must be serviced by authorized technicians when:
  - The power cord or plug is damaged;
  - Liquid has penetrated the equipment;
  - It has been exposed to high humidity/moisture;
  - It is not functioning or does not function according to the user's manual;
  - It has been dropped and/or damaged; and/or,
  - It has an obvious sign of breakage.

Getting Service

Contact us should you require any service or assistance.

ADLINK Technology, Inc.
Address: 9F, No.166 Jian Yi Road, Zhonghe District
New Taipei City 235, Taiwan
新北市中和區建一路 166 號 9 樓
Tel: +886-2-8226-5877
Fax: +886-2-8226-5717
Email: service@adlinktech.com

Ampro ADLINK Technology, Inc.
Address: 5215 Hellyer Avenue, #110
San Jose, CA 95138, USA
Tel: +1-408-360-0200
Toll Free: +1-800-966-5200 (USA only)
Fax: +1-408-360-0222
Email: info@adlinktech.com

ADLINK Technology (China) Co., Ltd.
Address: 上海市浦东新区张江高科技园区芳春路 300 号 (201203)
300 Fang Chun Rd., Zhangjiang Hi-Tech Park
Pudong New Area, Shanghai, 201203 China
Tel: +86-21-5132-8988
Fax: +86-21-5132-3588
Email: market@adlinktech.com

ADLINK Technology Beijing
Address: 北京市海淀区上地东路 1 号盈创动力大厦 E 座 801 室(100085)
Rm. 801, Power Creative E, No. 1 Shang Di East Rd.
Beijing, 100085 China
Tel: +86-10-5885-8666
Fax: +86-10-5885-8626
Email: market@adlinktech.com

ADLINK Technology Shenzhen
Address: 深圳市南山区科技园南区高新南七道 数字技术园
A1 栋 2 楼 C 区 (518057)
2F, C Block, Bldg. A1, Cyber-Tech Zone, Gao Xin Ave. Sec. 7
High-Tech Industrial Park S., Shenzhen, 518054 China
Tel: +86-755-2643-4858
Fax: +86-755-2664-6353
Email: market@adlinktech.com

LiPPERT ADLINK Technology GmbH
Address: Hans-Thoma-Strasse 11, D-68163
Mannheim, Germany
Tel: +49-621-43214-0
Fax: +49-621 43214-30
Email: emea@adlinktech.com

ADLINK Technology, Inc. (French Liaison Office)
Address: 6 allée de Londres, Immeuble Ceylan
91940 Les Ulis, France
Tel: +33 (0) 1 60 12 35 66
Fax: +33 (0) 1 60 12 35 66
Email: france@adlinktech.com

ADLINK Technology Japan Corporation
Address: 〒101-0045 東京都千代田区神田鍛冶町 3-7-4
神田 374 ビル 4F
KANDA374 Bldg. 4F, 3-7-4 Kanda Kajicho,
Chiyoda-ku, Tokyo 101-0045, Japan
Tel: +81-3-4455-3722
Fax: +81-3-5209-6013
Email: japan@adlinktech.com

ADLINK Technology, Inc. (Korean Liaison Office)
Address: 137-881 서울시 서초구 서초대로 326, 802 (서초동, 모인터빌딩)
802, Mointer B/D, 326 Seocho-daero, Seocho-Gu,
Seoul 137-881, Korea
Tel: +82-2-2057-0565
Fax: +82-2-2057-0563
Email: korea@adlinktech.com

ADLINK Technology Singapore Pte. Ltd.
Address: 84 Genting Lane #07-02A, Cityneon Design Centre
Singapore 349584
Tel: +65-6844-2261
Fax: +65-6844-2263
Email: singapore@adlinktech.com

ADLINK Technology Singapore Pte. Ltd. (Indian Liaison Office)
Address: #50-56, First Floor, Spearhead Towers
Margosa Main Road (between 16th/17th Cross)
Malleswaram, Bangalore - 560 055, India
Tel: +91-80-65605817, +91-80-42246107
Fax: +91-80-23464606
Email: india@adlinktech.com

ADLINK Technology, Inc. (Israeli Liaison Office)
Address: 27 Maskit St., Corex Building
PO Box 12777
Herzliya 4673300, Israel
Tel: +972-54-632-5251
Fax: +972-77-208-0230
Email: israel@adlinktech.com

ADLINK Technology, Inc. (UK Liaison Office)
Tel: +44 774 010 59 65
Email: UK@adlinktech.com