8259A - STUDY CARD

1. INTRODUCTION

Electro Systems Associates Private Limited (ESA) manufactures trainers for most of the popular microprocessors viz 8085, Z-80, 8031 8086/88, 68000 and 80196. ESA offers a variety of modules, which can be interfaced to these trainers. These modules can be effectively used for teaching/training in the Laboratories.

The 8259 Study Card incorporates Intel's 8259A(PIC) Programmable Interrupt Controller. The Study Card is designed to demonstrate the different modes of operation of 8259.

This Manual presents the User about Functional description of 8259, implementation of the circuit and sample programs for 8259.

2. DESCRIPTION OF THE CIRCUIT:

The 8259 Study Card allows the user to study the different modes of operation of 8259 by connecting it to different microprocessor/controller trainers. The interrupts to 8259 can be given from on-board provision or from external sources through jumper selections. The on-board interrupt source uses a four-way dipswitch to select the eight different interrupts and the push button switch is to give the interrupt. For the onboard interrupts user has to place the jumpers JP1 to JP8 in the position 23. For external interrupt place the jumpers JP1 to JP8 at 12 position, depends on the interrupt number. The Study Card has got two 26-Pin (J3 & J4) and one 50-Pin (P1) connectors for interfacing with different Trainers.
The user can find more details about 8259A (i.e. Programming, Pin details etc) in the next section.

Default factory settings for onboard interrupts for MPS 85-3, ESA 85-2, ESA 31/51, ESA 51E, and ESA 86E Trainers are as follows.

JP1 = 23	JP6 = 23
JP2 = 23	JP7 = 23
JP3 = 23	JP8 = 23
JP4 = 23	JP9 = 23
JP5 = 23	JP10 = 12

JP11, JP12 & JP13 must be left open.

Default factory settings for onboard interrupts for ESA 86/88-2/3 Trainers are as follows.

JP1 = 23	JP6 = 23
JP2 = 23	JP7 = 23
JP3 = 23	JP8 = 23
JP4 = 23	JP9 = 12
JP5 = 23	JP10 = 12

JP11, JP12 & JP13 must be Closed.

4 -Way Dip Switch selection for different interrupts are as follows

SW1 4 WAY

3	2	1	Interrupt No
OFF	OFF	OFF	IR0
OFF	OFF	ON	IR1
OFF	ON	OFF	IR2
OFF	ON	ON	IR3
ON	OFF	OFF	IR4
ON	OFF	ON	IR5
ON	ON	OFF	IR6
ON	ON	ON	IR7

8259A

PROGRAMMABLE INTERRUPT CONTROLLER
(8259A/8259-2)

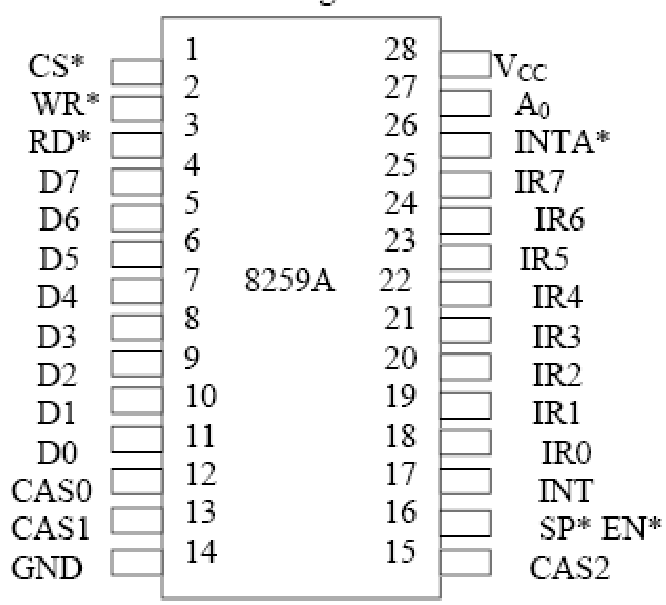
THEORY:
- **IAPX 86, IAPX 88 Compatible**
- **MCS-80, MCS-85Compatible**
- **Eight-Level Priority Controller**
- **Expandable to 64 Levels**
- **Programmable Interrupt Modes**
- **Individual Request (No Clocks)**
- **28-Pin Dual-In-Line Package**

The Intel 8259A Programmable Interrupt Controller handles up to eight-vectored priority interrupts for the CPU. It is cascadable for up to 64-vectored priority interrupts without additional circuitry. It is packaged in a 28-pin DIP, uses NMOS technology, and requires a single +5V supply. Circuitry is static, requiring no clock input.

The 8259A is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

The 8259A is fully upward compatible with the Intel 8259. Software originally written for the 8259 will operate the 8259A equivalent modes (MCS-80/85, Non-Buffered, Edge Triggered).

Pin Configuration



D_7-D_0	Data Bus (Bi directional)
RD*	Read Input
WR*	Write Input
A0	Command Select Address
CS*	Chip Select
CAS2 CAS0	Cascade lines
SP* EN*	Slave Program Enable Buffer
INT	Interrupt Output
INTA*	Interrupt Acknowledge Input
IR0 IR7	Interrupt Request Inputs

Block Diagram

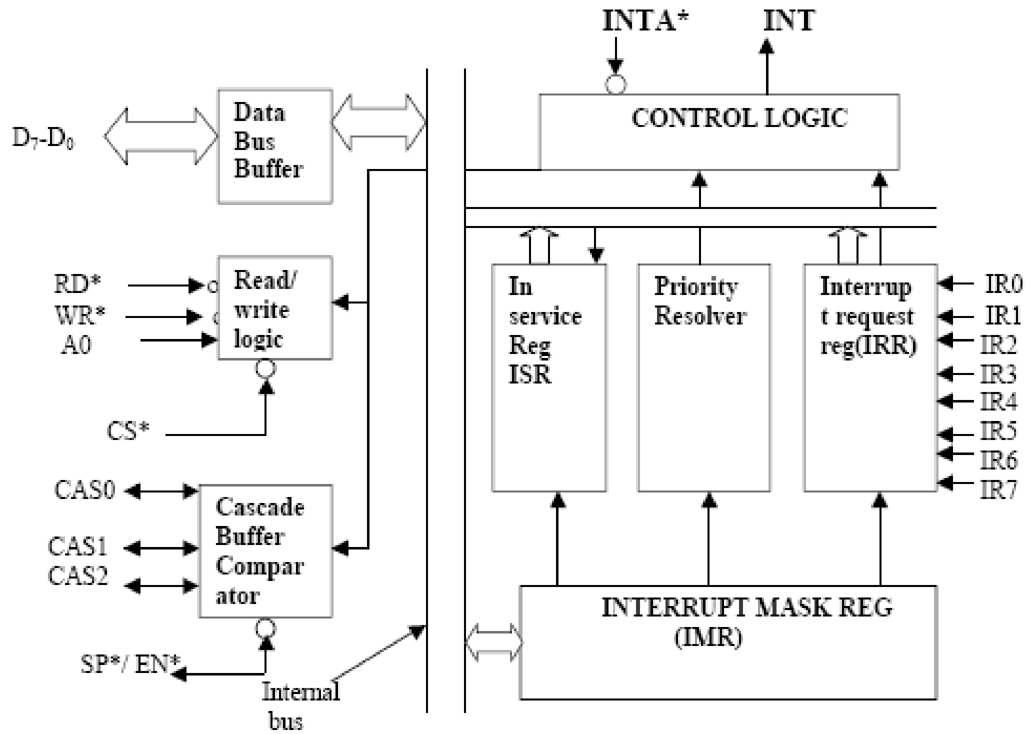


Table 1. Pin Description

Symbol	Pin No	Type	Name and Function
VCC	28	1	**Supply:** +5V Supply
GND	14	1	Ground.
CS*	1	1	**Chip Select:** A low on this pin enables RD* and WR* communication Between the CPU and the 8259A. INTA functions are independent of CS.
WR*	2	0	**Write:** A low on this pin when CS is low enables the 8259A to accept command words from the CPU.
RD*	3	1	**Read:** A low on this pin when CS* is low enables the 8259A to release Status onto the data bus for the CPU.
D_7- D_0	4 – 11	I/O	**Bi-directional Data Bus:** Control, status and interrupt-vector information is transferred via this bus.
CAS_0-CAS_2	12, 13, 15	I/O	**Cascade Lines:** The CAS lines form a private 8259A bus to control a multiple 8259A structure. These pins are outputs for a master 8259A and inputs for a slave 8259A.
SP*/EN*	16	I/O	**Slave Program/Enable Buffer:** This is a dual function pin. When in the Buffered Mode it can be used as an output to control buffer transceivers (EN). When not in the buffered mode it is used as an input to designate a master (SP = 1) or slave (SP = 0).
INT	17	O	**Interrupt:** This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to CPU's

			interrupt pin.
IR_0- IR_7	18-25	1	**Interrupt Requests:** Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode).
INTA*	26	1	**Interrupt Acknowledge:** This pin is used to enable 8259A interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
A_0	27	1	**AO Address Line:** This pin acts in conjunction with the CS*, WR*, and RD* pins. It is used by the 8259A to decipher various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A_0 address (A_1 for IAPX 86, 88).

FUNCTIONAL DESCRIPTION

Interrupts in Microcomputer Systems

Microcomputer system design requires that I/O devices such as keyboards, displays, sensors and other components receive servicing in an efficient manner so that large amounts of the total system tasks can be assumed by the microcomputer with little or no effect on through put.

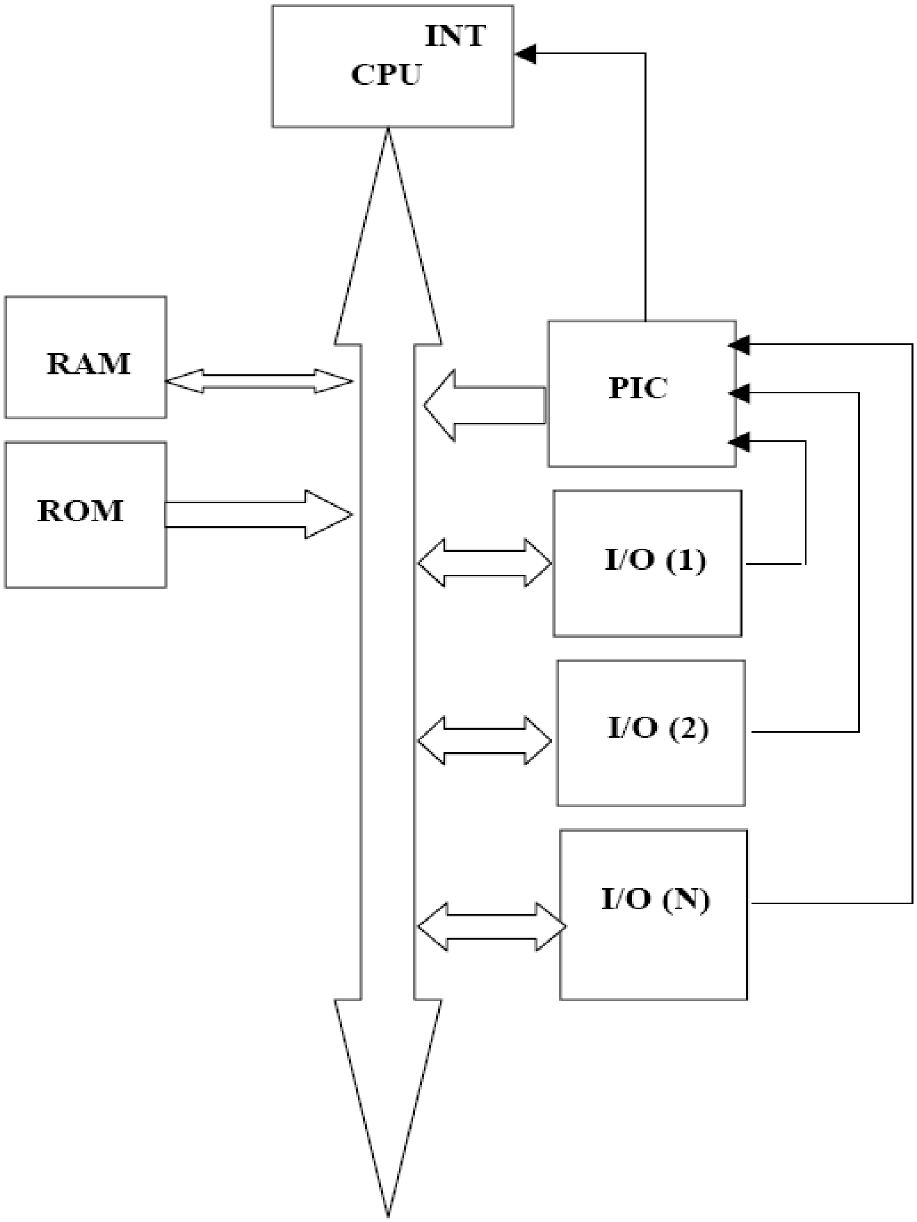
The most common method of servicing such devices is the Polled approach. This is where the processor must test each device in sequence and in effect “ask” each one if it needs servicing. It is easy to see that a large portion of the main program is looping through this continuous polling cycle and that such a method would have a serious, detrimental effect on system through-put, thus limiting the tasks that could be assumed by the microcomputer and reducing the cost effectiveness of using such devices.

A more desirable method would be one that would allow the microprocessor to be executing its main program and only stop to service peripheral devices when it is told to do so by the device itself. In effect, the method would provide an external asynchronous input that would inform the processor that it should complete whatever instruction is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is complete, however, the processor would resume exactly where it left off.

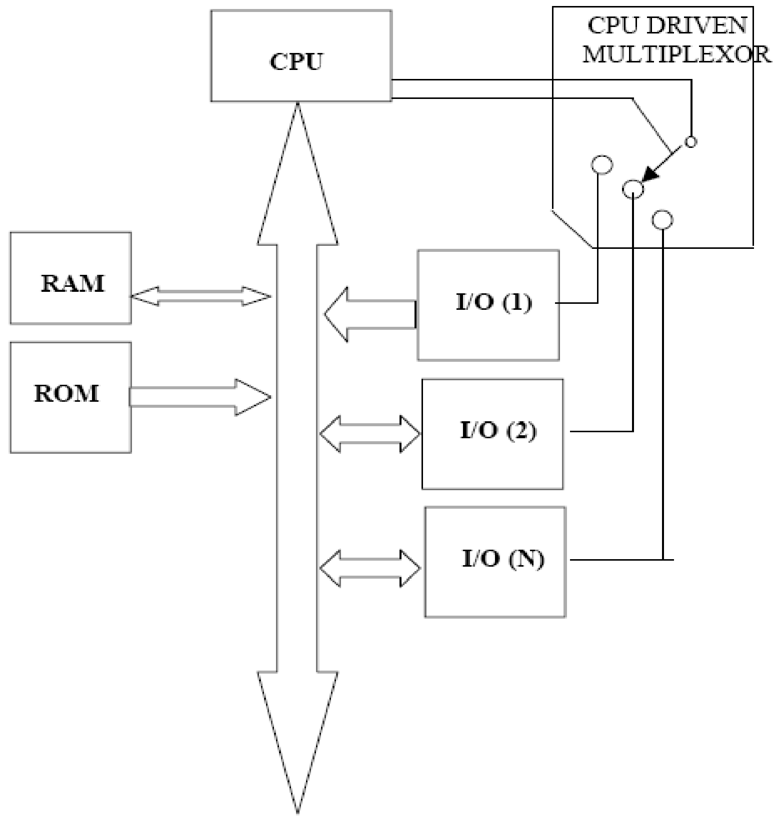
This method is called interrupt. It is easy to see that system throughput would drastically increase, and thus more tasks could be assumed by the microcomputer to further enhance its cost effectiveness.

The Programmable interrupt Controller (PIC) functions as an overall manager in an interrupt-Driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and issues an interrupt to the CPU based on this determination.

Each peripheral device or structure usually has a special program or “routine” that is associated with its specific functional or operational requirements; this is referred to as a “service routine”. The PIC, after issuing an interrupt to the CPU must somehow input information into the CPU that can “point” the Program Counter to the service routine associated with the requesting device. This “pointer” is an address in a vectoring table and will often be referred to, in this document, as vectoring data.



Interrupt Method



Polled Method

The 8259A is a device specifically designed for use in real time, interrupt driven microcomputer systems. It manages eight levels or requests and has built-in features for expandability to other 8259A's (up to 64 levels). It is programmed by the system's software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the 8259A can be configured to match his system requirements. The priority modes can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.

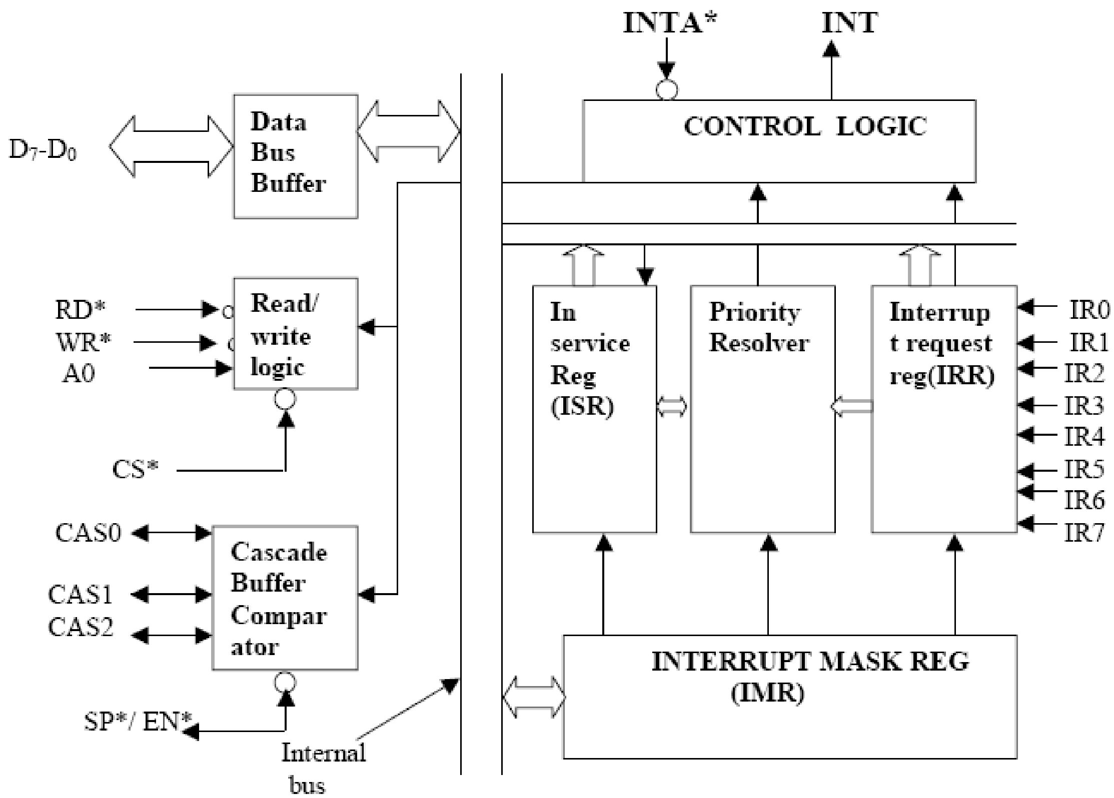


Figure: 4a:8259A Block Diagram

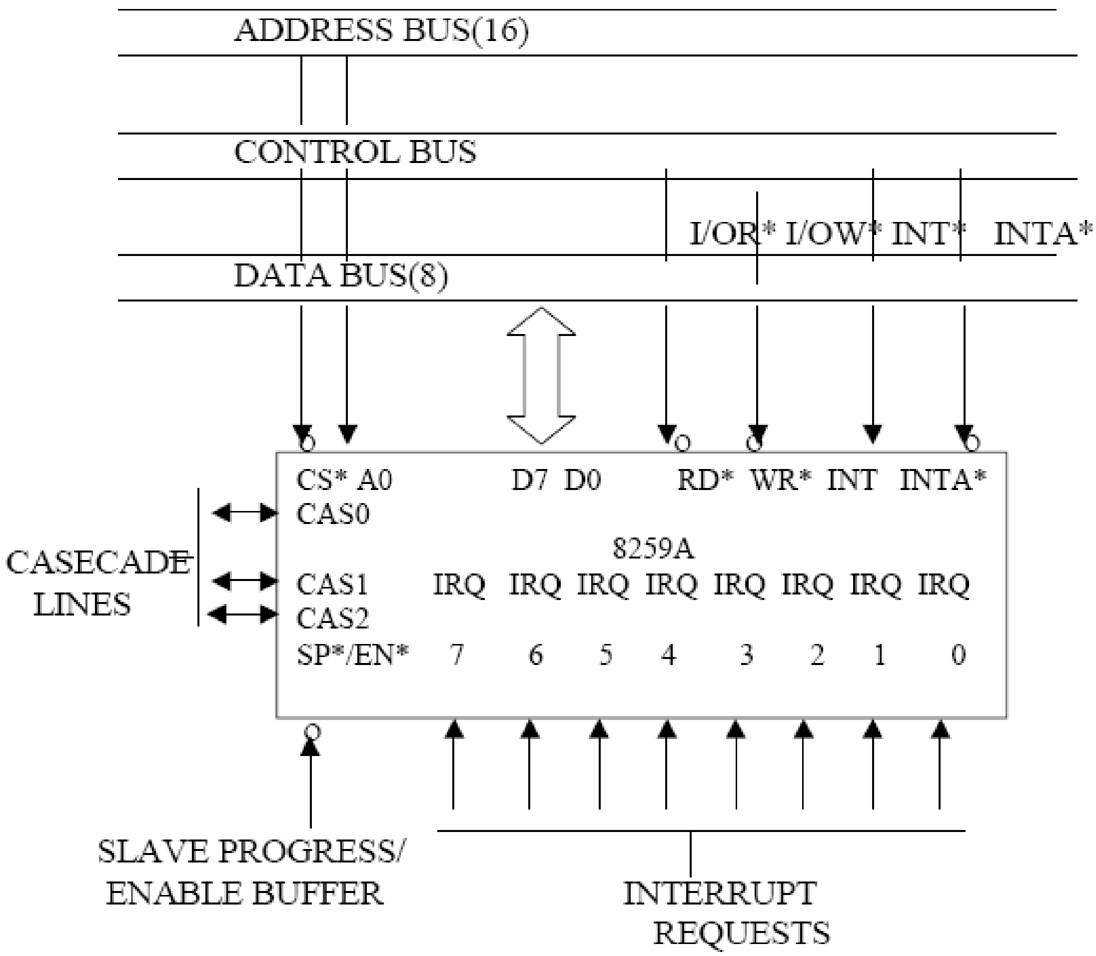


Figure 5. 8259A Interface to Standard System Bus

INTERRUPT REQUEST REGISTER (IRR) AND IN-SERVICE REGISTER (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels, which are requesting service; and the ISR is used to store all the interrupt levels, which are being serviced.

PRIORITY RESOLVER

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during INTA* pulse.

INTERRUPT MASK REGISTER (IMR)

The IMR stores the bits, which mask the interrupt lines to be masked. The IMR operates on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

INT (INTERRUPT)

This output goes directly to the CPU interrupt input. The V_{OH} level on this line is designed to be fully compatible with the 8080A. 8085A and 8086 input levels.

INTA* (INTERRUPT ACKNOWLEDGE)

INTA* puises will cause the 8259A to release vectoring information onto the data bus. The format of this data depends on the system mode of the 8259A.

DATA BUS BUFFER

This 3-state, bi-directional 8-bit buffer is used to interface the 8259A to the system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

READ/WRITE CONTROL LOGIC

The function of this block is to accept OUTPUT commands from the CPU. It contains the initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the 8259A to be transferred onto the Data Bus.

CS* (CHIP SELECT)

A LOW on this input enables the 8259A. No reading or writing of the chip will occur unless the device is selected.

WR* (WRITE)
A LOW on this input enables the CPU to write control words (ICWs and OCWs) to the 8259A.

RD* (READ)

A LOW on this input enables the 8259A to send the status of the interrupt Request Register (IRR), In Service Register (ISR), the Interrupt Mask Register (IMR), or the interrupt level onto the Data Bus.

A_0
This input signal is used in conjunction with WR* and RD* signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

THE CASCADE BUFFER/COMPARATOR

This function block stores and compares the IDs of all 8259A's used in the system. The associated three I/O pins (CAS0-2) are outputs when the 8259A is used as a master and are inputs when the 8259A is used as a slave. As a master, the 8259A sends the ID of the interrupting slave device onto the CAS0-2 lines. The slave thus selected will send its preprogrammed subroutines address onto the Data Bus during the next one or two consecutive INTA* pulses. (See section "Cascading the 8259A").

INTERRUPT SEQUENCE

The powerful features of the 8259A in a microcomputer system are its programmability and the interrupt routine address capability. The latter allows direct or indirect jumping to the specific interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

The events occur as follows in a MCS-80/85 system.

1. One or more of the INTERRUPT REQUEST lines (IR7-0) are raised high, setting the corresponding IRR bit (s).

2. The 8259A evaluates these requests, and sends an INT to the CPU, if appropriate.

3. The CPU acknowledges the INT and responds with an INTA* pulse.

4. Upon receiving an INTA* from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The 8259A will also release a CALL instruction code (11001101) onto the 8-bit Data Bus through its D7-0 pins.

5. This CALL instruction will initiate two more INTA* pulses to be sent to the 8259A from the CPU group.

6. These two INTA* pulses allow the 8259A to release its preprogrammed subroutine address onto the Data Bus. The lower 8-bit address is released at the first INTA* pulse and the higher 8-bit address is released at the second INTA* pulse.

7. This completes the 8-byte CALL instruction released by the 8259A. In the AEOI mode the ISR bit is reset at the end of the third INTA* pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The events occurring in an iAPX 86 systems are the same until step 4.

4. Upon receiving an INTA* from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The 8259A does not drive the Data Bus during this cycle.

5. The iAPX 86/10 will initiate a second INTA* pulse. During the pulse, the 8259A releases an 8-bit pointer onto the Data Bus where it is read by the CPU.

6. This completes the interrupt cycle. In the AEOI mode the ISR bit is reset at the end of the second INTA* pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt request present at step 4 of either sequence (i.e., the request was too short in duration) the 8259A will issue an interrupt level 7. Both the vectoring bytes and the CAS lines will look like an interrupt level 7 was requested.

INTERRUPT SEQUENCE OUTPUTS

MCS-80, MCS-85

This sequence is timed by three INTA* pulses. During the first INTA* pulse the CALL opcode is enabled onto the data bus.

Content of First Interrupt Vector Byte

	D7	D6	D5	D4	D3	D2	D1	D0
CALL CODE	1	1	0	0	1	1	0	1

During the second INTA* pulse the lower address of the appropriate service routine is enabled onto the data bus. When interval = 4 bits A_5-A_7 are programmed, while A_0-A_4 are automatically inserted by the 8259A. When interval = 8 only A_6 and A_7 are programmed, while A_0-A_5 are automatically inserted.

Content of Second Interrupt Vector Byte

IR	**INTERVAL = 4**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	1	0	0
0	A7	A6	A5	0	0	0	0	0

IR	**INTERVAL = 8**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

During the third INTA pulse the higher address of the appropriate service routine, which was programmed as byte 2 of the initialization sequence (A_8-A_{15}), is enabled onto the bus.

Content of Third Interrupt Vector Byte

D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
A15	A14	A13	A12	A11	A10	A9	A8

IAPX 86, IAPX 88

IAPX 86 mode is similar to MCS-80 mode except that only two interrupt acknowledge cycles are issued by the processor and no CALL opcode is sent to the processor. The first interrupt acknowledge cycle is similar to that of MCS-80, 85 systems in that the 8259A uses it to internally freeze the state of the interrupts for priority resolution and as a master it issues the interrupt code on the cascade lines at the end of the INTA pulse. On this first cycle it does not issue any data to the processor and leaves its data bus buffers disabled. On the second interrupt acknowledge cycle in IAPX 86 mode the master (or slave if so programmed) will send a byte of data to the processor with the acknowledged interrupt code composed as follows (note the state of the ADI mode control is ignored and A_5-A_{11} are unused in iAPX 86 mode):

Content of Interrupt Vector Byte for IAPX 86 System Mode

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

PROGRAMMING THE 8259A

The 8259A accepts two types of command words generated by the CPU.

1. **Initialization Command Words (ICWS):** Before normal operation can begin, each 8259A in the system must be brought to a starting point – by a sequence of 2 to 4 bytes timed by WR* pulses.

2. **Operation Command Words (OCWS):** These are the command words, which command the 8259A to operate in various interrupt modes. These modes are:

a. Fully nested mode
b. Rotating priority mode
c. Special mask mode
d. Polled mode

The OCWs can be written into the 8259A anytime after initialization.

INITILIZATION COMMAND WORDS (ICWS)

GENERAL

Whenever a command is issued with A0 = 0 and D4 = 1, this is interpreted as initialization Command Word 1 (ICW1), ICW1 starts the initialization sequence during which the following automatically occur.

a. The edge sense circuit is reset, which means that following initialization, an interrupt request (IR) input must make a low-to-high transition to generate an interrupt.

b. The interrupt Mask Register is cleared.

c. IR7 input is assigned priority 7.

d. The slave mode address is set to 7.
e. Special Mask Mode is cleared and Status Read is set to IRR.

f. If IC4 = 0, then all functions selected in ICW4 are set to zero. (Non-Buffered mode*, no Auto-EO1, MCS-80, 85 system).

Note: Master/Slave in ICW4 is only used in the buffered mode.

INITILIZATION COMMAND WORDS 1 AND 2 (ICW, ICW2)

A_5-A_{15}: Page starting address of service routines. In an MCS 80/85 system, the 8 request levels will generate CALLs to 8 locations equally spaced at intervals of 4 of 8 memory locations, thus the 8 routines will occupy a page of 32 or 64 bytes, respectively.

The address format is 2 bytes long (A_0-A_{15}). When the routine interval is 4, A_0-A_4 are automatically inserted by the 8259A, while A_5-A_{15} are programmed externally. When the routine interval is 8, A_0-A_5 are automatically inserted by the 8259A. While A6-A15 are programmed externally.

The 8-byte interval will maintain compatibility with current software while the 4-byte interval is best for a compact jump table.

In an iAPX 86 system A_{15}-A_{11} are inserted in the five most significant bits of the vectoring byte and the 8259A sets the three least significant bits according to the interrupt level, A_{10}-A_5 are ignored and ADI (Address interval) has no effect.

LTIM: If LTIM = 1, then the 8259A will operate in the level interrupt mode. Edge detect logic on the interrupt mode. Edge defect logic on the interrupt inputs will be disabled.

ADI: CALL address interval. ADI=1then interval =4; ADI=0 then interval = 8.
SNGL: Single, Means that this is the only 8259A in the system. If SNGL = 1 no ICW3 will be issued.

IC4: If this bit is set – ICW4 has to be read. If ICW4 is not needed, set IC4=0.

INITILIZATION COMMAND WORD 3 (ICW3)

This word is read only when there is more than one 8259A in the system and cascading is used, in which case SNGL=0, it will load the 8-bit slave register. The functions of this register are:

a. In the master mode (either when SP=1, or in buffered mode when M/S = 1 in ICW4) a "1" is set for each slave in the system. The master then will release byte 1 of the call sequence (for MCS-80/85 system) and will enable the corresponding slave to release bytes 2 and 3 (for iAPX 86 only byte 2) through the cascade lines.

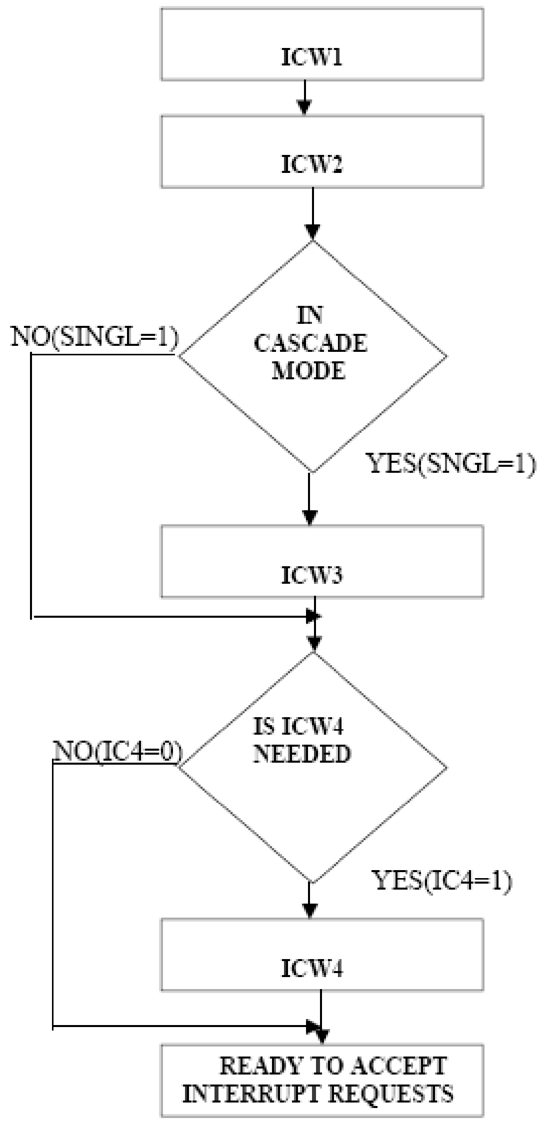
b. In the slave mode (either when SP* = 0, or if BUF = 1 and M/S =0 in ICW4) bits 2-0 identify the slave. The slave compares its cascade input with these bits and, if they are equal, bytes 2 and 3 of the call sequence (or just byte 2 for iAPX 86 are released by it on the Data Bus.

INITIALIZATION COMMAND WORD 4 (ICW4)

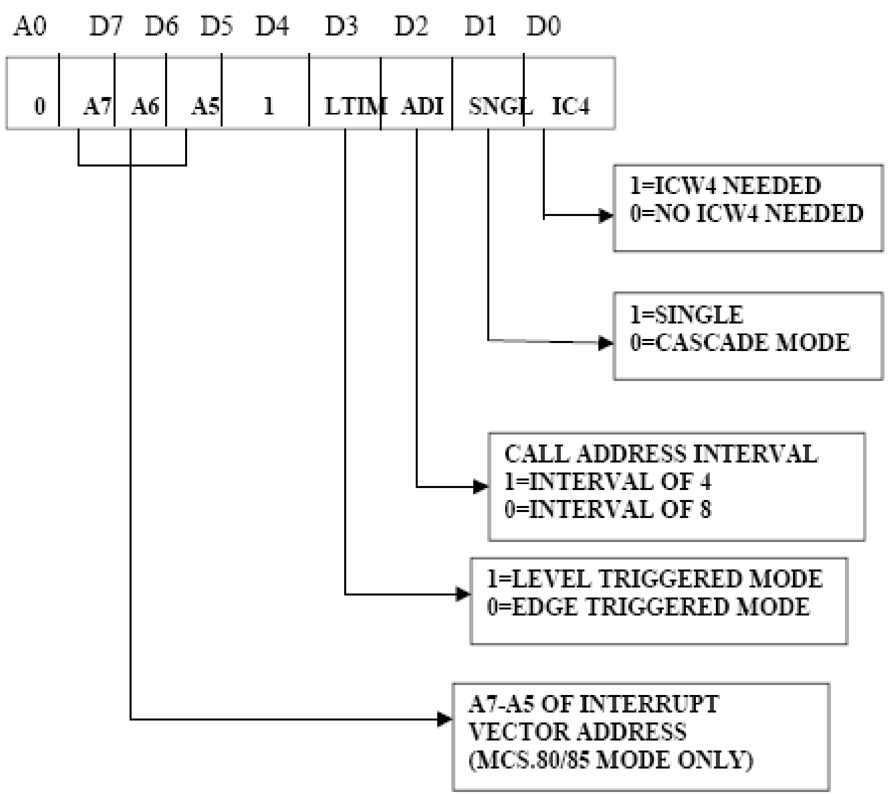
SFNM: If SFNM = 1the special fully nested mode is programmed.
BUF: If BUF = 1 the buffered mode is programmed. In buffered mode SP*/EN* becomes an enable output and the master/slave determination is by M/S.

M/S: If buffered mode is selected M/S = 1 means the 8259A is programmed to be a master, M/S = 0 means the 8259A is programmed to be a slave. If BUF = 0, M/S has no function.

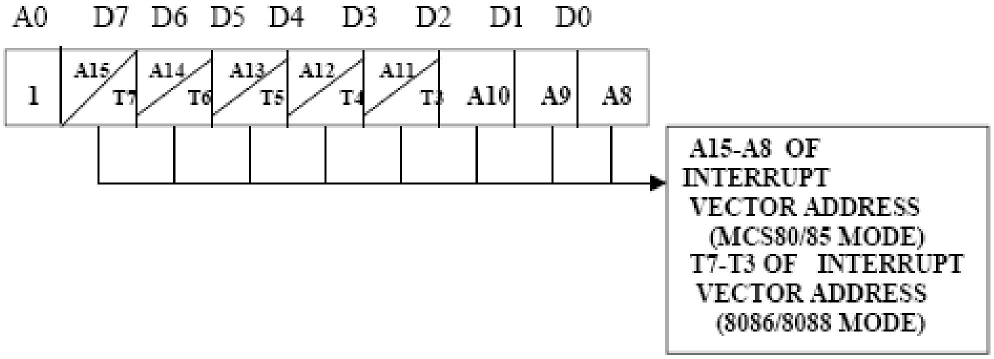
AEOI: If AEOI = 1 the automatic end of interrupt mode is programmed.
uPM: Microprocessor mode: uPM = 0 sets the 8259A for MCS-80, 85 system operation. uPM = 1 sets the 8259A for iAPX 86 system operation.


ICW1
ICW2
NO(SINGL=1)
IN
CASCADE
MODE
YES(SNGL=1)
ICW3
NO(IC4=0)
IS ICW4
NEEDED
YES(IC4=1)
ICW4
READY TO ACCEPT
INTERRUPT REQUESTS

ICW1


A0 D7 D6 D5 D4 D3 D2 D1 D0
0 A7 A6 A5 1 LTIM ADI SNGL IC4
1=ICW4 NEEDED
0=NO ICW4 NEEDED
1=SINGLE
0=CASCADE MODE
CALL ADDRESS INTERVAL
1=INTERVAL OF 4
0=INTERVAL OF 8
1=LEVEL TRIGGERED MODE
0=EDGE TRIGGERED MODE
A7-A5 OF INTERRUPT
VECTOR ADDRESS
(MCS.80/85 MODE ONLY)

ICW2


A0
D7
D6
D5
D4
D3
D2
D1
D0
1
A15 T7
A14 T6
A13 T5
A12 T4
A11 T3
A10
A9
A8
A15-A8 OF INTERRUPT VECTOR ADDRESS (MCS80/85 MODE)
T7-T3 OF INTERRUPT VECTOR ADDRESS (8086/8088 MODE)

ICW3(MASTER DEVICE)

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	**S7**	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**	**S0**

1= IR INPUT HAS A SLAVE
0= IR INPUT DOES NOT HAVE A SLAVE

ICW3 (SLAVE DEVICE)

A0	D7	D6	D5	D4	D3	D2	D1	D0
1	**0**	**0**	**0**	**0**	**0**	**ID2**	**ID1**	**D0**

SLAVE ID'S

0	1	2	3	4	5	6	7
0	1	0	1	0	1	0	1
0	0	1	1	0	0	1	1
0	0	0	0	1	1	1	1

ICW4

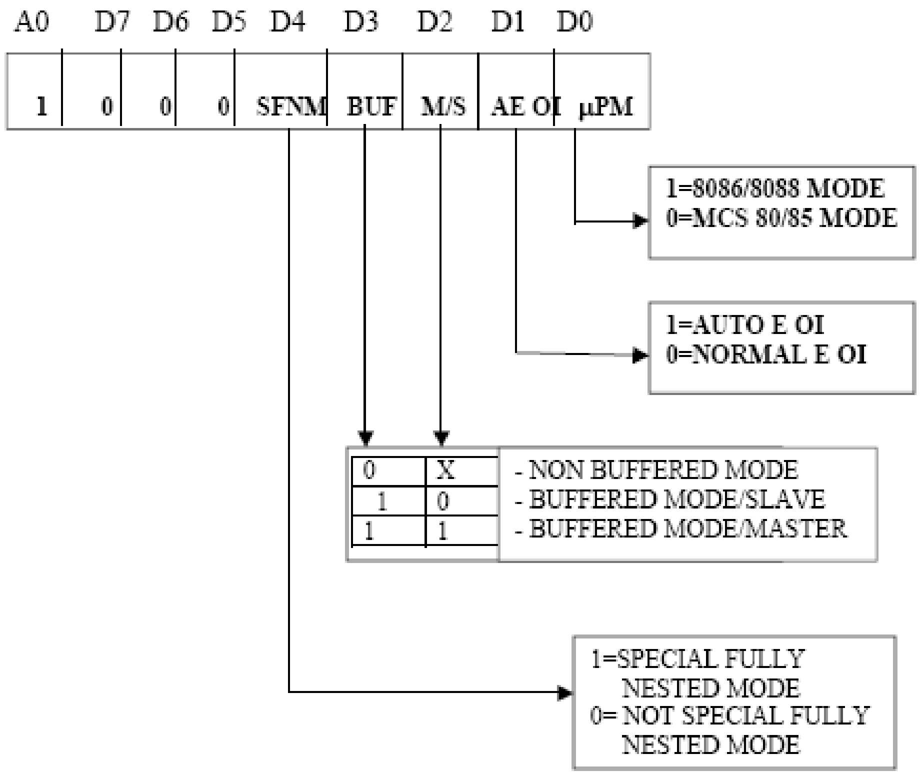


Figure 7. Initialization Command Word Format .

OPERATION COMMAND WORDS (OCWs)

After the initialization Command Words (ICWs) are programmed into the 8259A, the chip is ready to accept interrupt requests at its input lines. However, during the 8259A operation, a selection of algorithms can command the 8259A to operate in various modes through the Operation Command Words (OCWs).

OPERATION CONTROL WORDS (OCWs)

OCW1

A0								
1	D7	D6	D5	D4	D3	D2	D1	D0
	M7	M6	M5	M4	M3	M2	M1	M0

OCW2

A0								
0	R	SL	EOI	0	0	L2	L1	L0

OCW3

A0								
0	0	ESMM	SMM	0	1	P	RR	RIS

OPERATION CONTROL WORD 1 (OCW1)

OCW1 sets and clears the mask bits in the interrupt Mask Register (IMR). M_7-M_0 represents the eight mask bits. M = 1 indicates the channel is masked (inhibited), M=0 indicates the channel is enabled.

OPERATION CONTROL WORD 2 (OCW2)

R, SL, EOI – These three bits control the Rotate and End of interrupt modes and combinations of the two-A chart of these combinations can be found on the Operation Command Word Format.

$L_{2,}$ L_1, L_0- These bits determine the interrupt level acted upon when the SL bit is active.

OPERATION CONTROL WORD 3 (OCW3)

ESMM- Enable Special Mask Mode. When this bit is set to 1 it enables the SMM bit to set or reset the Special Mask Mode. When ESMM =0 the SMM bit becomes a “don’t care”.

SMM – Special Mask Mode. If ESMM = 1 and SMM = 1 the 8259A will enter Special Mask Mode. If ESMM=1and SMM = 0 the 8259A will revert to normal mask mode. When ESMM = 0, SMM has no effect.

FULLY NESTED MODE

This mode is entered after initialization unless another mode is programmed. The interrupt requests are ordered in priority form 0 through 7 (0 highest). When an interrupt is acknowledged the highest priority request is determined and its vector placed on the bus. Additionally, a bit of the interrupt Service register (ISO-7) is set. End of interrupt (EO1) command immediately before returning from the service routine, or if AEO1 (Automatic End of Interrupt) bit is set, until the trailing edge of the last INTA. While the bit **IS** set, all further interrupts of the same or lower priority are inhibited. While higher levels will generate an interrupt (Which will be acknowledged only if the microprocessor internal interrupt enable flip-flop has been re-enabled through software).

After the initialization sequence, IR0 has the highest priority and IR7 the lowest. Priorities can be changed, as will be explained, in the rotating priority mode.

END OF INTERRUPT (EOI)

The in Service (IS) bit can be reset either automatically following the trailing edge of the last in sequence INTA* pulse (when AEOI) bit in ICW1 is set) or by a command word that must be issued to the 8259A before returning from a service routine (EOI command). An EOI command must be issued twice if in the Cascade mode, once for the master and once for the corresponding slave.

There are two forms of EOI command: Specific and non-specific. When the 8259A is operated in modes, which preserve the fully nested structure, it can determine which IS bit to reset on EOI. When a Non-Specific EOI command is issued the 8259A will automatically reset the highest IS bit of those that are set, since in the fully nested mode the highest IS level was necessarily the last level acknowledged and serviced. A non-specific EOI can be issued with OCW2 (EOI=1, SL=0, R=0).

When a mode is used which may disturb the fully nested structure, the 8259A may no longer be able to determine the last level acknowledged. In this case a Specific End of interrupt must be issued which includes as part of the command the IS level to be reset. A specific EOI can be issued with OCW2 (EO1 = 1, SL=1, R = 0, and LO-L2 is the binary level of the IS bit to be reset).

It should be noted that an IS bit that is masked by an IMR bit will not be cleared by a non-specific EOI if the 8259A is in the Special Mask Mode.

AUTOMATIC END OF INTERRUPT (AEOI) MODE

If AEOI = 1 in ICW4, then the 8259A will operate in AEOI mode continuously until reprogrammed by ICW4. In this mode the 8259A will automatically perform a non-specific EOI operation at the trailing edge of the last interrupt acknowledge pulse (third pulse in MCS-80/85, second in iAPX 86). Note that from a system standpoint, this mode should be used only when a nested multilevel interrupt structure is not required within a single 8259A.

The AEOI mode can only be used in a master 8259A and not a slave.

AUTOMATIC ROTATION (Equal Priority Devices)

In some applications there are a number of interrupting devices of equal priority. In this mode a device after being serviced, receives the lowest priority, so a device requesting an interrupt will have to wait, in the worst case until each of 7 other devices are serviced at most once. For example, if the priority and "in service" status is:

Before Rotate (IR4 the highest priority requiring service).

" IS" Status	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
	0	1	0	1	0	0	0	0

Priority Status Lowest Priority Highest Priority

7	6	5	4	3	2	1	0

After Rotate (IR4 was serviced, all other priorities rotated correspondingly)

" IS" Status	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
	0	1	0	0	0	0	0	0

Priority Status Lowest Priority Highest Priority

2	1	0	7	6	5	4	3

There are two ways to accomplish Automatic Rotation using OCW2, the Rotation on Non-specific EOI Command (R=1, SL = 0, EOI = 1) and Rotate in Automatic EOI Mode, which is set by (R = 1, SL=0, EOI = 0) and cleared.

SPECIFIC ROTATION (specific Priority)

The programmer can change priorities by programming the bottom priority and thus fixing all other priorities; i.e., if IR5 is programmed as the bottom priority device then IR6 will have the highest one.

The Set Priority command is issued in OCW2 where; R=1, SL=1, LO-L2 is the binary priority level code of the bottom priority device.

Observe that in this mode internal status is updated by software control during OCW2. However, it is independent of the End of interrupt (EOI) command (also executed by OCW2). Priority changes can be executed during an EOI in OCW2 (R=1, SL=1, EOI = 1 and LO-L2 = IR level to receive bottom priority).

INTERRUPT MASKS

Each Interrupt Request input can be masked individually by the interrupt Mask Register (IMR) programmed through OCW1. Each bit in the IMR masks one interrupt channel if it is set (1). Bit 0 masks IR0, Bit 1 masks IRI and so forth. Masking an IR channel does not affect the other channels operation.

SPECIAL MASK MODE

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The difficulty here is that if an interrupt Request is acknowledged and an End of Interrupt command did not reset its IS bit (i.e., while executing a service routine), the 8259A would have inhibited all lower priority requests with no easy way for the routine to enable them.

That is where the Special Mask Mode comes in. In the special Mask Mode, when a mask bit is set in OCW1, it inhibits further interrupts at that level and enables interrupts from all other levels (lower as well as higher) that are not masked.

Thus, any interrupts may be selectively enabled by loading the mask register.

The special Mask Mode is set by OCW3 where SSMM=1, SMM=1, and cleared where SSMM=1, SMM=0.

POLL COMMAND

In this mode the INT output is not used or the microprocessor internal interrupt Enable flip-flop is reset, disabling its interrupt input, Service to devices is achieved by software using a Poll command.

The Poll command is issued by setting P=”1” in OCW3. The 8259A treats the next RD* pulse to the 8259A (i.e., RD*=0, CS*=0) as an interrupt acknowledge, sets the appropriate IS bit if there is a request, and reads the priority level. Interrupt is frozen from WR* to RD*.

The word enabled onto the data bus during RD* is:

D7	D6	D5	D4	D3	D2	D1	D0

1	----	---	----	----	W2	W1	W0

W0-W2: Binary code of the highest priority level requesting service.

1: Equal to a "1" if there is an interrupt.
This mode is useful if there is a routine command common to several levels so that the INTA* sequence is not needed (saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.

READING THE 8259A STATUS

The input status of several internal registers can be read to update the user information on the system. The following registers can be read via OCW3 (IRR and ISR or OCW1 [IMR]).

Interrupt Request Register (IRR): 8-bit register, which contains the levels requesting an interrupt to be acknowledged. The highest request level is reset from the IRR. When an Interrupt is acknowledged (not affected by IMR).

In-Service Register (ISR): 8 bit register, which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt Command is issued.

Interrupt Mask Register: 8-bit register, which contains the interrupt request, lines which are masked.

The IRR can be read when, prior to the RD pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS=0).

The ISR can be read when, prior to the RD pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 0).

There is no need to write an OCW3 before every status read operation, as long as the status read corresponds with the previous one; i.e., the 8259A "remembers" whether the IRR or ISR has been previously selected by the OCW3. This is not true when poll is used.

After initialization the 8259A is set to IRR.

For reading the IMR, no OCW3 is needed. The output data bus will contain the IMR whenever RD* is active and AO=1 (OCW1).

Polling overrides status read when P=1, RR = 1 in OCW3.

EDGE AND LEVEL TRIGGERED MODES

This mode is programmed using bit 3 in ICW1.

If LTIM = '0', an interrupt request will be recognized by a low to high transition on an IR input. The IR input can remain high without generating another interrupt.

If LTIM='1', an interrupt request will be recognized by a 'high' level on IR input, and there is no need for an edge detection. The interrupt request must be removed before the EOI Command is issued or the CPU interrupt is enabled to prevent a second interrupt from occurring.

The priority cell diagram shows a conceptual circuit of the level sensitive and edge sensitive input circuitry of the 8259A. Be sure to note that the request latch is a transparent D type latch.

In both the edge and level triggered modes the IR inputs must remain high until after the falling edge of the first INTA. If the IR input goes low before this time a DEFAULT IR7 will occur when the CPU acknowledges the interrupt. This can be a useful safeguard for detecting interrupts caused by spurious noise glitches on the IR inputs. To implement this feature the IR7 routine is used for "clean up simply executing a return instruction, thus ignoring the interrupt. If IR7 is needed for other purposes a default IR7 can still be detected by reading the ISR, a normal IR7 interrupt will set the corresponding ISR bit, a default IR7 won't. If a default IR7 routine occurs during a normal IR7 routine, however, the ISR will remain set. In this case it is necessary to keep track of whether or not the IR7 routine was previously entered. If another IR7 occurs it is a default.

THE SPECIAL FULLY NESTED MODE

This mode will be used in the case of a big system where cascading is used, and the priority has to be conserved within each slave. In this case the fully nested mode will be programmed to the master (using ICW4). This mode is similar to the normal nested mode with the following exceptions:

a. When an interrupt request from a certain slave is in service this slave is not locked out from the master's priority logic and further interrupt requests from higher priority IR's within the slave will be recognized by the master and will initiate interrupts to the processor. (In the normal nested mode a slave is masked out when its request is in service and no higher requests from the same slave can be serviced.

b. When exiting the interrupt Service routine the software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a non-specific End of interrupt (EOI) command to the slave and then reading its in-service register and checking for zero. If it is empty, a non-specific EOI can be sent to the master too. If not, no EOI should be sent.

BUFFERED MODE

When the 8259A is used in a large system where bus-driving buffers are required on the data bus and the cascading mode is used, there exists the problem of enabling buffers.

The buffered mode will structure the 8259A to send an enable signal on SP*/EN* to enable the buffers. In this mode, whenever the 8259A's data bus outputs are enabled, the SP*/EN* output becomes active.

This modification forces the use of software programming to determine whether the 8259A is a master or a slave Bit 3 in ICW4 programs the buffered mode, and bit 2 in ICW4 determines whether it is a master or a slave.

CASCADE MODE

The 8259A can be easily interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels.

The master controls the slaves through the 3-line cascade bus. The cascade bus acts like chip selects to the slaves during the INTA* sequence.

In a cascade configuration, the slave interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and afterwards acknowledged, the master will enable the corresponding slave to release the device routine address during bytes 2 and 3 of INTA. (Byte 2 only for 8086 / 8088).

The cascade bus lines are normally low and will contain the slave address code from the trailing edge of the first INTA pulse to the trailing edge of the third pulse. Each 8259A in the system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice: once for the master and once for the corresponding slave. An address decoder is required to active the Chip Select (CS) input of each 8259A.

The cascade lines of the Master 8259A are activated only for slave inputs, non-slave inputs leave the cascade line inactive (low).

3.0 INSTALLATION AND CONFIGURATION

The Connector details for connecting the Study Card to different Trainers are mentioned below.

<table>
<tr><th>TRAINER</th><th>CONNECTORS ON TRAINER</th><th colspan="2">CONNECTORS ON STUDY CARD ADAPTER</th><th>CONNECTORS ON STUDY CARD</th></tr>
<tr><td>MPS 85-3</td><td>J3 (26 PIN)
J4 (26 PIN)</td><td colspan="2">-
-</td><td>J3 (26 PIN)
J4 (26 PIN)</td></tr>
<tr><td>ESA 85-2</td><td>P1 (50 PIN)</td><td colspan="2">-</td><td>P1 (50 PIN)</td></tr>
<tr><td>ESA 86/88-2/3 *</td><td>J1 (50 PIN)
J2 (50 PIN)</td><td>J1 (50 PIN)
J2 (50 PIN)</td><td>J3 (26 PIN)
J4 (26 PIN)</td><td>J3 (26 PIN)
J4 (26 PIN)</td></tr>
<tr><td>ESA 86E Ver 2.00</td><td>J6 (26 PIN)
J7 (26 PIN)</td><td colspan="2">-
-</td><td>J3 (26 PIN)
J4 (26 PIN)</td></tr>
<tr><td>ESA 51E</td><td>J4</td><td>P3 (50 PIN)</td><td>P1(26 PIN)
P2 (26 PIN)</td><td>J3 (26 PIN)
J4 (26 PIN)</td></tr>
<tr><td>ESA 51E Ver 4.00</td><td>J4 (26 PIN)
J6 (26 PIN)</td><td colspan="2">-
-</td><td>J3 (26 PIN)
J4 (26PIN)</td></tr>
</table>

*** External Study Card Adapter is required to connect the Study Card with the Trainer**

Connect the Study Card by following the above-mentioned connectors with FRCs respectively.

Switch Off Power to the Trainer while connecting the Study Card. Press Reset after giving power to the Trainer.

4. DEMONSTRATION PROGRAM FOR 8085 SERIES KITS.
4A. DEMONSTRATION PROGRAMS FOR MPS 85-3 TRAINER

Connect the Study Card's J3 & J4 connectors to Trainer's J3 & J4 connectors using FRCs respectively.

EXAMPLE 1:

The following program configures the 8259 to accept the all the interrupts from 0 to 8. User can give interrupt from the on board push button switch or from external sources. For on board interrupts select the interrupt number by Dipswitch selection and press the push button to generate the interrupt. Execute the Program in Serial mode of operation of the Trainer. The program displays the corresponding interrupt number on the console or on serial monitor.

ADDRESSES OF 8259 ARE 90H AND 91H

```
                    DISPM  EQU   0B5BH    ;DISPLAY ROUTINE ADDRESS TO DISPLAY
                                          ;MESSAGE ON SERIAL
                           ORG   8000H
8000   3E 12     START: MVI   A,12H    ;single, edge triggerd mode,
                                          ; call address interval 8.
8002   D3 90            OUT   90H
8004   3E 81            MVI   A,81H    ;interrupt vector address.
8006   D3 91            OUT   91H
8008   3E 00            MVI   A,00H    ;Normal EOI,for 80/85
800A   D3 91            OUT   91H       ;mode for 8259.
800C   3E 20            MVI   A,20H     ;Non specific EOI command.
800E   D3 90            OUT   90H
8010   FB               EI
8011   C3 11 80   SSS:  JMP   SSS
8014   DF          UP:  RST   3
                        ORG   8100H
8100   21 46 81         LXI   H,MES0   ;Routine to display the massage.
8103   C3 40 81         JMP   SUBRT
8106   00               NOP
8107   00               NOP
```

```
8108    21 5B 81        LXI     H,MES1
810B    C3 40 81        JMP     SUBRT
810E    00              NOP
810F    00              NOP
8110    21 70 81        LXI     H,MES2
8113    C3 40 81        JMP     SUBRT
8116    00              NOP
8117    00              NOP
8118    21 85 81        LXI     H,MES3
811B    C3 40 81        JMP     SUBRT
811E    00              NOP
811F    00              NOP
8120    21 9A 81        LXI     H,MES4
8123    C3 40 81        JMP     SUBRT
8126    00              NOP
8127    00              NOP
8128    21 AF 81        LXI     H,MES5
812B    C3 40 81        JMP     SUBRT
812E    00              NOP
812F    00              NOP
8130    21 C4 81        LXI     H,MES6
8133    C3 40 81        JMP     SUBRT
8136    00              NOP
8137    00              NOP
8138    21 D9 81        LXI     H,MES7
813B    C3 40 81        JMP     SUBRT
813E    00              NOP
813F    00              NOP
8140    CD 5B 0B SUBRT:CALL     DISPM
8143    C3 14 80        JMP     UP

8146    49 52 30 20 49      MES0: DB "IR0 IS INTERRUPTED",0DH,0AH,00H
814B    53 20 49 4E 54
8150    45 52 52 55 50
8155    54 45 44 0D 0A
815A    00
815B    49 52 31 20 49      MES1: DB "IR1 IS INTERRUPTED",0DH,0AH,00H
```

```
    8160   53 20 49 4E 54
    8165   45 52 52 55 50
    816A   54 45 44 0D 0A
    816F   00
    8170   49 52 32 20 49      MES2: DB "IR2 IS INTERRUPTED",0DH,0AH,00H
    8175   53 20 49 4E 54
    817A   45 52 52 55 50
    817F   54 45 44 0D 0A
    8184   00
    8185   49 52 33 20 49      MES3: DB "IR3 IS INTERRUPTED",0DH,0AH,00H
    818A   53 20 49 4E 54
    818F   45 52 52 55 50
    8194   54 45 44 0D 0A
    8199   00
    819A   49 52 34 20 49      MES4: DB "IR4 IS INTERRUPTED",0DH,0AH,00H
    819F   53 20 49 4E 54
    81A4   45 52 52 55 50
    81A9   54 45 44 0D 0A
    81AE   00
    81AF   49 52 35 20 49      MES5: DB "IR5 IS INTERRUPTED",0DH,0AH,00H
    81B4   53 20 49 4E 54
    81B9   45 52 52 55 50
    81BE   54 45 44 0D 0A
    81C3   00
    81C4   49 52 36 20 49      MES6: DB "IR6 IS INTERRUPTED",0DH,0AH,00H
    81C9   53 20 49 4E 54
    81CE   45 52 52 55 50
    81D3   54 45 44 0D 0A
    81D8   00
    81D9   49 52 37 20 49      MES7: DB "IR7 IS INTERRUPTED",0DH,0AH,00H
    81DE   53 20 49 4E 54
    81E3   45 52 52 55 50
    81E8   54 45 44 0D 0A
    81ED   00
```

EXAMPLE 2:

This Program configures the 8259 to accept 8 interrupt requests from onboard sources. Keep the dipswitch SW1 for corresponding interrupt. Execute the program from 8000H.Then press the push button switch.

Execute the program in KEYBOARD mode only.

```
                        RDKBD    EQU     03BAH   ;Routine to read the keys
                                                 ;on the hexpad
                                 ORG     8000H
8000   3E 12            START:   MVI     A,12H   ;single,edge triggerd mode,
                                                 ;call address interval 8.
8002   D3 90                     OUT     90H
8004   3E 82                     MVI     A,82H   ;interrupt vector address.
8006   D3 91                     OUT     91H
8008   3E 00                     MVI     A,00H   ;Normal EOI,for 80/85
800A   D3 91                     OUT     91H     ;mode for 8259.
800C   3E 20                     MVI     A,20H   ;Non specific EOI command.
800E   D3 90                     OUT     90H
8010   FB                        EI
8011   C3 11 80           SSS:   JMP     SSS
                                 ORG    8200H
8200   CD 3E 82                  CALL   R0      ;Routine to Display int
8203   C3 5B 82                  JMP    S0      ;number on the Trainer
8206   00                        NOP
8207   00                        NOP
8208   CD 3E 82                  CALL    R0
820B   C3 66 82                  JMP     S1
820E   00                        NOP
820F   00                        NOP
8210   CD 3E 82                  CALL    R0
8213   C3 71 82                  JMP     S2
8216   00                        NOP
8217   00                        NOP
8218   CD 3E 82                  CALL    R0
821B   C3 7C 82                  JMP     S3
821E   00                        NOP
821F   00                        NOP
8220   CD 3E 82                  CALL    R0
8223   C3 87 82                  JMP     S4
```

```
8226   00              NOP
8227   00              NOP
8228   CD 3E 82        CALL   R0
822B   C3 92 82        JMP    S5
822E   00              NOP
822F   00              NOP
8230   CD 3E 82        CALL   R0
8233   C3 9D 82        JMP    S6
8236   00              NOP
8237   00              NOP
8238   CD 3E 82        CALL   R0
823B   C3 A8 82        JMP    S7
823E   3E 90       R0: MVI    A,90H   ;Routine to display
8240   D3 31           OUT    31H     ;Intr 00 on seven segment
8242   3E 60           MVI    A,60H   ;display.
8244   D3 30           OUT    30H
8246   3E 45           MVI    A,45H
8248   D3 30           OUT    30H
824A   3E 87           MVI    A,87H
824C   D3 30           OUT    30H
824E   3E 05           MVI    A,05H
8250   D3 30           OUT    30H
8252   3E F3           MVI    A,0F3H
8254   D3 30           OUT    30H
8256   3E 00           MVI    A,00H
8258   D3 30           OUT    30H
825A   C9              RET
825B   3E 95       S0: MVI    A,95H
825D   D3 31           OUT    31H
825F   3E F3           MVI    A,0F3H
8261   D3 30           OUT    30H
8263   C3 B0 82        JMP    LOOP
8266   3E 95       S1: MVI    A,95H
8268   D3 31           OUT    31H
826A   3E 60           MVI    A,60H
826C   D3 30           OUT    30H
826E   C3 B0 82        JMP    LOOP
```

```
8271   3E 95         S2: MVI    A,95H
8273   D3 31             OUT    31H
8275   3E B5             MVI    A,0B5H
8277   D3 30             OUT    30H
8279   C3 B0 82          JMP    LOOP
827C   3E 95         S3: MVI    A,95H
827E   D3 31             OUT    31H
8280   3E F4             MVI    A,0F4H
8282   D3 30             OUT    30H
8284   C3 B0 82          JMP    LOOP
8287   3E 95         S4: MVI    A,95H
8289   D3 31             OUT    31H
828B   3E 66             MVI    A,66H
828D   D3 30             OUT    30H
828F   C3 B0 82          JMP    LOOP
8292   3E 95         S5: MVI    A,95H
8294   D3 31             OUT    31H
8296   3E D6             MVI    A,0D6H
8298   D3 30             OUT    30H
829A   C3 B0 82          JMP    LOOP
829D   3E 95         S6: MVI    A,95H
829F   D3 31             OUT    31H
82A1   3E D7             MVI    A,0D7H
82A3   D3 30             OUT    30H
82A5   C3 B0 82          JMP    LOOP
82A8   3E 95         S7: MVI    A,95H
82AA   D3 31             OUT    31H
82AC   3E 70             MVI    A,70H
82AE   D3 30             OUT    30H
82B0   CD BA 03    LOOP: CALL   RDKBD   ;Waiting for NEXT key.
82B3   FE 1C             CPI    1CH
82B5   C2 B0 82          JNZ    LOOP
82B8   EF                RST    5
```

EXAMPLE 3:

`This Program` configures 8259 to accept only Int1 using the interrupt mask command in OCW1. Keep the dipswitch SW1 for IR1 interrupt. . Execute the program from 8000H.Then press the push button switch.

Execute the program in SERIAL mode only.

```
                DISPM   EQU     0B5BH
                                ORG     8000H
8000   3E 12            START:  MVI     A,12H   ;single,edge triggerd mode,
                                                ;call address interval 8.
8002   D3 90                    OUT     90H
8004   3E 81                    MVI     A,81H   ;interrupt vector address.
8006   D3 91                    OUT     91H
8008   3E 00                    MVI     A,00H   ;Normal EOI,for 80/85
800A   D3 91                    OUT     91H     ;mode for 8259.
800C   3E FD                    MVI     A,0FDH  ;Enable only IR1 interrupt
800E   D3 91                    OUT     91H     ;in OCW1.
8010   FB                       EI
8011   C3 11 80           SSS:  JMP     SSS
8014   DF                  UP:  RST     3
                                ORG    8100H
8100   21 46 81                 LXI     H,MES0 ;Routine to display the
8103   C3 40 81                 JMP     SUBRT  ;message.
8106   00                       NOP
8107   00                       NOP
8108   21 5B 81                 LXI     H,MES1
810B   C3 40 81                 JMP     SUBRT
810E   00                       NOP
810F   00                       NOP
8110   21 70 81                 LXI     H,MES2
8113   C3 40 81                 JMP     SUBRT
8116   00                       NOP
8117   00                       NOP
8118   21 85 81                 LXI     H,MES3
811B   C3 40 81                 JMP     SUBRT
811E   00                       NOP
811F   00                       NOP
8120   21 9A 81                 LXI     H,MES4
8123   C3 40 81                 JMP     SUBRT
8126   00                       NOP
8127   00                       NOP
```

```
8128   21 AF 81              LXI      H,MES5
812B   C3 40 81              JMP      SUBRT
812E   00                    NOP
812F   00                    NOP
8130   21 C4 81              LXI      H,MES6
8133   C3 40 81              JMP      SUBRT
8136   00                    NOP
8137   00                    NOP
8138   21 D9 81              LXI      H,MES7
813B   C3 40 81              JMP      SUBRT
813E   00                    NOP
813F   00                    NOP
8140   CD 5B 0B      SUBRT:  CALL     DISPM
8143   C3 14 80              JMP      UP

8146   49 52 30 20 49        MES0: DB "IR0 IS INTERRUPTED",0DH,0AH,00H
814B   53 20 49 4E 54
8150   45 52 52 55 50
8155   54 45 44 0D 0A
815A   00
815B   49 52 31 20 49        MES1: DB "IR1 IS INTERRUPTED",0DH,0AH,00H
8160   53 20 49 4E 54
8165   45 52 52 55 50
816A   54 45 44 0D 0A
816F   00
8170   49 52 32 20 49        MES2: DB "IR2 IS INTERRUPTED",0DH,0AH,00H
8175   53 20 49 4E 54
817A   45 52 52 55 50
817F   54 45 44 0D 0A
8184   00
8185   49 52 33 20 49        MES3: DB "IR3 IS INTERRUPTED",0DH,0AH,00H
818A   53 20 49 4E 54
818F   45 52 52 55 50
8194   54 45 44 0D 0A
8199   00
819A   49 52 34 20 49        MES4: DB "IR4 IS INTERRUPTED",0DH,0AH,00H
819F   53 20 49 4E 54
```

```
81A4    45 52 52 55 50
81A9    54 45 44 0D 0A
81AE    00
81AF    49 52 35 20 49      MES5: DB "IR5 IS INTERRUPTED",0DH,0AH,00H
81B4    53 20 49 4E 54
81B9    45 52 52 55 50
81BE    54 45 44 0D 0A
81C3    00
81C4    49 52 36 20 49      MES6: DB "IR6 IS INTERRUPTED",0DH,0AH,00H
81C9    53 20 49 4E 54
81CE    45 52 52 55 50
81D3    54 45 44 0D 0A
81D8    00
81D9    49 52 37 20 49      MES7: DB "IR7 IS INTERRUPTED",0DH,0AH,00H
81DE    53 20 49 4E 54
81E3    45 52 52 55 50
81E8    54 45 44 0D 0A
81ED    00
```

EXAMPLE 4:

This Program configures 8259 to accept priority interrupt by using Set priority command. In this program IR5 is fixed as the bottom priority device. So IR6 will have the highest one. Execute this program in SERIAL mode only.

Note: **To test this program, Connect 8255 (at U12) PA0 to PA7 pins to EIR0 to EIR7 pins of J2. Put the jumper JP1 to JP7 at 12 positions on the Study Card.**

```
                        DISPM   EQU     0B5BH
                                ORG     8000H
8000    3E 80                   MVI     A,80H   ;Configure 8255 all
8002    D3 43                   OUT     43H     ;ports O/P.
8004    3E 16                   MVI     A,16H   ;Single, edge triggerd mode,
                                                ;call address interval 4.
8006    D3 90                   OUT     90H
8008    3E 81                   MVI     A,81H   ;Interrupt vector address.
800A    D3 91                   OUT     91H
800C    3E C5                   MVI     A,0C5H  ;Fix IR5 as bottom priority.
800E    D3 90                   OUT     90H  ;by set priority command in OCW2.
8010    FB                      EI
8011    3E FF                   MVI     A,0FFH  ;Send all IR0 to IR7 high at a
```

```
8013   D3 40            OUT     40H     ;time.
                    ORG     8100H
8100   C3 21 81     JMP     R0      ;Interrupt vector address for IR0.
8103   00           NOP
8104   C3 2A 81     JMP     R1      ;Interrupt vector address for IR1.
8107   00           NOP
8108   C3 33 81     JMP     R2      ;and so on.
810B   00           NOP
810C   C3 3C 81     JMP     R3
810F   00           NOP
8110   C3 45 81     JMP     R4
8113   00           NOP
8114   C3 4E 81     JMP     R5
8117   00           NOP
8118   C3 57 81     JMP     R6
811B   00           NOP
811C   C3 60 81     JMP     R7
811F   00           NOP
8120   DF      UP:  RST     3
8121   21 69 81       R0: LXI    H,MES0 ;Routine to display messages.
8124   CD 5B 0B           CALL    DISPM
8127   C3 20 81           JMP     UP
812A   21 7E 81       R1: LXI     H,MES1
812D   CD 5B 0B           CALL    DISPM
8130   C3 20 81           JMP     UP
8133   21 93 81       R2: LXI     H,MES2
8136   CD 5B 0B           CALL    DISPM
8139   C3 20 81           JMP     UP
813C   21 A8 81       R3: LXI     H,MES3
813F   CD 5B 0B           CALL    DISPM
8142   C3 20 81           JMP     UP
8145   21 BD 81       R4: LXI     H,MES4
8148   CD 5B 0B           CALL    DISPM
814B   C3 20 81           JMP     UP
814E   21 D2 81       R5: LXI     H,MES5
8151   CD 5B 0B           CALL    DISPM
8154   C3 20 81           JMP     UP
```

```
8157   21 E7 81        R6: LXI     H,MES6
815A   CD 5B 0B            CALL    DISPM
815D   C3 20 81            JMP     UP
8160   21 FC 81        R7: LXI     H,MES7
8163   CD 5B 0B            CALL    DISPM
8166   C3 20 81            JMP     UP

8169   49 52 30 20 49       MES0: DB "IR0 IS INTERRUPTED",0DH,0AH,00H
816E   53 20 49 4E 54
8173   45 52 52 55 50
8178   54 45 44 0D 0A
817D   00
817E   49 52 31 20 49       MES1: DB "IR1 IS INTERRUPTED",0DH,0AH,00H
8183   53 20 49 4E 54
8188   45 52 52 55 50
818D   54 45 44 0D 0A
8192   00
8193   49 52 32 20 49       MES2: DB "IR2 IS INTERRUPTED",0DH,0AH,00H
8198   53 20 49 4E 54
819D   45 52 52 55 50
81A2   54 45 44 0D 0A
81A7   00
81A8   49 52 33 20 49       MES3: DB "IR3 IS INTERRUPTED",0DH,0AH,00H
81AD   53 20 49 4E 54
81B2   45 52 52 55 50
81B7   54 45 44 0D 0A
81BC   00
81BD   49 52 34 20 49       MES4: DB "IR4 IS INTERRUPTED",0DH,0AH,00H
81C2   53 20 49 4E 54
81C7   45 52 52 55 50
81CC   54 45 44 0D 0A
81D1   00
81D2   49 52 35 20 49       MES5: DB "IR5 IS INTERRUPTED",0DH,0AH,00H
81D7   53 20 49 4E 54
81DC   45 52 52 55 50
81E1   54 45 44 0D 0A
81E6   00
```

```
81E7   49 52 36 20 49      MES6: DB "IR6 IS INTERRUPTED",0DH,0AH,00H
81EC   53 20 49 4E 54
81F1   45 52 52 55 50
81F6   54 45 44 0D 0A
81FB   00
81FC   49 52 37 20 49      MES7: DB "IR7 IS INTERRUPTED",0DH,0AH,00H
8201   53 20 49 4E 54
8206   45 52 52 55 50
820B   54 45 44 0D 0A
8210   00
```

5. DEMONSTRATION PROGRAMS FOR ESA 85-2 TRAINER

Connect the FRC between the connectors P1 of Trainer and P1 of Study Card.

***** Change the Jumper selection JP5 of the Trainer to 23 position before executing the following programs.***

EXAMPLE 1:

The following Program configures the 8259 to accept 8 interrupt requests. The interrupts can be given from onboard switch or from external sources. For onboard interrupts select the interrupt number using the dipswitch SW1 for corresponding interrupt. Execute the program from 8000H.Then press the push button switch to give the interrupt. Execute the program in SERIAL mode only. The displays the corresponding interrupt number on the console or on the serial monitor.

ADDRESSES OF STUDY CARD 8259 ARE 90H AND 91H

```
                         DISPM   EQU  0B04H    ;Display Routine to
                                                 ;display message on serial
                              ORG    8000H

8000   3E 12       START: MVI    A,12H   ;single,edge triggerd mode,
8002   D3 90              OUT    90H     ;call address interval 8.
8004   3E 81              MVI    A,81H   ;interrupt vector address.
8006   D3 91              OUT    91H
8008   3E 00              MVI    A,00H   ;Normal EOI,for 80/85
800A   D3 91              OUT    91H     ;mode for 8259.
800C   3E 20              MVI    A,20H   ;Non specific EOI command.
800E   D3 90              OUT    90H
8010   FB                 EI
8011   C3 11 80      SSS: JMP    SSS
8014   DF             UP: RST    3

                       ORG    8100H

8100   21 46 81        LXI    H,MES0  ;Routine to display the massage.
8103   C3 40 81        JMP    SUBRT
8106   00              NOP
8107   00              NOP
8108   21 5B 81        LXI     H,MES1
```

```
810B   C3 40 81         JMP     SUBRT
810E   00               NOP
810F   00               NOP
8110   21 70 81         LXI     H,MES2
8113   C3 40 81         JMP     SUBRT
8116   00               NOP
8117   00               NOP
8118   21 85 81         LXI     H,MES3
811B   C3 40 81         JMP     SUBRT
811E   00               NOP
811F   00               NOP
8120   21 9A 81         LXI     H,MES4
8123   C3 40 81         JMP     SUBRT
8126   00               NOP
8127   00               NOP
8128   21 AF 81         LXI     H,MES5
812B   C3 40 81         JMP     SUBRT
812E   00               NOP
812F   00               NOP
8130   21 C4 81         LXI     H,MES6
8133   C3 40 81         JMP     SUBRT
8136   00               NOP
8137   00               NOP
8138   21 D9 81         LXI     H,MES7
813B   C3 40 81         JMP     SUBRT
813E   00               NOP
813F   00               NOP
8140   CD 04 0B SUBRT:CALL    DISPM
8143   C3 14 80         JMP     UP

8146   49 52 30 20 49      MES0: DB "IR0 IS INTERRUPTED",0DH,0AH,00H
814B   53 20 49 4E 54
8150   45 52 52 55 50
8155   54 45 44 0D 0A
815A   00
815B   49 52 31 20 49      MES1: DB "IR1 IS INTERRUPTED",0DH,0AH,00H
8160   53 20 49 4E 54
8165   45 52 52 55 50
816A   54 45 44 0D 0A
816F   00
8170   49 52 32 20 49      MES2: DB "IR2 IS INTERRUPTED",0DH,0AH,00H
8175   53 20 49 4E 54
817A   45 52 52 55 50
817F   54 45 44 0D 0A
8184   00
8185   49 52 33 20 49      MES3: DB "IR3 IS INTERRUPTED",0DH,0AH,00H
818A   53 20 49 4E 54
818F   45 52 52 55 50
8194   54 45 44 0D 0A
8199   00
819A   49 52 34 20 49      MES4: DB "IR4 IS INTERRUPTED",0DH,0AH,00H
819F   53 20 49 4E 54
81A4   45 52 52 55 50
81A9   54 45 44 0D 0A
81AE   00
81AF   49 52 35 20 49      MES5: DB "IR5 IS INTERRUPTED",0DH,0AH,00H
```

```
81B4   53 20 49 4E 54
81B9   45 52 52 55 50
81BE   54 45 44 0D 0A
81C3   00
81C4   49 52 36 20 49      MES6: DB "IR6 IS INTERRUPTED",0DH,0AH,00H
81C9   53 20 49 4E 54
81CE   45 52 52 55 50
81D3   54 45 44 0D 0A
81D8   00
81D9   49 52 37 20 49      MES7: DB "IR7 IS INTERRUPTED",0DH,0AH,00H
81DE   53 20 49 4E 54
81E3   45 52 52 55 50
81E8   54 45 44 0D 0A
81ED   00
```

EXAMPLE 2:

The following Program configures 8259 to accept 8 interrupt requests from onboard sources. Keep the dip switch SW1 for corresponding interrupt. Execute the program from 8000H.Then press the push button switch.

Execute the program in KEYBOARD mode only.

```
                         RDKBD   EQU     0514H  ;Routine to read the
                                                ;keys from hex key pad
                         ORG    8000H
8000   3E 12     START:  MVI     A,12H   ;single,edge triggerd mode,
                                         ;call address interval 8.
8002   D3 90             OUT     90H
8004   3E 82             MVI     A,82H   ;interrupt vector address.
8006   D3 91             OUT     91H
8008   3E 00             MVI     A,00H   ;Normal EOI,for 80/85
800A   D3 91             OUT     91H     ;mode for 8259.
800C   3E 20             MVI     A,20H   ;Non specific EOI command.
800E   D3 90             OUT     90H
8010   FB                EI
8011   C3 11 80     SSS: JMP     SSS
                        ORG     8200H
8200   CD 3E 82         CALL    R0
8203   C3 5B 82         JMP     S0
8206   00               NOP
8207   00               NOP
8208   CD 3E 82         CALL    R0
820B   C3 66 82         JMP     S1
```

```
820E   00                NOP
820F   00                NOP
8210   CD 3E 82          CALL    R0
8213   C3 71 82          JMP     S2
8216   00                NOP
8217   00                NOP
8218   CD 3E 82          CALL    R0
821B   C3 7C 82          JMP     S3
821E   00                NOP
821F   00                NOP
8220   CD 3E 82          CALL    R0
8223   C3 87 82          JMP     S4
8226   00                NOP
8227   00                NOP
8228   CD 3E 82          CALL    R0
822B   C3 92 82          JMP     S5
822E   00                NOP
822F   00                NOP
8230   CD 3E 82          CALL    R0
8233   C3 9D 82          JMP     S6
8236   00                NOP
8237   00                NOP
8238   CD 3E 82          CALL    R0
823B   C3 A8 82          JMP     S7
823E   3E 90         R0: MVI     A,90H   ;Routine to display
8240   D3 31             OUT     31H     ;Intr 00 on seven segment
8242   3E 60             MVI     A,60H   ;display.
8244   D3 30             OUT     30H
8246   3E 45             MVI     A,45H
8248   D3 30             OUT     30H
824A   3E 87             MVI     A,87H
824C   D3 30             OUT     30H
824E   3E 05             MVI     A,05H
8250   D3 30             OUT     30H
8252   3E F3             MVI     A,0F3H
8254   D3 30             OUT     30H
8256   3E 00             MVI     A,00H
```

```
8258   D3 30           OUT    30H
825A   C9              RET
825B   3E 95       S0: MVI    A,95H
825D   D3 31           OUT    31H
825F   3E F3           MVI    A,0F3H
8261   D3 30           OUT    30H
8263   C3 B0 82        JMP    LOOP
8266   3E 95       S1: MVI    A,95H
8268   D3 31           OUT    31H
826A   3E 60           MVI    A,60H
826C   D3 30           OUT    30H
826E   C3 B0 82        JMP    LOOP
8271   3E 95       S2: MVI    A,95H
8273   D3 31           OUT    31H
8275   3E B5           MVI    A,0B5H
8277   D3 30           OUT    30H
8279   C3 B0 82        JMP    LOOP
827C   3E 95       S3: MVI    A,95H
827E   D3 31           OUT    31H
8280   3E F4           MVI    A,0F4H
8282   D3 30           OUT    30H
8284   C3 B0 82        JMP    LOOP
8287   3E 95       S4: MVI    A,95H
8289   D3 31           OUT    31H
828B   3E 66           MVI    A,66H
828D   D3 30           OUT    30H
828F   C3 B0 82        JMP    LOOP
8292   3E 95       S5: MVI    A,95H
8294   D3 31           OUT    31H
8296   3E D6           MVI    A,0D6H
8298   D3 30           OUT    30H
829A   C3 B0 82        JMP    LOOP
829D   3E 95       S6: MVI    A,95H
829F   D3 31           OUT    31H
82A1   3E D7           MVI    A,0D7H
82A3   D3 30           OUT    30H
82A5   C3 B0 82        JMP    LOOP
```

```
82A8   3E 95        S7: MVI     A,95H
82AA   D3 31            OUT     31H
82AC   3E 70            MVI     A,70H
82AE   D3 30            OUT     30H
82B0   CD 14 05   LOOP: CALL    RDKBD    ;Waiting for NEXT key.
82B3   FE 1C            CPI     1CH
82B5   C2 B0 82         JNZ     LOOP
82B8   DF               RST     3
```

EXAMPLE 3:

Configure 8259 to accept interrupt requests from onboard sources by using interrupt mask command in OCW1.

Keep the dipswitch SW1 for IR1 interrupt. Execute the program from 8000H.Then press the push button switch.

Execute the program in SERIAL mode only.

```
                          DISPM   EQU     0B04H
                                  ORG 8000H
8000   3E 12      START:  MVI     A,12H   ;single,edge triggerd mode,
                                           ;call address interval 8.
8002   D3 90              OUT     90H
8004   3E 81              MVI     A,81H   ;interrupt vector address.
8006   D3 91              OUT     91H
8008   3E 00              MVI     A,00H   ;Normal EOI,for 80/85
800A   D3 91              OUT     91H     ;mode for 8259.
800C   3E FD              MVI     A,0FDH  ;Enable only IR1 interrupt
800E   D3 91              OUT     91H     ;in OCW1.
8010   FB                 EI
8011   C3 11 80     SSS:  JMP     SSS
8014   DF            UP:  RST     3
                          ORG     8100H
8100   21 46 81           LXI     H,MES0 ;Routine to display
8103   C3 40 81           JMP     SUBRT  ;the message
8106   00                 NOP
8107   00                 NOP
```

```
8108   21 5B 81          LXI     H,MES1
810B   C3 40 81          JMP     SUBRT
810E   00                NOP
810F   00                NOP
8110   21 70 81          LXI     H,MES2
8113   C3 40 81          JMP     SUBRT
8116   00                NOP
8117   00                NOP
8118   21 85 81          LXI     H,MES3
811B   C3 40 81          JMP     SUBRT
811E   00                NOP
811F   00                NOP
8120   21 9A 81          LXI     H,MES4
8123   C3 40 81          JMP     SUBRT
8126   00                NOP
8127   00                NOP
8128   21 AF 81          LXI     H,MES5
812B   C3 40 81          JMP     SUBRT
812E   00                NOP
812F   00                NOP
8130   21 C4 81          LXI     H,MES6
8133   C3 40 81          JMP     SUBRT
8136   00                NOP
8137   00                NOP
8138   21 D9 81          LXI     H,MES7
813B   C3 40 81          JMP     SUBRT
813E   00                NOP
813F   00                NOP
8140   CD 04 0B   SUBRT: CALL    DISPM
8143   C3 14 80          JMP     UP

8146   49 52 30 20 49    MES0: DB "IR0 IS INTERRUPTED",0DH,0AH,00H
814B   53 20 49 4E 54
8150   45 52 52 55 50
8155   54 45 44 0D 0A
815A   00
815B   49 52 31 20 49      MES1: DB "IR1 IS INTERRUPTED",0DH,0AH,00H
```

```
8160   53 20 49 4E 54
8165   45 52 52 55 50
816A   54 45 44 0D 0A
816F   00
8170   49 52 32 20 49      MES2: DB "IR2 IS INTERRUPTED",0DH,0AH,00H
8175   53 20 49 4E 54
817A   45 52 52 55 50
817F   54 45 44 0D 0A
8184   00
8185   49 52 33 20 49      MES3: DB "IR3 IS INTERRUPTED",0DH,0AH,00H
818A   53 20 49 4E 54
818F   45 52 52 55 50
8194   54 45 44 0D 0A
8199   00
819A   49 52 34 20 49      MES4: DB "IR4 IS INTERRUPTED",0DH,0AH,00H
819F   53 20 49 4E 54
81A4   45 52 52 55 50
81A9   54 45 44 0D 0A
81AE   00
81AF   49 52 35 20 49      MES5: DB "IR5 IS INTERRUPTED",0DH,0AH,00H
81B4   53 20 49 4E 54
81B9   45 52 52 55 50
81BE   54 45 44 0D 0A
81C3   00
81C4   49 52 36 20 49      MES6: DB "IR6 IS INTERRUPTED",0DH,0AH,00H
81C9   53 20 49 4E 54
81CE   45 52 52 55 50
81D3   54 45 44 0D 0A
81D8   00
81D9   49 52 37 20 49      MES7: DB "IR7 IS INTERRUPTED",0DH,0AH,00H
81DE   53 20 49 4E 54
81E3   45 52 52 55 50
81E8   54 45 44 0D 0A 00
```

EXAMPLE 4:

Configure 8259 to accept priority interrupt by using Set priority command. In this program IR5 is fixed as the bottom priority device. So IR6 will have the highest one. Execute this program in SERIAL mode only.

Note: **To test this program, connect 8255 (at U35) PA0 to PA7 pins to EIR0 to EIR7 pins of J2.Put the jumper JP1 to JP7 at 12 position.**

```
                        DISPM   EQU     0B04H
                        ORG 8000H
8000    3E 80           MVI     A,80H   ;Configure 8255 all
8002    D3 43           OUT     43H     ;ports O/P.
8004    3E 16           MVI     A,16H   ;Single, edge triggerd mode,
                                        ;call address interval 4.
8006    D3 90           OUT     90H
8008    3E 81           MVI     A,81H   ;Interrupt vector address.
800A    D3 91           OUT     91H
800C    3E C5           MVI     A,0C5H  ;Fix IR5 as bottom priority.
800E    D3 90           OUT     90H     ;by set priority command in OCW2.
8010    FB              EI
8011    3E FF           MVI     A,0FFH  ;Send all IR0 to IR7 high at a time.
8013    D3 40           OUT     40H
                        ORG     8100H
8100    C3 21 81        JMP     R0      ;Interrupt vector address for IR0.
8103    00              NOP
8104    C3 2A 81        JMP     R1      ;Interrupt vector address for IR1.
8107    00              NOP
8108    C3 33 81        JMP     R2      ;and so on.
810B    00              NOP
810C    C3 3C 81        JMP     R3
810F    00              NOP
8110    C3 45 81        JMP     R4
8113    00              NOP
8114    C3 4E 81        JMP     R5
8117    00              NOP
8118    C3 57 81        JMP     R6
811B    00              NOP
811C    C3 60 81        JMP     R7
811F    00              NOP
8120    DF          UP: RST 3

8121    21 69 81          R0: LXI    H,MES0 ;Routine to display messages.
8124    CD 04 0B              CALL    DISPM
```

```
8127   C3 20 81          JMP    UP
812A   21 7E 81      R1: LXI    H,MES1
812D   CD 04 0B          CALL   DISPM
8130   C3 20 81          JMP    UP
8133   21 93 81      R2: LXI    H,MES2
8136   CD 04 0B          CALL   DISPM
8139   C3 20 81          JMP    UP
813C   21 A8 81      R3: LXI    H,MES3
813F   CD 04 0B          CALL   DISPM
8142   C3 20 81          JMP    UP
8145   21 BD 81      R4: LXI    H,MES4
8148   CD 04 0B          CALL   DISPM
814B   C3 20 81          JMP    UP
814E   21 D2 81      R5: LXI    H,MES5
8151   CD 04 0B          CALL   DISPM
8154   C3 20 81          JMP    UP
8157   21 E7 81      R6: LXI    H,MES6
815A   CD 04 0B          CALL   DISPM
815D   C3 20 81          JMP    UP
8160   21 FC 81      R7: LXI    H,MES7
8163   CD 04 0B          CALL   DISPM
8166   C3 20 81          JMP    UP

8169   49 52 30 20 49    MES0: DB "IR0 IS INTERRUPTED",0DH,0AH,00H
816E   53 20 49 4E 54
8173   45 52 52 55 50
8178   54 45 44 0D 0A
817D   00
817E   49 52 31 20 49    MES1: DB "IR1 IS INTERRUPTED",0DH,0AH,00H
8183   53 20 49 4E 54
8188   45 52 52 55 50
818D   54 45 44 0D 0A
8192   00
8193   49 52 32 20 49    MES2: DB "IR2 IS INTERRUPTED",0DH,0AH,00H
8198   53 20 49 4E 54
819D   45 52 52 55 50
81A2   54 45 44 0D 0A
```

```
81A7    00
81A8    49 52 33 20 49    MES3: DB "IR3 IS INTERRUPTED",0DH,0AH,00H
81AD    53 20 49 4E 54
81B2    45 52 52 55 50
81B7    54 45 44 0D 0A
81BC    00
81BD    49 52 34 20 49    MES4: DB "IR4 IS INTERRUPTED",0DH,0AH,00H
81C2    53 20 49 4E 54
81C7    45 52 52 55 50
81CC    54 45 44 0D 0A
81D1    00
81D2    49 52 35 20 49    MES5: DB "IR5 IS INTERRUPTED",0DH,0AH,00H
81D7    53 20 49 4E 54
81DC    45 52 52 55 50
81E1    54 45 44 0D 0A
81E6    00
81E7    49 52 36 20 49    MES6: DB "IR6 IS INTERRUPTED",0DH,0AH,00H
81EC    53 20 49 4E 54
81F1    45 52 52 55 50
81F6    54 45 44 0D 0A
81FB    00
81FC    49 52 37 20 49    MES7: DB "IR7 IS INTERRUPTED",0DH,0AH,00H
8201    53 20 49 4E 54
8206    45 52 52 55 50
820B    54 45 44 0D 0A
8210    00
```

5.DEMONSTRATION PROGRAM FOR 8086 SERIES KITS.

5A. DEMONSTRATION PROGRAM FOR ESA 86/88-2 TRAINER

The following Program configures the Study Card's 8259 as Slave and onboard 8259 (i.e. Trainer's) as Master in cascade mode. The Slave interrupt will be connected to INT0 of Master. The interrupts to Slave can be given from on board dipswitch and push button. Keep the dipswitch SW1 for corresponding interrupt. Execute the program from 2000H. Then press the push button switch. Execute the program in serial mode.

*****Place a Jumper between 1 and 2 (INT0) of JP8 on the Trainer before executing the Program.***

Onboard 8259 addresses are FFF4 and FFF6

Study Card's 8259 addresses are 0090 and 0092

```
                                ORG   2000H
0000:2000   FA                  CLI                 ;CLEAR INTERRUPT FLAG
0000:2001   B8 00 00            MOVW  AX, #0000     ;INITIALIZE SEGMENT
0000:2004   8E C8               MOVW  CX, AX        ;REGISTERS
0000:2006   8E C0               MOVW  ES, AX
0000:2008   80 D0               MOVW  SS, AX
0000:200A   BC 00 30            MOVW  SP, #3000     ;INITIALIZE SP

                                      ;INTERRUPT VECTOR INITIALIZATION
0000:200D   26                  ES
0000:200E   C7 06 20 01 00 22   MOVW  0120, #2200   ;INT0 VECTOR ADDRESS
0000:2014   26                  ES
0000:2015   C7 06 22 01 00 00   MOVW  0122, #0000   ;(SLAVE)
0000:201B   26                  ES
0000:201C   C7 06 24 01 50 22   MOVW  0124, #2250   ;INT1 VECTOR ADDRESS
0000:2022   26                  ES
0000:2023   C7 06 26 01 00 00   MOVW  0126, #0000   ;(SLAVE)
0000:2029   26                  ES
0000:202A   C7 06 28 01 00 23   MOVW  0128, #2300   ;INT2 VECTOR ADDRESS
0000:2030   26                  ES
0000:2031   C7 06 2A 01 00 00   MOVW  012A, #0000   ;(SLAVE)
0000:2037   26                  ES
0000:2038   C7 06 2C 01 50 23   MOVW  012C, #2350   ;INT3 VECTOR ADDRESS
0000:203E   26                  ES
```

```
0000:203F   C7 06 2E 01 00 00  MOVW  012E, #0000      ;(SLAVE)
0000:2045   26                 ES
0000:2046   C7 06 30 01 00 24  MOVW  0130, #2400      ;INT4 VECTOR ADDRESS
0000:204C   26                 ES
0000:204D   C7 06 32 01 00 00  MOVW  0132, #0000      ;(SLAVE)
0000:2053   26                 ES
0000:2054   C7 06 34 01 50 24  MOVW  0134, #2450      ;INT5 VECTOR ADDRESS
0000:205A   26                 ES
0000:205B   C7 06 36 01 00 00  MOVW  0136, #0000      ;(SLAVE)
0000:2061   26                 ES
0000:2062   C7 06 38 01 00 25  MOVW  0138, #2500      ;INT6 VECTOR ADDRESS
0000:2068   26                 ES
0000:2069   C7 06 3A 01 00 00  MOVW  013A, #0000      ;(SLAVE)
0000:206F   26                 ES
0000:2070   C7 06 3C 01 50 25  MOVW  013C, #2550      ;INT7 VECTOR ADDRESS
0000:2076   26                 ES
0000:2077   C7 06 3E 01 00 00  MOVW  013E, #0000      ;(SLAVE)

                              ;INITIALIZATION SEQUENCE FOR SLAVE
0000:207D   BA 90 00           MOVW  DX,#0090   ;ICW1
0000:2080   B0 15              MOVB  AL,#15     ;SGL MODE, ICW4 NEEDED
0000:2082   EE                 OUTB  DX         ;EDGE TRIGGERED INTERRUPT
0000:2083   BA 92 00           MOVW  DX,#0092   ;ICW2
0000:2086   B0 48              MOVB  AL,#48     ;BASE ADDRESS = 72d
0000:2088   EE                 OUTB  DX         ;FOR TYPE 48 INTERRUPT
0000:2089   B0 00              MOVB  AL,#00     ;ICW3 (SLAVE)
0000:208B   EE                 OUTB  DX         ;SLAVE ID = 000
0000:208C   B0 05              MOVB  AL,#05     ;ICW4
0000:208E   EE                 OUTB DX          ;86/88 MODE, AEOI
0000:208F   B0 00              MOVB AL, #00     ;OCW1
0000:2091   EE                 OUTB DX    ;NO INTERRUPTS MASKED ON SLAVE

                    ;INITIALIZATION SEQUENCE FOR MASTER INTERRUPT CONTROLLER
0000:2092   BA F4 FF          MOVW DX,#0FFF4    ;ICW1
0000:2095   B0 15             MOVB AL , #15     ;CAS MODE,ICW4 NEEDED
0000:2097   EE                OUTB DX           ;EDGE TRIGGERED INTERRRUPT
0000:2098   BA F6 FF          MOVW DX, #0FFF6   ;ICW2
```

```
0000:209B   B0 48               MOVB AL, #48        ;BASE ADDRESS =72d
0000:209D   EE                  OUTB DX
0000:209E   B0 01               MOVB AL, #01        ;ICW3 (MASTER)
0000:20A0   EE                  OUTB DX             ;IR0 HAS A SLAVE ON IT
0000:20A1   B0 0D               MOVB AL, #0D        ;ICW4 (MASTER)
0000:20A3   EE                  OUTB DX             ;86/88 MODE, AEOI
0000:20A4   B0 FE               MOVB AL, #0FE       ;OCW1 ALL INTERRUPTS
0000:20A6   EE                  OUTB DX             ;ARE MASKED EXCEPT INT0
0000:20A7   FB                  STI                 ;SET INTERRUPT FLAG
0000:20A8   EB FE               JMP  20A8

0000:20AA   0A 0A               DB   0A ,0A
0000:20AC   0D                  DB   0D
0000:20AD   49 4E 54 45 52 52 ASC  'INTERRUPT - `
0000:20B3   55 50 54 20 2D 20
0000:20B9   00                  DB  00
0000:20BA   20 4F 43 43 55      ASC `OCCURRED ! `
0000:20BF   52 52 45 44 21
0000:20C4   00                  DB  00

                                ORG   2200          :ISR FOR INTERRUPT 0
0000:2200   FA                  CLI
0000:2201   2E                  CS
0000:2202   8D 16 AA 20         LEA   DX, 20AA
0000:2206   BA C2               MOVW  AX,DX
0000:2208   9A 55 1B 00 FE      CALLS FE00:1B55
0000:220D   B0 30               MOVB  AL, #30
0000:220F   9A 50 1B 00 FE      CALLS FE00:1B50
0000:2214   2E                  CS
0000:2215   8D 16 BA 20         LEA   DX, 20BA
0000:2219   BA C2               MOVW  AX, DX
0000:221B   9A 55 1B 00 FE      CALLS FE00:1B55
0000:2220   CC                  INT3

                                ORG   2250          :ISR FOR INTERRUPT 1
0000:2250   FA                  CLI
0000:2251   2E                  CS
```

```
0000:2252   8D 16 AA 20        LEA   DX, 20AA
0000:2256   BA C2              MOVW  AX,DX
0000:2258   9A 55 1B 00 FE     CALLS FE00:1B55
0000:225D   B0 31              MOVB  AL, #31
0000:225F   9A 50 1B 00 FE     CALLS FE00:1B50
0000:2264   2E                 CS
0000:2265   8D 16 BA 20        LEA   DX, 20BA
0000:2269   BA C2              MOVW  AX,DX
0000:226B   9A 55 1B 00 FE     CALLS FE00:1B55
0000:2270   CC                 INT3

                               ORG   2300        :ISR FOR INTERRUPT 2
0000:2300   FA                 CLI
0000:2301   2E                 CS
0000:2302   8D 16 AA 20        LEA   DX, 20AA
0000:2306   BA C2              MOVW  AX,DX
0000:2308   9A 55 1B 00 FE     CALLS FE00:1B55
0000:230D   B0 32              MOVB  AL, #32
0000:230F   9A 50 1B 00 FE     CALLS FE00:1B50
0000:2314   2E                 CS
0000:2315   8D 16 BA 20        LEA   DX, 20BA
0000:2319   BA C2              MOVW  AX,DX
0000:231B   9A 55 1B 00 FE     CALLS FE00:1B55
0000:2320   CC                 INT3

                               ORG   2350        :ISR FOR INTERRUPT 3
0000:2350   FA                 CLI
0000:2351   2E                 CS
0000:2352   8D 16 AA 20        LEA   DX, 20AA
0000:2356   BA C2              MOVW  AX,DX
0000:2358   9A 55 1B 00 FE     CALLS FE00:1B55
0000:235D   B0 33              MOVB  AL, #33
0000:235F   9A 50 1B 00 FE     CALLS FE00:1B50
0000:2364   2E                 CS
0000:2365   8D 16 BA 20        LEA   DX, 20BA
0000:2369   BA C2              MOVW  AX,DX
0000:236B   9A 55 1B 00 FE     CALLS FE00:1B55
```

```
0000:2370   CC                INT3

                              ORG   2400        :ISR FOR INTERRUPT 4
0000:2400   FA                CLI
0000:2401   2E                CS
0000:2402   8D 16 AA 20       LEA   DX, 20AA
0000:2406   BA C2             MOVW  AX,DX
0000:2408   9A 55 1B 00 FE    CALLS FE00:1B55
0000:240D   B0 34             MOVB  AL, #34
0000:240F   9A 50 1B 00 FE    CALLS FE00:1B50
0000:2414   2E                CS
0000:2415   8D 16 BA 20       LEA   DX, 20BA
0000:2419   BA C2             MOVW  AX,DX
0000:241B   9A 55 1B 00 FE    CALLS FE00:1B55
0000:2420   CC                INT3

                              ORG   2450        :ISR FOR INTERRUPT 5
0000:2450   FA                CLI
0000:2451   2E                CS
0000:2452   8D 16 AA 20       LEA   DX, 20AA
0000:2456   BA C2             MOVW  AX,DX
0000:2458   9A 55 1B 00 FE    CALLS FE00:1B55
0000:245D   B0 35             MOVB  AL, #35
0000:245F   9A 50 1B 00 FE    CALLS FE00:1B50
0000:2464   2E                CS
0000:2465   8D 16 BA 20       LEA   DX, 20BA
0000:2469   BA C2             MOVW  AX,DX
0000:246B   9A 55 1B 00 FE    CALLS FE00:1B55
0000:2470   CC                INT3

                              ORG   2500        :ISR FOR INTERRUPT 6
0000:2500   FA                CLI
0000:2501   2E                CS
0000:2502   8D 16 AA 20       LEA   DX, 20AA
0000:2506   BA C2             MOVW  AX,DX
0000:2508   9A 55 1B 00 FE    CALLS FE00:1B55
0000:250D   B0 36             MOVB  AL, #36
```

```
0000:250F   9A 50 1B 00 FE    CALLS FE00:1B50
0000:2514   2E                CS
0000:2515   8D 16 BA 20       LEA   DX, 20BA
0000:2519   BA C2             MOVW  AX,DX
0000:251B   9A 55 1B 00 FE    CALLS FE00:1B55
0000:2520   CC                INT3

                              ORG   2550        :ISR FOR INTERRUPT 7
0000:2550   FA                CLI
0000:2551   2E                CS
0000:2552   8D 16 AA 20       LEA   DX, 20AA
0000:2556   BA C2             MOVW  AX,DX
0000:2558   9A 55 1B 00 FE    CALLS FE00:1B55
0000:255D   B0 37             MOVB  AL, #37
0000:255F   9A 50 1B 00 FE    CALLS FE00:1B50
0000:2564   2E                CS
0000:2565   8D 16 BA 20       LEA   DX, 20BA
0000:2569   BA C2             MOVW  AX,DX
0000:256B   9A 55 1B 00 FE    CALLS FE00:1B55
0000:2570   CC                INT3
```

5B. DEMONSTRATION PROGRAM FOR ESA 86/88-3 TRAINER

The following Program configures the Study Card's 8259 as Slave and onboard 8259 (i.e. Trainer's) as Master in cascade mode. The Slave interrupt will be connected to INT0 of Master. The interrupts to Slave can be given from on board dipswitch and push button. Keep the dipswitch SW1 for corresponding interrupt. Execute the program from 2000H. Then press the push button switch. Execute the program in serial mode.

*****Place a Jumper between A and B (INT0) of JP15 on the Trainer before executing the Program.***

Onboard (Trainer's) 8259 addresses are FFF4 and FFF6

Study Card's 8259 addresses are 0090 and 0092

```
                           ORG   2000H

0000:2000   B8 00 00      MOV     AX,0000H         ;INITIALIZE SEGMENT
0000:2003   8E C8         MOV     CS,AX            ;REGISTERS
0000:2005   8E C0         MOV     ES,AX
0000:2007   8E D0         MOV     SS,AX
0000:2009   BC 00 30      MOV     SP,3000H         ;INITIALIZE SP
            ;INTERRUPT VECTOR TABLE INITIALIZATION
0000:200C   BE 20 01      MOV     SI,0120H         ;INT0 VECTOR ADDRESS
0000:200F   B8 00 22      MOV     AX,2200H         ;0120H IS THE BASE OF INT
0000:2012   89 04         MOV     [SI],AX          ; VECTOR TABLE
0000:2014   83 C6 02      ADD     SI,02H
0000:2017   B8 00 00      MOV     AX,0000H
0000:201A   89 04         MOV     [SI],AX

0000:201C   83 C6 02      ADD     SI,02H           ;INT1 VECTOR ADDRESS
0000:201F   B8 10 22      MOV     AX,2210H
0000:2022   89 04         MOV     [SI],AX
0000:2024   83 C6 02      ADD     SI,02H
0000:2027   B8 00 00      MOV     AX,0000H
0000:202A   89 04         MOV     [SI],AX

0000:202C   83 C6 02      ADD     SI,02H           ;INT2 VECTOR ADDRESS
0000:202F   B8 20 22      MOV     AX,2220H
```

```
0000:2032   89 04        MOV    [SI],AX
0000:2034   83 C6 02     ADD    SI,02H
0000:2037   B8 00 00     MOV    AX,0000H
0000:203A   89 04        MOV    [SI],AX

0000:203C   83 C6 02     ADD    SI,02H        ;INT3 VECTOR ADDRESS
0000:203F   B8 30 22     MOV    AX,2230H
0000:2042   89 04        MOV    [SI],AX
0000:2044   83 C6 02     ADD    SI,02H
0000:2047   B8 00 00     MOV    AX,0000H
0000:204A   89 04        MOV    [SI],AX

0000:204C   83 C6 02     ADD    SI,02H        ;INT4 VECTOR ADDRESS
0000:204F   B8 40 22     MOV    AX,2240H
0000:2052   89 04        MOV    [SI],AX
0000:2054   83 C6 02     ADD    SI,02H
0000:2057   B8 00 00     MOV    AX,0000H
0000:205A   89 04        MOV    [SI],AX

0000:205C   83 C6 02     ADD    SI,02H        ;INT5 VECTOR ADDRESS
0000:205F   B8 50 22     MOV    AX,2250H
0000:2062   89 04        MOV    [SI],AX
0000:2064   83 C6 02     ADD    SI,02H
0000:2067   B8 00 00     MOV    AX,0000H
0000:206A   89 04        MOV    [SI],AX

0000:206C   83 C6 02     ADD    SI,02H        ;INT6 VECTOR ADDRESS
0000:206F   B8 60 22     MOV    AX,2260H
0000:2072   89 04        MOV    [SI],AX
0000:2074   83 C6 02     ADD    SI,02H
0000:2077   B8 00 00     MOV    AX,0000H
0000:207A   89 04        MOV    [SI],AX

0000:207C   83 C6 02     ADD    SI,02H        ;INT7 VECTOR ADDRESS
0000:207F   B8 70 22     MOV    AX,2270H
0000:2082   89 04        MOV    [SI],AX
0000:2084   83 C6 02     ADD    SI,02H
```

```
0000:2087   B8 00 00      MOV     AX,0000H
0000:208A   89 04         MOV     [SI],AX

;INITIALIZATION SEQUENCE FOR SLAVE (study card’s interrupt controller)
0000:208C   BA 90 00      MOV     DX,0090H        ;ICW1
0000:208F   B0 15         MOV     AL,15H          ;SGL MODE,ICW4
0000:2091   EE            OUT     DX,AL           ;EDGE TRIGGERED INTERRUPT
0000:2092   BA 92 00      MOV     DX,0092H        ;ICW2
0000:2095   B0 48         MOV     AL,48H          ;BASE ADDRESS
0000:2097   EE            OUT     DX,AL
0000:2098   B0 00         MOV     AL,00H          ;ICW3 (SLAVE)
0000:209A   EE            OUT     DX, AL          ;SLAVE ID = 0
0000:209B   B0 05         MOV     AL,05H          ;ICW4
0000:209D   EE            OUT     DX,AL           ;86/88 MODE,
0000:209E   B0 00         MOV     AL,00H          ;OCW1
0000:20A0   EE            OUT     DX,AL           ;NO INTERRUPTS MASKE

        ;INITIALIZATION SEQUENCE FOR MASTER INTERRUPT CONTROLLER
0000:20A1   BA F4 FF      MOV     DX,0FFF4H       ;ICW1
0000:20A4   B0 15         MOV     AL,15H          ;CAS MODE,ICW4 NEED
0000:20A6   EE            OUT     DX,AL           ;EDGE TRIGGERED INT
0000:20A7   BA F6 FF      MOV     DX,0FFF6H       ;ICW2
0000:20AA   B0 48         MOV     AL,48H          ;BASE ADDRESS =72d
0000:20AC   EE            OUT     DX,AL
0000:20AD   B0 01         MOV     AL,01H          ;ICW3 (MASTER)
0000:20AF   EE            OUT     DX,AL           ;IR0 HAS A SLAVE ON
0000:20B0   B0 0D         MOV     AL,0DH          ;ICW4 (MASTER)
0000:20B2   EE            OUT     DX,AL           ;86/88 MODE AEOI
0000:20B3   B0 FE         MOV     AL,0FEH         ;OCW1
0000:20B5   EE            OUT     DX,AL           ;ALL BUT IR0 MASKED
0000:20B6   FB            STI                     ;SET INTERRUPT FLAG
0000:20B7   E9 FD FF HERE:JMP     HERE

                             ORG   2100H           ;MESSAGES FOR ISRs
0000:2100 20 20 0A 49 4E 54 MSG0:DB 20H,20H,0AH,'INT0 OCCURRED',0AH,0DH,00H
0000:2106 30 20 4F 43 43 55
0000:210C 52 52 45 44 0A 0D
```

```
0000:2112 00
0000:2113 20 20 0A 49 4E 54 MSG1:DB 20H,20H,0AH,'INT1 OCCURRED',0AH,0DH,00H
0000:2119 31 20 4F 43 43 55
0000:211F 52 52 45 44 0A 0D
0000:2125 00
0000:2126 20 20 0A 49 4E 54 MSG2:DB 20H,20H,0AH,'INT2 OCCURRED',0AH,0DH,00H
0000:212C 32 20 4F 43 43 55
0000:2132 52 52 45 44 0A 0D
0000:2138 00
0000:2139 20 20 0A 49 4E 54 MSG3:DB 20H,20H,0AH,'INT3 OCCURRED',0AH,0DH,00H
0000:213F 33 20 4F 43 43 55
0000:2145 52 52 45 44 0A 0D
0000:214B 00
0000:214C 20 20 0A 49 4E 54 MSG4:DB 20H,20H,0AH,'INT4 OCCURRED',0AH,0DH,00H
0000:2152 34 20 4F 43 43 55
0000:2158 52 52 45 44 0A 0D
0000:215E 00
0000:215F 20 20 0A 49 4E 54 MSG5:DB 20H,20H,0AH,'INT5 OCCURRED',0AH,0DH,00H
0000:2165 35 20 4F 43 43 55
0000:216B 52 52 45 44 0A 0D
0000:2171 00
0000:2172 20 20 0A 49 4E 54 MSG6:DB 20H,20H,0AH,'INT6 OCCURRED',0AH,0DH,00H
0000:2178 36 20 4F 43 43 55
0000:217E 52 52 45 44 0A 0D
0000:2184 00
0000:2185 20 20 0A 49 4E 54 MSG7:DB 20H,20H,0AH,'INT7 OCCURRED',0AH,0DH,00H
0000:218B 37 20 4F 43 43 55
0000:2191 52 52 45 44 0A 0D 00
                              ORG     2200H              ;ISR FOR INTERRUPT0
0000:2200   FA                CLI
0000:2201   2E 8D 16 00 21 LEA     DX,MSG0
0000:2206   E9 71 00          JMP     DISP
0000:2209   CC                INT     03H

                              ORG     2210H             ;ISR FOR INTERRUPT1
0000:2210   FA                CLI
0000:2211   2E 8D 16 13 21 LEA     DX,MSG1
```

```
0000:2216   E9 61 00        JMP     DISP
0000:2219   CC              INT     03H

                            ORG     2220H               ;ISR FOR INTERRUPT2
0000:2220   FA              CLI
0000:2221   2E 8D 16 26 21  LEA     DX,MSG2
0000:2226   E9 51 00        JMP     DISP
0000:2229   CC              INT     03H

                            ORG     2230H               ;ISR FOR INTERRUPT3
0000:2230   FA              CLI
0000:2231   2E 8D 16 39 21  LEA     DX,MSG3
0000:2236   E9 41 00        JMP     DISP
0000:2239   CC              INT     03H

                            ORG     2240H               ;ISR FOR INTERRUPT4
0000:2240   FA              CLI
0000:2241   2E 8D 16 4C 21  LEA     DX,MSG4
0000:2246   E9 31 00        JMP     DISP
0000:2249   CC              INT     03H

                            ORG     2250H               ;ISR FOR INTERRUPT5
0000:2250   FA              CLI
0000:2251   2E 8D 16 5F 21  LEA     DX,MSG5
0000:2256   E9 21 00        JMP     DISP
0000:2259   CC              INT     03H
0000:225A
                            ORG     2260H               ;ISR FOR INTERRUPT6
0000:2260   FA              CLI
0000:2261   2E 8D 16 72 21  LEA     DX,MSG6
0000:2266   E9 11 00        JMP     DISP
0000:2269   CC              INT     03H

                            ORG     2270H               ;ISR FOR INTERRUPT7
0000:2270   FA              CLI
0000:2271   2E 8D 16 85 21  LEA     DX,MSG7
0000:2276   E9 01 00        JMP     DISP
```

```
0000:2279   CC              INT     03H

0000:227A   8B C2   DISP:  MOV     AX,DX
0000:227C   9A 13 00 00 FE CALL FAR 0FE00:0013H
0000:2281   CC              INT     03H
```

5C. DEMONSTRATION PROGRAM FOR ESA 86E Ver 2.00 TRAINER

Connect 26 –Pin FRCs between the J3 & J4 of the Study Card and J4 & J6 of Trainer respectively. The following demo Program Enables all the interrupts of 8259. User can give interrupts to 8259 using onboard dipswitch and push button. Execute the program from 2000H in Serial mode only. The program will be continuously polling for the interrupt, so press reset on trainer to come out of program.

ADDRESSES OF 8259 ARE   FFC8 AND FFCA

```
                            ORG     2000H
0000:2000   B8 00 00        MOV     AX,0000H
0000:2003   8E C8           MOV     CS,AX
0000:2005   8E C0           MOV     ES,AX
0000:2007   8E D0           MOV     SS,AX
0000:2009   BC 00 30        MOV     SP,3000H
0000:200C   BE 20 01        MOV     SI,0120H            ;INT0 VECTOR ADDRESS
0000:200F   B8 00 22        MOV     AX,2200H            ;0120H IS THE BASE OF
0000:2012   89 04           MOV     [SI],AX             ;INT VECTOR TABLE
0000:2014   83 C6 02        ADD     SI,02H
0000:2017   B8 00 00        MOV     AX,0000H
0000:201A   89 04           MOV     [SI],AX
0000:201C   83 C6 02        ADD     SI,02H              ;INT1 VECTOR ADDRESS
0000:201F   B8 10 22        MOV     AX,2210H
0000:2022   89 04           MOV     [SI],AX
0000:2024   83 C6 02        ADD     SI,02H
0000:2027   B8 00 00        MOV     AX,0000H
0000:202A   89 04           MOV     [SI],AX
0000:202C   83 C6 02        ADD     SI,02H              ;INT2 VECTOR ADDRESS
0000:202F   B8 20 22        MOV     AX,2220H
0000:2032   89 04           MOV     [SI],AX
0000:2034   83 C6 02        ADD     SI,02H
0000:2037   B8 00 00        MOV     AX,0000H
0000:203A   89 04           MOV     [SI],AX
0000:203C   83 C6 02        ADD     SI,02H              ;INT3 VECTOR ADDRESS
```

```
0000:203F   B8 30 22      MOV    AX,2230H
0000:2042   89 04         MOV    [SI],AX
0000:2044   83 C6 02      ADD    SI,02H
0000:2047   B8 00 00      MOV    AX,0000H
0000:204A   89 04         MOV    [SI],AX
0000:204C   83 C6 02      ADD    SI,02H              ;INT4 VECTOR ADDRESS
0000:204F   B8 40 22      MOV    AX,2240H
0000:2052   89 04         MOV    [SI],AX
0000:2054   83 C6 02      ADD    SI,02H
0000:2057   B8 00 00      MOV    AX,0000H
0000:205A   89 04         MOV    [SI],AX
0000:205C   83 C6 02      ADD    SI,02H                ;INT5 VECTOR ADDRESS
0000:205F   B8 50 22      MOV    AX,2250H
0000:2062   89 04         MOV    [SI],AX
0000:2064   83 C6 02      ADD    SI,02H
0000:2067   B8 00 00      MOV    AX,0000H
0000:206A   89 04         MOV    [SI],AX
0000:206C   83 C6 02      ADD    SI,02H               ;INT6 VECTOR ADDRESS
0000:206F   B8 60 22      MOV    AX,2260H
0000:2072   89 04         MOV    [SI],AX
0000:2074   83 C6 02      ADD    SI,02H
0000:2077   B8 00 00      MOV    AX,0000H
0000:207A   89 04         MOV    [SI],AX
0000:207C   83 C6 02      ADD    SI,02H               ;INT7 VECTOR ADDRESS
0000:207F   B8 70 22      MOV    AX,2270H
0000:2082   89 04         MOV    [SI],AX
0000:2084   83 C6 02      ADD    SI,02H
0000:2087   B8 00 00      MOV    AX,0000H
0000:208A   89 04         MOV    [SI],AX
                                               ;8259   INTIALIZATION
0000:208C   BA C8 FF      MOV    DX,0FFC8H
0000:208F   B0 17         MOV    AL,17H        ;ICW1 (IC4 NEEDED, SINGLE,
0000:2091   EE            OUT    DX,AL         ; INTERVAL 4 ,EDGE TRIG INT)
0000:2092   BA CA FF      MOV    DX,0FFCAH   ;ICW2 (MULTIPLE FOR INT VECTOR
0000:2095   B0 48         MOV    AL,48H      ;ADDRESS TABLE)FOR MAKING 120H
0000:2097   EE            OUT    DX,AL  ;AS BASE ADDRESS OF INT VECT TABLE
0000:2098   B0 03         MOV    AL,03H      ;ICW4 (8086 MODE, AUTO EOI)
```

```
0000:209A   EE              OUT     DX,AL
0000:209B   B0 00           MOV     AL,00H       ;OCW1 (ENABLE ALL INTERRUPTS)
0000:209D   EE              OUT     DX,AL
0000:209E   FB              STI                 ;ENABLE INTR OF (8086) TRAINER
0000:209F   E9 FD FF HERE:JMP     HERE


                                ORG    2100H      ;MESSAGES FOR ISRs
0000:2100   20 20 0A 49 4E 54 MSG0: DB  20H,20H,0AH,'INT0 OCCURRED',0AH,0DH
0000:2106   30 20 4F 43 43 55
0000:210C   52 45 44 0A 0D

0000:2111   20 20 0A 49 4E 54 MSG1: DB  20H,20H,0AH,'INT1 OCCURRED',0AH,0DH
0000:2117   31 20 4F 43 43 55
0000:211D   52 45 44 0A 0D

0000:2122   20 20 0A 49 4E 54 MSG2: DB  20H,20H,0AH,'INT2 OCCURRED',0AH,0DH
0000:2128   32 20 4F 43 43 55
0000:212E   52 45 44 0A 0D

0000:2133   20 20 0A 49 4E 54 MSG3: DB  20H,20H,0AH,'INT3 OCCURRED',0AH,0DH
0000:2139   33 20 4F 43 43 55
0000:213F   52 45 44 0A 0D

0000:2144   20 20 0A 49 4E 54 MSG4: DB  20H,20H,0AH,'INT4 OCCURRED',0AH,0DH
0000:214A   34 20 4F 43 43 55
0000:2150   52 45 44 0A 0D

0000:2155   20 20 0A 49 4E 54 MSG5: DB  20H,20H,0AH,'INT5 OCCURRED',0AH,0DH
0000:215B   35 20 4F 43 43 55
0000:2161   52 45 44 0A 0D

0000:2166   20 20 0A 49 4E 54 MSG6: DB  20H,20H,0AH,'INT6 OCCURRED',0AH,0DH
0000:216C   36 20 4F 43 43 55
0000:2172   52 45 44 0A 0D

0000:2177   20 20 0A 49 4E 54 MSG7: DB  20H,20H,0AH,'INT7 OCCURRED',0AH,0DH
```

```
0000:217D   37 20 4F 43 43 55
0000:2183   52 45 44 0A 0D



                            ORG     2200H           ;INT0 ISR
0000:2200   FA              CLI
0000:2201   2E 8D 16 00 21  LEA     DX,MSG0
0000:2206   E9 F7 00        JMP     DISP
0000:2209   CC              INT     03

                            ORG     2210H           ;INT1 ISR
0000:2210   FA              CLI
0000:2211   2E 8D 16 11 21  LEA     DX,MSG1
0000:2216   E9 E7 00        JMP     DISP
0000:2219   CC              INT     03

                            ORG     2220H           ;INT2 ISR
0000:2220   FA              CLI
0000:2221   2E 8D 16 22 21  LEA     DX,MSG2
0000:2226   E9 D7 00        JMP     DISP
0000:2229   CC              INT     03

                            ORG     2230H           ;INT3 ISR
0000:2230   FA              CLI
0000:2231   2E 8D 16 33 21  LEA     DX,MSG3
0000:2236   E9 C7 00        JMP     DISP
0000:2239   CC              INT     03

                            ORG     2240H           ;INT4 ISR
0000:2240   FA              CLI
0000:2241   2E 8D 16 44 21  LEA     DX,MSG4
0000:2246   E9 B7 00        JMP     DISP
0000:2249   CC              INT     03

                            ORG     2250H           ;INT5 ISR
0000:2250   FA              CLI
```

```
0000:2251   2E 8D 16 55 21  LEA     DX,MSG5
0000:2256   E9 A7 00        JMP     DISP
0000:2259   CC              INT     03


                            ORG     2260H      ;INT6 ISR
0000:2260   FA              CLI
0000:2261   2E 8D 16 66 21  LEA     DX,MSG6
0000:2266   E9 97 00        JMP     DISP
0000:2269   CC              INT     03

                            ORG     2270H      ;INT7 ISR
0000:2270   FA              CLI
0000:2271   2E 8D 16 77 21  LEA     DX,MSG7
0000:2276   E9 87 00        JMP     DISP
0000:2279   CC              INT     03

                            ORG     2300H       ;COMMON DISPLAY ROUTINE
0000:2300   8B F2     DISP: MOV     SI,DX       ;FOR ALL ISRs
0000:2302   B9 11 00        MOV     CX,011H
0000:2305   8A 04      L1:  MOV     AL,[SI]
0000:2307   9A 00 00 00 FE  CALL FAR 0FE00:0000H  ;CALL ROUTINE TO
0000:230C   46              INC     SI            ; DISPLAY THE MSGS
0000:230D   E2 F6           LOOP    L1
0000:230F   FB              STI
0000:2310   CF              IRET                 ;RETURN FROM INTERRUPT
```

6.DEMONSTRATION PROGRAM FOR 8051 SERIES KITS.
6A. DEMONSTRATION PROGRAM FOR ESA 51E / ESA51E Ver 4.00 TRAINER

The following program demonstrates the Polled Mode operation of 8259, the program first initializes the 8259 for interrupts using ICW1, ICW4 and OCW2. The interrupt output from the 8259 is connected to External interrupt (INT1) of the micro controller. The program also enables the INT1of the micro controller. Select the interrupt number using 4-way dipswitch and press the push button switch to give the interrupt to 8259, now the 8259 will interrupt the Trainer. The ISR of the INT1 will read the Interrupt Request Register of 8259 in Poll mode.

The program displays the corresponding interrupt number on Serial or on LCD depends on the mode of operation of the Trainer.

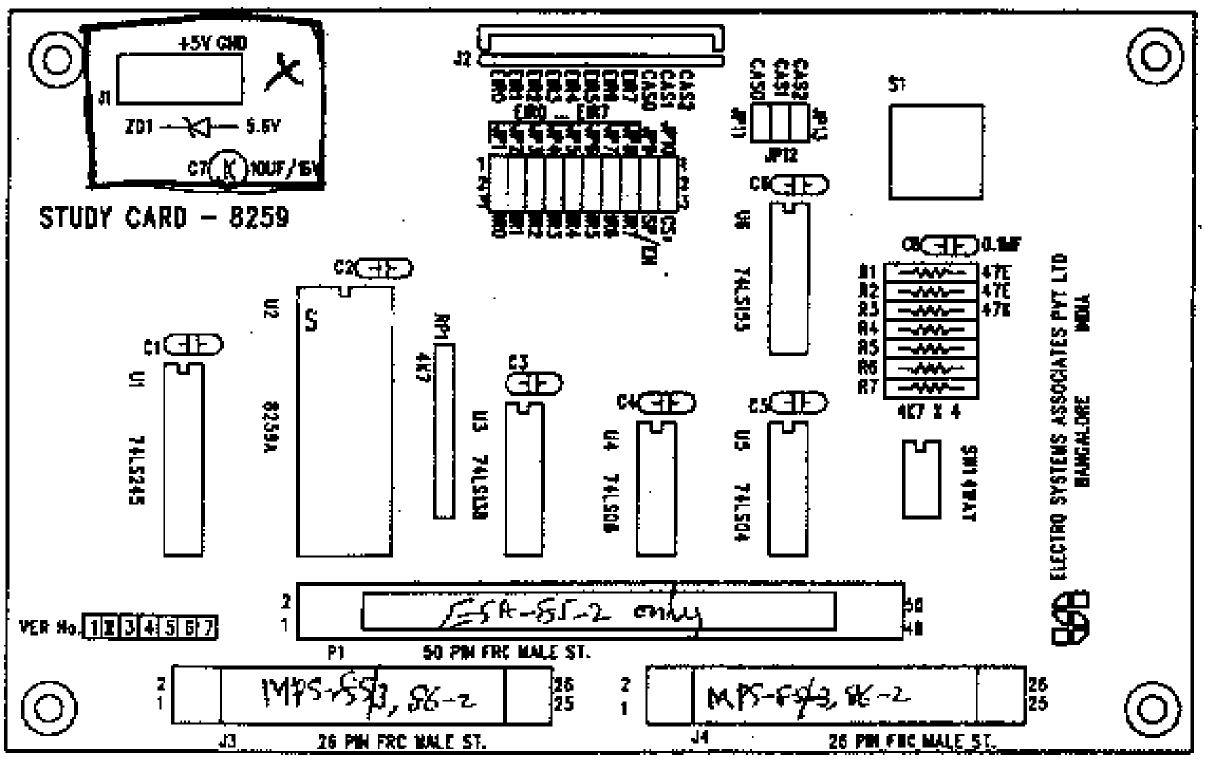
ADDRESSES OF 8259 ARE F190 AND F191

```
                        ORG      8000H

8000    75 A0 F1     MOV    P2,#0F1H          ;F190H ONE OF 8259 ADDRESSES
8003    78 90        MOV    R0,#90H
8005    74 17        MOV    A,#17H            ;ICW1 (ICW4, SINGLE, INTERVAL4,
8007    F2           MOVX   @R0,A             ;EDGE TRIGGERED INTERRUPT)
8008    78 91        MOV    R0,#91H           ;F191H ONE OF 8259 ADDRESSES
800A    74 02        MOV    A,#02H            ;ICW4(8085 MODE)
800C    F2           MOVX   @R0,A
800D    74 00        MOV    A,#00H            ;OCW1(ENABLE ALL INTERRUPTS)
800F    F2           MOVX   @R0,A
8010    78 90        MOV    R0,#90H
8012    D2 8A        SETB   TCON.2            ;SELECT EDGE TRIGGER FOR ExINT1
8014    75 A8 84     MOV    IE,#84H           ;ENABLE THE INTERRUPT
8017    80 FE HERE:  SJMP   HERE              ;WAIT FOR THE INTERRUPT

                     ORG   0FFF3H             ;ISR LOCATION FOR INT1 of TRAINER
FFF3    02 81 00     LJMP   8100H              ;JUMP TO 8100H
                     ORG    8100H
8100    78 90        MOV    R0,#90H
8102    74 0E        MOV    A,#0EH      ;OCW3( SELECT THE POLLING MODE OF 8259)
8104    F2           MOVX   @R0,A       ;TO READ THE IR REGISTER
8105    E2           MOVX   A,@R0       ;READ THE IR REGISTER FOR INT NUMBER
8106    54 07        ANL    A,#07H      ;FIND THE INTERRUPT REQUEST NUMBER
8108    25 E0        ADD    A,A         ;ADD THE OFFSET TO JUMP LOCATION
810A    90 82 00     MOV    DPTR,#8200H
```

```
810D   73          JMP   @A+DPTR
810E   02 00 03    LJMP  03H
                   ORG   8200H

8200   41 13       AJMP    INT0            ;JUMP INT0 ROUTINE
8202   41 1F       AJMP    INT1            ;JUMP INT1 ROUTINE
8204   41 2B       AJMP    INT2            ;JUMP INT2 ROUTINE
8206   41 37       AJMP    INT3            ;JUMP INT3 ROUTINE
8208   41 43       AJMP    INT4            ;JUMP INT4 ROUTINE
820A   41 4F       AJMP    INT5            ;JUMP INT5 ROUTINE
820C   41 5B       AJMP    INT6            ;JUMP INT6 ROUTINE
820E   41 67       AJMP    INT7            ;JUMP INT7 ROUTINE
8210   02 00 03    LJMP    03H

8213   90 85 00  INT0: MOV   DPTR,#MSG0  ;TO DISPLAY THE MESSAGE
8216   C2 D5           CLR   PSW.5        ; INT0 OCCURRED
8218   12 03 FA        LCALL 03FAH       ;CALL ROUTINE TO DISPLAY THE MESSAGE
821B   74 60           MOV   A,#60H       ;CLEAR THE INTERRUPT REQUEST WITH
821D   F2              MOVX  @R0,A        ;SPECIFIC EOI COMMAND USING OCW2
821E   32              RETI               ;RETURN FROM INTERRUPT

821F   90 85 13  INT1: MOV     DPTR,#MSG1
8222   C2 D5           CLR     PSW.5
8224   12 03 FA        LCALL   03FAH
8227   74 61           MOV     A,#61H
8229   F2              MOVX    @R0,A
822A   32              RETI

822B   90 85 26  INT2: MOV     DPTR,#MSG2
822E   C2 D5           CLR     PSW.5
8230   12 03 FA        LCALL   03FAH
8233   74 62           MOV     A,#62H
8235   F2              MOVX    @R0,A
8236   32              RETI

8237   90 85 39  INT3: MOV     DPTR,#MSG3
823A   C2 D5           CLR     PSW.5
```

```
823C   12 03 FA          LCALL   03FAH
823F   74 63             MOV     A,#63H
8241   F2                MOVX    @R0,A
8242   32                RETI

8243   90 85 4C   INT4:  MOV     DPTR,#MSG4
8246   C2 D5             CLR     PSW.5
8248   12 03 FA          LCALL   03FAH
824B   74 64             MOV     A,#64H
824D   F2                MOVX    @R0,A
824E   32                RETI

824F   90 85 5F   INT5:  MOV     DPTR,#MSG5
8252   C2 D5             CLR     PSW.5
8254   12 03 FA          LCALL   03FAH
8257   74 65             MOV     A,#65H
8259   F2                MOVX    @R0,A
825A   32                RETI

825B   90 85 72   INT6:  MOV     DPTR,#MSG6
825E   C2 D5             CLR     PSW.5
8260   12 03 FA          LCALL   03FAH
8263   74 66             MOV     A,#66H
8265   F2                MOVX    @R0,A
8266   32                RETI

8267   90 85 85   INT7:  MOV     DPTR,#MSG7
826A   C2 D5             CLR     PSW.5
826C   12 03 FA          LCALL   03FAH
826F   74 67             MOV     A,#67H
8271   F2                MOVX    @R0,A
8272   32                RETI

                         ORG     8500H   ;LOOK UP TABLE TO STORE THE MESSAGES

8500   20 20 0A 49 4E    MSG0:   DB  20H,20H,0AH,'INT0 OCCURRED',0AH,0DH,00H
8505   54 30 20 4F 43
```

```
850A   43 55 52 52 45
850F   44 0A 0D 00

8513   20 20 0A 49 4E  MSG1:   DB  20H,20H,0AH,'INT1 OCCURRED',0AH,0DH,00H
8518   54 31 20 4F 43
851D   43 55 52 52 45
8522   44 0A 0D 00

8526   20 20 0A 49 4E MSG2:    DB  20H,20H,0AH,'INT2 OCCURRED',0AH,0DH,00H
852B   54 32 20 4F 43
8530   43 55 52 52 45
8535   44 0A 0D 00

8539   20 20 0A 49 4E MSG3:    DB  20H,20H,0AH,'INT3 OCCURRED',0AH,0DH,00H
853E   54 33 20 4F 43
8543   43 55 52 52 45
8548   44 0A 0D 00

854C   20 20 0A 49 4E MSG4:    DB  20H,20H,0AH,'INT4 OCCURRED',0AH,0DH,00H
8551   54 34 20 4F 43
8556   43 55 52 52 45
855B   44 0A 0D 00

855F   20 20 0A 49 4E MSG5:    DB  20H,20H,0AH,'INT5 OCCURRED',0AH,0DH,00H
8564   54 35 20 4F 43
8569   43 55 52 52 45
856E   44 0A 0D 00

8572   20 20 0A 49 4E MSG6:    DB   20H,20H,0AH,'INT6 OCCURRED',0AH,0DH,00H
8577   54 36 20 4F 43
857C   43 55 52 52 45
8581   44 0A 0D 00
8585   20 20 0A 49 4E MSG7:    DB   20H,20H,0AH,'INT7 OCCURRED',0AH,0DH,00H
858A   54 37 20 4F 43
858F   43 55 52 52 45
8594   44 0A 0D 00
```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5.6V
C7
10UF/16V
J2
U2
8259A
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U3
74LS138
U4
74LS08
U5
74LS04
U6
74LS153
RP1
4K7
R1
R2
R3
R4
R5
R6
R7
47E
4K7 X 4
0.1MF
SW1 4WAY
S1
JP11
JP12
JP13
CAS0
CAS1
CAS2
VER No. 1 2 3 4 5 6 7
P1
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ESA-85-2 only
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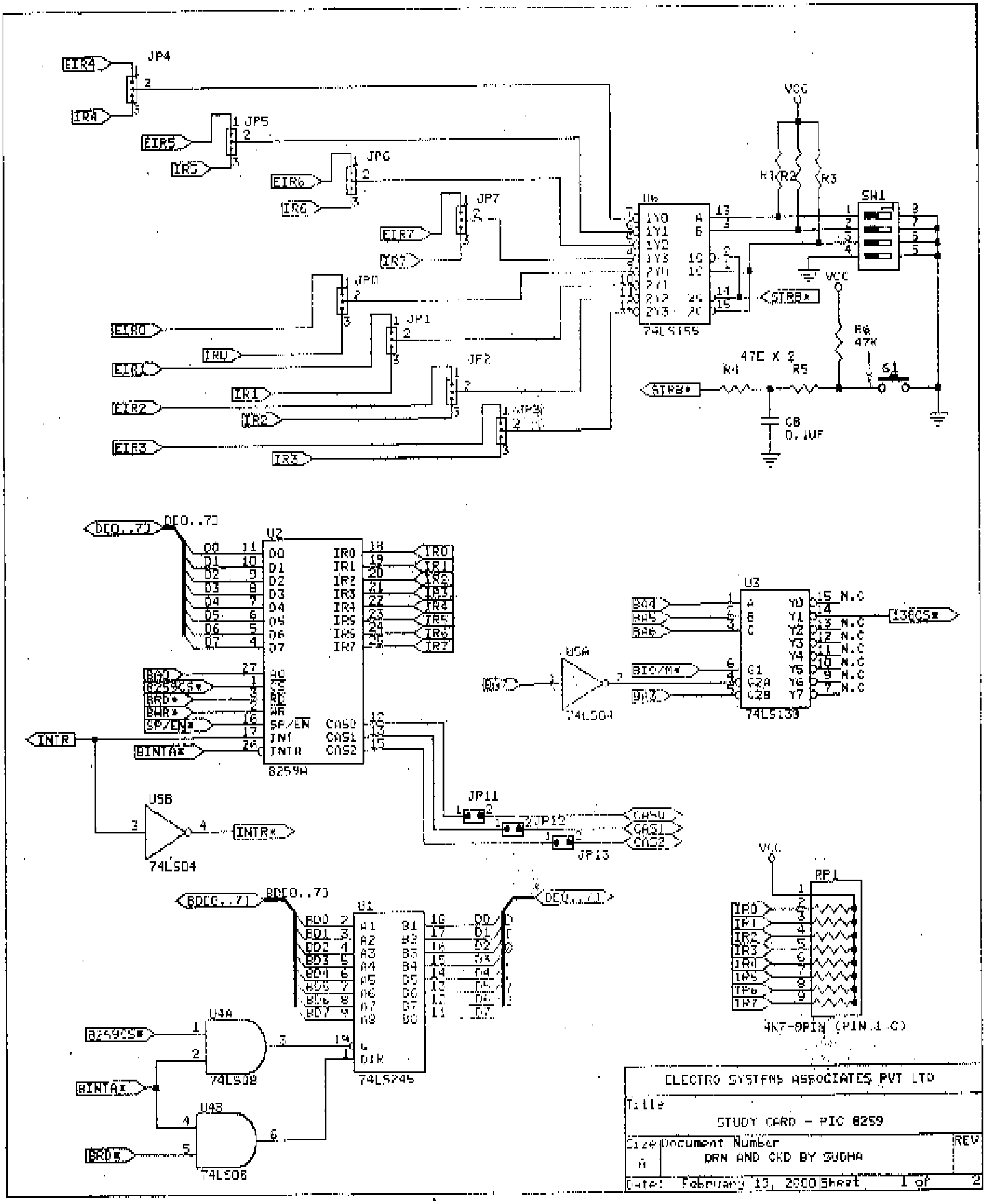
ELECTRO SYSTEMS ASSOCIATES PVT LTD
BANGALORE
INDIA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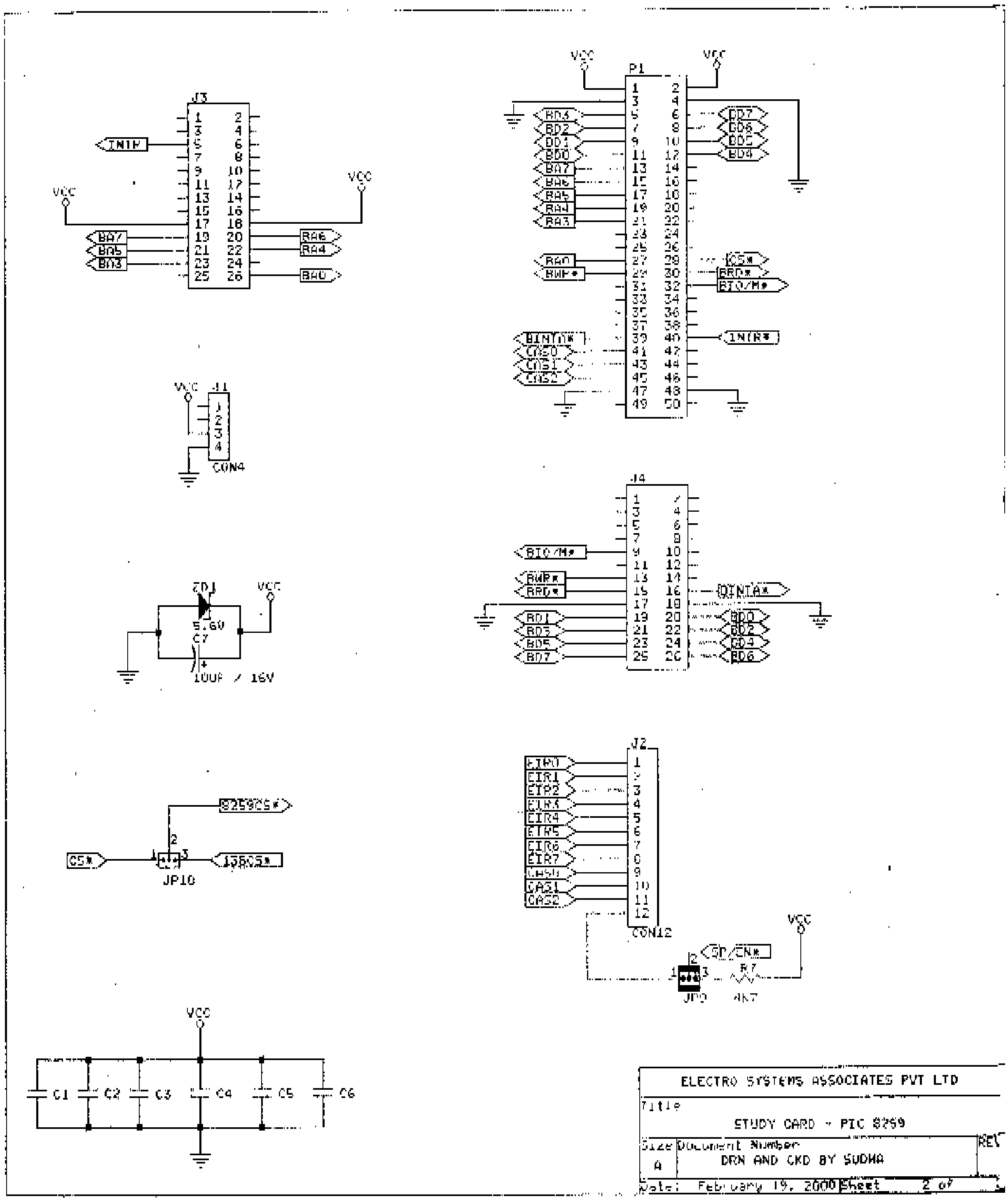
Sheet 1 of 2



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C7
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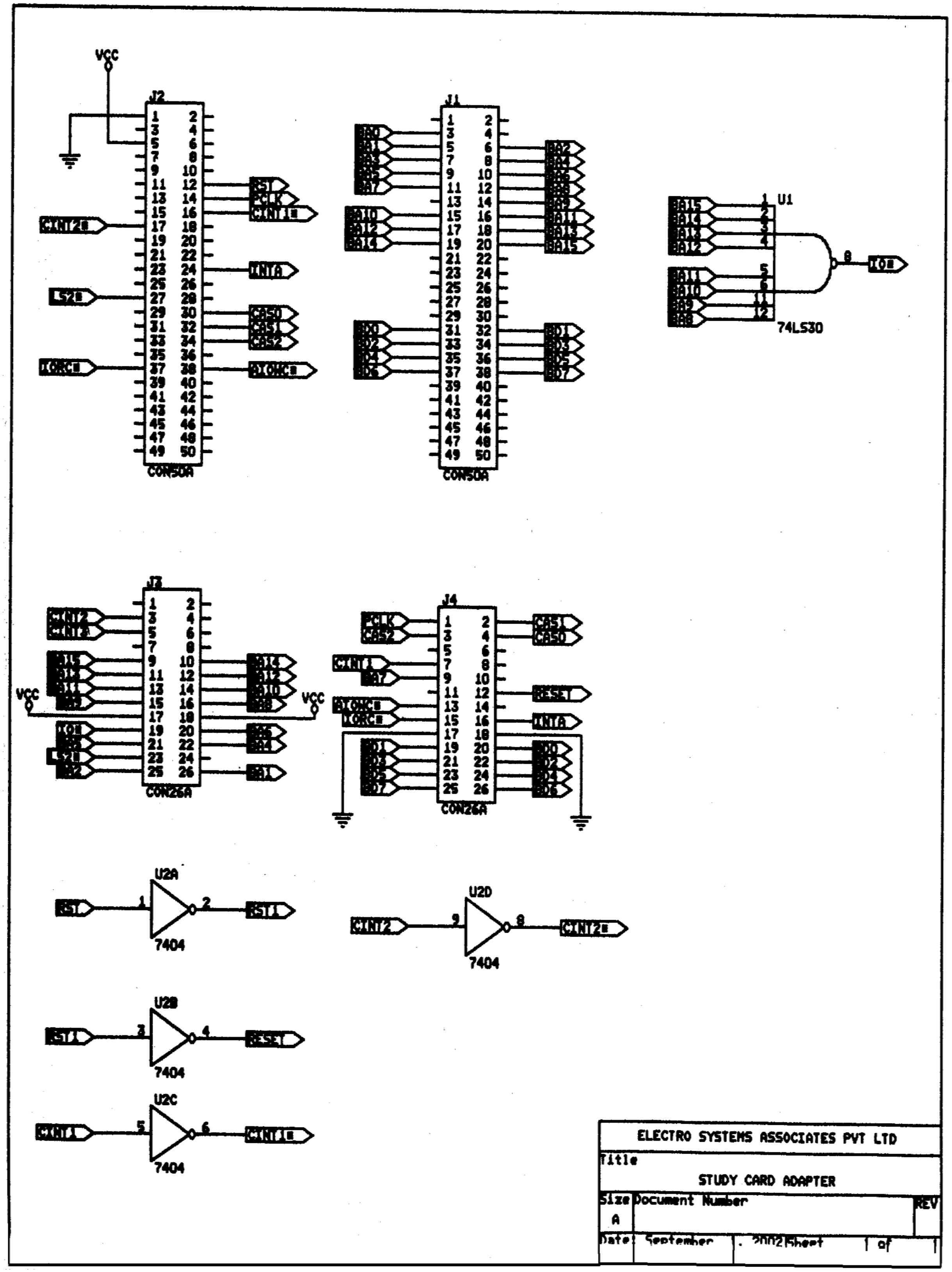

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