QuickWorks® Tutorial User Manual

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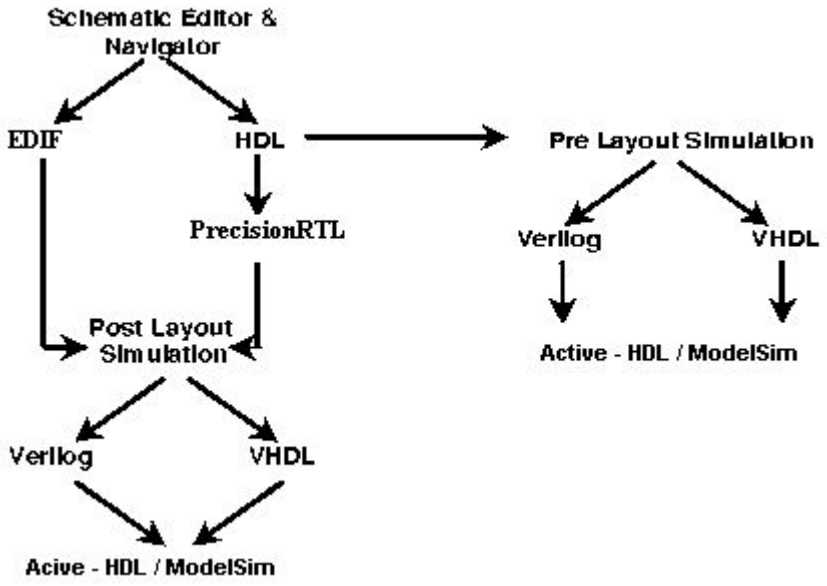
Chapter 1
Schematic Design Tutorial

This tutorial describes the QuickWorks Schematic Design process. To become familiar with the design process, you will create a top-level schematic containing a simple 4-bit counter. For more details on design flows and the QuickWorks tools, refer to the *Design Overview* chapter of the *QuickWorks User Manual*.

This chapter contains the following sections:

1.1 Functional Overview

Figure 1-1: Schematic Entry Design Flow



As the design flow presented in **Figure 1-1** illustrates, in this tutorial you will:

- Launch SpDE
- Launch the Schematic Editor and Hierarchy Navigator tools
- Create a schematic design
- Use the Hierarchy Navigator to inspect the design
- Export the Verilog functional simulation netlist
- Create the simulation stimuli
- Simulate the design for functionality using Active-HDL
- View the simulation results in the Data Analyzer
- Create and load an EDIF netlist into SpDE, where the design will be automatically optimized, placed, and routed
- Simulate the design for timing using Active-HDL

NOTE: This tutorial assumes that you have a working knowledge of Microsoft Windows. The *Getting Started* and *Basic Skills* chapters of the *Microsoft Windows User's Guide* contains a great deal of useful information for those new to Windows.

The following sections describe how to create a low level schematic-based design.

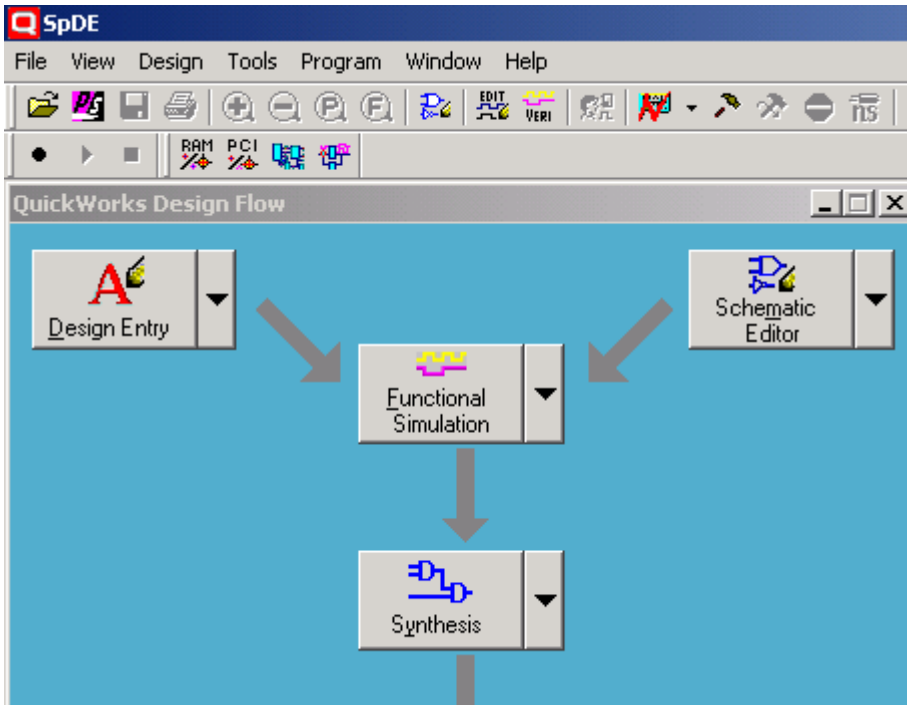
1.2 Creating a Schematic Design

1.2.1 Entering a Schematic Design

To enter a schematic design:

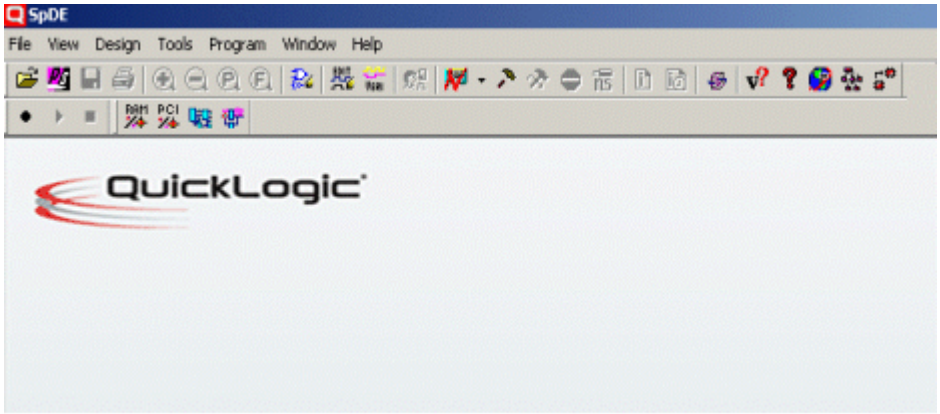
1. Select **Start>Programs>QuickLogic>SpDE**, or click the **SpDE** icon on your desktop.

   The SpDE window is displayed and all of the QuickWorks design resources are now available for use.



2. Close the QuickWorks Design Flow window by clicking the **X** in the upper right corner. This method of design will not be used for this tutorial.

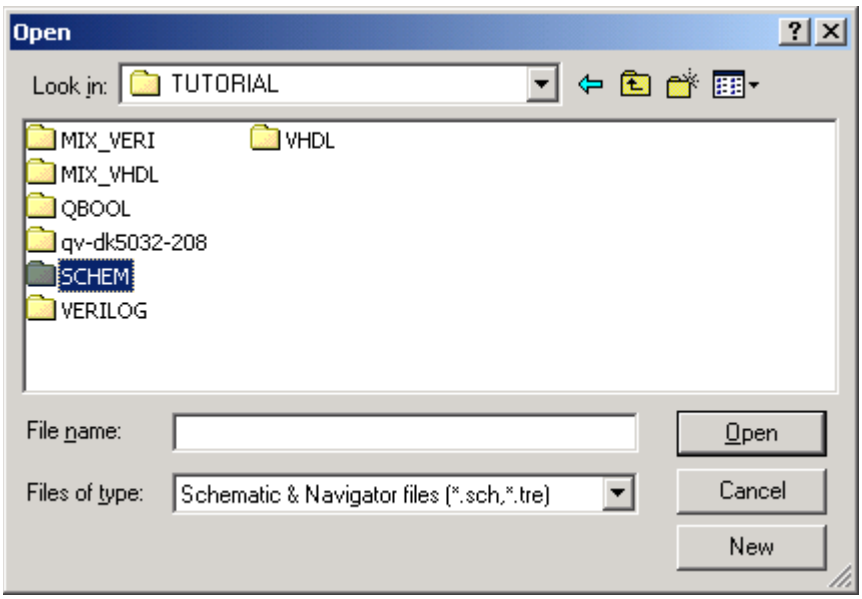
   The SpDE window is displayed. The SpDE toolbar contains icon buttons for executing commands quickly. The status bar at the bottom of the SpDE window displays status messages periodically.



NOTE: See the SpDE Menu Command Reference chapter of the *QuickWorks User Manual* for a full explanation of all available icons.

3. From the SpDE menu bar, select **Design>Schematic Editor & Navigator**, or click the  icon.

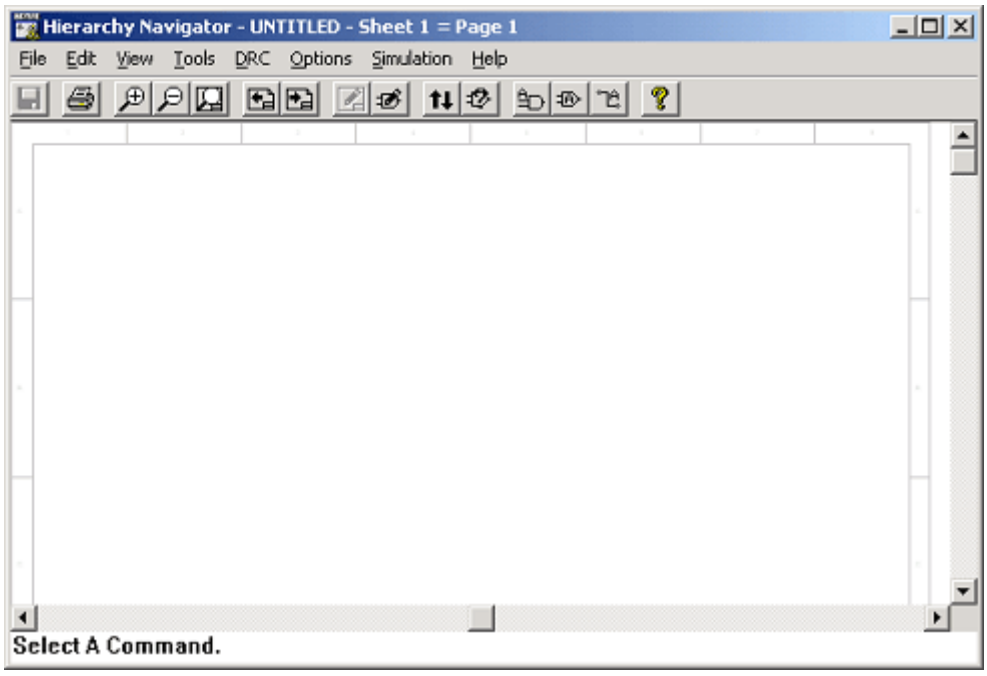
   The Open window is displayed.



4. Navigate to the default directory `C:\pasic\design\TUTORIAL\SCHEM\.`

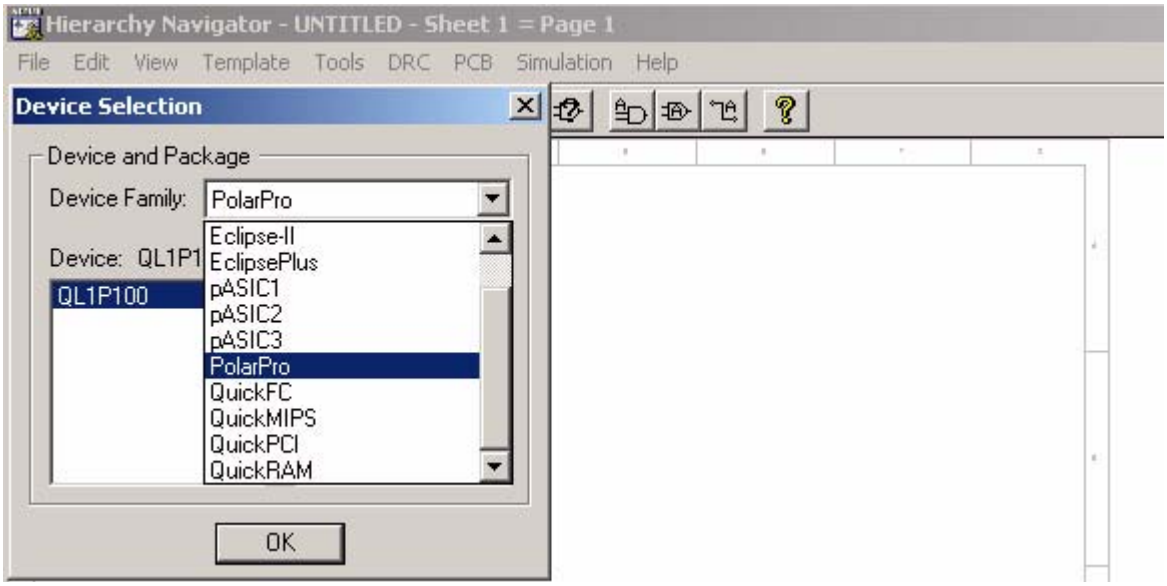
5. Click **New**.

   The Hierarchy Navigator window is displayed.



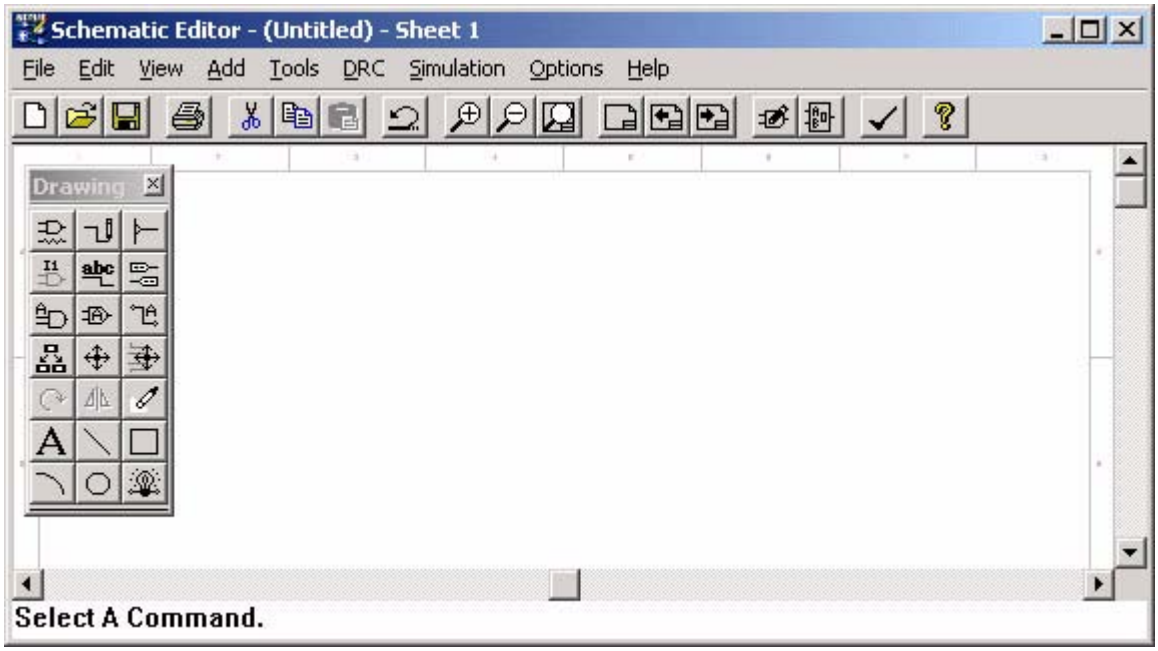
6. From the Hierarchy Navigator menu bar, select **File>Create Schematic**.

The Device Selection window is displayed.



7. Select **PolarPro** for the Device Family, **QL1P100** for the Device, and **PF144** for the Package.
8. Click **OK**.

   The Schematic Editor is displayed.



9. Click the **Maximize** button in the upper-right corner to enlarge the window to full screen.
10. Select **View>Full Fit**.

    Click anywhere within the schematic border to perform this operation.
11. Select **View>Zoom In**.

    Position the cursor in the upper-left corner of the schematic view and click to increase the magnification. Repeat this operation until you can read the border marks.

1.2.1.1 Adding Symbols

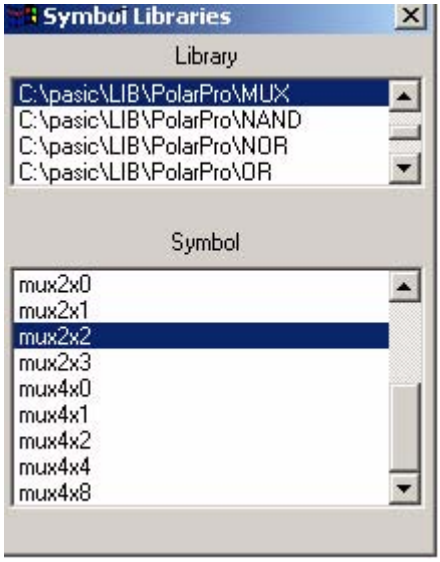
To add symbols to the schematic design:

1. From the Schematic Editor menu bar, select **Add>Symbol.**

   The Symbol Libraries window is displayed.

2. In the Library list, scroll down and select the library **C:\pasic\LIB\PolarPro\MUX**.

   The Symbol list displays all macros in this portion of the library. For a description of the library naming conventions, refer to the *Macro Library* chapter of the *QuickWorks User Manual*, or to the on-line help for PC Windows platforms.



3. In the Symbol list, scroll down and select the two-input multiplexer **MUX2X2**.

   The status bar line reads: `Symbol - Click to Place Symbol 'MUX2X2'.`

4. Move the cursor inside the schematic border.

   Notice that the cursor drags the outline of the symbol.

5. Position the cursor in the center of the sheet and place the symbol by clicking once.

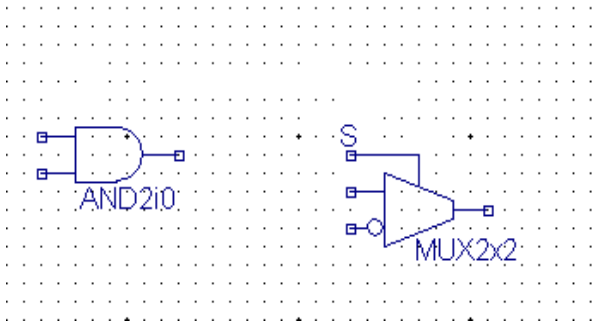
6. In the Library list, select the **AND** library.

7. In the Symbol list, select an **and2i0** macro.

8. Move the cursor inside the schematic border.

   Notice that the cursor drags the outline of the symbol.

9. Position the cursor to place the and2i0 macro as shown in the following arrangement and click once.



1.2.1.1.1 Adding Symbols by Name

As an alternative to using the Symbol Libraries window, you can specify the macro by name:

1. Right-click to cancel and stop dragging the AND gate.
2. Type: **`DFFC`** into the status bar at the bottom of the Schematic Editor window.

   The Schematic Editor is case-sensitive, except when you are adding symbols to your schematic.
3. Press **Enter** on the keyboard.
4. Place the symbol by clicking once into the configuration as shown in the following arrangement.

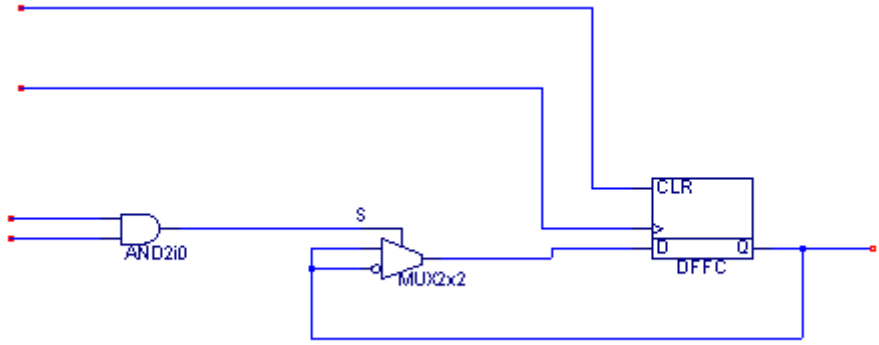
1.2.1.2 Connecting the Symbols

To add wires to connect the symbols:

1. From the Schematic Editor menu bar, select **Add>Wire**.

   The status bar line reads: `Wire - Click or Drag to Begin Wire`.
2. Add wires until your schematic looks like the following arrangement.
   a. Add a wire to the upper and lower inputs of the **AND** gate.
   b. Add a wire to the **Q** output of the flip-flop.
   c. Add a wire to the clock and clear inputs of the flip-flop.
   d. Connect the **AND** gate to the multiplexer.
   e. Create the feedback path from the output of the flip-flop to the inputs of the multiplexer. Click on the multiplexer's non-inverting input pin to start the wire.
   f. Route the wire around the multiplexer and the flip-flop. Attach the end of the wire to a mid-point on the short wire on the output of the flip-flop, then terminate the wire.

g. Finally, create a short wire connecting the inverting input of the multiplexer and the previous feedback path.



NOTE: To delete wires, select **Edit>Delete** and click on the wire to be deleted.

1.2.1.3 Defining the Net Names

To define the net names:

1. From the Schematic Editor menu bar, select **Add>Net Name**.

   The status bar line reads: `Net Name - Enter Net Name =`.

2. Type: **`CLK`**.

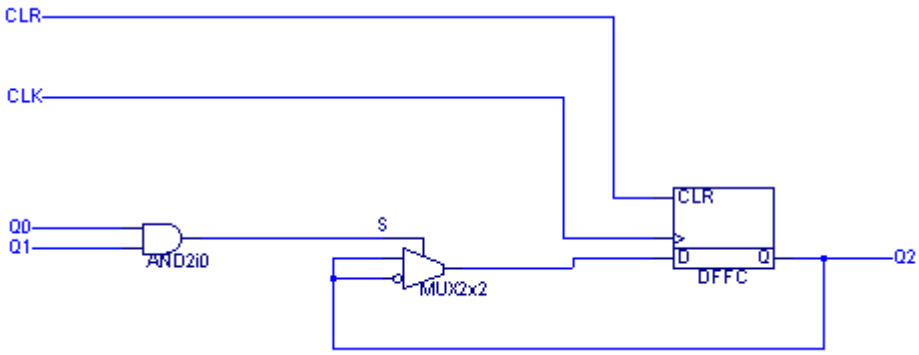
3. Press **Enter** on the keyboard.

   The status bar line reads: `Net Name - Place Net Name Flag 'CLK' - Shift Key to Rename`.

4. Position the crosshairs of the cursor on the end of the clock wire created previously and click.

   This places the CLK flag at the end of the selected wire.

5. Add the net names, **`CLR, Q0, Q1,`** and **`Q2`** as shown in the following arrangement.



1.2.1.4 Defining Ports

The primary inputs and outputs of the schematic must now be marked with I/O markers.

1. From the Schematic Editor menu bar, select **Add>I/O Marker**.

   The status bar line reads: `Select Net Name Flag on End of Wire`. The I/O Markers window appears.

1.2.1.4.1 Adding an Input Marker

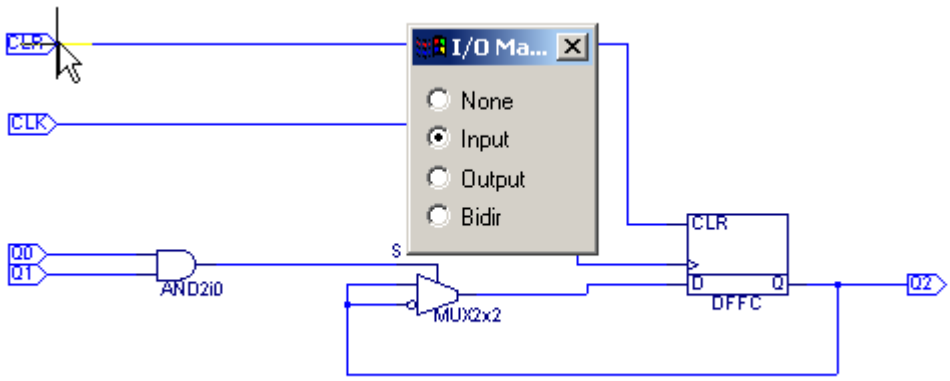
To add an input marker:

1. Click the **Input** option in the I/O Markers window.
2. Position the crosshairs of the cursor at the end of the clock wire and click.

   This places an input marker on the CLK flag.

   NOTE: To create an I/O marker, the net name flag must be placed at the end of its wire (as opposed to along the length of its wire).

3. Repeat this operation for the CLR, Q0,and Q1 flags. All three input markers can be added in one operation by dragging a rectangle around the three net names.



1.2.1.4.2 Adding an Output Marker

To add an output marker:

1. Click the **Output** option in the I/O Markers window.
2. Position the crosshairs of the cursor at the end of the output wire on the Q2 flag, and click to create the output marker.

1.2.1.5 Saving the Schematic

To save the schematic:

1. From the Schematic Editor menu bar, select **File>Save As**.

   A dialog box prompts you for the name of the file.

2. Browse to `C:\pasic\design\TUTORIAL\SCHEM` and type: **`BBIT2`**.
3. Click **Save**.

1.2.1.6 Creating Symbols

1.2.1.6.1 Schematic Symbols

To make a matching symbol for this schematic:

1. From the Schematic Editor menu bar, select **File>Matching Symbol.**

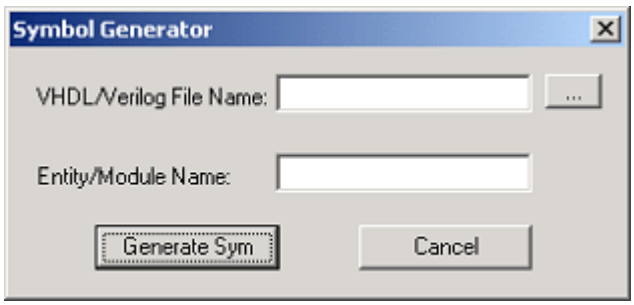
   You now have a symbol for this schematic to also use in other schematics.

1.2.1.6.2 HDL Symbols

Symbols for HDLs can be created automatically with the symbol generator.

1. From the Schematic Editor menu bar, select **Add>Generate Symbol**.

   A Symbol Generator dialog box is displayed.



2. Type or browse to the Verilog/VHDL file for which the symbol needs to be generated.

   For example: browse to `C:\pasic\design\TUTORIAL\VERILOG\DRAMCTRL.V` and click **Open**.

3. Type the Module/Entity Name from the Verilog/VHDL file.

   For this example: `dramctrl.`

4. Click **Generate Sym**.

   A symbol for the given HDL file is created.

   NOTE: To create a symbol for the design, ensure that the complete design is contained within a single file (VHDL).

1.3 Checking Consistency

To check for consistency in the schematic:

1. From the Schematic Editor menu bar, select **DRC>Consistency Check.**

   This runs the schematic checker. The Error Report window should indicate the following: **No errors detected**.

1.4 Completing the Schematic Counter

To complete the schematic counter:

1. From the Schematic Editor menu bar, select **File>Open**.

   The Open window is displayed.

2. Double-click `bcount4.sch` (the default library is `C:\pasic\design\TUTORIAL\SCHEM\bcount4.sch`). This is the 4-bit schematic counter that has been partially completed for you.

   NOTE: If the Error Report window appears, you are still in error-reporting mode. Close this window by clicking the X in the upper right corner.

At this stage the schematic is almost complete. Next you must add **`BBIT2`** by performing the following steps:

1. Select **Add>Symbol.**
2. Type: **`BBIT2`** into the status bar at the bottom of the Schematic Editor window.
3. Press **Enter** on the keyboard.

   The cursor includes the outline of the symbol.

4. Position the symbol on the schematic so the pins coincide with the open nets near the center of the design. Click to place the symbol.

   NOTE: You *do not* have to make a symbol for the top-level schematic.

5. Select **DRC>Consistency Check** (this verifies that the schematic is error-free).

   You should get no errors and the following warning: `No Symbol for This Schematic`. You can ignore the warning.

6. Select **File>Save** to save the file.
7. Select **File>Exit.**

You have now finished entering the design.

1.5 Schematic Design Editor Shortcuts

Table 1-1 on page 11 lists shortcuts for many of the operations described in the sections above. These usually eliminate keystrokes and save time when executing frequently used commands.

Table 1-1: Schematic Editor Shortcuts

Menu	Operation	Shortcut Operation
View	Full Fit	Control-F
Add	Symbol	F2 function key
Add	Wire	F3 function key
Add	Net Name	F4 function key

The toolbar is used for many of the basic functions often used during schematic design entry.

1.6 Launching the Hierarchy Navigator

The Hierarchy Navigator is used to:

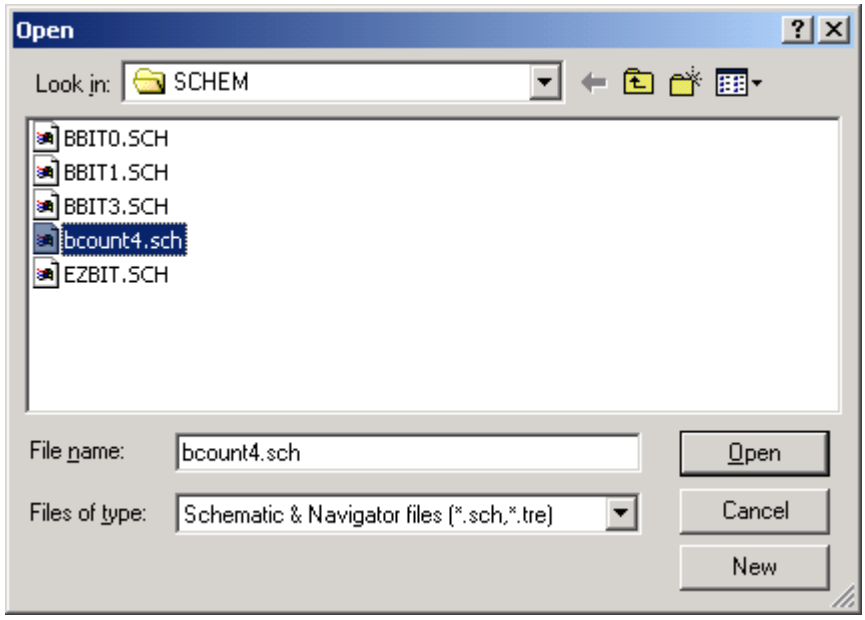
- View the complete design hierarchy
- Create instance attributes
- Create a QuickLogic netlist

The Navigator can be used to edit schematics.

To launch the Navigator:

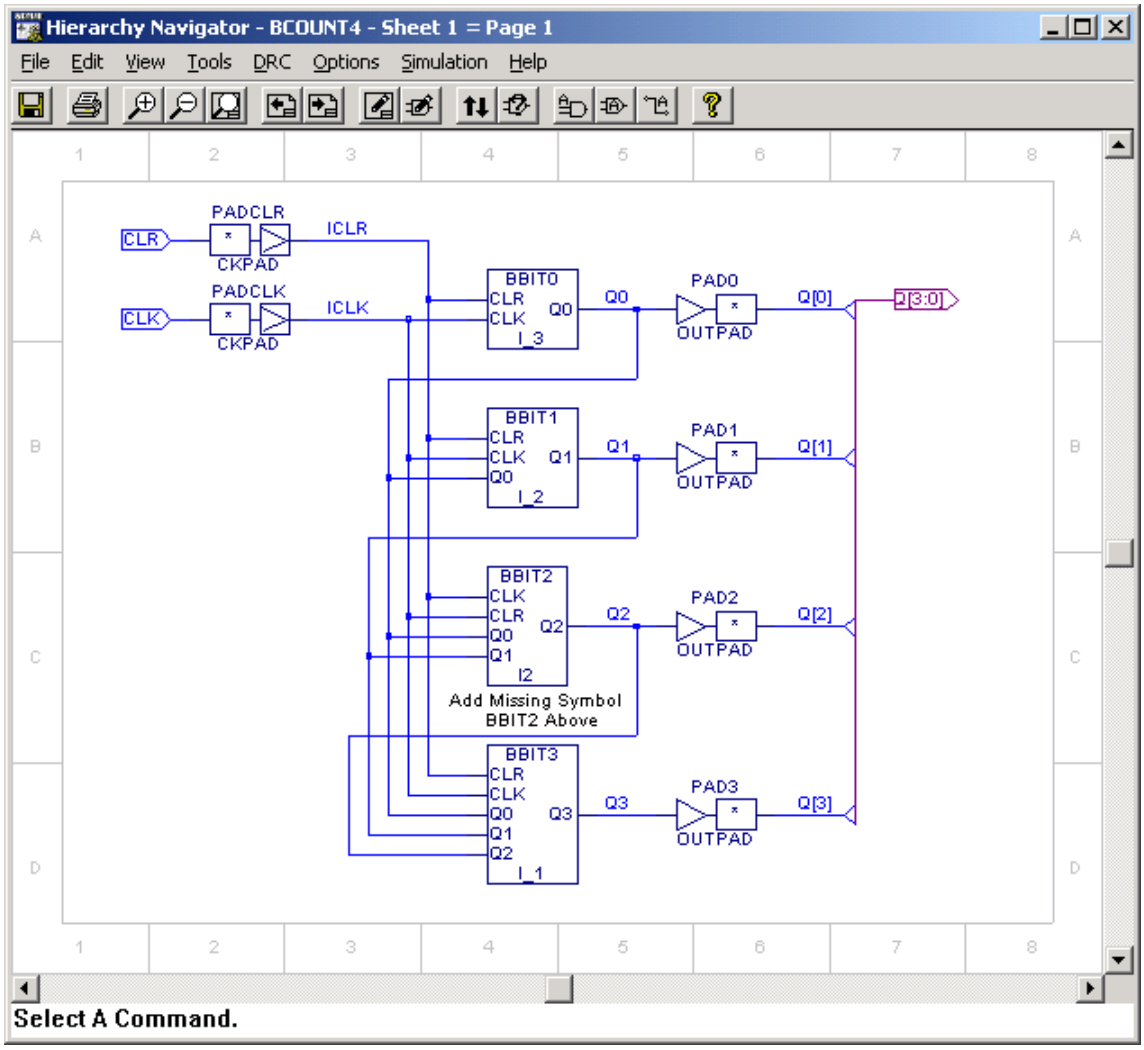
1. From the SpDE menu bar, select **Design>Schematic Editor & Navigator**, or click the  icon.

   The Open window is displayed. Navigator files have the extension `.tre` and schematic files have the extension `.sch`. Currently no `.tre` files appear in the tutorial directory.



2. Select **`bcount4.sch`** and click **Open**.

The Hierarchy Navigator window is displayed. You have now identified this schematic as being at the top level in the design hierarchy.



3. Click the **Maximize** button to enlarge the window to full screen.
4. Select **View>Full Fit**.

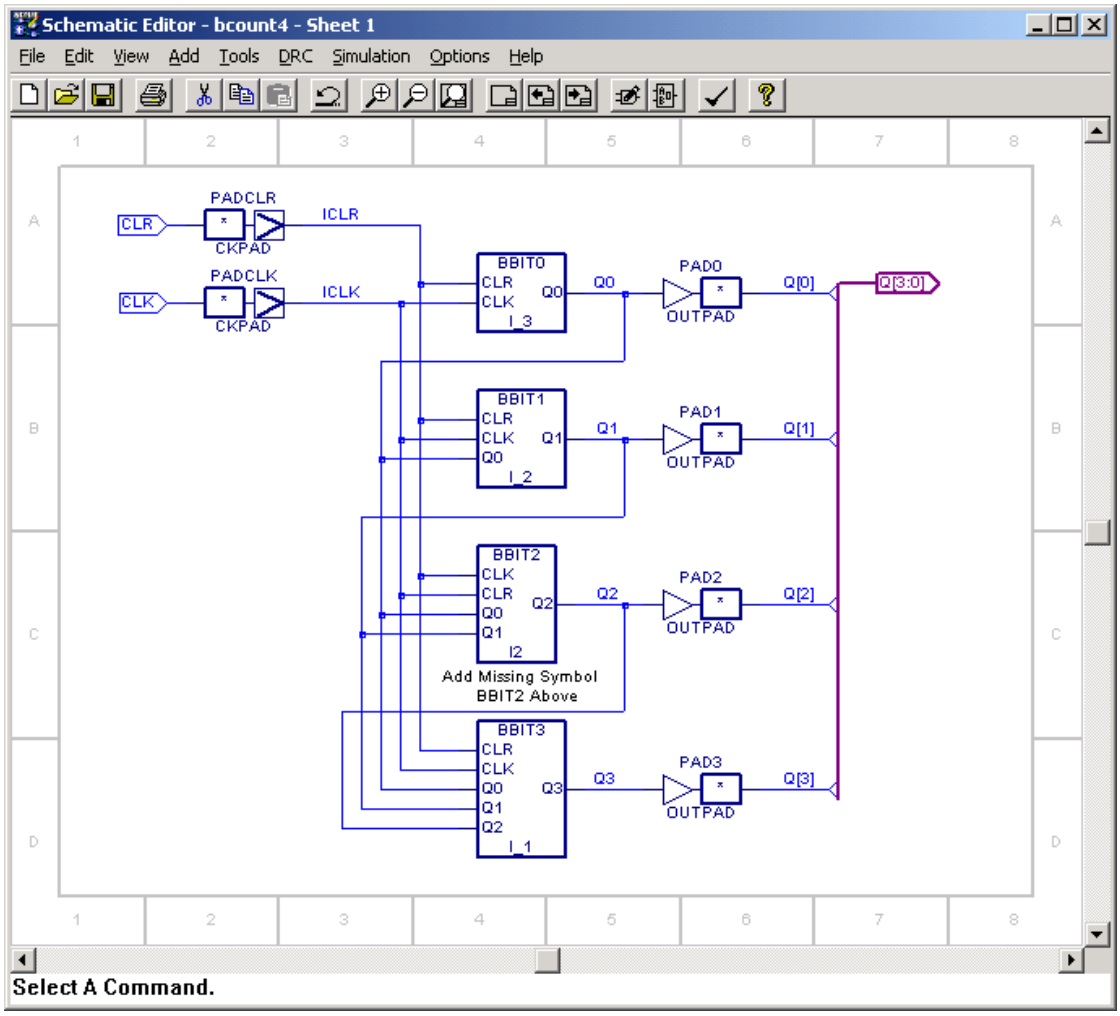
   Click anywhere within the schematic border to perform this operation. The Hierarchy Navigator displays the completed designs.

1.6.1 Editing the Schematic Design

To edit a schematic design in the Hierarchy Navigator:

1. Select **File>Edit Schematic**.

   The Schematic Editor opens displaying the schematic design to be edited.

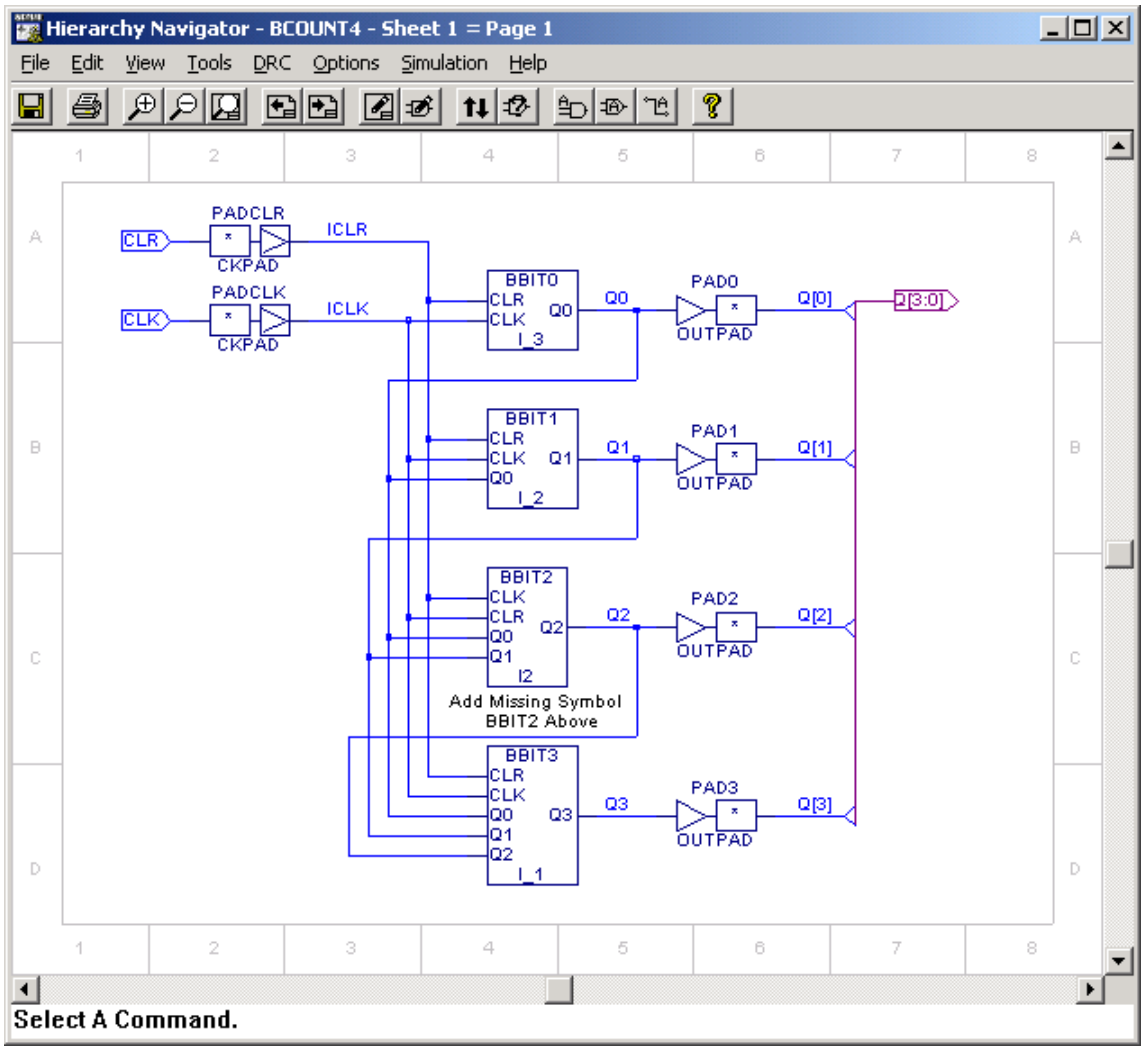


2. After editing the schematic, select **File>Save** and close the Schematic Editor.

   It will automatically load the schematic design in the Hierarchy Navigator.

1.6.2 Using the Push/Pop Mode to Browse the Design

The Hierarchy Navigator looks much like the Schematic Editor, except that it maintains the full context of the hierarchy.



To browse the design:

1. From the Hierarchy Navigator menu bar, select **View>Push/Pop** or click the **Push/Pop** button on the tool bar.

   The profile of the cursor changes to a cross. The status bar line reads: `Push/Pop=`.

2. Position the cursor over the symbol BBIT2 (the one you created earlier).

3. Click to "push" the symbol into a lower level of the hierarchy.

   Use the Zoom In or Zoom Out commands from the View menu or toolbar to get a better view of your design. When finished, right-click to cancel out of the mode.

4. To return to the top-level schematic, or "pop" back to the top, click on the white space in the schematic.

1.6.3 Performing a Query

The Hierarchy Navigator provides detailed information on instances, pins, and nets within the design hierarchy.

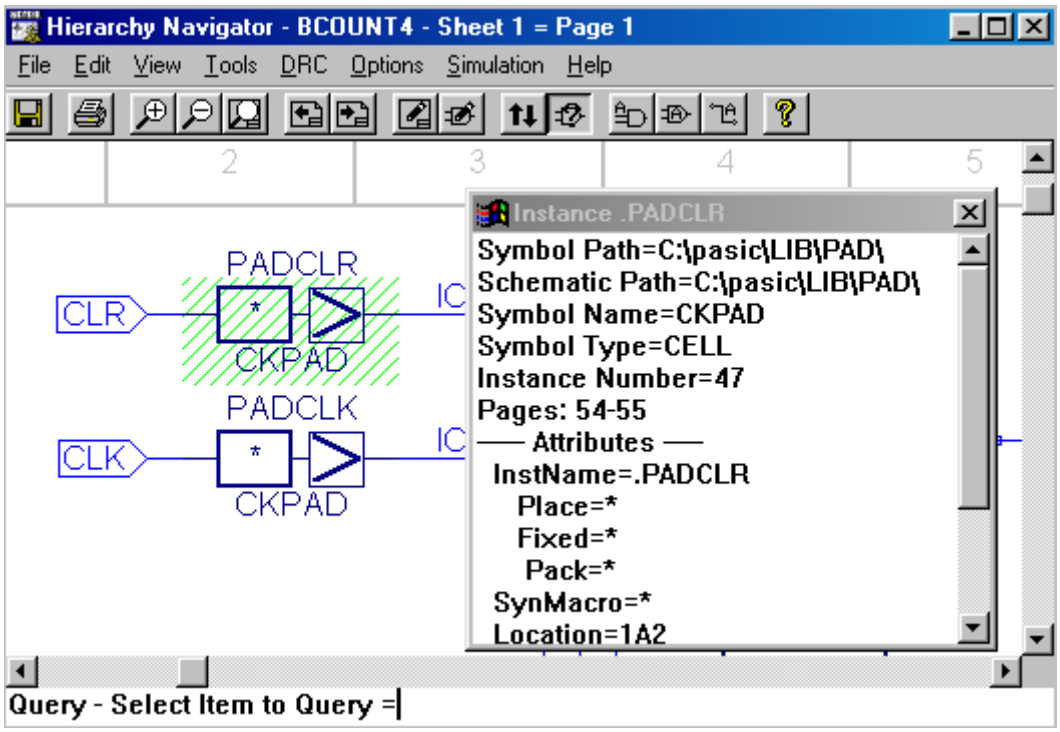
To perform a query:

1. From the Hierarchy Navigator menu bar, select **DRC>Query**.

   The status bar line reads: `Query - Select Item to Query =`.

2. Position the cursor on one of the CKPADs and click.

   The selected instance becomes highlighted. The Symbol Instance window displays information about the CKPAD including its instance name and the ports on the instance.



1.6.4 Using the Mark Command to Trace Nets

To use the `Mark` command for tracing nets in the design:

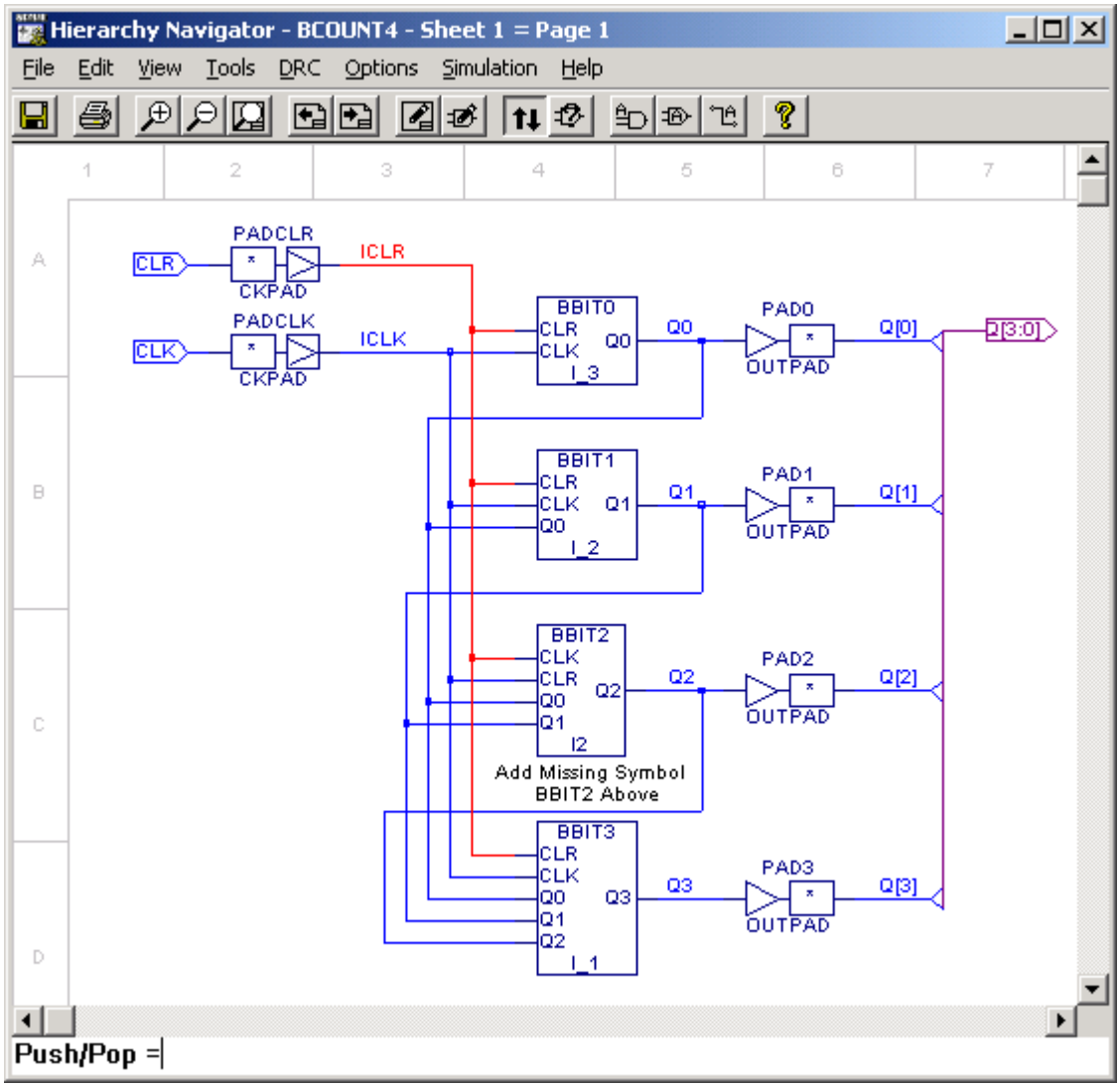
1. From the Hierarchy Navigator menu bar, select **DRC>Mark**.

   The status bar line reads: `Mark - Select Net or Instance to Mark =`.

2. Position the cursor on the net ICLR coming out of the upper CKPAD.

3. Click to mark this net.

   The net is now highlighted in red.



1.6.5 Using the Push/Pop Mode to Trace Marked Nets

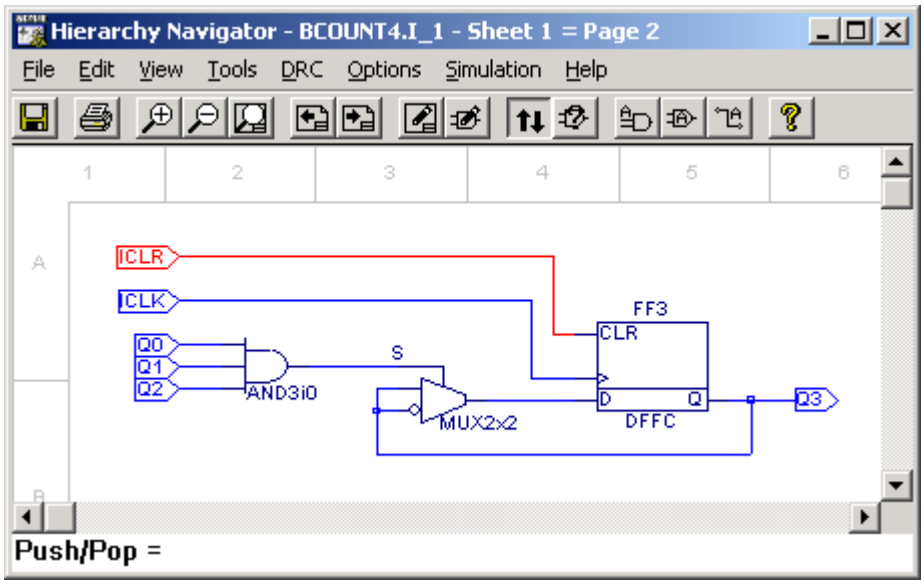
To trace marked nets:

1. From the Hierarchy Navigator menu bar, select **View>Push/Pop**.

   The status bar line reads: `Push/Pop=`.

2. Click on the symbol: `BBIT3`.

   The Navigator displays the schematic for BBIT3, highlighting the ICLR signal. This technique allows you to easily trace marked nets up and down the hierarchy.



3. To pop back up one level, click on an empty part of the schematic.
4. Right-click once to cancel out of Push/Pop mode and re-enter Mark mode.
5. Unmark the ICLR signal by clicking on it once.

1.6.6 Hierarchy Navigator Shortcuts

Table 1-2 lists shortcuts for many of the operations described in the sections above.

Table 1-2: Shortcuts for the Hierarchy Navigator

Menu	Operation	Shortcut Operation
View	Full Fit	Control-F
View	Push/Pop	F2 function key
DRC	Query	Control-Q
DRC	Mark	F3 function key

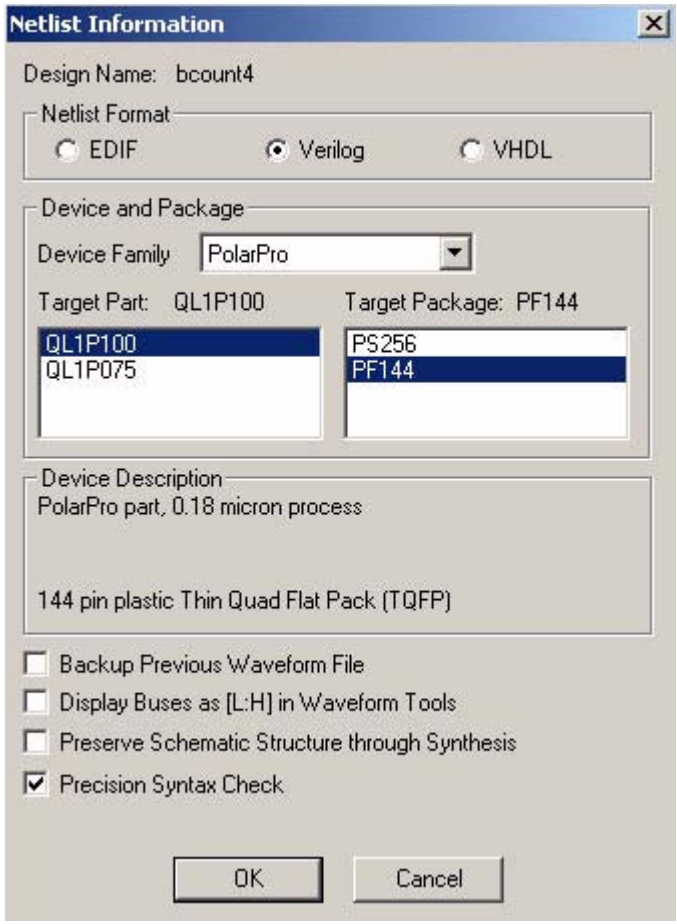
You may also use the toolbar for many of these basic functions.

1.7 Exporting the Verilog Functional Simulation Netlist

The design will now be simulated to verify functionality. In order to run a pre-layout simulation (i.e., before place and route simulation), a Verilog or VHDL netlist must be generated. This netlist can be used with the Aldec Active-HDL Simulator included with QuickWorks.

1. From the Hierarchy Navigator menu bar, select **Tools>Export QuickLogic**.

   The Netlist Information dialog box opens.



2. Select **Verilog** in the Netlist Format.
3. From the Device Family pull-down menu, select **PolarPro**.
4. From the Target Part list, select **QL1P100**.
5. From the Target Package list, select **PF144** or **PS256**.

   The Device Description reads:

   ```
   PolarPro part, 0.18 micron process
   144 pin plastic Thin Quad Flat Pack (TQFP) or
   256 pin Ball Grid Array (CTBGA)
   ```

6. Click **OK**.

   The Pre-layout Information window is displayed.

7. Click **Done**.
8. From the Hierarchy Navigator menu bar, select **File>Save**.

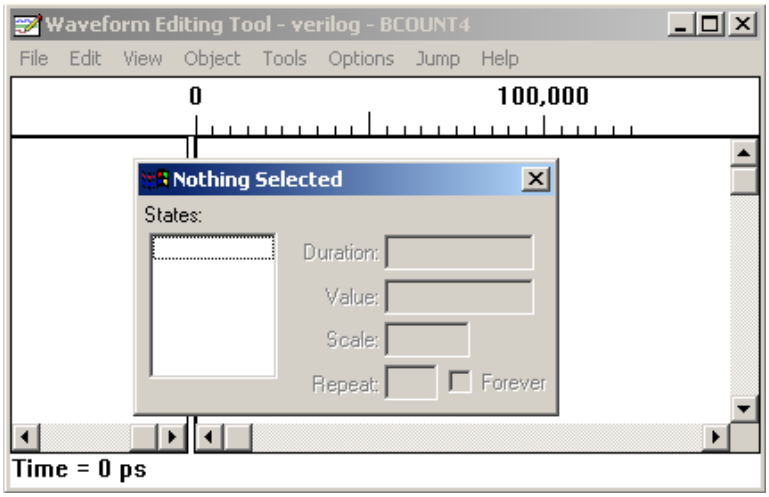
   This saves the part and package configurations you have just specified. Keep the Hierarchy Navigator window open (you may want to minimize the window) because you will be using it in the next section of the tutorial. You now have a Verilog functional simulation netlist for your top-level design.

1.8 Creating the Simulation Stimuli

The Waveform Editor is an interactive graphical environment used to enter stimulus for the simulator. You may also create a test fixture (set of input vectors) by hand, although this method is suggested for experienced Verilog users only.

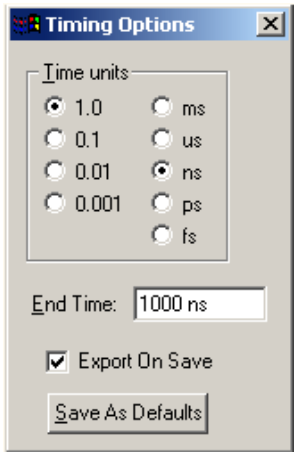
1. From the Hierarchy Navigator menu bar, select **Simulation>Waveform Editor**.

   The Waveform Editing Tool window is displayed, with the Nothing Selected dialog box inside it.



2. From the Waveform Editor menu bar, select **Options>Timing Options**.

The Setup Options dialog box is displayed. In this window you will select basic parameters for the Waveform Editor.



3. Select the Time units as **1.0 ns**.

   This is the smallest time unit for the Waveform Editor.

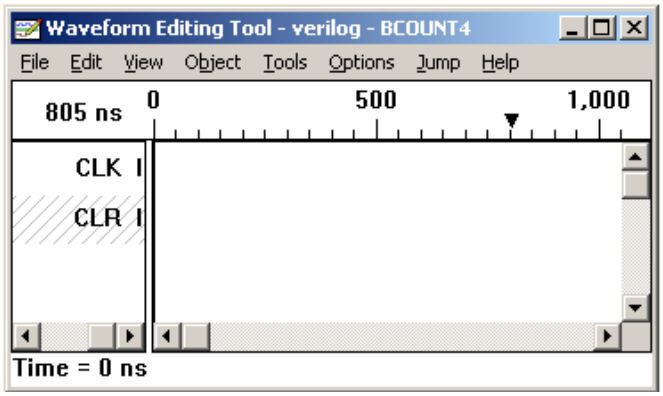
4. Type a Simulation Time of **1000 ns**.

   This is the maximum time for the input waveforms (it can be changed at any time).

   NOTE: Notice that the **Export on Save** check box is checked. This setting means that simulation patterns will be automatically exported as a Verilog test fixture for the simulator when the waveforms are saved.

5. Click the **Save as Defaults** button.
6. Close the dialog box.
7. From the Waveform Editor, select **View>Full Fit**.

   The Waveform Editor displays the input signals to your design.



8. From the Waveform Editor, select **View>Zoom In**.
9. Move the cursor over the window until it turns into a Z (letting you know you are in Zoom mode).
10. Click until you can see the `100` marker in the time scale.

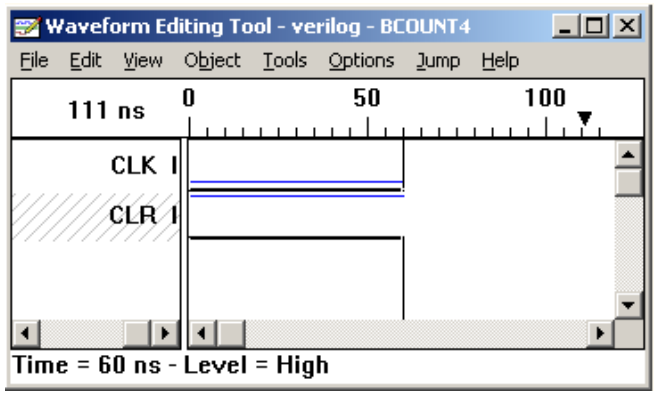
You may need to use the horizontal scroll bar at the bottom of the window.

11. Right-click to exit Zoom mode.
12. If the CLR signal is not already highlighted, position the cursor over the signal name on the left side of the Waveform Editor window and click.
13. Position the cursor at the `60 ns` mark.

    The cursor time is reflected in the upper-left corner of the window.
14. Click to insert an edge.

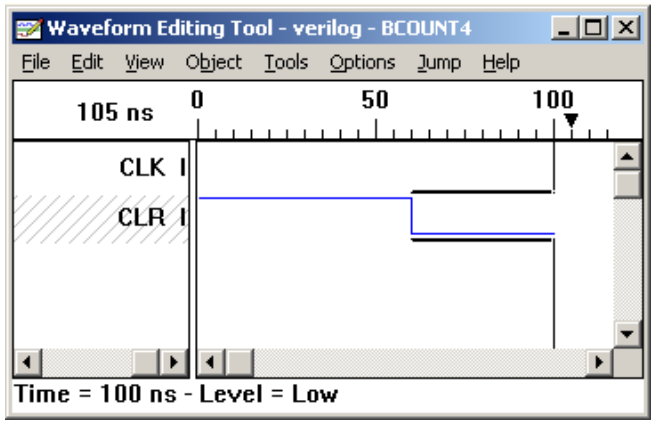
    This creates a high pulse between `0 ns` and `60 ns`.

    NOTE: If you didn't click exactly on the `60 ns` mark, you can make the correction by using the edit window titled Selected Bit Pulse. If this editing window is not available, use the menu command **Object>Edit Mode**. In this window, you can change the value and/or the duration of the current selected pulse. To change the duration of a pulse, type in a new value.



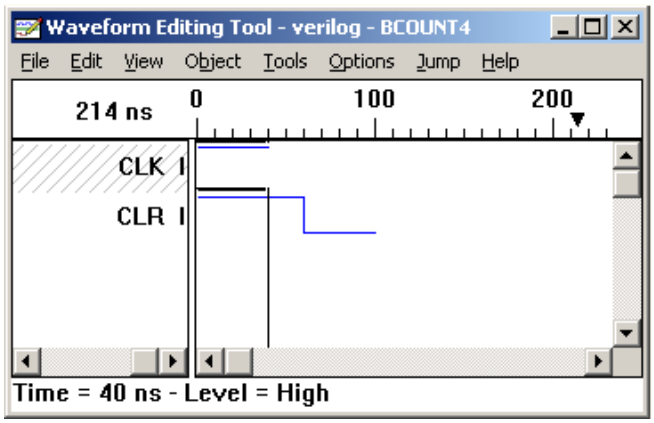
15. Position the cursor at the `100 ns` mark within the CLR waveform, then click once to insert another edge.

    This completes the CLR signal.



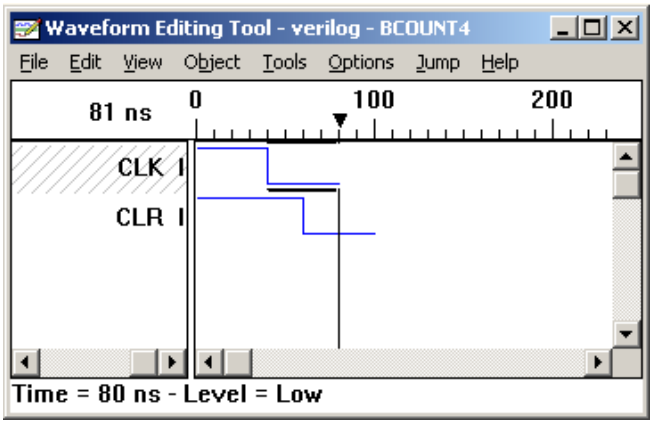
16. Position the cursor over the CLK signal name on the left side of the window and click to highlight.

17. Position the cursor at the `40 ns` mark and click to insert an edge.



18. Position the cursor at the `80 ns` mark and click to insert the second edge.

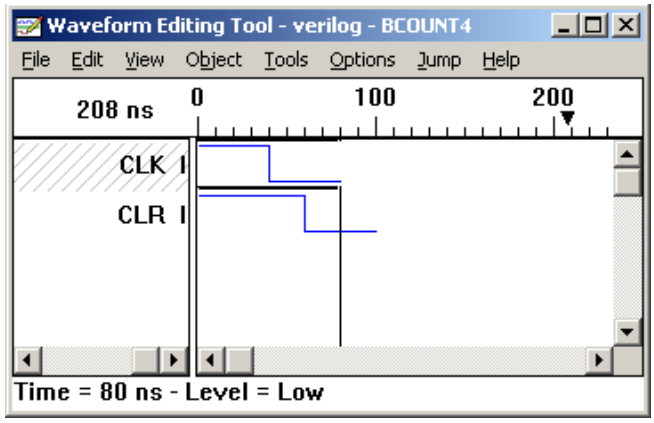
Remember that you can always change the duration of any pulse by using the Select Bit Pulse window.



To continue adding more edges to the CLK signal, the clock can be repeated by identifying the edges entered above and repeating them.

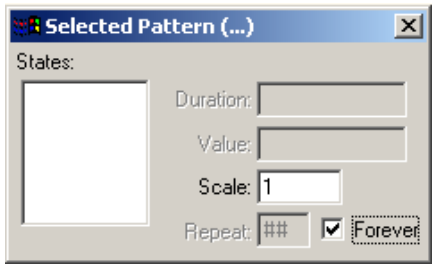
19. Position the cursor directly on the highlighted portion of the CLK waveform (between `40` and `80 ns`), and click.

The entire CLK waveform should be highlighted.

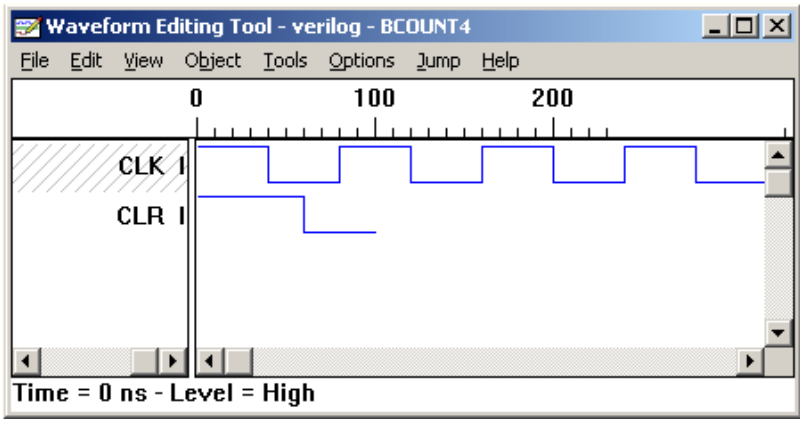


20. The title in the Edit dialog box should read: Selected Entire Pattern CLK.

NOTE: If you have previously closed this dialog box, from the Waveform Editor, select **Object>Edit Mode**. Repeat the mouse clicks on the CLK waveform.



21. Select the **Forever** check box to indicate that you want the CLK pattern to be repeated forever. The Waveform Editor now displays the completed stimulus.



22. From the Waveform Editor, select **File>Save** to save the stimulus.

1.9 Checking Consistency in the Waveform Editor

Before exiting the Waveform Editor, you should run a quick consistency check:

1. In the Waveform Editor, select **File>Consistency Check**.

   This command reports any problems, such as an inconsistency between the signal names in the Waveform Editor and the names in your design. In this tutorial, you will see two error messages: `No Pattern Defined for Global VCC in Schematic` and `No Pattern Defined for Global GND in Schematic`. Since it is not mandatory to define stimulus for VCC and GND, these messages can be ignored.

2. Select **File>Exit** to exit the Waveform Editor.

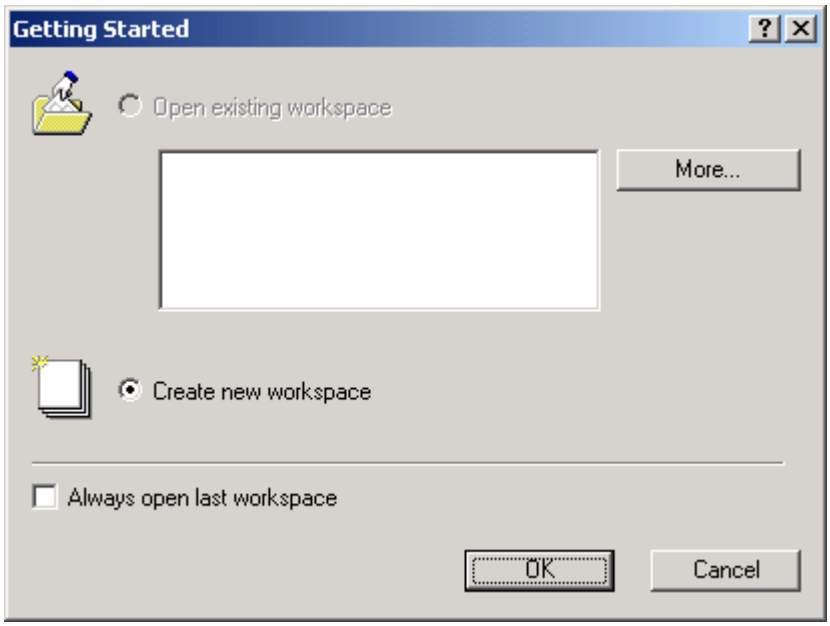
1.10 Simulating the Design for Functionality Using Active-HDL

1.10.1 Creating a Workspace

To perform a pre-layout functional simulation you must first create a workspace in Active-HDL:

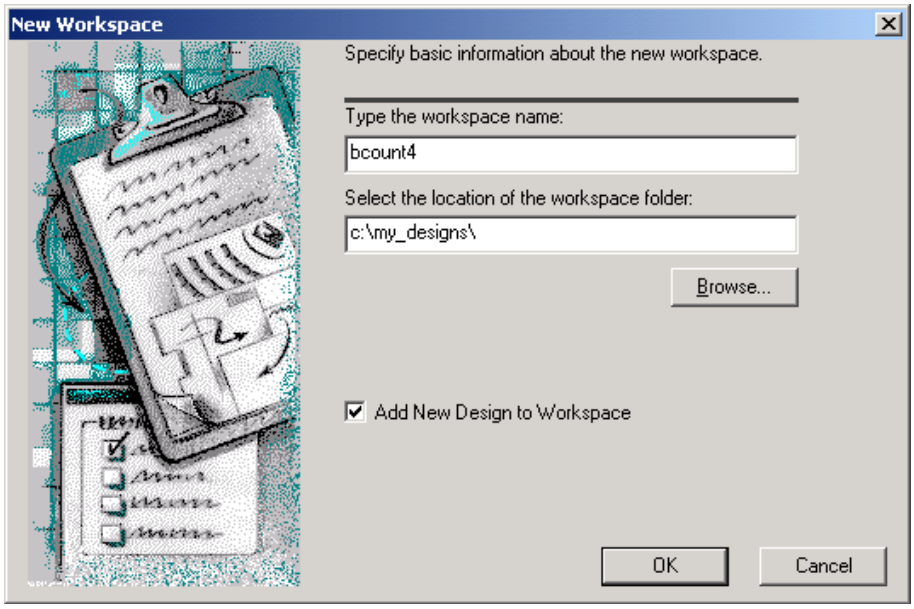
1. From the Hierarchy Navigator menu bar, select **Simulation>Run Simulation**.

   The Active-HDL simulation program begins and the Getting Started screen is displayed.



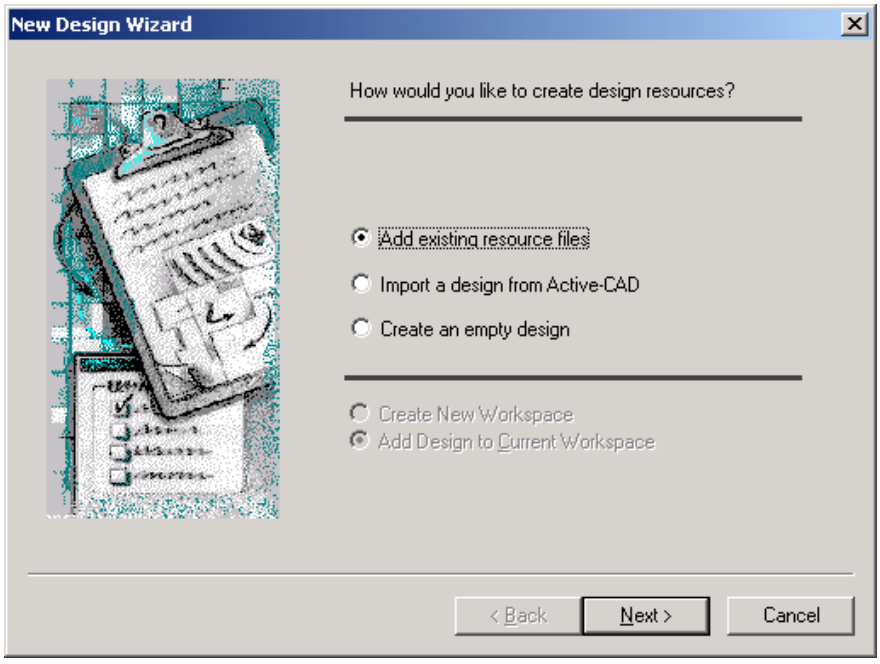
2. Select the **Create new workspace** radio button.
3. Click **OK**.

The New Workspace screen is displayed.



4. Type the workspace name.
5. Click **OK**.

   The New Design Wizard is displayed.

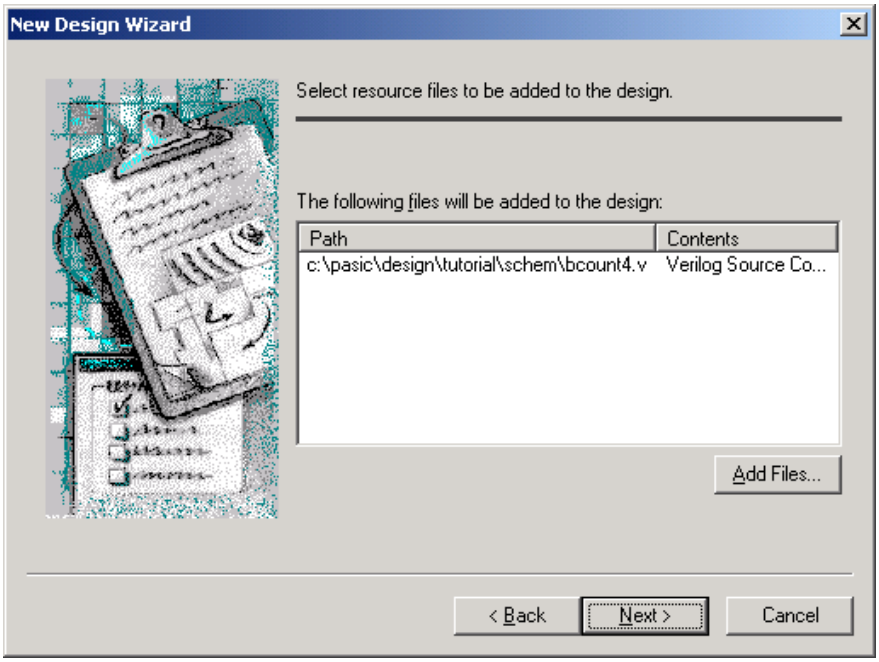


1.10.2 Creating a New Design

To create a new design using the New Design Wizard from the previous step:

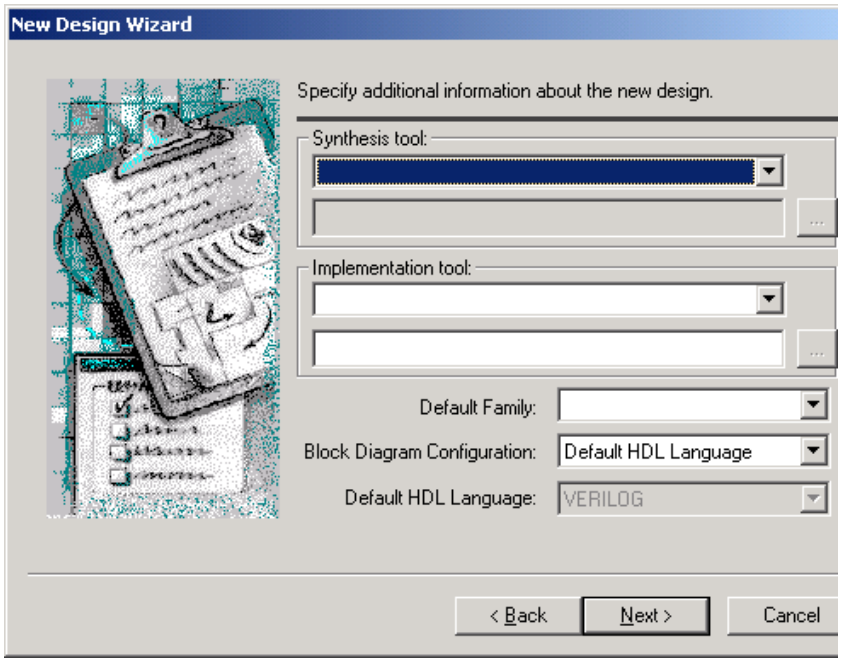
1. Select the **Add existing resource files** radio button.
2. Click **Next**.

   The New Design Wizard screen is displayed prompting you to add files to the design.



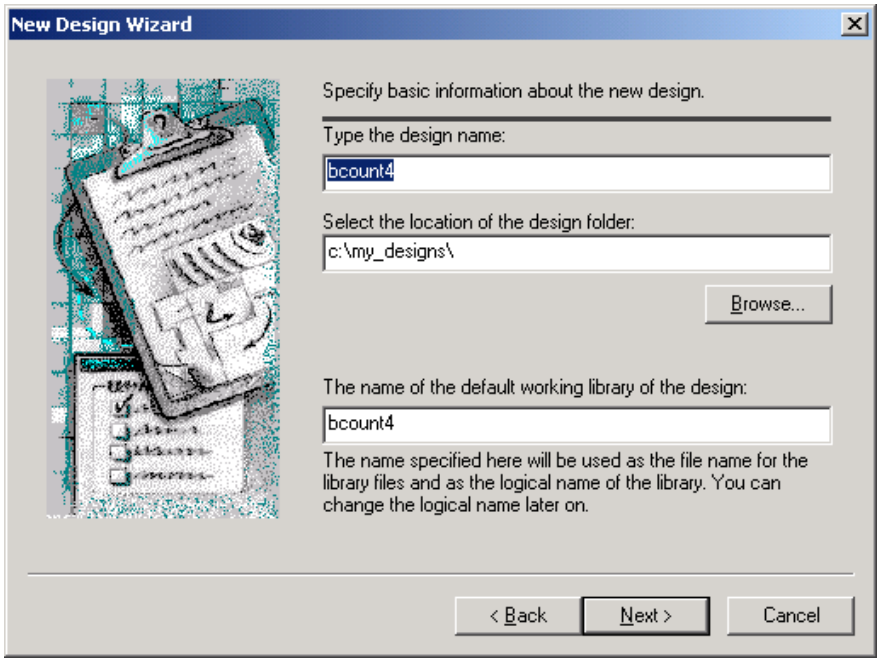
3. Click **Add Files** to browse and add the design files.
4. Click **Next**.

The following screen is displayed.



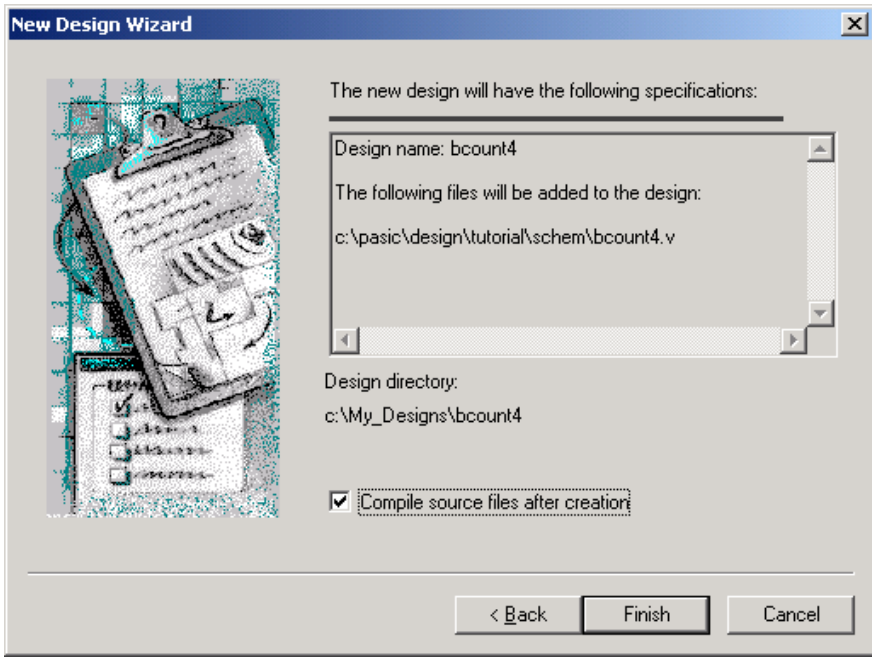
5. Select the **Default HDL Language** option.
6. Click **Next**.

   The New Design Wizard screen is displayed.



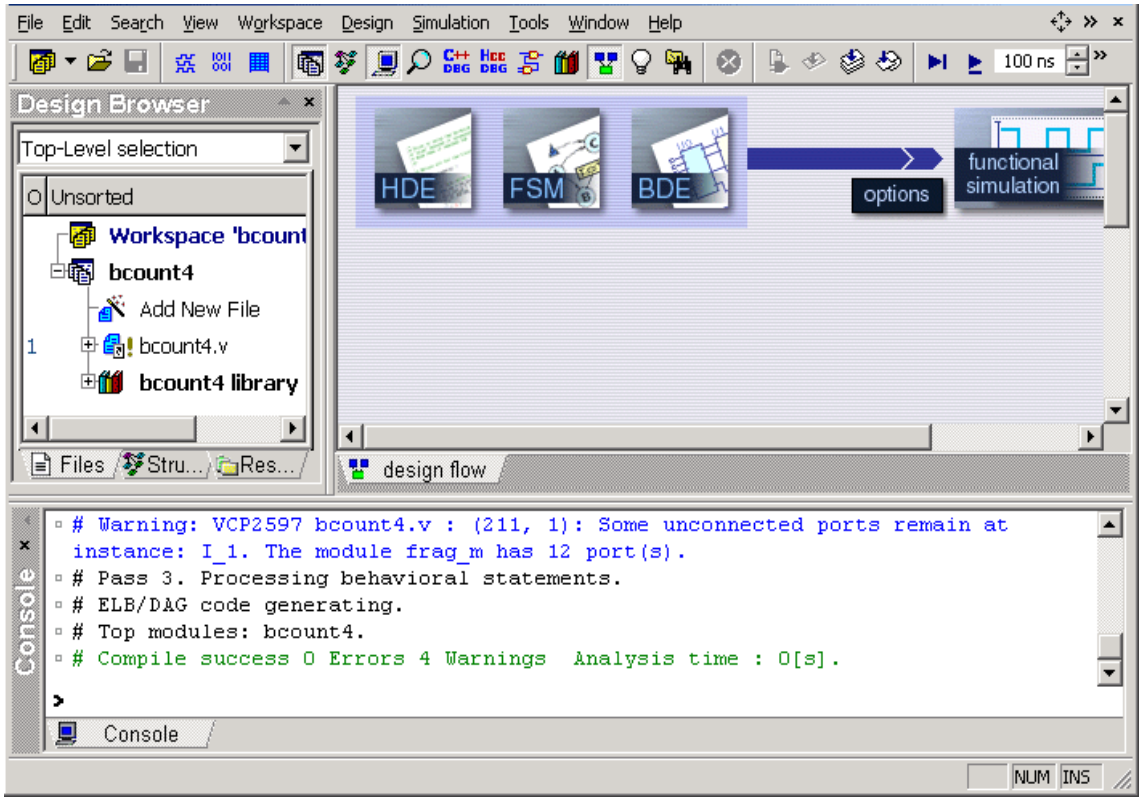
7. Type the design name.
8. Click **Next**.

The New Design Wizard screen is displayed.



9. Click **Finish**.

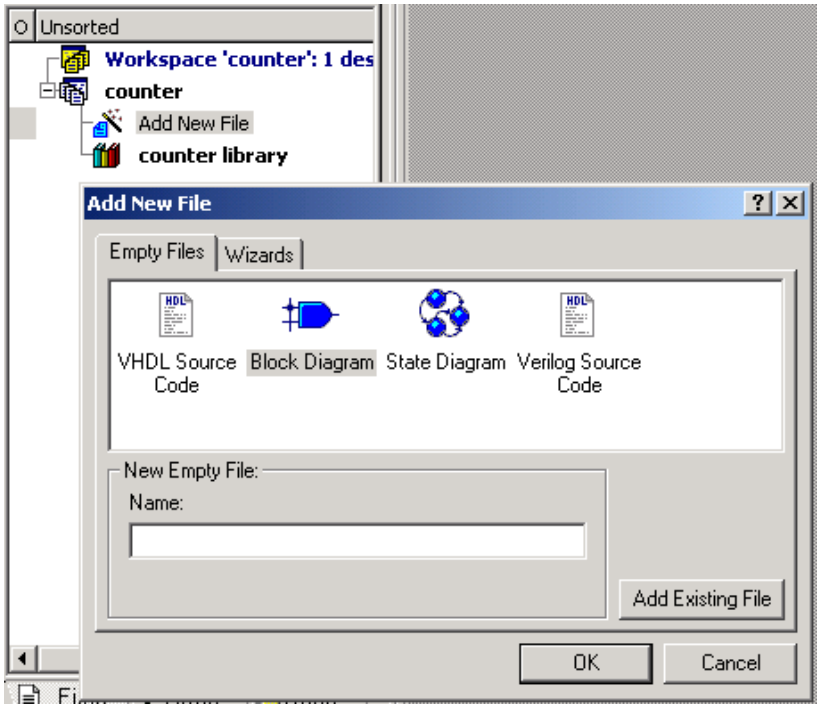
The Active-HDL screen is displayed.



1.10.2.1 Adding a New File

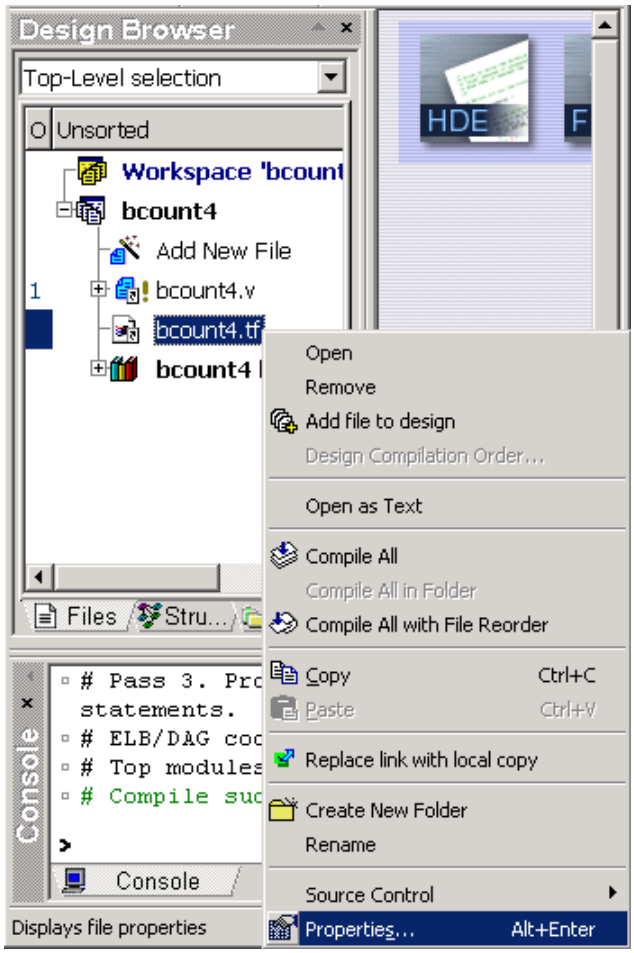
To add new files that where not added during the New Design Wizard process:

1. Double-click on **Add New File** and the following dialog box opens.

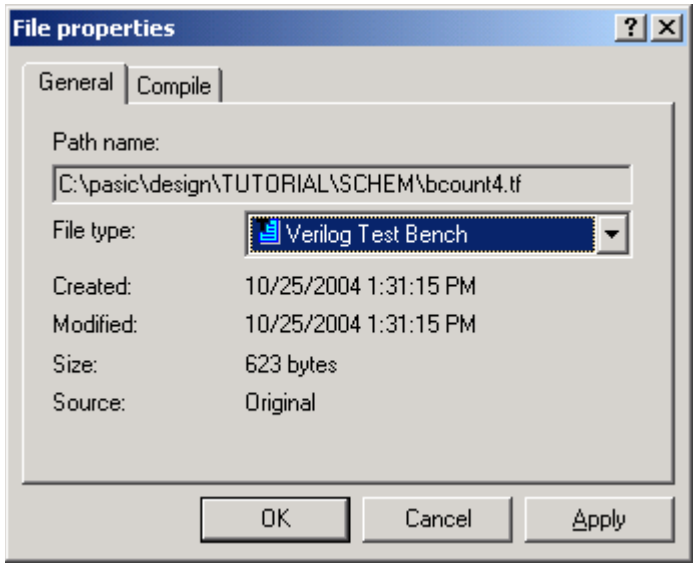


2. Click on **Add Existing File**.
3. Navigate to `C:\pasic\design\TUTORIAL\SCHEM\`, select **bcount4.tf**, and click **Add**.

4. Right-click on **bcount4.tf** and select **Properties**.



The File properties screen is displayed.

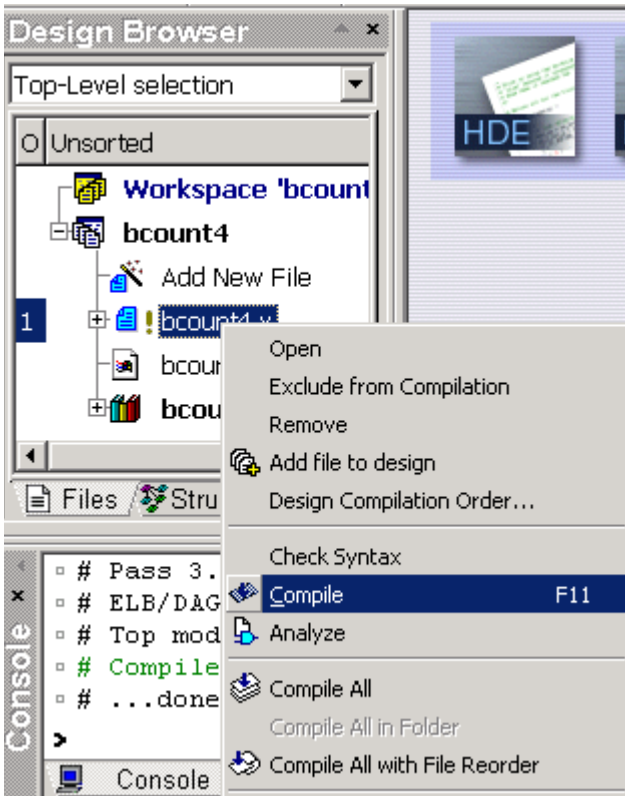


5. Scroll down to select **Verilog Test Bench** from the **File type** pull-down menu.
6. Click **OK**.

1.10.2.2 Compiling the Files

To compile the files:

1. Right-click on **bcount4.v** and select **Compile**.
2. Right-click on **bcount4.tf** and select **Compile**.

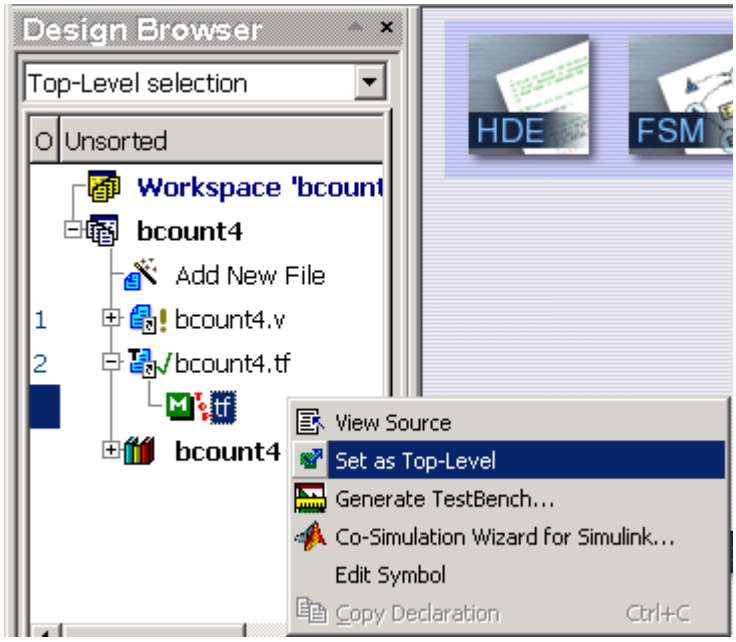


1.10.3 Setting a Design as a Top Level Design

To set `.tf` testbench module as the top level design:

1. Click on the plus sign (+) to expand `bcount4.tf`.

2. To set the design as top level right-click on `tf` and select **Set as Top-Level**.



1.10.4 Initializing the Pre-Layout Simulation

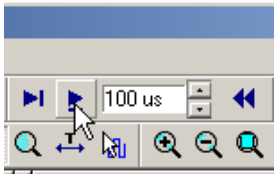
To initialize the simulation in the Waveform Editor screen:

1. From the Active-HDL menu bar, select **Simulation>Initialize Stimulation**.

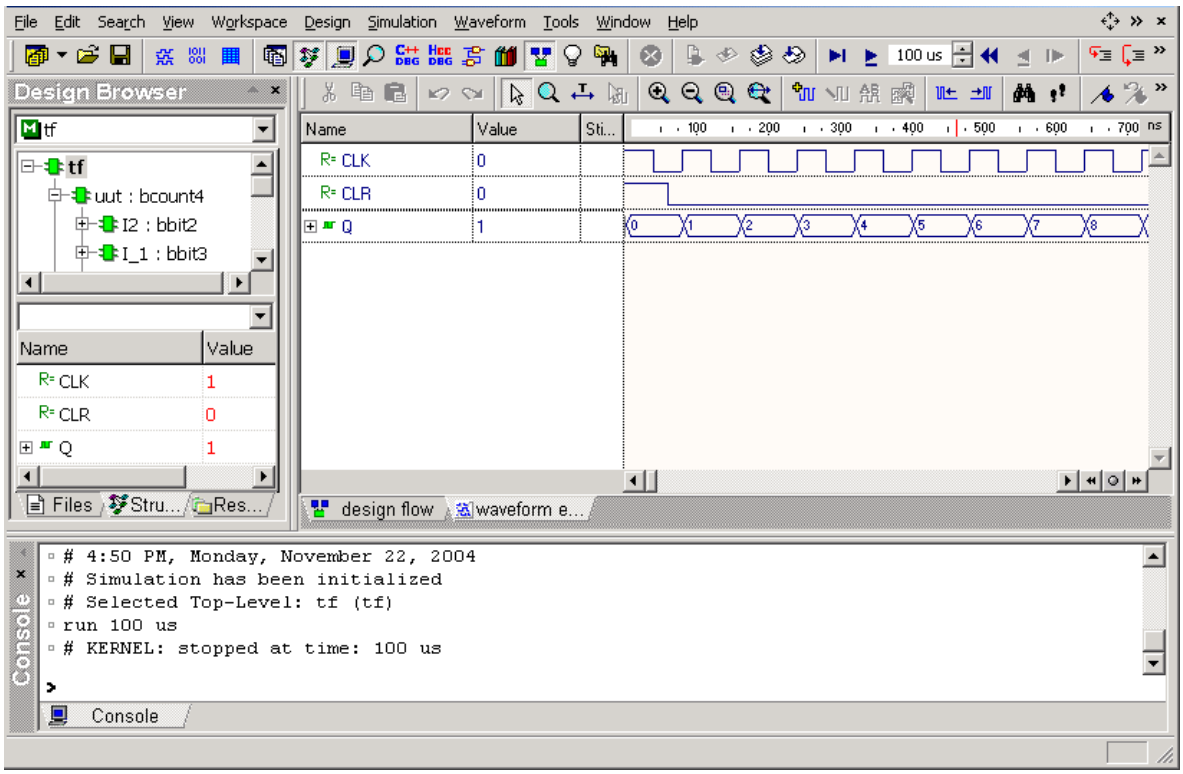
1.10.5 Running the Pre-Layout Simulation

To start running the pre-layout simulation:

1. From the Active-HDL toolbar, click on the waveform icon.
2. Drag the signal names from the left panel to the right panel.
3. Expand the screen, in the menu bar type in **`100 us`** and then click the **Run** arrow to the left.



The output of the waveform counters is displayed.



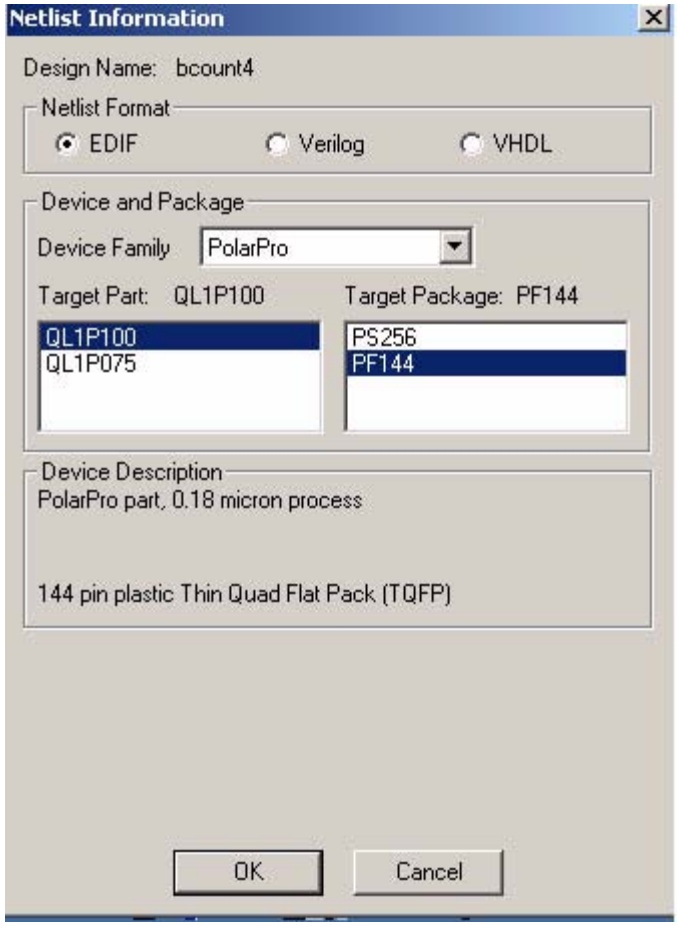
4. After completing the simulation, exit Active-HDL.

1.11 Creating an EDIF Netlist

After you have verified the functionality of the design, place and route the design into a device.

1. From the Hierarchy Navigator menu bar, select **Tools>Export QuickLogic**.

   The Export QuickLogic dialog box is displayed with some saved default settings.



2. In the Netlist Format list, select **EDIF** format to place and route schematic design.

   Earlier in this tutorial you created a Verilog netlist from this window for functional simulation, so Verilog is the current saved default. Now you are creating a QDIF file in order to place and route the design.

3. In the Target Part list, select **QL1P100**.

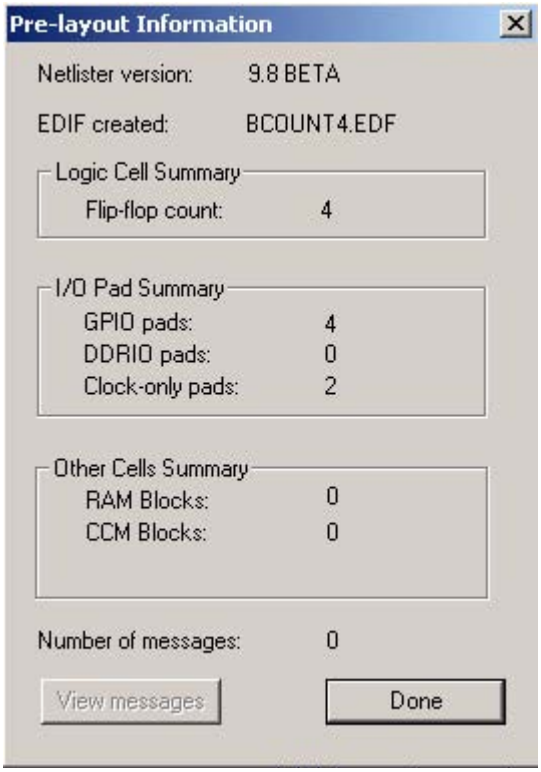
4. In the Target Package list, select **PS256** or **PF144**.

   The Device Description reads:

   ```
   PolarPro part, 0.18 micron process
   144 pin plastic Thin Quad Flat Pack (TQFP) or
   256 pin Ball Grid Array (CTBGA)
   ```

5. Click **OK**.

The Pre-Layout Information is displayed.



6. Click **Done**.

   You now have an EDIF netlist for your design.

7. From the Hierarchy Navigator menu bar, select **File>Save**.

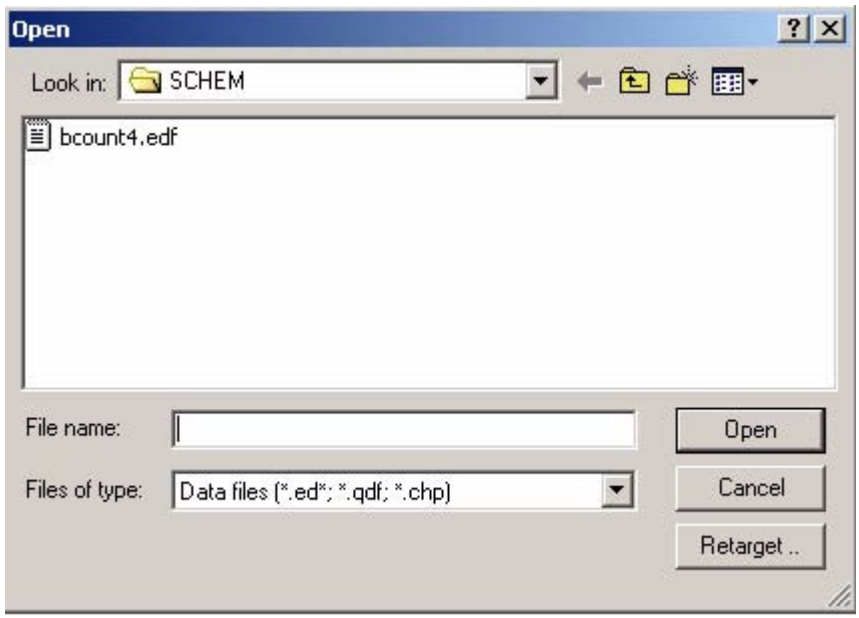
   This creates the hierarchy tree file `BCOUNT4.TRE`. This file contains the part and package selections made above. Minimize the Hierarchy Navigator, but keep it open, because you will be using it later in the tutorial. The SpDE window should now be visible.

1.12 Placing and Routing the Design

In the SpDE window, the workspace area below the toolbar provides a Physical View of the PolarPro. After running the functional simulation you created a `.edf` netlist for your design. In the following procedure, you will load this `.edf` file into SpDE.

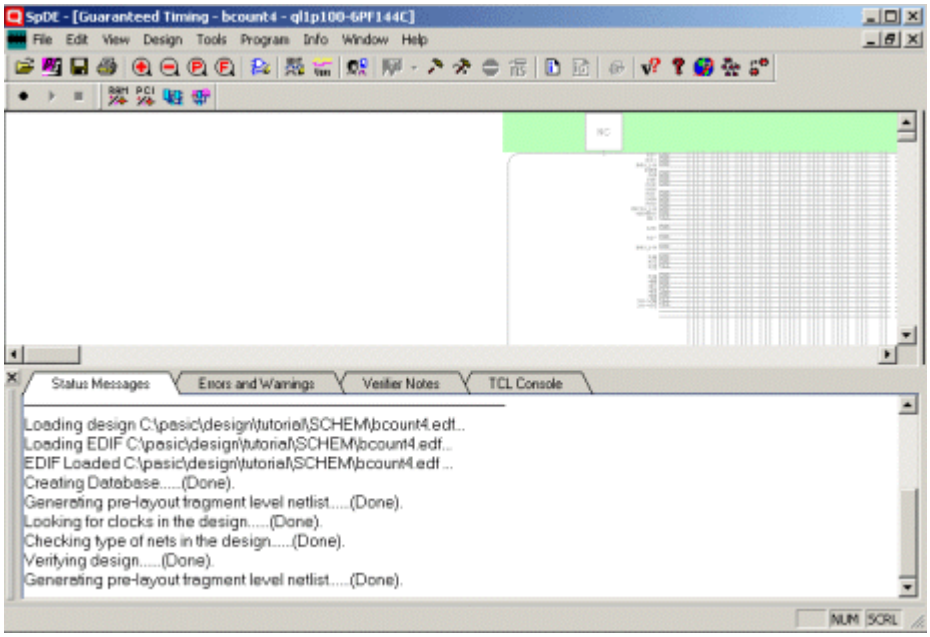
1. From the SpDE menu bar, select **File>Open**.

   The Open window is displayed.



2. Select **bcount4.edf** and click **Open.**

   The design is automatically imported into SpDE. The workspace displays the I/O pads of the QL1P100 device, and a blank inside of the chip.

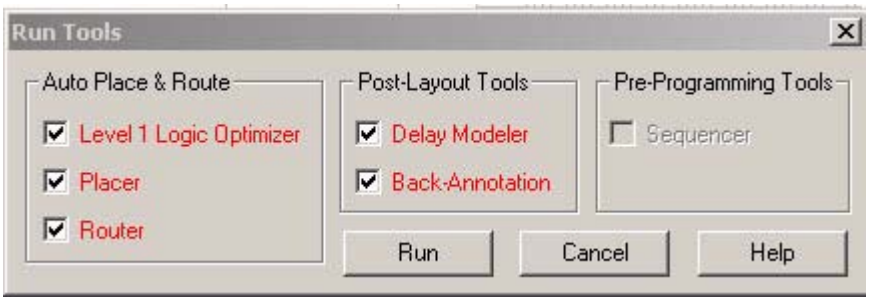


1.12.1 Running the Automatic Tools

The automatic tools will require anywhere from 30 seconds to a few minutes (depending on your hardware configuration) to optimize, place, route, sequence, and delay model this small design.

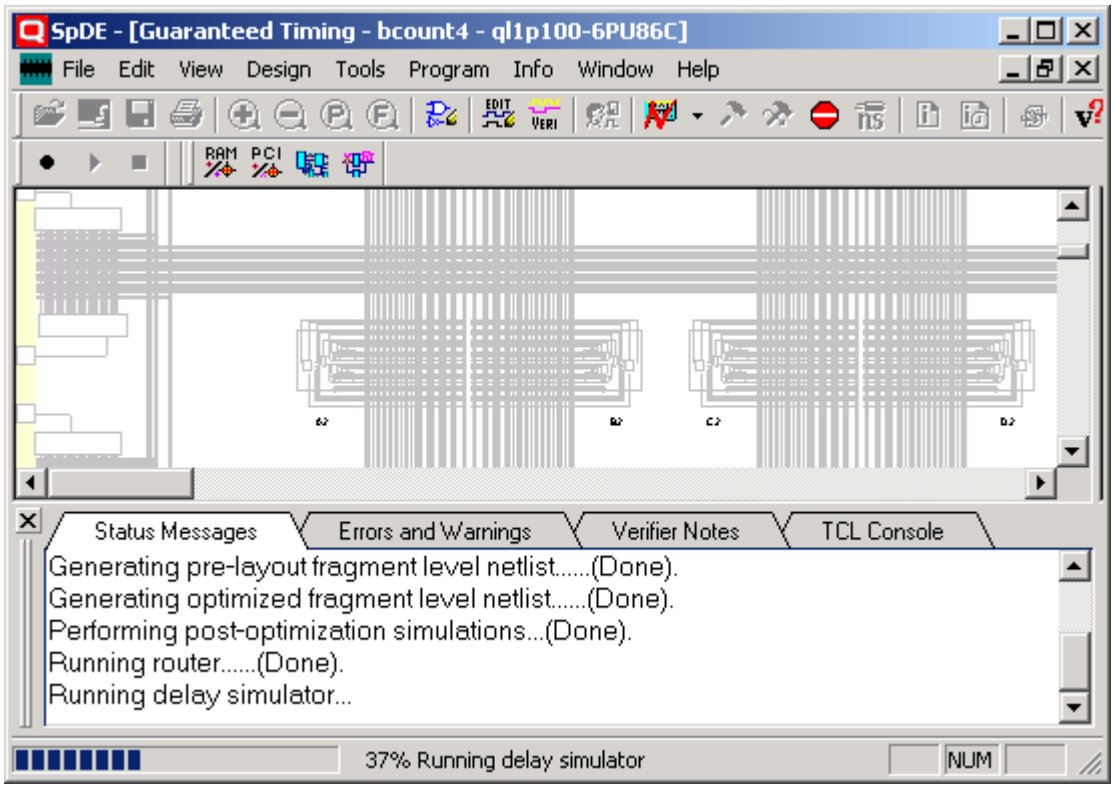
1. From the SpDE menu bar, select **Tools>Run Selected Tools,** or click the  icon.

   The Run Tools window is displayed.

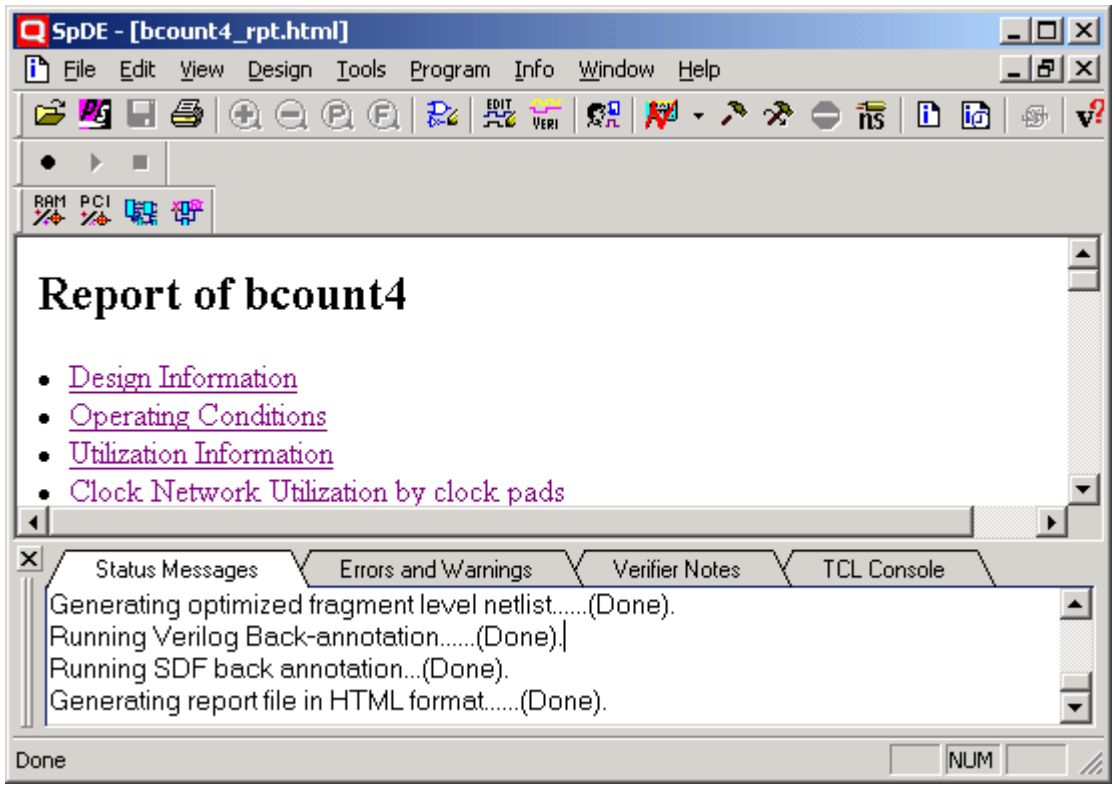


2. Ensure that all the tool check boxes are selected.
3. Click **Run**.

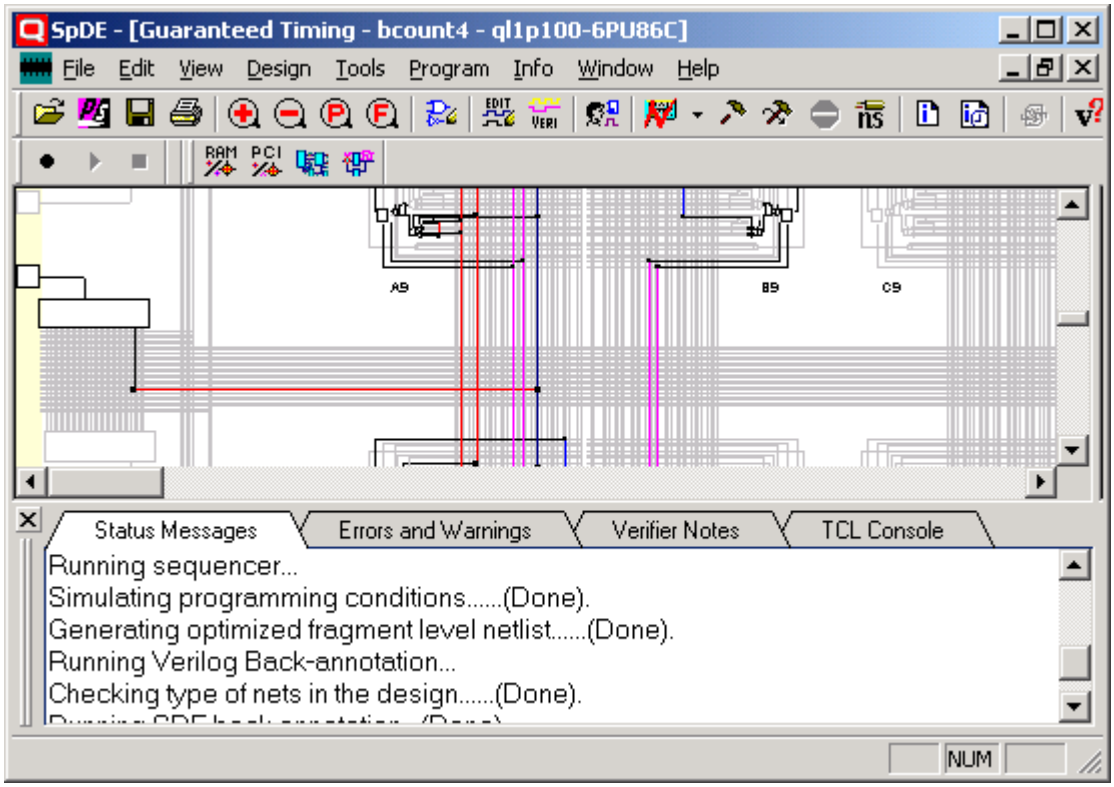
   Each tool runs in sequence. This may go too fast for you to see in this small design. You can view the status of the tools run in the transcript window.



After running tools, the report file is displayed.



Initially, the SpDE workspace displays the upper-left corner of the PolarPro with a medium zoom factor. This may or may not include the portion of the chip used by the counter design. The scroll bars may be used to view the rest of the chip.



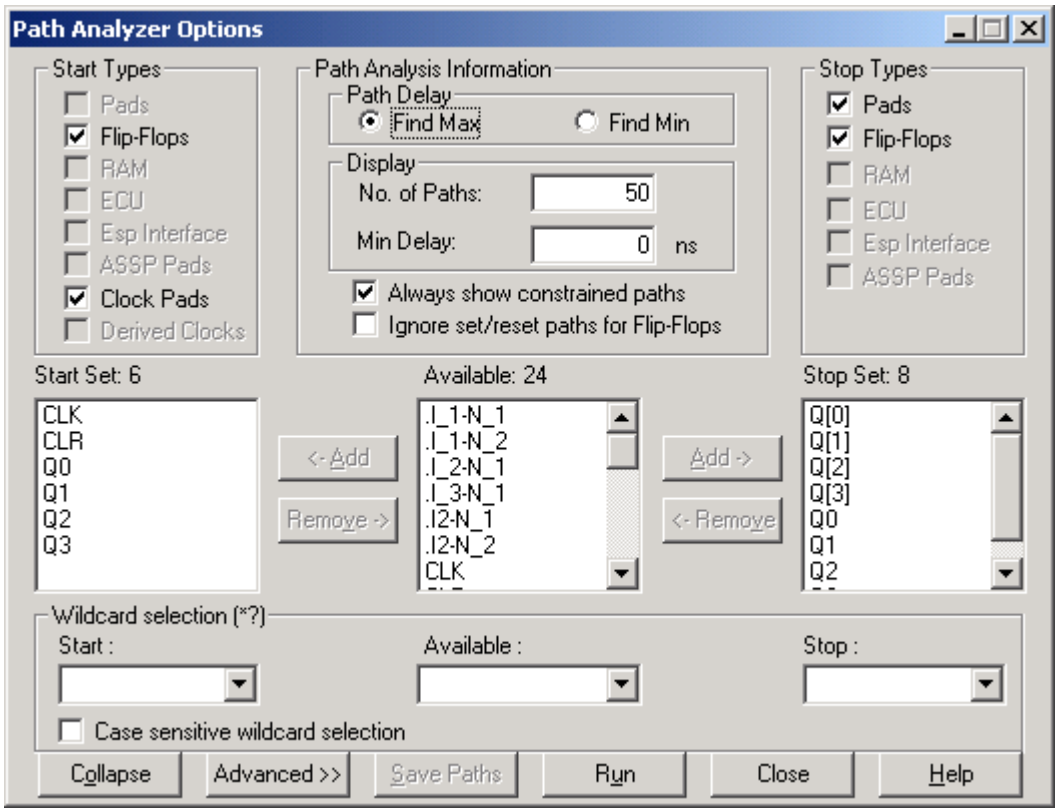
4. Select **View>Full Fit** to view the entire PolarPro at once.
5. Select **View>Zoom In.**
6. To identify the new viewing area, drag a rectangle around the area with the counter.
   a. Position the cursor on the upper-left corner of this area.
   b. Press and hold-down the mouse button.
   c. Drag the cursor to the lower-right corner of this area.
   d. Release the mouse button.

   The workspace now features a portion of the placed and routed layout of `bcount4`. The magenta lines are the internally buffered clock networks. The blue and black lines are the segmented wires. The placement of the logic cells may not seem optimal at first, but it does in fact result in the fastest-possible four-bit counter.

1.12.2 Running the Path Analyzer

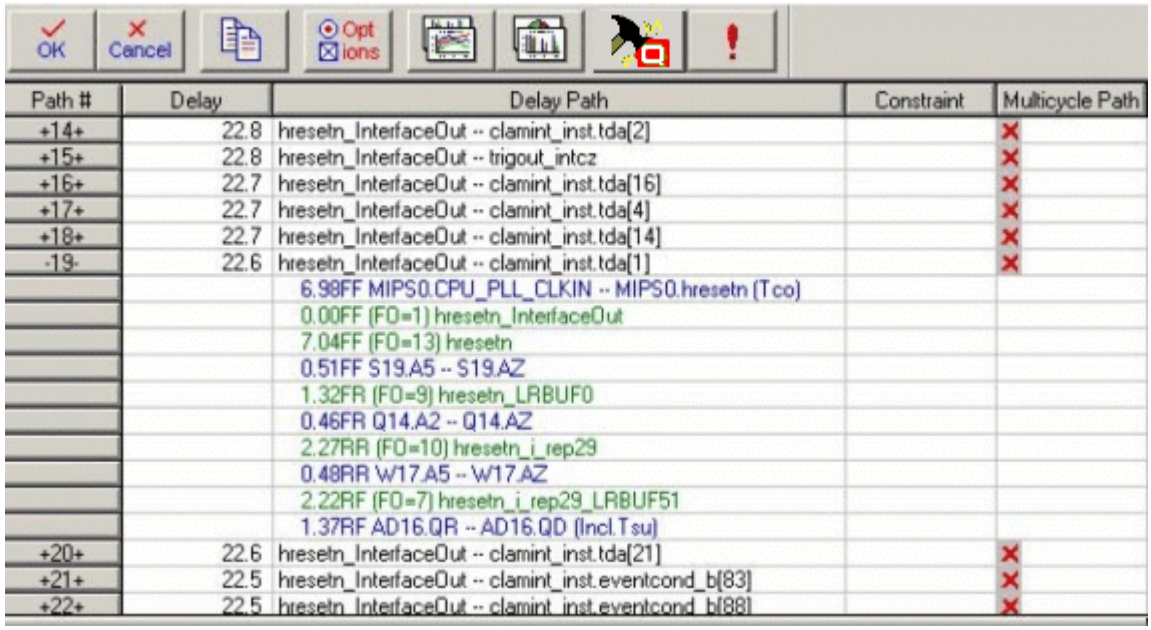
1. From the SpDE menu bar, select **Tools>Path Analyzer,** or click the  icon.

   The Path Analyzer Options window is displayed.



2. Click **Run**.

   After a moment of calculation, the Path Analyzer is displayed.



Path #	Delay	Delay Path	Constraint	Multicycle Path
+14+	22.8	hresetn_InterfaceOut -- clamint_inst.tda[2]		X
+15+	22.8	hresetn_InterfaceOut -- trigout_intcz		X
+16+	22.7	hresetn_InterfaceOut -- clamint_inst.tda[16]		X
+17+	22.7	hresetn_InterfaceOut -- clamint_inst.tda[4]		X
+18+	22.7	hresetn_InterfaceOut -- clamint_inst.tda[14]		X
-19-	22.6	hresetn_InterfaceOut -- clamint_inst.tda[1]		X
		6.98FF MIPS0.CPU_PLL_CLKIN -- MIPS0.hresetn (Tco)		
		0.00FF (FO=1) hresetn_InterfaceOut		
		7.04FF (FO=13) hresetn		
		0.51FF S19.A5 -- S19.AZ		
		1.32FR (FO=9) hresetn_LRBUF0		
		0.46FR Q14.A2 -- Q14.AZ		
		2.27RR (FO=10) hresetn_i_rep29		
		0.48RR W17.A5 -- W17.AZ		
		2.22RF (FO=7) hresetn_i_rep29_LRBUF51		
		1.37RF AD16.QR -- AD16.QD (Incl.Tsu)		
+20+	22.6	hresetn_InterfaceOut -- clamint_inst.tda[21]		X
+21+	22.5	hresetn_InterfaceOut -- clamint_inst.eventcond_b[83]		X
+22+	22.5	hresetn_InterfaceOut -- clamint_inst.eventcond_b[88]		X

Since the Path Analyzer Options window remains open, you can reduce the size of the window by clicking the **Collapse** button. If you choose to change the Path Analyzer Options, you can bring the Options window back to the original size by clicking on the **Options** icon in the Path Analyzer window, or by double-clicking on the title bar of the Path Analyzer Options window.

By default, 50 paths are listed, with the longest path listed first. The Path Analyzer offers flexible configuration that allows the listing to be filtered to only the paths of interest. For a more complete discussion of the Path Analyzer's features, refer to the *Design Constraints and Analysis* chapter of the *QuickWorks User Manual*.

3. Double-click on a path under the **Delay Path** column heading.

   Notice that the path is highlighted in SpDE.

4. Double-click on path numbers under the **Path#** column heading.

   Notice that the path is expanded showing:

   - Each element of the delay
   - The rising or falling edge
   - The fanout of the signal

   For this tutorial most delays include only one logic cell delay, so an expanded path reveals only one element.

5. When you are finished viewing the options, close the Path Analyzer window by clicking **OK**.
6. From the SpDE menu bar, select **File>Save**.

   This will save the design as: `BCOUNT4.CHP`. This is a chip file containing all placement, routing, programming, delay, and test vector information for the design.

1.12.3 Creating a Report File

1. From SpDE, select **Info>Reporting>Report File**. The report file will be saved with the extension `.html` (in this case `BCOUNT4_rpt.html`). The Internet Explorer is launched, displaying this file. This report file contains general design reference information.
2. To view the timing information, select **Info>Reporting>Timing Report**. This report file contains the timing summary along with general design information.

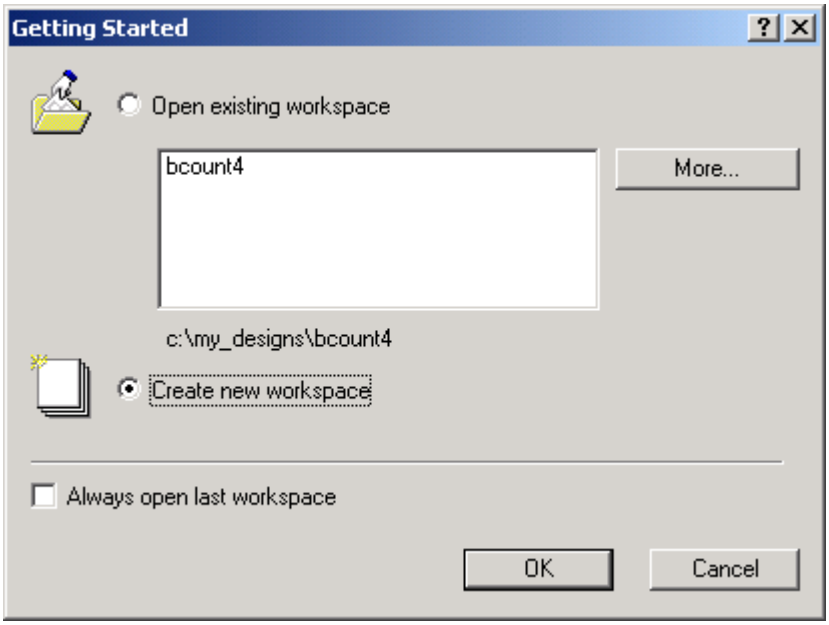
1.13 Simulating the Design for Timing Using Active-HDL

The timing (post-layout) simulation is performed in almost exactly the same way as the functional simulation, which you did earlier in this tutorial.

NOTE: Before performing the post-layout simulation, be sure that you have exited from the pre-layout simulation and closed Active-HDL. Otherwise, the program will not function properly.

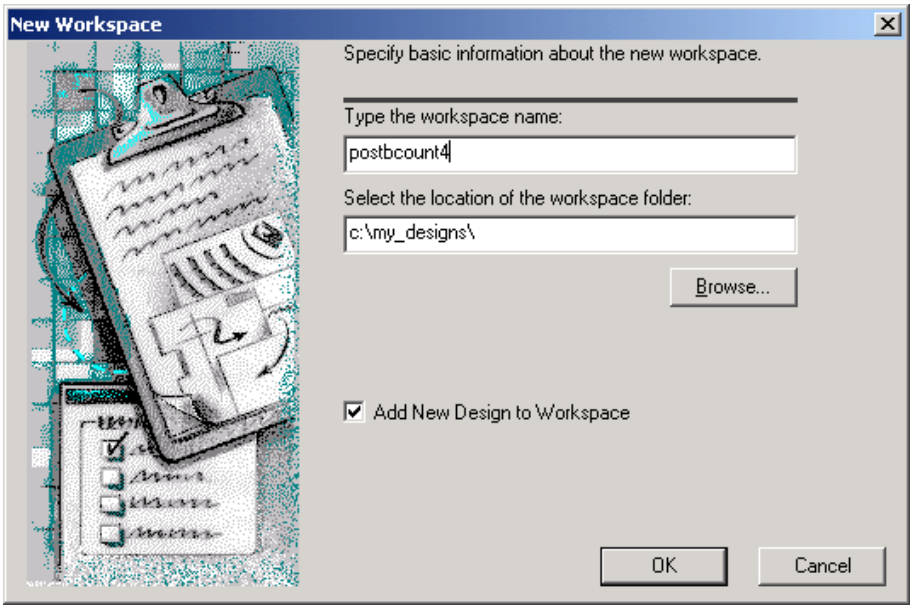
1. From the Hierarchy Navigator menu bar, select **Simulation>Run Simulation**.

The Active-HDL simulation program begins and the Getting Started screen is displayed.



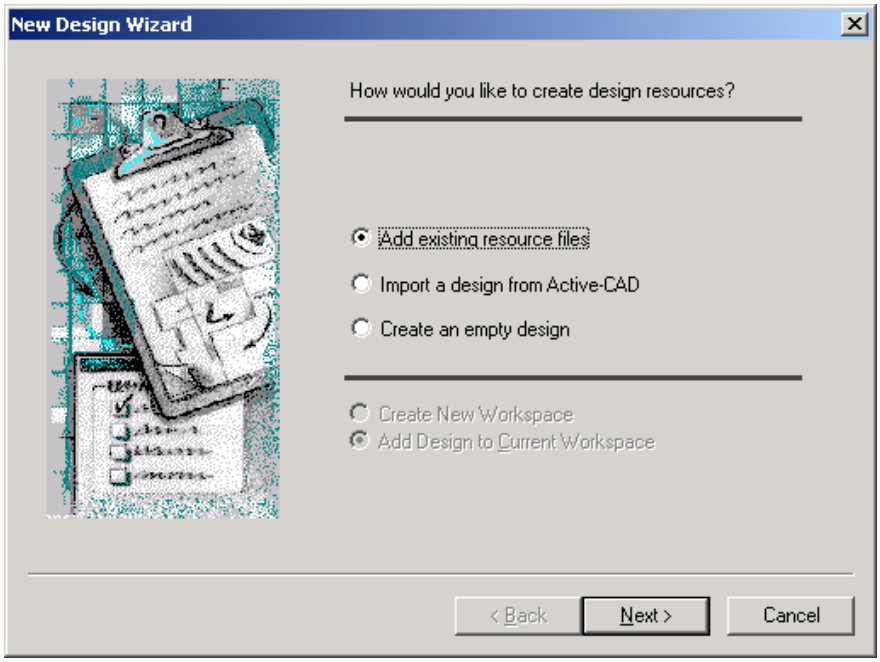
2. Select the **Create new workspace** radio button.
3. Click **OK**.

   The New Workspace screen is displayed.



4. Type the workspace name.
5. Click **OK**.

The New Design Wizard is displayed.

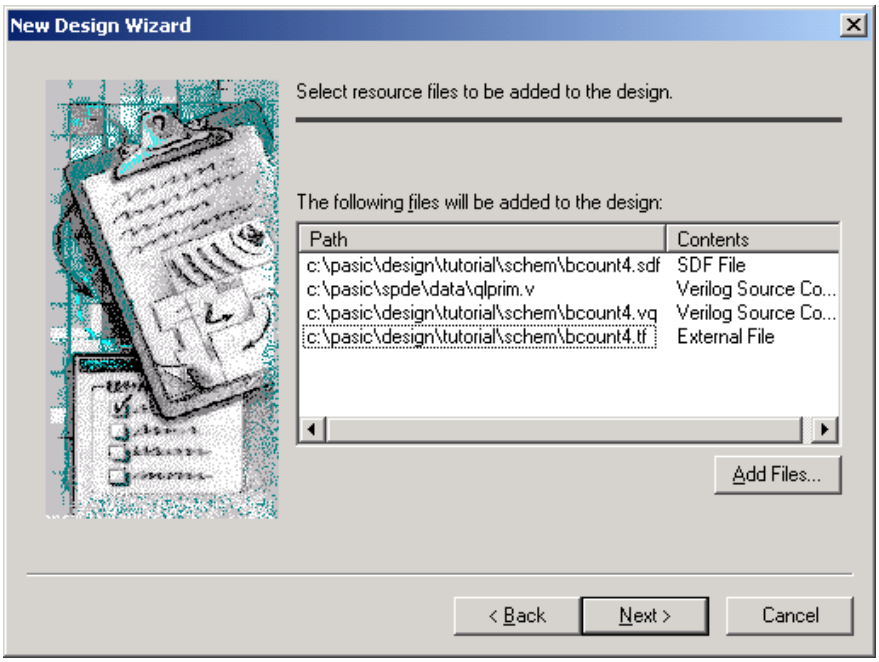


1.13.1 Creating a New Design

To create a new design using the New Design Wizard from the previous step:

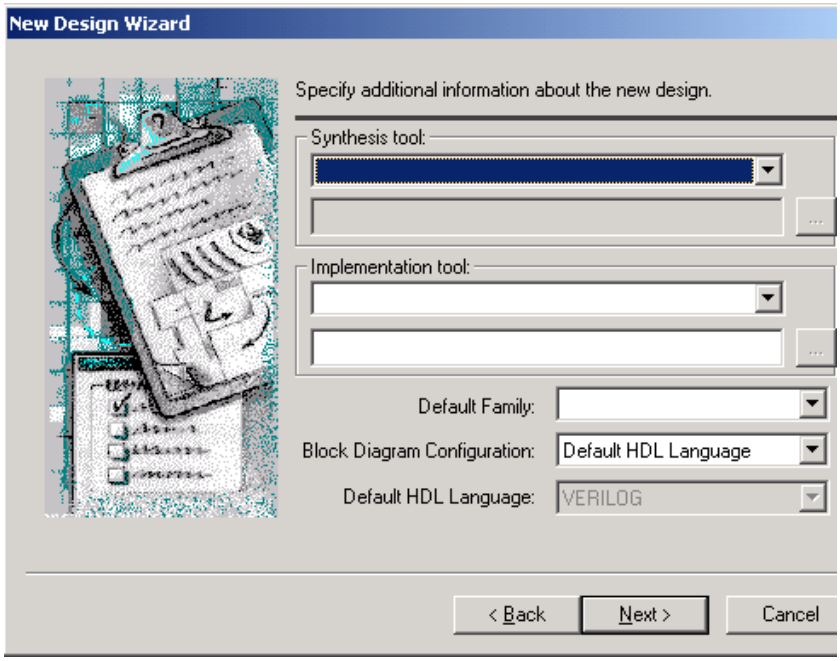
1. Select the **Add existing resource files** radio button.
2. Click **Next**.

   The following screen is displayed prompting you to add files to the design.



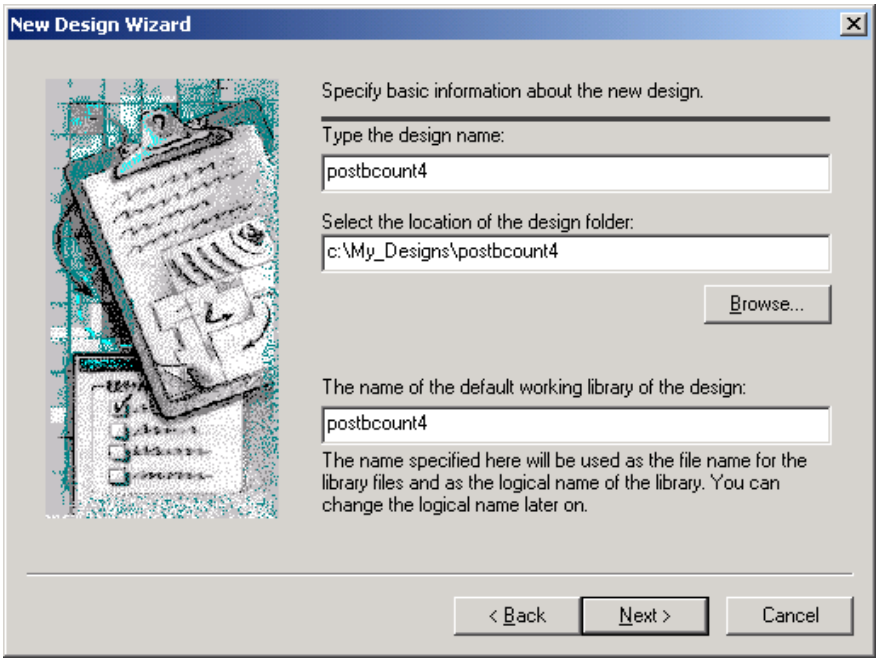
3. Click **Add Files** to browse and add the design files.
4. Click **Next**.

   The following screen is displayed.



5. Select the **Default HDL Language** option.
6. Click **Next**.

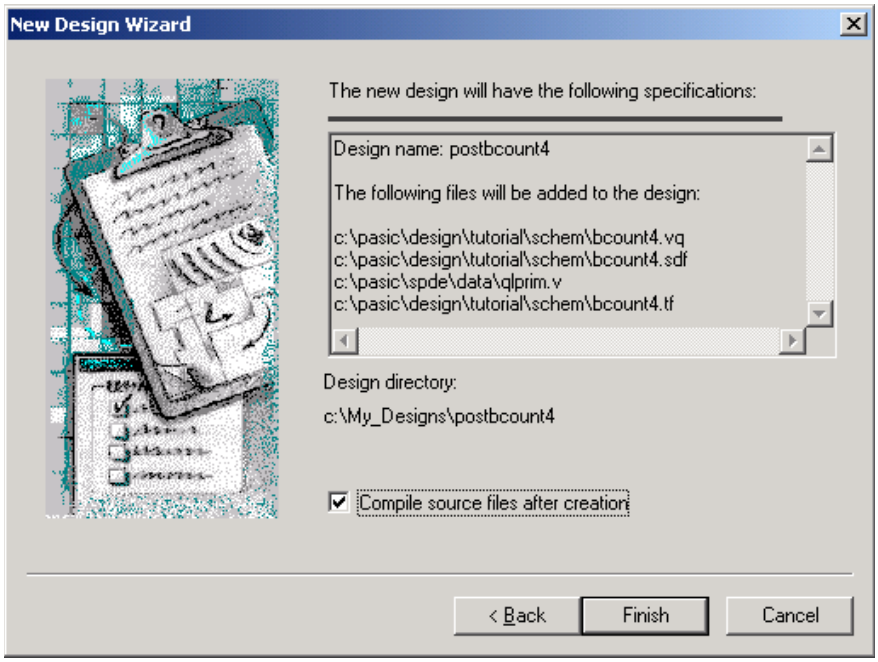
   The following screen is displayed.



7. Type the design name.

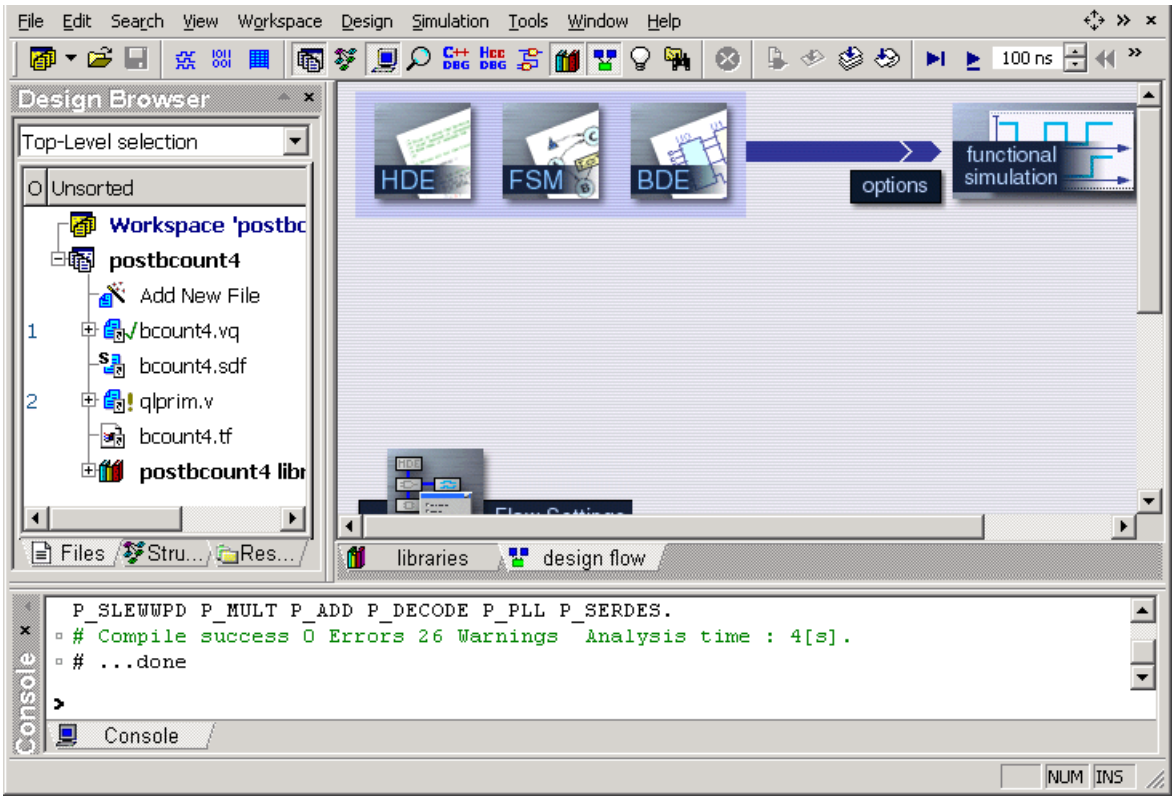
8. Click **Next**.

   The following screen is displayed.



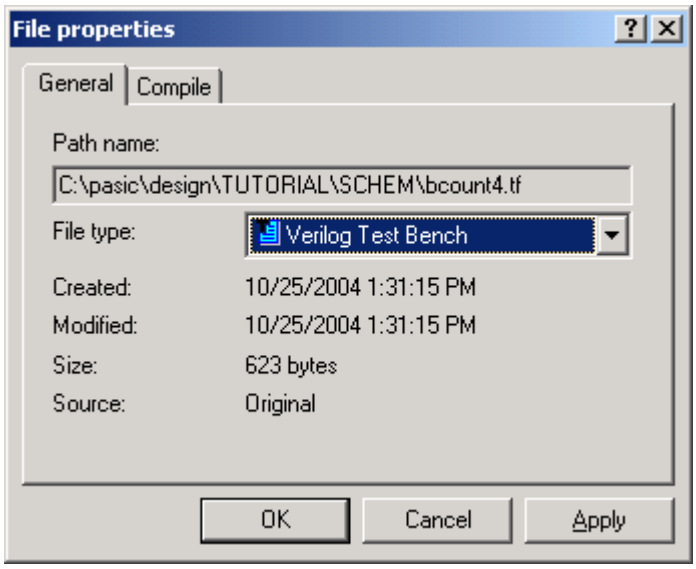
9. Click **Finish**.

   The Active-HDL screen is displayed.



10. Right-click on **bcount4.tf** and select **Properties**.

    The File properties screen is displayed.

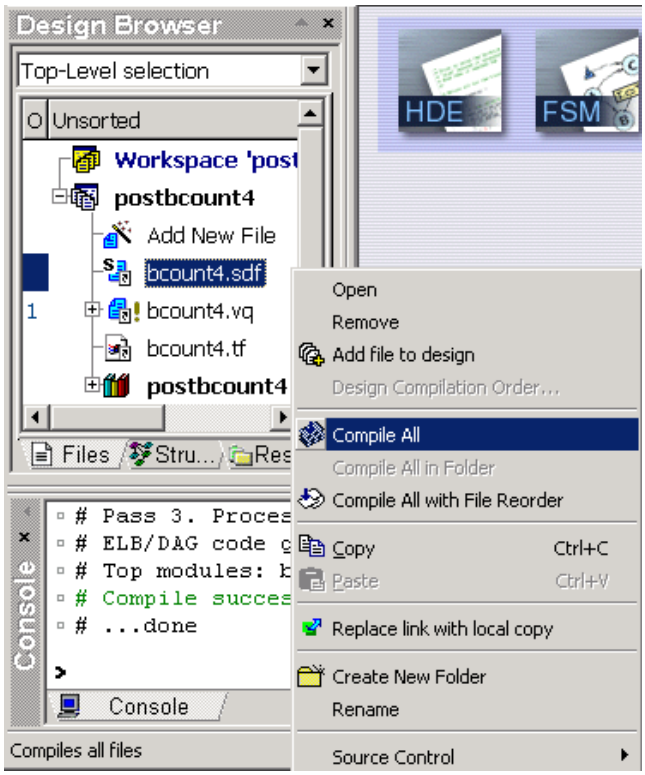


11. Scroll down to select **Verilog Test Bench** from the **File type** pull-down menu.
12. Click **OK**.

1.13.1.1 Compiling the Files

To compile the files:

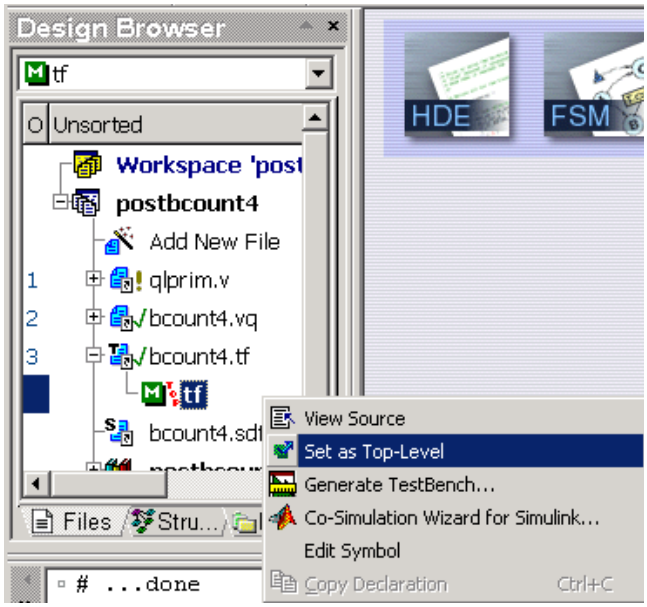
1. Right-click on each file and select **Compile** or **Compile All**.



1.13.2 Setting a Design as a Top Level Design

In this section we will set `.tf` testbench module as the top level design.

1. Click on the plus sign (+) to expand `bcount4.tf`. To set the design as top level right-click on `tf` and select **Set as Top-Level**.



1.13.3 Initializing the Post-Layout Simulation

To initialize the simulation in the Waveform Editor screen:

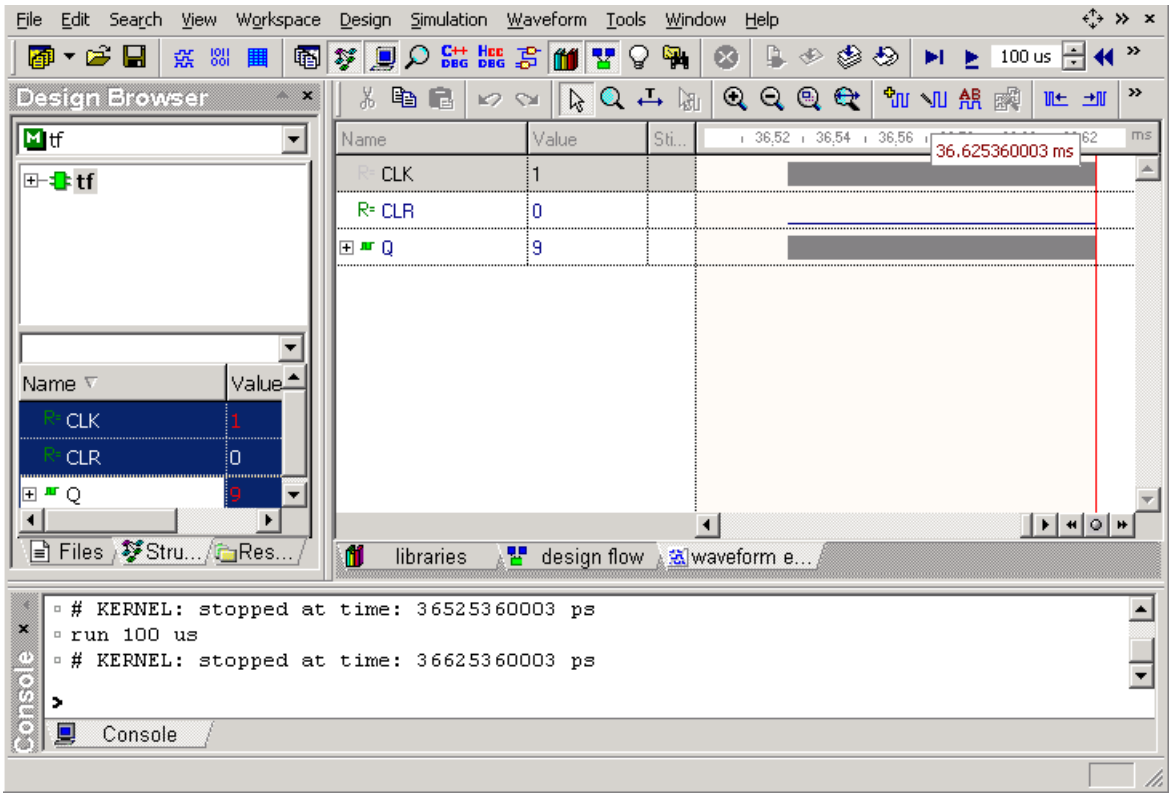
1. From the Active-HDL menu bar, select **Simulation>Initialize Stimulation**.

1.13.4 Running the Post-Layout Simulation

To start running the post-layout simulation:

1. From the Active-HDL toolbar, click on the waveform icon.
2. Drag the signal names from the left panel to the right panel.
3. Expand the screen, in the menu bar type in **`100 us`** and then click the **Run** arrow to the left.

The output of the waveform counters is displayed.



4. After completing the simulation, exit Active-HDL.

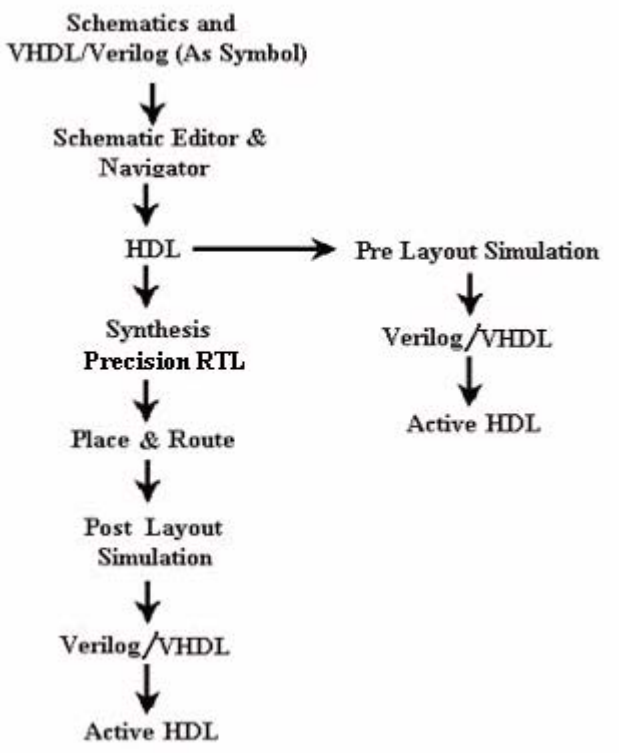
Chapter 2
Mixed Schematic/Verilog Design

This tutorial describes the QuickWorks Mixed Schematic/Verilog design using the Schematic Editor. It contains the following sections:

NOTE: The tutorial assumes that you have a working knowledge of Microsoft Windows. *The Microsoft Windows User's Guide* contains a great deal of useful information for those new to Windows.

2.1 Functional Overview

Figure 2-1: Mixed-Mode Design Flow with Verilog



For reference on design entry and tools, see:

- *Design Flows and Reference* section of the *QuickWorks User Manual*, and the *SCS Schematic Entry User's Manual* for tips on using SCS Design Entry.
- *Precision RTL User's Guide* for information on Precision.

In this tutorial you will create a top-level schematic containing two 4-bit counters. One of the counters will be created using schematics, and the other using Verilog. You will enter the schematics using the Schematic Editor, and the Verilog code with any HDL text editor. The complete design will be inspected using the Hierarchy Navigator, and a Verilog netlist will be generated. The netlist will be synthesized with Precision RTL, and a post-synthesis/pre-layout Verilog and VHDL netlists will be generated. After the simulation outputs have been inspected and proper functionality verified, the design will be optimized, placed, and routed. The Delay Modeler will generate precise post-layout delays, which will be back-annotated for simulation. Post-layout simulation will be run, this time producing accurate timing results.

Figure 2-2: Top Level Design

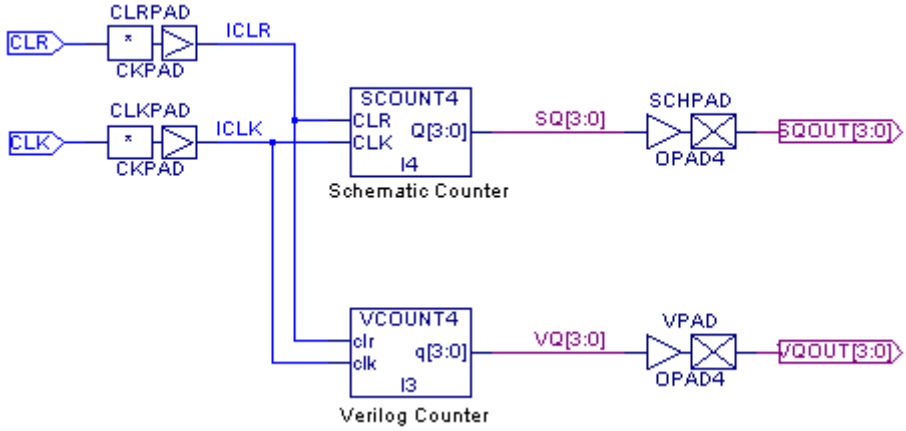
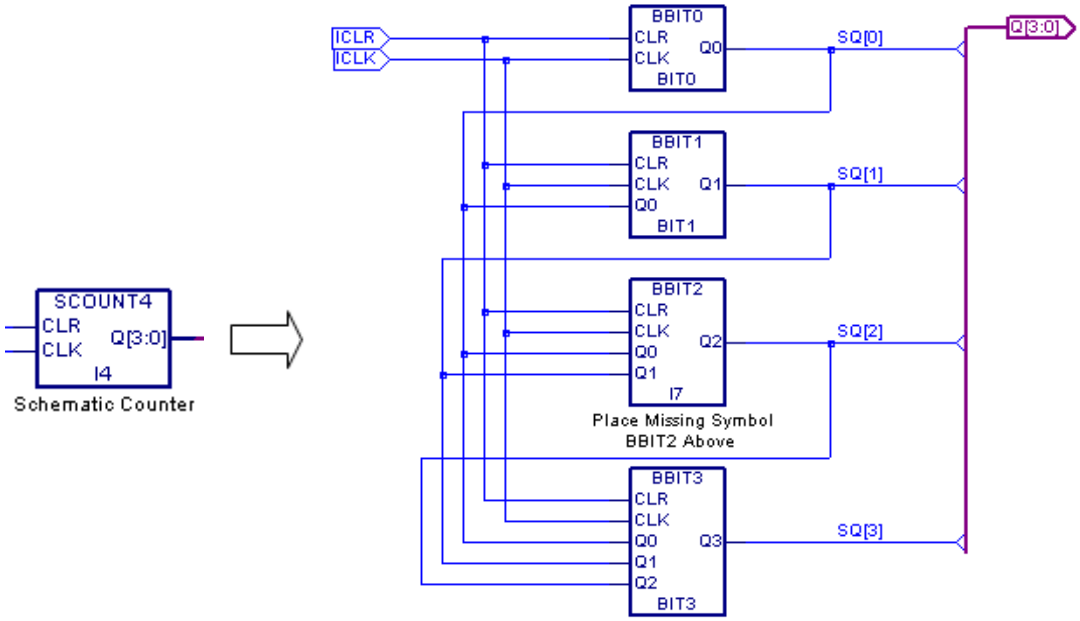


Figure 2-3: Push Down View of SCOUNT4



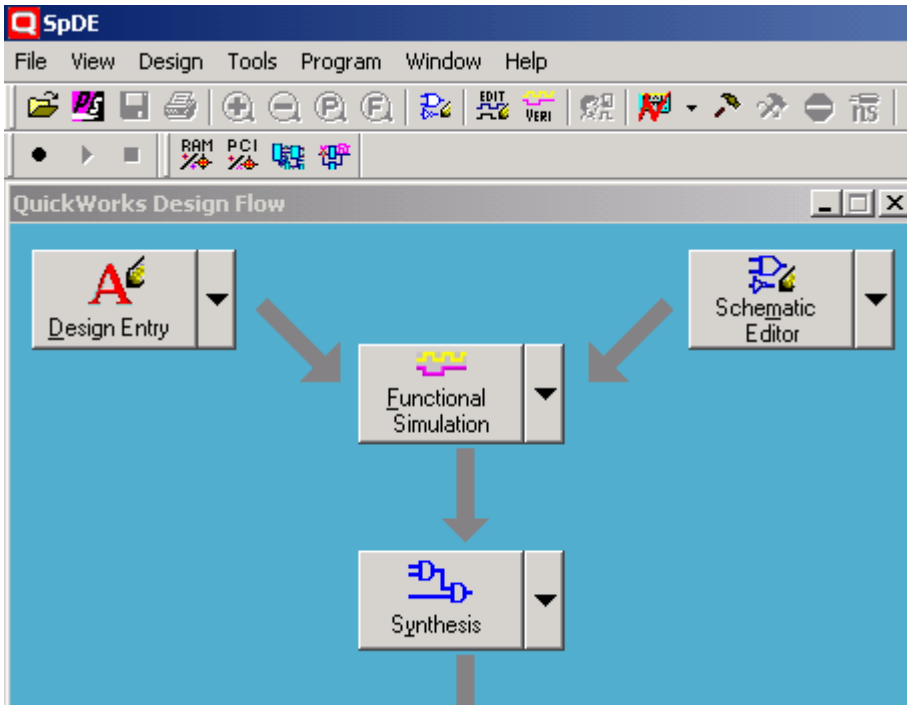
2.2 Creating a Schematic Design

2.2.1 Entering a Schematic Design

To create a mixed schematic Verilog design:

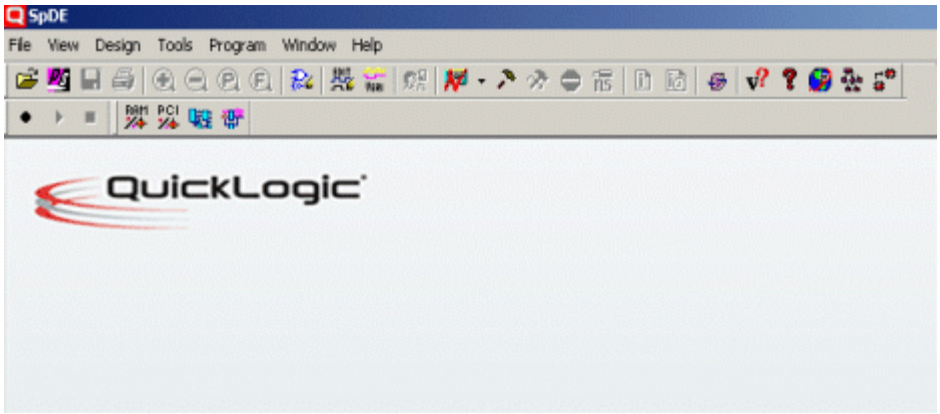
1. Select **Start>Programs>QuickLogic>SpDE**, or click the **SpDE** icon on your desktop.

The SpDE window is displayed and all of the QuickWorks design resources are now available for use.



2. Close the QuickWorks Design Flow window by clicking the **X** in the upper right corner. This method of design will not be used for this tutorial.

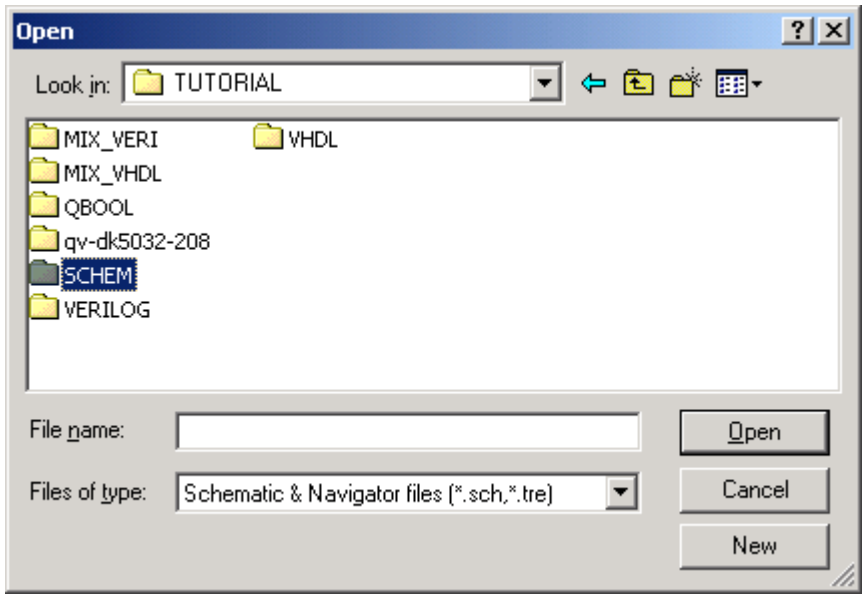
   The SpDE window is displayed. The SpDE toolbar contains icon buttons for executing commands quickly. The status bar at the bottom of the SpDE window displays status messages periodically.



NOTE: See the SpDE Menu Command Reference chapter of the *QuickWorks User Manual* for a full explanation of all available icons.

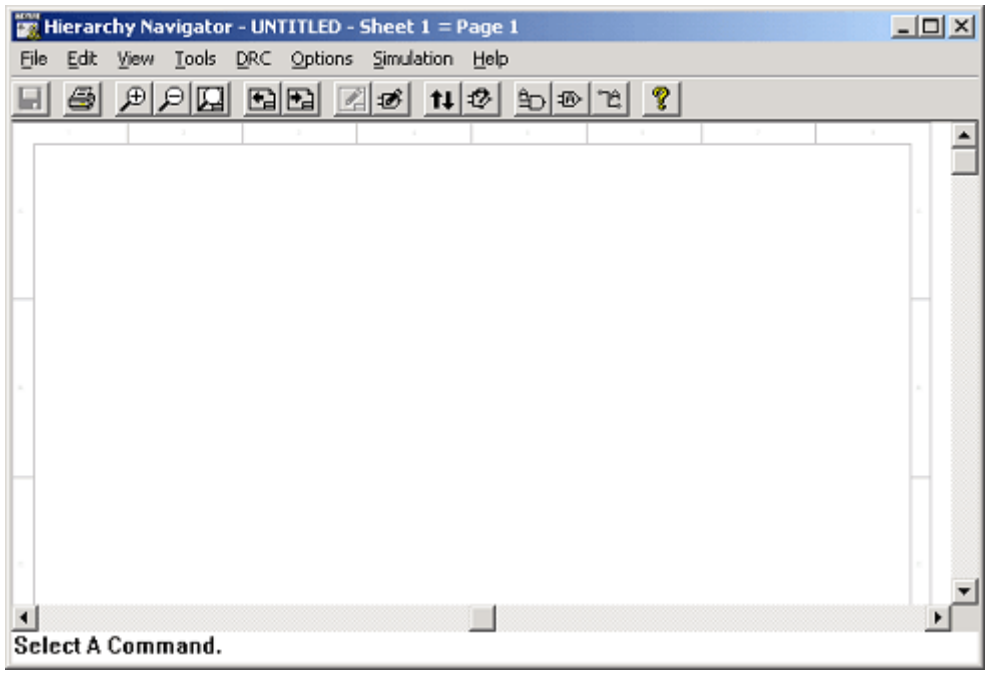
3. From the SpDE menu bar, select **Design>Schematic Editor & Navigator**, or click the  icon.

The Open window is displayed.



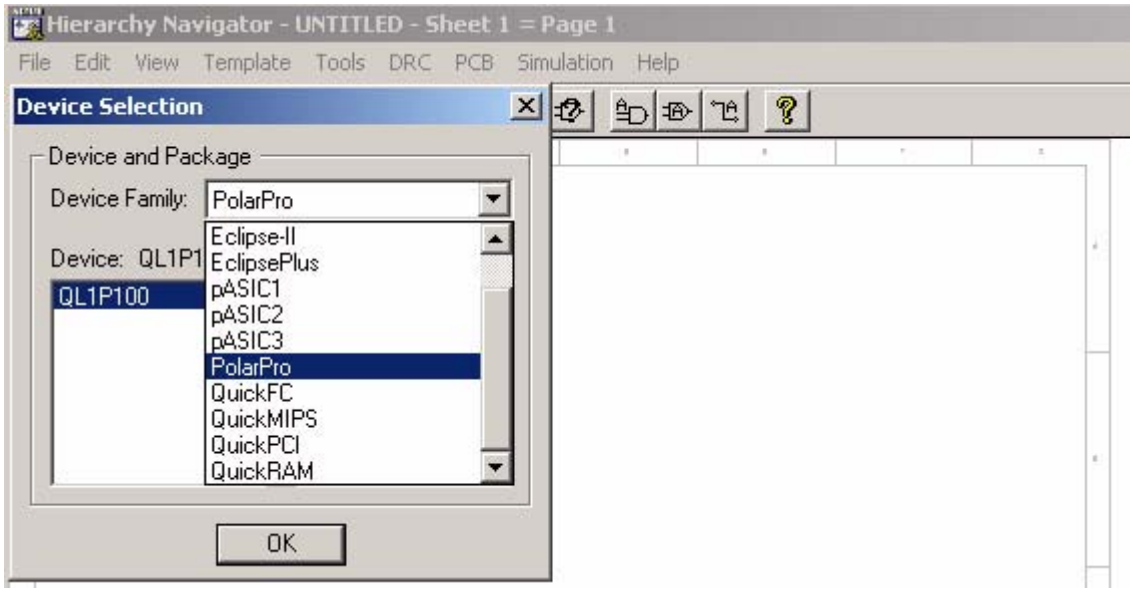
4. Navigate to the default directory `C:\pasic\design\TUTORIAL\SCHEM\.`
5. Click **New**.

   The Hierarchy Navigator window is displayed.



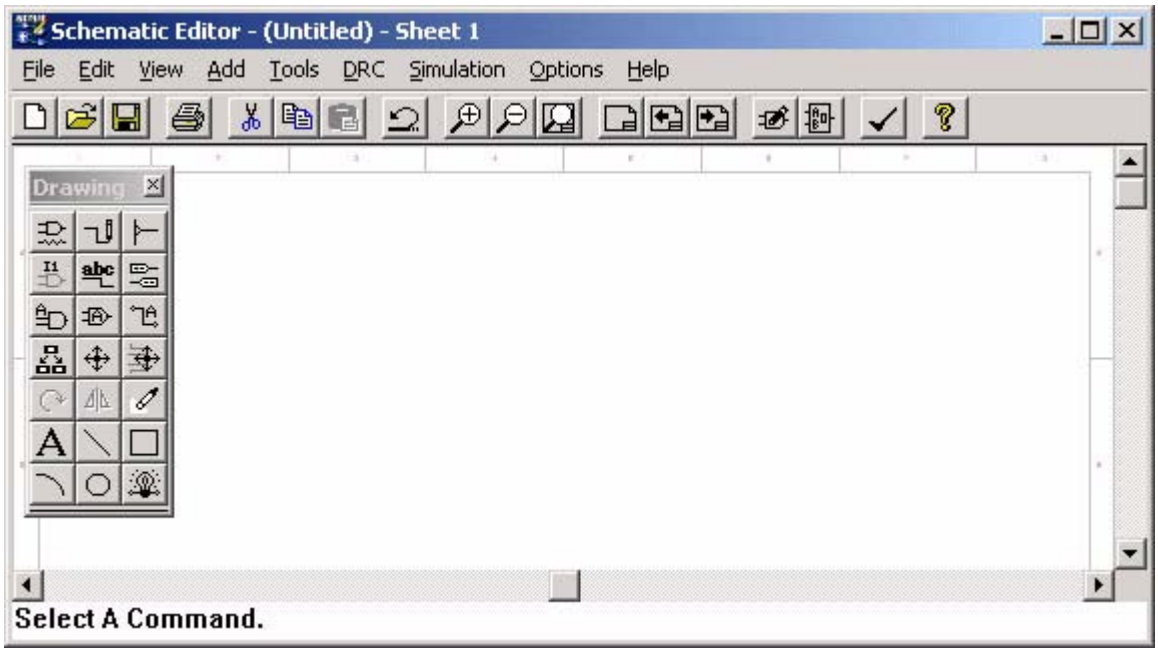
6. From the Hierarchy Navigator menu bar, select **File>Create Schematic**.

The Device Selection window is displayed.



7. Select **PolarPro** for the Device Family, **QL1P100** for the Device, and **PF144** for the Package.
8. Click **OK**.

   The Schematic Editor is displayed.



You will create the schematic. But first, you must create the lower level as shown in the following.

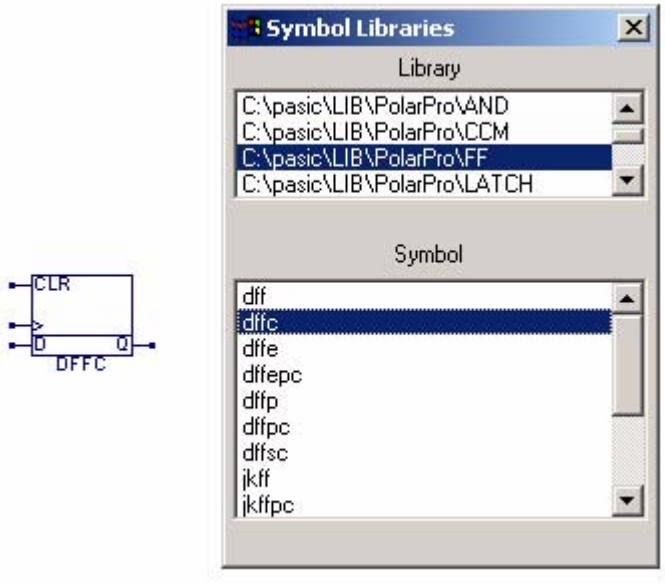
2.2.1.1 Adding Symbols

To add symbols to the schematic design:

1. From the Schematic Editor menu bar, select **Add>Symbol.**

   The Symbol Libraries window is displayed.

2. In the `C:\pasic\LIB\PolarPro\FF` library, select the **DFFC** symbol and drag it onto the workspace. Left-click to place it on the workspace and left-click to release your selection.



3. Continue to add symbols until the schematic looks like the following schematic.

   See “Adding Symbols” on page 6 for more detailed information.

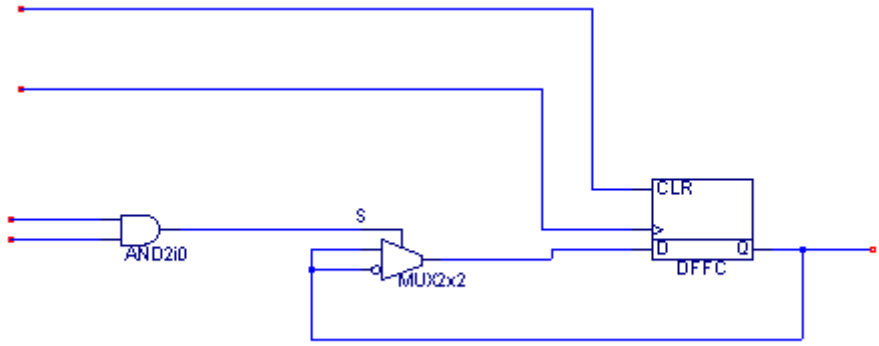
2.2.1.2 Connecting the Symbols

To add wires to connect the symbols:

1. From the Schematic Editor menu bar, select **Add>Wire**.

   The status bar line reads: `Wire - Click or Drag to Begin Wire`.

2. Add wires until your schematic looks like the following arrangement.



NOTE: To delete wires, select **Edit>Delete** and click on the wire to be deleted.

2.2.1.3 Adding Net Names

To define the net names.

1. From the Schematic Editor menu bar, select **Add>Net Name**.

   The status bar line reads: `Net Name - Enter Net Name =`.

2. Type: **`CLK`**.

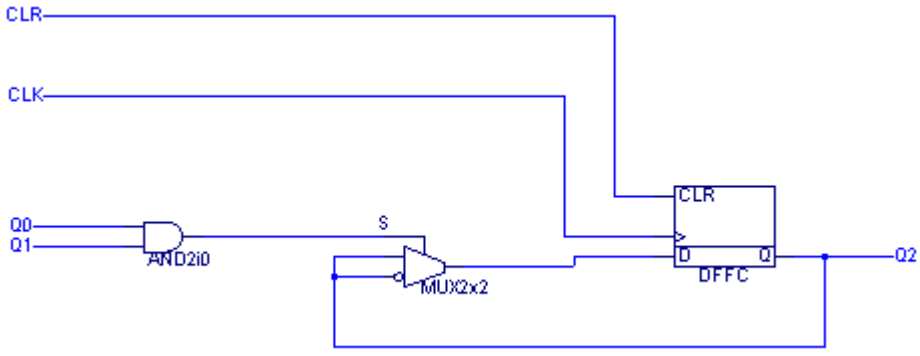
3. Press **Enter** on the keyboard.

   The status bar line reads: `Net Name - Place Net Name Flag 'CLK' - Shift Key to Rename`.

4. Position the crosshairs of the cursor on the end of the clock wire created above and click.

   This places the CLK flag at the end of the selected wire.

5. Add the net names, **`CLR, Q0, Q1,`** and **`Q2`** as shown in the following arrangement.



2.2.1.4 Defining Ports

The primary inputs and outputs of the schematic must now be marked with I/O markers.

1. From the Schematic Editor menu bar, select **Add>I/O Marker**.

   The status bar line reads: `Select Net Name Flag on End of Wire`. The I/O Markers window appears.

2.2.1.4.1 Adding an Input Marker

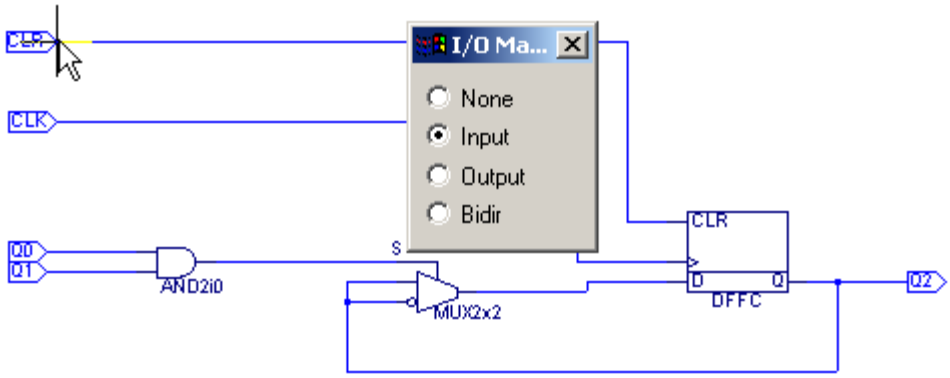
To add an input marker:

1. Click the **Input** option in the I/O Markers window.
2. Position the crosshairs of the cursor at the end of the clock wire and click.

   This places an input marker on the CLK flag.

NOTE: To create an I/O marker, the net name flag must be placed at the end of its wire (as opposed to along the length of its wire), as shown in the figures above.

3. Repeat this operation for the CLR, Q0,and Q1 flags. All three input markers can be added in one operation by dragging a rectangle around the three net names.



2.2.1.4.2 Adding an Output Marker

To add an output marker:

1. Click the **Output** option in the I/O Markers window.
2. Position the crosshairs of the cursor at the end of the output wire on the Q2 flag, and click to create the output marker.

2.2.1.5 Saving the Schematic

To save the schematic:

1. From the Schematic Editor menu bar, select **File>Save As**.

   A dialog box prompts you for the name of the file.

2. Navigate to the default directory `C:\pasic\design\TUTORIAL\MIX_VERI` and type: **`BBIT2.sch`**.
3. Click **Save**.

2.2.1.6 Creating a Symbol

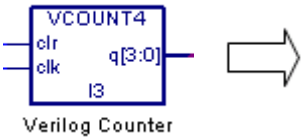
To make a matching symbol for this schematic:

1. From the Schematic Editor menu bar, select **File>Matching Symbol.**

   You now have a symbol for this schematic to also use in other schematics.

2.3 Creating a Verilog Counter

You will now create the Verilog counter as shown. You will then combine this counter with the top level design.




```
module vcount4 (q, clk, clr);

input clk, clr;
output [3:0] q;
reg [3:0] q;

always @(posedge clk or posedge clr)
 begin
    if(clr)
        q = 0;
    else
        q = q + 1;
    end

endmodule
```

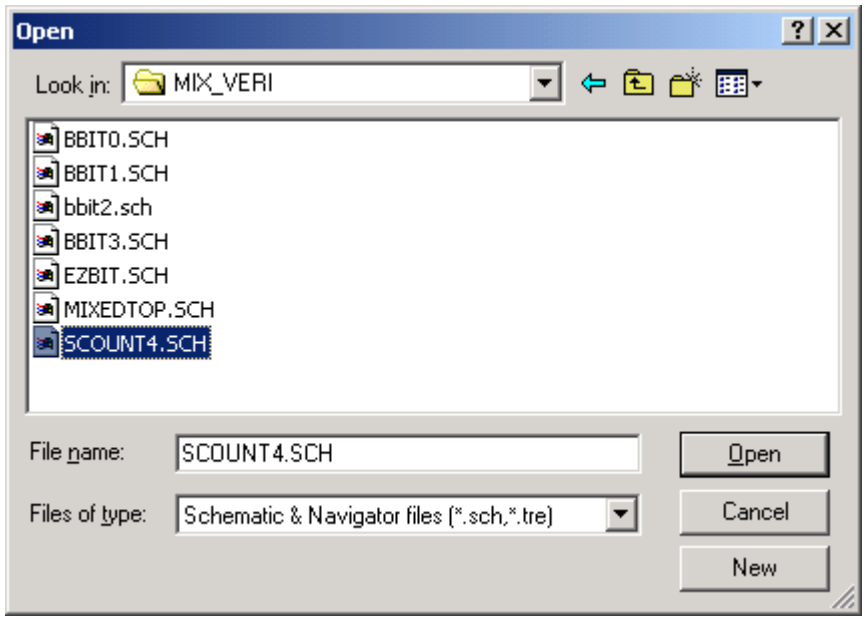
After finishing, save the file as `VCOUNT4.V` in the `MIX_VERI` folder.

2.4 Creating the Top Level Design

2.4.1 Opening a Schematic

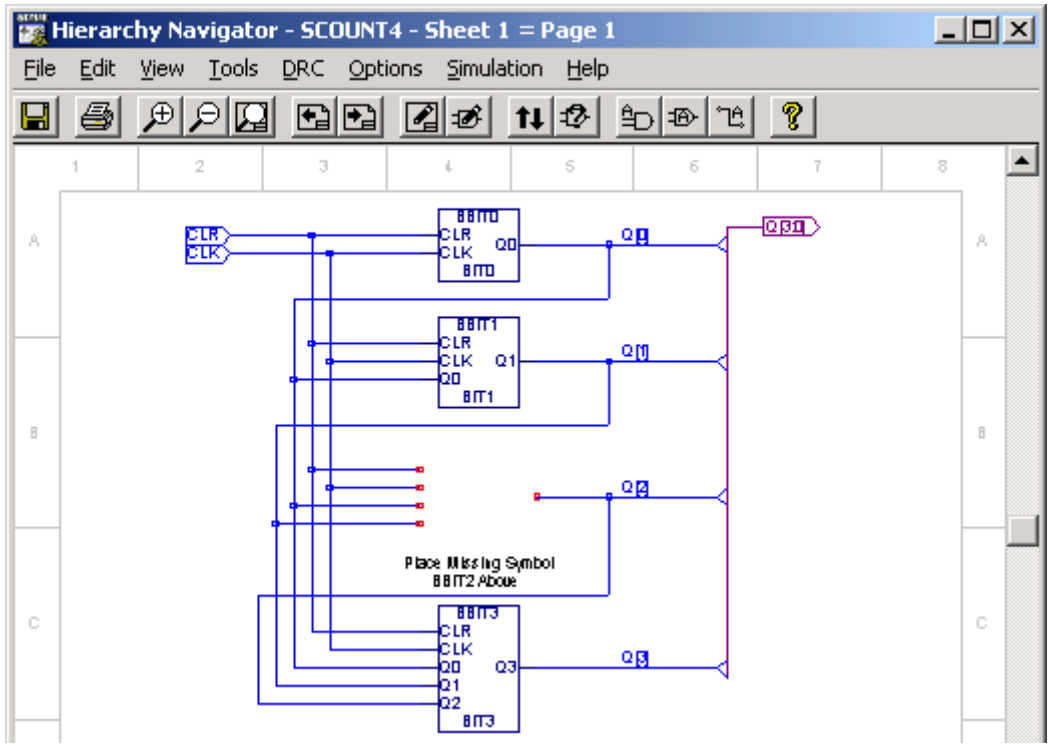
1. From the SpDE menu bar, select **Design>Schematic Editor & Navigator**, or click the  icon.

   The Open window is displayed.



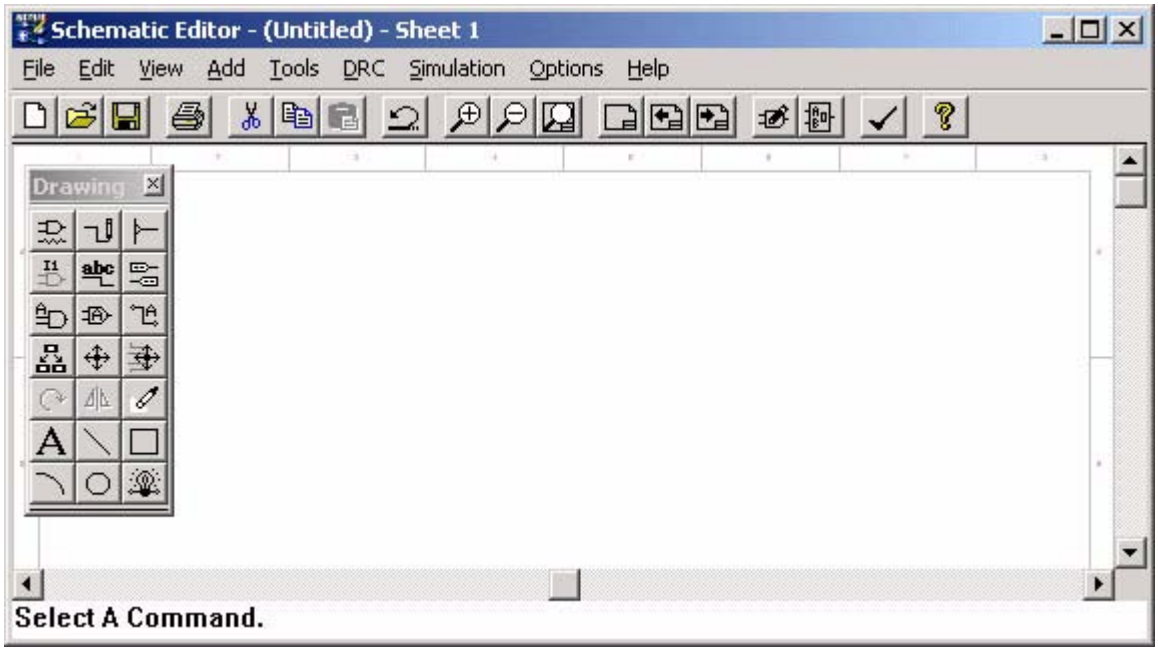
2. Navigate to the default directory `C:\pasic\design\TUTORIAL\MIX_VERI\.`
3. Select `SCOUNT4.SCH` and click **Open**.

The Hierarchy Navigator window is displayed.

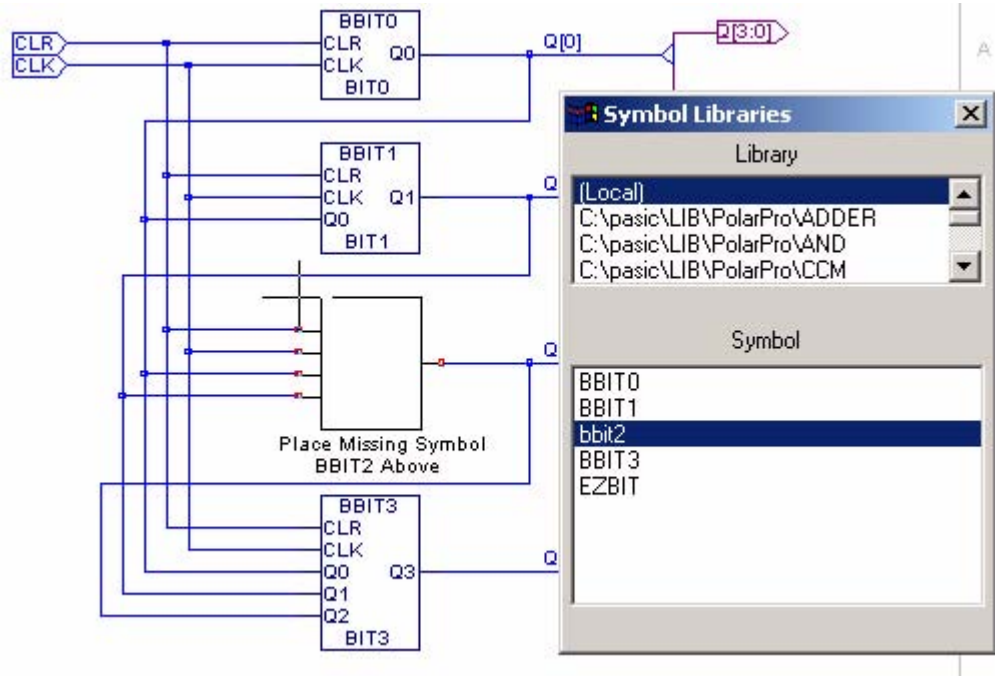


4. From the Hierarchy Navigator menu bar, select **File>Edit Schematic**.

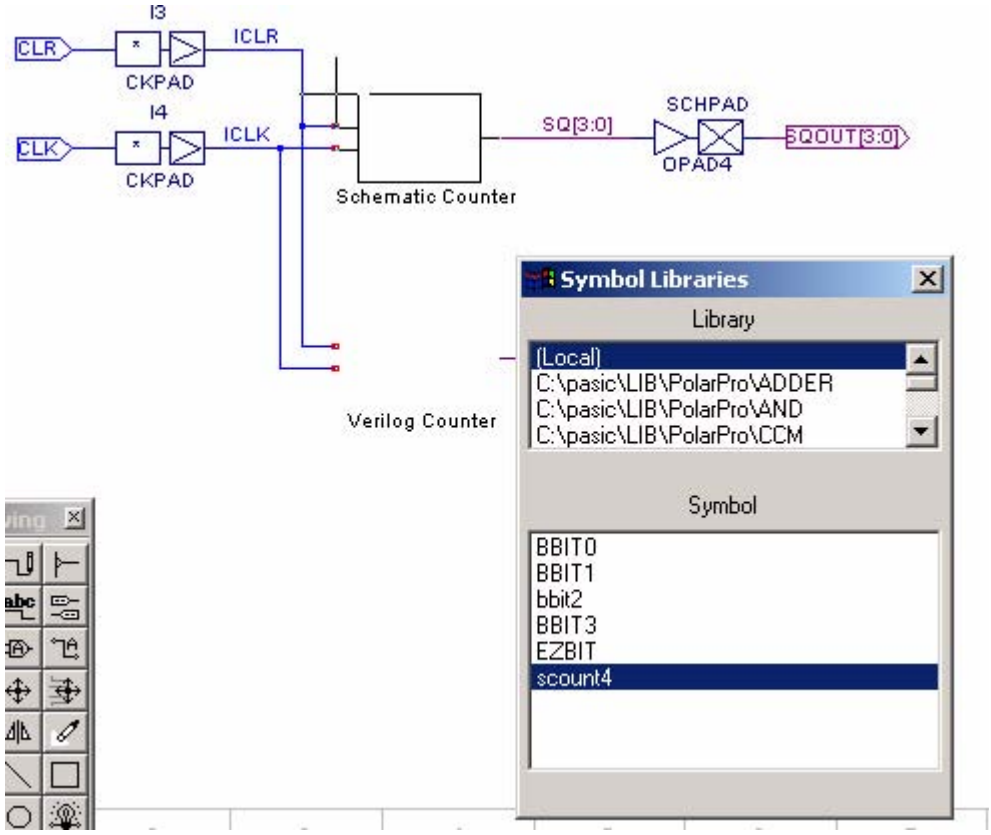
   The Schematic Editor is displayed.



5. From the Schematic Editor menu bar, select **Add>Symbol** and select the **bbit2** symbol that you created earlier. Drag it to the location shown below. Left-click to place the symbol.



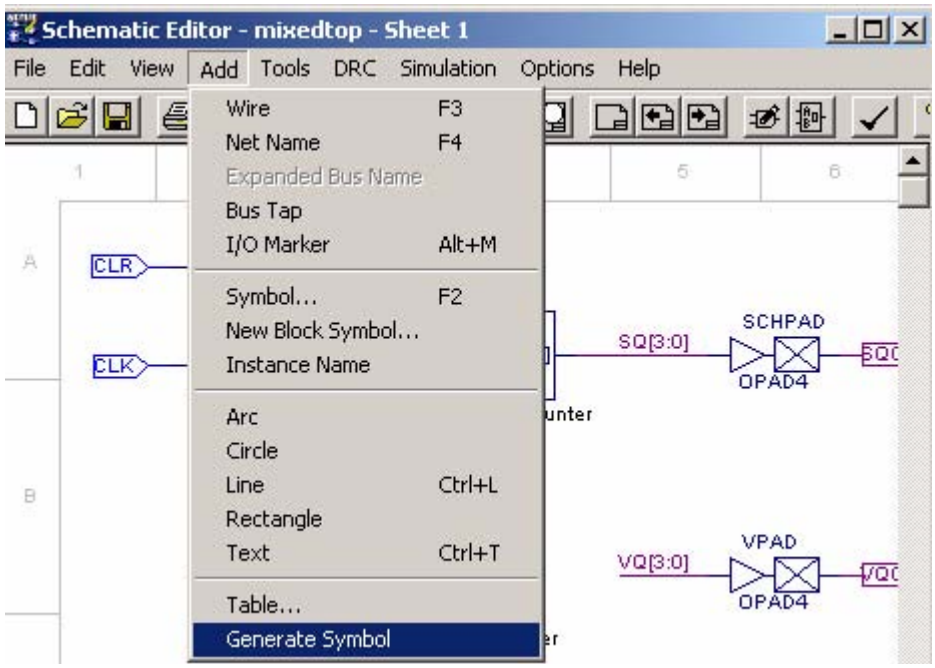
6. Select **File>Matching Symbol** to create a matching symbol.
7. Select **File>Open** and double-click on `MIXEDTOP.SCH`.
8. Select **Add>Symbol** and add the **scount4** symbol as shown.



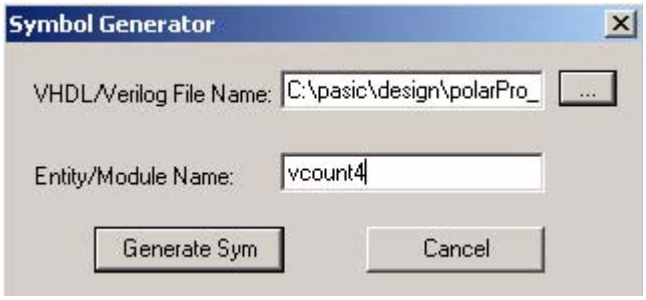
2.4.2 Adding a New Block Symbol

In this section will create a symbol for the Verilog counter and add it to `MIXEDTOP.SCH`.

1. From the Schematic Editor menu bar, select **Add>Generate Symbol**.

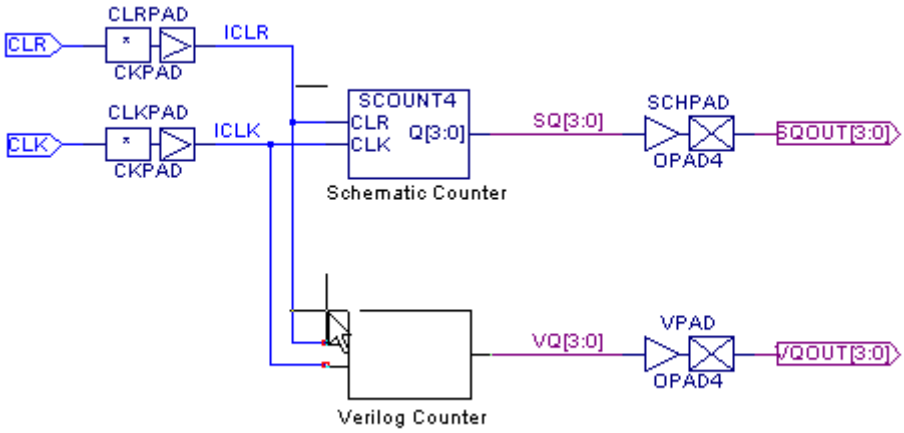


2. To create a symbol for the Verilog counter, select **PolarPro** and type **vcount4** as shown in the following.



3. Click **Generate Sym**.

4. When the symbol appears, drag and drop the symbol as shown in the following.



5. Select **File>Save** to save the file.

2.5 Exporting the Schematic to Verilog Code

In this section you will export the schematic you have created to Verilog code. Then, you will use this code to perform a pre- and post-layout simulation.

2.5.1 Opening the Schematic

To open the schematic:

1. From the SpDE menu bar, select **Design>Schematic Editor & Navigator**, or click the  icon.

   The Open window is displayed.

2. Navigate to the default directory `c:\pasic\design\TUTORIAL\MIX_VERI\MIXEDTOP.SCH` and click **Open**.

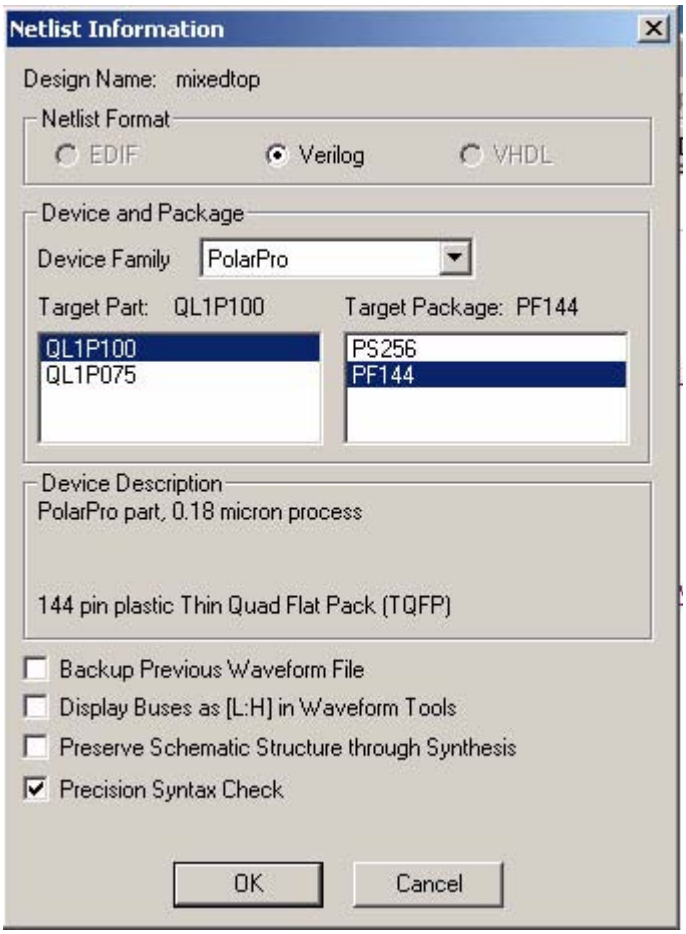
   The Hierarchy Navigator is displayed.

2.5.2 Exporting to Verilog

To export to Verilog:

1. From the Hierarchy Navigator menu bar, select **Tools>Export QuickLogic**.

The Netlist Information window is displayed.



2. Select all the options shown and click **OK**.
3. In the Pre-layout Information dialog box, click **Done**.

4. From the Hierarchy Navigator menu bar, select **File>Save**.

2.5.3 Verifying Creation of mixedtop.v

To verify that `mixedtop.v` has been created, go to the folder `C:\pasic\design\TUTORIAL\MIX_VERI.`

2.6 Pre-Layout Simulation Using Active-HDL

In this section you will use `mixedtop.v` to do a pre-layout simulation using Active-HDL. You will use the Waveform Editor to create a test waveform. The file will be saved as a `.tf` file and will be used to test the design shown previously in this chapter.

2.6.1 Creating the Test Waveform

2.6.1.1 Launching the Waveform Editor

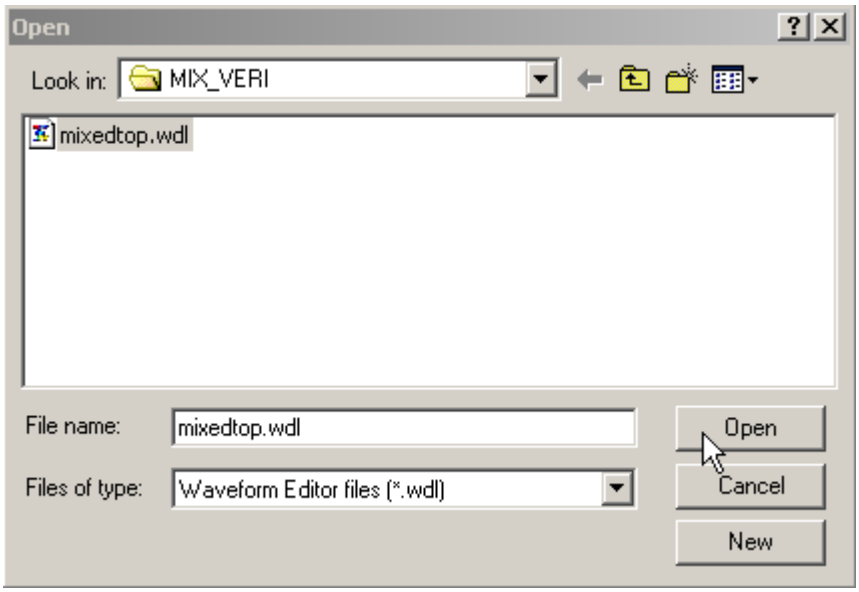
To launch the Waveform Editor:

1. From the SpDE toolbar, click on the **Waveform Editor**  icon.

2.6.1.2 Creating the Test Waveform

To create a test waveform:

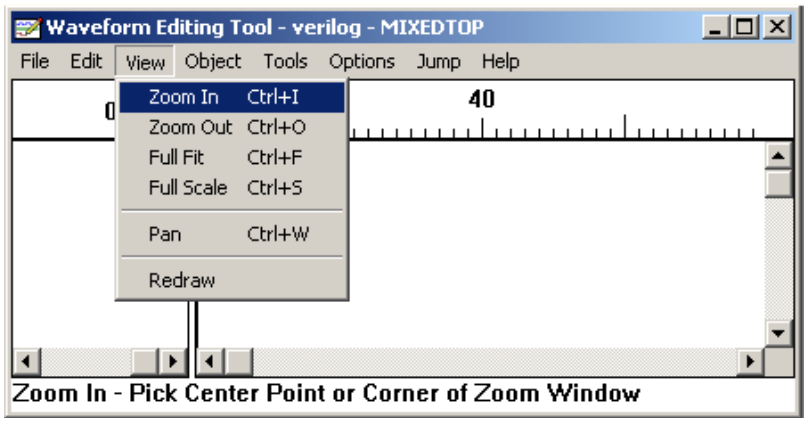
1. Select **mixedtop.wdl** and click on **Open**.



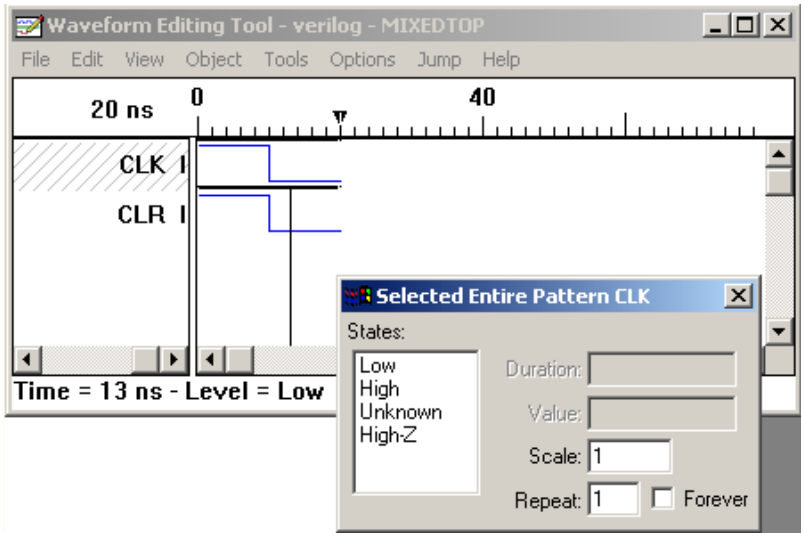
2. Select **View>Zoom In**.

   The pointer will change into a large Z.

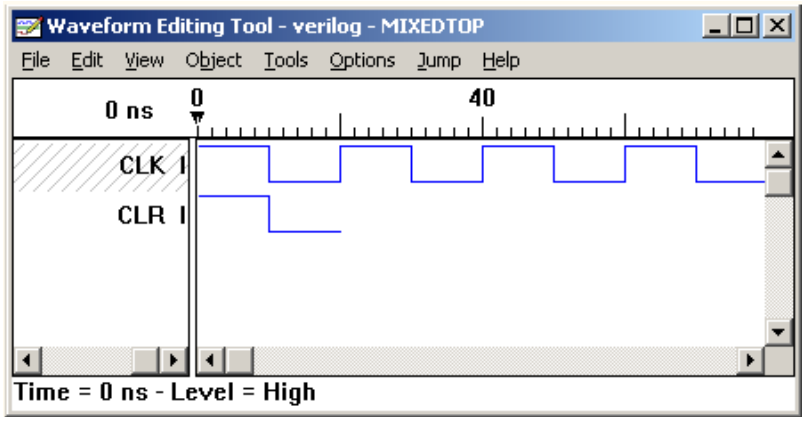
3. Click on the screen to zoom in until the scale matches the setting shown as follows.



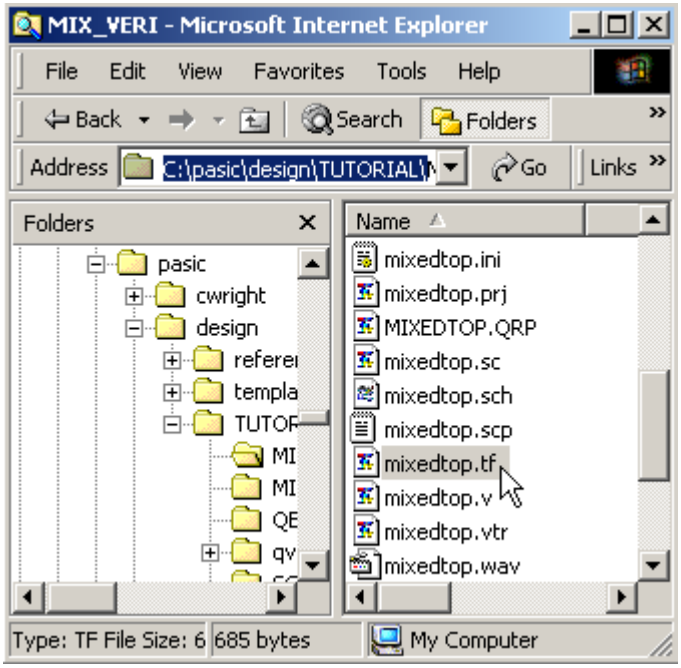
4. Right-click to discontinue the Zoom In function.
5. Click on **CLR** until it resembles the following screen.
6. Click on **CLK** until it resembles the following screen.
7. Check **Forever** in the Selected Entire Pattern CLK screen to create the clock waveform. Click on the line as shown to get the screen to appear.



The completed waveform will look as follows.



8. To save the waveform click **File/Save** which creates the file **mixedtop.tf**.
9. To verify that the `.tf` file was created, open Windows Explorer and go to `C:\pasic\design\TUTORIAL\MIX_VERI`. The `mixedtop.tf` file should be there.



2.6.2 Starting Active-HDL

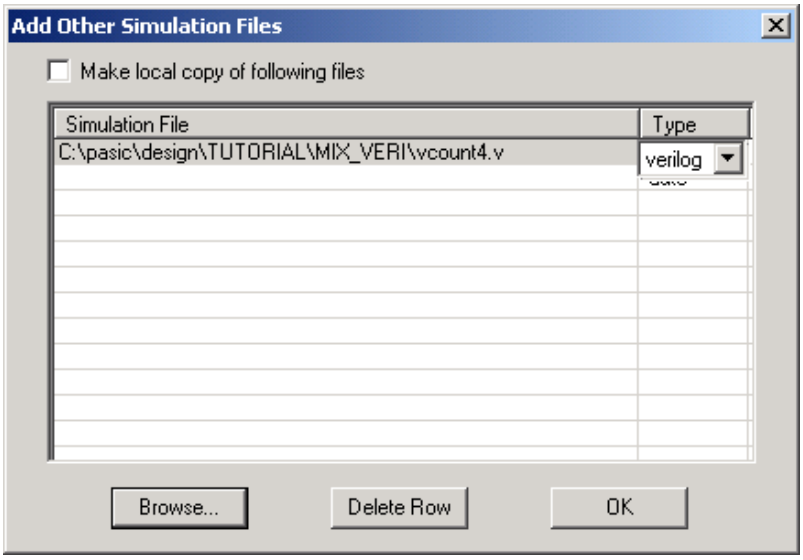
To launch Active-HDL:

1. From the SpDE toolbar, click on the **Active-HDL Simulator** icon.

   The Active-HDL Interface screen is displayed.

2. Select **Verilog** and **Pre-Layout** for the Simulation Type.
3. Select **PolarPro** as the Target Family and **QL1P100** as the Target Part from the pull-down menus.
4. Browse to select `mixedtop.tf` as the Test Fixture File and `mixedtop.v` as the Design File located in the default directory `C:\pasic\design\TUTORIAL\MIX_VERI`.
5. Type `tf` as the Top Module Name.
6. Click **Add Other Files...**.

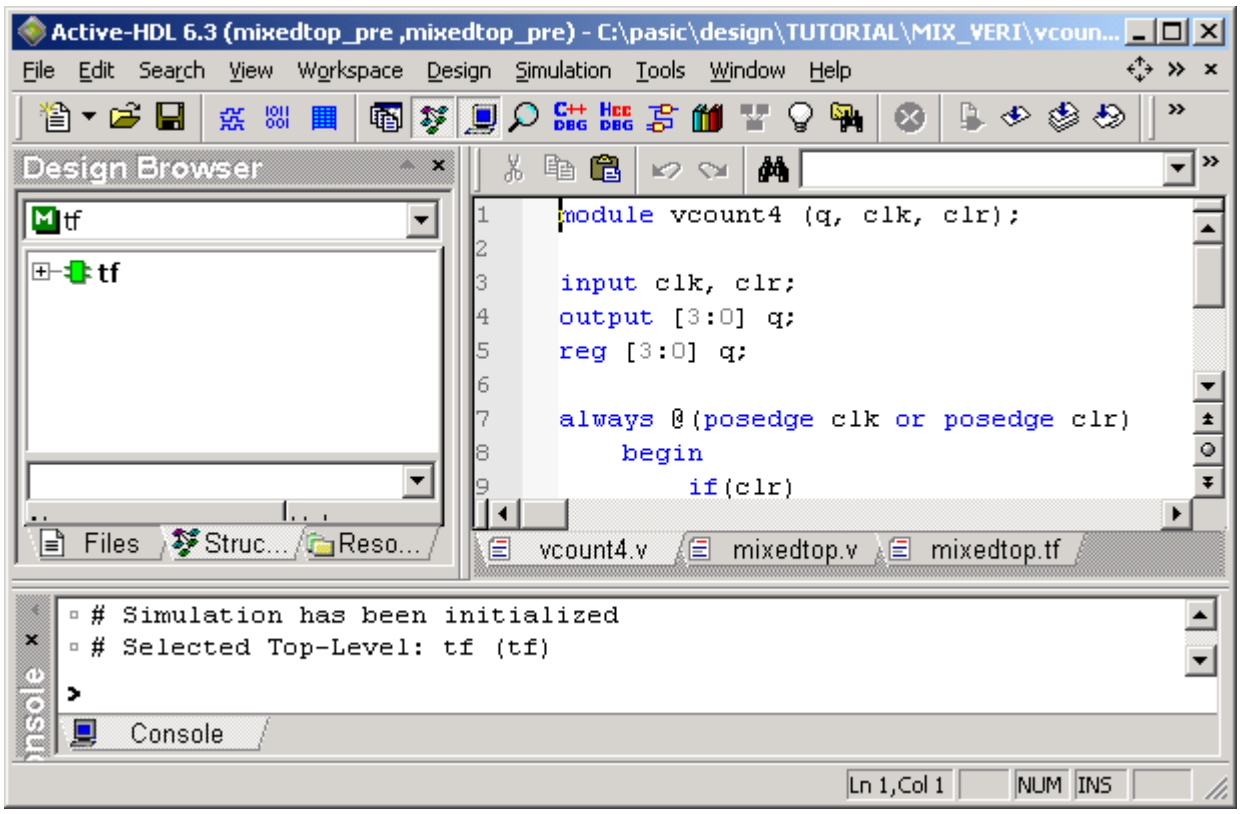
The Add Other Simulation Files screen is displayed.



7. Click to highlight the first line and then click **Browse** to add the file `vcount4.v` located in the default directory `C:\pasic\design\TUTORIAL\MIX_VERI`.
8. Select **verilog** from the Type pull-down menu.
9. Click **OK.**

   The Active HDL Interface screen is displayed.
10. Click **OK**.

The Active HDL simulator creates a new workspace and adds all the simulation files. All files are compiled automatically and the top module is selected.



2.6.3 Running the Pre-Layout Simulation

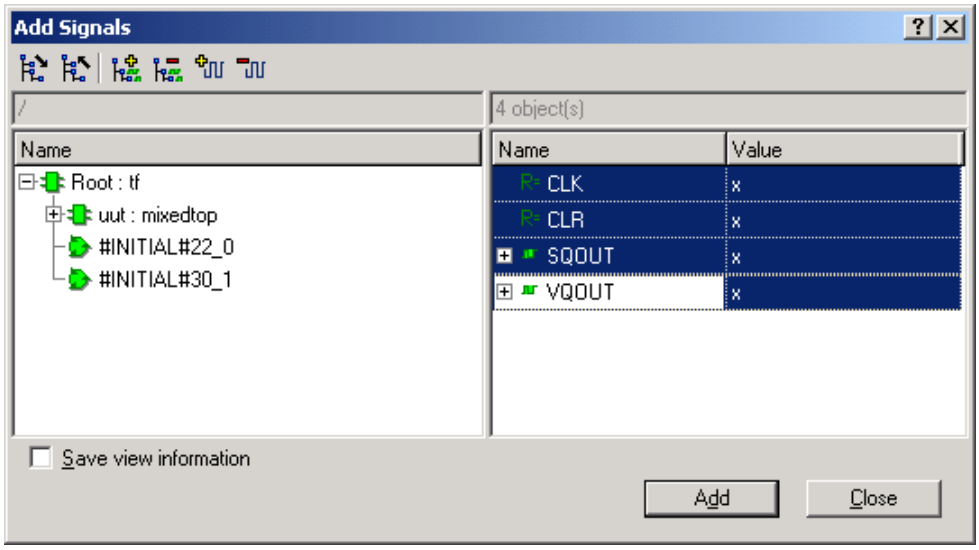
To run the pre-layout simulation:

1. From the Active-HDL toolbar, click on the **New Waveform** icon.

   A new waveform is created.

2. Right-click on the waveform and select **Add Signals**.

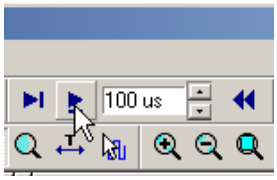
The Add Signals screen is displayed.



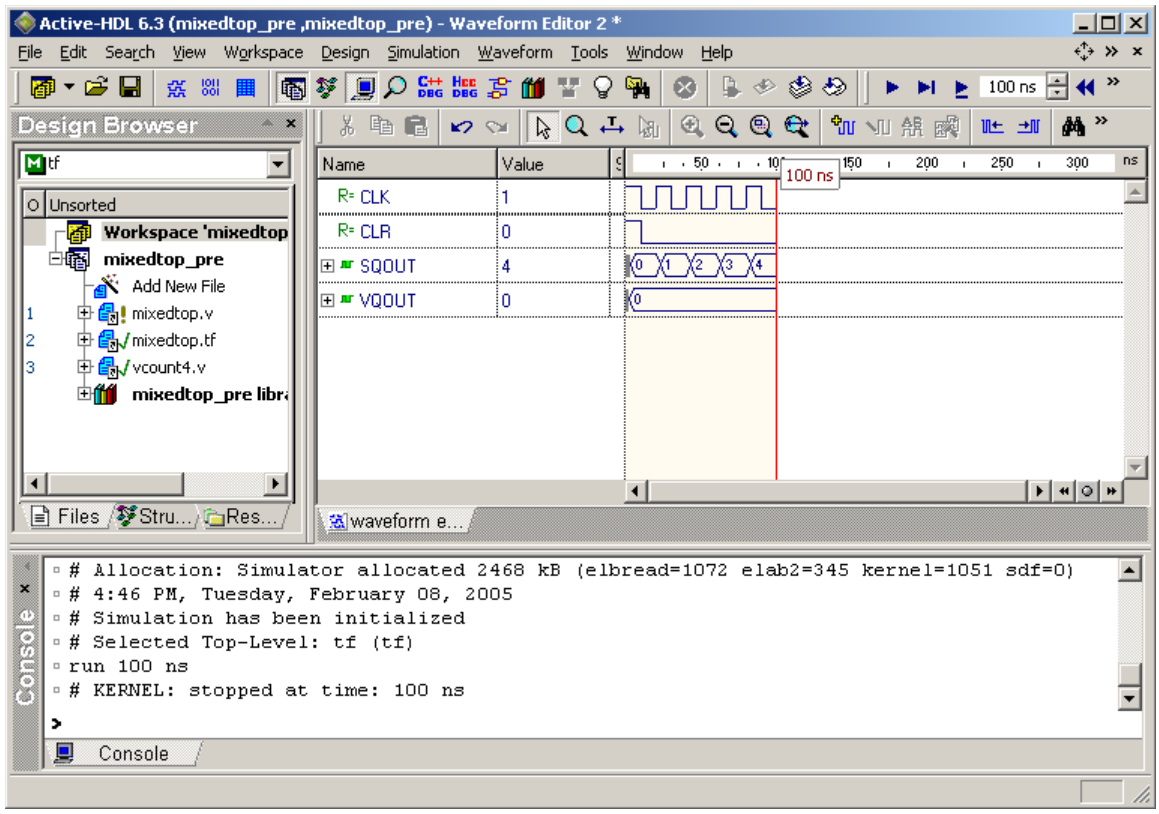
3. Select all signals on the right panel and click **Add** and **Close**.

   The signals are added to the waveform.

4. Expand the screen, in the menu bar type in **`100 us`** and then click the **Run** arrow to the left.



The output of the waveform counters are displayed.



5. After completing the simulation, exit Active-HDL.

2.7 Post-Layout Simulation Using Active-HDL

To perform a post-layout simulation for the design you have just created, you need to synthesize and do back annotation to get the `.vq` and `.sdf` files:

2.7.1 Starting Synthesis

To start the synthesis tool Mentor Graphics Precision RTL:

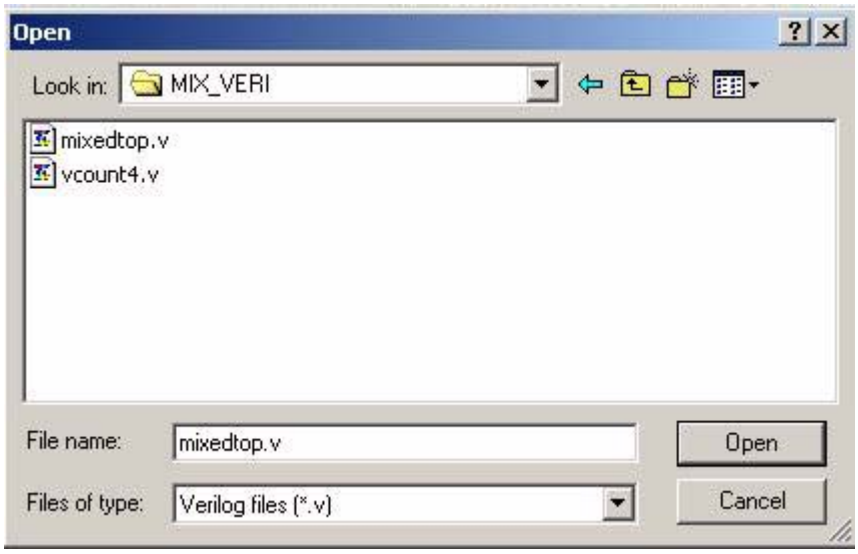
1. From the SpDE menu bar, select **File>Import Using Precision RTL**, or click the **Import Precision** icon.

   The Open window is displayed.

2.7.2 Running a Design in Precision

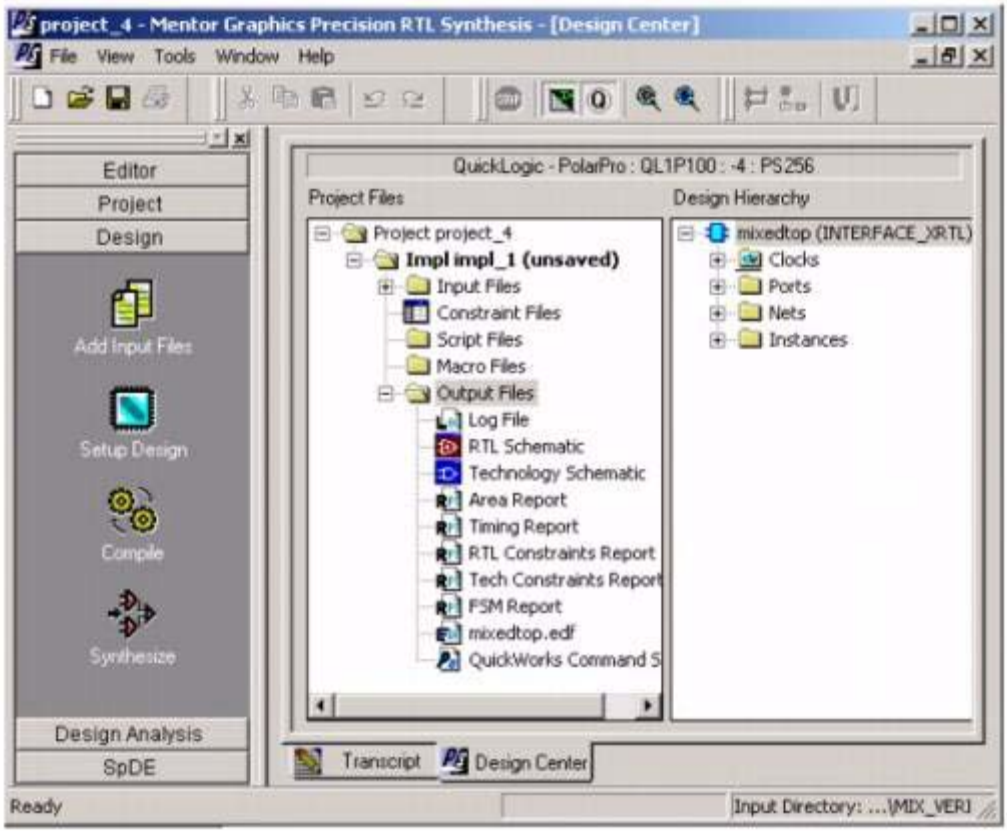
There are two ways to run a design in Precision, the first is as follows:

1. Navigate to the default directory `C:\pasic\design\TUTORIAL\MIX_VERI\.`
2. Select **Verilog files (*.v)** from the Files of type pull-down menu.



3. Select **`mixedtop.v`** and click **Open**.

The Precision RTL Synthesis screen is displayed and automatically a `.tcl` script is generated to create a project file.



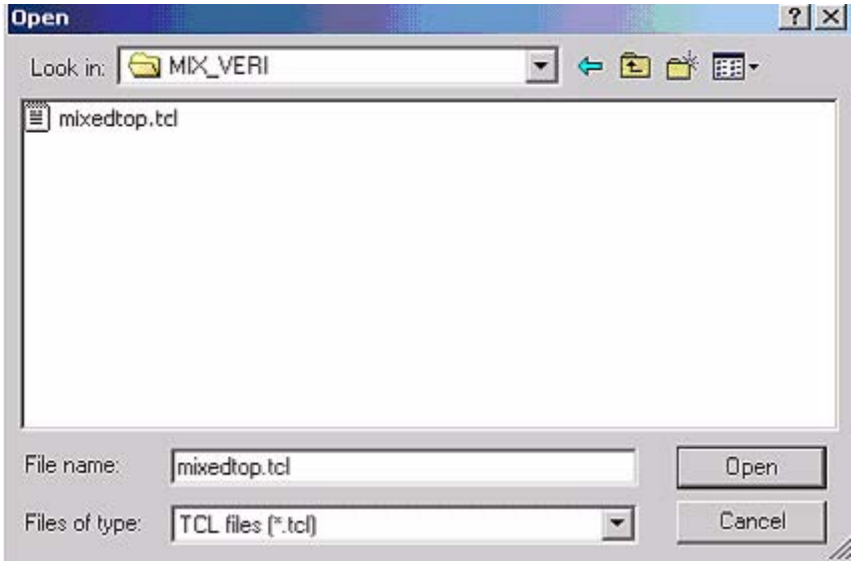
4. Select the **Design** tab on the left side of the Precision RTL Window.
5. Click **Add Input files** to add the Verilog file.
6. Click **Setup Design**.
   a. Select the desired **product family** from the Technology menu.
   b. Select the **device** from the Package menu.
   c. Select the device **Speed grade** from Speed menu
4. Click **Compile** to compile the Verilog design files.
5. Click **Synthesize** to complete the design synthesis.

   If there are errors, view the transcript window.
6. Select **File>Exit** to quit Precision RTL and load the generated EDIF file using the **SpDE** tab.

The following is an alternate method of running a design in Precision:

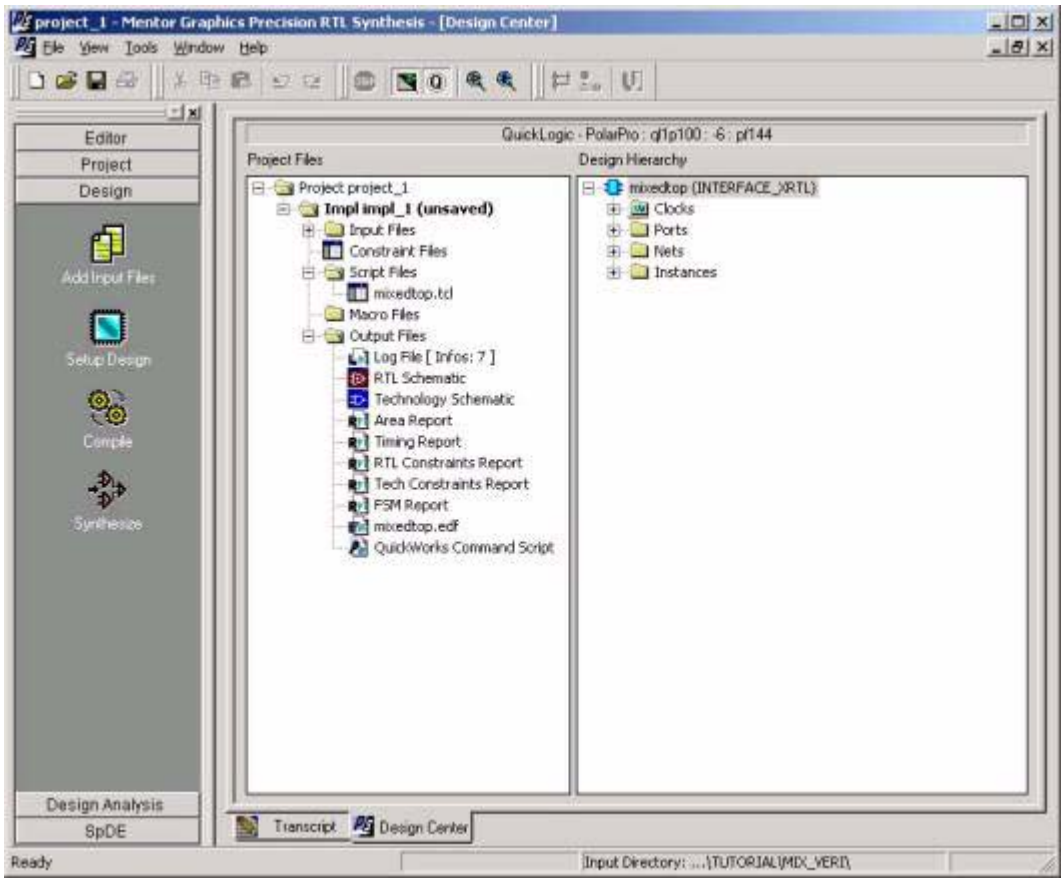
1. Navigate to the default directory `C:\pasic\design\TUTORIAL\MIX_VERI\.`

   Select **TCL files (*.tcl)** from the Files of type pull-down menu.



2. Select **`mixedtop.tcl`** and click **Open**.

   The Precision RTL program is displayed and automatically generates the EDIF.



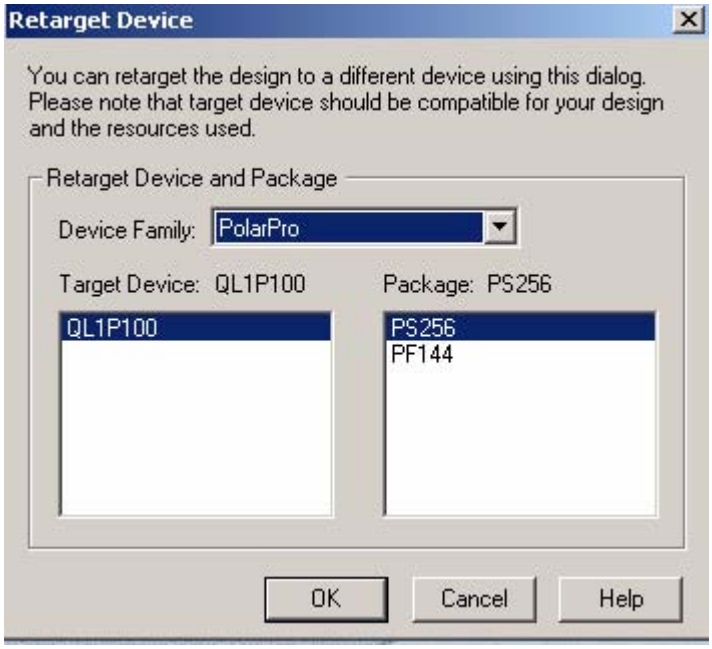
2.7.3 Running a Design in SpDE

If the EDIF netlist is generated by loading HDL in Precision RTL, follow this step to load the design:

1. From the SpDE menu bar, select **Tools -> Run TCL Script...** (*.tcl generated by Precision RTL).

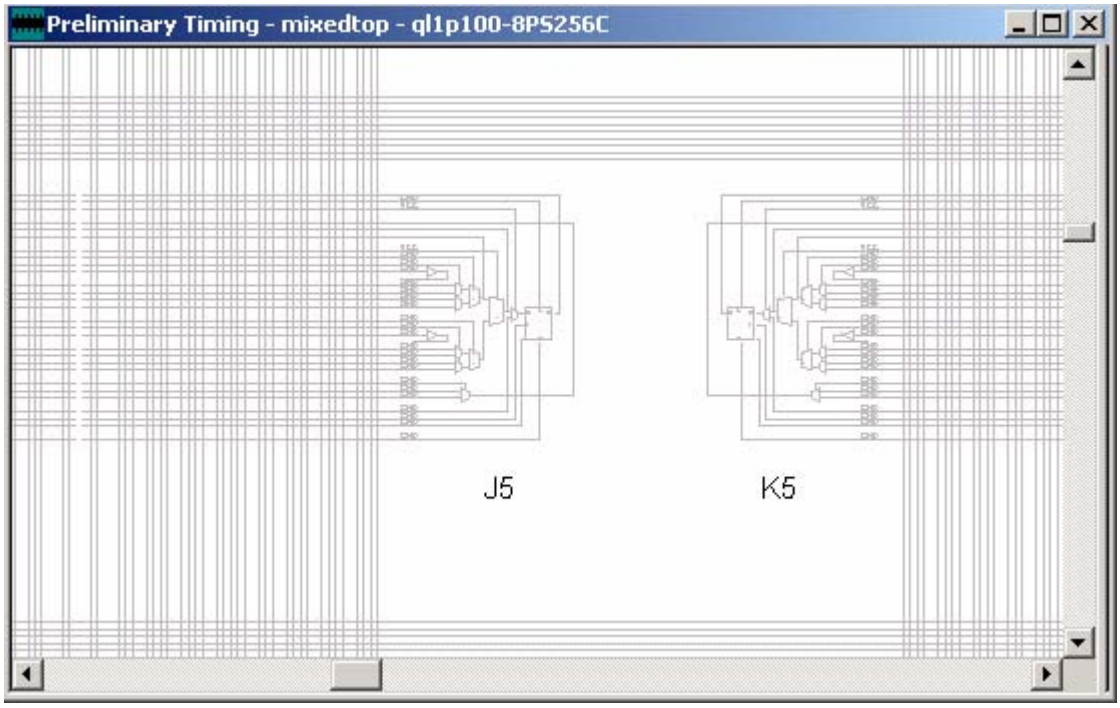
   This automatically runs all the tools and generates the `.chp` file.

   If the EDIF netlist is generated by running `.tcl` (generated by the schematic editor), the EDIF netlist is automatically loaded into SpDE after exiting from the synthesis tool. The Retarget Device screen is displayed.



2. Select the Device Family, Target Device, and Package and click **OK**.

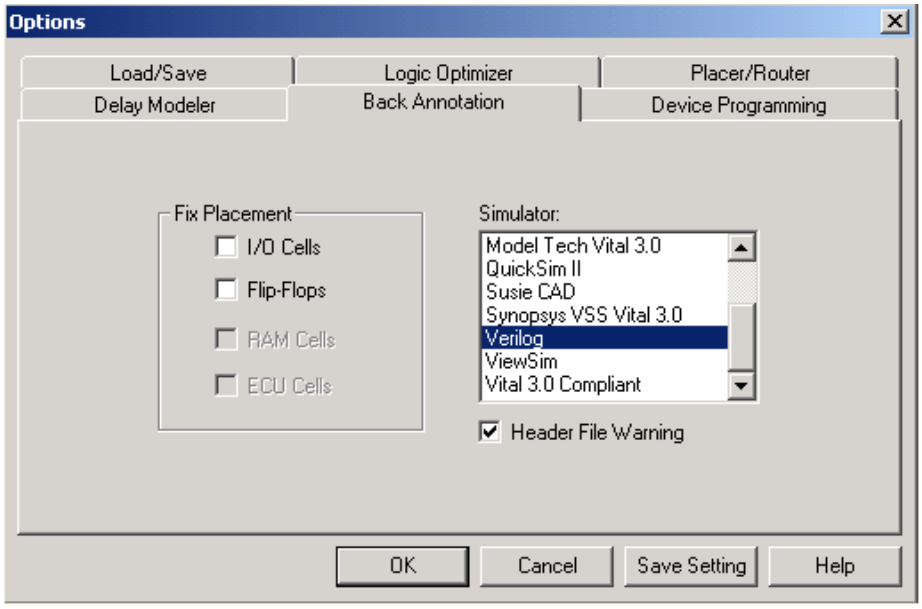
The Preliminary Timing screen is displayed.



2.7.4 Setting Options for Back Annotation

To set options for back annotation:

1. From the SpDE menu bar, select **Tools>Options.**
2. In the Tools Options dialog box, click on the **Back Annotation** tab. Select **Verilog** in the Simulator window. Click **Save Setting** and then **OK**.

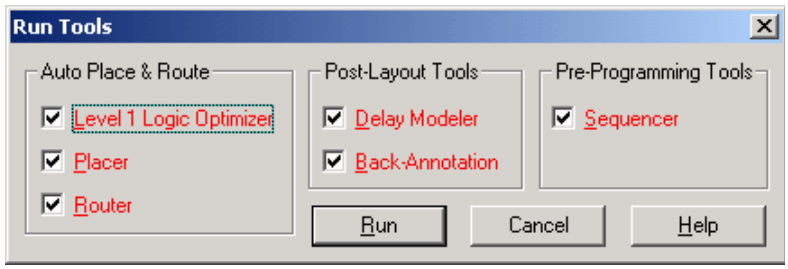


2.7.5 Selecting and Running Tools

To select and run tools:

1. From the SpDE menu bar, select **Tools>Run Selected Tools,** or click the  icon.

   The Run Tools window is displayed.



2. Click **Run**.
3. Verify the creation of the `mixedtop.vq` and `mixedtop.sdf` files in the default directory `C:\pasic\design\TUTORIAL\MIX_VERI`.

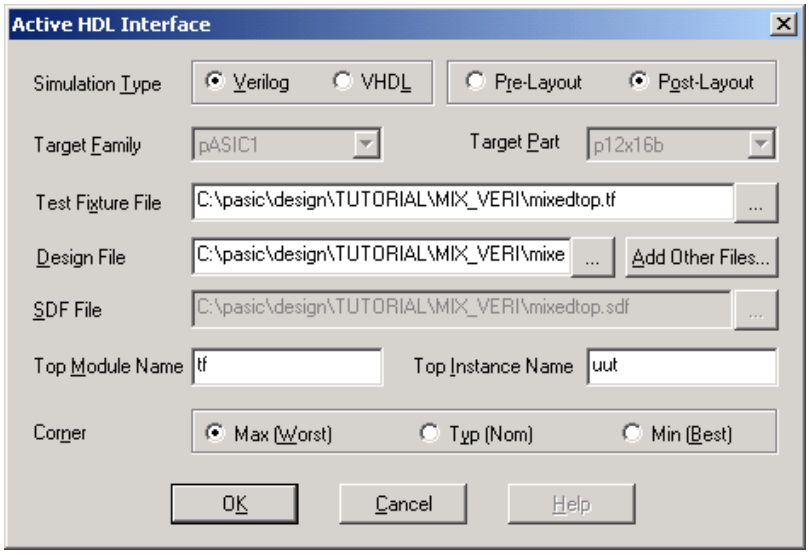
2.7.6 Using Active-HDL Design for Post-Layout Simulation

The timing (post-layout) simulation is similar to the functional simulation, which you did earlier in this tutorial.

NOTE: Before performing the post-layout simulation, be sure that you have exited from the pre-layout simulation and closed Active-HDL. Otherwise, the program will not function properly.

1. From the SpDE toolbar, click on the **Active-HDL Simulator**  icon.

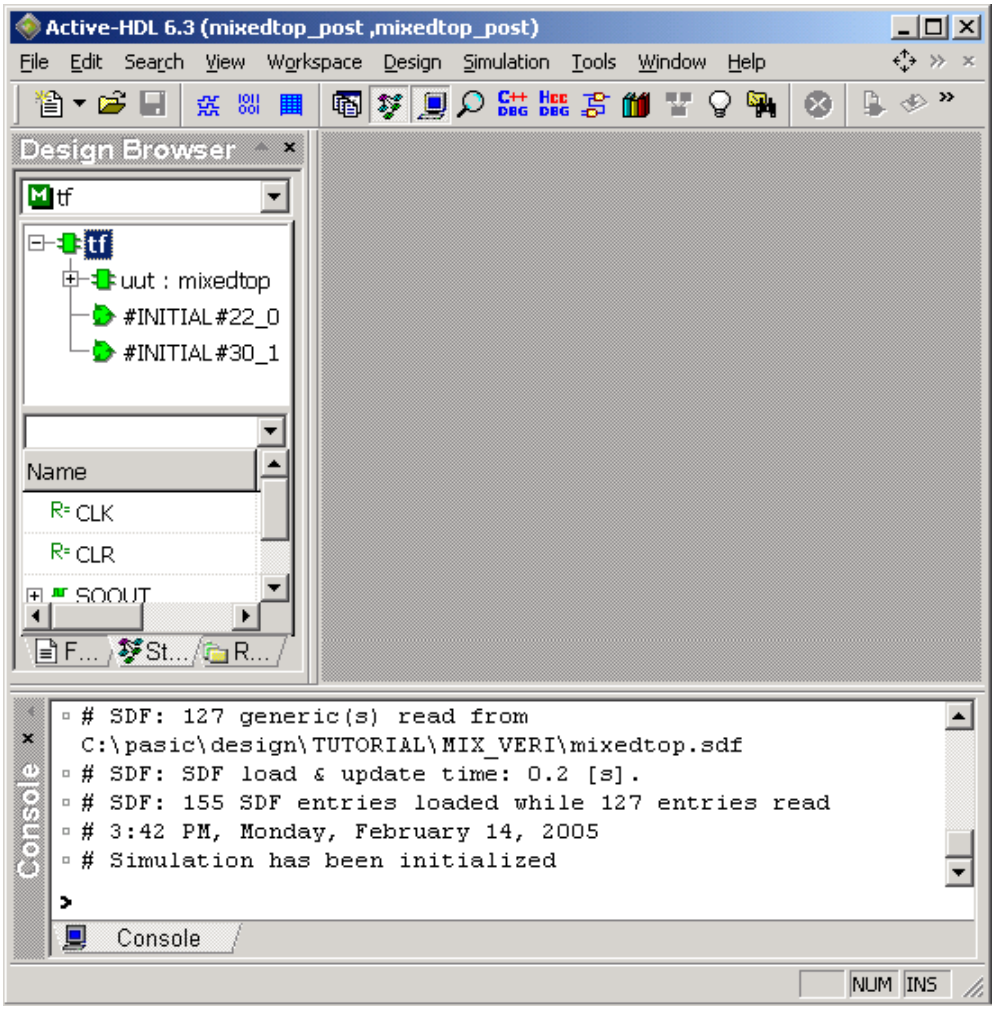
   The Active-HDL Interface screen is displayed with most of the information included.



2. Type **tf** for the Top Module Name and **uut** for the Top Instance Name.

3. Click **OK**.

   The Active HDL simulator creates a new workspace and adds all the simulation files. All files are compiled automatically and the top module is selected.



2.7.7 Running the Post-Layout Simulation

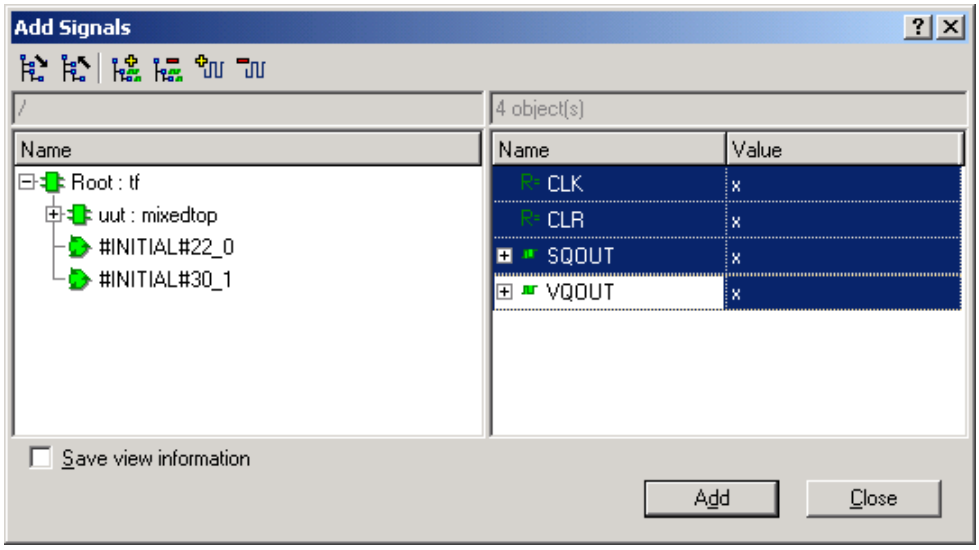
To run the post-layout simulation:

1. From the Active-HDL toolbar, click on the **New Waveform** icon.

   A new waveform is created.

2. Right-click on the waveform and select **Add Signals**.

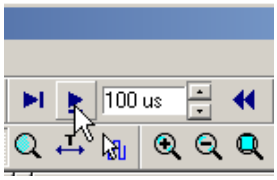
The Add Signals screen is displayed.



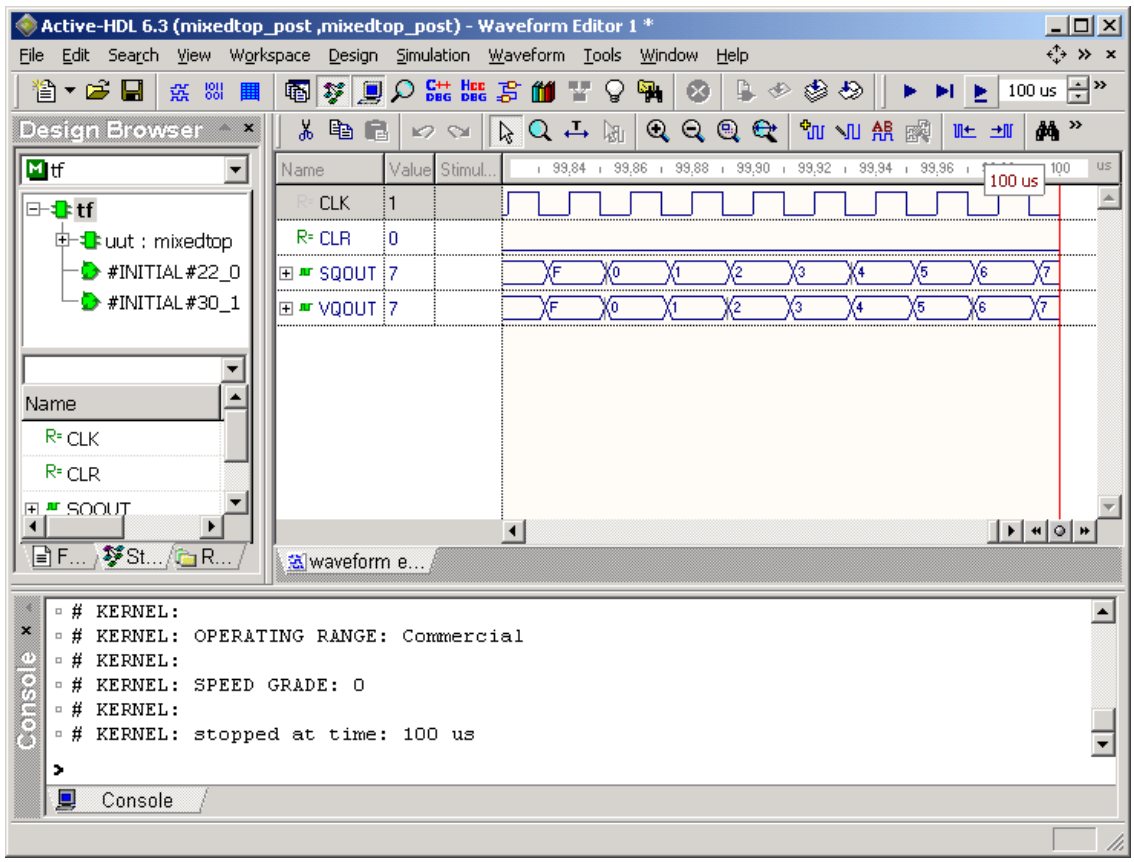
3. Select all signals on the right panel and click **Add** and **Close**.

   The signals are added to the waveform.

4. Expand the screen, in the menu bar type in **`100 us`** and then click the **Run** arrow to the left.



The output waveform should look as follows.



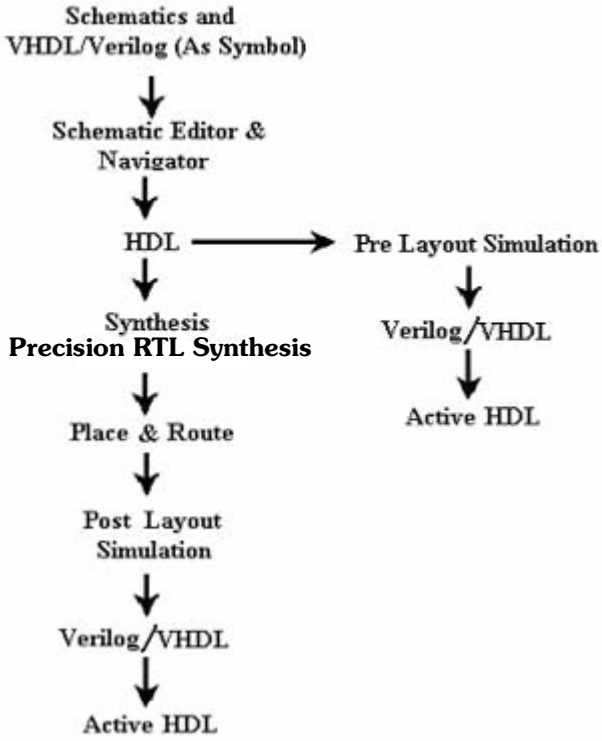
Chapter 3
Mixed Schematic/VHDL Design

This tutorial describes the QuickWorks Mixed Schematic/VHDL design using Schematic Editor. It contains the following sections:

NOTE: The tutorial assumes that you have a working knowledge of Microsoft Windows. The *Microsoft Windows User's Guide* contains a great deal of useful information for those new to Windows.

3.1 Functional Overview

Figure 3-1: Mixed-Mode Design Flow with VHDL



For reference on design entry and tools, refer to the following documents:

- *Design Flows and Reference* section of the *QuickWorks User Manual*, and the *SCS Schematic Entry User's Manual* for tips on using SCS Design Entry.
- *Precision RTL User's Guide* for information on Precision RTL Synthesis.

In this tutorial you will create a top-level schematic containing two 4-bit counters. One of the counters will be created using schematics, and the other using VHDL. You will enter the schematics using the Schematic Editor, and the VHDL code with the use of any HDL text editor. The complete design will be inspected using the Hierarchy Navigator, and a VHDL netlist will be generated. The netlist will be synthesized with Precision RTL, and a post-synthesis/pre-layout Verilog and VHDL netlists will be generated. After the simulation outputs have been inspected and proper functionality verified, the design will be optimized, placed, and routed. The Delay Modeler will generate precise post-layout delays, which will be back-annotated for simulation. Post-layout simulation will be run, this time producing accurate-timing results.

Figure 3-2: Top Level Design

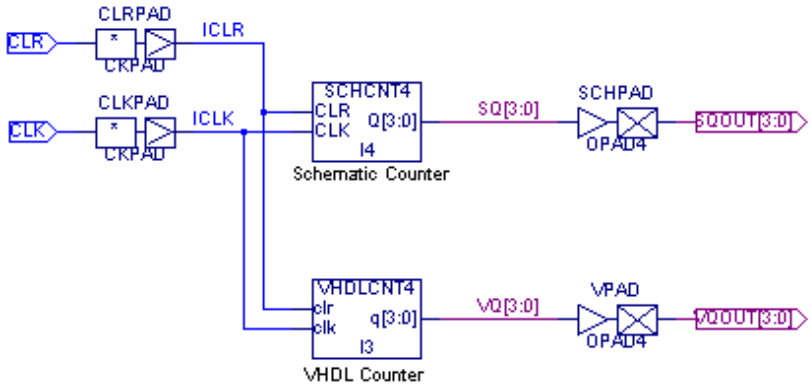
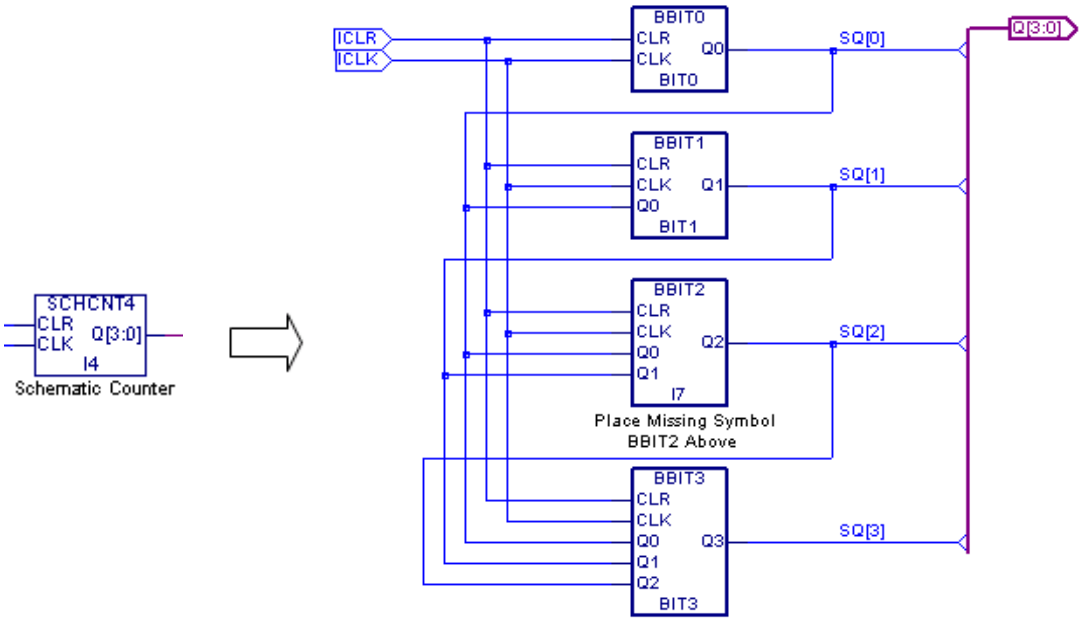


Figure 3-3: Push-Down View of SCHCNT4



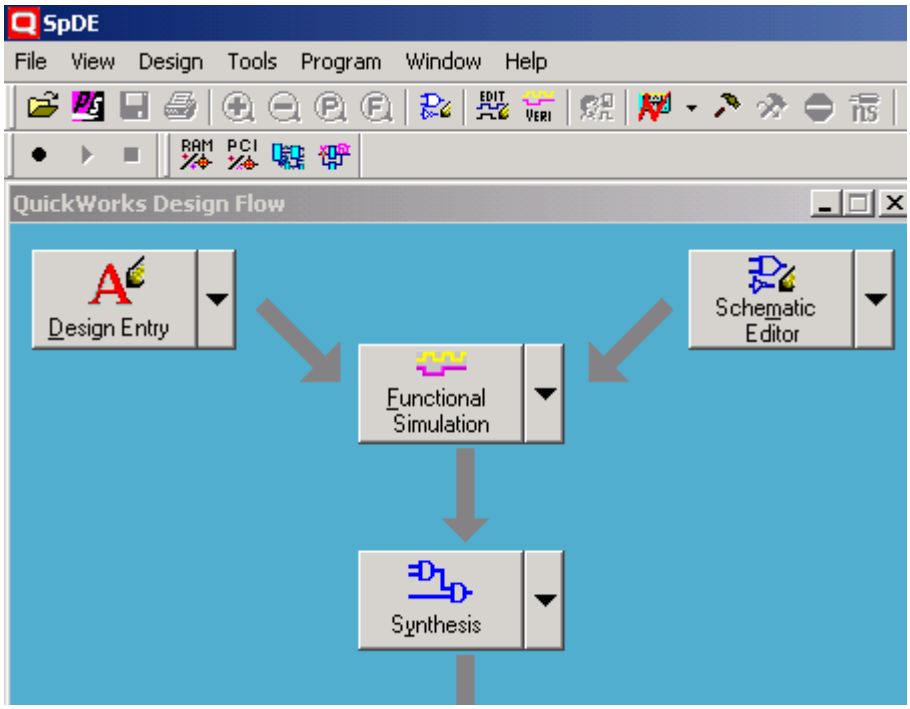
3.2 Creating a Schematic Design

3.2.1 Entering a Schematic Design

To create a mixed schematic VHDL design:

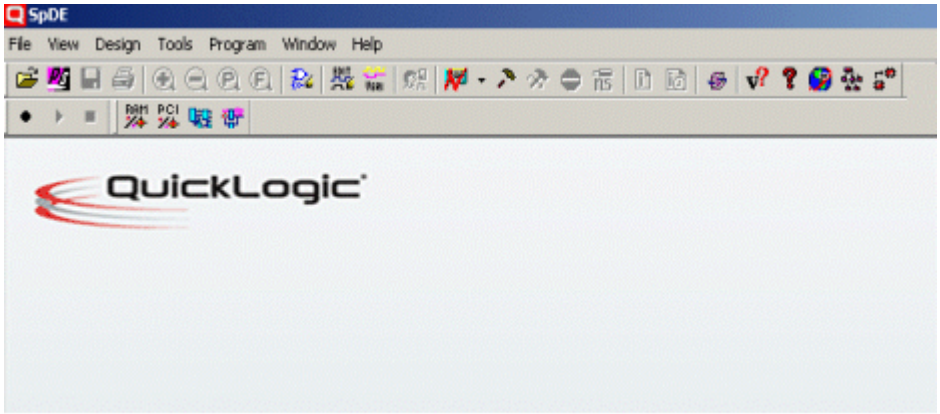
1. Select **Start>Programs>QuickLogic>SpDE**, or click the **SpDE** icon on your desktop.

The SpDE window is displayed and all of the QuickWorks design resources are now available for use.



2. Close the QuickWorks Design Flow window by clicking the **X** in the upper right corner. This method of design will not be used for this tutorial.

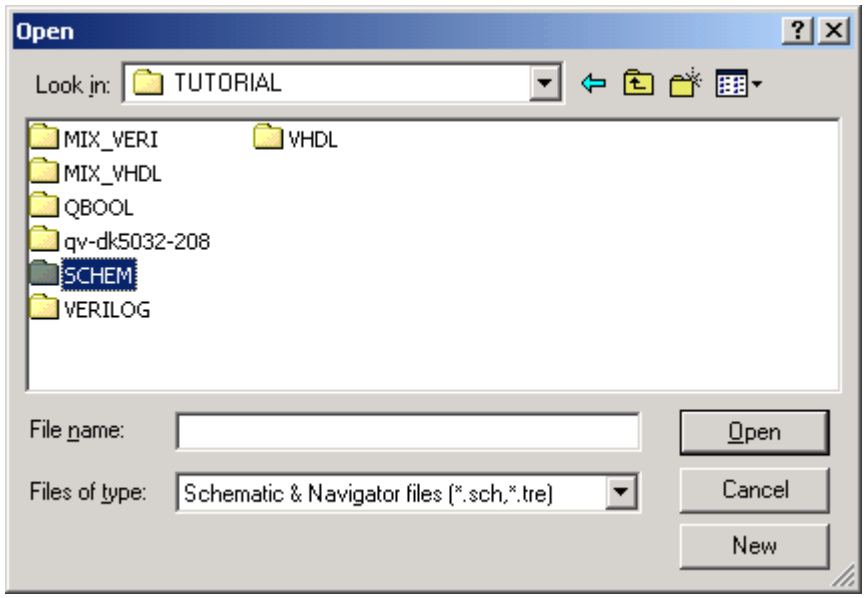
   The SpDE window is displayed. The SpDE toolbar contains icon buttons for executing commands quickly. The status bar at the bottom of the SpDE window displays status messages periodically.



NOTE: See the SpDE Menu Command Reference chapter of the *QuickWorks User Manual* for a full explanation of all available icons.

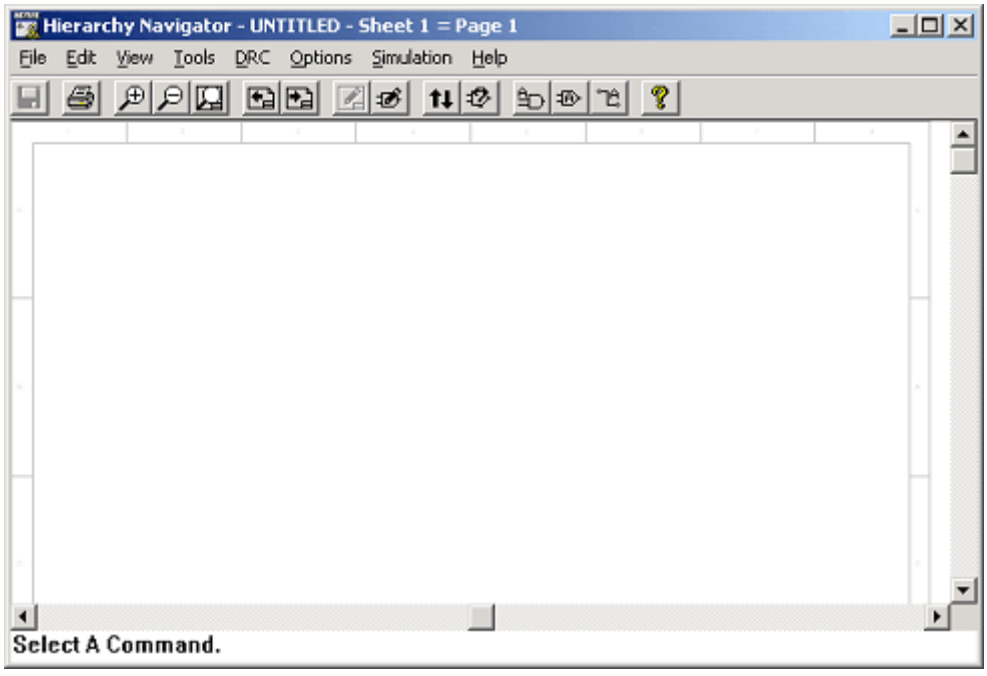
3. From the SpDE menu bar, select **Design>Schematic Editor & Navigator**, or click the  icon.

The Open window is displayed.



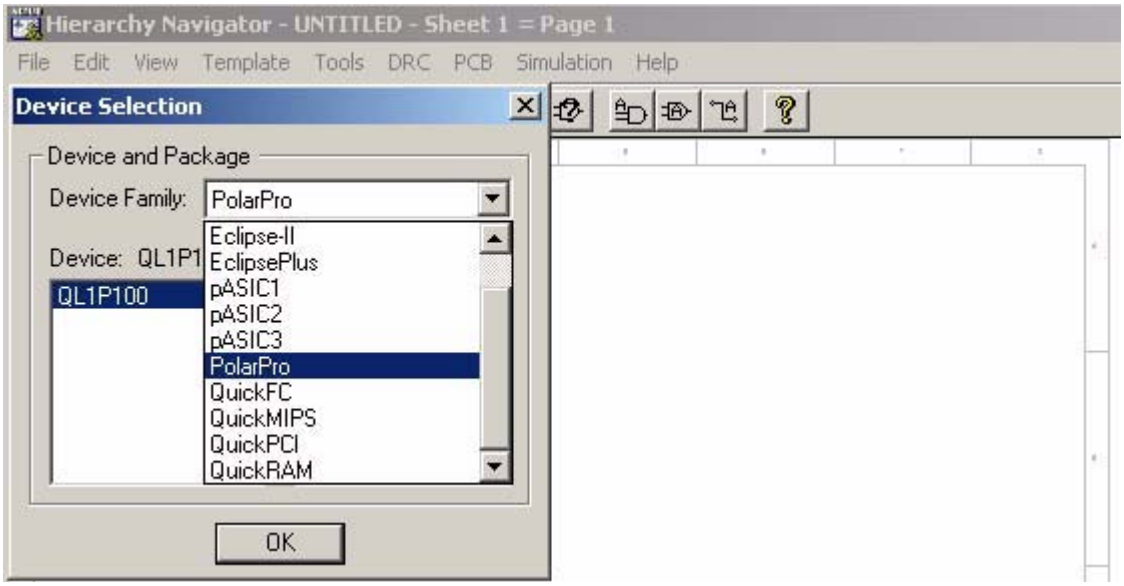
4. Navigate to the default directory `C:\pasic\design\TUTORIAL\SCHEM\.`
5. Click **New**.

   The Hierarchy Navigator window is displayed.



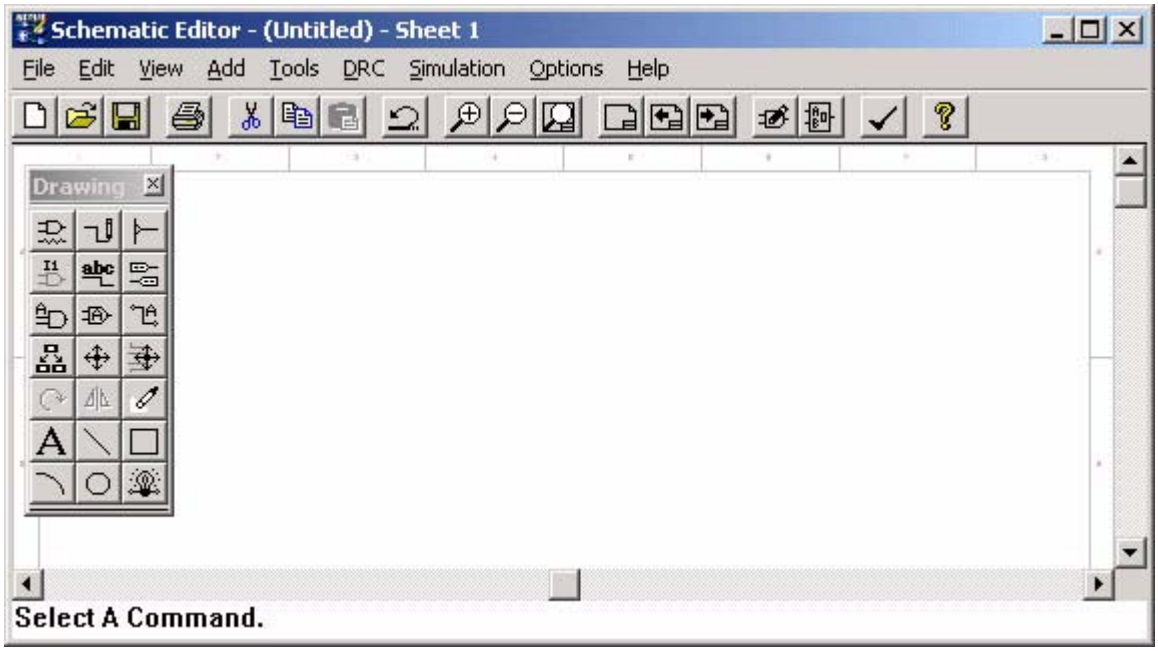
6. From the Hierarchy Navigator menu bar, select **File>Create Schematic**.

The Device Selection window is displayed.



7. Select **PolarPro** for the Device Family, **QL1P100** for the Device, and **PF144** for the Package.
8. Click **OK**.

   The Schematic Editor is displayed.



You will create the schematic. But first, you must create the lower level as described in the following.

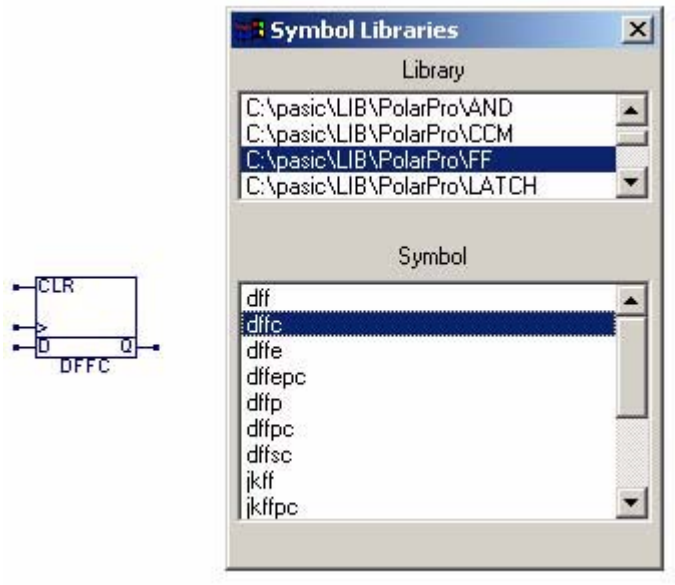
3.2.1.1 Adding Symbols

To add symbols to the schematic design:

1. From the Schematic Editor menu bar, select **Add>Symbol.**

   The Symbol Libraries window is displayed.

2. In the **`C:\pasic\LIB\PolarPro\FF`** library, select the **DFFC** symbol and drag it onto the workspace. Left-click to place it on the workspace and left-click to release your selection.



3. Continue to add symbols until the schematic looks like the following schematic.

   See “Adding Symbols” on page 6 for more detailed information.

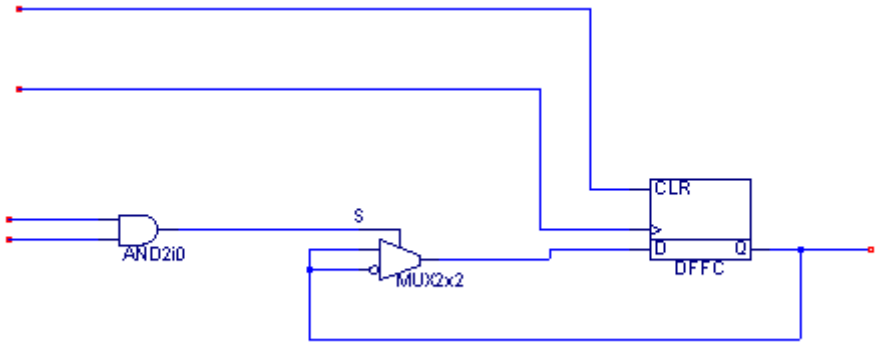
3.2.1.2 Connecting the Symbols

To add wires to connect the symbols:

1. From the Schematic Editor menu bar, select **Add>Wire**.

   The status bar line reads: `Wire - Click or Drag to Begin Wire`.

2. Add wires until your schematic looks like the following arrangement.



NOTE: To delete wires, select **Edit>Delete** and click on the wire to be deleted.

3.2.1.3 Adding Net Names

To define the net names.

1. From the Schematic Editor menu bar, select **Add>Net Name**.

   The status bar line reads: `Net Name - Enter Net Name =`.

2. Type: **`CLK`**.

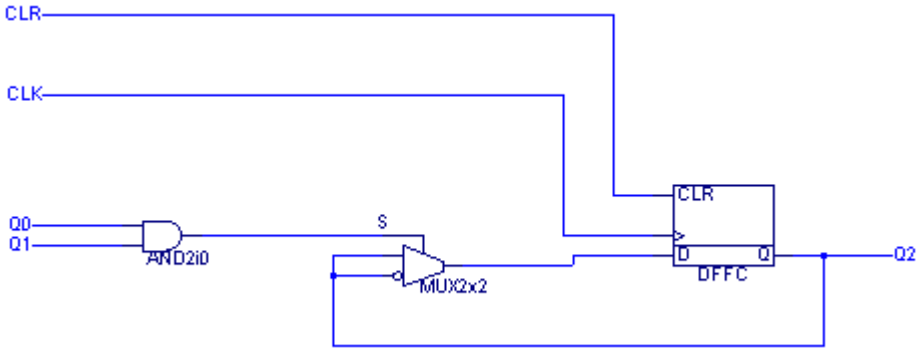
3. Press **Enter** on the keyboard.

   The status bar line reads: `Net Name - Place Net Name Flag 'CLK' - Shift Key to Rename`.

4. Position the crosshairs of the cursor on the end of the clock wire created above and click.

   This places the CLK flag at the end of the selected wire.

5. Add the net names, **`CLR, Q0, Q1,`** and **`Q2`** as shown in the following arrangement.



3.2.1.4 Defining Ports

The primary inputs and outputs of the schematic must now be marked with I/O markers.

1. From the Schematic Editor menu bar, select **Add>I/O Marker**.

   The status bar line reads: `Select Net Name Flag on End of Wire`. The I/O Markers window appears.

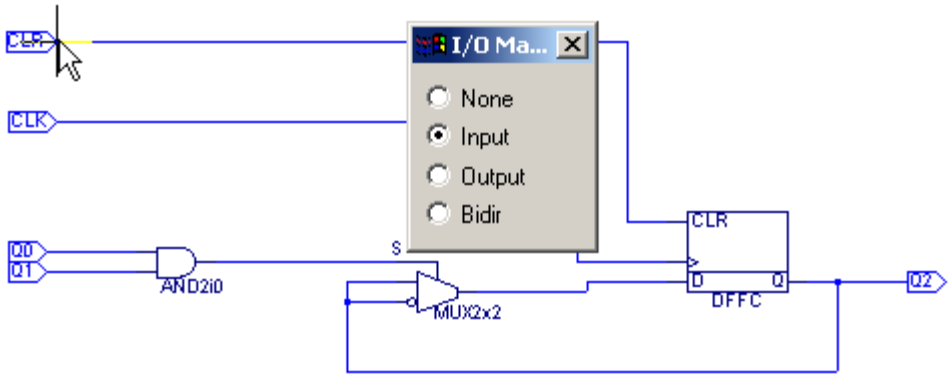
3.2.1.4.1 Adding an Input Marker

To add an input marker:

1. Click the **Input** option in the I/O Markers window.
2. Position the crosshairs of the cursor at the end of the clock wire and click.

   This places an input marker on the CLK flag.

   NOTE: To create an I/O marker, the net name flag must be placed at the end of its wire (as opposed to along the length of its wire), as shown in the figures above.
3. Repeat this operation for the CLR, Q0,and Q1 flags. All three input markers can be added in one operation by dragging a rectangle around the three net names.



3.2.1.4.2 Adding an Output Marker

To add an output marker:

1. Click the **Output** option in the I/O Markers window.
2. Position the crosshairs of the cursor at the end of the output wire on the Q2 flag, and click to create the output marker.

3.2.1.5 Saving the Schematic

To save the schematic:

1. From the Schematic Editor menu bar, select **File>Save As**.

   A dialog box prompts you for the name of the file.
2. Browse to `C:\pasic\design\TUTORIAL\MIX_VHDL` and type: **`BBIT2.sch`**.
3. Click **Save**.

3.2.1.6 Creating a Symbol

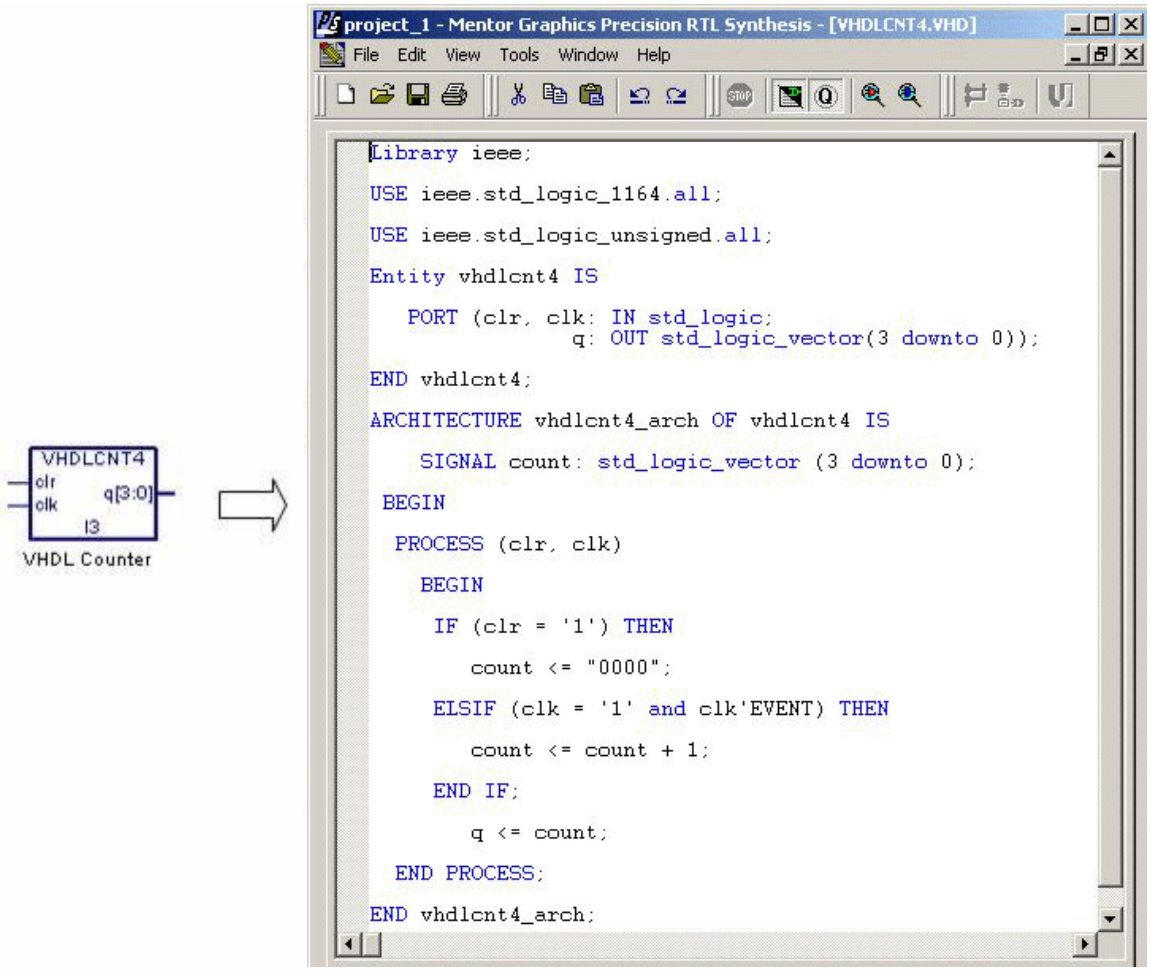
To make a matching symbol for this schematic:

1. From the Schematic Editor menu bar, select **File>Matching Symbol.**

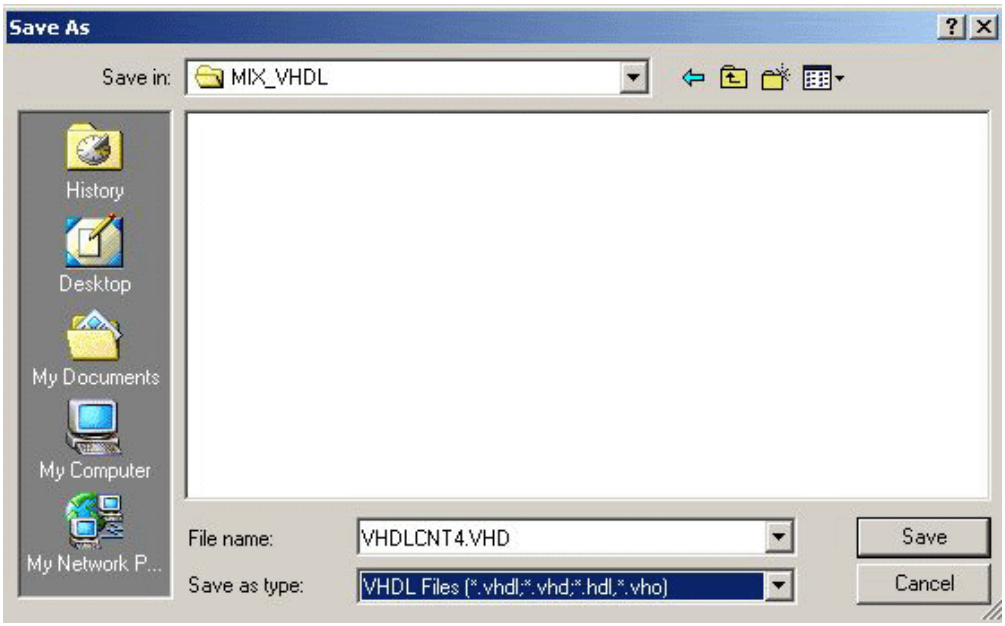
   You now have a symbol for this schematic to also use in other schematics.

3.3 Creating a VHDL Counter

You will now create a VHDL counter as shown. You will combine this counter with the top level design.



After finishing the design, save the file as `VHDLCNT4.VHD` in the `MIX_VHDL` folder.



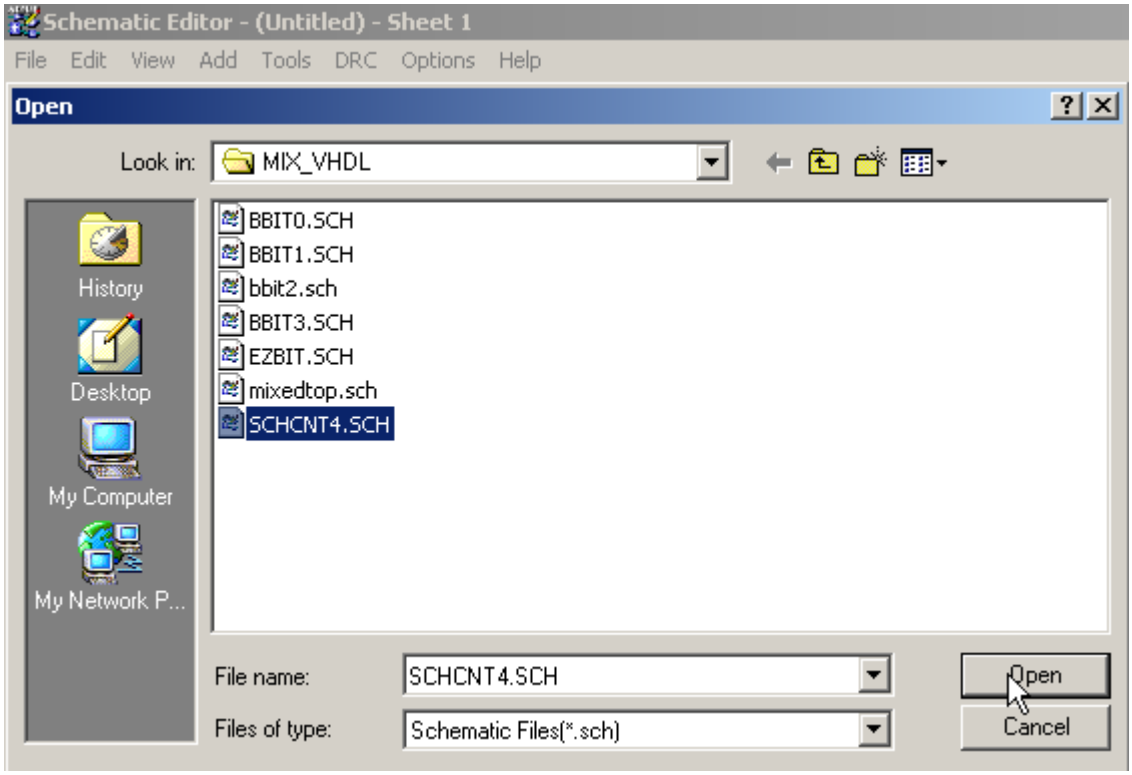
Next, you will combine the schematic and `.vhdl` counter to form the top level design.

3.4 Creating the Top Level Design

3.4.1 Opening a Schematic

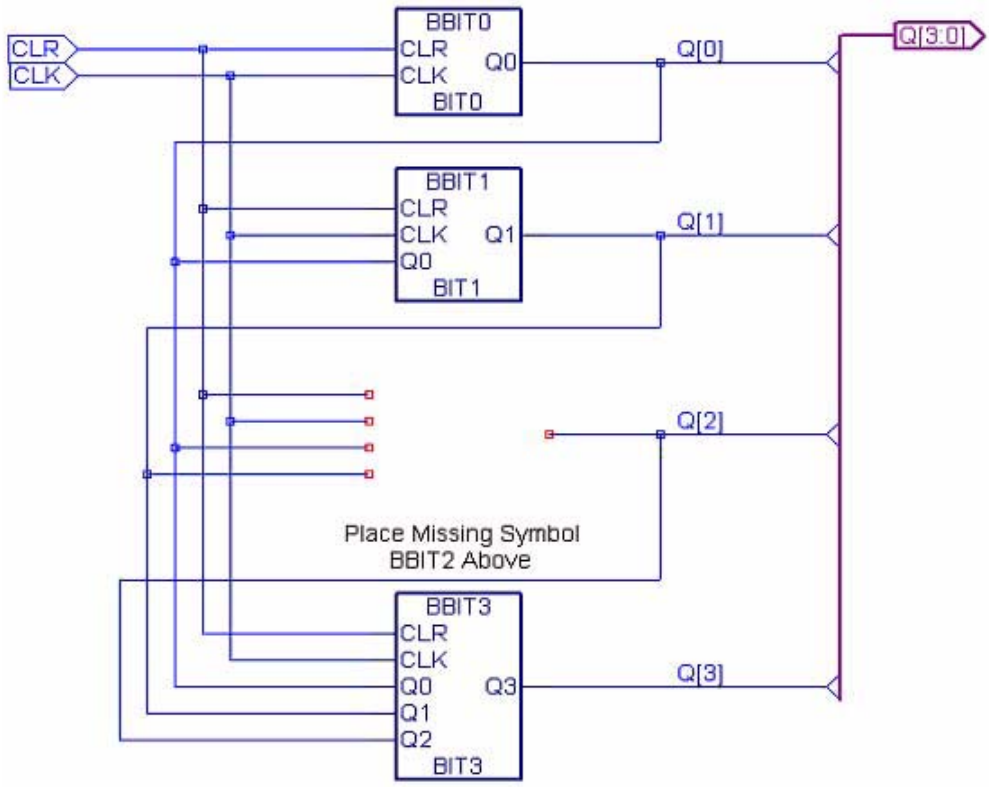
1. From the SpDE menu bar, select **Design>Schematic Editor & Navigator**, or click the  icon.

The Open window is displayed.



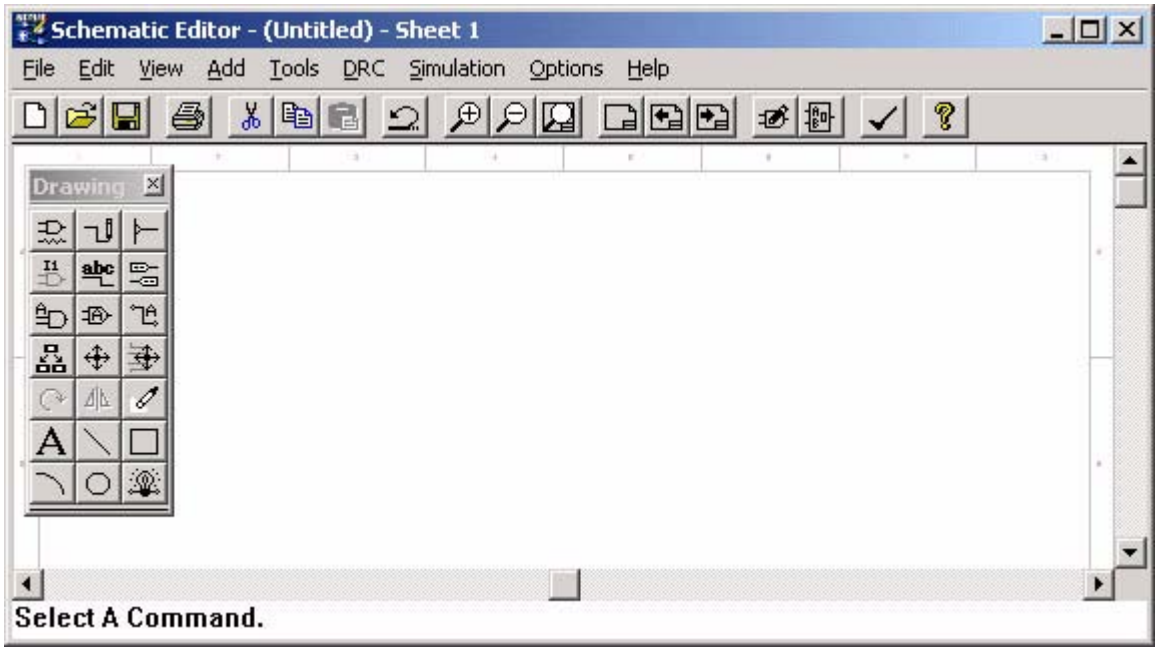
2. Browse to the default directory `C:\pasic\design\TUTORIAL\MIX_VHDL\.`
3. Select `SCHCNT4.SCH` and click **Open**.

The Hierarchy Navigator window is displayed.

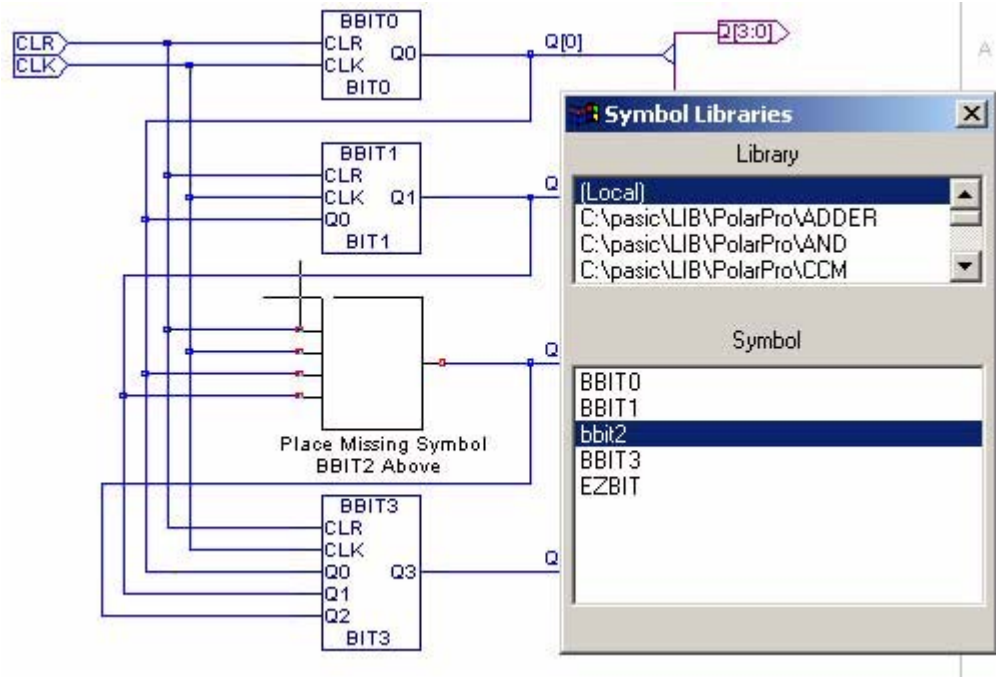


4. From the Hierarchy Navigator menu bar, select **File>Edit Schematic**.

The Schematic Editor is displayed.

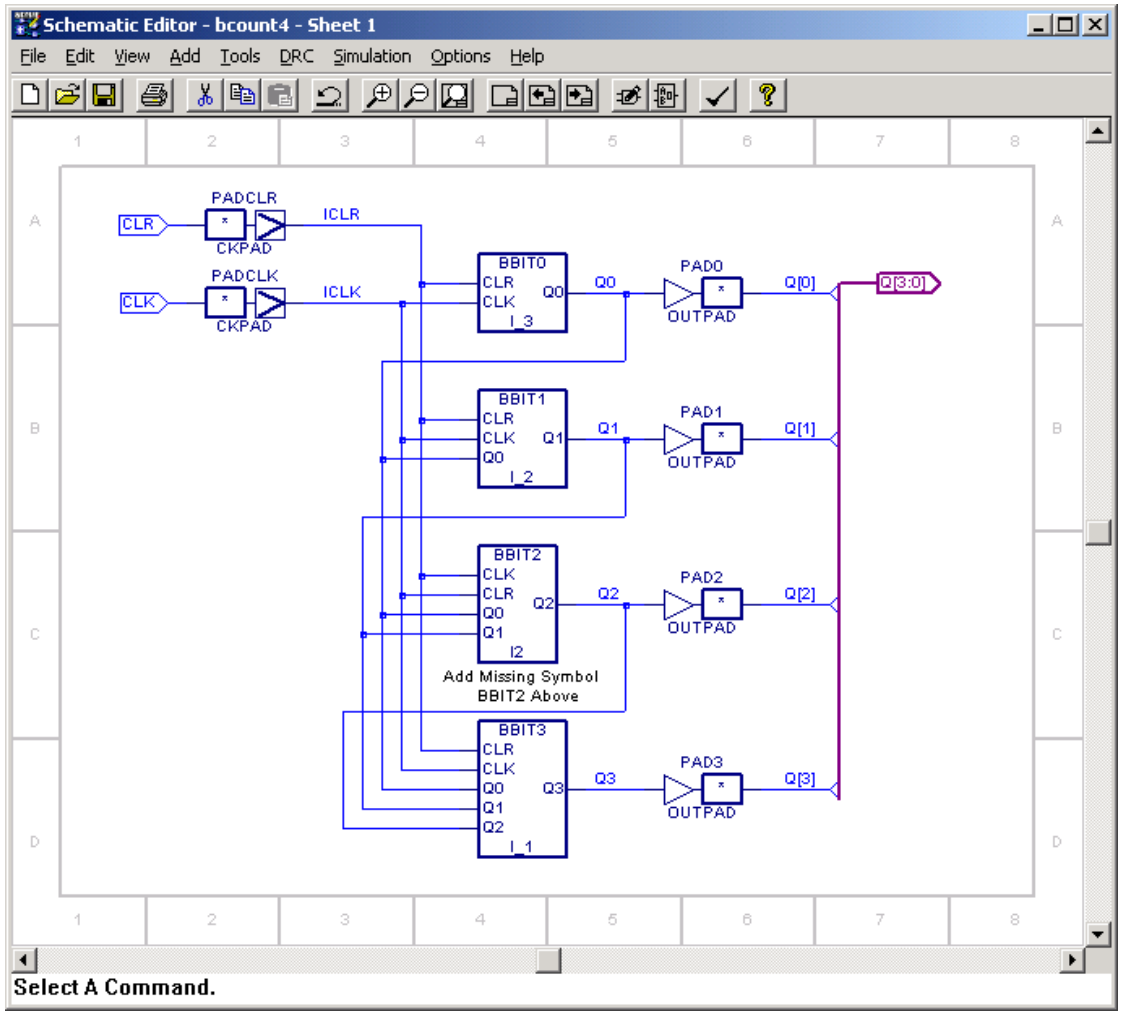


5. From the Schematic Editor menu bar, select **Add>Symbol** and select the **bbit2** symbol that you created earlier. Drag it to the location shown below. Left-click to place the symbol.



6. Select **File>Matching Symbol** to create a matching symbol.
7. Select **File>Open** and double-click on `MIXEDTOP.SCH`.

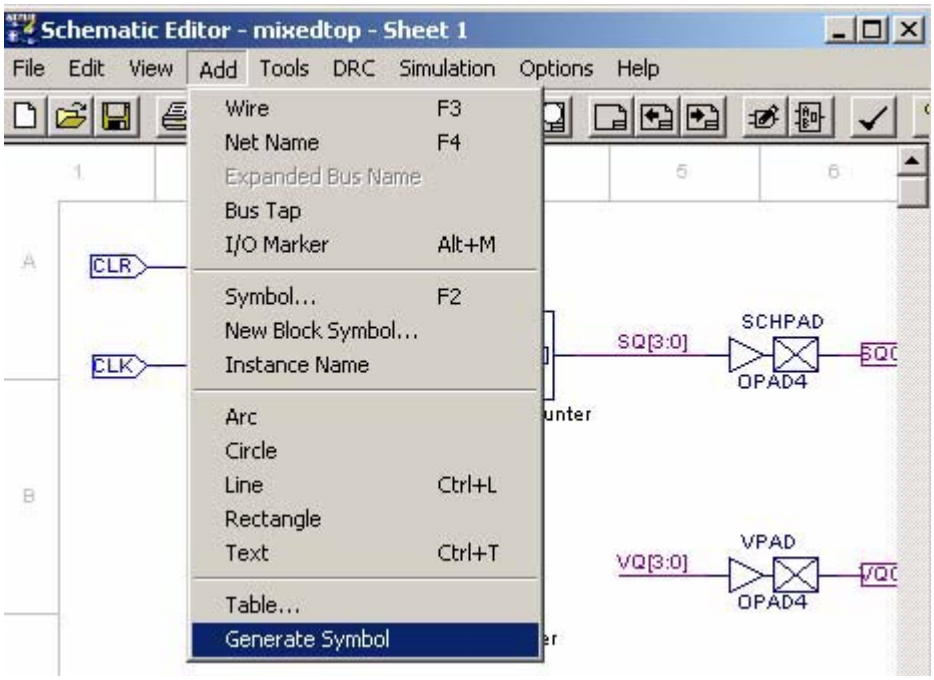
8. Select **Add>Symbol** and add the **schcnt4** symbol from the Local Library.



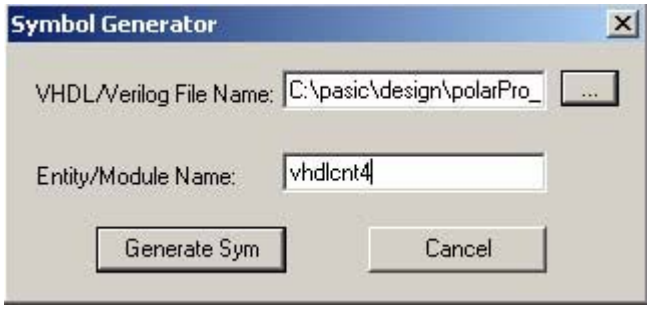
3.4.2 Adding a New Block Symbol

In this section you will create a symbol for the VHDL counter and add it to `MIXEDTOP.SCH`.

1. From the Schematic Editor menu bar, select **Add>Generate Symbol**.

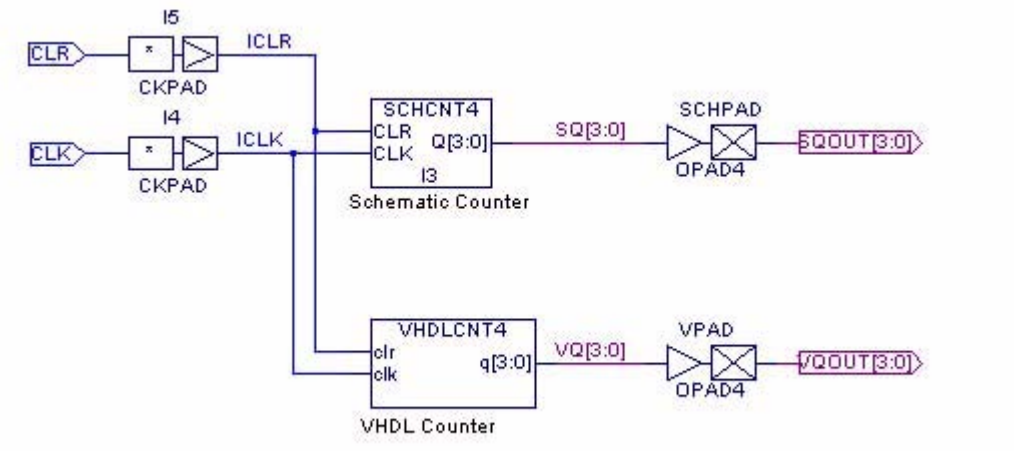


2. To create a symbol for the VHDL counter, type exactly as shown in the following dialog box.



3. Click **Generate Sym**.

4. When **Add Symbol** appears, drag and drop the symbol as shown.



5. Select **File>Save** to save the file.

3.5 Exporting the Schematic to VHDL

In this section you will export the schematic you have created to VHDL code. Then, you will use the code to do pre- and post-layout simulation.

3.5.1 Opening the Schematic

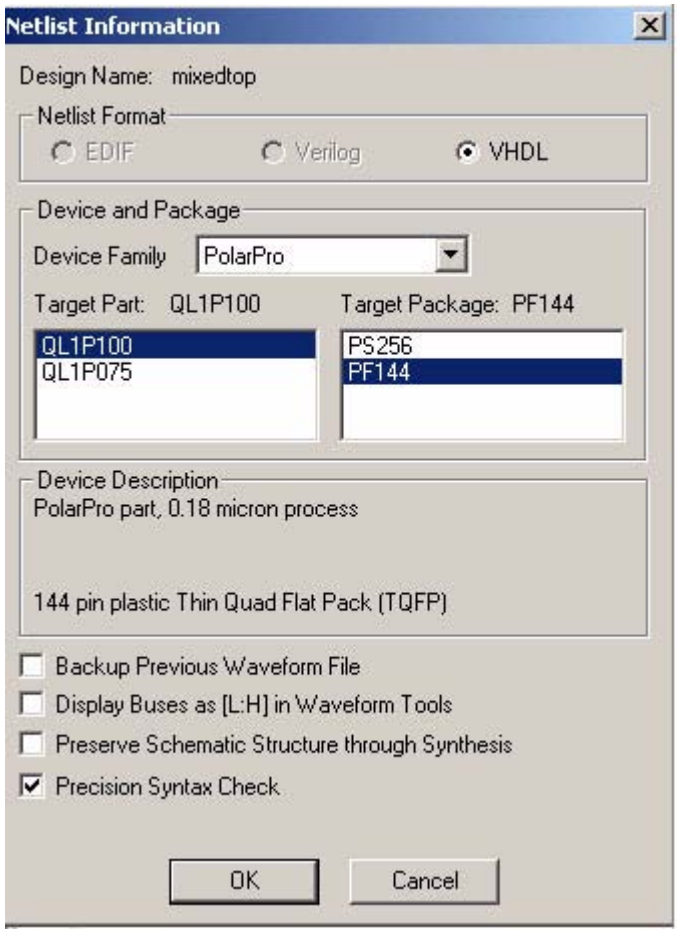
1. From the SpDE menu bar, select **Design>Schematic Editor & Navigator**, or click the  icon.
2. Select `MIXEDTOP.SCH` and click **Open**.

   The Hierarchy Navigator is displayed.

3.5.2 Exporting to VHDL

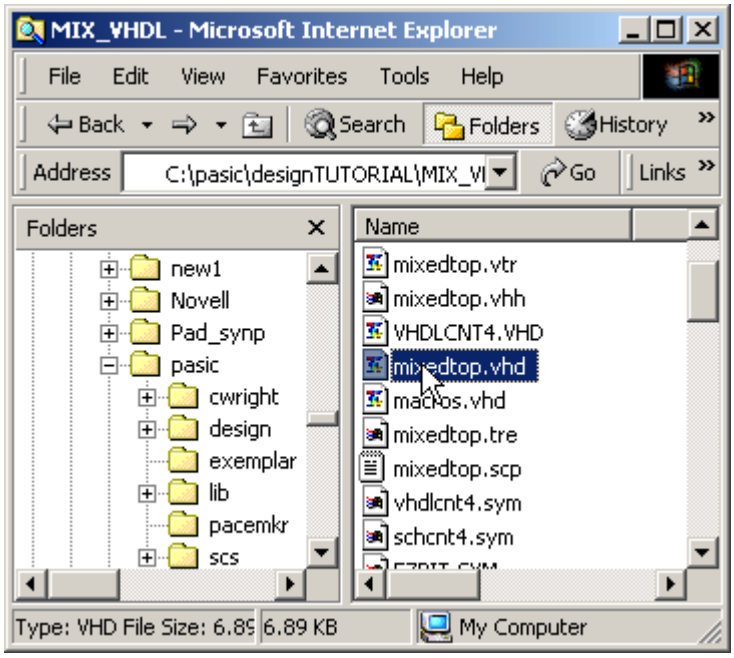
1. From the Hierarchy Navigator, select **Tools>Export QuickLogic**.

2. Select all the options shown below and click **OK**.



3. In the Pre-layout Information dialog box, click **Done**.

4. To verify that `MIXEDTOP.VHD` has been created, browse to the folder `C:\pasic\design\TUTORIAL\MIX_VHDL`.



3.6 Pre-Layout Simulation Using Active-HDL

In this section you will use `mixedtop.vhd` to do a pre-layout simulation using Active-HDL.

3.6.1 Starting Active-HDL

To launch Active-HDL:

1. Select **Start**>**Programs**>**Active-HDL**.

   Active-HDL is launched and the Getting Started screen is displayed.

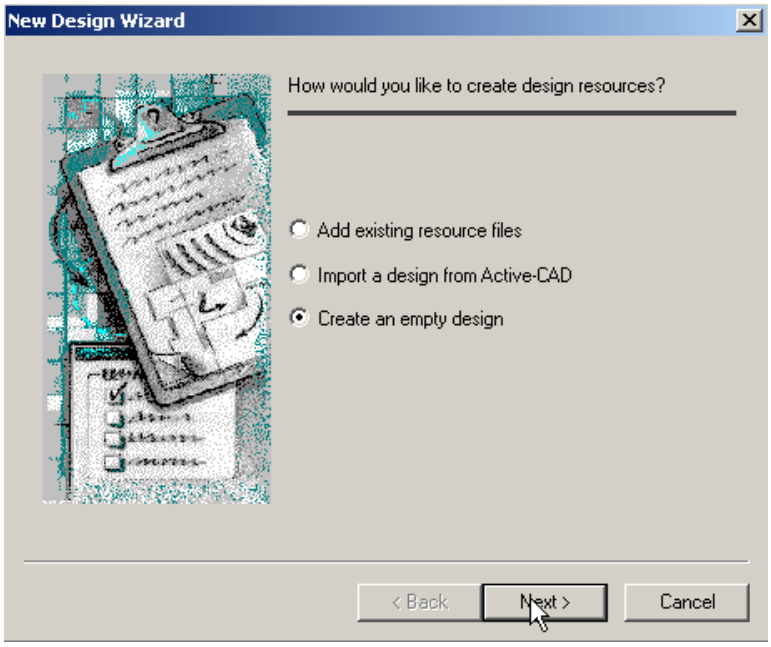
2. Click **Cancel**.

3.6.2 Creating a New Design

To create a new design:

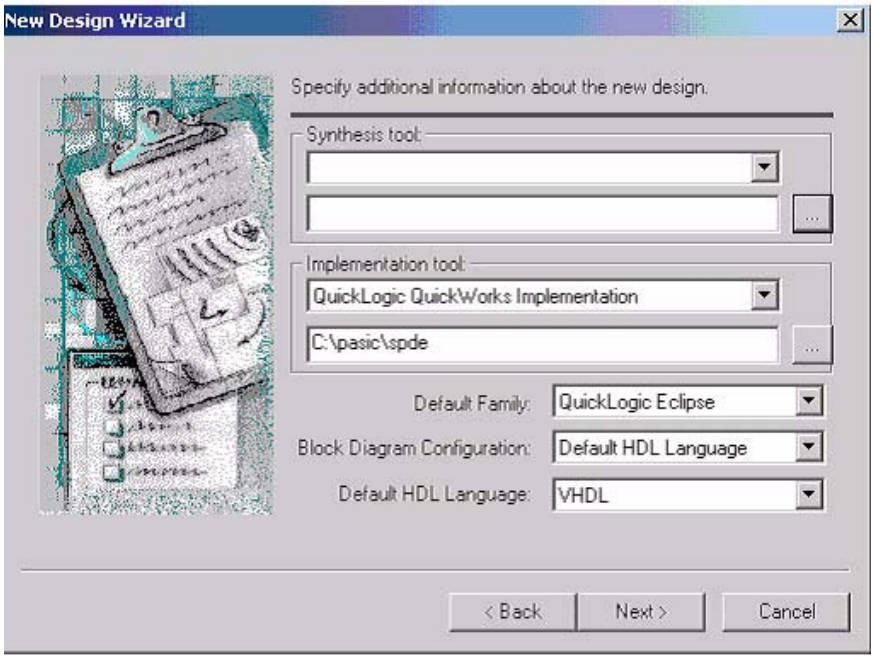
1. From the Active-HDL menu bar, select **File>New>Design.**

The New Design Wizard screen is displayed.



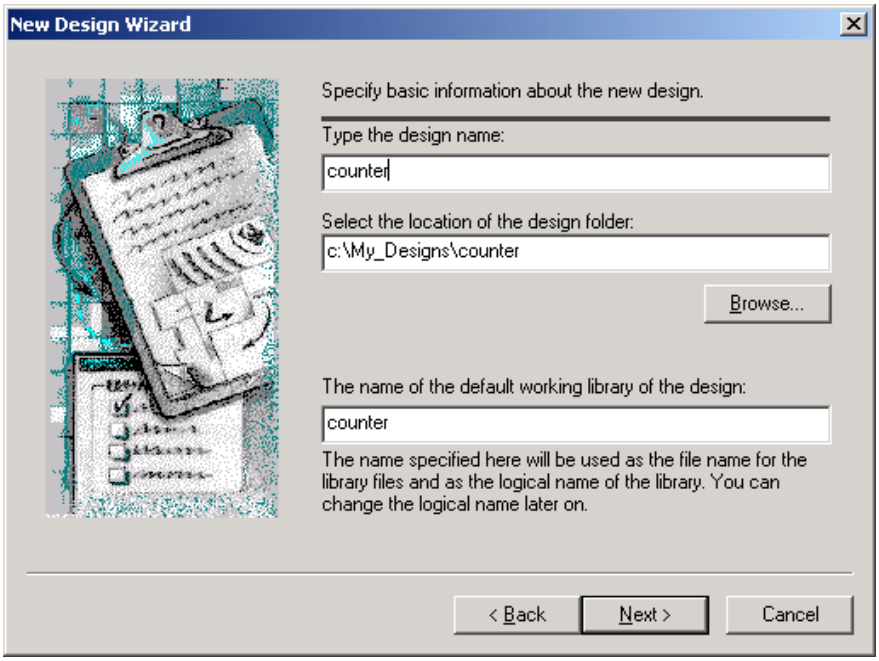
2. Select **Create an empty design** and click **Next**.

   The following screen is displayed.



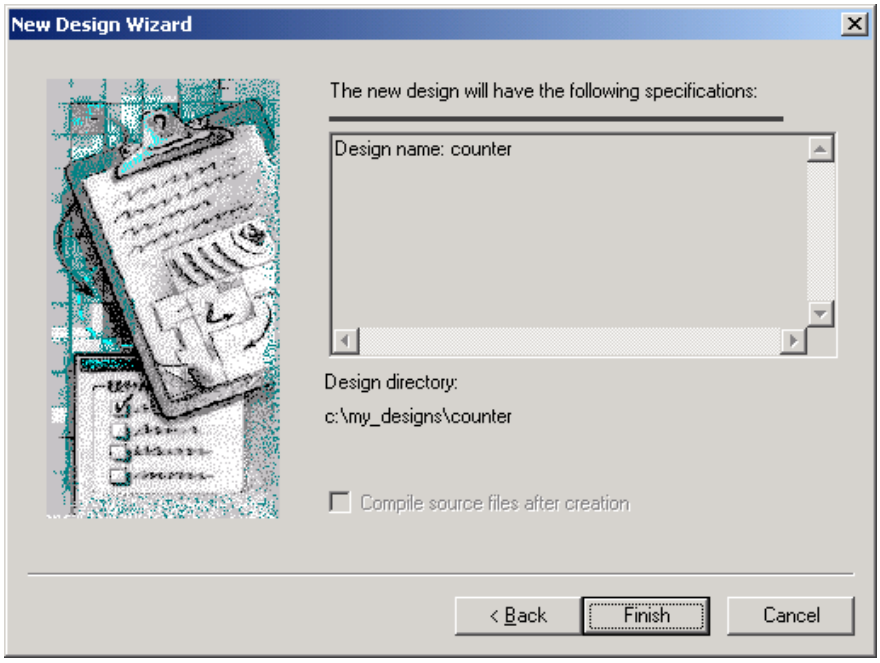
3. Populate the screen as shown, and select **Default HDL Language** (VHDL) option.
4. Click **Next**.

The following screen is displayed.



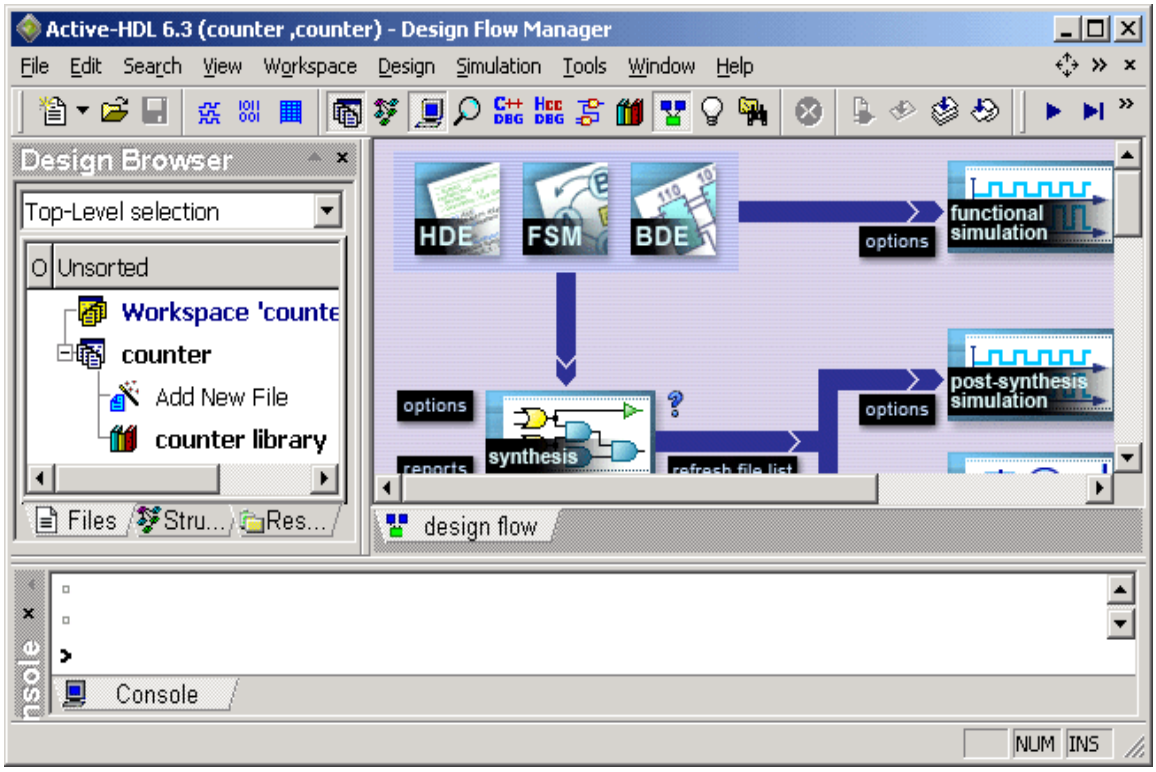
5. Type the design name and location of the design folder.
6. Click **Next**.

   The following screen is displayed.



7. Click **Finish**.

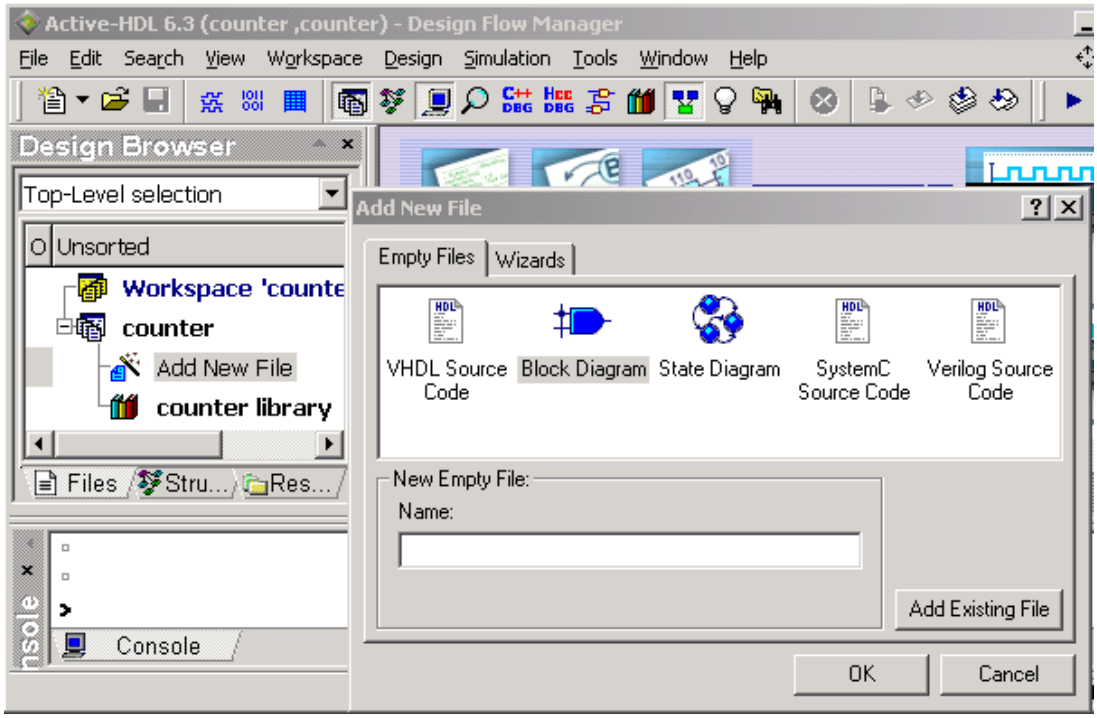
The Active-HDL screen is displayed.



3.6.3 Adding a New File

To add new files that where not added during the New Design Wizard process:

1. Double-click on **Add New File** and the following dialog box opens.

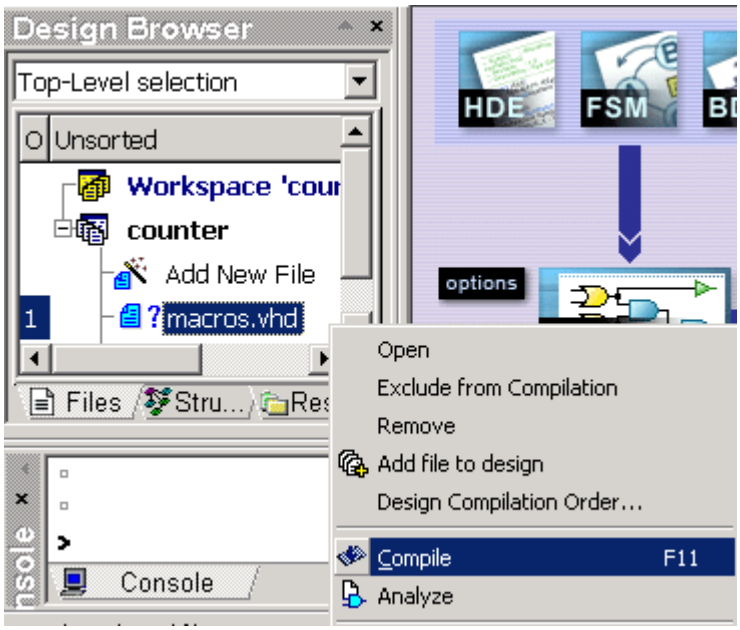


2. Click on **Add Existing File**.
3. Navigate to `c:\pasic\spde\data`, select **macros.vhd** (or **macros_pp.vhd** for PolarPro devices), and click **Add**.

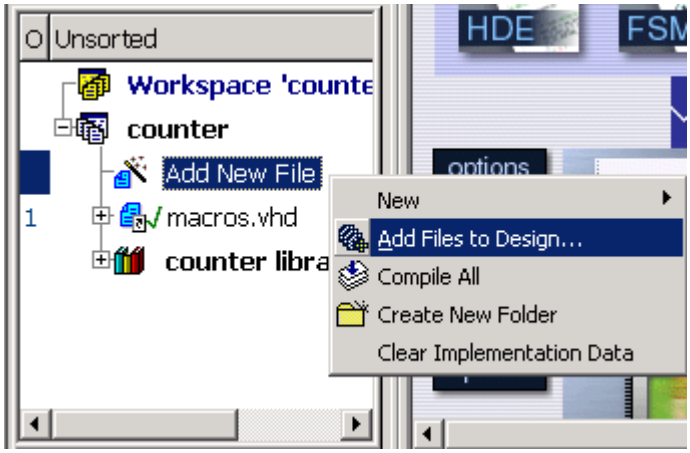
3.6.4 Compiling the Files

To compile the files:

1. Right-click on **marcos.vhd** and click on **Compile**.

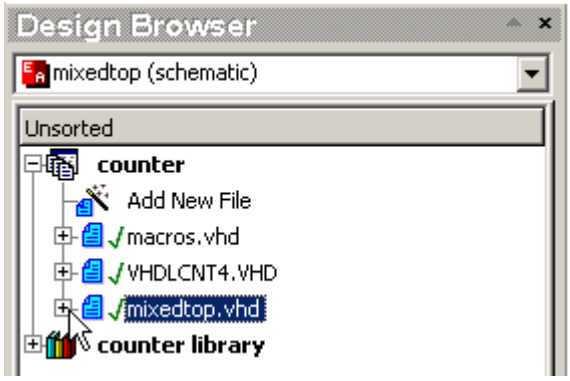


2. Right-click on **Add New File**.
3. Select **Add Files to Design**.



4. Navigate to `C:\pasic\design\TUTORIAL\MIX_VHDL`, select **VHDLCNT4.VHD** and **mixedtop.vhd**, and click **Add**.
5. Right-click on **VHDLCNT4.VHD** or **mixedtop.vhd** and select **Compile All**.

The Active-HDL Design Browser should look as follows:

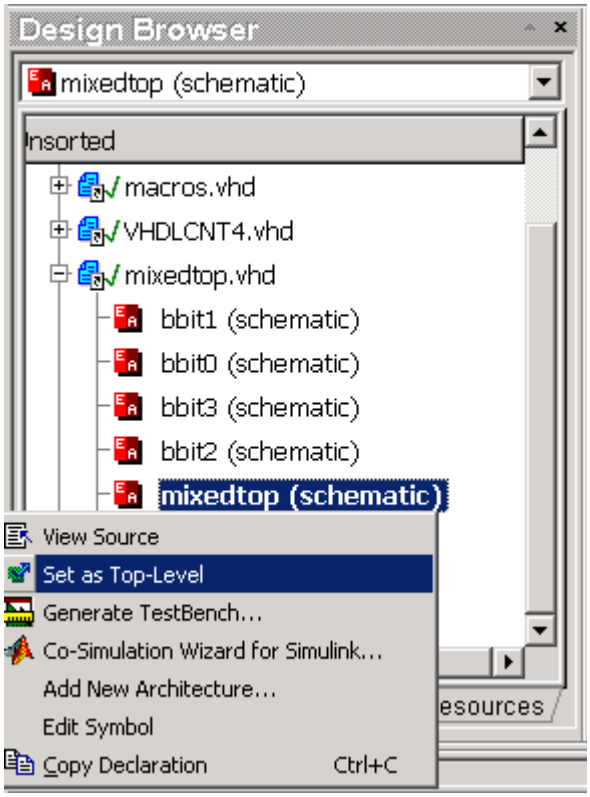


3.7 Setting the Top Level Design

3.7.1 Setting a Design as a Top Level Design

In this section you will set mixedtop as the top level design and create a test waveform for it.

1. Click on the plus sign (+) to expand `mixedtop.vhd`.
2. To set the design as top level right-click on **mixedtop** and select **Set as Top-Level**.



3.7.2 Creating a Test Waveform

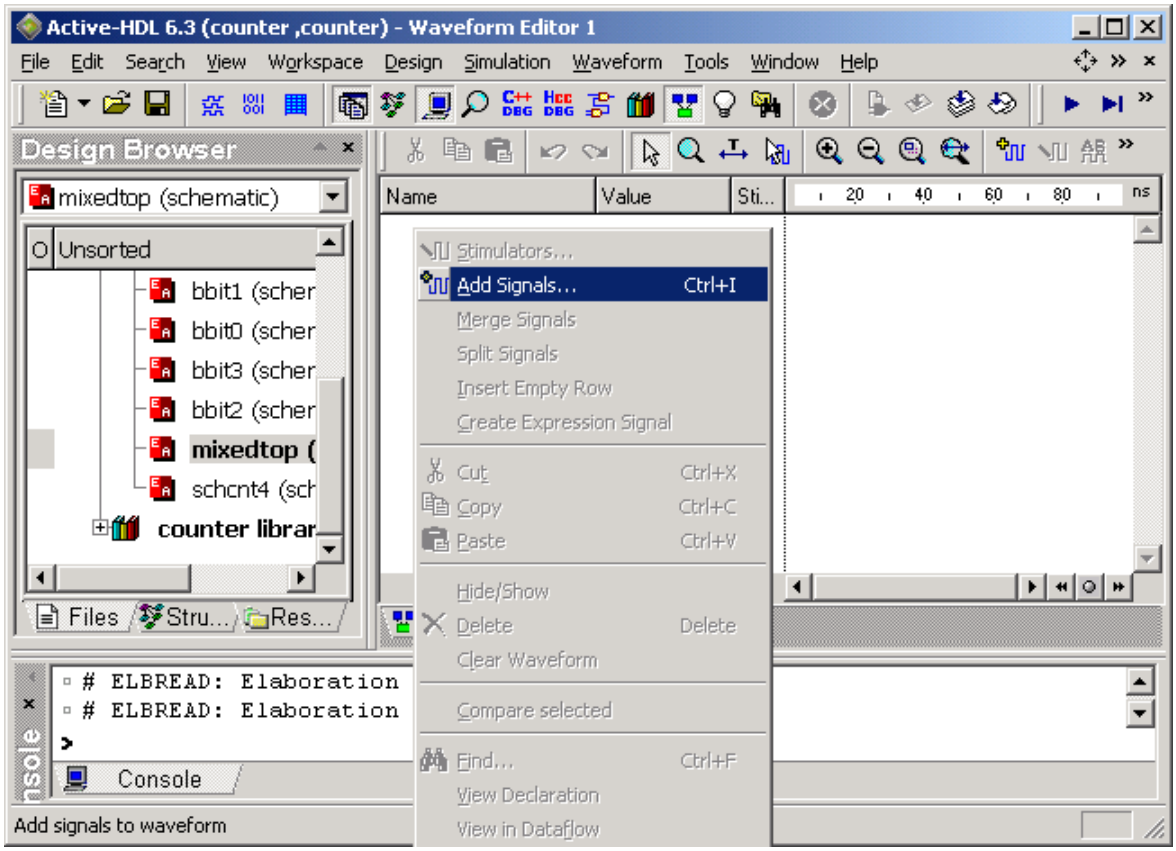
To create a test waveform:

1. From the Active-HDL toolbar, click on the **Waveform Editor** icon.

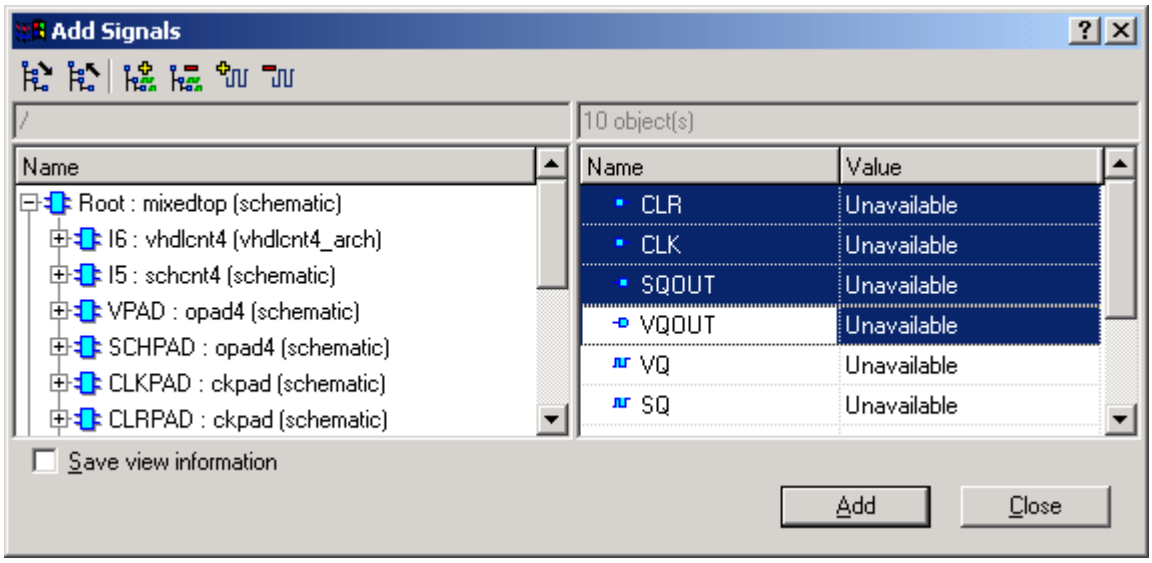
3.7.3 Adding Signals

To add signals:

1. After placing the cursor in the window as shown below, right-click and select **Add Signals**.



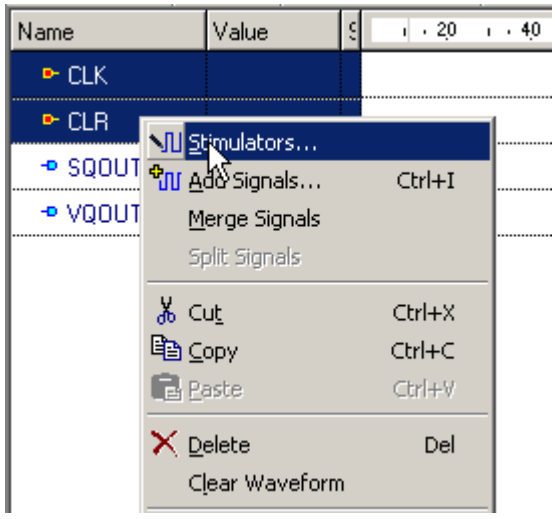
2. Select **CLR, CLK, SQOUT, VQOUT**. Click **Add** and then **Close**.



3.7.4 Opening Simulators

To open simulators:

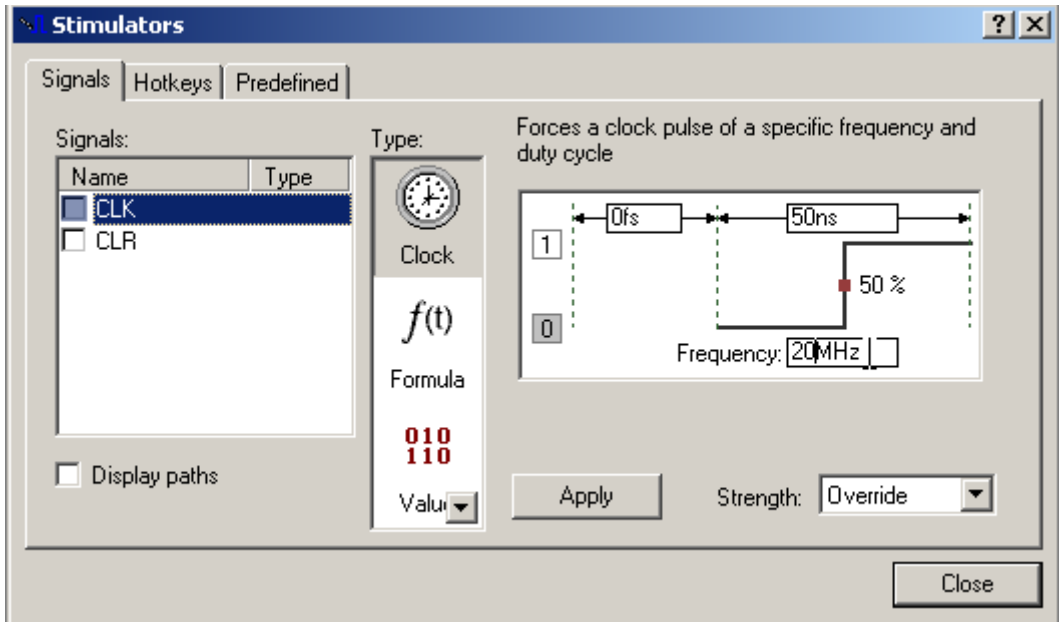
1. Select the simulators you want to open (in this case **CLR** and **CLK**), right-click, and select **Stimulators.**



3.7.5 Defining the Frequency

To define frequency:

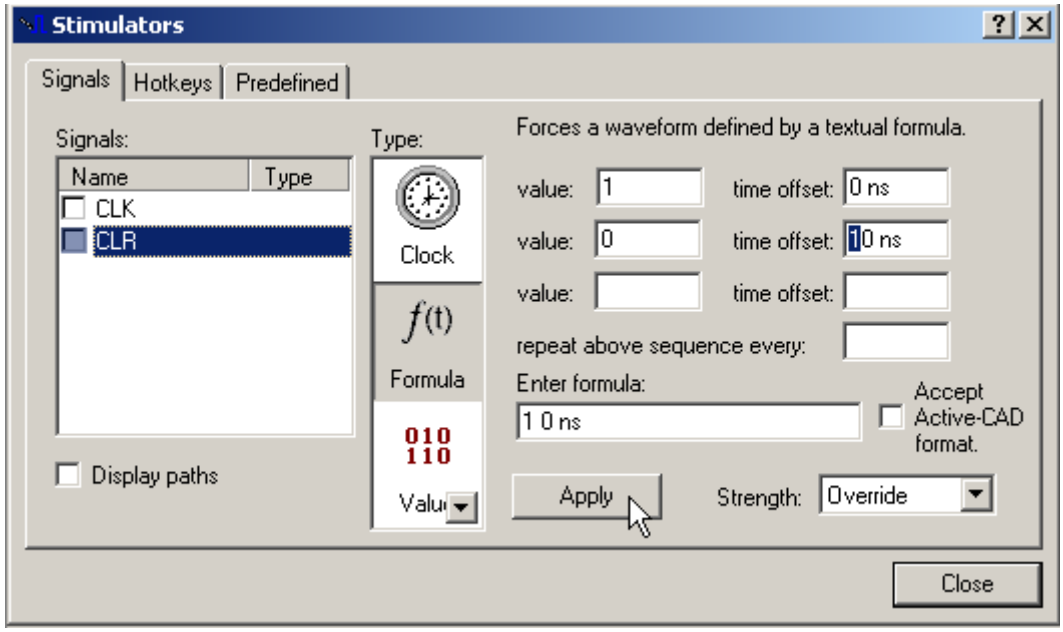
1. Select the **CLK** signal, select **Clock**, click in the Frequency field, type in the frequency (20 MHz in the example below), and then click **Apply**.



3.7.6 Defining a Formula

To define a formula:

1. Select **CLR** select **Formula**, and type the text shown below.



2. Click **Apply,** and then **Close**.

3.7.7 Initializing the Pre-Layout Simulation

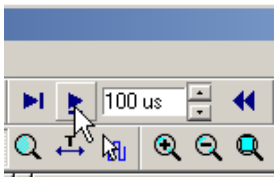
To initialize simulation in the Waveform Editor screen:

1. From the Active-HDL menu bar, select **Simulation>Initialize Stimulation**.

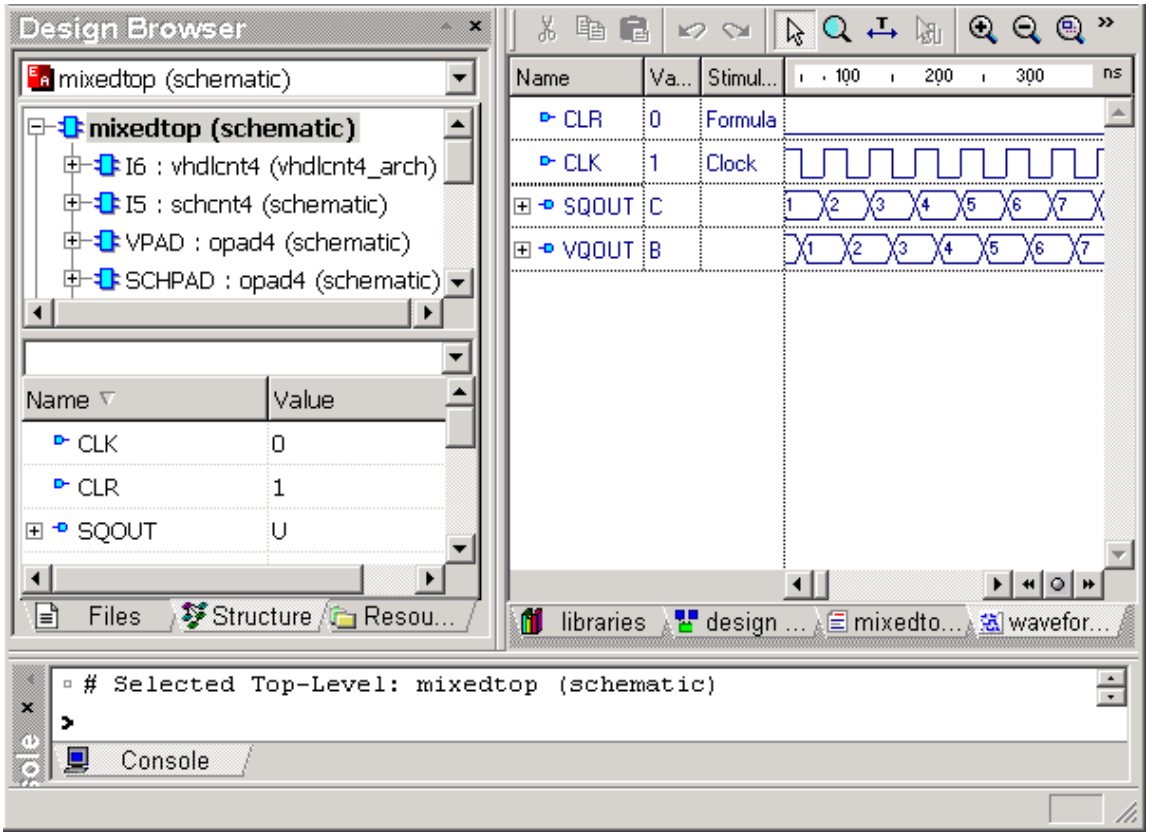
3.7.8 Running the Pre-Layout Simulation

To start running the pre-layout simulation:

1. Expand the screen, in the menu bar type in **`100 us`** and then click the **Run** arrow to the left.



The output of the waveform counters are displayed.



Use the zoom tools in the toolbar to view the waveform.

2. After completing the simulation, exit Active-HDL.

3.8 Post-Layout Simulation Using Active-HDL

To perform a post-layout simulation for the design you have just created, you need to synthesize to get the `.vhq` and `.sdf` files:

3.8.1 Starting Synthesis

To start the synthesis tool Mentor Graphics Precision RTL:

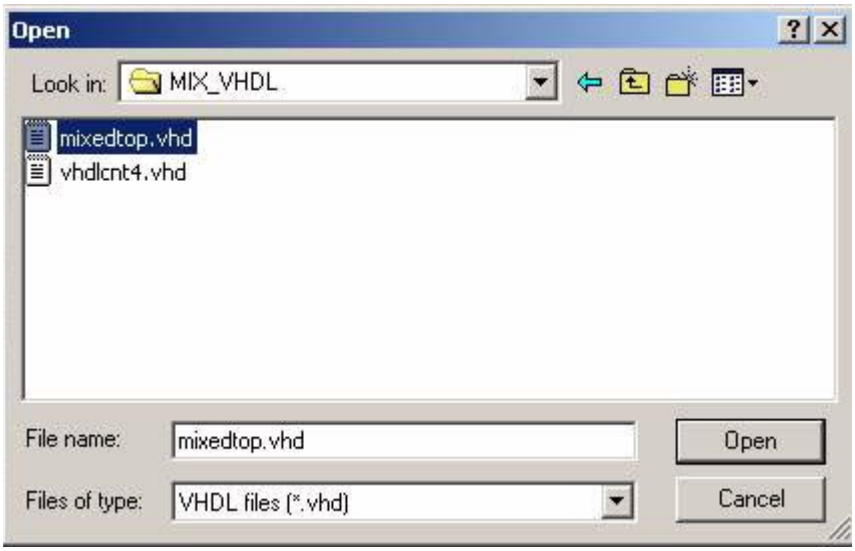
1. From the SpDE menu bar, select **File>Import Using Precision RTL**, or click the **Import Precision** icon.

   The Open window is displayed.

3.8.2 Running a Design in Precision

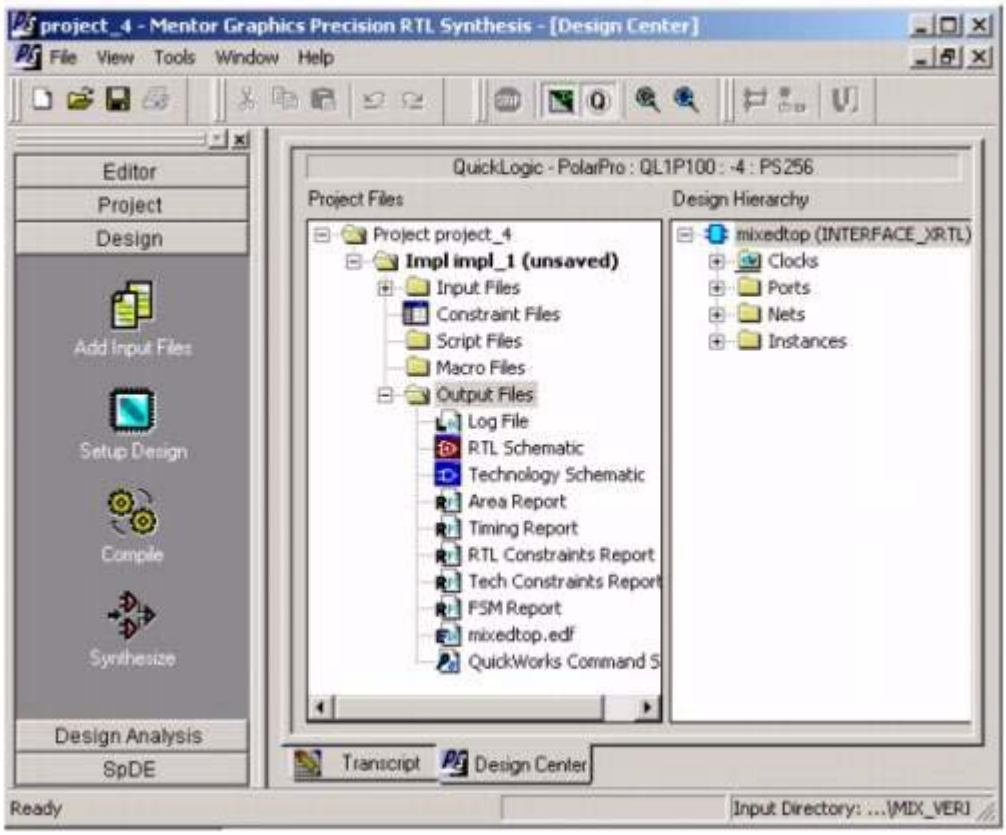
There are two ways to run a design in Precision, the first is as follows:

1. Navigate to the default directory `C:\pasic\design\TUTORIAL\MIX_VHDL\.`
2. Select **VHDL files (*.vhd)** from the Files of type pull-down menu.



3. Select **`mixedtop.vhd`** and click **Open**.

The Precision RTL Synthesis screen is displayed and automatically a `.tcl` script is generated to create a project file.

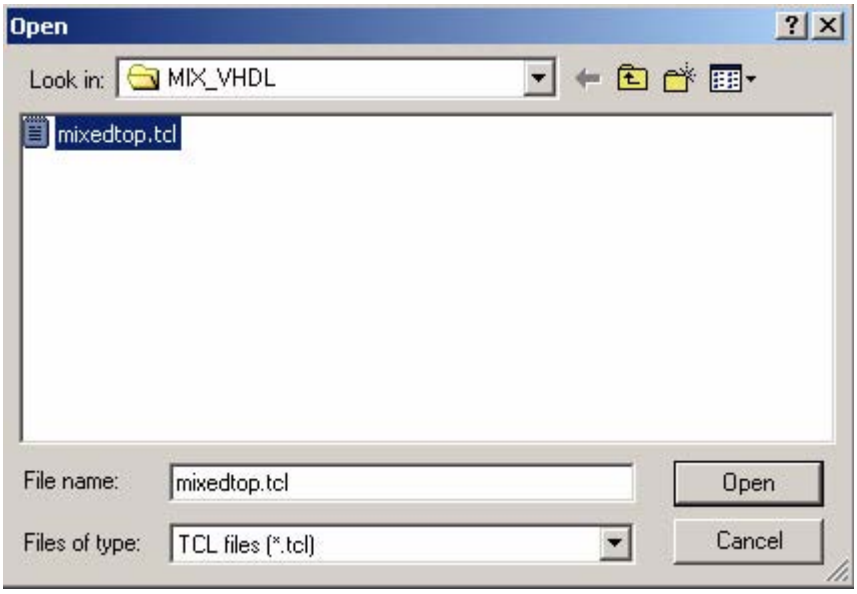


4. Select the **Design** tab on the left side of the Precision RTL dialog box.
5. Click **Add Input files** to add the VHDL file.
6. Click **Setup Design**.
   a. Select the desired **product family** from the Technology menu.
   b. Select the **device** from the Package menu.
   c. Select the device **Speed grade** from Speed menu.
4. Click **Compile** to compile the VHDL design files.
5. Click **Synthesize** to complete the design synthesis.

   If there are errors, view the transcript window.
6. Select **File>Exit** to quit Precision RTL and load the generated EDIF file using the **SpDE** tab.

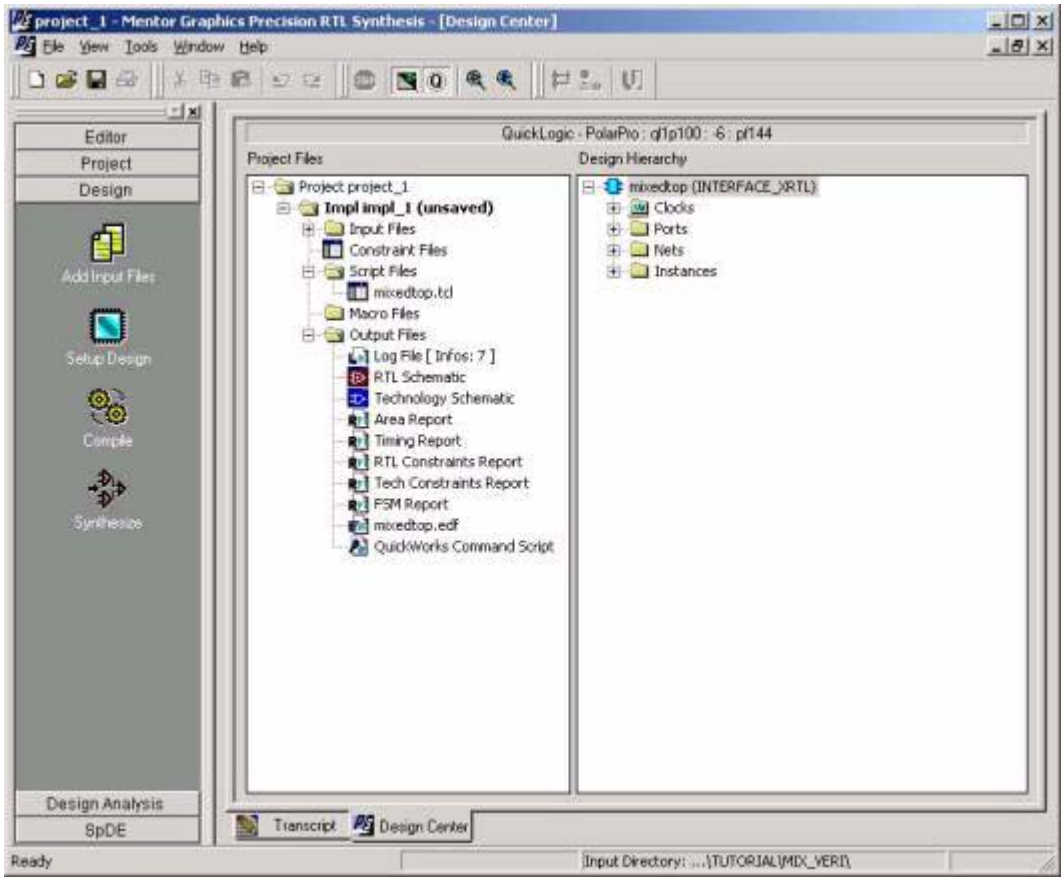
The following is an alternate method of running a design in Precision RTL:

1. Navigate to the default directory `C:\pasic\design\TUTORIAL\MIX_VHDL\.`
2. Select **TCL files (*.tcl)** from the Files of type pull-down menu.



3. Select **`mixedtop.tcl`** and click **Open**.

The Precision RTL program is displayed and automatically generates the EDIF.



3.8.3 Running a Design in SpDE

If the EDIF netlist is generated by loading HDL in Precision RTL, follow this step to load the design:

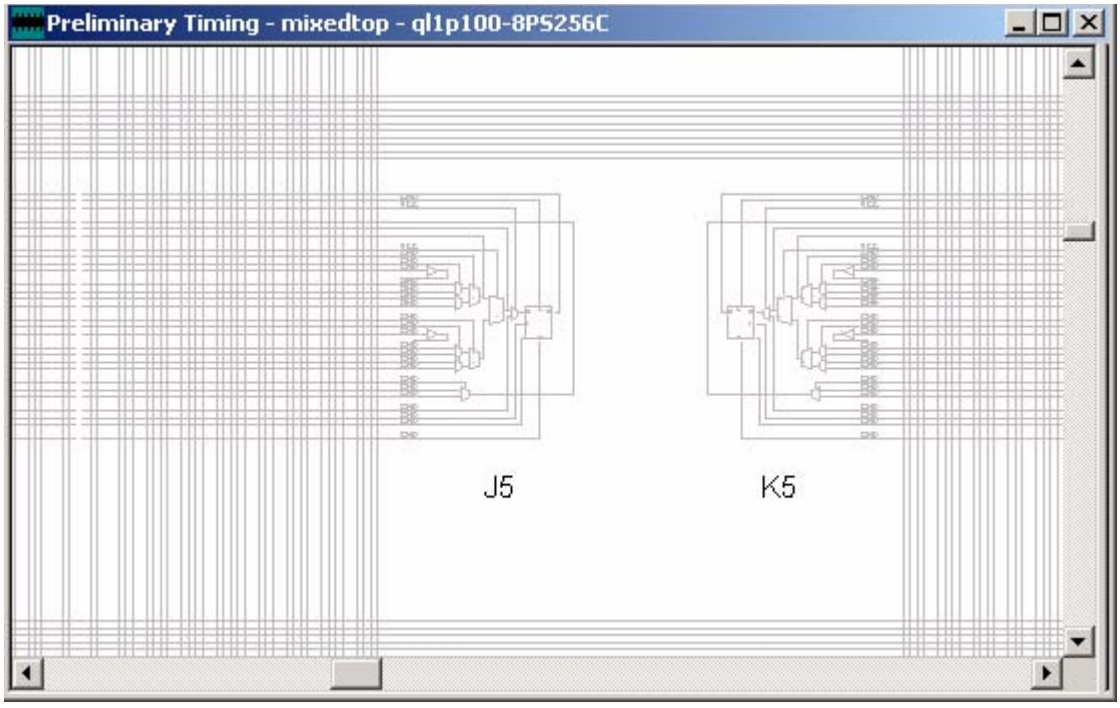
1. From the SpDE menu bar, select **Tools>Run TCL Script...** (*.tcl generated by Precision RTL).

   This automatically runs all the tools and generates the `.chp` file.

If the EDIF netlist is generated by running `.tcl` (generated by the schematic editor), the EDIF netlist is automatically loaded into SpDE after exiting from the synthesis tool. The Retarget Device screen is displayed.

2. Select the Device Family, Target Device, and Package and click **OK**.

   The Preliminary Timing screen is displayed.

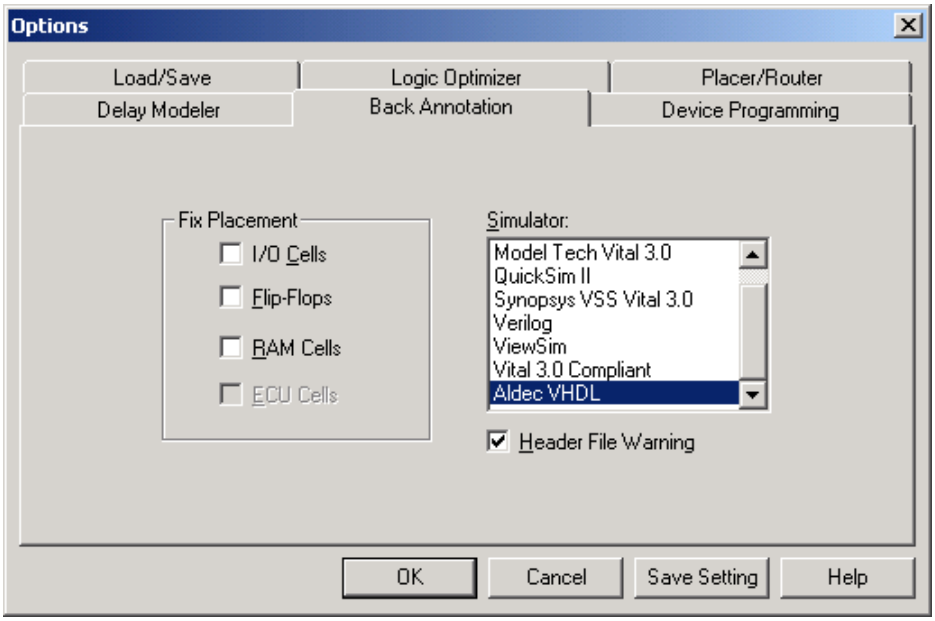


3.8.4 Setting Options for Back Annotation

To set options for back annotation:

1. From the SpDE menu bar, select **Tools>Options**.

   The Options window is displayed.



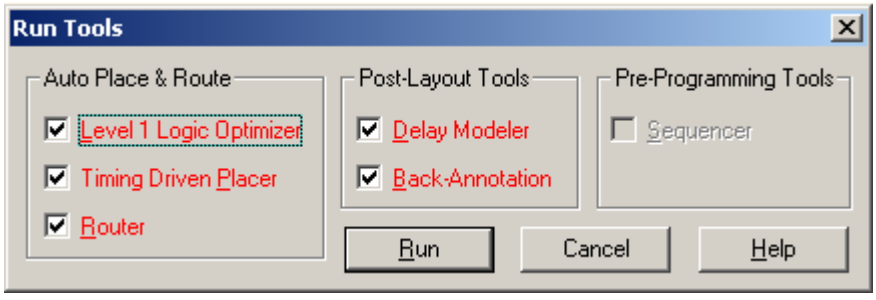
2. Click on the **Back Annotation** tab.
3. Select **Aldec VHDL** in the Simulator window.
4. Click **Save Setting** and then click **OK**.

3.8.5 Selecting and Running Tools

To select and run tools:

1. From the SpDE menu bar, select **Tools>Run Selected Tools,** or click the  icon.

   The Run Tools window is displayed.



2. Click **Run**.

   After the tools have run, a report is displayed.

3. Verify the creation of the `mixedtop.vhq` and `mixedtop.sdf` files in the in `C:\pasic\design\TUTORIAL\MIX_VHDL`.

As described in the following sections, next you will use the `.vhq` and `.sdf` files to do a post-layout simulation on your design.

3.8.6 Starting Active-HDL

To launch Active-HDL:

1. Select **Start**>**Programs**>**Active-HDL**.

   Active-HDL is launched and the Getting Started screen is displayed.

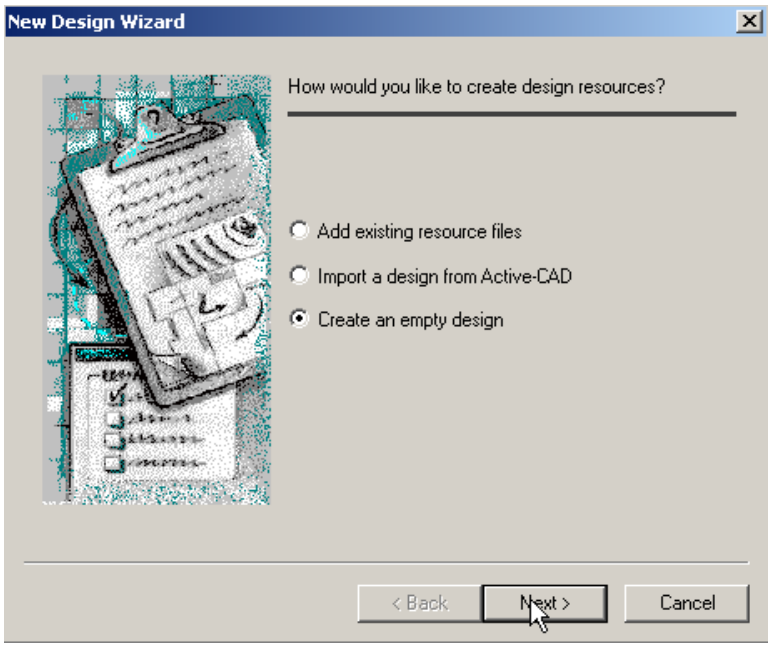
2. Click **Cancel**.

3.8.7 Creating a New Design

To create a new design:

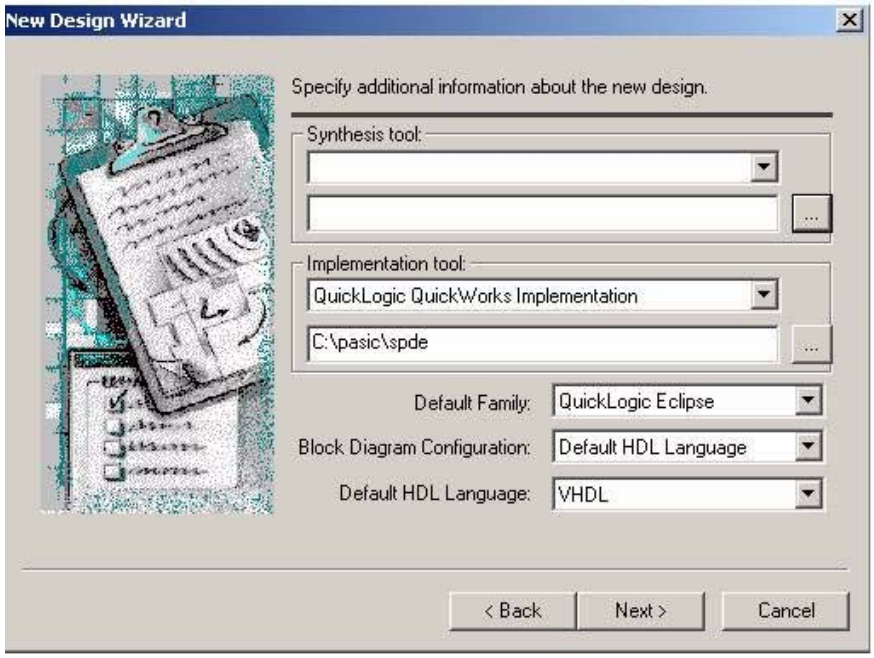
1. From the Active-HDL menu bar, select **File**>**New**>**Design.**

   The New Design Wizard screen is displayed.



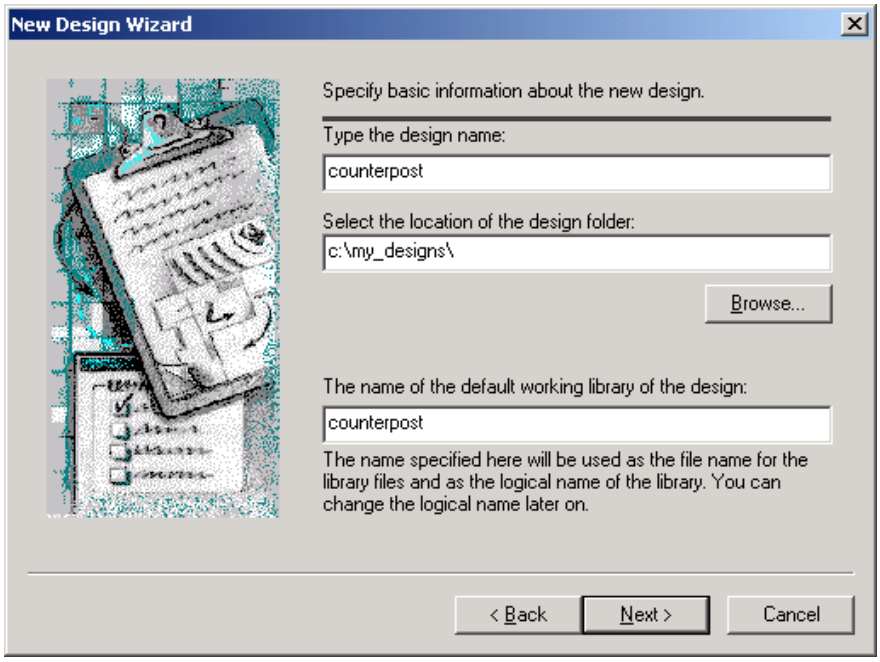
2. Select **Create an empty design** and click **Next**.

The New Design Wizard screen is displayed.



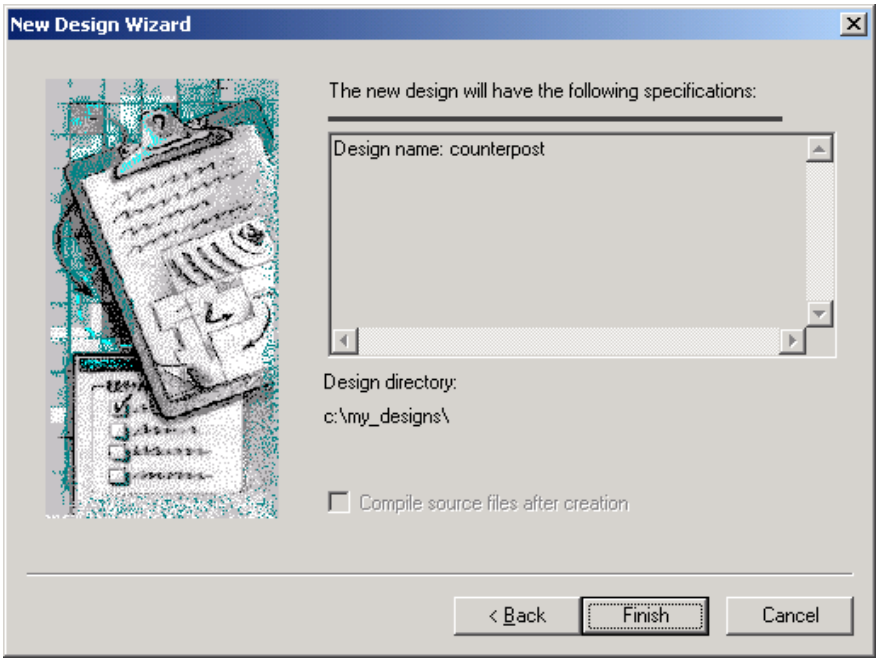
3. Populate the screen as shown, select **Default HDL Language** option.
4. Click **Next**.

   The New Design Wizard screen is displayed.

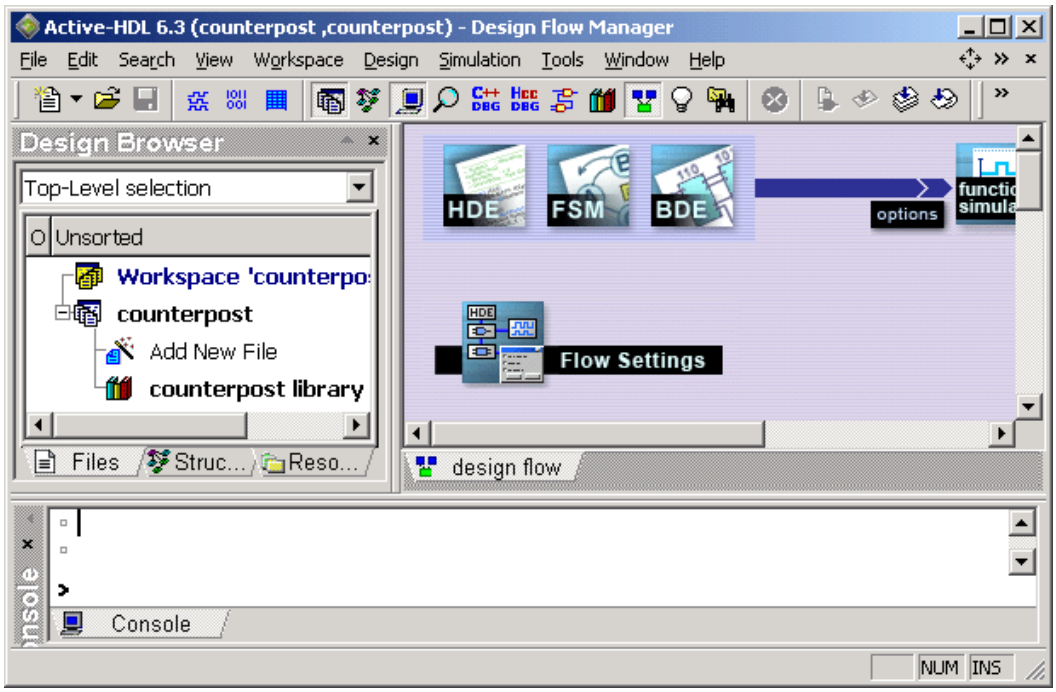


5. Type the design name **counterpost**.
6. Click **Next**.

The New Design Wizard screen is displayed.



7. Click **Finish**.
8. The Active-HDL screen is displayed.

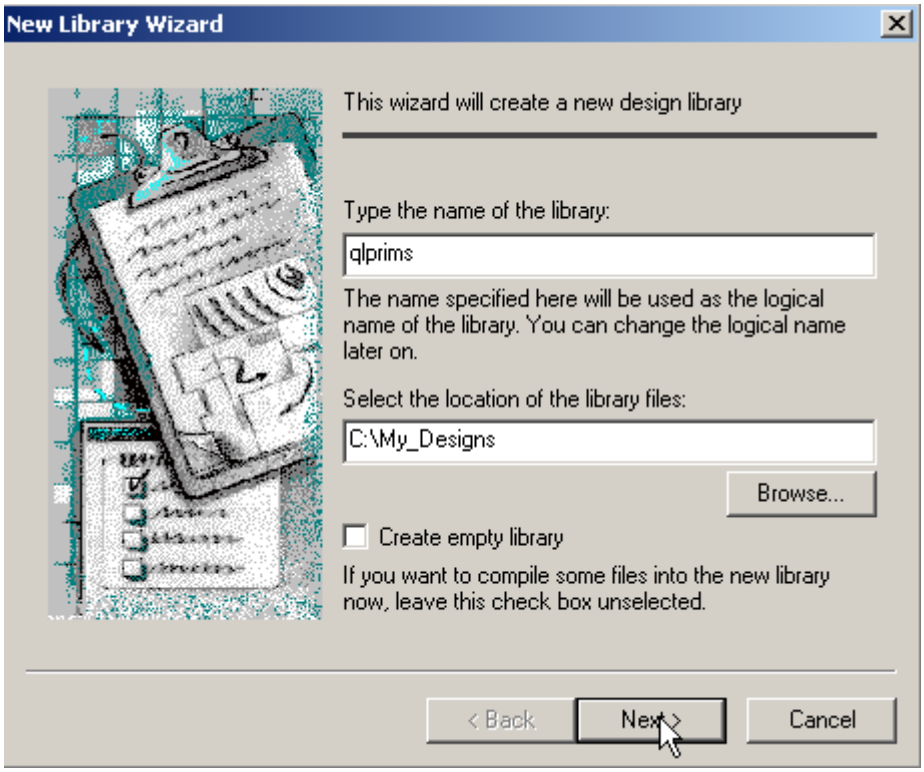


3.8.8 Creating a Library

To create a library:

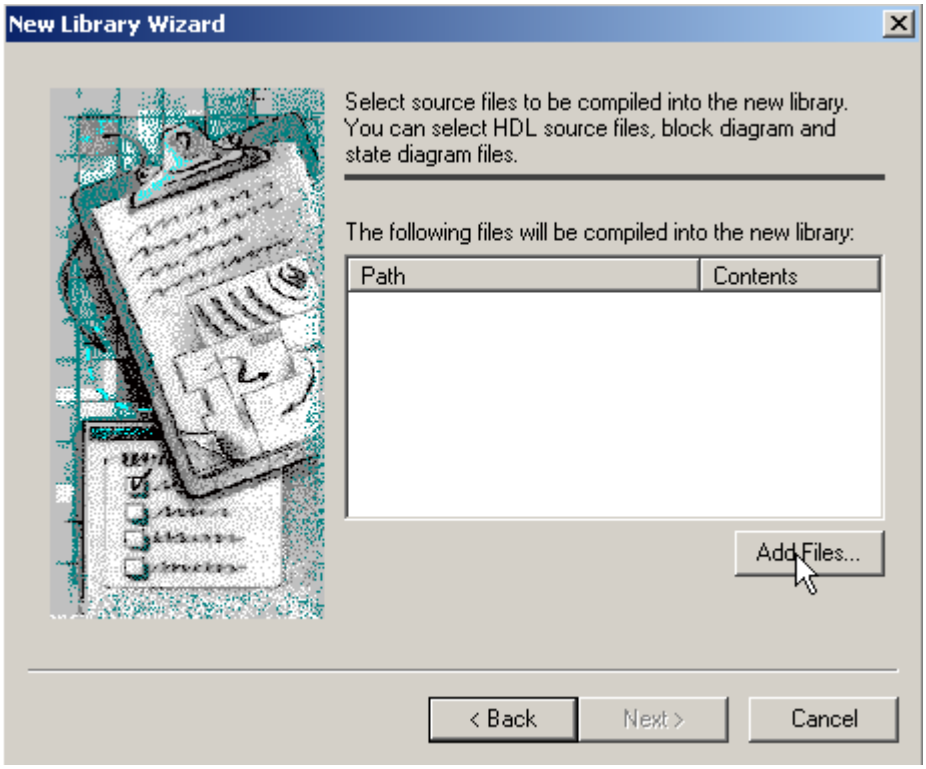
1. From the Active-HDL menu bar, select **Design>Create Library.**

   The New Library Wizard is displayed.

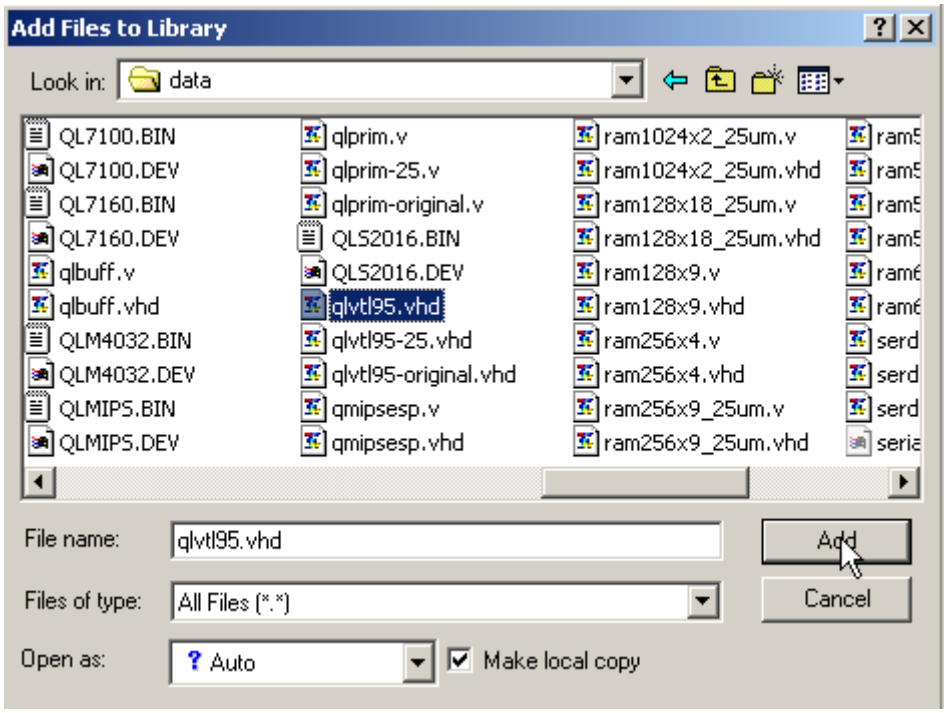


2. In the space provided, type in **`qlprims`** and click **Next**.

3. Click **Add Files.**



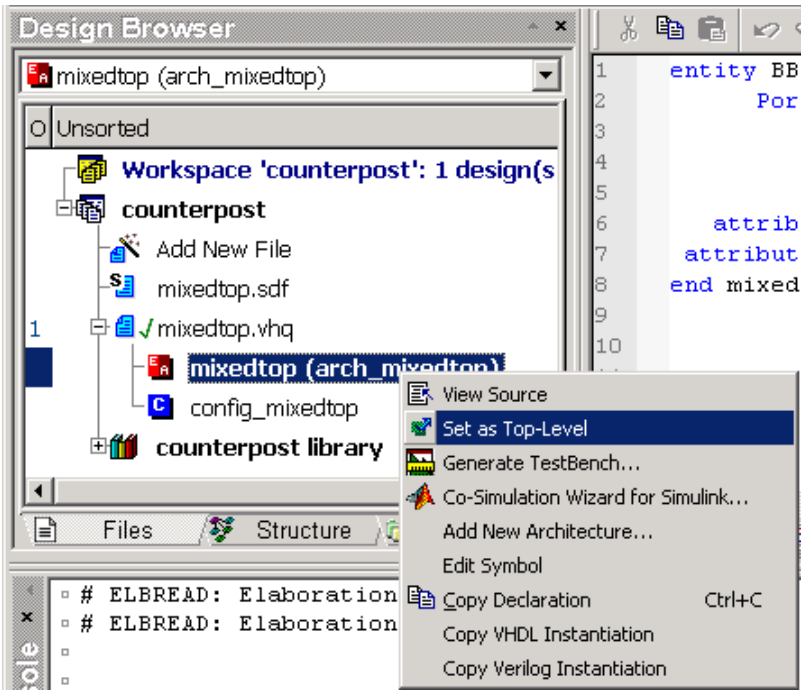
4. Browse to `c:\pasic\spde\data` and select **qlvtl95.vhd.** Click **Add**, **Next** and then **Finish**.



3.8.9 Adding Source Files

To add source files to the Design Browser in Active-HDL:

1. Right-click on **Add New File**, browse to `C:\pasic\design\TUTORIAL\MIX_VHDL` and select **mixedtop.sdf**, and click **Add**.
2. Right-click on **Add New File**, browse to `C:\pasic\design\TUTORIAL\MIX_VHDL` and select **mixedtop.vhq**, and click **Add**.
3. Right-click on **mixedtop.vhq** and select **Compile**.
4. To set **mixedtop** as Top-Level, click on the plus sign (+) to expand **mixedtop.vhq**, right-click on **mixedtop**, and select **Set as Top-Level**.

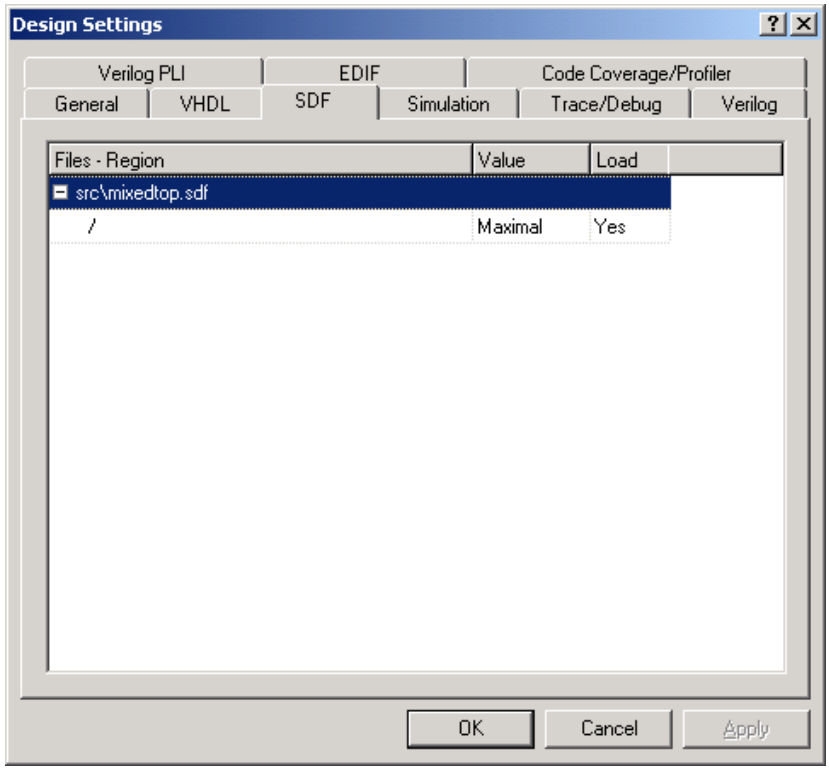


3.8.10 Selecting SDF Options

To apply the setting for the `.sdf` file:

1. From the Active-HDL menu bar, select **Design>Settings.**

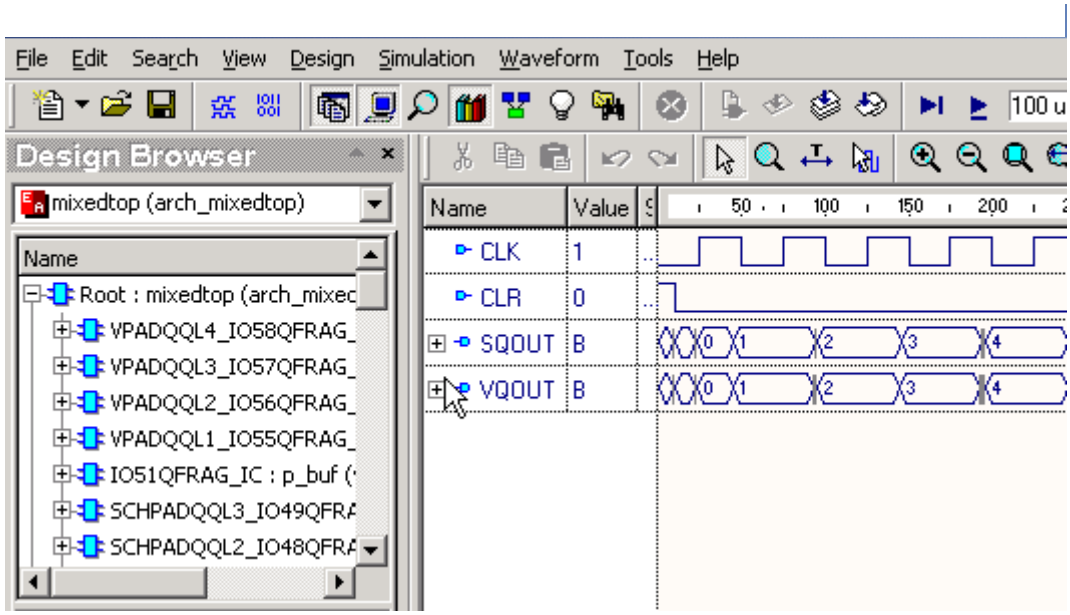
The Design Settings dialog box is displayed.



2. Click on the **SDF** tab.
3. Change Load to **Yes** and Value to **Maximal**.
4. Click **Apply** and **OK**.

3.8.11 Viewing the Post-Layout Simulation Output Waveform

The steps for running the post-layout simulation are similar to running the pre-layout simulation. Repeat the steps in **Section 3.7.2, "Creating a Test Waveform," on page 108** through **Section 3.7.8, "Running the Pre-Layout Simulation," on page 111**. The output waveform should look as follows.



Chapter 4
Verilog-Only Design Tutorial

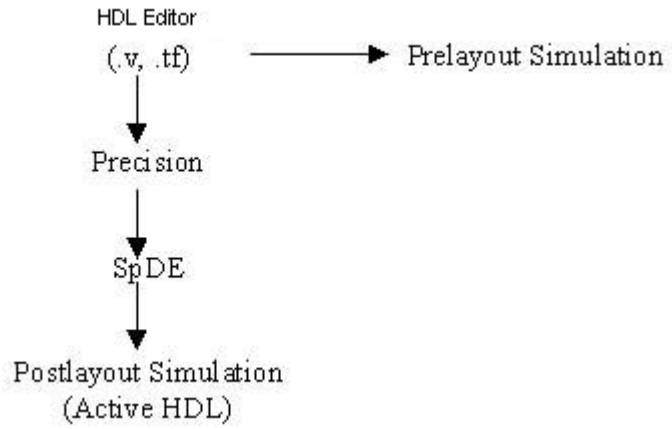
This tutorial describes the Verilog HDL design flow. For more detailed information, refer to the *Design Overview* chapter of the *QuickWorks User Manual* and the *Precision RTL User's Guide* included with QuickWorks.

This chapter contains the following sections:

NOTE: This tutorial assumes that you have a working knowledge of Microsoft Windows. Experience with Verilog will help, but is not required.

4.1 Functional Overview

Figure 4-1: Verilog-Only Design Flow



This tutorial will walk you through a complete Verilog HDL design. The design you will implement is the `RAS/CAS` state machine for the DRAM controller described in QuickLogic *Application Note 5 (QAN5)* at http://www.quicklogic.com/images/appnote05.pdf. You do not need any knowledge of this application note to make use of this tutorial.

For Verilog-only design flow use the Verilog-HDL designs located on the default directory at `C:/pasic/design//TUTORIAL/VERILOG/DRAMCTRL.V`.

You will use Active-HDL to run a functional simulation and to view the results. You will then use SpDE to optimize, place, and route the design. Last, you will re-run the simulator to perform a post-layout or timing simulation.

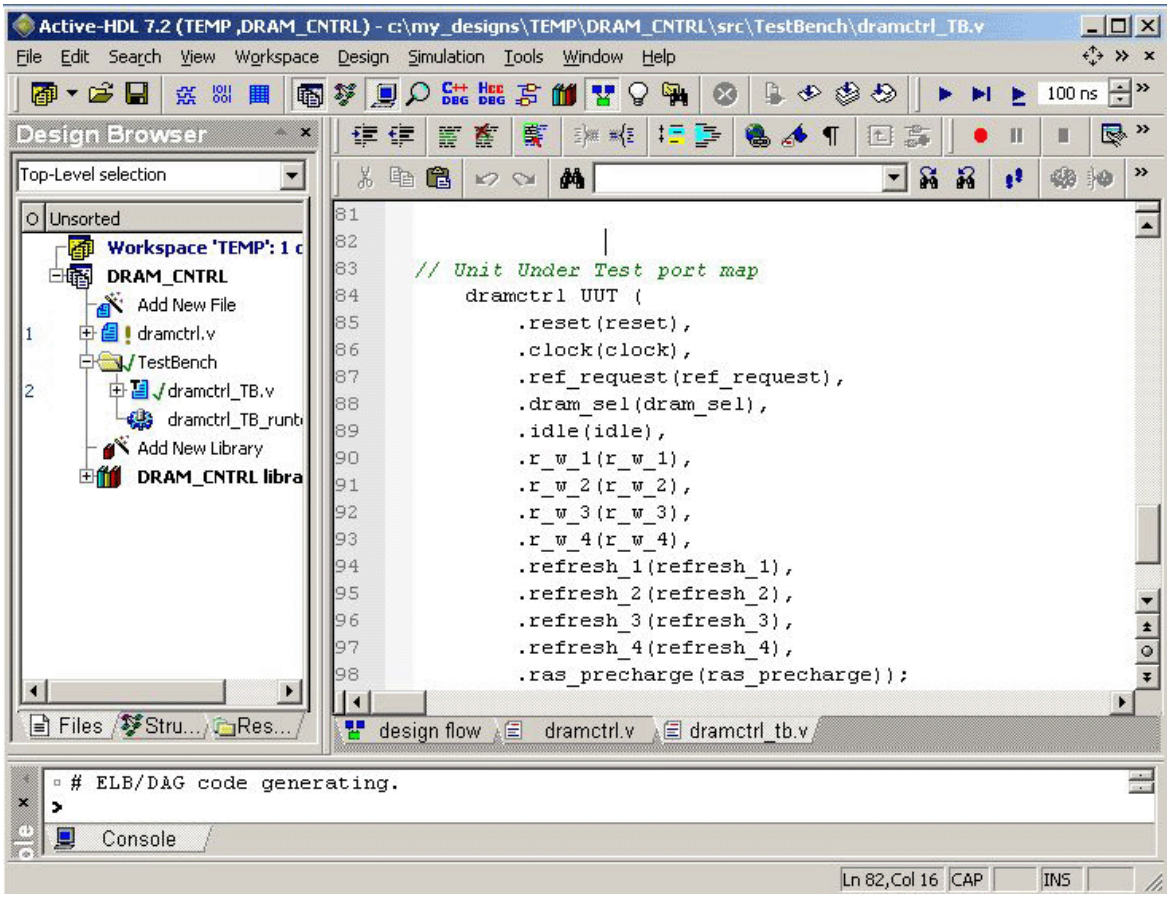
4.2 Creating a Test Waveform

Before you can run a simulation on your Verilog design, you need to create input vectors (referred to as a test fixture or test bench) for your design. Although the Waveform Editor can be used to create these vectors graphically, you can use any simulator to create your own test fixture.

To create a Verilog test fixture:

1. From the Active-HDL menu bar (with the `dramctrl.v` design file displayed in the active window), select **Tools>Generate Test Bench**.

   A new file is created, `dramctrl_TB.v`. This file can be used as a template to easily add input stimulus for your Verilog design. The newly created test bench for your design should now be displayed in a new window as follows.



2. Near the end of the file, after the initial statement, type the following lines of Verilog code, as shown in the following:

```
initial begin
    reset = 0;
    #50 reset = 1;
     #50 reset = 0;
end
initial begin
     clock = 1;
     forever
     begin
                 #20 clock = 0;
                 #29 clock = 1;
     end
end
initial begin
     ref_request = 0;
     #750 ref_request = 1;
end
initial begin
     dram_sel = 0;
     #250 dram_sel = 1;
     #1000 dram_sel = 0;
end
```

These code lines are the Verilog equivalent of the waveforms used to simulate the design.

3. Select **File>Save**.
4. Select **File>Exit** to quit Active-HDL.

4.3 Pre-Layout Simulation Using Active-HDL for Verilog

In this section you will use `MIXEDTOP.V` to perform a pre-layout simulation using Active-HDL. You will use the Waveform Editor to create a test waveform. The file will be saved as a `.tf` file and will be used to test the design shown previously in this chapter.

4.3.1 Creating the Test Waveform

4.3.1.1 Launching the Waveform Editor

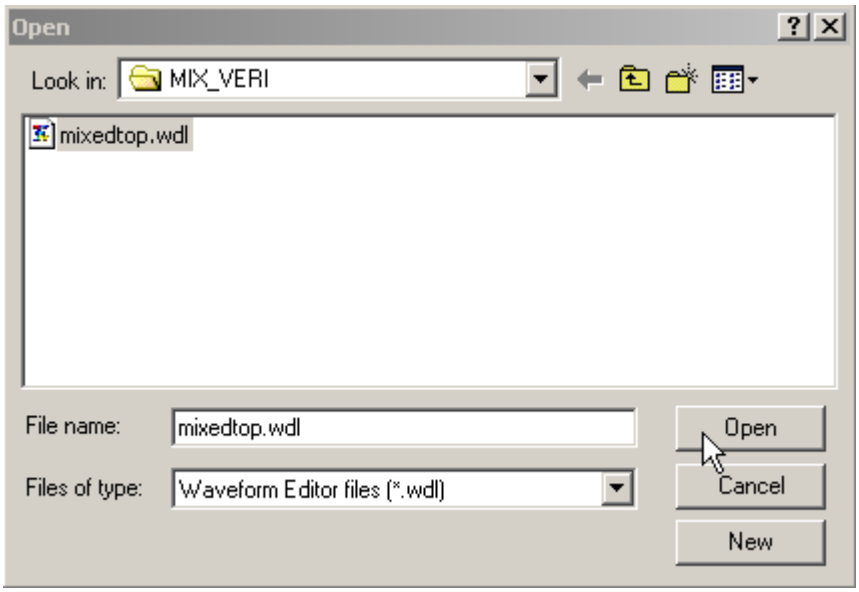
To launch the Waveform Editor:

1. From the SpDE toolbar, click on the **Waveform Editor** icon.

4.3.1.2 Creating the Test Waveform

To create a test waveform:

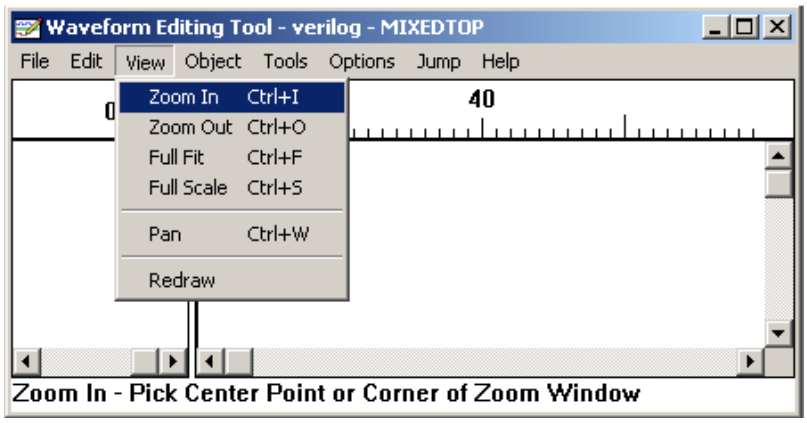
1. Select **mixedtop.wdl** and click on **Open**.



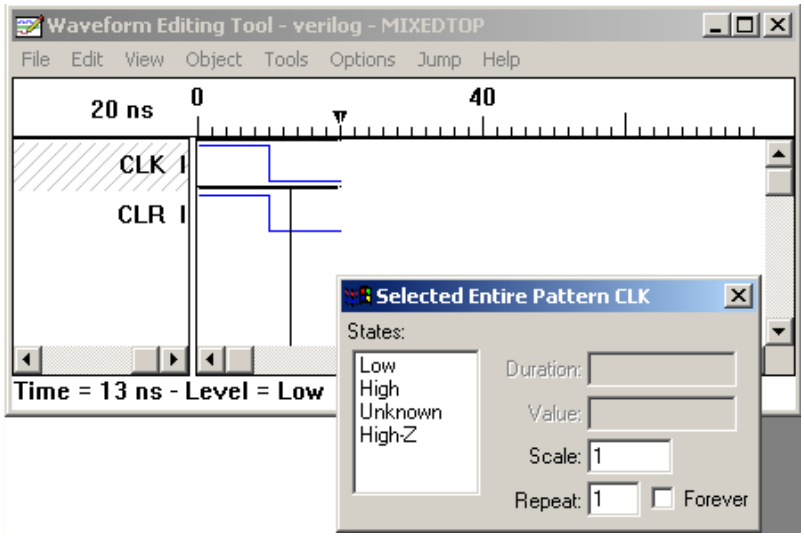
2. Select **View>Zoom In**.

   The pointer will change into a large Z.

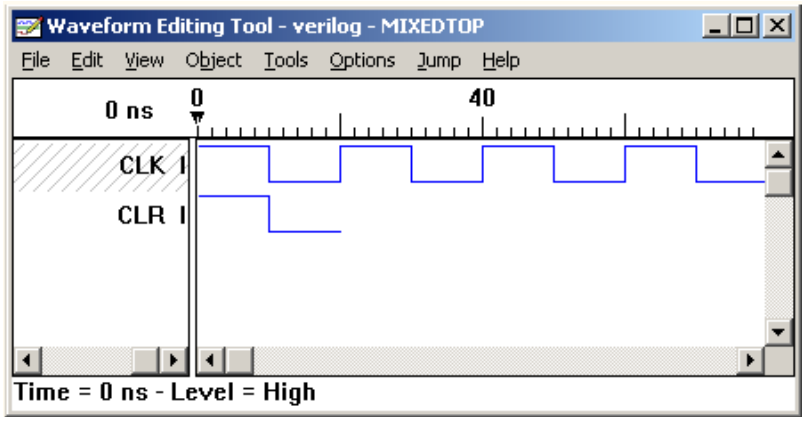
3. Click on the screen to zoom in until the scale matches the setting shown as follows.



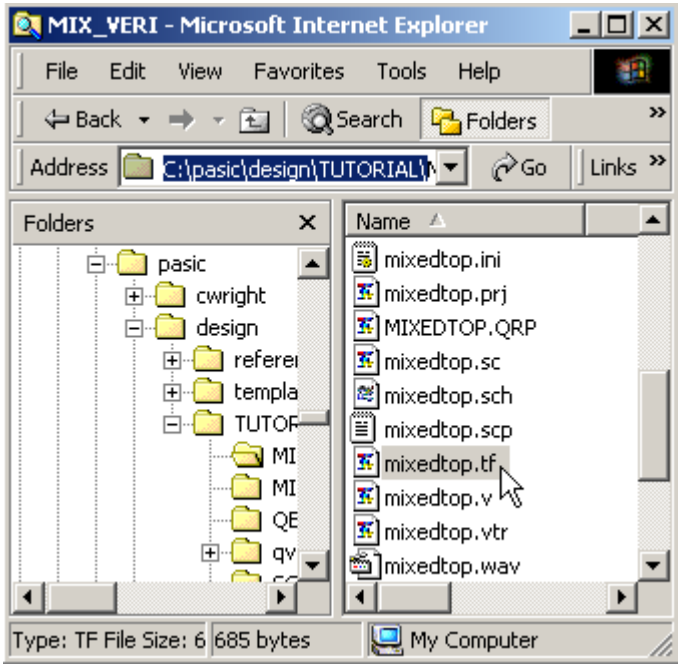
4. Right-click to discontinue the Zoom In function.
5. Click on **CLR** until it resembles the following screen.
6. Click on **CLK** until it resembles the following screen.
7. Check **Forever** in the Selected Entire Pattern CLK screen to create the clock waveform. Click on the line as shown to get the screen to appear.



The completed waveform will look as follows.



8. To save the waveform select **File>Save** which creates the file **mixedtop.tf**.
9. To verify that the `.tf` file was created, open Windows Explorer and go to `C:\pasic\design\TUTORIAL\MIX_VERI`. The `mixedtop.tf` file should be there.

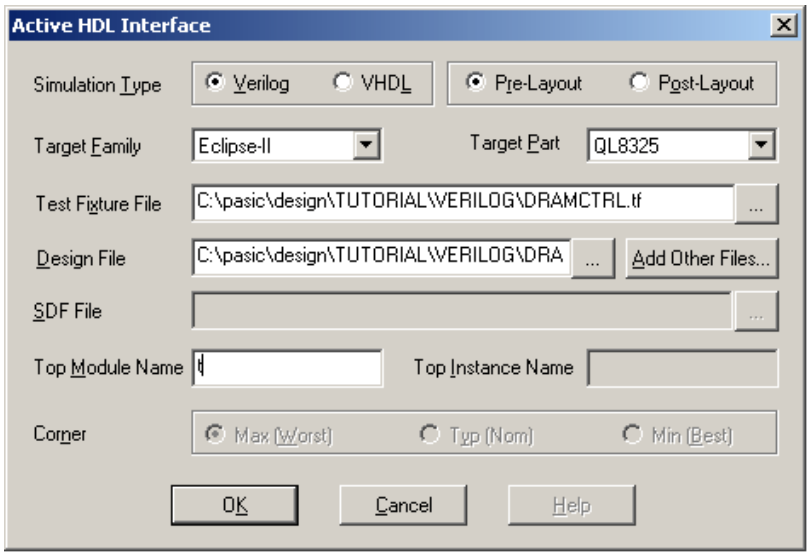


4.3.2 Launching Active-HDL

To launch Active-HDL:

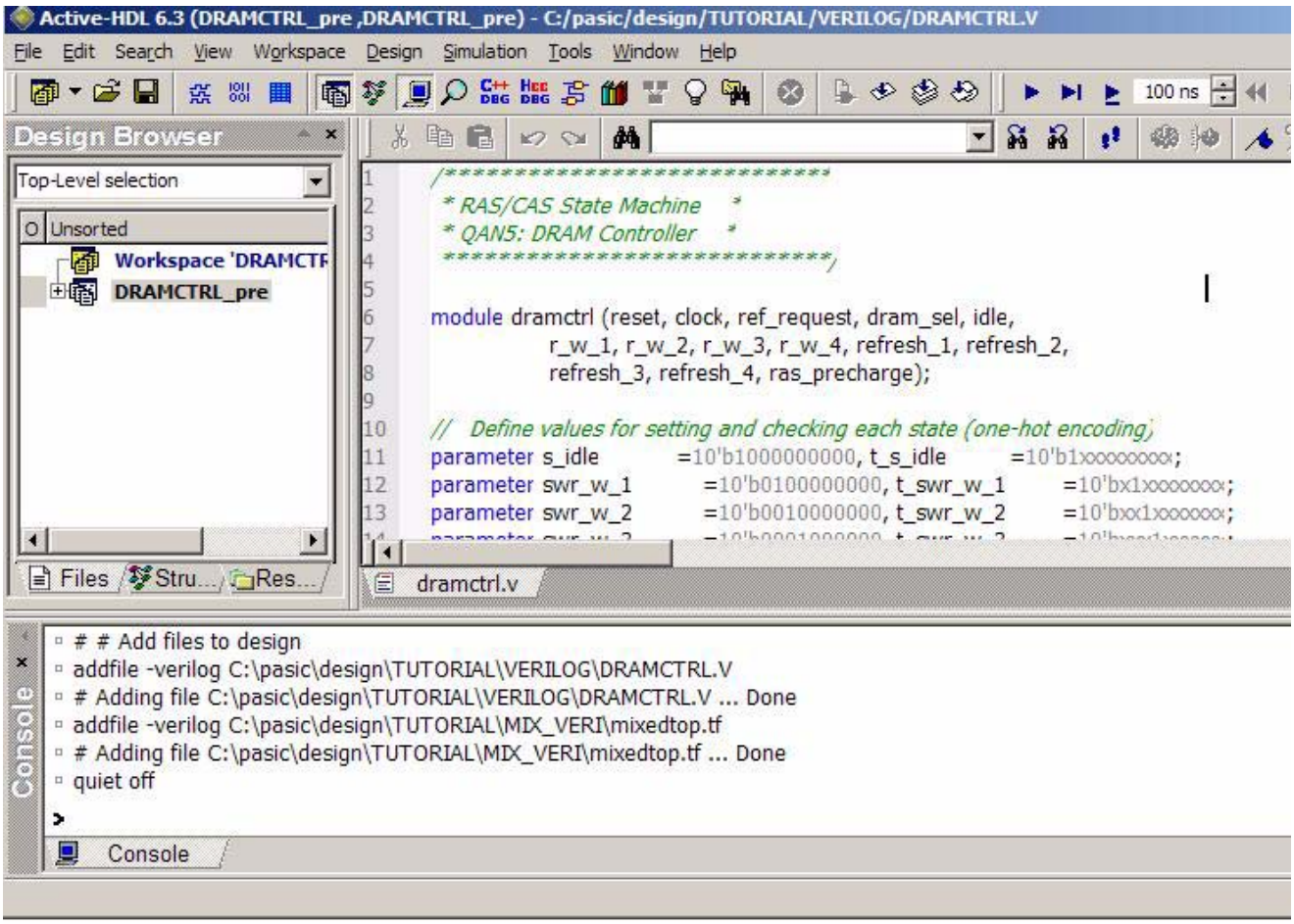
1. From the SpDE toolbar, click on the **Active-HDL Simulator** icon.

   The Active-HDL Interface screen is displayed.



2. Select **Verilog** and **Pre-Layout** for the Simulation Type.
3. Select **Eclipse II** as the Target Family and **QL8325** as the Target Part from the pull-down menus.
4. Browse to select `DRAMCTRL.tf` as the Test Fixture File and `DRAMCTRL.v` as the Design File located in the default directory `C:\pasic\design\TUTORIAL\VERILOG`.
5. Type `t` as the Top Module Name.
6. Click **OK**.

The Active HDL simulator creates a new workspace and adds all the simulation files. All files are compiled automatically and the top module is selected.



4.3.3 Running the Pre-Layout Simulation

To run the pre-layout simulation:

1. From the Active-HDL toolbar, click on the **New Waveform** icon.

   A new waveform is created.

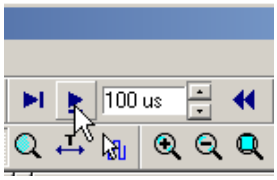
2. Right-click on the waveform and select **Add Signals**.

   The Add Signals screen is displayed.

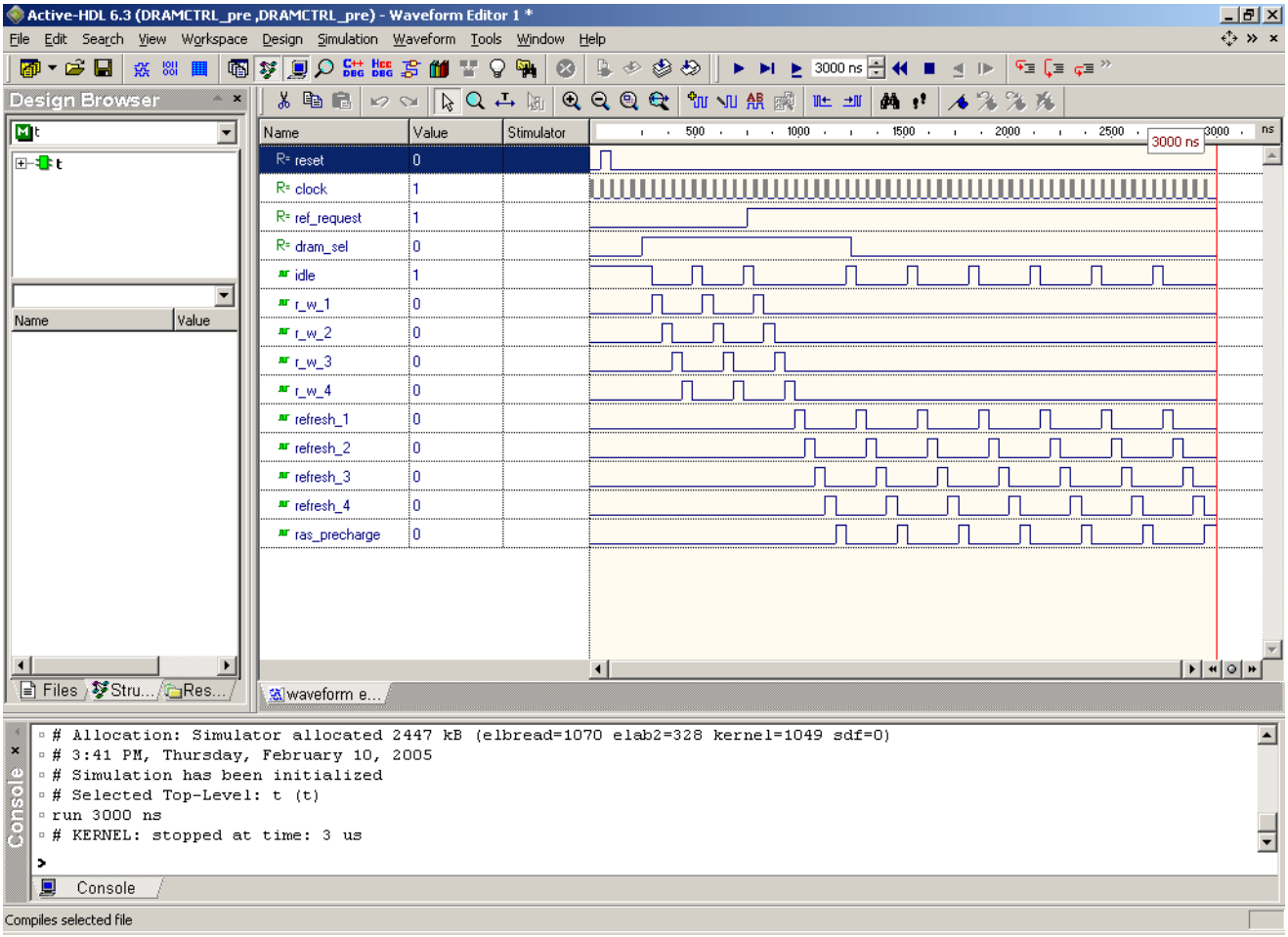
3. Select all signals on the right panel and click **Add** and **Close**.

   The signals are added to the waveform.

4. Expand the screen, in the menu bar type in **`100 us`** and then click the **Run** arrow to the left.



The output of the waveform counters are displayed.



5. After completing the simulation, exit Active-HDL.

4.4 Post-Layout Simulation Using Active-HDL

To perform a post-layout simulation for the design you have just created, you need to synthesize and perform back annotation to get the `.vq` and `.sdf` files:

4.4.1 Starting Synthesis

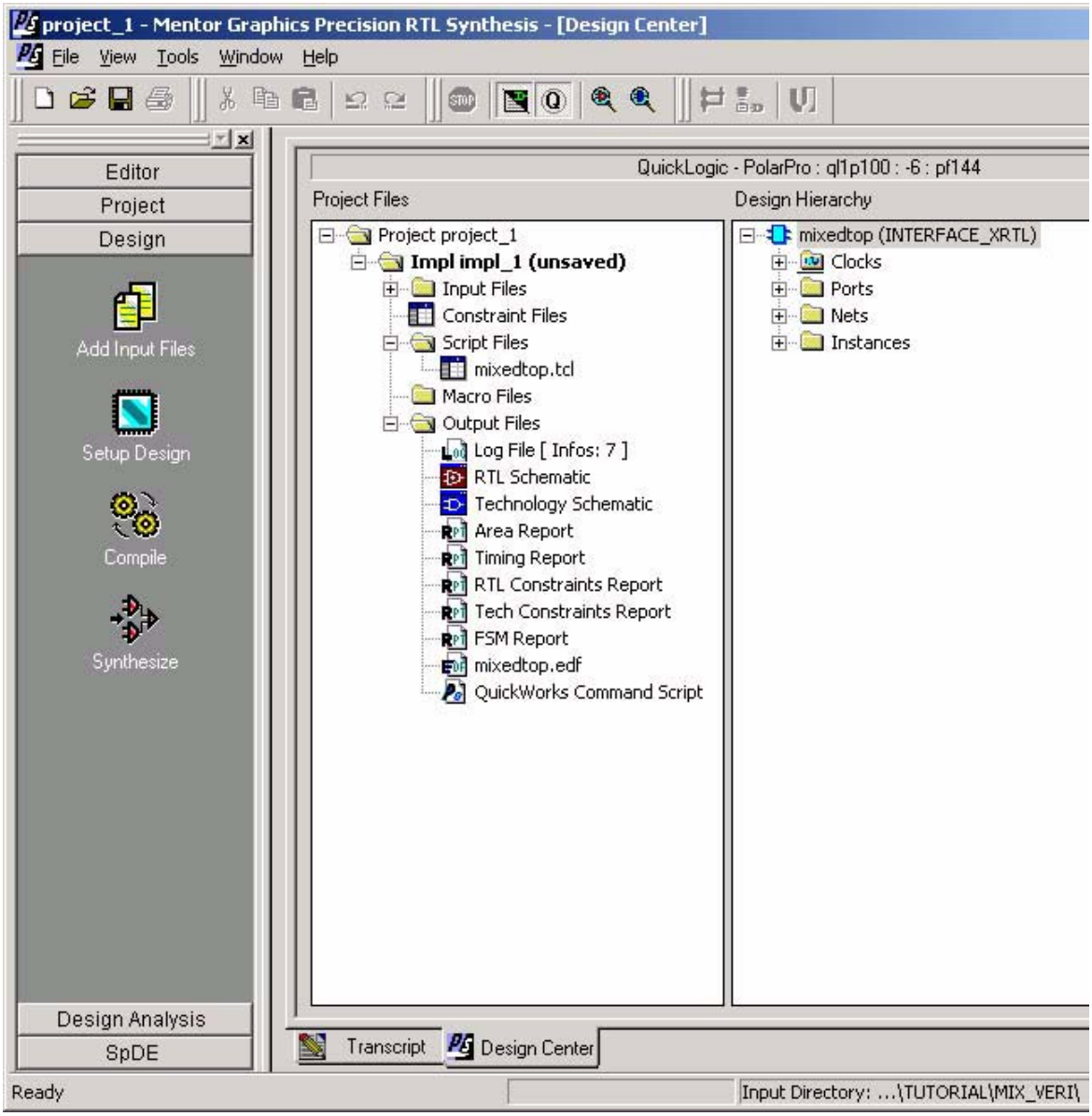
To start the synthesis tool:

1. From the SpDE menu bar, select **File>Import Precision**, or click the **Import Precision**  icon.

   The Open window is displayed.

2. Select the project (**mixedtop.v**) and click **Open**.

   The Precision RTL Synthesis screen is displayed and automatically generates a `.tcl` script to create a project file.



4.4.2 Running the Synthesis

To create the project and start synthesis:

1. Select the **Design** tab on the left side of the Precision RTL Synthesis screen.
2. Click **Add Input files** to add the Verilog file.
3. Click **Setup Design**.
   a. Select the desired product family from the Technology menu.
   b. Select the device from the Package menu.
3. Click **Compile** to compile the Verilog design files.
4. Click **Synthesis** to complete the design synthesis.

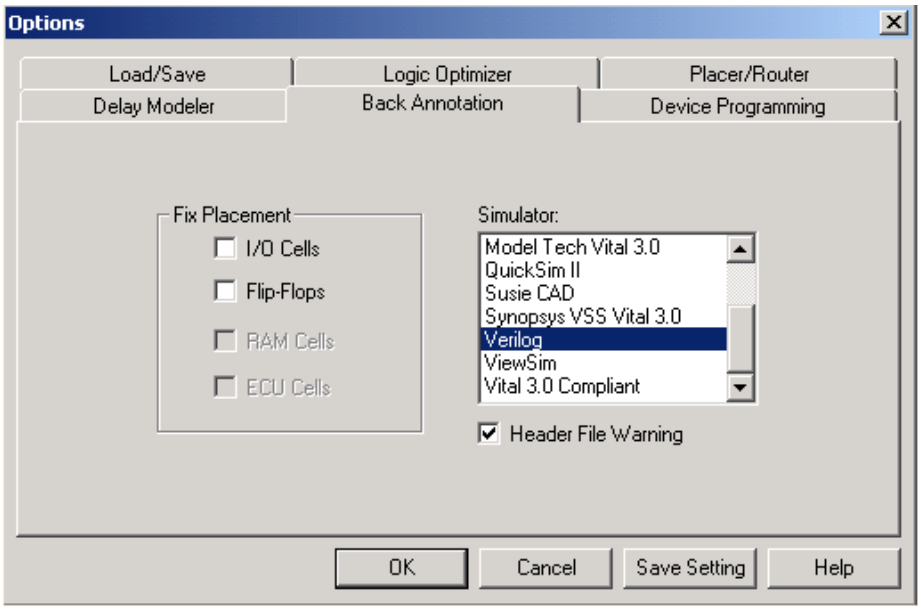
If there are errors, view the transcript log by clicking on the **Transcript** tab at the bottom of the screen.

5. Select **File>Exit** to quit Precision RTL and load the generated EDIF file.

4.4.3 Setting Options for Back Annotation

To set options for back annotation:

1. From the SpDE menu bar, select **Tools>Options.**
2. In the Tools Options dialog box, click on the **Back Annotation** tab. Select **Verilog** in the Simulator window. Click **Save Setting** and then **OK**.

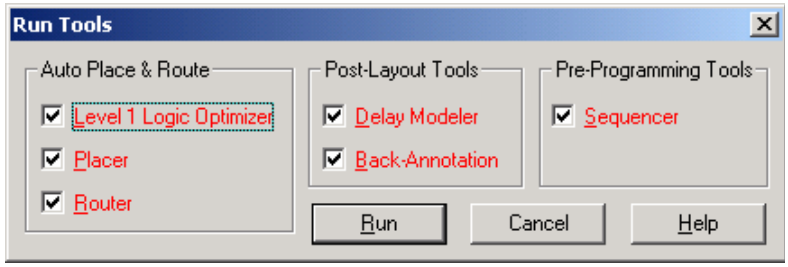


4.4.4 Selecting and Running Tools

To select and run tools:

1. From the SpDE menu bar, select **Tools>Run Selected Tools,** or click the icon.

   The Run Tools window is displayed.



2. Click **Run**.
3. Verify the creation of the `mixedtop.vq` and `mixedtop.sdf` files in `C:\pasic\design\TUTORIAL\MIX_VERI`.

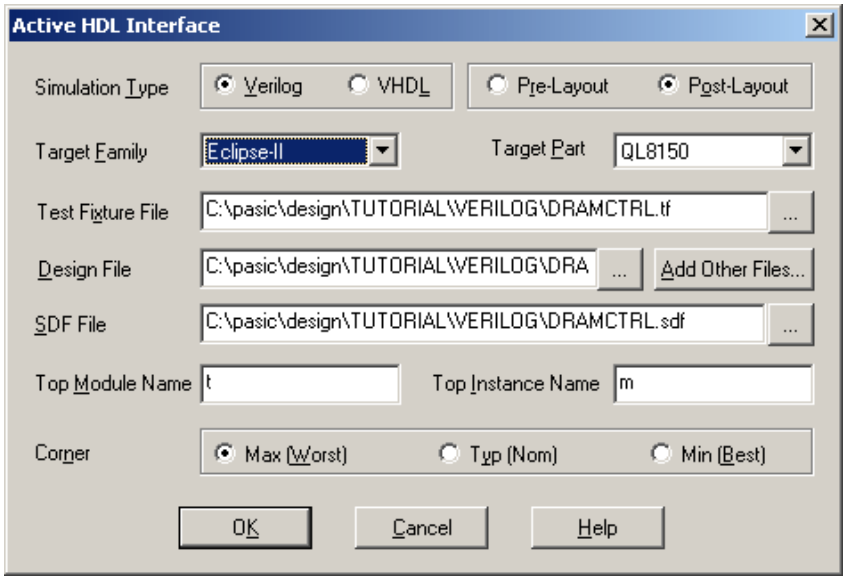
4.4.5 Using Active-HDL Design for Post-Layout Simulation

The timing (post-layout) simulation is similar to the functional simulation, which you did earlier in this tutorial.

NOTE: Before performing the post-layout simulation, be sure that you have exited from the pre-layout simulation and closed Active-HDL. Otherwise, the program will not function properly.

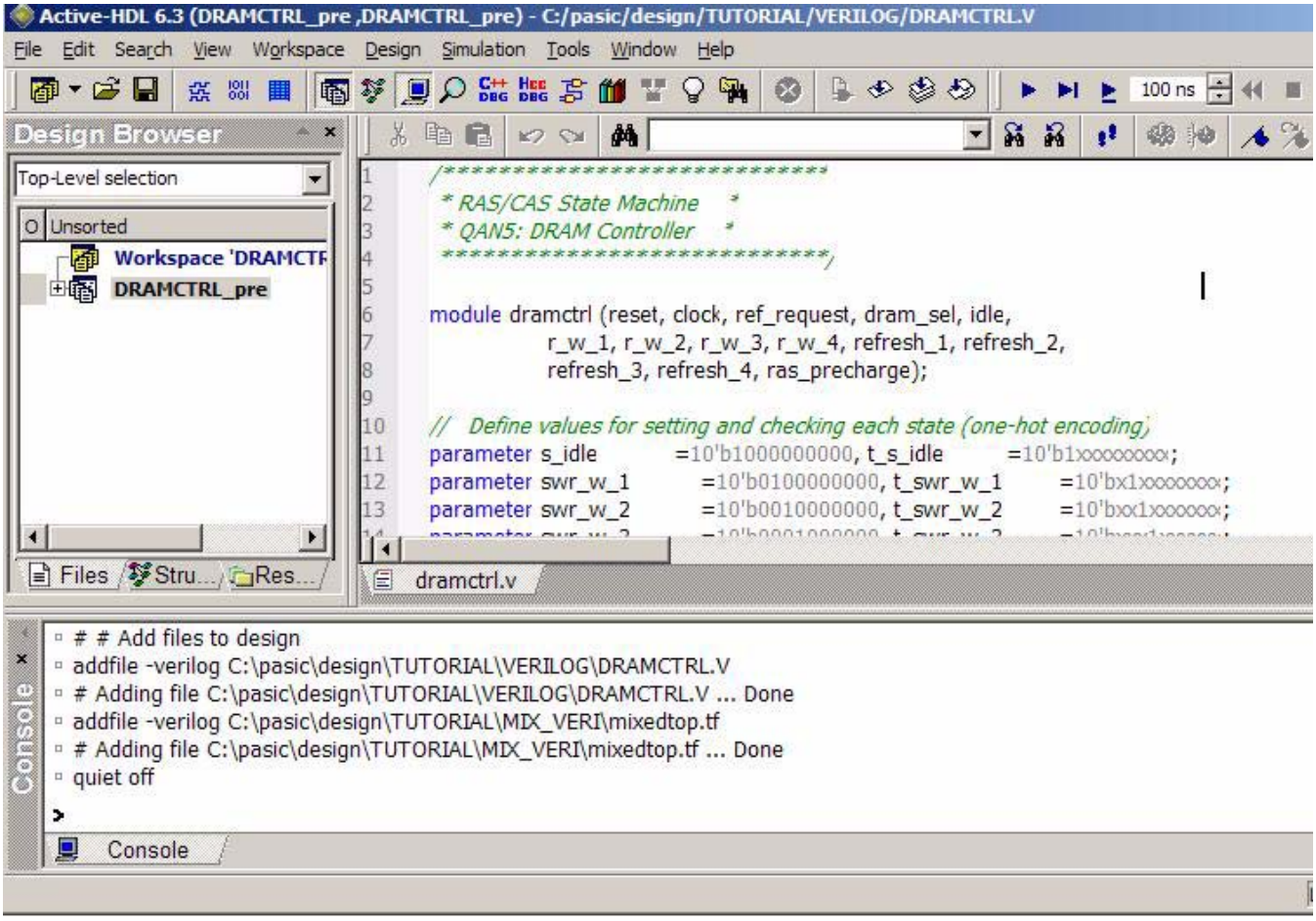
1. From the SpDE toolbar, click on the **Active-HDL Simulator** icon.

   The Active-HDL Interface screen is displayed with most of the information included.



2. Type **t** for the Top Module Name and **m** for the Top Instance Name.
3. Click **OK**.

The Active HDL simulator creates a new workspace and adds all the simulation files. All files are compiled automatically and the top module is selected.



4.4.6 Running the Post-Layout Simulation

To run the post-layout simulation:

1. From the Active-HDL toolbar, click on the **New Waveform** icon.

   A new waveform is created.

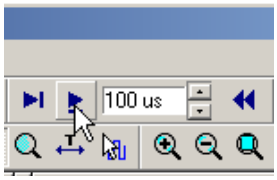
2. Right-click on the waveform and select **Add Signals**.

   The Add Signals screen is displayed.

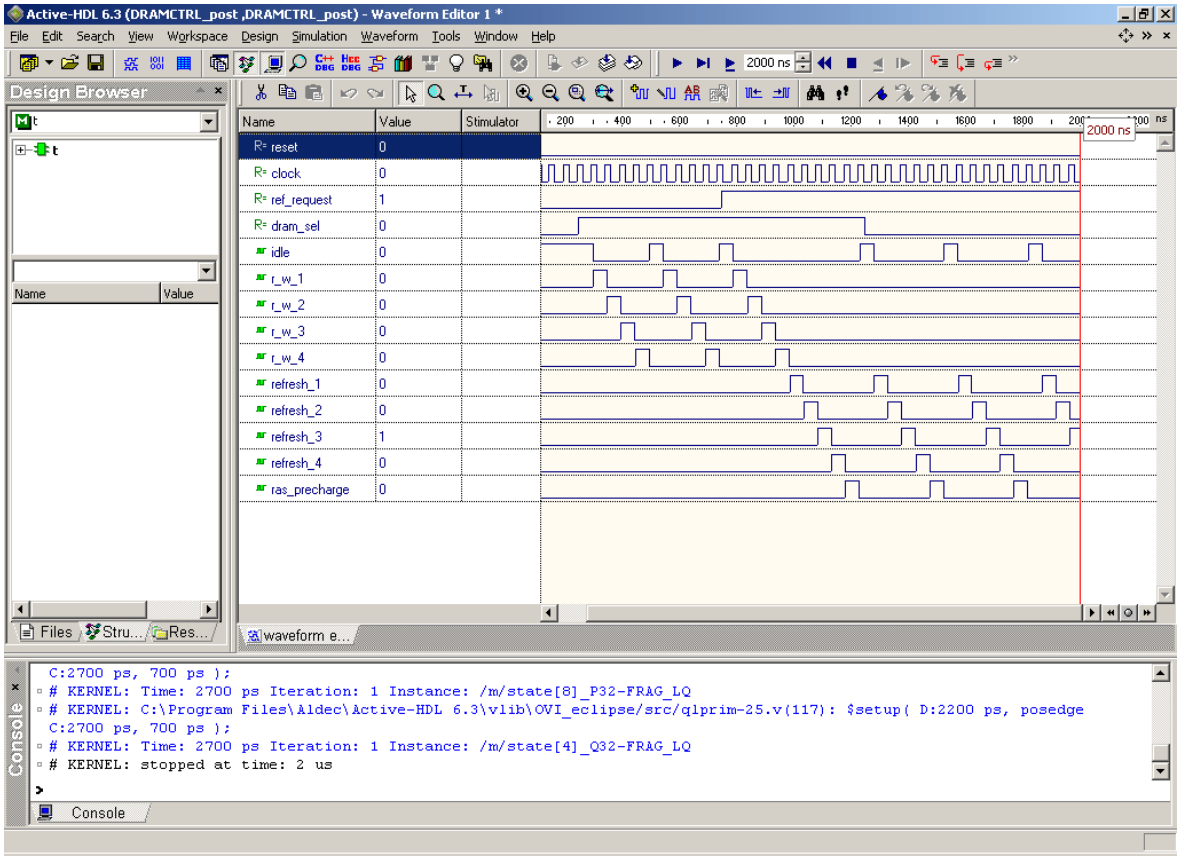
3. Select all signals on the right panel and click **Add** and **Close**.

   The signals are added to the waveform.

4. Expand the screen, in the menu bar type in **`100 us`** and then click the **Run** arrow to the left.



The output waveform should look as follows.



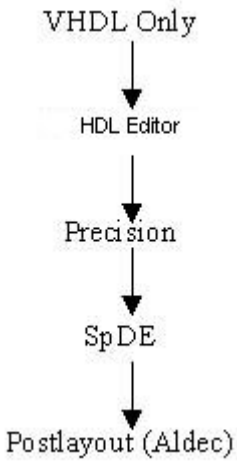
Chapter 5
VHDL-Only Design Tutorial

This tutorial describes the VHDL design using Precision RTL Synthesis and Active-HDL Simulator. For a more detailed information on Active-HDL Simulator, refer to the products' user manuals included with QuickWorks, or the specific tool's user manual, if you are using RTL Synthesis, Model Technology's V System, Synopsys' VSS or another VITAL compliant VHDL simulator.

This chapter contains the following sections:

5.1 Functional Overview

Figure 5-1: Simulation With VHDL Simulator
(Recommended Flow for VHDL Design and Optional Simulation Flow)



The Active-HDL simulator is included in QuickWorks. If you have Model Technology's V System, Synopsys' VSS, or some other third-party VHDL simulator, you can use that for true VHDL behavioral simulation. You will then use Precision RTL to synthesize the design, and use SpDE for place and route, and then use a VITAL-VHDL compliant third-party VHDL simulator for full timing simulation as shown in **Figure 5-1 on page 143**.

NOTE: This tutorial assumes that you understand the basic operation of Microsoft Windows. Although knowledge of VHDL is not necessary for this tutorial, due to the complexity of VHDL, some formal training in VHDL is highly recommended for doing actual designs.

For VHDL-only design flow use the VHDL designs located on the default directory at `C:/pasic/design/VHDL/VOICE.VHD`.

5.2 Creating a Test Waveform

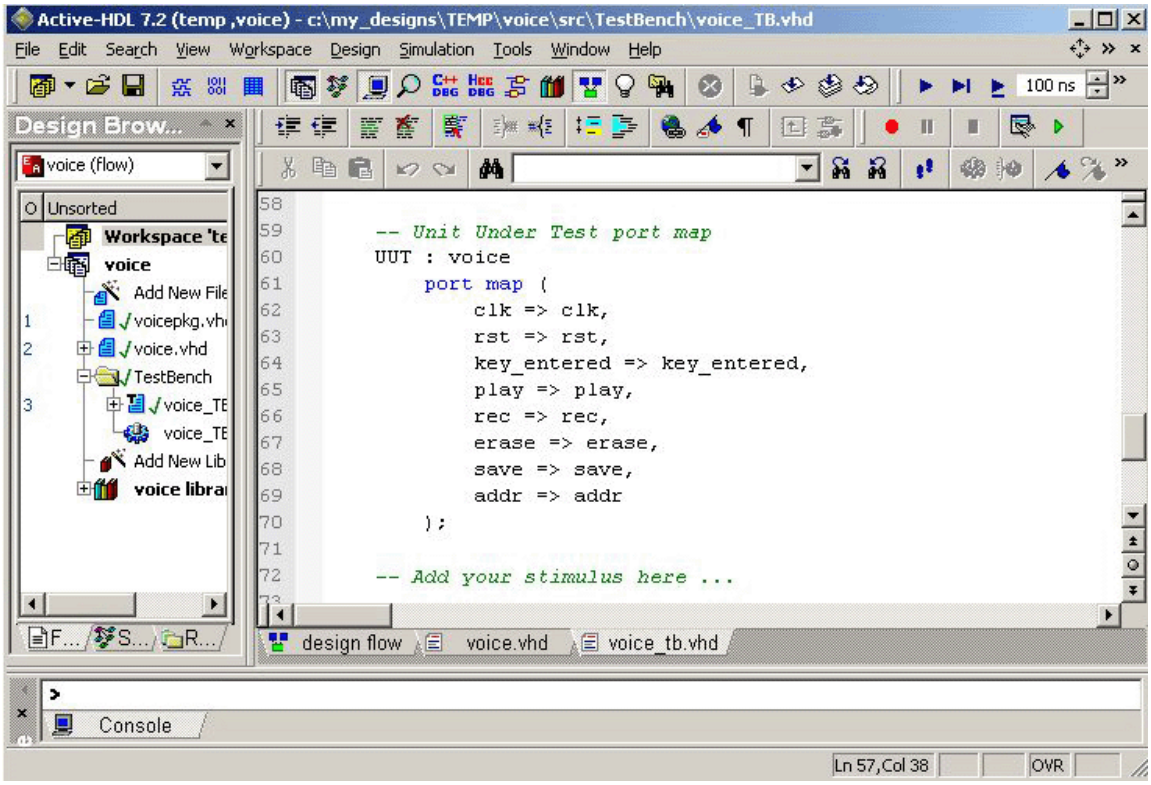
Before you can run a simulation on your VHDL design, you need to create input vectors (referred to as a test fixture or test bench) for your design.

If you are using Active-HDL Simulator or a third-party VHDL simulator for simulation, you will need to create your own VHDL test bench.

To create a VHDL test bench:

1. From the Active-HDL menu bar (with the `VOICE.VHD` design file displayed in the active window), select **Tools>Generate Test Bench**.

   A new file is created, `VOICE_TB.vhd`. This file can be used as a template to easily add input stimulus for your VHDL design. The newly created test bench for your design should now be displayed in a new window as follows.



2. Type the lines of VHDL code that are in boldface print. You can cut and paste the code from the VOICE_TB.vhd file located in your tutorial directory.

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE WORK.voicepkg.ALL;

ENTITY TestBench IS
END TestBench;

ARCHITECTURE HTWTestBench OF TestBench IS

COMPONENT voice
    PORT (clk,rst : IN std_logic;
                  key_entered : IN std_logic_vector(3 downto 0);
                  play,rec,erase,save,addr : OUT std_logic
                  );
END COMPONENT;

    SIGNAL clk,rst :  std_logic :='0';
           SIGNAL key_entered :  std_logic_vector(3 downto 0);
           SIGNAL play,rec,erase,save,addr :  std_logic;

BEGIN
          clk <= NOT clk after 20 ns;
          rst <= '1' after 20 ns,'0' after 40 ns;
          key_entered<=zero,--initialize vector;
                    one   after 90 ns,zero after 130 ns,
                    one   after 170 ns, zero after 210 ns,
                    two   after 250 ns,    zero after 290 ns,
                    three after 330 ns,    zero after 370 ns,
                    pound after 410 ns,    two   after 450 ns,
                    zero after 490 ns,    pound after 530 ns,
                    five after 570 ns,    pound after 610 ns,
                    zero after 650 ns,    zero after 690 ns,
                    zero after 710 ns;

    U1 : voice PORT MAP (clk,rst,key_entered,play,rec,erase,save,addr);
END HTWTestBench;

CONFIGURATION config_voice_tb OF testbench IS
FOR HTWTestBench
END FOR;
END config_voice_tb;
```

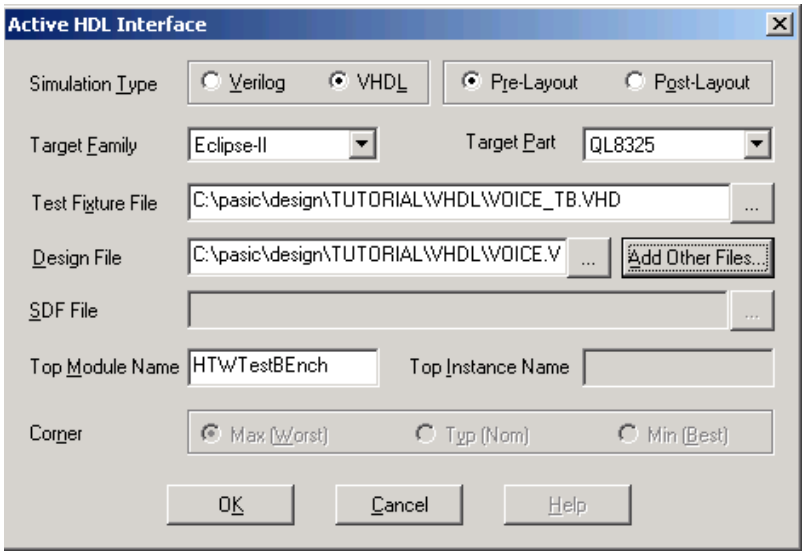
3. Select **File>Save**.
4. Select **File>Exit** to quit Active-HDL.

5.3 Pre-Layout Simulation Using Active-HDL

To launch Active-HDL:

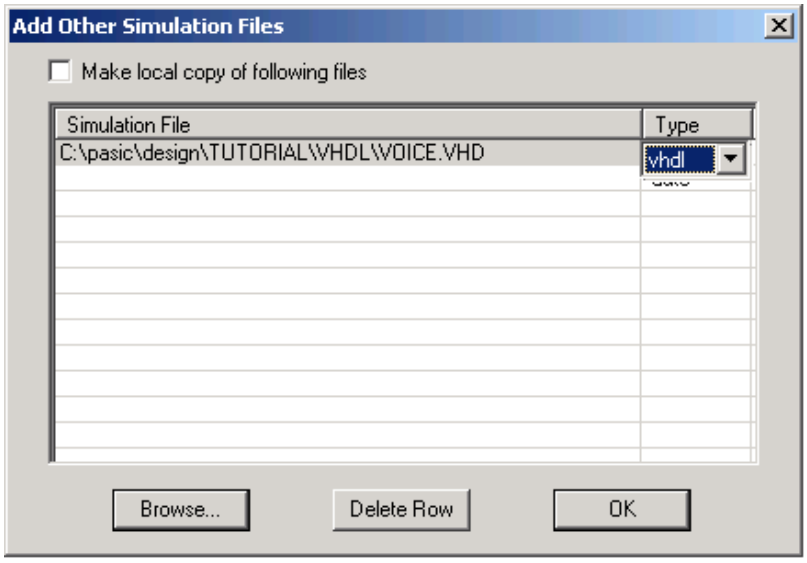
1. From the SpDE toolbar, click on the **Active-HDL Simulator** icon.

   The Active-HDL Interface dialog box is displayed.



2. Select **VHDL** and **Pre-Layout** for the Simulation Type.
3. Select **Eclipse II** as the Target Family and **QL8325** as the Target Part from the pull-down menus.
4. Browse to select `VOICE_TB.VHD` as the Test Fixture File and `VOICE.V` as the Design File located in the default directory `C:\pasic\design\TUTORIAL\VHDL`.
5. Type `HTWTestBEnch` as the Top Module Name.
6. Click **Add Other Files...**.

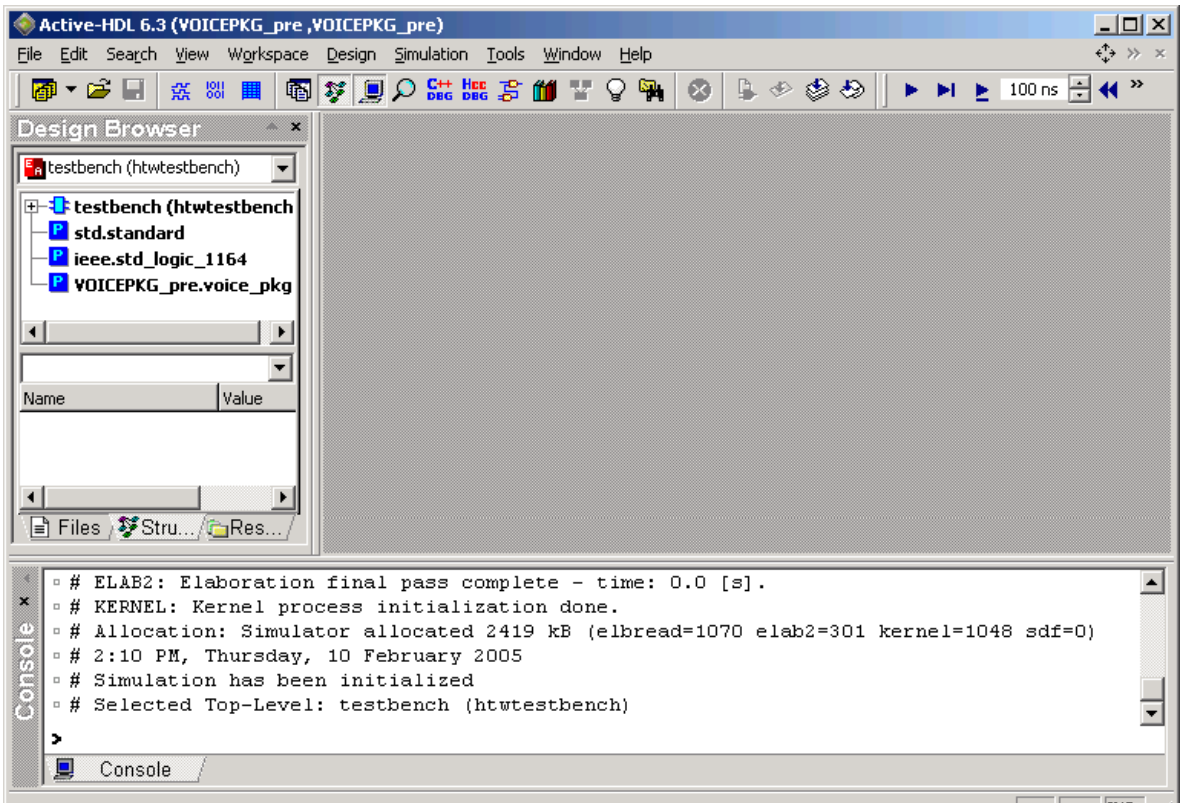
The Add Other Simulation Files screen is displayed.



7. Click to highlight the first line and then click **Browse** to add the file `VOICE.VHD` located in the default directory `C:\pasic\design\TUTORIAL\VHDL`.
8. Select **vhdl** from the Type pull-down menu.
9. Click **OK.**

   The Active HDL Interface screen is displayed.
10. Click **OK**.

The Active HDL simulator creates a new workspace and adds all the simulation files. All files are compiled automatically and the top module is selected.



5.3.1 Running the Pre-Layout Simulation

To run the pre-layout simulation:

1. From the Active-HDL toolbar, click on the **New Waveform** icon.

   A new waveform is created.

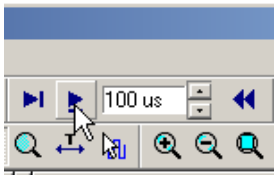
2. Right-click on the waveform and select **Add Signals**.

   The Add Signals screen is displayed.

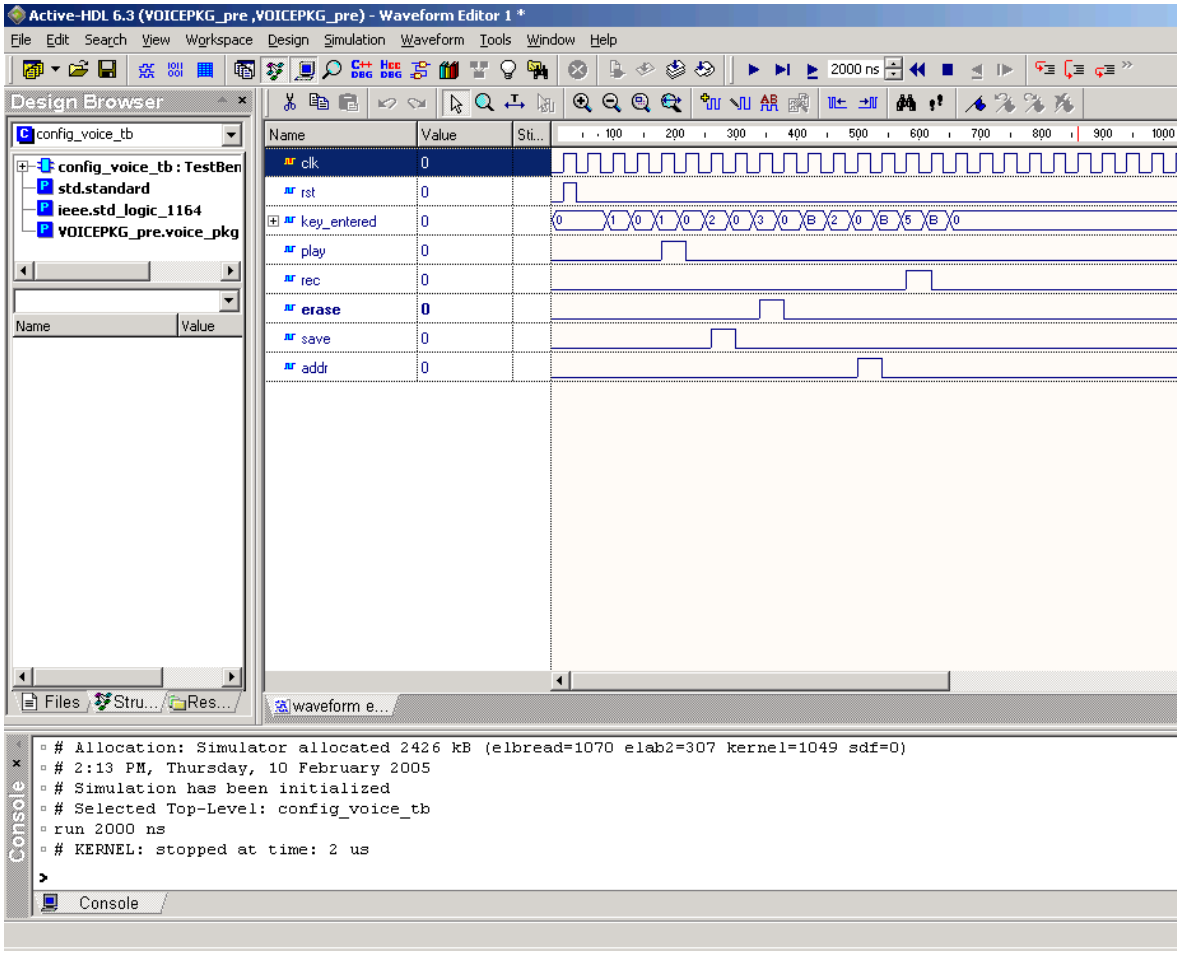
3. Select all signals on the right panel and click **Add** and **Close**.

   The signals are added to the waveform.

4. Expand the screen, in the menu bar type in **`100 us`** and then click the **Run** arrow to the left.



The output of the waveform counters are displayed.



5. After completing the simulation, exit Active-HDL.

5.4 Post-Layout Simulation Using Active-HDL

To perform a post-layout simulation for the design you have just created, you need to synthesize the design and run the automatic place and route.

5.4.1 Starting Synthesis

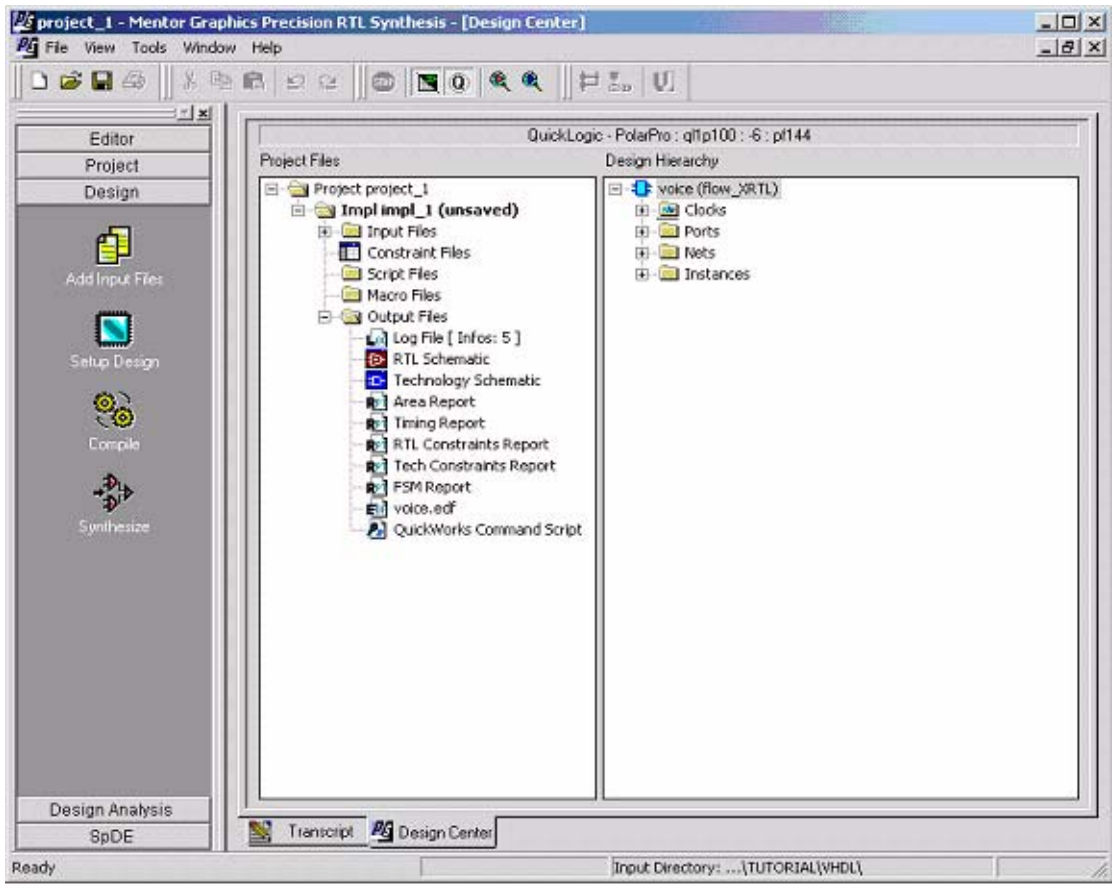
To start the synthesis tool:

1. From the SpDE menu bar, select **File>Import Precision**, or click the **Import Precision** icon.

   The Open window is displayed.

2. Select **VOICE.VHD** and click **Open**.

   The Precision RTL Synthesis screen is displayed. Precision RTL automatically generates a `.tcl` script to create a project file and adds the selected VHDL file.



5.4.2 Running the Synthesis

To create the project and start synthesis:

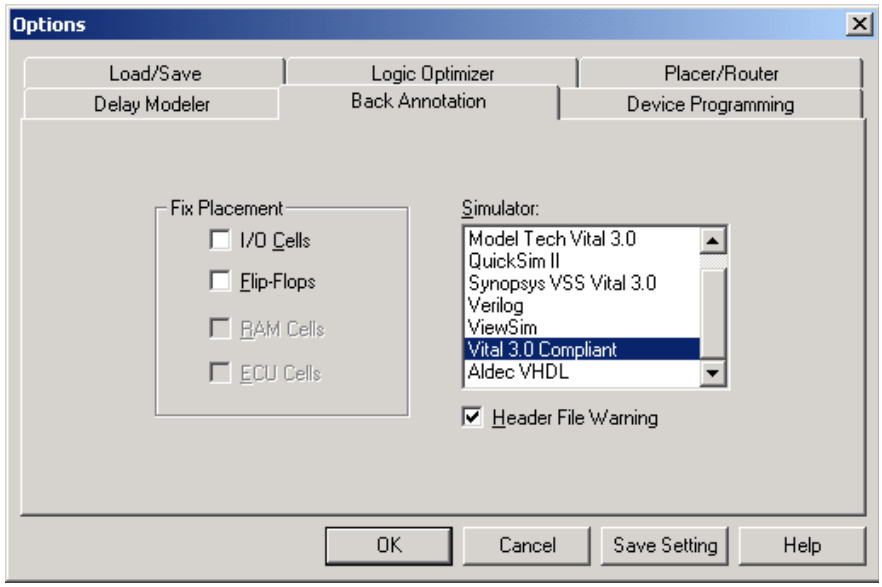
1. Select the **Design** tab on the left side of the Precision RTL Synthesis screen.
2. Click **Add Input files** to add the VHDL file.
3. Click **Setup Design**.
   a. Select the desired product family from the Technology menu.
   b. Select the device from the Package menu.
3. Click **Compile** to compile the VHDL design files.
4. Click **Synthesis** to complete the design synthesis.

   If there are errors, view the transcript log by clicking on the **Transcript** tab at the bottom of the screen.
5. Select **File>Exit** to quit Precision RTL and load the generated EDIF file.

5.4.3 Setting Options for Back Annotation

To set options for back annotation:

1. From the SpDE menu bar, select **Tools>Options.**
2. In the Tools Options dialog box, click on the **Back Annotation** tab. Select **VITAL 3.0 Compliant** in the Simulator window. Click **Save Setting** and **OK**.



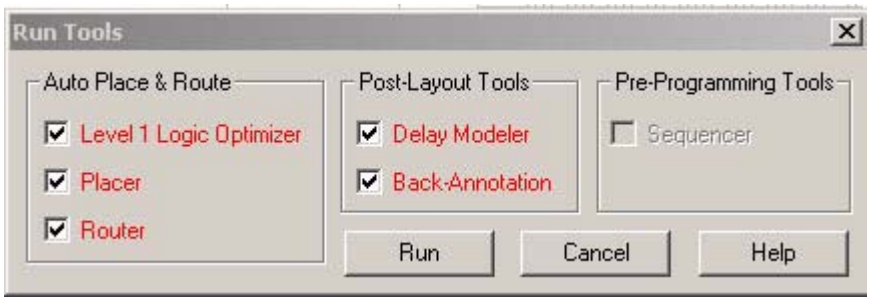
SpDE will produce a VITAL compliant netlist with `.vhq` extension, and a delay file with the `.sdf` extension when the back annotation tool is run. After you have set your simulator option, you are ready to run the tools.

5.4.4 Selecting and Running Tools

To select and run tools:

1. From the SpDE menu bar, select **Tools>Run Selected Tools,** or click the  icon.

   The Run Tools window is displayed.



2. Click **Run**.
3. Verify the creation of the `voice.vhq` and `voice.sdf` files in `C:\pasic\design\TUTORIAL\VHDL`.
4. To continue, click **No**.

   You will now be able to view the physical implementation of your design.
5. Select **View>Full Fit** to see the entire device, or use the **View>Zoom In** and **Zoom Out** commands to see any section in more detail.
6. Select **File>Save** to save a chip file (extension `.CHP`) for your design. This chip file contains all the place and route information for your design.

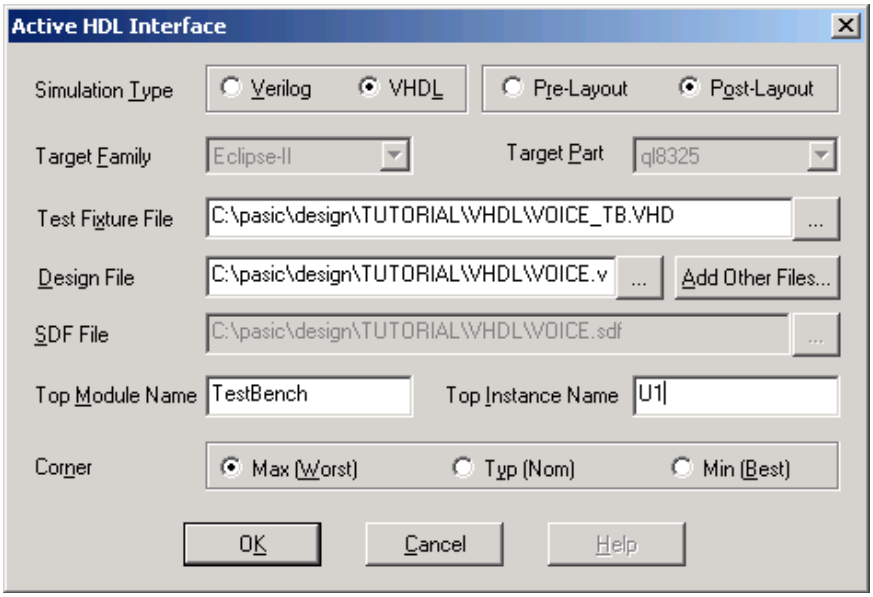
5.4.5 Using Active-HDL for Post-Layout Simulation

The timing (post-layout) simulation is similar to the functional simulation, which you did earlier in this tutorial.

NOTE: Before performing the post-layout simulation, be sure that you have exited from the pre-layout simulation and closed Active-HDL. Otherwise, the program will not function properly.

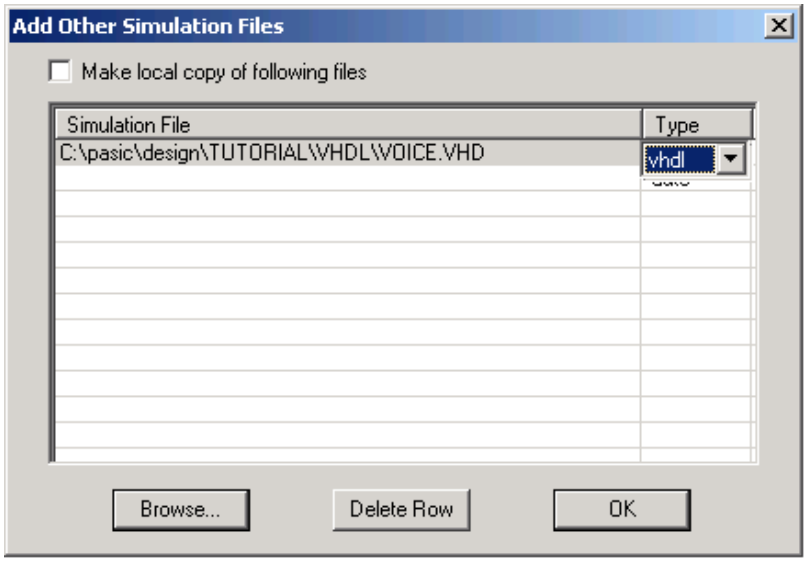
1. From the SpDE toolbar, click on the **Active-HDL Simulator** icon.

   The Active-HDL Interface screen is displayed with most of the information included.



2. Type **`Test Bench`** for the Top Module Name and **U1** for the Top Instance Name.
3. Click **Add Other Files...**.

   The Add Other Simulation Files screen is displayed.

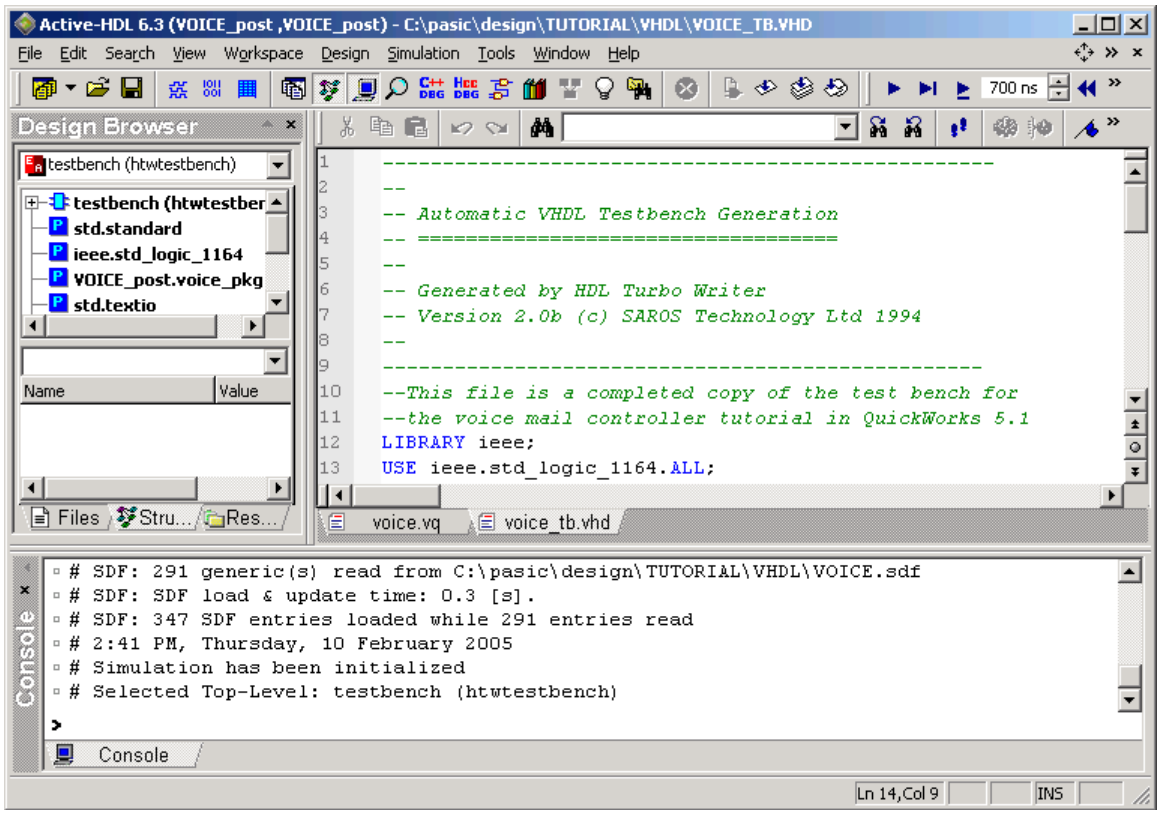


4. Click to highlight the first line and then click **Browse** to add the file `VOICE.VHD` located in the default directory `C:\pasic\design\TUTORIAL\VHDL`.
5. Select **vhdl** from the Type pull-down menu.
6. Click **OK.**

   The Active HDL Interface screen is displayed.

7. Click **OK**.

   The Active HDL simulator creates a new workspace and adds all the simulation files. All files are compiled automatically and the top module is selected.



5.4.6 Running the Post-Layout Simulation

To run the post-layout simulation:

1. From the Active-HDL toolbar, click on the **New Waveform** icon.

   A new waveform is created.

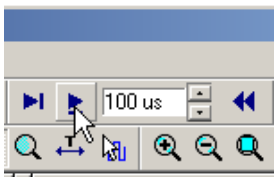
2. Right-click on the waveform and select **Add Signals**.

   The Add Signals screen is displayed.

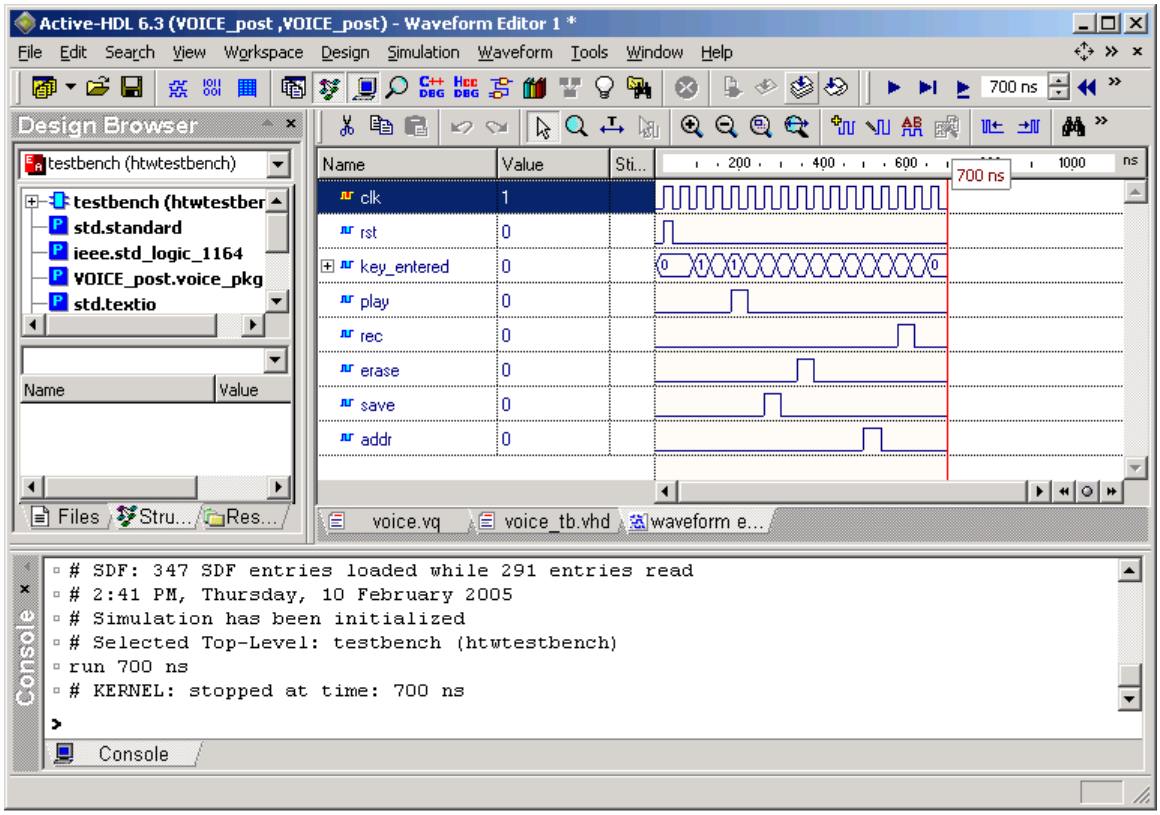
3. Select all signals on the right panel and click **Add** and **Close**.

   The signals are added to the waveform.

4. Expand the screen, in the menu bar type in **`100 us`** and then click the **Run** arrow to the left.



The output waveform should look as follows.



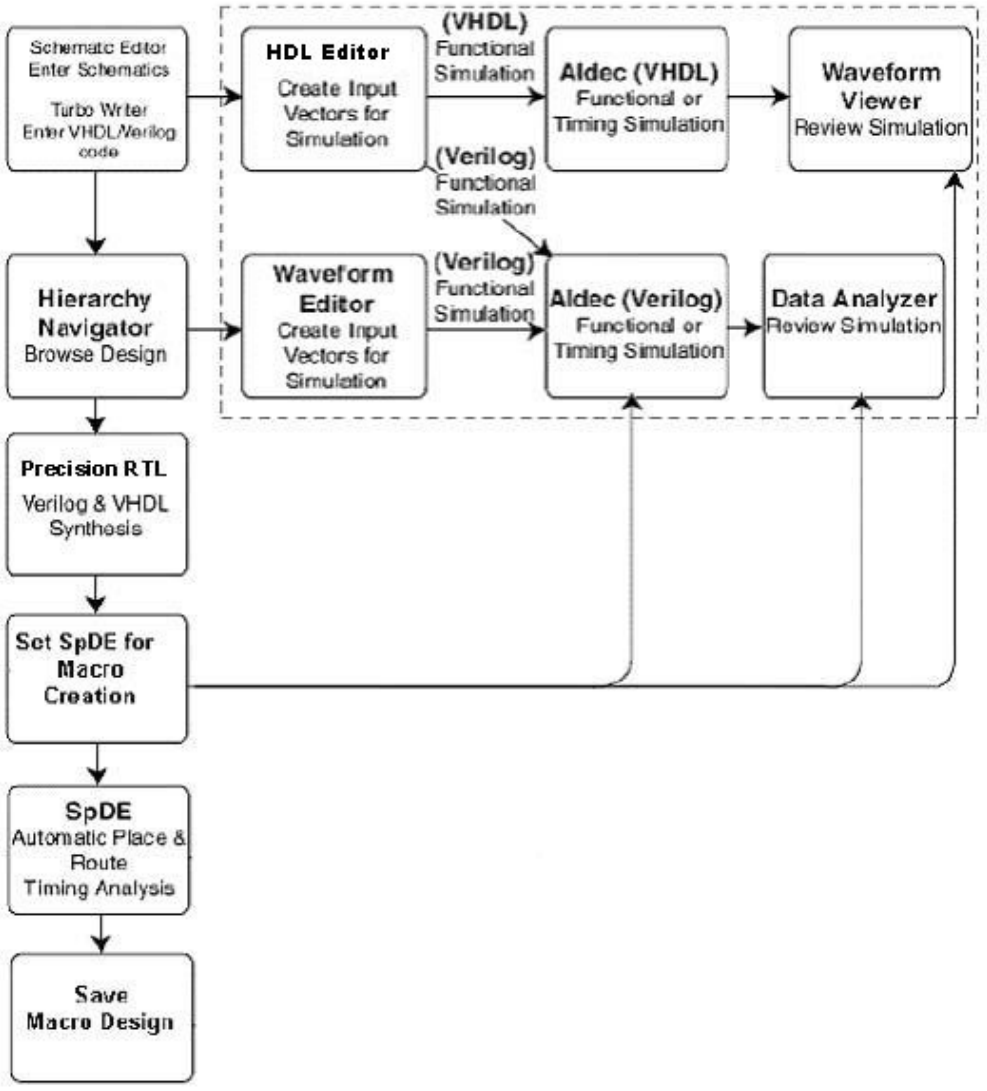
Chapter 6
Macro Tutorial

This chapter contains the following sections:

6.1 Macro Design Tutorial

This section provides a tutorial of the QuickWorks Macro design process, as shown in **Figure 6-1**. To become familiar with the macro design process, you will create a schematic containing a simple 16-bit `counter16` and `adder16` design.

Figure 6-1: Schematic Entry Macro Design Flow



As the design flow chart in **Figure 6-1** illustrates, in this tutorial you will perform the following functions:

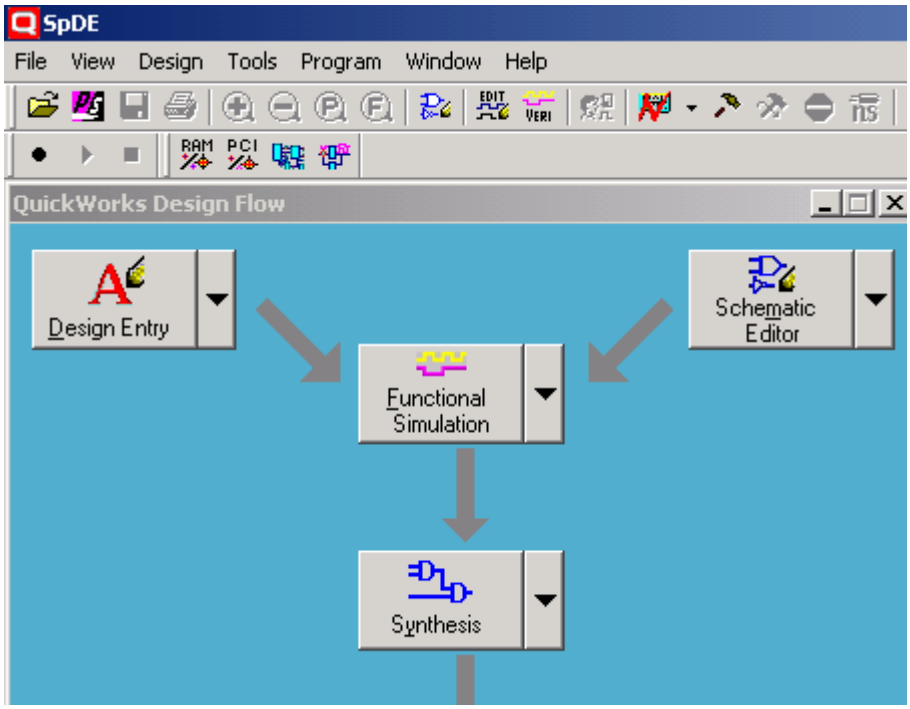
- Launch SpDE
- Launch Schematic Editor & Navigator to create and inspect the design
- Export the Verilog Functional Simulation Netlist
- Simulate the design for functionality using the Aldec Simulation Environment
- View the simulation results
- Set SpDE for Macro creation
- Specifiy constraint for I/Os to be part of macro:
  - set macro int net–pin <netname>
  - set macro int net–pin <netname>
  - set macro int net–pin <netname>
- Specify constraint for macro interface I/Os:
  - set macro int net <netname>
  - set macro int net <netname>
  - set macro int net <netname>
  - set macro int net <netname>
- Create and load a QDIF/EDIF Netlist into SpDE, where the design will be automatically optimized, placed and routed
- Simulate the design for timing using Aldec Simulation Environment (post-layout simulation)
- Review the results
- Save the Macro design

6.1.1 Entering a Schematic Design

To enter a schematic design:

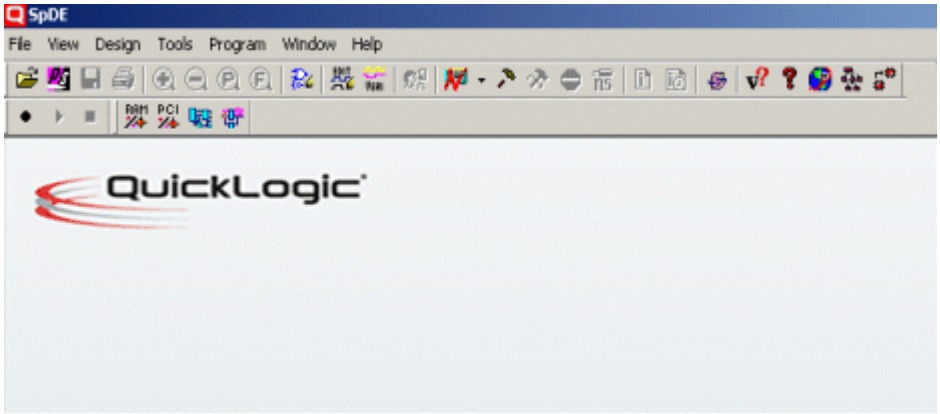
1. Select **Start>Programs>QuickLogic>SpDE**, or click the **SpDE** icon on your desktop.

The SpDE window is displayed and all of the QuickWorks design resources are now available for use.



2. Close the QuickWorks Design Flow window by clicking the **X** in the upper right corner. This method of design will not be used for this tutorial.

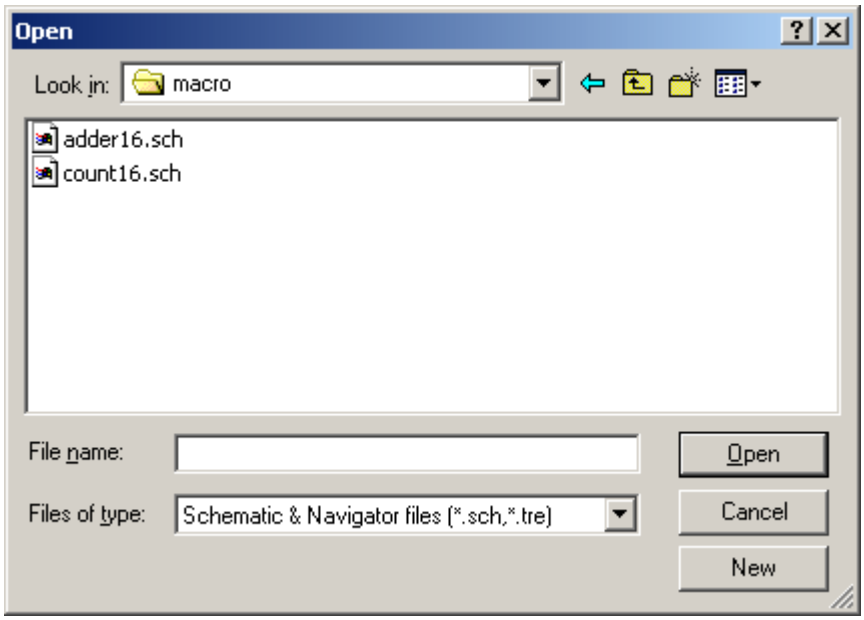
   The SpDE window is displayed. The SpDE toolbar contains icon buttons for executing commands quickly. The status bar at the bottom of the SpDE window displays status messages periodically



NOTE: See the SpDE Menu Command Reference chapter of the *QuickWorks User Manual* for a full explanation of all available icons.

3. From the SpDE menu bar, select **Design>Schematic Editor & Navigator**, or click the  icon.

The Open window is displayed.



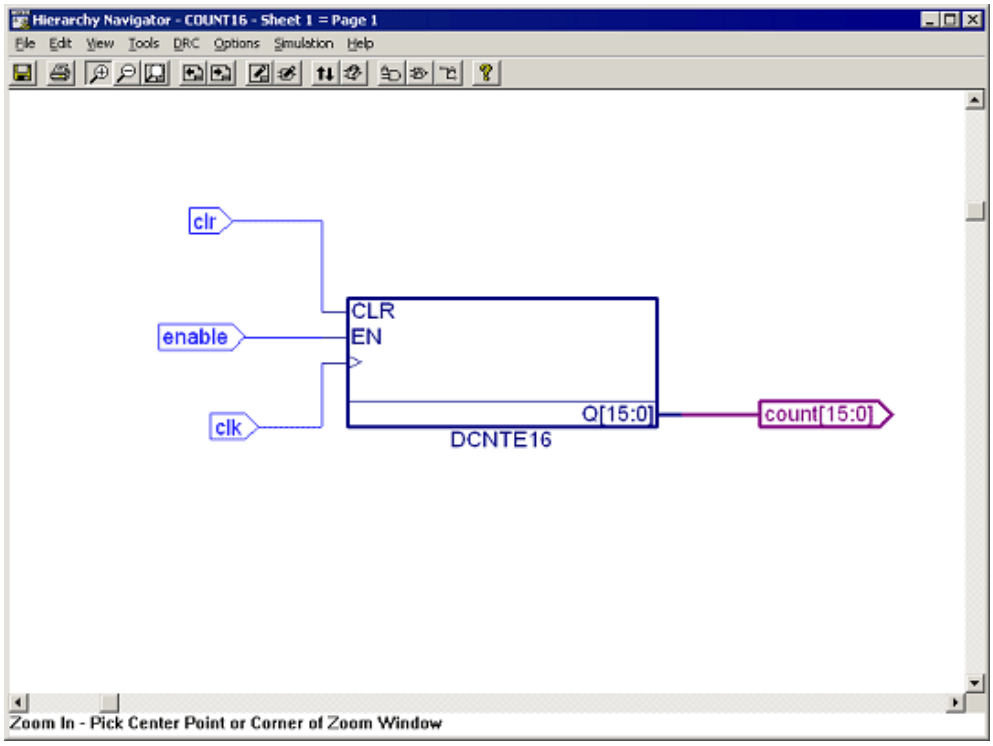
4. Navigate to default directory `C:\pasic\design\TUTORIAL\mac\macro\`, select **count16.sch**, and click **Open**.

   The Hierarchy Navigator window is displayed.

   NOTE: For more details about using schematic tools refer to the schematic based design flow.

5. From the Hierarchy Navigator menu bar, select **View>Full Fit**. Click anywhere within the schematic page to perform this operation.

The Hierarchy Navigator displays the completed design.



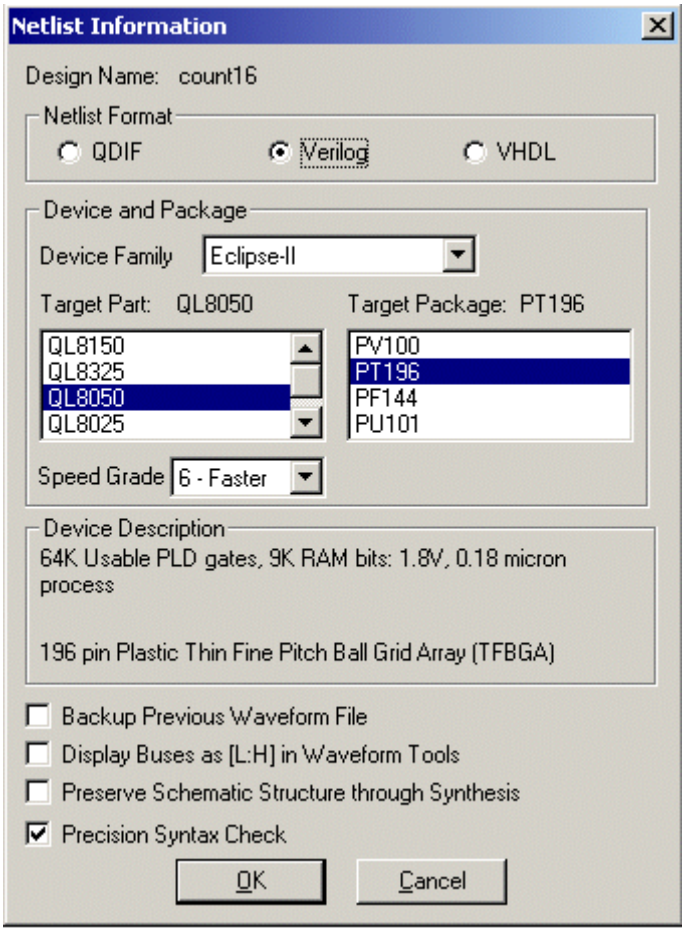
6.1.2 Exporting a Design to a Verilog Functional Simulation Netlist

The design will now be simulated to verify the functionality. To run a pre-layout simulation, a Verilog or VHDL netlist must be generated. This netlist can be used in Aldec Verilog Simulator.

To generate a Verilog netlist:

1. From the Hierarchy Navigator menu bar, select **Tools>Export QuickLogic**.

The Netlist Information dialog box is displayed.



2. Select **Verilog** as the Netlist Format.
3. Select **Eclipse II** as the Device Family.
4. Select **QL8050** as the Target Part.
5. Select **PT196** as the Target Package.
6. Click **OK**.

   The Pre-layout Information window is displayed.
7. Click **Done**.
8. From the Hierarchy Navigator menu bar, select **File>Save**.

6.1.3 Simulating the Design for Functionality

Refer to section **Section 4.3, "Pre-Layout Simulation Using Active-HDL for Verilog," on page 130** for more details about using schematic based design flow.

6.1.4 Using SpDE for Macro Creation

To begin the macro creation mode:

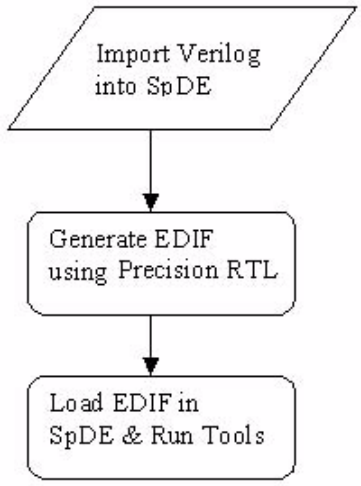
1. From the SpDE menu bar, select **Tools>Macro Creation Mode**, or click the **Macro Creation Mode** icon, or press **Ctrl+Alt+M**.

6.1.5 Creating and Loading a QDIF/EDIF

As shown in **Figure 6-2**, the QDIF/EDIF design flow consists of:

1. Importing the Verilog file to SpDE.
2. Selecting the part and package in Precision RTL before compiling.
3. Generating the EDIF Netlist.
4. Loading the Netlist into SpDE.
5. Running the tools until back annotation.

Figure 6-2: EDIF Design Flow

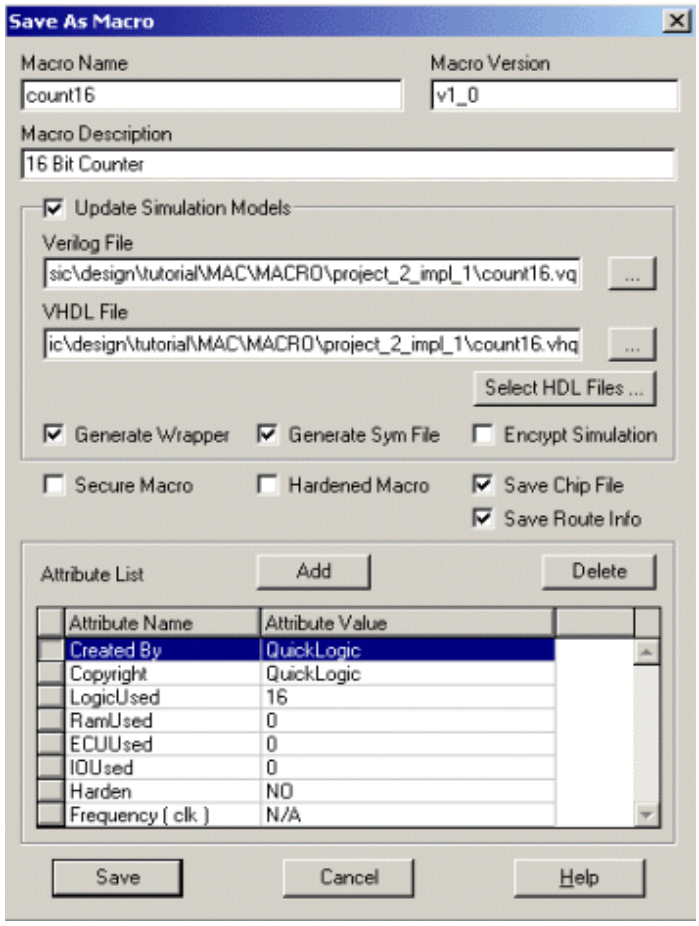


6.1.6 Saving the Macro Design

After running the design until back annotation, save the macro design:

1. From the SpDE menu bar, select **Tools>Save As Macro**, or click the **Save Macro File** icon, or press **Ctrl+Alt+A**.

TheSave Macro dialog box is displayed containing the Macro Name and mandatory Attributes.

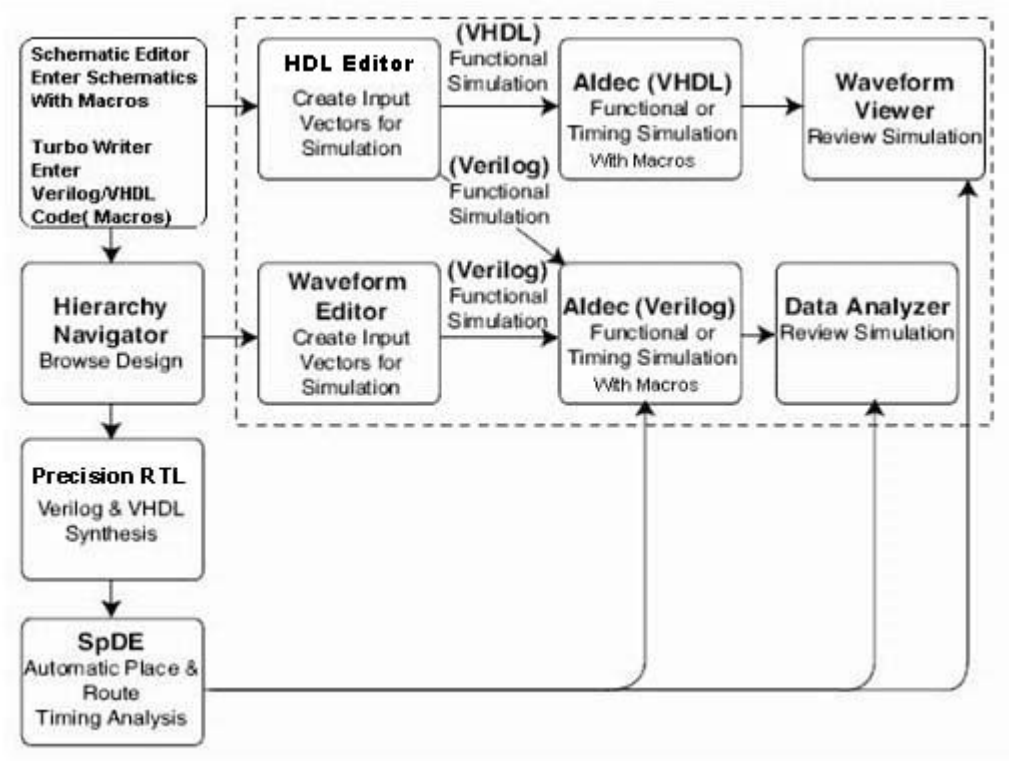


2. Type the Macro Version, Macro Description, and Simulation Models.
3. If desired, check the Encrypt Simulation and Secure Macro checkboxes.
4. If you want to save the macro as hardened i.e., the location needs to be fixed even in the target device, then check the Hardened Macro check box.
5. If you want to save the macro with placement information only, then un-check the SaveRouteInfo check box. By default, this checkbox is checked.
6. Click **Save**.
7. Repeat the same process for `C:\pasic\design\TUTORIAL\mac\macro\adder16.sch`.

6.2 Macro Usage Tutorial

This section is a tutorial of the QuickWorks Macro usage process, as shown in **Figure 6-3**. To become familiar with using a macro, you will create a schematic using the `adder16` and `counter16` macros.

Figure 6-3: Schematic Entry for Macro Usage Flow



As the design flow chart in **Figure 6-3** illustrates in this tutorial you will:

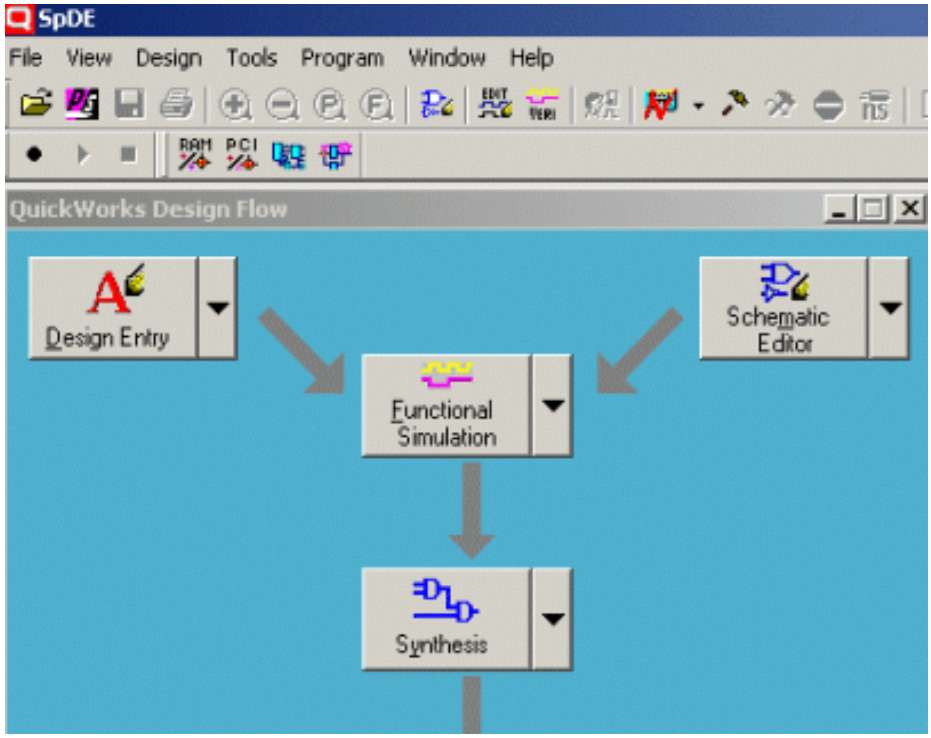
- Launch SpDE
- Launch Schematic Editor & Navigator to create and inspect the design using Macros
- Export the Verilog Functional Simulation Netlist
- Simulate the design for functionality using Aldec Simulation Environment
- View the Simulation Results
- Create and load a EDIF Netlist into SpDE.
- Shift to HM Planner to place the Routed Macros. It is mandatory to place the routed macros.
- If you select a routed macro, it will show possible valid locations where the macro can fit.
- Place the Pre-routed macro location and close the HM Planner.
- The design will be automatically optimized, placed and routed.
- Simulate the design for timing using Aldec Simulation Environment
- Review the results

6.2.1 Entering a Schematic Design

To enter a schematic design:

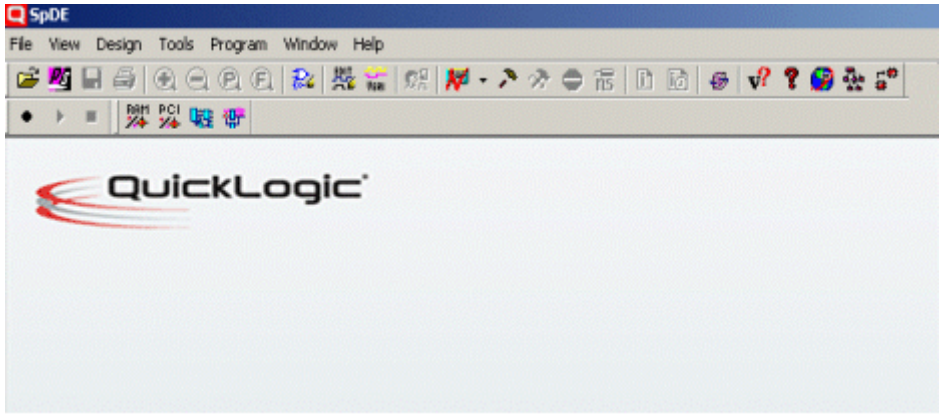
1. Select **Start>Programs>QuickLogic>SpDE**, or click the **SpDE** icon on your desktop.

   The SpDE window is displayed and all of the QuickWorks design resources are now available for use.



2. Close the QuickWorks Design Flow window by clicking the **X** in the upper right corner. This method of design will not be used for this tutorial.

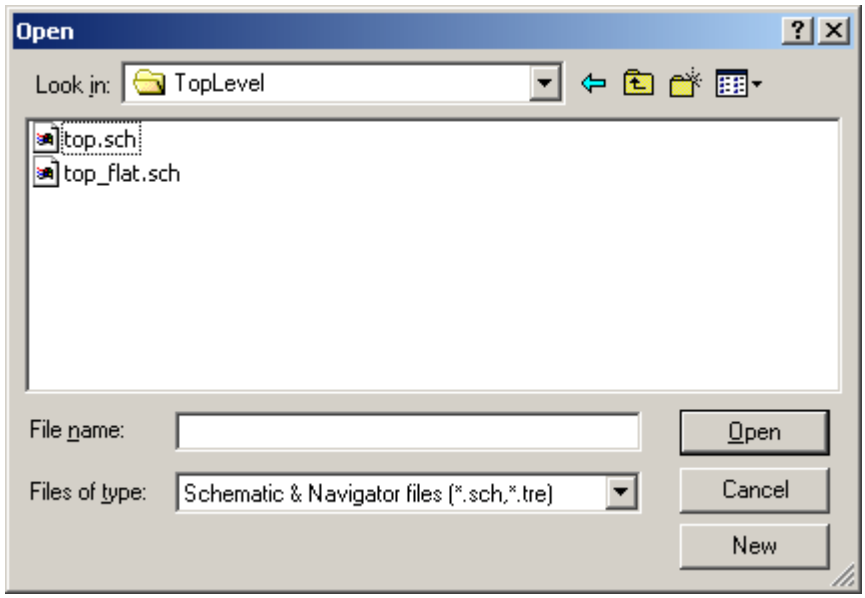
   The SpDE window is displayed. The SpDE toolbar contains icon buttons for executing commands quickly. The status bar at the bottom of the SpDE window displays status messages periodically.



NOTE: See the SpDE Menu Command Reference chapter of the *QuickWorks User Manual* for a full explanation of all available icons.

3. From the SpDE menu bar, select **Design>Schematic Editor & Navigator**, or click the  icon.

   The Open window is displayed.



4. Navigate to default directory `C:\pasic\design\TUTORIAL\mac\TopLevel\`.
5. Click **New**.

   The Hierarchy Navigator window is displayed.

6. Select **File>Create Schematic**.

   The Schematic Editor window is displayed.

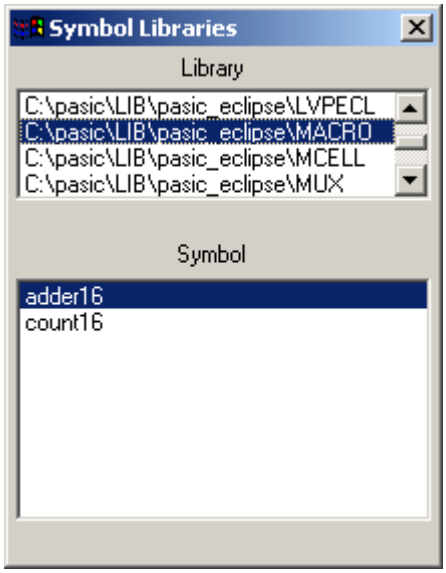
6.2.2 Adding Symbols

To add symbols to the schematic design:

1. From the Schematic Editor menu bar, select **Add>Symbol.**

   The Symbol Libraries window is displayed.

2. In the **C:\pasic\LIB\pasic_eclipse\MACRO** library, select the **adder16** macro symbol and drag it onto the workspace. Left-click to place it on the workspace and left-click to release your selection.



3. Move the cursor inside the schematic border.

   Notice that the cursor drags the outline of the symbol.

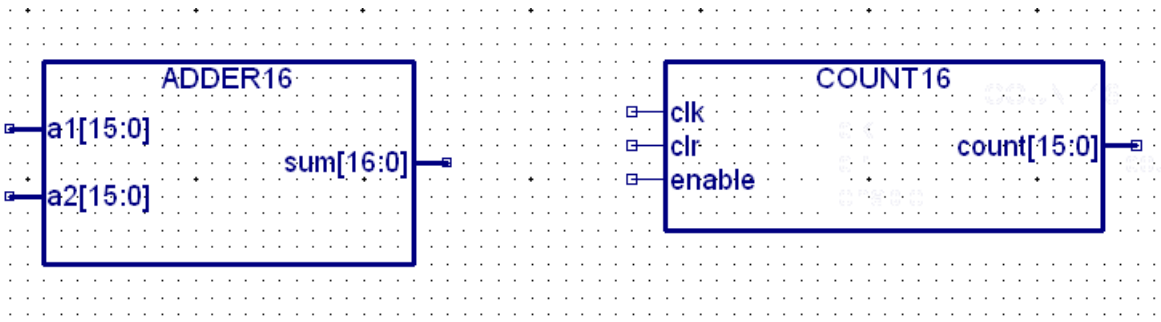
4. Position the cursor in the center of the sheet and place the symbol by clicking once.

5. In the **C:\pasic\LIB\pasic_eclipse\MACRO** library, select the **count16** symbol and drag it onto the workspace. Left-click to place it on the workspace and left-click to release your selection.

6. Move the cursor inside the schematic border.

   Notice that the cursor drags the outline of the symbol.

7. Position the cursor in the center of the sheet and place the symbol by clicking once.



8. Create your own design by adding wires, net names and so forth using these macro symbols along with other library symbols.

   For more information about creating a schematic, see “Creating a Schematic Design” on page 3.

6.2.3 Using the Tutorial Design

Refer to “Pre-Layout Simulation Using Active-HDL” on page 66 for more details about using schematic based design flow.

To use the tutorial design.

1. From the SpDE menu bar, select **Design>Schematic Editor & Navigator**, or click the  icon.

   The Open window is displayed.

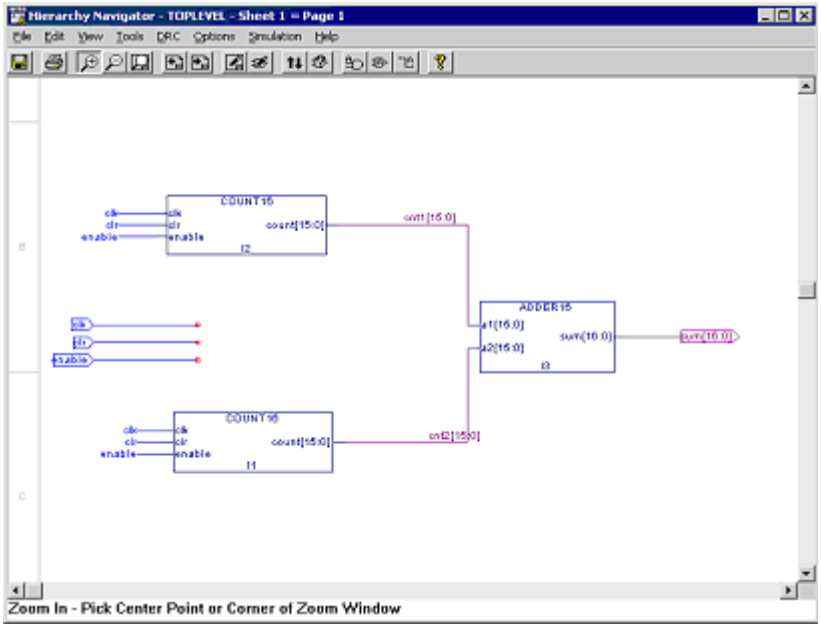
2. Navigate to `C:\pasic\design\TUTORIAL\mac\Macro\TopLevel\` and select **TopLevel.sch**.

3. Click **Open**.

   The Hierarchy Navigator is displayed.

4. From the Hierarchy Navigator menu bar, select **View>Full Fit**.

   Click anywhere within the schematic border to perform this operation.



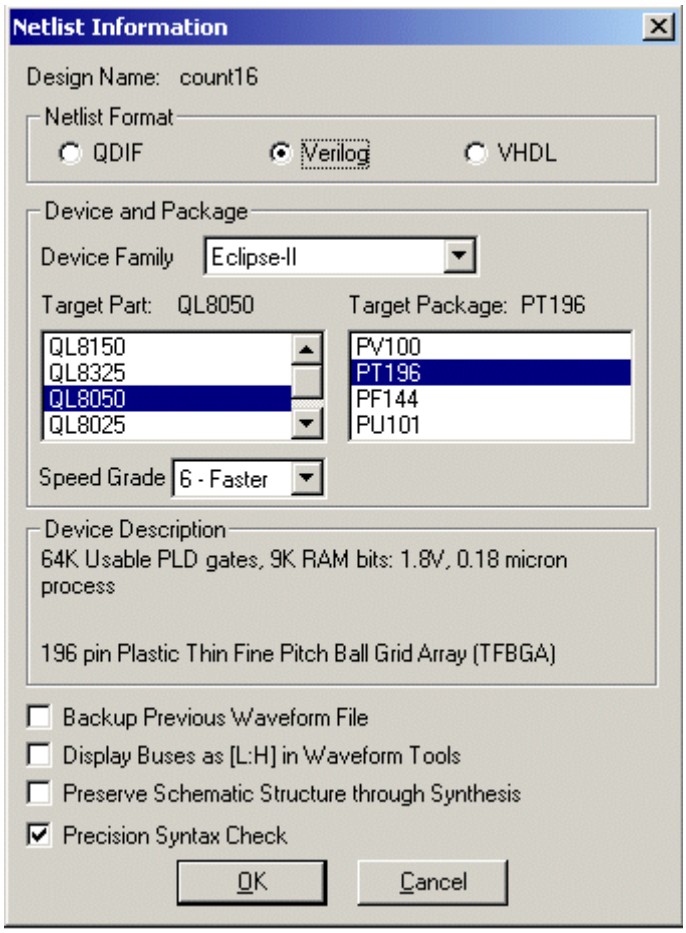
6.2.4 Exporting the Verilog Functional Simulation Netlist

The design will now be simulated to verify the functionality. In order to run a pre-layout simulation, a Verilog or VHDL netlist must be generated. This netlist can be used with the Aldec Active-HDL Simulator included with QuickWorks.

To export to Verilog:

1. From the Hierarchy Navigator menu bar, select **Tools>Export QuickLogic**.

The Netlist Information dialog box opens.



1. Select **Verilog** in the Netlist Format.
2. From the Device Family pull-down menu, select **Eclipse-II**.
3. From the Target Part list, select **QL8050**.
4. From the Target Package list, select a **PT196**.
5. Click **OK**. The Pre-layout Information window is displayed.
6. Click **Done**.
7. From the Hierarchy Navigator menu bar, select **File>Save**.

6.2.5 Simulating the Design for Functionality

While simulating the design using macros, the following files should be included in the simulation script (Wrapper file and Core Simulation Model):

For Verilog:

```
C:\pasic\spde\data\macro\adder16\adder16.v
C:\pasic\spde\data\macro\adder16\v1_0\adder16_design.v
```

For VHDL:

```
C:\pasic\spde\data\macro\adder16\adder16.vhd
C:\pasic\spde\data\macro\adder16\v1_0\adder16_design.vhd
```

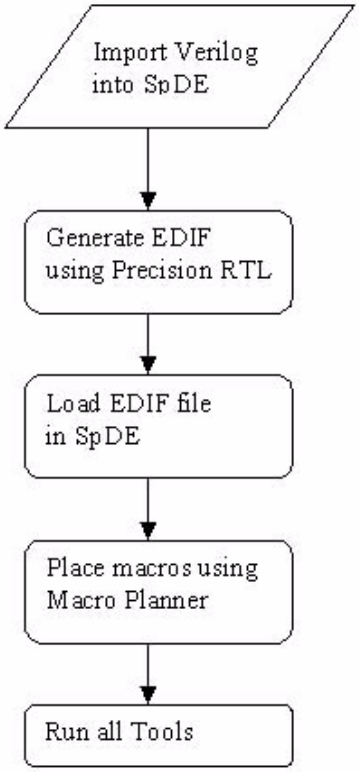
Refer to “Pre-Layout Simulation Using Active-HDL” on page 66 for more details about this topic.

After viewing functional simulation results, you can synthesize the Verilog file and generate a EDIF netlist. Now you will load this netlist file into SpDE.

6.2.6 Creating and Loading a EDIF Netlist

See **Figure 6-4** for the EDIF design flow.

Figure 6-4: EDIF Design Flow



6.2.7 Placing and Routing the Design

To place and route the design:

1. From the SpDE menu bar, select **File>Import Precision**, or click the **Import Precision** icon.

   The Open window is displayed.

2. Browse to default directory `C:\pasic\design\TUTORIAL\mac\macro\TopLevel\` and select **toplevel.v/toplevel.vhd**.

3. Click **Open**.

The Precision RTL program is displayed.

4. In the Precision RTL window, select the part and package.
5. Click **Compile**.
6. Click **Synthesis**.

   See "Starting Synthesis" on page 112 for more information.
7. When completed, select **File>Exit**.
8. Generate the EDIF Netlist.

   See "Creating an EDIF Netlist" on page 35 for information.
9. From the SpDE menu bar, select **File>Open**.

   The Open window is displayed.
10. Navigate to default directory `C:\pasic\design\TUTORIAL\mac\macro\TopLevel\` and select `TopLevel.edf`.
11. Click **Open**.

    The Retarget Device screen is displayed.
12. Select the Device Family, Target Device, and Package and click **OK** to retarget to a compatible device.

    The design is automatically imported into SpDE. The macros `adder16` and `counter16` appear as colored blocks. Initially, the macros are placed automatically. Use Macro Planner to place Macros (see "Running the Macro Planner" on page 173).

    The black color locations shown in the Macro Planner diagram below are possible valid locations to place the count16 macro. Similarly, if you can find valid locations for adder16.

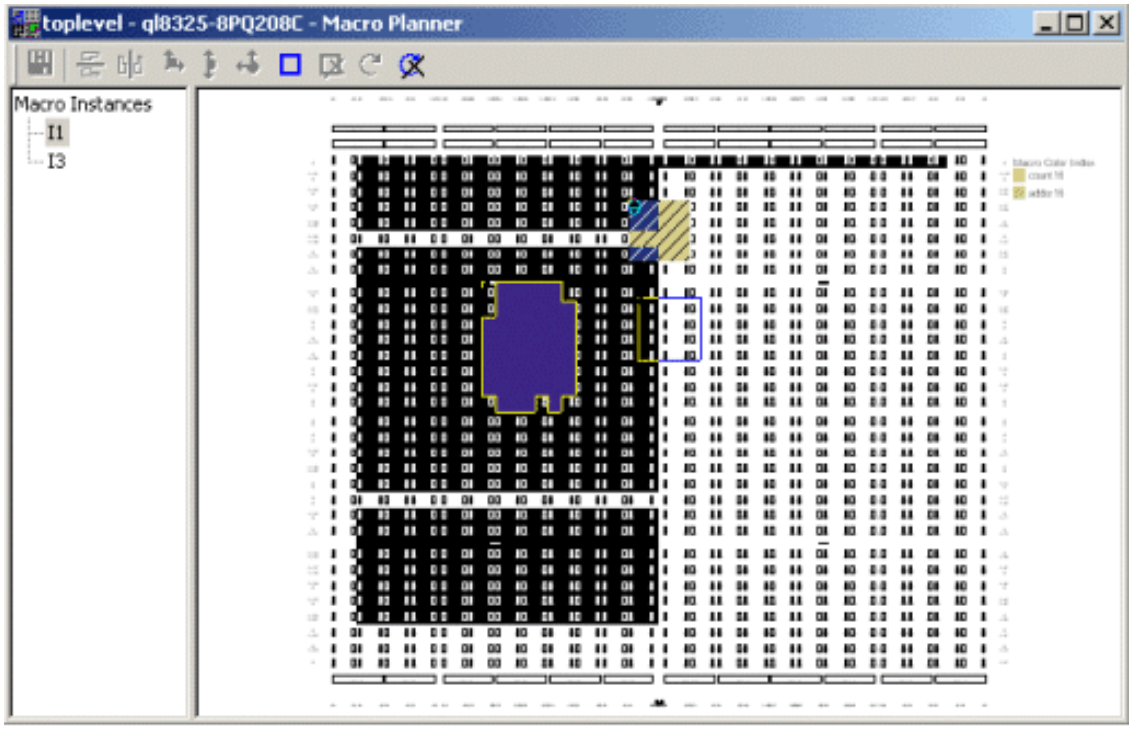
    NOTE: While moving an instance, valid location are highlighted only if the instance is pre-routed. For the others all locations are valid.
13. Set the options for back annotation.

    See "Setting Options for Back Annotation" on page 117 for more information.
14. Select and run all tools.

    See "Selecting and Running Tools" on page 117 for more information.
15. Run the post-layout simulation using Aldec Active-HDL.

    See "Starting Active-HDL" on page 101 for more information.

16. From the SpDE menu bar, select **File>Save** to save the `.chp` file.

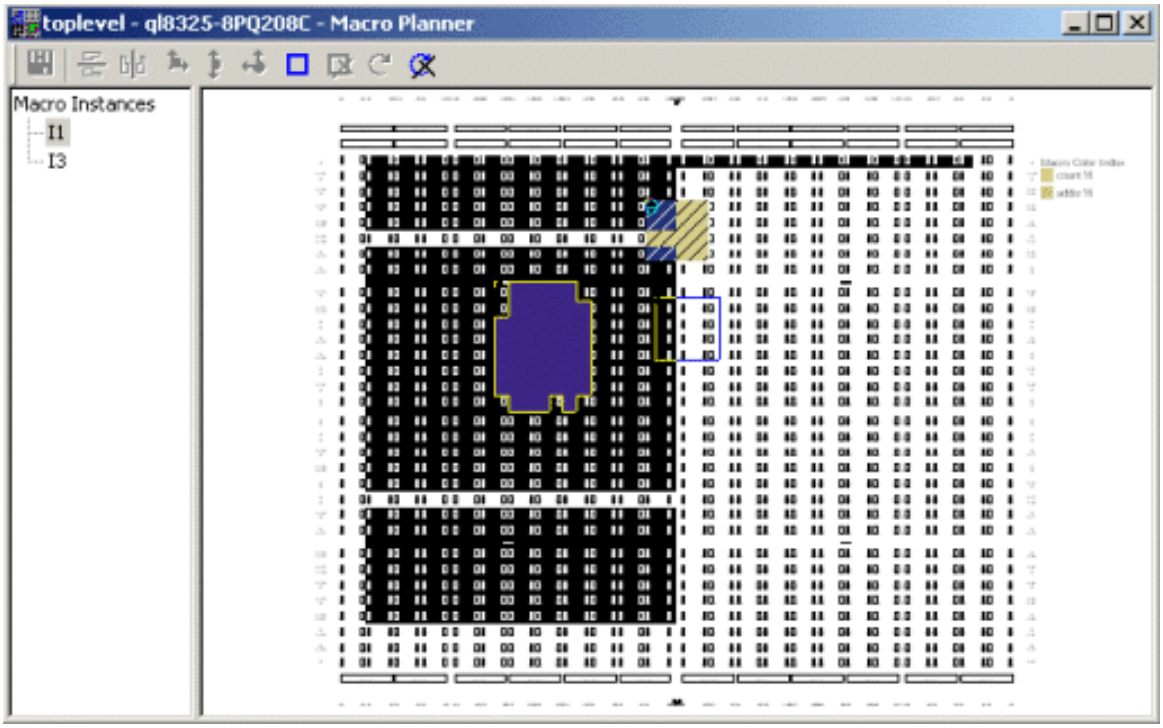


6.2.8 Running the Macro Planner

To start the Macro Planner:

1. From the SpDE menu bar, click on the **Macro Planner**  icon, or select **Tools-> Macro Planner,** or press **Ctrl+Alt+P**.

The Macro Planner is displays Tree view of macro instances.

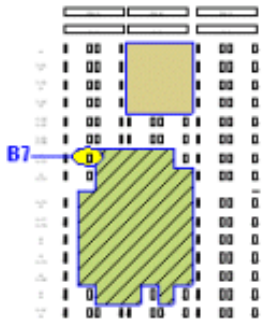


2. Click on Instance **I3**.

   The corresponding instance is selected in the macro view.

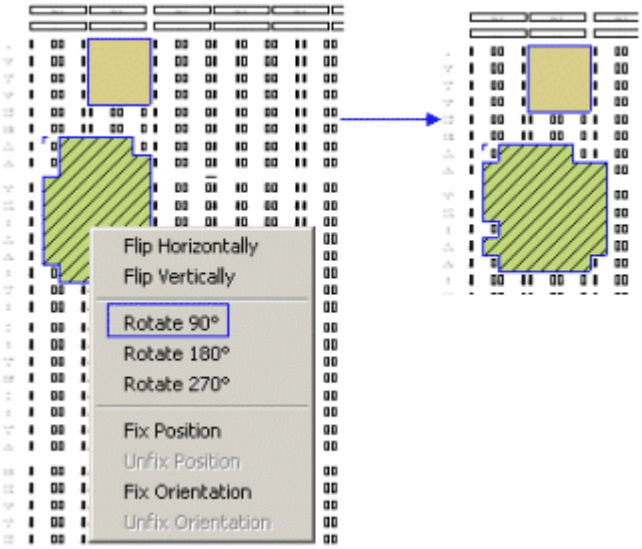
3. Move the selected instance in the macro view to the logic cell B7.

   Use the status bar to see the top left cell name while moving.



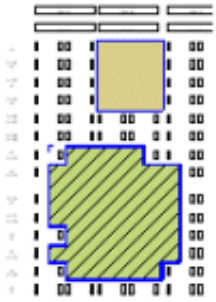
4. Right-click on the selected instance in the macro view and select **Rotate 90°** from the menu.

The instance is rotated by 90 degrees.



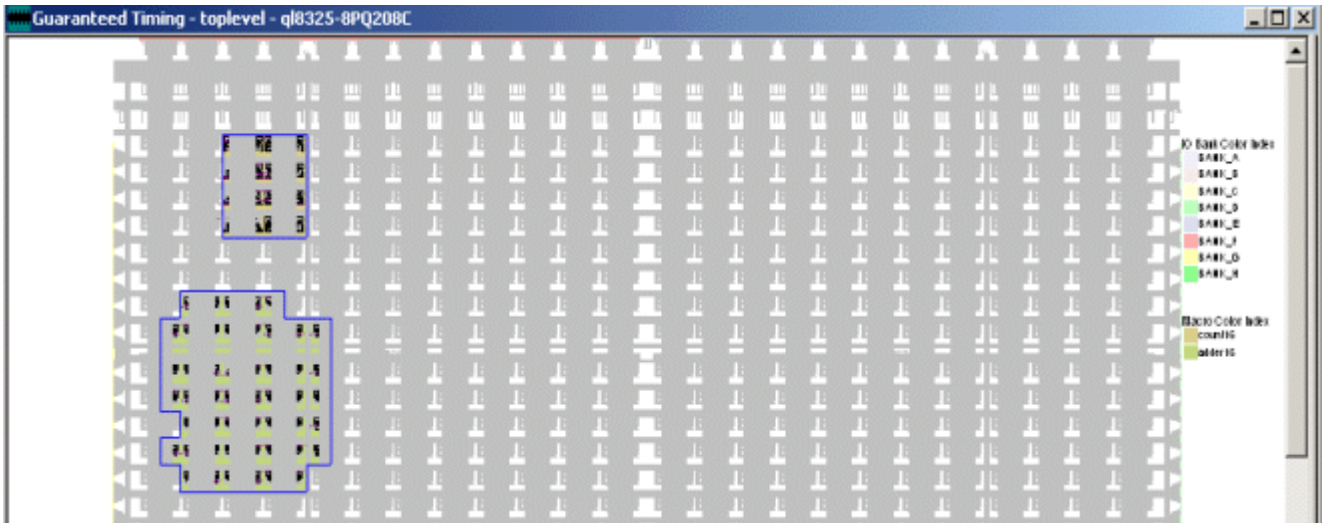
5. Right-click on the selected instance in the macro view and select **Fix Position**.

   The instance is fixed at cell B7.



6. Save the macro placement by selecting **File>Save**.

   After running all tools, the `.chp` file is displayed.



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