United Electronic Industries

The High-Performance Alternative

DNx-AI-224

—

User Manual

4-Channel, High Speed, Strain Gauge Analog Input Layer for the PowerDNA Cube and PowerDNR RACKtangle

Release 4.6

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PN Man-DNx-AI-224-913

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Table of Contents

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List of Figures

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Chapter 1 Introduction

This document outlines the feature set and use of the DNR- and DNA-AI-224 layer. The AI-224 is a four-channel strain gauge input module for the PowerDNA I/O Cube (DNA-AI-224) and the PowerDNR HalfRACK, RACKtangle, and the FlatRACK chassis (DNR-AI-224).

1.1 Organization of Manual

This AI-224 User Manual is organized as follows:

- **Introduction**
  This chapter provides an overview of DNx-AI-224 Strain Gauge Analog Input Board features, device architecture, connectivity, and logic. This chapter also describes the the shunt calibration and auto-null features of the DNx-AI-224 layer.
- **Programming with the High-Level API**
  This chapter provides an overview of the how to create a session, configure the session, and interpret results with the Framework API.
- **Programming with the Low-Level API**
  This chapter is an overview of low-level API commands for configuring and using the AI-224 series layer.
- **Appendix A - Accessories**
  This appendix provides a list of accessories available for use with the DNx-AI-224 board.
- **Appendix B - Shunt Calibration**
  This appendix describes shunt calibration support in the Framework.
- **Index**
  This is an alphabetical listing of the topics covered in this manual.

Manual Conventions

To help you get the most out of this manual and our products, please note that we use the following conventions:

Tips are designed to highlight quick ways to get the job done or to reveal good ideas you might not discover on your own.

NOTE: Notes alert you to important information.

CAUTION! *Caution advises you of precautions to take to avoid injury, data loss, and damage to your boards or a system crash.*

Text formatted in **bold** typeface generally represents text that should be entered verbatim. For instance, it can represent a command, as in the following example: “You can instruct users how to run setup using a command such as **setup.exe**.”

Text formatted in `fixed` typeface generally represents source code or other text that should be entered verbadim into the source code, initialization, or other file.

Examples of Manual Conventions

Before plugging any I/O connector into the Cube or RACKtangle, be sure to remove power from all field wiring. Failure to do so may cause severe damage to the equipment.

Usage of Terms

Throughout this manual, the term “Cube” refers to either a PowerDNA Cube product or to a PowerDNR RACKtangle™ rack mounted system, whichever is applicable. The term DNR is a specific reference to the RACKtangle, DNA to the PowerDNA I/O Cube, and DNx to refer to both.

1.2 The AI-224 Interface Board

The DNA-AI-224 and DNR-AI-224 are high speed, four channel strain gauge input boards for UEI's data acquisition and control Cubes and RACKtangle I/O racks respectively. The boards provide an ideal combination of high speed, accuracy and connection flexibility and are suitable for use in a wide variety of applications that include industrial, military, and testing applications.

The analog inputs offer 18-bit resolution at sample rates up to 100,000 samples per second (100kS/s). Each channel has an A/D converter and all four channels are sampled simultaneously. The combination of the 18-bit resolution with the board's automatic offset zeroing and automatic gain calibration ensure the measurements are extremely accurate. Each channel also includes an anti-aliasing filter that automatically is configured to match the sample rate. The complex anti-aliasing filter can reduce error by at least 72dB at rates of 100kHz.

The DNx-AI-224 accepts inputs from full, half or quarter bridge gauges and load cells. Bridge completion resistors are built in for use with 120Ω, 350Ω and 1000Ω gauges; also full-bridge gauges of any resistance value may also be measured. Each channel offers an independent excitation output, user-programmable from 0 to ±10 V_{dc} in 65535 steps (3mV). The excitation outputs can drive up to 50 mA each, allowing 1kΩ bridges to be driven at ±10 V_{dc}, 350 ohm bridges at ±8.75 V and 120 ohm bridges at up to ± 3 V_{dc}.

The board provides on-board compression and tension shunt calibration with shunt-calibration values selectable between 6.7kΩ and 170kΩ, within 1.1kΩ. Connections for external, user supplied shunt resistors are also provided. An automatic input nulling/balancing capability has also been built in allowing most bridges to be quickly and easily balanced before testing actually begins.

As with all UEI PowerDNA boards, the DNx-AI-224 can be operated in harsh environments and has been tested at 5*g* vibration, 50*g* shock, -40 to +85°C temperature, and altitudes up to 70,000 feet or 21000 meters. Each board provides 350 V_{rms} isolation between channels and also between the board and its enclosure, or any other installed boards.

Software for the DNA/DNR-AI-224 is provided as part of the UEI Framework. The framework provides a comprehensive yet easy to use API that supports all popular Windows programming languages as well as supporting programmers using Linux and most real-time operating systems including QNX, RTX, RT Linux and more. Finally, the framework supplies complete support for those creating applications in LabVIEW, MATLAB/Simulink, DASYLab or any application supporting ActiveX or OPC servers.

1.3 Features

The AI-224 layer has the following features:

- 4 strain gauge or load cell input channels
- 18-bit resolution, up to 100 kS/s
- Simultaneous sampling on all channels
- Built-in aliasing filters (both digital and analog) 72dB min. rejection
- Full, half, and quarter-bridge (3-wire) strain gauge inputs
- Input ranges of +/-10, ..., +/-0.078125 V_{DC} across full differential span, where each differential input must be under 12V with respect to AGND.
- Input impedance of 10 megaohm
- 120, 350, and 1000-ohm bridge completion resistors provided on board for each channel
- Built-in tension/compression shunt calibration resistors, selectable between 6.7k-170k, within 1.1kΩ, measured with 0.02% accuracy
- Connections provided for two external shunt resistors
- Independent 0 to ±10 V DC or 20 V differential span (14V AC[1]) programmable excitation output on each channel (16-bit resolution)
- Excitation outputs can drive up to 70 mA each — allows 1k bridges to be driven across 20 V span, 350-ohm at 17.5 Vdc and 120-ohm at 6 Vdc
- Automatic input nulling (16-bit resolution over a ±10V range) permits bridge balancing before starting tests
- Input ground to system ground isolation: $350V_{rms}$
- Power consumption 3.5W max
- Weight of 136 g or 4.79 oz for DNA-AI-224; 817 g or 28.8 oz with PPC5
- Tested to withstand 5g Vibration, 50g Shock, -40 to +85°C Temperature, and Altitude up to 70,000 ft or 21000 meters
- UEI Framework Software API may be used with all popular Windows programming languages and most real time operating systems such as RT Linux, RTX, or QNX and graphical applications such as LabVIEW, MATLAB, DASYLab and any application supporting ActiveX or OPC

1. Board is capable of providing AC excitation, but this feature is not software-supported in the current release.

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1.4 Specification

The technical specification for the DNx-AI-224 board are listed in **Table 1-1**.

Table 1-1. DNx-AI-224 Technical Specifications

Inputs	
Number of channels	4, simultaneously sampled
Configuration	Full, Half, or Quarter bridge
Resolution	18-bit
Input ranges	*†See table below.*
Sample rate	100 kilosamples per second, max
Accuracy	
Integral non-linearity	±0.0015%
Offset error @ 25 °C, G=2	0.0005% typical (see graphs on next page)
Gain error @ 25 °C, G=2	0.003% typical (see graphs on next page)
Offset drift per °C	2ppm typical / 10ppm max
Gain drift per °C	2ppm typical / 10ppm max
Overall error	< 250 µV
Bridge resistance	120, 350 or 1000 Ohm
Anti-aliasing filter*	Automatic, 72 dB minimum rejection
Input impedance	10 megohm, min
Excitation Outputs	
Number of channels	Two (P+, P-) per channel, independently programmable
Output voltage	0 to ±10 Vdc (each output); 20Vdc diff span
Resolution	16-bit
Output drive current	50 mA, max
Output error	± 5 mV, max, measured to the same accuracy as the analog input
Shunt Calibration	
Shunt range	6.7 k to 170k ohm (tension or compression) internal. Also provides two connections for user supplied shunt resistors.
Shunt resolution	1.1k ohm
Automatic Bridge Nulling / Balancing	
Null/balance range	19-bit resolution @ ±10V (auto-null 1 mV max)
General Specifications	
Electrical isolation	350 Vrms, chan-chan and chan-chassis
Operating temperature	Tested -40 °C to +85 °C
Vibration *IEC 60068-2-6* *IEC 60068-2-64*	5 g, 10-500 Hz, sinusoidal 5 g (rms), 10-500 Hz, broad-band random
Shock *IEC 60068-2-27*	50 g, 3 ms half sine, 18 shocks @ 6 orientations 30 g, 11 ms half sine, 18 shocks @ 6 orientations
Humidity	0 to 95%, non-condensing
Altitude	0 to 70,000 feet
Power consumption	6.0 Watts + 1.5 × (excitation power supplied)

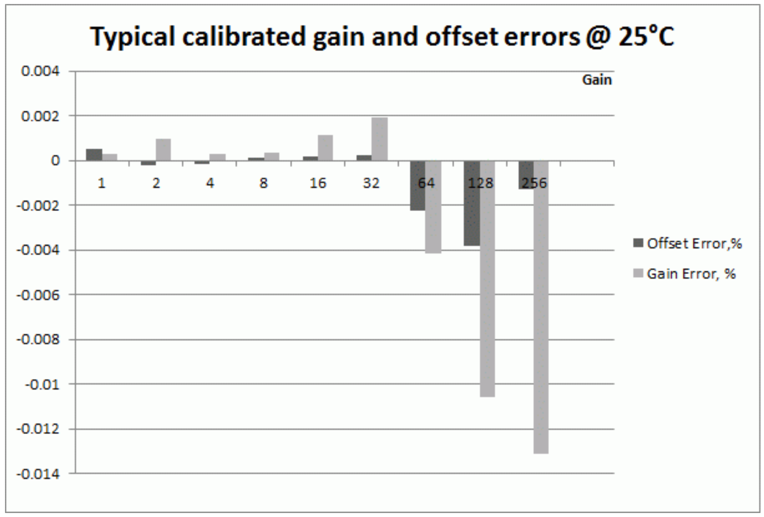
Input	Range (Vdc)	±10*	±10	±5	±2.5	±1.25	±0.625	±0.3125	±0.15625	±0.078125
	Gain	1	2	4	8	16	32	64	128	256

* For general purpose analog input note: gain of 1x corresponds to a ±20V_{dc} range that is limited to ±12.5V. Input voltage on S+ & S- should not be allowed to exceed +12.5V or -12.5V relative to AGND.

1.4.1 Characteristic Graphs

The following graphs show the characteristic behavior of the AI-224 layer.

Figure 1-1 shows typical offset gain error that can be expected at various gain factors, in percent, e.g. 0.0003% offset error at a gain of 1. For the same set of measurements, the noise in microvolts RMS that corresponds to gain is shown on the right.



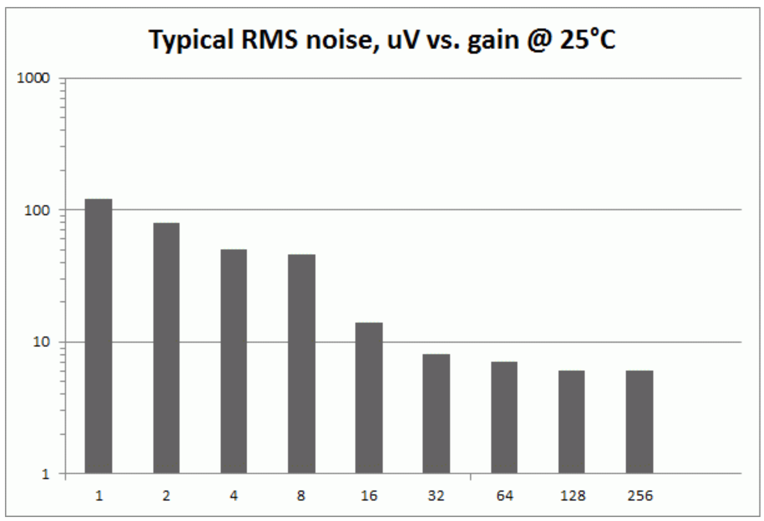


Figure 1-1. Offset error and RMS noise vs. gain

Temperature changes the characteristics of the measured signal with this layer:

	Input range +/-uV	drift, uV/°C	drift, ppm/°C
G=64	78125	0.5	2
G=64	312500	1	1.5
G=16	2500000	4	1
G=2	10000000	16	1

Table 1-2. Typical Temperature Drift for the AI-224 layer

The figure below shows the noise amplitude observed at gain of 1, 16, and 64 for the full range of the supported sampling frequencies. The noise amplitude is the difference in amplitude of the actual measurement and the ideal result. For example, at gain 1 and sampling rate of 100kHz the difference between actual and ideal measurement is a typical -100dB of full scale or 0.00001V.

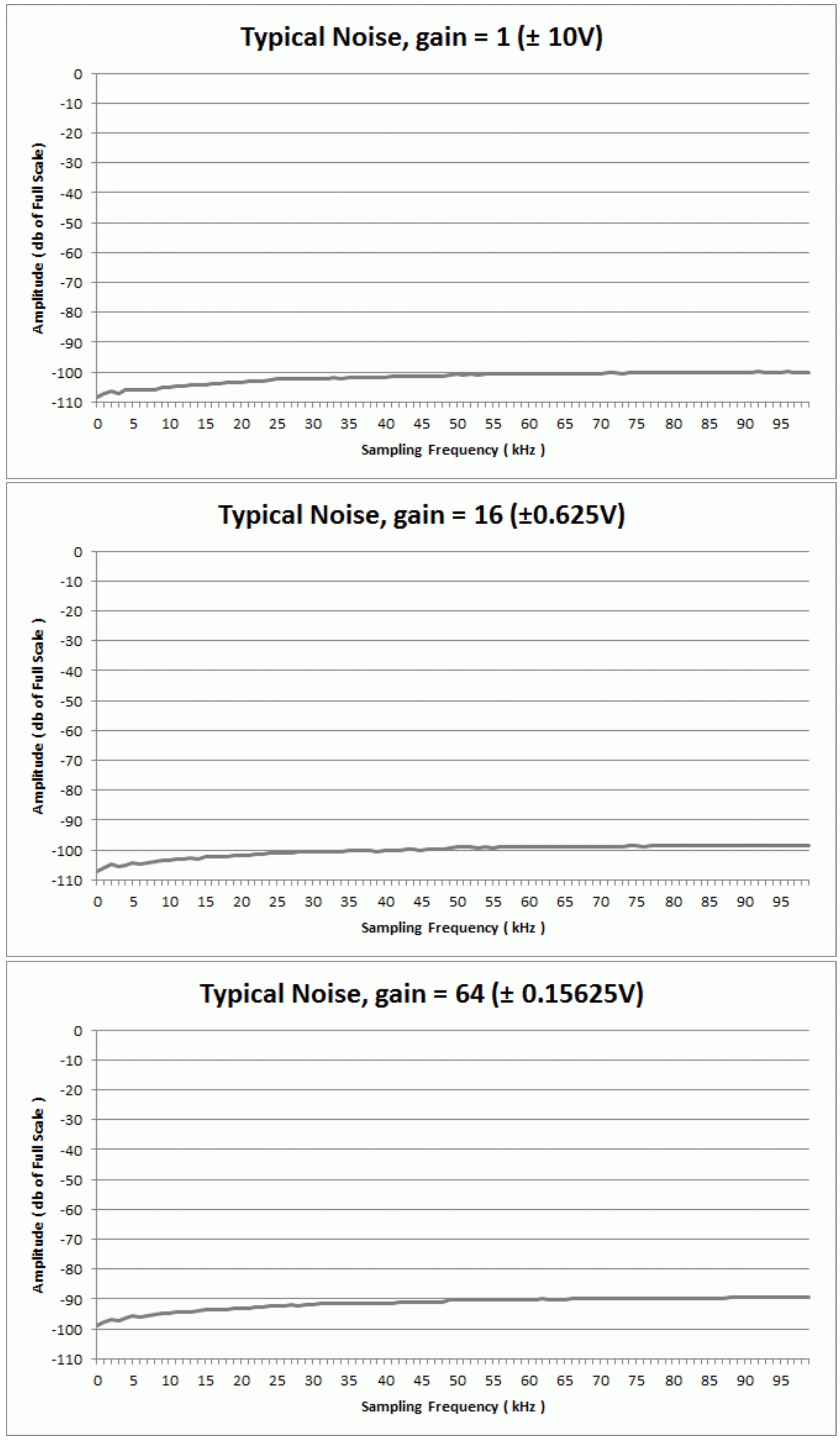


Figure 1-2. Noise amplitude at various sampling rates

1.5 Device Architecture

Figure 1-3 is a block diagram of the architecture of the AI-224 layer.

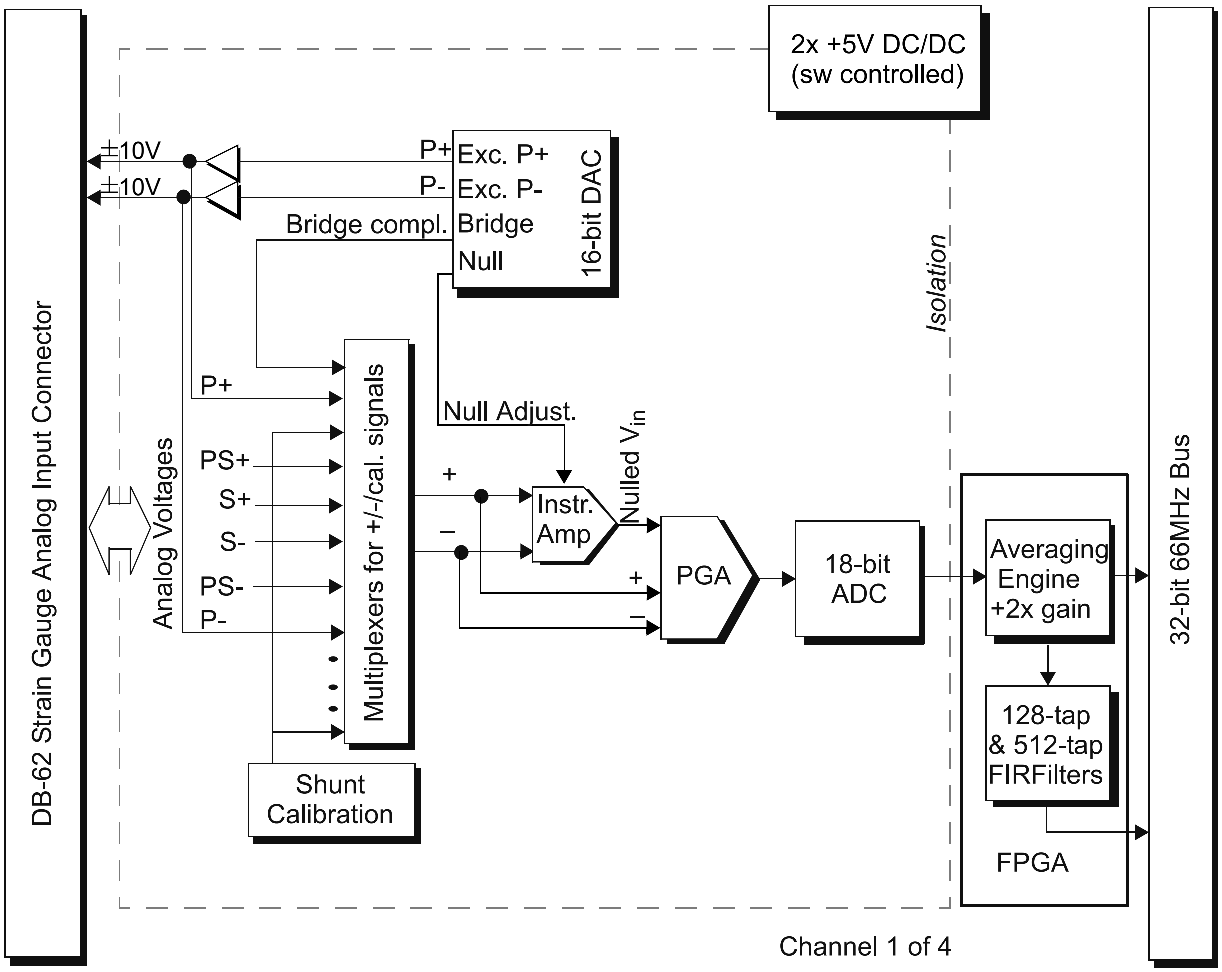


Figure 1-3. Block Diagram of the AI-224 Layer

Each quarter bridge strain gauge sensor is combined with bridge completion resistors mounted on the AI-224 board or an applicable STP board to form a half-bridge which is combined with a DAC voltage to simulate a full bridge (or equivalent). Similarly, each half bridge sensor is combined with a DAC voltage to simulate a full bridge. The output of each full bridge sensor is sensed directly by the AI-224 without completion resistors or DAC (except for excitation). Refer to **Figure 1-6** to **Figure 1-10** for the various connection circuits used.

Excitation for the strain gauge is supplied from a 16-bit quad DAC under program control. The DAC can produce two excitation voltages, either static (DC) or dynamic (AC), in a range of ±10 volts (dual outputs). As an option, these two voltages may be configured to produce a single voltage of ±10 Volts. The AC excitation mode is not software-supported in the current release of the AI-224.

The analog measurement voltages from each strain gauge bridge, as shown in **Figure 1-3**, are fed through input multiplexers to a programmable gain amplifier. They may be strain measurements or miscellaneous voltage signals used to compute values of resistors in various internal circuits, then passed to the A/D converter. The A/D converter (one per channel) is a successive approximation 18-bit device, which also performs signal averaging for further noise reduction.

The output is then passed to two cascaded FIR filters, which among other functions, performs additional anti-aliasing digital filtering. The combination of the low pass analog filter and digital filtering in the averaging engine produces an extremely sharp cutoff filter, much steeper than would be possible with an analog filter alone. This offers the additional benefit of providing perfectly uniform group delay/phase shift for all four channels. Note also that the filter coefficients are automatically set to match the selected sampling rate without introducing any gain/offset error.

The measurement data is then processed by the CPU and transmitted over the network to the host in the normal manner. Refer to Chapters 2 and 3 for programming information.

1.6 Auto-Null Adjustment

To correct for any initial unbalance in the bridge, the AI-224 may be automatically nulled by using the 224AutoNull function on any channel of the module. This program automatically measures the zero unbalance and corrects the gain to eliminate the error.

1.7 Indicators

A photo of the DNx-AI-224 unit is illustrated below.

The front panel has two LED indicators:

- RDY: indicates that the layer is receiving power and operational.
- STS: can be set by the user using the low-level framework.

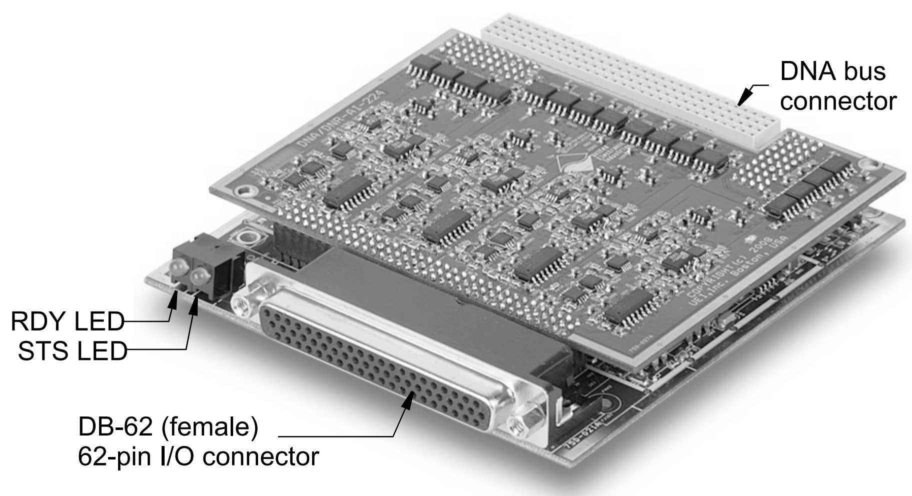
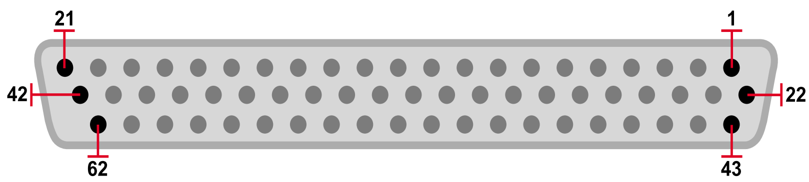


Figure 1-4. The DNA-AI-224 Analog-Input Layer

1.8 Layer Connectors and Wiring

Figure 1-5 below illustrates the pinout of the AI-224.



	Pin	*Signal*	*Pin*	*Signal*	*Pin*	*Signal*
Channel 0	1.	QB1K CH 0	22.	GND CH 0	43.	P– CH 0
	2.	PS+ CH 0	23.	PS– CH 0	44.	P+ CH 0
	3.	QB CH 0 (S– CH 0)	24.	QB120 CH 0	45.	QB350 CH 0
	4.	S+ CH 0	25.	S– CH 0	46.	SHA+ CH 0 (P+ CH 0)
	5.	SHB– CH 0 (P– CH 0)	26.	SHA– CH 0 (S– CH 0)	47.	NC
Channel 1	6.	GND CH 1	27.	NC	48.	QB1K CH 1
	7.	P+ CH 1	28.	P– CH 1	49.	QB120 CH 1
	8.	PS+ CH 1	29.	PS– CH 1	50.	QB CH 1 (S– CH 1)
	9.	S+ CH 1	30.	S– CH 1	51.	QB350 CH 1
	10.	SHA+ CH 1 (P+ CH 1)	31.	SHA– CH 1 (S– CH 1)	52.	SHB– CH 1 (P– CH 1)
Channel 2	11.	QB1K CH 2	32.	NC	53.	P– CH 2
	12.	PS+ CH 2	33.	PS– CH 2	54.	P+ CH 2
	13.	QB350 CH 2	34.	GND CH 2	55.	QB120 CH 2
	14.	S+ CH 2	35.	S– CH 2	56.	QB CH 2 (S– CH 2)
	15.	SHA+ CH 2 (P+ CH 2)	36.	SHA– CH 2 (S– CH 2)	57.	NC
			37.	SHB– CH 2 (P– CH 2)		
Channel 3	16.	GND CH 3			58.	QB1K CH 3
	17.	P+ CH 3	38.	P– CH 3	59.	QB120 CH 3
	18.	PS+ CH 3	39.	PS– CH 3	60.	QB CH 3 (S– CH 3)
	19.	NC	40.	QB350 CH 3	61.	S– CH 3
	20.	SHA+ CH 3 (P+ CH 3)	41.	SHA– CH 3 (S– CH 3)	62.	S+ CH 3
	21.	SHB– CH 3 (P– CH 3)	42.	NC		

NC — No Connection (Do not use)
Rsvd — Reserved for future use

Figure 1-5. Pinout Diagram of the AI-224 Layer

NOTE: If you are using a DNA-STP-62 accessory panel with the AI-224, please refer to **Figure 1-9** on page 14 for a layout drawing of the board and to the Appendix for a description of the panel.

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1.8.1 Full Bridge Gauge Connections

Figure 1-6 shows the connections between a full bridge strain gauge and the AI-224 board. Excitation voltage is applied between P+ and P- and sensed between PS+ and PS-. Since no bridge completion is required with a full bridge sensor, the DAC input to MUX1 is not used in this configuration.

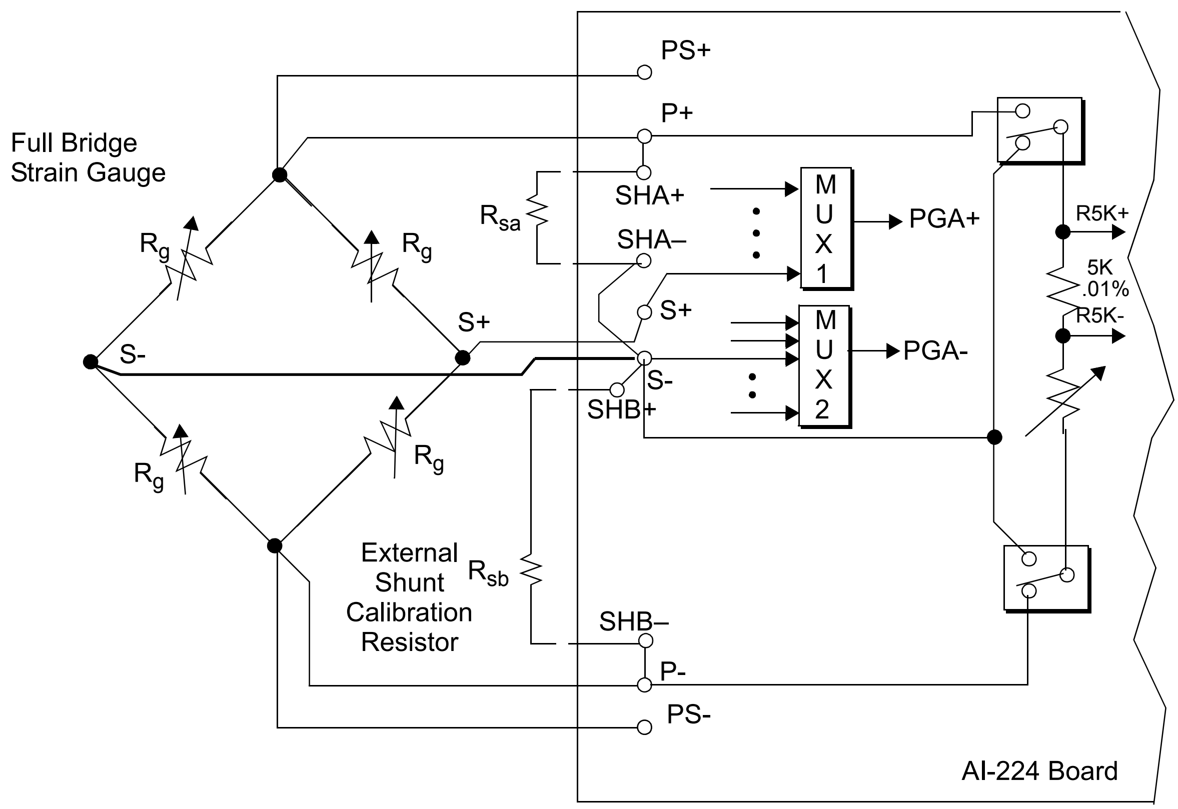

Figure 1-6. Full Bridge Strain Gauge Circuit.

As part of the internal shunt calibration function, the AI-224 board measures the voltage drop across a precision 5K resistor and computes the exact value of the digital shunt with ~.02% accuracy. This value is reported to the software. The shunt may be adjusted from ~6.7K to 170K ohms. Note that the shunt may be switched to either side of the bridge (tension or compression).

1.8.2 Half Bridge Gauge Connections

Figure 1-7 shows the connections between a half bridge strain gauge and the AI-224 board. Excitation voltage is applied between P+ and P- and sensed between PS+ and PS-. As shown in the diagram below, the board uses a programmable DAC to simulate the other half of the bridge. The DAC output is fed to the PGA+ input and the S- point is connected to the PGA- input of the first differential PGA amplifier.

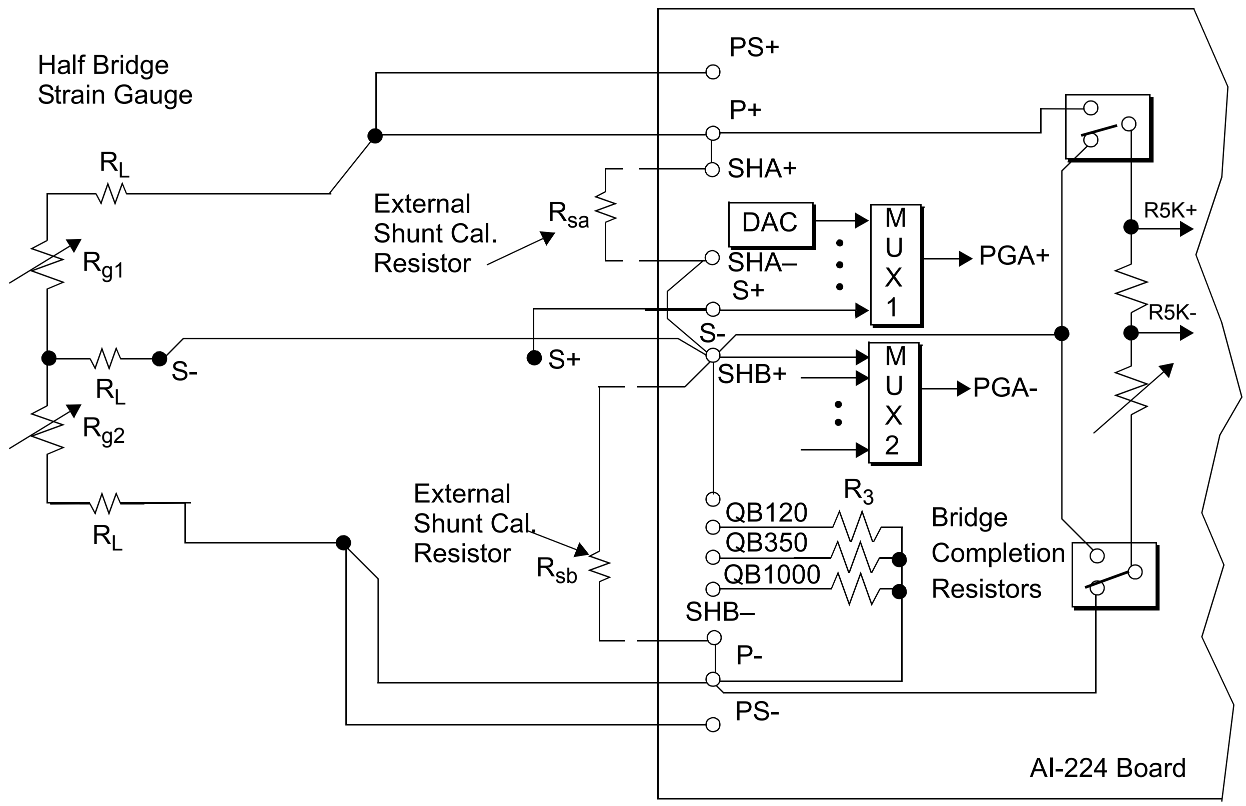

Figure 1-7. Half Bridge Strain Gauge Circuit.

As part of the internal shunt calibration function, the AI-224 board measures the voltage drop across a precision 5K resistor and computes the exact value of the digital shunt with ~.02% accuracy. This value is reported to the software. The shunt may be adjusted from ~6.7K to 170K ohms. Note that the shunt may be switched to either side of the bridge (tension or compression).

1.8.3 Quarter Bridge Gauge Connections

Figure 1-8 shows the connections between a quarter bridge strain gauge and the AI-224 board. Excitation voltage is applied between P+ and P- and sensed between PS+ and PS-. As shown in the diagram below, the board uses a programmable DAC to simulate the other half (R_3, R_4) of the bridge. The DAC output is fed to the PGA+ input and the S- point is connected to the PGA- input of the first differential PGA amplifier.

To complete the bridge, three bridge completion resistors (120, 350, and 1K ohm resistors) are mounted on the AI-224 board between S+ and P-. To select one of the three resistors to serve as R_2 for a particular application, install a jumper connector between applicable terminals on the I/O connector or STP board.

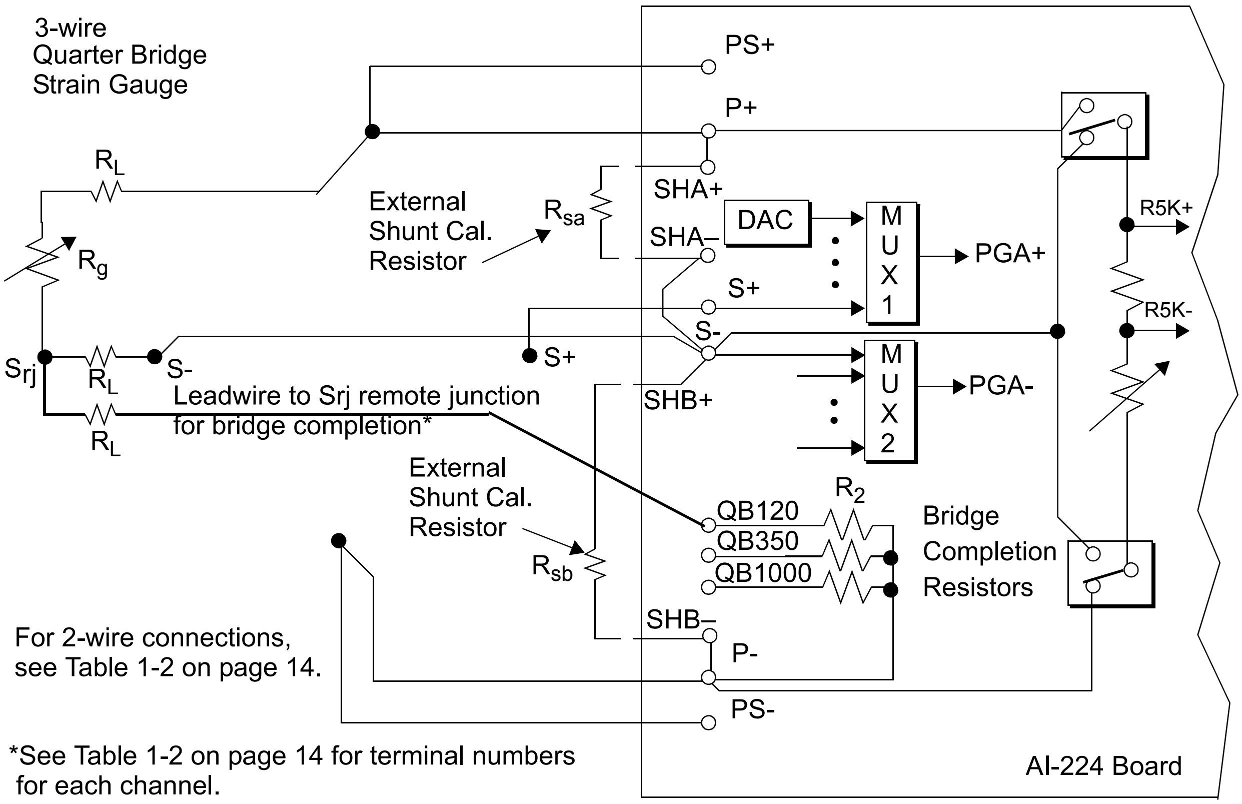

Figure 1-8. 3-Wire Quarter Bridge Strain Gauge Circuit

As part of the internal shunt calibration function, the AI-224 board measures the voltage drop across a precision 5K resistor and computes the exact value of the digital shunt with ~.05% accuracy. This value is reported to the software. The shunt may be adjusted from ~6.7K to 170k ohms. Note that the shunt may be switched to either side of the bridge (tension or compression).

1.8.4 Connecting Bridge Completion Resistors

It is recommended to use a DNA-STP-62 screw terminal panel accessory for making connections to bridge completion resistors. Layout of a DNA-STP-62 is shown in **Figure 1-9** below and **Figure A-1** on page 21 of the Appendix.

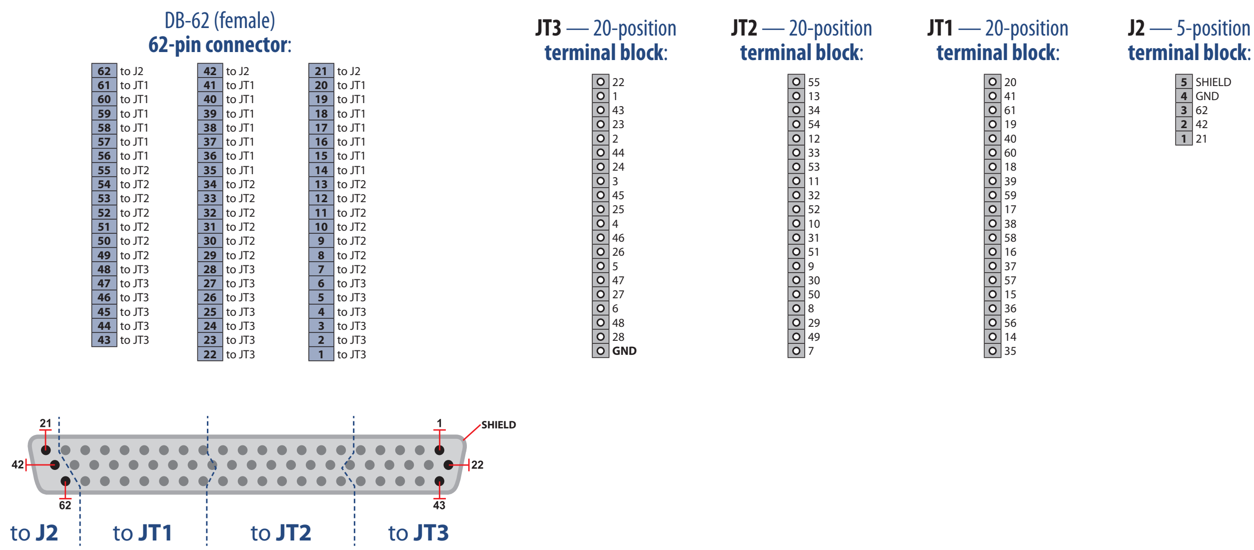

Figure 1-9. Layout of DNA-STP-62 Screw Terminal Panel

For quarter bridge measurement using a DNA-STP-62 screw terminal panel, install connection leads as shown in Table 1-3 on page 14. The leads will connect the bridge completion resistors between P- and the 3-wire remote junction point, S_{rj}. Refer to **Figure 1-8** on page 13 for a drawing of the circuit. The figure also shows the setup for using the bridge completion DAC. Refer to **Figure 1-7** on page 12 for a half bridge setup that does not use bridge completion resistors.

Table 1-3. Lead Connections for Quarter Bridge Circuits

Bridge Competion Resistor	Leads Required for 3-wire Quarter Bridge Measurement			
	Ch 0 Lead	Ch 1 Lead	Ch 2 Lead	Ch 3 Lead
120 ohm	S_{rj} to 24	S_{rj} to 49	S_{rj} to 55	S_{rj} to 59
350 ohm	S_{rj} to 45	S_{rj} to 51	S_{rj} to 13	S_{rj} to 40
1000 ohm	S_{rj} to 1	S_{rj} to 48	S_{rj} to 11	S_{rj} to 58
NOTE: For 2-wire quarter-bridge circuit, connect bridge completion leadwire to S- instead of S_{rj} (Pin 3 for Ch0, Pin 50 for Ch1, Pin 56 for Ch2, Pin 60 for Ch3).				

1.8.5 Raw Analog Input with Excitation

The AI-224 can be used for traditional analog input, with the added bonus of an optional continous analog excitation/output. This mode is useful for applications where strain gages are not used, or where bridge completion is either not necessary or already provided by an external circuit.

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1.9 Shunt Calibration

Shunt calibration of a strain gauge bridge is performed by placing a known resistor across one leg of the measurement Wheatstone bridge. The purpose of this technique is to simulate the effect of applying a specific physical load to the bridge sensor without actually doing so. Placing the shunt across the excitation and the signal leg of the bridge can be used for tension shunt calibration; placing it across the excitation and the alternate leg of the bridge can be used for compression shunt calibration.

The DNx-AI-224 provides built-in shunt calibration resistors that can be set in tension or compression in the range from 6.7 kOhm to 170 kOhm in about 1.1kOhm increments. Terminals are also provided to allow the connection of external shunt calibration resistors if desired.

The on-board shunt calibration system is limited. Finding actual resistor networks that would provide this functionality and maintain the required accuracy over this wide temperature range within the space available on the DNx-AI-224 is not possible. However it is relatively straightforward to fit a resistance measurement system that performs resistance measurements at a level suitable for high accuracy shunt calibration. In the AI-224, a 200kohm nominal 256-tap digital potentiometer is used as internal shunt calibrator, allowing characterization of a load cell. Note that the digital shunt can be switched to connect to either side of the bridge (tension or compression), as shown in **Figure 1-6** through **Figure 1-8**. The digital potentiometer is then adjusted to bring the bridge into balance with the shunt resistor in parallel with the strain gauge.

To perform shunt calibration with the DNx-AI-224, the user selects the shunt resistance desired as well as whether compression or tension simulation is desired. The DNx-AI-224 driver/software then selects the shunt resistor to the setting closest to the desired value. The resolution of the shunt resistance selection is approximately 1.1 kOhm. The DNx-AI-224 software then performs an automatic measurement of the selected shunt resistor and returns the measured resistance within 0.02% of the reading. This measured value is then used by the application's calibration routine as the shunt resistance "switched in".

The board also provides for connection of two user-supplied external shunt calibration resistors. Refer to **Figure 1-5** for the pinout. Note that the calibration resistors connect to terminals SHA+ (P+) and SHA- (S-), or SHA- (S-) and SHB- (P-).

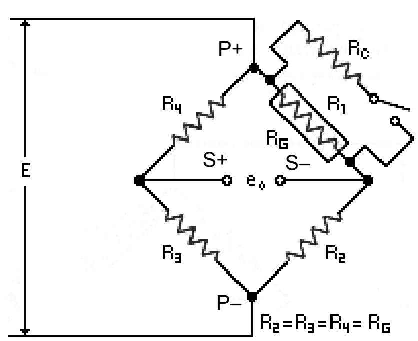

Figure 1-10. Shunt Calibration

NOTE: Refer to Appendix B for a more detailed description of the shunt calibration method used in the AI-224 modules.

Chapter 2 Programming with the High Level API

This section describes how to control the DNx-AI-224 using the UeiDaq Framework High Level API.

UeiDaq Framework is object oriented and its objects can be manipulated in the same manner from different development environments such as Visual C++, Visual Basic or LabVIEW.

The following section focuses on the C++ API, but the concept is the same no matter what programming language you use.

Please refer to the “UeiDaq Framework User Manual” for more information on use of other programming languages.

2.1 Creating a Session

The Session object controls all operations on your PowerDNx device. Therefore, the first task is to create a session object:

```
// create a session object for input
CUeiSession aiSession;
```

2.2 Configuring the Resource String

UeiDaq Framework uses resource strings to select which device, subsystem and channels to use within a session. The resource string syntax is similar to a web URL:

```
<device class>://<IP address>/<Device Id>/<Subsystem><Channel list>
```

For PowerDNA and RACKtangle, the device class is **pdna**.

For example, the following resource string selects analog input lines 0,1,2,3 on device 1 at IP address 192.168.100.2: “pdna://192.168.100.2/Dev1/Ai0:3” as a range, or as a list “pdna://192.168.100.2/Dev1/Ai0,1,2,3”.

2.3 Configuring for Input

The AI-224 can be configured for strain gauge input.

The gain to be applied on each channel is specified with low and high input limits.

For example, the AI-224 available gains are 1, 2, 4, 8, 16, 32, 64, 128, 256 and the maximum input range is the full 20V differential span.

To select a gain of 128, you must specify input limits of [-0.1V, 0.1V]:

```
// Configure channels 0,1 to use gain 128 in differential mode
aiSession.CreateAIChannel(“pdna://192.168.100.2/Dev0/Ai0,1”,
                          -0.1,
                           0.1,
                          UeiAIChannelInputModeDifferential);
```

Be mindful of your gain setting. Note that when reading any of the channels in point-by-point mode, the hardware actively keeps the data just below the gain-limit. When the gain is set too high, the output will appear as an inverted approximate of the actual signal, scaled down under the gain limit. Try a lower gain value, or begin with one.

To program the excitation circuitry, you need to configure the channel list using the session object method **CreateAIVExChannel()** instead of **CreateAIChannel()**.

This method also gives you the ability to select the bridge configuration you want and to select whether or not you wish to obtain the acquired data already scaled in mV/V (acquired voltage divided by actual excitation voltage), as follows:

```
// Configure channels 0,1 to use a gain of 128 in differential mode,
// program the excitation to 10V and turn on scaling with excitation

aiSession.CreateAIVExChannel("pdna://192.168.100.2/Dev0/Ai0,1",
                             -0.1,0.1,
                             UeiSensorFullBridge,
                             10.0,
                             true,
                             UeiAIChannelInputModeDifferential);;
```

CreateAIVExChannel() only gives access to a few of the channel properties.

You can access advanced channel properties (such as offset nulling, shunt calibration, bridge completion) using channel objects associated with each channel configured in the resource string.

You will first need to get a pointer to the channel object for wich you wish to change properties using the index of the channel in the channel list:

```
// Get pointer to channel object

CUeiAIVExChannel *pChan =
dynamic_cast<CUeiAIVExChannel*>session.GetChannel(index);
```

2.3.1 Bridge Completion

Use **CreateAIVexChannel()**'s bridgeType parameter to specify whether you are using a full-, half- or quarter-bridge configuration.

If quarter- or half-bridge is specifed, the bridge completion circuitry will be enabled automatically. You can specify the bridge completion DAC level with:

```
// Set bridge completion DAC level

pChan->SetBridgeCompletionSetting(0.0);
```

Using a setting value of 0.0 will automatically calculate the proper setting value to complete the bridge (make sure your strain gauge or load cell is not under stress). Start the session, read a few data points and verify that they are close to 0.0. Stop the session and read the setting value that was calculated.

```
// Get bridge completion DAC level (auto-calculated by setting to 0.0)

bcSetting = pChan->GetBridgeCompletionSetting();
```

2.3.2 AC Excitation

CreateAIVexChannel() configures the excitation as a DC signal by default. You can change it to an AC signal by changing the channel “frequency “attribute”:

```
// Change the excitation frequency property (default value is 0.0 for DC)
pChan->SetExcitationFrequency(60.0);
```

The AC excitation function is supported by hardware, but not supported in software release 4.6. Contact UEI for more information of how to get this function.

2.3.3 Offset Nulling

Offset Nulling is turned-on using the channel object:

```
// enable Offset Nulling
pChan->EnableOffsetNulling(true);
```

You then need to set the offset nulling setting which will program the offset nulling DAC.

```
// set Offset Nulling (0.0 for auto)
pChan->SetOffsetNullingSetting(0.0);
```

Using a setting value of 0.0 will automatically calculate the setting value that will balance the bridge (make sure your strain gauge or load cell is not under stress).

Start the session, read a few data points and verify that they are close to 0.0.

Stop the session and read the setting value that was calculated to balance your bridge.

```
// get Offset Nulling setting (auto-calculated by setting to 0.0)
offsetNullSetting = pChan->GetOffsetNullingSetting();
```

Store that value and program it using **SetOffsetNullingSetting()** each time you start a strain measurement session. If you change anything in your bridge wiring, you will need to re-do the offset nulling setting calculation.

2.4 Configuring the Timing

You can configure the AI-224 to run in simple mode (point by point) or high-throughput buffered mode (ACB mode), or high-responsiveness (DMAP) mode.

In simple mode, the delay between samples is determined by software on the host computer. In DMAP mode, the delay between samples is determined by the AI-224 on-board clock and data is transferred one scan at a time between PowerDNA and the host PC. In buffered mode, the delay between samples is determined by the AI-224 on-board clock and data is transferred in blocks between PowerDNA and the host PC.

The following sample shows how to configure the simple mode. Please refer to the “UeiDaq Framework User’s Manual” to learn how to use other timing modes.

```
// configure timing of input for point-by-point (simple mode)
aiSession.ConfigureTimingForSimpleIO();
```

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2.5 Read Data

Reading data is done using *reader* object(s). The following sample code shows how to create a scaled reader object and read samples.

```
// create a reader and link it to the analog-input session’s stream
CUeiAnalogScaledReader aiReader(aiSession.GetDataStream());
// the buffer must be big enough to contain one value per channel
double data[2];
// read one scan, where the buffer will contain one value per channel
aiReader.ReadSingleScan(data);
```

2.6 Cleaning-up the Session

The session object will clean itself up when it goes out of scope or when it is destroyed. To reuse the object with a different set of channels or parameters, you can manually clean up the session as follows:

```
// clean up the session
aiSession.CleanUp();
```

Chapter 3 Programming with the Low-level API

The PowerDNA cube and PowerDNR RACKtangle and HalfRACK can be programmed using the low-level API. The low-level API offers direct access to PowerDNA DAQBios protocol and also allows you to access device registers directly.

However, we recommend that, when possible, you use the UeiDaq Framework High-Level API (see **Chapter 2**), because it is easier to use. You should need to use the low-level API only if you are using an operating system other than Windows.

For additional information about low-level programming of the AI-224, please refer to the PowerDNA API Reference Manual document under:

Start » Programs » UEI » PowerDNA » Documentation

Refer to the PowerDNA API Reference Manual on how to use the following low-level functions of AI-224, as well as others related to cube operation:

Function	Description
`DqAdv224Read`	Returns continously sampled data from input channel.
`DqAdv224SetAveraging`	Sets the data averaging factor for any channel.
`DqAdv224SetBridgeCompletion`	Sets the internal bridge completion voltage.
`DqAdv224SetExcitation`	Sets the excitation voltage [-20V, +20V] of a channel.
`DqAdv224SetFIR`	Sets the FIR configuration for one or more channels.
`DqAdv224SetNullLevel`	Sets the nulling voltage and will null at gains up to 40.

3.1 Decimation

The default decimations and clock multiplication factors for the AI-224 are:

```
// FIR0 decimation-1,   2 = 3:1 is

static uint16 fir_tbl_decim0 [8] =
{   2,   2,   5,  11,  23,  47,   95,  95};

// FIR1 decimation-1 is

static uint16 fir_tbl_decim1 [8] =
{   0,   1,    1,   1,    1,   1,    1,   3};

// decimation factors multiplied together:

static uint16 fir_clock_mult [8] =
{   3,   6,   12,  24,   48,  96,  192, 384};
```

The first element (index 0) is for output data rates from >50,000 to 100,000 samples per second. The remainder of the elements of the array are:

Index	Data Rate [S/sec]	
0	> 50000	≤ 100000
1	> 25000	≤ 50000
2	> 12500	≤ 25000
3	> 6250	≤ 12500
4	> 3125	≤ 6250
5	> 1562.5	≤ 3125
6	> 781.25	≤ 1562.5
7	> 390.625	≤ 781.25

For all output data rates the clock source varies from >150,000 to 300,000Hz.

Appendix A

A. Accessories

The following cables and STP boards are available for the AI-224 layer.

DNA-CBL-62

This is a 62-conductor round shielded cable with 62-pin male D-sub connectors on both ends. It is made with round, heavy-shielded cable; 2.5 ft (75 cm) long, weight of 9.49 ounces or 269 grams; up to 10ft (305cm) and 20ft (610cm).

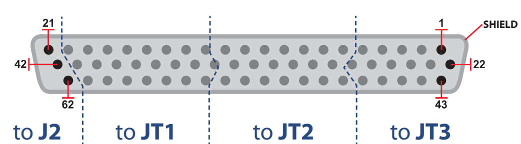
DNA-STP-62

The STP-62 is a Screw Terminal Panel with three 20-position terminal blocks (JT1, JT2, and JT3) plus one 3-position terminal block (J2). The dimensions of the STP-62 board are 4w x 3.8d x1.2h inch or 10.2 x 9.7 x 3 cm (with standoffs). The weight of the STP-62 board is 3.89 ounces or 110 grams.

DB-62 (female)
62-pin connector:

62	to J2	**42**	to J2	**21**	to J2
61	to JT1	**41**	to JT1	**20**	to JT1
60	to JT1	**40**	to JT1	**19**	to JT1
59	to JT1	**39**	to JT1	**18**	to JT1
58	to JT1	**38**	to JT1	**17**	to JT1
57	to JT1	**37**	to JT1	**16**	to JT1
56	to JT1	**36**	to JT1	**15**	to JT1
55	to JT2	**35**	to JT1	**14**	to JT1
54	to JT2	**34**	to JT2	**13**	to JT2
53	to JT2	**33**	to JT2	**12**	to JT2
52	to JT2	**32**	to JT2	**11**	to JT2
51	to JT2	**31**	to JT2	**10**	to JT2
50	to JT2	**30**	to JT2	**9**	to JT2
49	to JT2	**29**	to JT2	**8**	to JT2
48	to JT3	**28**	to JT3	**7**	to JT2
47	to JT3	**27**	to JT3	**6**	to JT3
46	to JT3	**26**	to JT3	**5**	to JT3
45	to JT3	**25**	to JT3	**4**	to JT3
44	to JT3	**24**	to JT3	**3**	to JT3
43	to JT3	**23**	to JT3	**2**	to JT3
		22	to JT3	**1**	to JT3

JT3 — 20-position terminal block:	JT2 — 20-position terminal block:	JT1 — 20-position terminal block:	J2 — 5-position terminal block:	
22	55	20	**5**	SHIELD
1	13	41	**4**	GND
43	34	61	**3**	62
23	54	19	**2**	42
2	12	40	**1**	21
44	33	60		
24	53	18		
3	11	39		
45	32	59		
25	52	17		
4	10	38		
46	31	58		
26	51	16		
5	9	37		
47	30	57		
27	50	15		
6	8	36		
48	29	56		
28	49	14		
GND	7	35		



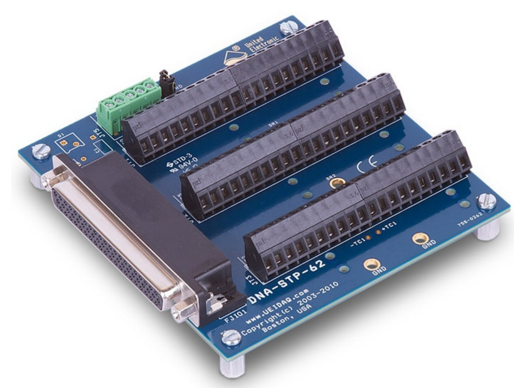


Figure A-1. Pinout and photo of DNA-STP-62 screw terminal panel

Appendix B

Shunt Calibration Support in Framework

B.1 Introduction

Strain-gauges and load cell measurements are typically based on the Wheatstone bridge, which allows the measurement of the very small resistance changes that characterize strain gauges.

The values measured from a Wheatstone bridge are very sensitive to the resistance of its branches and can be attenuated by lead resistances.

Shunt calibration is used to compensate for the loss of sensitivity caused by leadwire resistances (The strain gauge is “desensitized”).

Shunt calibration is the action of simulating a load on one of the branches of a Wheatstone bridge with a resistor of a known value and comparing the measured value to the calculated ideal value.

The ratio between the ideal value and the measured value is called “Gain Adjustment Factor”. It should be very close to 1. Multiplying the measurement value by the gain adjustment factor compensates for the loss of sensitivity introduced by the lead resistances in a four-wire gauge.

B.2 Theory

Load cell and strain gauge measurement are normally done through a Wheatstone bridge.

For load cells, the Wheatstone bridge is built into the cell.

For strain gauges, the bridge is part of the wiring.

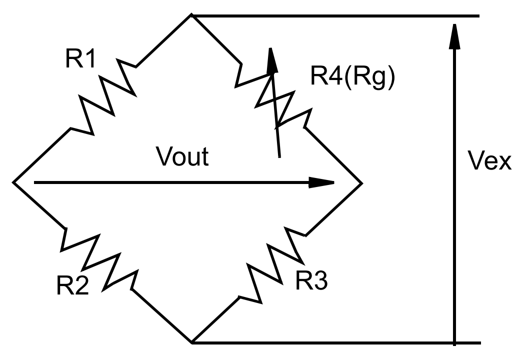


Figure B-1. Strain Gauge Bridge

V_{ex} is the excitation voltage applied to the bridge by the instrument.

V_{out} is the output voltage measured by the instrument.

The formula to calculate V_{out}, knowing V_{ex}, is:

Eq. 1:

$$Vout = Vex\left(\frac{R4}{R3 + R4} - \frac{R1}{R1 + R2}\right)$$

Simulating a load is usually done by adding a larger resistance in parallel with one of the branches. To simulate a compression load, we need to add a shunt resistance to Rg and to simulate a tension load, we need to add a resistance to R3.

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The following figure assumes that all branch resistances are equal to Rg (strain gauge resistance) and that the R4 branch was shunted with a resistance Rs (shunt resistance).

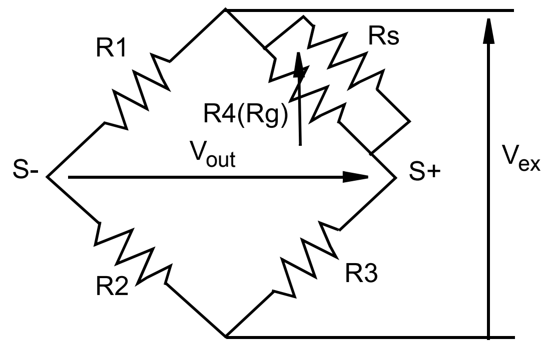

Figure B-2. Strain Gauge with Shunt Resistance R_s Added

After replacing R4 with (R4.Rs)/(R4+Rs) in Equation 1, the voltage output of the bridge when the shunt calibration resistor is enabled is:

Eq. 2:
$$\mathrm{Vout} = \mathrm{Vex}\left(\frac{\frac{R4}{R4+Rs}}{R3+\frac{R4}{R4+Rs}} - \frac{R1}{R1+R2}\right)$$

The voltage output change after enabling the shunt resistor is
$\Delta V_{out} = V_{outs} - V_{out}$.

Eq. 3:
$$\Delta\mathrm{Vout} = \mathrm{Vex}\left(\frac{\frac{R4}{R4+Rs}}{R3+\frac{R4}{R4+Rs}} - \frac{R4}{R3+R4}\right)$$

In most applications, all branches of the Wheatstone bridge use the same resistance. Standard values for Rg are 120, 350, and 1000 Ohms. After setting R1= R2= R3=Rg, Equation 3 becomes:

Eq. 4:
$$\Delta\mathrm{Vout} = -\mathrm{Vex}\left(\frac{Rg}{4Rs+2Rg}\right)$$

Shunting branch R3 instead of R4 to simulate a tensile load gives:

Eq. 5: $$\Delta\mathrm{Vout} = \mathrm{Vex}\left(\frac{\mathrm{Rg}}{4 \cdot \mathrm{Rs} + 2 \cdot \mathrm{Rg}}\right)$$

Now that we know how to calculate the theoretical offset on the Wheatstone bridge output when one of the branch resistances is changed with a known value, we can compare it with the measured value and get the Gain Adjustment Factor:

Eq. 6: $$\mathrm{Gaf} = \frac{\Delta\mathrm{VoutCalculated}}{\Delta\mathrm{VoutMeasured}}$$

Multiplying each measured values by the “Gain Adjustment Factor” gives us calibrated measurements.

Index