# AIP-24

## 24 Channel Analogue Input Board


## User Manual

# AIP-24

# User Manual

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|---|---|
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# Amendment History

| Issue Level | Issue Date | Author | Amendment Details |
|---|---|---|---|
| 1.1 | | | First draft |
| 1.2 | 24.11.97 | SEJ | Window front cover and logo. See ECN 98/085 |

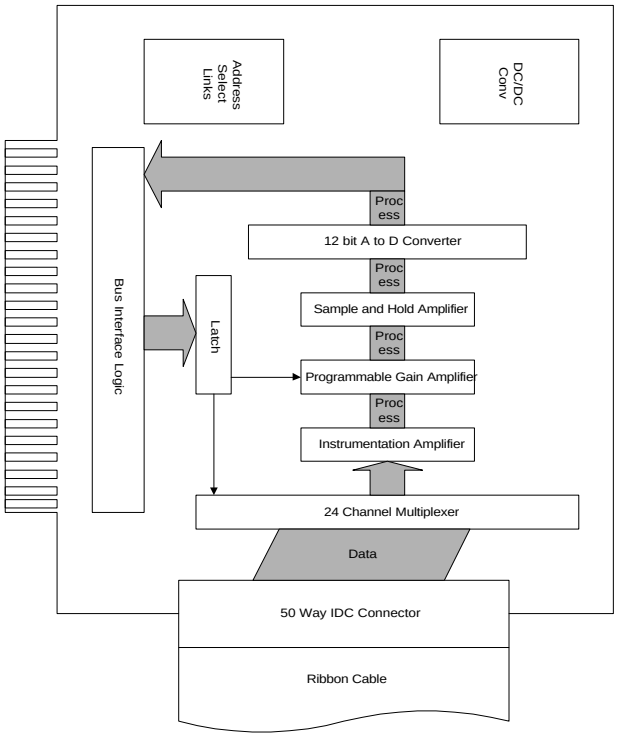
# 1.0 INTRODUCTION

This card provides 24 differential 12 bit analogue inputs. It is suitable for measuring voltages in the ranges of 0-10, -5 to +5 or-10 to +10 volts.

The AIP board may be thought of as s number of functional blocks each of which must be correctly handled in order to achieve the desired overall result. The main blocks are illustrated in the block diagram. The particular signal to be measured is selected from the 24 input channels by an electronic switch (Multiplexer) which is controlled by writing the channel number into a latch.

This signal is then conditioned by an instrumentation amplifier (to convert it to ground reference voltage) and amplified by a programmable gain amplifier which is also controlled by the latch referred to earlier as detailed in Section 2.2.

Finally, the voltage signal is converted by the A to D converter to a digital signal which may be read by the host computer as shown in detail later (Section 4).




## Quick Start for the Experience User

For those Users who are in a hurry to see this product perform and are sure that the factory settings for the ports of 300-303 Hex (768-771 Decimal) don't conflict with any other boards in the computer, then just plug the board in and run the program AIPMON on the demo disk.

The readings displayed are likely to change continually if the inputs are not connected. Any unused input should be shorted out for a zero reading to be guaranteed. Further changes can be induced by touching the bare pins of the IDC connector. This must not be attempted if there is any possibility that you are charged with static electricity.

# 1.0 SPECIFICATIONS

## 1.1 Electrical Specification

| | |
|---|---|
| Number of Inputs | 24 |
| Maximum Input Voltage | 12V |
| Power Requirement | 5V and +/- 12V D.C |
| Power Dissipation | 2 Watts |
| Conversion Time | 25 Microseconds |
| Settling Time | 25 Microseconds (Unity Gain) |
| Throughput | 16KHz on IBM AT |

## 1.2 Physical Specification

| | |
|---|---|
| Height | 107mm |
| Width | 15mm |
| Depth | 132mm |

## ELECTROMAGNETIC COMPATIBILITY (EMC)

This product meets the requirements of the European EMC Directive (89/336/EEC) and is eligible to bear the CE mark.

It has been assessed operating in a Blue Chip Technology Icon industrial PC. However, because the board can be installed in a variety of computers, certain conditions have to be applied to ensure that the compatibility is maintained. It meets the requirements for an industrial environment ( Class A product) subject to those conditions.

- The board must be installed in a computer system which provides screening suitable for the industrial environment.

- Any recommendations made by the computer system manufacturer/supplier must be complied with regarding earthing and the installation of boards.

- The board must be installed with the backplate securely screwed to the chassis of the computer to ensure good metal-to-metal (i.e. earth) contact.

- Most EMC problems are caused by the external cabling to boards. Analogue boards fitted with IDC ribbon cable connectors on the metal mounting bracket require particularly careful installation of the external cabling. It is imperative that any external cabling to the board is totally screened, and that the screen of the cable connects to the metal end bracket of the board and hence to earth. The cabling must be totally screened; the type of ribbon cable which is rolled to a round form with a braided wire screen is best. Standard ribbon cable will not be adequate unless it is contained wholly within the cabinetry housing the industrial PC. Keep the unscreened section as short as possible. The mounting bracket of the board includes a captive nut as an screen earth point. Connect the screen of the cable to this by the shortest possible wire.

- If difficulty with interference is experienced the cable should also be fitted with a ferrite clamp as close possible to the connector. The preferred type is the Chomerics clip-on style, type H8FE-1004-AS.

- It is recommended that cables are kept as short as possible, particularly when dealing with low level signals.

- Ensure that the screen of the external cable is bonded to a good RF earth at the remote end of the cable.

Failure to observe these recommendations may invalidate the EMC compliance.

> Warning
> This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

### EMC Specification

A Blue Chip Technology Icon industrial PC fitted with this card meets the following specification:

| | | |
|---|---|---|
| Emissions: | EN 55022:1995 | |
| | Radiated | Class A |
| | Conducted | Class A & B |
| Immunity: | EN 50082-1:1992 incorporating | |
| | Electrostatic Discharge | IEC 801-2:1984<br>Performance Criteria B |
| | Radio Frequency Susceptibility | IEC 801-3:1984<br>Performance Criteria A |
| | Fast Burst Transients | IEC 801-4:1988<br>Performance Criteria B |

# 2.0 USER ADJUSTMENTS

## 2.1 Selecting the Base Address (JP1)

The board may be located in any 62 pin ISA slot in the PC motherboard, but must be set up to appear at a specified position (or 'address') in the computer's port map.

Available positions are shown in the IBM-PC Technical Reference Guide. However, for those who do not possess a copy of this document a good place is the location normally allocated to the prototyping card as supplied by IBM. This address is 300 (hex) or 768 (decimal). All Blue Chip Technology cards are preset to this address at the factory.

However, no two devices should be used while set to the same address since contention will occur and neither board will work. If your machine contains a card with a conflicting address then another reasonably safe address is 200 to 21F (hex).

A set of links on the board set the base address of the board within the IBM-PC port map. The address is in binary with the presence of a link representing a 0 and the absence of a link representing a 1.

To set the base address to 300 hex (768 decimal) set the pattern on the links as indicated below:

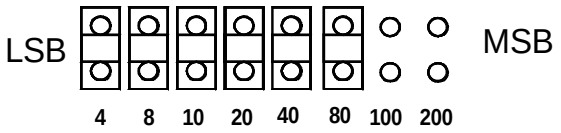



***Figure 1 - Selecting the Base Address***

More example addresses are shown in Appendix A.

Note: No Two cards must occupy the same address.

## 2.2 Port Map

In order to use the AIP card a channel must be selected, conversion started and data read back. This is controlled via four 8 bit ports which have specified functions as described below.

| Address | Read | Write |
|---|---|---|
| Base + 0 | N/A | Multiplexer channel select + gain select Start Conversion |
| Base + 1 | N/A | |
| Base + 2 | Lower 8 Bits of data | |
| Base + 3 | Upper four bits of data + busy bit + digital input bit | |

Bit 6 5 | 4 3 2 1 0

ADDRESS XX0H (W/O)

Gain Select
00 + x 1
01 + x 10
10 = x 100

Channel Select
(0 to 23)

# 3.0 ELECTRICAL OPTIONS

## 3.1 Input Connections

A 50 way insulation displacement connector (IDC) is provided on the PC rear panel of the board for input signal connection. If access to individual channels is required, a 50 way IDC ribbon cable may be used to connect the inputs to 50 way DIN rail mounting screw terminal block available from Blue Chip Technology as part number ST-24. The pins are numbered as shown in the following diagram.

Pins 1-48 contain the input channels. The analogue inputs are differential with the even numbered pins being positive and the odd numbered pins being negative on the AIP-24 to conform with the other cards in the range. Pin 49 and 50 are inputs to a TTL level buffer which appear as the top two bits on port 3. The action of shorting these pins to ground switches them from a 1 to a 0 thus providing a method of detecting a contact closure suitable for using as triggers for data acquisition software.

When the connector is viewed from the back of the system, odd numbered pins are on the left and even numbered pins are on the right with pin 1 at the top of the connector.

Pin Detail

| | | | |
|---|---|---|---|
| Pin 1 | O | O | Pin 2 |
| Pin 3 | O | O | Pin 4 |
| - | O | O | - |
| - | O | O | - |
| - | | | - |
| - | | | - |
| - | | | - |
| - | O | O | - |
| - | O | O | - |
| Pin 47 | O | O | Pin 48 |
| Pin 49 | O | O | Pin 50 |

View with gold edge connector downwards.

## 3.2 Connector Pin Details

| Function | | Pin | Pin | Function | |
|---|---|---|---|---|---|
| Channel 0 | -ve | 1 O | O 2 | Channel 0 | +ve |
| Channel 1 | -ve | 3 O | O 4 | Channel 1 | +ve |
| Channel 2 | -ve | 5 O | O 6 | Channel 2 | +ve |
| Channel 3 | -ve | 7 O | O 8 | Channel 3 | +ve |
| Channel 4 | -ve | 9 O | O 10 | Channel 4 | +ve |
| Channel 5 | -ve | 11 O | O 12 | Channel 5 | +ve |
| Channel 6 | -ve | 13 O | O 14 | Channel 6 | +ve |
| Channel 7 | -ve | 15 O | O 16 | Channel 7 | +ve |
| Channel 8 | -ve | 17 O | O 18 | Channel 8 | +ve |
| Channel 9 | -ve | 19 O | O 20 | Channel 9 | +ve |
| Channel 10 | -ve | 21 O | O 22 | Channel 10 | +ve |
| Channel 11 | -ve | 23 O | O 24 | Channel 11 | +ve |
| Channel 12 | -ve | 25 O | O 26 | Channel 12 | +ve |
| Channel 13 | -ve | 27 O | O 28 | Channel 13 | +ve |
| Channel 14 | -ve | 29 O | O 30 | Channel 14 | +ve |
| Channel 15 | -ve | 31 O | O 32 | Channel 15 | +ve |
| Channel 16 | -ve | 33 O | O 34 | Channel 16 | +ve |
| Channel 17 | -ve | 35 O | O 36 | Channel 17 | +ve |
| Channel 18 | -ve | 37 O | O 38 | Channel 18 | +ve |
| Channel 19 | -ve | 39 O | O 40 | Channel 19 | +ve |
| Channel 20 | -ve | 41 O | O 42 | Channel 20 | +ve |
| Channel 21 | -ve | 43 O | O 44 | Channel 21 | +ve |
| Channel 22 | -ve | 45 O | O 46 | Channel 22 | +ve |
| Channel 23 | -ve | 47 O | O 48 | Channel 23 | +ve |
| TTL Trigger Input (Pulled up to 5V by 4K7 Ohm) | | 49 O | O 50 | GND | |

# 4.0 OPERATING GUIDE

## 4.1 Using the Device

A total of 24 input signals may be connected to the AIP-24 contains only one analogue to digital converter chip the 24 inputs are achieved by using analogue multiplexers which select the appropriate channel s defined by the state of the lower 5 bits of the mutliplexwe select port (PORT 0). These feed the selected differential signal into an instrumentation amplifier which converts the signal into single ended drive. This in turn feeds the programmable gain amplifier (PGA 102) the gain of which is controlled by bits 5 and 6 f the multiplexer channel select port (PORT 0).

The output of the PGA is then taken to a sample and hold amplifier (AD585), which freezes the signal during conversion. Significant errors can arise when changing signals are measured by boards without a sample and hold amplifier.

The conversion "BUSY" signal appears as bit 5 of port 3 and can be monitored under software control to determine the end of the conversion cycle which takes about 25 microseconds. More information about the converter and the instrumentation amp can be found in the appropriate data sheet on the chip from Analog Devices Limited.

A typical sequence of events to use the card would be:

1. Select the channel by writing 0-23 to Base + 0. If gain is being used then the value written to Base + 0 when selecting the channel must tale this into account (see Port Map). For instance, if a gain of 10 is being used then 32 must be added to the required channel number or 64 for a gain of 100.
2. Write any value to Base + 1 to begin conversion.
3. Read Base = 3 and monitor the ADC busy bit. The ADC conversion time is 25 microseconds. When using a fast language (e.g. Assembler) it it necessary to ensure that the ADC has finished converting the analogue signal before reading the result. This s achieved by checking bit 5 of Base + 3. However, this is not necessary when using a slow language (e.g. Basic).

4. Read Base + 2.
5. Read Base + 3.
6. Combine Base +2 and Base + 3 to get the result.

## 4.2 Programming Guide

The value of an input may be determined by using the following method as a subroutine in Microsoft BASIC A or GW BASIC:

```
10      REM CH CONTAINS VALUE FOR REQUESTED CHANNEL
20      REM P=AIP24 BASE PORT NUMBER
30      OUT P,CH
40      OUT P+1,0 ;START CONVERSION
50      L=INP (P+2): H=INP (P+3) ;GET LOW AND HIGH HALVES OF NUMBER
60      IF H AND &H20 THEN 50 ;WAIT FOR CONVERSION TO FINISH
70      N=256*(H and 15) +L
80      N = N-2047 ;IF BI-POLAR MODE THIS LINE IS NEEDED
90      RETURN
100     REM N = THE ANALOGUE VALUE
```

## 4.3 Example Program

The following program written in Microsoft BASIC will run under the BASIC A or GW BASIC interpreter and is intended to display the values of the inputs of the AIP-24 ports on the screen in decimal. This enables the user to see the state of each input channel.

The base address used for the program is 300 Hex or 768 decimal which is the default factory setting for link A.

```
10      REM PROGRAM TO TEST AIP-24 BOARD
20      CLS : KEY OFF : LOCATE 1,1
30      P=0
40      FOR Y=1 TO 3
50      FOR X=1 TO 80 STEP 10
60      LOCATE Y, X
70      GOSUB 150
80      P=P+1
90      IF P>23 THEN P=0
100     PRINT N; "   ";
110     NEXT
120     NEXT
130     GOTO 40
```

```
150     OUT &H300, P
160     OUT &H301, O
170     A=INP (&H302) :B=INP (&H303)
180     C=B AND &HF
190     N=(256*C) +A
200     N=N 2047 ; TAKE THIS LINE OUT FOR UNI-POLAR MODE
210     RETURN
```

The program cycles continuously and has to be stopped by pressing Control-Break on the PC keyboard.

# 5.0 COMMERCIAL DATA ACQUISITION PACKAGES

The Blue Chip Technology Iap-24 can be used with almost any data acquisition package that can read information directly from a PC input port.

## 5.1 Use of the AIP-24 Board with ASYST

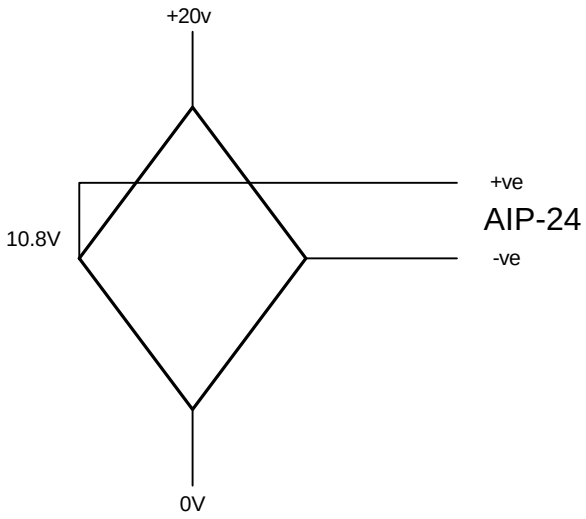
The board has been tested with and is installable as 2 IO.PORT devices in the ASYST scientific software package by Macmillan Software Company. It is not, however, installed as a normal analogue device.

For more details about this package and other PC data acquisition software, please contact Blue Chip Technology.

# 6.0 APPLICATION NOTES

## 6.1 Introduction to Concepts

In order to make best use of this board it is useful to understand the concepts of differential and common mode signals. A typical application might involve a bridge transducer as below:




Where voltages are expressed relative to the same zero (ground) voltage as used by the computer. This typically arises because both the transducer and computer use the safety earth as their zero volt reference.

Now the user wants to see the bridge signal which is (10.8 - 9.9)V or 0.9V.

The AIP does this automatically because its input is differential, i.e. it measures the difference between the two signals. The alternative type of input is called single-ended and measures an input relative to zero volts. Two single-ended inputs could be used to measure the bridge voltages above and the difference calculated by the computr to give the true differential bridge signal.

In the above example the input circuitry of the AIP board sees a differential signal of 0.9V superimposed upon a common mode signal of 9.9V. The common mode voltage is in a sense of common to both inputs. The AIP circuitry can accept input voltages of up to +/-12V with respect to the computer ground. Signals outside this range can lead to false readings both on the channel involved and other channels. For this reason the board is said to have a +/- 12V common mode voltage range. It is not acceptable to have for example a 3V signal superimposed upon a common mode signal of 11V, since one input would be at 14 which is outside the acceptable range.

When it is necessary to measure differential signals with a common mode component which exceeds the input capability of the AIP, then either individual isolation amplifiers can be used together with the AIP.

## 6.2 Common Mode Voltage

This board used solid-state multiplexers. These devices will not operate properly is either signal voltage input exceeds + or -12volts. These limits define the common mode voltage range. The board has a differential input and will accept signals which are floating with respect to the computer system ground. But these signals must still lie within the common mode voltage range (CMVR) in order to obtain satisfactory operation. In some cases it may be necessary to tie external signals to the computer ground via suitable resistors to hold them within CMVR. Failure to do so may result in erratic readings. The board provides resistors R10 and R11 (1M) which may be used to pull the input signals towards ground, by fitting links LG and LH. This resistor value generally proves satisfactory, but lower values may be needed in electrically noisy environments. Since the resistors in combination with the multiplexer resistance form a potential divider, there will be a small attenuation of the signal. This is less than one bit with 1M resistors and can easily be corrected for during calibration.

## 6.3 Settling Time

When the input channel is switched the analogue circuitry will take a short time to settle to the new value. This is referred to as the settling time.

The settling time is a combination of the settling times for the individual stages involved i.e. instrumentation amplifier, programmable gain amplifier, sample and hold together with an filters. The switching time of the mutliplexer is short compared with these other factors and so is not considered further. The manufacturers figures for settling to 0.01% are given below in microseconds:

| | Gain = 1 | 10 | 100 |
|---|---|---|---|
| Instrumentation Amplifier | 15.0 | 15.0 | 15.0 |
| Programmable Gain Amplifier | 2.8 | 2.8 | 8.2 |
| Sample and Hold | 5.0 | 5.0 | 5.0 |
| **Sum** | 22.8 | 22.8 | 28.2 |

These figures are worst case for a full 20V step input and ignore the fact that all stages settle together, not sequentially.

A major contribution is made to settling time by the on-board filters. Three RC filters are provided on the board to reduce interference by high frequency noise. Two filters are formed by R12/C19 and R13/C20. The third filter is formed by C24 and the on-resistance of the multiplexer devices, (typically 360R total). The three filters give a nominal time constant of 10uS. However, a period of around ten time constants is required to allow settling to .01%.

In cases where very fast conversion is required the filters may be eliminated be removing C19, C20 and C24. Further speed improvements may be made by eliminating the programmable gain amplifier assuming only unity gain is required and by using faster amplifiers. Conversion speed may ablso be improved by using alternative pin compatible devices for the ADC.

The program 'SETTLAIP' allows the settling time to be measured. In order to use the program set the board address to 300H, apply 10 volts to channel 0 and 0 volts to channel 1. The program creates a variable setting delay. When the program is run it will show how the reading is effected by reducing the delay time allowed for settling.

The delay is set by executing the assembler 'LOOP' instruction number of times. The program displays the number of 'LOOPS' performed, the reading obtained and the ratio of this to the reading with a very long settling time. Theoretically, the reading reaches 0.63 of its full value, when the settling time is equal to the time constant. At least five time constants should be allowed for settling to 12 bit accuracy.

## 6.4 Range Selection

The board my used to measure either uni-polar (positive polarity only) or bi-polar (negative and positive) signals according to the link settings on the board. The standard version of the board as supplied from the factory is bi-polar +10V to -10V (i.e. 5mV/vbit). Other versions can be supplied to special order or the board may be re-configured and re-calibrated by the user.

The input range is set by links Links LC and LF select uni-polar or bi-polar mode. The bi-polar mode is selected by fitting links at positions LC and LD only, whereas the uni-polar mode is selected by fitting links at LE and LF. In the bi-polar mode RV2 is used to set the reading with a short circuit input to 2047 (zero setting). For both uni and bi-polar modes LB sets the full scale span of the converter. In the position marked 2.5 (corresponding to 2.5mV/bit), the span is 10V i.e. 0 to +10V uni-polar or +5 to -5V bi-polar. Similarly, when LB is in the 5 position (5mV/bit) the span is 0 to +20V or +10V to -10V. Note that inputs above +12V cannot be measured properly as discussed in Section 6.1.

## 6.5 Calibration

### 6.5.1 Uni-polar +/-10V Range

i. Remove links LC, LD and fit at LE, LF. Check position of LB (normally 2.5) as discussed above.

ii. Apply 0.5 LSB (1.25mV) and adjust RV2 so that the reading is changing between 0 and 1. This sets the zero point.

iii. Apply 10.000V to one input and check the measured value. Adjust RV1 if needed to give the correct reading. The standard factory calibration is to adjust the reading to be 4000 for 10.000V input (i.e. 2.5mV/bit). This sets the full scale reading.

### 6.5.2 Bi-polar

i. Remove links LE, LF and fit at LC, LD. Check position of LB as 6.3 above.

ii. Short one input and adjust RV2 so that the reading is 2047.

iii. Apply either +5.000V (for LB=2.5) or +10.000V (for LB=5) and adjust RV1 to give a reading of 4047.

iv. Apply -5.000V or +10.000V corresponding to iii and check reading is 47+/-1.

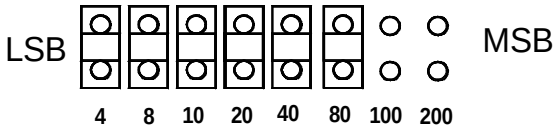
Note for the above procedures sample software is available on the disk supplied with the board which performs an average and allows finer adjustment of the calibration.

Whilst ever effort has been taken to ensure that the information provided is accurate, Blue Chip Technology cannot assume responsibility for any errors in this manual or their consequences. Should any errors be detected, the company would greatly appreciate being informed of them preferably in writing. A policy of continuous product development is operated, resulting in the contents of this document being subject to change without notice.

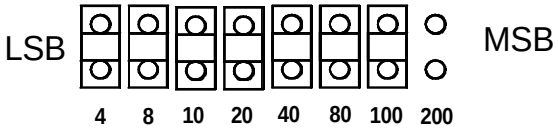
# APPENDIX A

Note: View board with back panel on RHS.

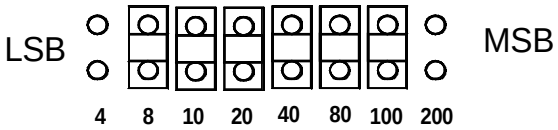
**Address Settings for Port 300H**



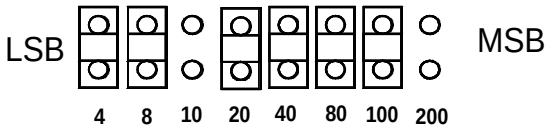

**Address Settings for Port 200H**



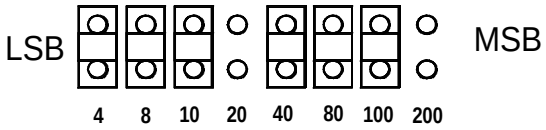

**Address Settings for Port 204H**



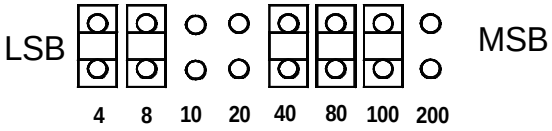

**Address Settings for Port 210H**



**Address Settings for Port 220H**




**Address Settings for Port 230H**



# APPENDIX B

## PC/XT/AT Port Map
## I/O Address Map

| Address (Hex) | Allocated to |
|---|---|
| 000-01F | DMA Controller 1, 8237A-5 |
| 020-03F | Interrupt Controller 1, 8259A |
| 040-05F | Timer, 8254 |
| 060-06F | Keyboard Controller 8742; Control Port B |
| 070-07F | RTC And CMOS RAM, NMI Mask (Write) |
| 080-09F | DMA Page Register (Memory Mapper) |
| 0A0-0BF | Interrupt Controller 2, 8259 |
| 0F0 | Clear NPX (80287) Busy |
| 0F1 | Reset NPX, 80287 |
| 0F8-0FF | Numeric Processor Extension, 80287 |
| 1F0-1F8 | Hard Disk Drive Controller |
| 200-207 | Reserved |
| 278-27F | Reserved For Parallel Printer Port 2 |
| 2F8-2FF | Reserved For Serial Port 2 |
| 300-31F | Reserved |
| 360-36F | Reserved |
| 378-37F | Parallel Printer Port 1 |
| 380-38F | Reserved For SDLC Comms, Bisynch 2 |
| 3A0-3AF | Reserved For Bisynch 1 |
| 3B0-3BF | Reserved |
| 3C0-3CF | Reserved |
| 3D0-3DF | Display Controller |
| 3F0-3F7 | Diskette Drive Controller |
| 3F8-3FF | Serial Port 1 |

# APPENDIX C

## PC/XT Interrupt Map

| Number | Usage |
|---|---|
| NMI | Parity |
| 0 | Timer |
| 1 | Keyboard |
| 2 | Reserved |
| 3 | Asynchronous Communications<br>(Secondary) SDLC Communications |
| 4 | Asynchronous Communications<br>(Primary) SDLC Communications |
| 5 | Fixed Disk |
| 6 | Diskette |
| 7 | Parallel Printer |

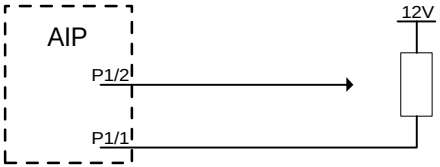
# APPENDIX D

## AT Interrupt Map

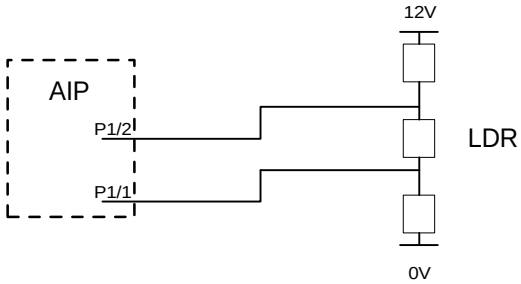
| Level | | Function |
|---|---|---|
| Microprocessor NMI Parity or I/O Channel Check | | |
| Interrupt Controllers | | |
| CTLR 1 | CTLR2 | |
| IRQ 0 | | Timer Output 0 |
| IRQ 1 | | Keyboard (Output Buffer Full) |
| IRQ 2 | | Interrupt from CTLR 2 |
| | IRQ 8 | Realtime Clock Interrupt |
| | IRQ 9 | Software redirected to INT 0AH (IRQ 2) |
| | IRQ 10 | Reserved |
| | IRQ 11 | Reserved |
| | IRQ 12 | Reserved |
| | IRQ 13 | Coprocessor |
| | IRQ 14 | Fixed Disk Controller |
| | IRQ 15 | Reserved |
| IRQ 3 | | Serial Port 2 |
| IRQ 4 | | Serial Port 1 |
| IRQ 5 | | Parallel Port 2 |
| IRQ 6 | | Diskette Controller |
| IRQ 7 | | Parallel Port 1 |

# Typical Methods of Interfacing From the AIP Card to Other Circuitry

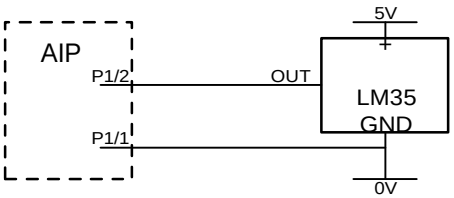
Single Ended Input From A Linear Transducer



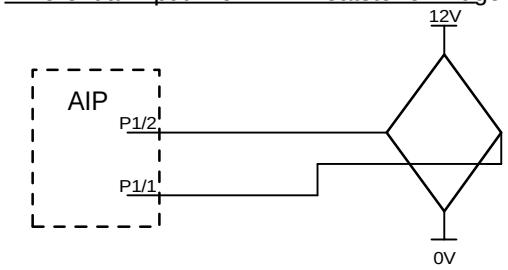

Differential Input From An LDR

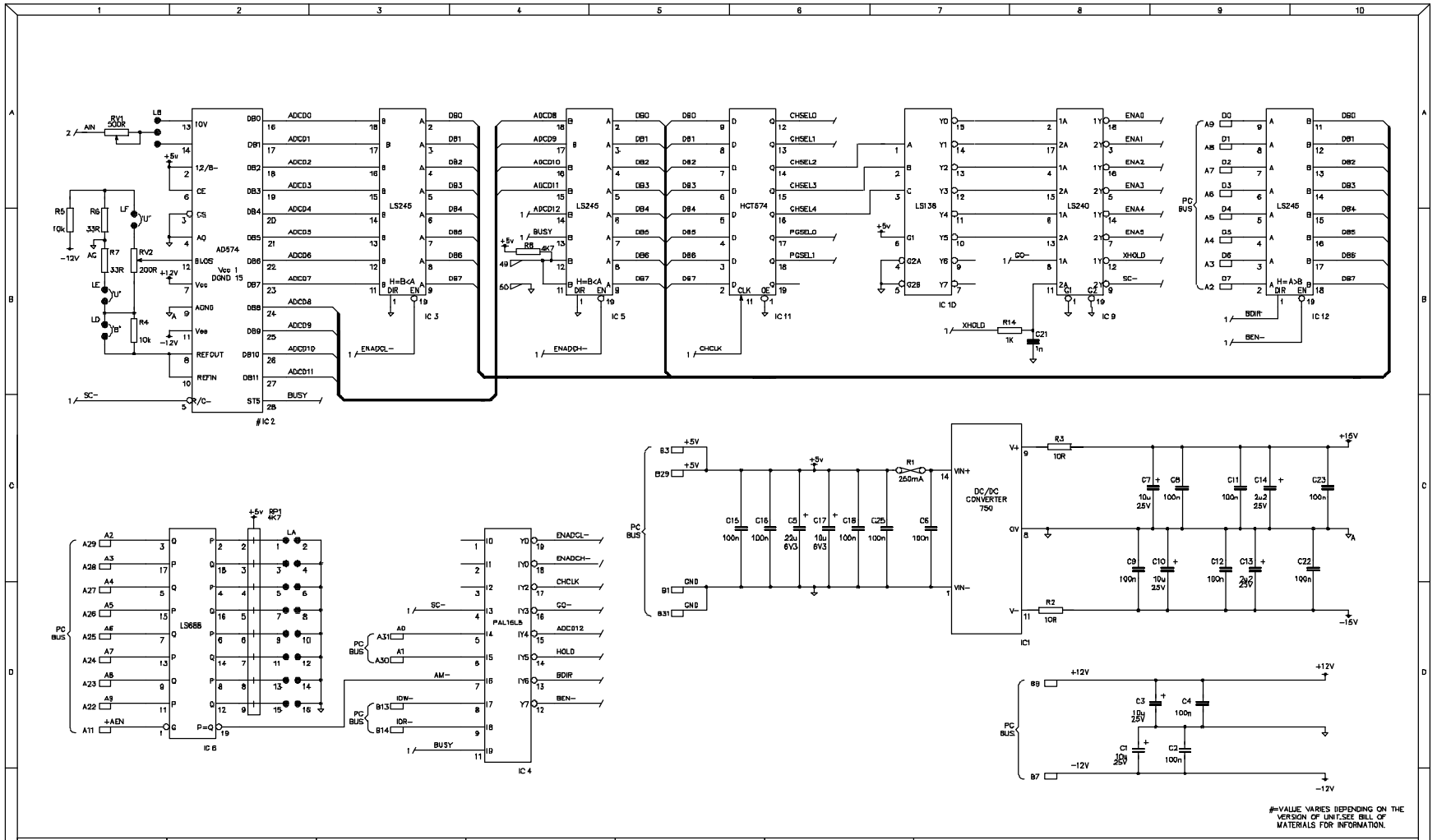



Variable Voltage Input From A Temperature Censor

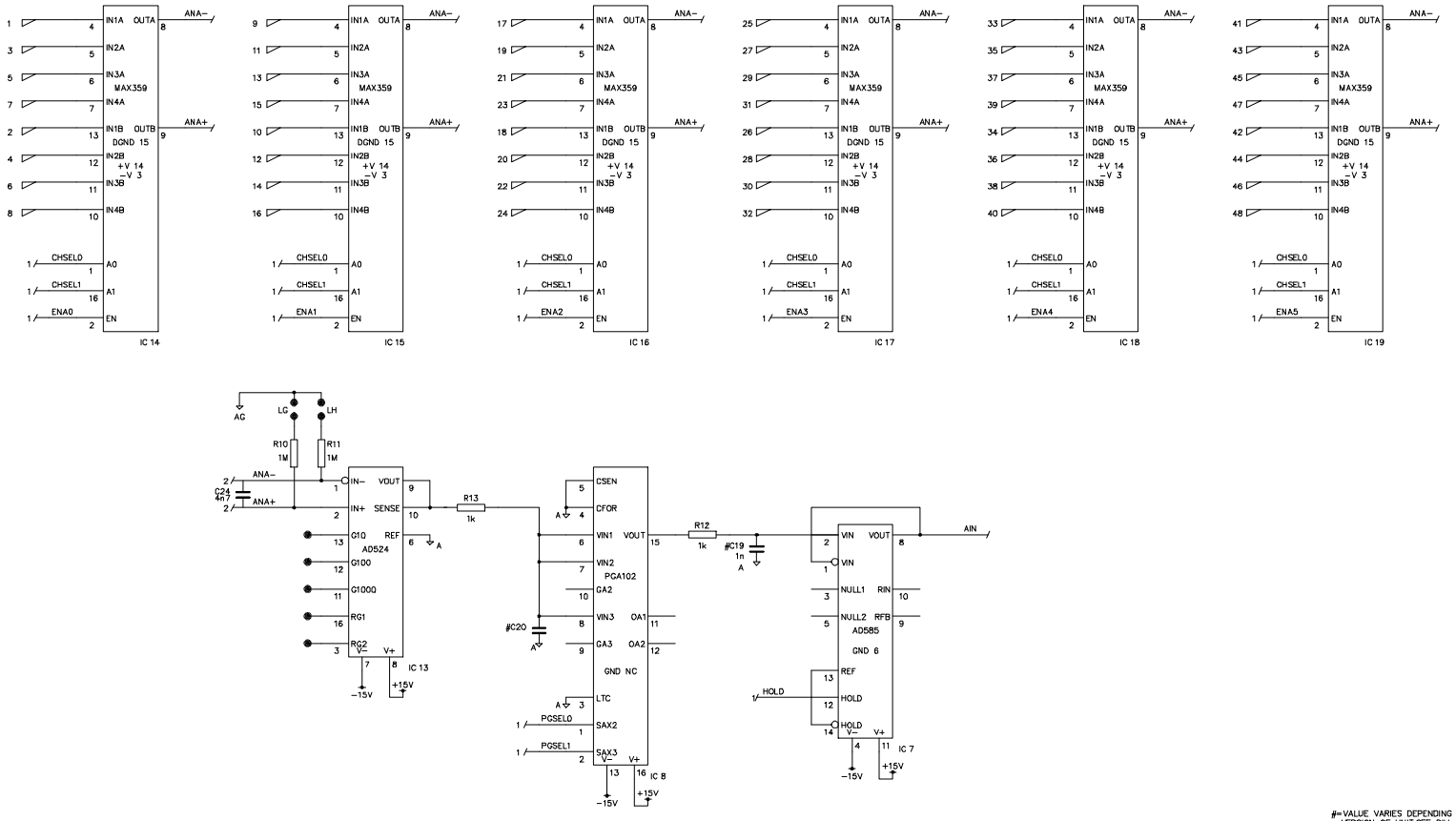



Differential Input From A Wheatstone Bridge






| ISSUE NO:– | | | ISSUE NO:– | | | ISSUE NO:– | | | ISSUE NO:– | | | ISSUE NO:– 3<br>SCHEMATIC UPDATED TO CURRENT ISSUE OF PARTS LIST. | | | ISSUE NO:– 2<br>POLARITY OF CAPACITORS ADDED | | | BLUE CHIP TECHNOLOGY LIMITED<br>MAIN AVENUE, HAWARDEN INDUSTRIAL PARK, DEESIDE, CH5 3PP TEL: (0244) 520222 TELEX. 61471 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DWN. | APPD. | DATE | DWN. | APPD. | DATE | DWN. | APPD. | DATE | DWN. | APPD. | DATE | DWN. | APPD. | DATE | DWN. | APPD. | DATE | SCALE(A3) 0.66<br>CHK'D MMc<br>DRAWN S.E.<br>DATE: 87/09/09 | TITLE:<br>AIP24 REV.F<br>ADC,DIGITAL & POWER SUPPLY CIRCUITS<br>DRAWING NUMBER. AIP24F1C ISS: 3 |
| | | | | | | | | | | | | GM | MMc | 17/01/91 | A.P.W. | MMc | 87/10/14 | | |




#=VALUE VARIES DEPENDING ON THE VERSION OF UNIT.SEE BILL OF MATERIALS FOR INFORMATION.

| ISSUE NO: – | ISSUE NO: – | ISSUE NO: – | ISSUE NO: – | ISSUE NO: – 3<br>IC's 14 TO 19 WERE DG509 | ISSUE NO: – 2<br>SCHEMATIC UPDATED TO CURRENT PARTS LIST. |
|---|---|---|---|---|---|
| DWN. APPD. DATE | DWN. APPD. DATE | DWN. APPD. DATE | DWN. APPD. DATE | DWN. APPD. DATE | DWN. APPD. DATE |
| | | | | MMc 10-06-91 | GM MMc 17/01/91 |

**BLUE CHIP TECHNOLOGY LIMITED**

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| | |
|---|---|
| SCALE(A3) 0.66 | TITLE: AIP24 REV.F<br>ANALOG INPUT PATH |
| CHK'D MMc | |
| DRAWN S.E. | |
| DATE: 87/09/09 | DRAWING NUMBER: AIP24F2C ISS: 2 |