User's Manual

TPS-1

User's Manual: Hardware

RENESAS ASSP
Ethernet Controller for PROFINET IO Devices

Renesas Electronics
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Instructions for the use of product

In this section, the precautions are described for over whole of CMOS device. Please refer to this manual about individual precaution. When there is a mention unlike the text of this manual, a mention of the text takes first priority

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   - The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
     In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

     In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the MCU. It is intended for users designing application systems incorporating the MCU. A basic knowledge of electric circuits, logical circuits, and MCUs is necessary in order to use this manual.

The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the TPS-1. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
Data Sheet	Hardware overview and electrical characteristics	TPS-1 Datasheet	R19DS0069EJ
User's manual for Hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and operation descriptiont	TPS-1 User's Manual: Hardware	This User's manual
User's manual		User Manual TPS-1	Note
Driver Manual	TPS-1 API functions	Driver Interface TPS-1	Note

Note: These documents are available from Phoenix Contact Software.

2. Notation of Numbers and Symbols

Note : Explanation of (Note) in the text

Caution : Item deserving extra attention

Remark : Supplementary explanation to the text

Numeric notation : Binary XXXb

Decimal XXXX

Hexadecimal XXXXH or 0x XXXX

Prefixes representing powers of 2 (address space, memory capacity)

k (kilo): 210 = 1024

M (mega): 220 = 10242 = 1.048.576

G (giga): 230 = 10243 = 1.073.741.824

Data Type : Word 32 bits

Halfword 16 bits

Byte 8 bits

3. List of Abbreviations and Acronyms

Abbreviation	Full Form
CSI	Clocked Serial Interface
FO	Fiber Optic
FPBGA	Fine Pitch Ball Grid Array
GND	Ground Potential
GPIO	General Purpose Input /Output
I	Input
I/O or IO	Input/Output
MISO	Master in Slave out (SPI signal)
MOSI	Master out Slave in (SPI signal)
MRP	Media Redundancy Protocol (IEC 61158)
O	Output
PCB	Printed Circuit Board
PCF	Photonic Crystal Fiber
PECL	Positive-Emitter-Coupled Logic
PLL	Phase Locked Loop
POF	Plastic Optical Fiber
POR	Power On Reset
RJ-45	Ethernet connection (copper wire)
SC-RJ	Ethernet connection (fiber optic)
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
n.c.	Not connected
ppm	Parts per Million

Abbreviation	Full Form
AR	Application Relation (PROFINET terms)
CR	Communication Relation (PROFINET terms)
I&M	Identification & Maintenance
IRT	Isochronous Real-Time (PROFINET operating mode)
NRT	Non Real Time (PRFINET terms)
PNIO	PROFINET IO
RT	Real-Time

Table of Contents

1. Overview

1.1. Features

PROFINET Device Chip

- Integrated PROFINET CPU
- Host CPU interface (SPI-Slave or 8/16 bit parallel)
- SPI Master-Interface for direct connection of SPI-Slaves (to exchange process data)
- 48 GPIO for direct connection of digital peripheral signals (digital I/Os)
- Serial Flash interface
- Support of PROFINET IO communication channels NRT, RT, and IRT
- Watchdog support for connected host CPUs
- Compliance with PROFINET Conformance Class C
- Hardware support for time-critical PROFINET protocols, including PTCP with LLDP
- Firmware download during the manufacturing process via JTAG Boundary Scan interface, Ethernet or UART interface
- Firmware update via Ethernet interface with BOOTP/TFTP
- Easy configuration of host interfaces and GPIOs
- 2 Fast Ethernet Ports with integrated PHYs
  - 100 Mbit full duplex data transmission
  - IRT Bridge Delay < 3 µsec
  - Auto Negotiation
  - Auto Cross-Over
  - Auto Polarity
  - Support for 100Base-TX and 100Base-FX ports
  - Monitoring of fiber optic transmission links with integrated I^2C interfaces
- Power dissipation around < 1 W

Host Interface

- Serial (SPI up to 25 MHz) and parallel (8 or 16 bit) interface for use with an external host CPU
- Data exchange (cyclic and acyclic) with external host via integrated Shared Memory Area (event and interrupt controlled)
- 340 Byte maximum data for cyclic exchange (inclusive IOxS)
- One application relation available (firmware version 1.1)
- The TPS-1 firmware allows a up to 64 Slot/Subslots (e.g. 1 Slot with up to 64 Subslots)
- Configuration of all host interfaces with software tool; configuration data are stored in a boot Flash

1.2. Abstract

The PROFINET Device Chip TPS-1 is designed for easy and cost-efficient implementation of PROFINET interfaces for automation devices. It is a highly integrated single chip solution that meets all requirements of the PROFINET protocols. The configurable host interfaces facilitate the flexible realization of different use cases like direct connection of an external host CPU or digital I/Os without additional circuitry.

The TPS-1 complies with PROFINET Conformance Class C. The integrated components realize the complete interface functionality. The internal structure is designed to fulfill the requirements of the IRT protocol. Special synchronous signals are available to realize all synchronization tasks. To support line topologies in PROFINET networks, the TPS-1 is equipped with two integrated PHYs and an integrated IRT switch. Time-critical PROFINET protocols are supported by hardware.

For the complete implementation of a PROFINET device interface, only the TPS-1, a serial Flash device, an oscillator, and the physical adaptations for the Ethernet interface (transformers and connectors) are needed. The serial Flash component contains the individual chip configuration and firmware for the PROFINET CPU.

Due to the low space requirement and low power dissipation of the TPS-1, a PROFINET interface can also be integrated into automation devices with special requirements regarding housing size and protection classes. Conductor routing between the balls is still possible in order to keep down PCB cost.

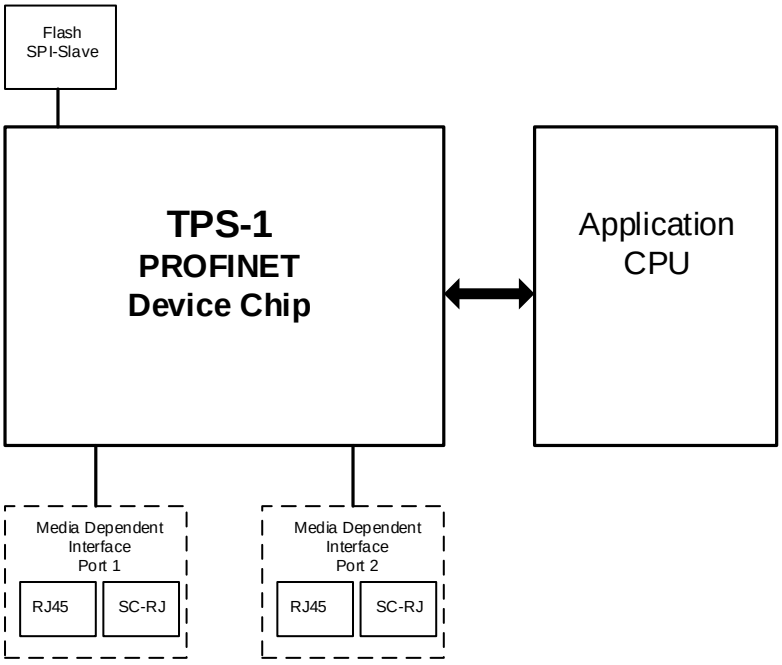

Figure 1-1: TPS-1 Overview

1.3. Block Diagram

The block diagram shows the internal structure and main components of the TPS-1.

The additional serial boot Flash component, the oscillator and the physical adaptation for the Ethernet interfaces are not listed.

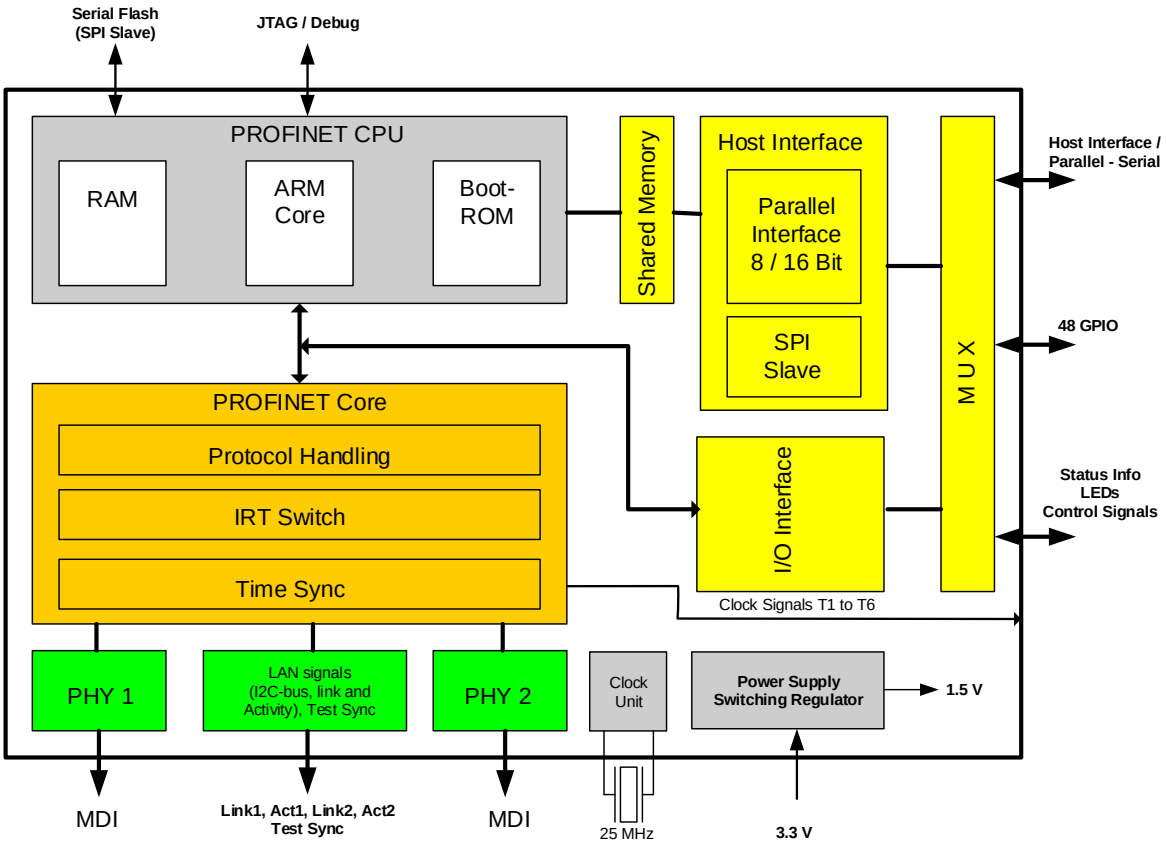

Figure 1-2: TPS-1 Block Diagram

The TPS-1 contains the PROFINET CPU, the PROFINET core, the I/O interface, and the Host Interface for connecting a host CPU.

The PROFINET core processes the PROFINET communication. All time-critical services are implemented in hardware to realize high performance.

The communication between an external host CPU and other PROFINET components is processed by the PROFINET CPU (connection establishment, administration and management of Application Relations, controlling of Ethernet connections, setup and monitoring of RT and IRT channels, etc.).

Simple IO interfaces can be realized with the I/O interface only (e.g. digital I/Os)

2. Pin function

2.1. Signal overview and description

Table 1 contains an overview about all signals of the TPS-1.

Table 2-1: TPS-1 signal overview and description

Pin	Designation	Type	Function	Remark
	SPI Master for Boot Flash ROM			
M12	CS_FLASH_OUT	O	SPI Master Interface Firmware Flash: Chip Select (TPS-1)	active low
N13	SPI3_SCLK_OUT	O	SPI Master Interface Firmware Flash: CLOCK (TPS-1)	
M13	SPI3_SRXD_IN	I	SPI Master Interface Firmware Flash: Receive Data (TPS-1) - MISO	
M14	SPI3_STXD_OUT	O	SPI Master Interface Firmware Flash: Send Data (TPS-1) - MOSI	
	Synchronization signals			
N12	TEST_SYNC	O	Clock signal for certification	Note 3)
J11	T1	O	Clock signal 1 (isochronous mode, IRT)	
H11	T2	O	Clock signal 2 (isochronous mode, IRT)	
G11	T3	O	Clock signal 3 (isochronous mode, IRT)	
F11	T4	O	Clock signal 4 (isochronous mode, IRT)	
E11	T5	O	Clock signal 5 (isochronous mode, IRT)	
D11	T6	O	Clock signal 6 (isochronous mode, IRT)	
	LED signals device status PROFINET			
B13	LED_BF_OUT	O	Control LED „Bus Failure“	active low
B11	LED_SF_OUT	O	Control LED „System Fail“	active low
C10	LED_READY_OUT	O	Control LED „Device Ready“	active low
B10	LED_MT_OUT	O	Control LED „Maintenance“	active low
	PHY Port 1			
C9	I2C_1_D_INOUT	I/O	Fiber Optic Port 1: I^2C-Bus “Data”	e.g. SC-RJ
C6	SCLK_1_INOUT	O	Fiber Optic Port 1: I^2C-Bus “Clock”	e.g. SC-RJ
C12	LINK_PHY1	O	LINK indication ETHERNET Port 1 (up or down)	active high
D10	ACT_PHY1	O	Activity ETHERNET Port 1	active high
F13	P1_TX_P	O	ETHERNET Port 1 transmit data (positive)	e.g. RJ45
F14	P1_TX_N	O	ETHERNET Port 1 transmit data (negative)	e.g. RJ45
E13	P1_RX_P	I	ETHERNET Port 1 Receive Data (positive)	e.g. RJ45
E14	P1_RX_N	I	ETHERNET Port 1 Receive Data (negative)	e.g. RJ45
B8	P1_SD_P	I	Fiber Optic Port 1: Signal Detect (positive)	e.g. SC-RJ
A8	P1_SD_N	I	Fiber Optic Port 1: Signal Detect (negative)	e.g. SC-RJ
B9	P1_RD_P	I	Fiber Optic Port 1: Receive Data (positive)	e.g. SC-RJ
A9	P1_RD_N	I	Fiber Optic Port 1: Receive Data (negative)	e.g. SC-RJ
B6	P1_TD_OUT_P	O	Fiber Optic Port 1: Transmit Data (negative)	e.g. SC-RJ
A6	P1_TD_OUT_N	O	Fiber Optic Port 1: Transmit Data (positive)	e.g. SC-RJ
A5	P1_FX_EN_OUT	O	Fiber Optic Port 1: Transmitter enable (active high)	e.g. SC-RJ
	PHY Port 2			
M11	I2C_2_D_INOUT	I/O	Fiber Optic Port 2: I^2C-Bus “Data”	e.g. SC-RJ
L11	SCLK_2_INOUT	O	Fiber Optic Port 2: I^2C-Bus “Clock”	e.g. SC-RJ
C11	LINK_PHY2	O	LINK indication ETHERNET Port 2 (up or down)	active high
A10	ACT_PHY2	O	Activity ETHERNET Port 2	active high
J13	P2_TX_P	O	ETHERNET Port 2 Transmit Data (positive)	e.g. RJ45
J14	P2_TX_N	O	ETHERNET Port 2 Transmit Data (negative)	e.g. RJ45
K13	P2_RX_P	I	ETHERNET Port 2 Receive Data (positive)	e.g. RJ45
K14	P2_RX_N	I	ETHERNET Port 2 Receive Data (negative)	e.g. RJ45
N8	P2_SD_P	I	Fiber Optic Port 2: Signal Detect (positive)	e.g. SC-RJ
P8	P2_SD_N	I	Fiber Optic Port 2: Signal Detect (negative)	e.g. SC-RJ
N9	P2_RD_P	I	Fiber Optic Port 2: Receive Data (positive)	e.g. SC-RJ
P9	P2_RD_N	I	Fiber Optic Port 2: Receive Data (negative)	e.g. SC-RJ
N6	P2_TD_OUT_P	O	Fiber Optic Port 2: Transmit Data (negative)	e.g. SC-RJ
P6	P2_TD_OUT_N	O	Fiber Optic Port 2: Transmit Data (positive)	e.g. SC-RJ

P5	P2_FX_EN_OUT	O	Fiber Optic Port 2: Transmitter enable (active high)	e.g. SC-RJ
	Oscillator			
N11	XCLK1	I	Connection external oscillator (1), 25 MHz	
P11	XCLK2	O	Connection external oscillator (2), 25 MHz	
	JTAG – Interface			
L4	TM0	I	Test Input 0 (Chip Test - 10k to GND)	pull down
J10	TM1	I	Test Input 1 (Chip Test - 10k to GND)	pull down
K5	TRSTN	I	JTAG-Interface: "Test Reset"	pull-down
L6	TMS	I	JTAG-Interface: "Test Mode Select"	pull-up
L7	TDO	O	JTAG-Interface: "Test Data Output"	
J5	TCK	I	JTAG-Interface: "Test Clock"	pull-up
L5	TDI	I	JTAG-Interface: "Test Data Input"	pull-up
	Reset / Test			
A12	RESETN	I	TPS-1 Reset (Global Reset)	active low
H12	ATP	I	Test pin for production test (n.c.)	
H13	EXTRES	O	External reference resistor (12.4 kΩ,1 %), connect to analog GND	
E10	TMC1	I	Test Mode Control 1 (production test)	pull down
K10	TMC2	I	Test Mode Control 2 (production test)	pull down
D6	TEST_1_IN	I	Test Pin 1 for hardware test of the TPS-1	pull down
D7	TEST_2_IN	I	Test Pin 2 for hardware test of the TPS-1	pull down
D8	TESTDOUT5	O	Test Data Output 5 (High Speed Signals for PHY)	
D9	TESTDOUT6	O	Test Data Output 6 (High Speed Signals for PHY)	
L8	TESTDOUT7	O	Test Data Output 7 (High Speed Signals for PHY)	
	Host interface			
A11	WD_IN	I	Watchdog input (from the Host)(the rising edge resets the watchdog counter of the TPS-1)	active high
B12	WD_OUT	O	Watchdog output (to the Host)	active low
K11	INT_OUT	O	Interrupt output (to the Host)	active low
	Boot interface (serial)			
C14	UART6_TX	O	Boot UART "Transmit Data"	
C13	UART6_RX	I	Boot UART "Receive Data"	
P12	BOOT_1	I	Forced Boot	
	Test signals for switching regulator			
H3	TEST1	I	Test Pin switching regulator (in combination with Test2, 3)	
G3	TEST2	I	Test Pin switching regulator (in combination with Test1, 3)	
E1	TEST3	I	Test Pin switching regulator (in combination with Test1, 2)	
	PHY supply voltages			
E12	VDD33ESD		Analog test supply, 3.3 V	
C8	VDDQ_PECL_B1	I	PECL buffer power supply 3.3 V (Port 1)	
M8	VDDQ_PECL_B2	I	PECL buffer power supply 3.3 V (Port 2)	
D14	P1VDDARXTX	I	Analog Rx/Tx port power supply Analog 1.5 V V_{DD} (must be generated via a filter from digital 1.5 V power supply) – Port 1	
L14	P2VDDARXTX	I	Analog Rx/Tx port power supply Analog 1.5 V V_{DD} (must be generated via a filter from digital 1,5 V power supply) – Port 2	
H14	VDDACB	I	Analog 3.3 V V_{DD} (must be generated via a filter from digital 3.3 V power supply)	
G13	VSSAPLLCB		Analog central GND	
G14	VDDAPLL		Analog central power supply for PHYs, 1.5 V	
	Pins for core PLL power supply			
L9	PLL_AGND		PLL analog GND (core PLL)	
L10	PLL_AVDD		PLL analog 1.0 V (core PLL)	
	Pins for switching regulator			
J1	BVDD	I	Supply voltage for the switching regulator (3.3 V supply for the switching transistor)	

G1	BGND		GND for switching regulator (please place bypass capacitor between analog power supply and GND).	
F2	AVDD_REG		Analog VDD for regulator (3.3 V supply), smoothed voltage to feed the internal POR.	Note 1)
G2	AGND_REG		Analog GND switching regulator	
H1	LX	O	1.5 V output of the internal switching regulator	
F1	FB	I	Feedback (regulator)	
	Configurable GPIOs			
	GPIO_00 - GPIO_47	I/O	(see table "Alternate use of the GPIO") After reset the GPIO pin are configured as **Inputs** (no pull up or down)	Note 2)

Notes:

1. Pin F2 must be always connected to VDD33 (refer Figure 8-2: Internal voltage regulator).
2. Unused GPIO pins should be connect with a pull up (10 kΩ) to VCC33. This resistor should not be greater than 10 kΩ.
3. The signal TEST_SYNC must be available for certification test (an accessible pad is sufficient).

2.2. GPIO multiplexing

Table 2-2: Alternate use of the GPIOs

Pin	Designation	Alternate Use	Description
D5	GPIO_0	LBU_WR_EN_IN	Write Enable
B5	GPIO_1	LBU_READ_EN_IN	Read Enable
C5	GPIO_2	LBU_CS_IN	Chip Select
C4	GPIO_3	LBU_BE_1_IN	Byte Selection (low)
A4	GPIO_4	LBU_BE_2_IN	Byte Selection (high)
B4	GPIO_5	LBU_READY_OUT	Ready Signal TPS-1 (Note 1), (Note 2)
C3	GPIO_6	LBU_DATA0	Data Bit
A3	GPIO_7	LBU_DATA1	Data Bit
B3	GPIO_8	LBU_DATA2	Data Bit
B2	GPIO_9	LBU_DATA3	Data Bit
D3	GPIO_10	LBU_DATA4	Data Bit
D4	GPIO_11	LBU_DATA5	Data Bit
C1	GPIO_12	LBU_DATA6	Data Bit
C2	GPIO_13	LBU_DATA7	Data Bit
D2	GPIO_14	LBU_DATA8	Data Bit
D1	GPIO_15	LBU_DATA9	Data Bit
E2	GPIO_16	LBU_DATA10	Data Bit
E3	GPIO_17	LBU_DATA11	Data Bit
E4	GPIO_18	LBU_DATA12	Data Bit
E5	GPIO_19	LBU_DATA13	Data Bit
F5	GPIO_20	LBU_DATA14	Data Bit
F4	GPIO_21	LBU_DATA15	Data Bit
F3	GPIO_22	LBU_A0_IN	Address Bit
G5	GPIO_23	LBU_A1_IN	Address Bit
G4	GPIO_24	LBU_A2_IN	Address Bit
H5	GPIO_25	LBU_A3_IN	Address Bit
H4	GPIO_26	LBU_A4_IN	Address Bit
J4	GPIO_27	LBU_A5_IN	Address Bit
J3	GPIO_28	LBU_A6_IN	Address Bit
K3	GPIO_29	LBU_A7_IN	Address Bit
K4	GPIO_30	LBU_A8_IN	Address Bit
K2	GPIO_31	LBU_A9_IN	Address Bit
L2	GPIO_32	LBU_A10_IN	Address Bit
L3	GPIO_33	LBU_A11_IN	Address Bit
L1	GPIO_34	LBU_A12_IN	Address Bit
M2	GPIO_35	LBU_A13_IN	Address Bit
M1	GPIO_36	LBU_SEG0_IN	Segment choice 1
M3	GPIO_37	LBU_SEG1_IN	Segment choice 2
P3	GPIO_38	HOST_RESET_IN	Reset Host SPI Interface
N3	GPIO_39	HOST_SFRN_IN	Start new SPI Transfer
N2	GPIO_40	HOST_SRXD_IN	SPI receive data
N4	GPIO_41	HOST_SCLK_IN	SPI Clock
M4	GPIO_42	HOST_STXD_OUT	SPI transmit data
P4	GPIO_43	HOST_SHDR_OUT	Header recognized
N5	GPIO_44	LOCAL_SCLK_OUT	SPI Clock (SPI master IO interface)
M5	GPIO_45	LOCAL_SFRN_OUT	SPI Chip Select (SPI master IO interface)
M6	GPIO_46	LOCAL_SRXD_IN	SPI receive date (SPI master IO interface)
M7	GPIO_47	LOCAL_STXD_OUT	SPI transmit data (SPI master IO interface)

Note: You can only use one interface exclusively. It is not allowed to use e.g. the parallel and serial host interface at the same time.

Note 1): The "LBU_READY_OUT" is designed to connect only to one microcontroller. If you want to connect additional devices you must add circuitry to realize the high-impedance state.

Note 2): If your processor does not have a READY Input, you can choose a wait time of 80 ns (8 CPU cycle) during each transfer cycle.

2.3. Supply Voltage Circuitry

The TPS-1 works with three operating voltages: VDD15 (1.5 V), VDD33 (3.3 V, IO) and VDD10 (1.0 V, core). Additionally the on-chip PLL for the device clock generation requires a supply called PLL_AVDD (1.0 V), which is typically a filtered version of VDD10. The integrated PHYs of the TPS-1 require additional filtered operating voltages.

Table 2-3: Supply Voltage Circuitry

Pin	Pin Name	Function	Supply Voltage Generation
D14, L14	P1VDDARXTX P2VDDARXTX	Analog port RX/TX power supply, 1.5 V (PHY port 1 and port 2)	Must be generated from VDD15 via a filter.
G14	VDDAPLL	Analog central power supply, 1.5 V (PHY)	
H14	VDDACB	Analog central power supply, 3.3 V (PHY)	Must be generated from VDD33 via a filter.
E12	VDD33ESD	Analog test power supply, 3.3 V (PHY)	
G13	VSSAPLLCB	Analog central GND (PHY)	Must be generated from GND Core/IO via a filter or connected to GND Core/IO at the far end from TPS-1.
C8, M8	VDDQ_PECL_B1 VDDQ_PECL_B2	PECL buffer power supply 3.3 V (port 1 and port 2)	
L9	PLL_AGND	Analog Ground for the internal CPU clock generation	
L10	PLL_AVDD	Power supply for the internal CPU clock generation (1.0V)	
A1, A14, B7, F7, F8, F9, G6, G7, G8, G9, G10, G12, H6, H7, H8, H9, H10, J2, J6, J7, J8, J9, J12, M10, N7, N10, P1, P14	GND	Digital GND	
D12, D13, L12, L13	AGND	Analog Ground for PHYs	
B1, B14, C7, F6, F10, H2, N1,N14, P7, P10	VDD33	Voltage Supply 3.3 V	External
A2, A7, A13, F12, K1, K12, M9, P2, P13	VDD15	Voltage Supply 1.5 V	form Switching Regulator or external
E6, E7, E8, E9, K6, K7, K8, K9	VDD10	Voltage Supply 1.0 V	External

3. Host Interface

The host interface is designed to connect external microprocessors. These processors access the internal shared memory of the TPS-1 in order to exchange cyclic or acyclic data with the PROFINET IO interface. The shared memory has an address space of 64 Kbyte. The data exchange is processed with the help of an **"Event Unit"**.
Another way to inform the external host CPU about a new PROFINET status is the integrated interrupt system. The parallel interface can be switched to Motorola or Intel mode.
It is only possible to use the Host parallel interface or the Host serial interface. It is not possible to use both at the same time.

3.1. Testing DPRAM Interface

For testing the DPRAM Interface it is useful to have addresses with defined values. After start of the TPS-1 firmware the TPS-1 writes the magic number and the NRT Area Size into the addresses 0x8000 and 0x8004.

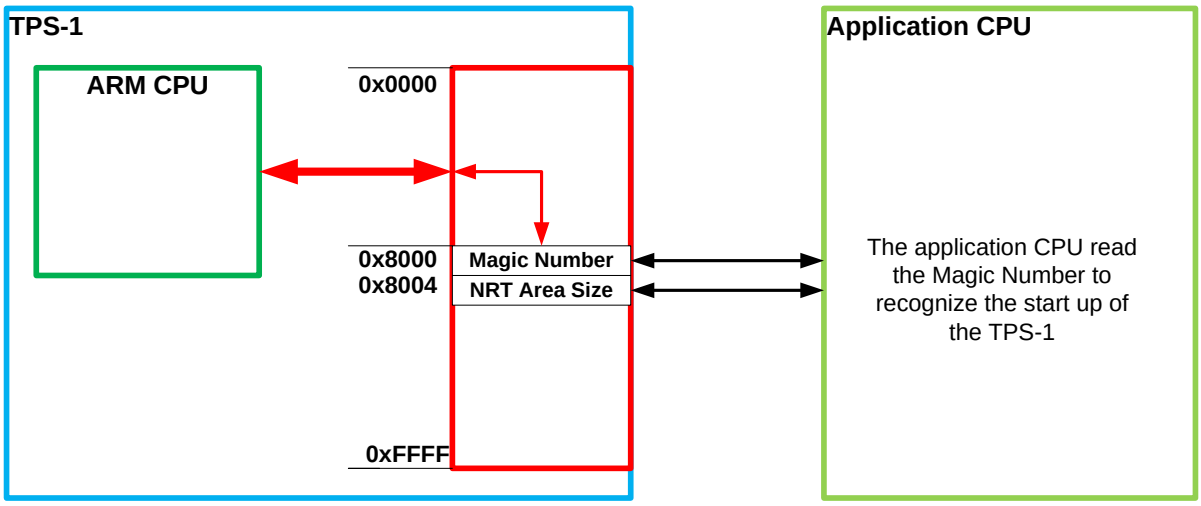

Figure 3-1: TPS-1 with address page 16 Kbyte

3.2. Parallel Interface

3.2.1. Operating modes of the parallel interface

The parallel interface can be used with an 8-bit or 16-bit data bus.

Table 3-1: Operating Modes of the parallel interface

Setting	Description
Operating mode	Separate Read / Write signal (Intel Mode)
	Read-/Write-Control (Motorola Mode)
Polarity of ready signal	Ready Signal "active low"
	Ready Signal "active high"
Data bus width	8 bit
	16 bit

The configuration of the parallel interface is also done with "TPS Configurator".

3.2.2. Signal description of the parallel interface

The shared memory has an address space of 64 Kbyte (refer to chapter **"Shared memory structure"**). The typical page size is 16 KByte. For a correct alignment you have to connect the highest address bits to the signals **LBU_SEG0_IN** and **LBU_SEG1_IN** (see Table 3-2**,** Figure 3-1 and Figure 3-2**)**.

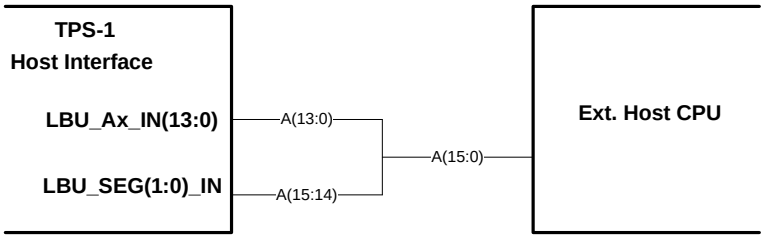

Figure 3-2: TPS-1 with address page 16 Kbyte

You can also choose a page size of 4 Kbyte. When you choose 4 Kbyte pages you have less space inside the NRT area for configuration slots and subslots.

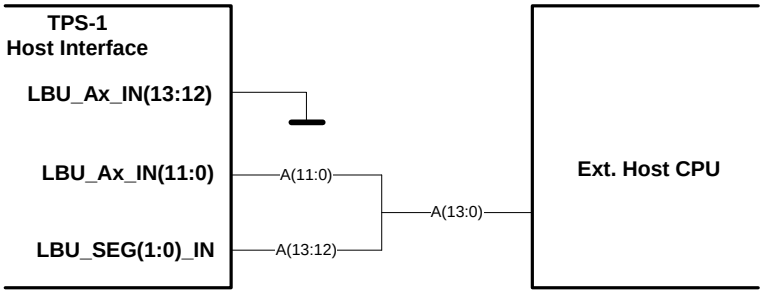

Figure 3-3: TPS-1 with address page 4 Kbyte

Table 3-2 describes all signals of the parallel Host interface.

Table 3-2: Parallel Host Interface Layout

Signal designation	Function	Remarks
LBU_WR_EN_IN	Write Control	active low (Intel mode)
		0: write; 1: read (Motorola mode)
LBU_READ_EN_IN	Read Control	active low (Intel-mode)
		no function (Motorola-Mode)
LBU_CS_IN	Chip Select	
LBU_BE_1_IN	Byte Selection 1	
LBU_BE_2_IN	Byte Selection 2	
LBU_READY_OUT	Ready Signal	polarity changeable
LBU_DATA0 – LBU_DATA15	data line 0 – 15	
LBU_A0_IN – LBU_A13_IN	Address lines 0 - 13	
LBU_SEG0_IN	Low Bit of the segment	page selection
LBU_SEG1_IN	High Bit of the segment	page selection

During a memory access, the TPS-1 behaves like a „16-bit Little Endian" device with an 8-bit or 16-bit memory. The possible access types are listed in Table 3-3.

Table 3-3: 16-Bit external Host Databus

LBU_BE_2_IN	LBU_BE_1_IN	Access type
1	0	8-Bit LOW
0	1	8-Bit HIGH
0	0	16-Bit
Other combinations		Not allowed

Table 3-4: 8-Bit external Host Databus

LBU_A[1:0]	LBU_BE_2_IN	LBU_BE_1_IN	Access type
00	1	0	8-Bit access
01	1	0	8-Bit access
10	1	0	8-Bit access
11	1	0	8-Bit access
Other combinations			Not allowed

An illegal access results in an „Error-IRQ" from the event unit.

3.2.3. Memory Segmentation at 4 kByte and 16 kByte page size

You decide the page size with the TPS Configurator. A connected Host CPU selected the pages with the LBU_SEGx_IN signals. Table 3-5 shows the page decoding.

Table 3-5: Page selection with LBU_SEGx_IN signals

LBU_SEG(1:0)	Selected Page
0 0	Page 00
0 1	Page 01
1 0	Page 02
1 1	Page 03

The segmentation with 16 Kbyte pages is shown in Figure 3-3. With 16 address lines you can reach the whole 64 kByte address space.

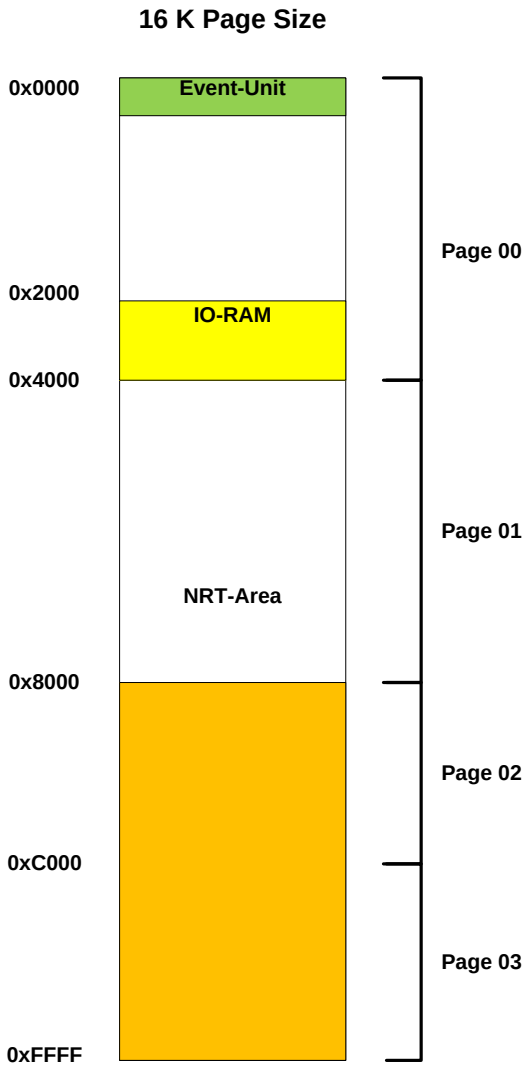

Figure 3-4: 16 kByte page size

Using the 4 kByte address pages limits the available address space of the NRT area. Figure 3-4 shows the pages. You can reach the complete Event-Unit and the complete IO-RAM. Out of the NRT area you can only use the address space between 0x8000 and 0x9FFF.

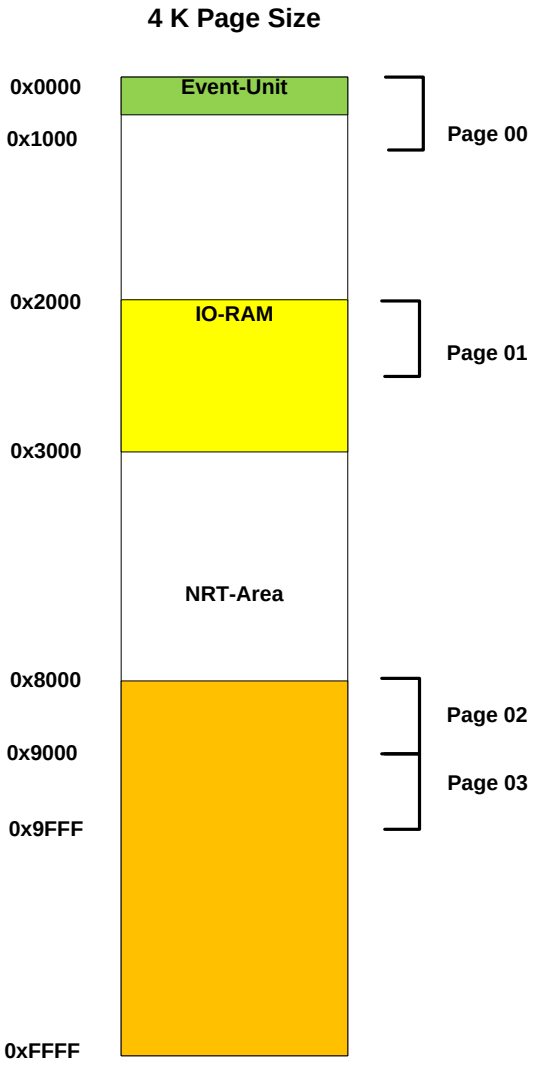

Figure 3-5: 4 kByte page size

Because of the page size, it is not possible to use the max. possible number of slots and subslots. Other page sizes than 16 kByte and 4 kByte are not possible.

3.2.4. Connection example for a 8bit data bus

Figure 3-5 shows a connection example of an 8-bit data bus to the TPS-1.

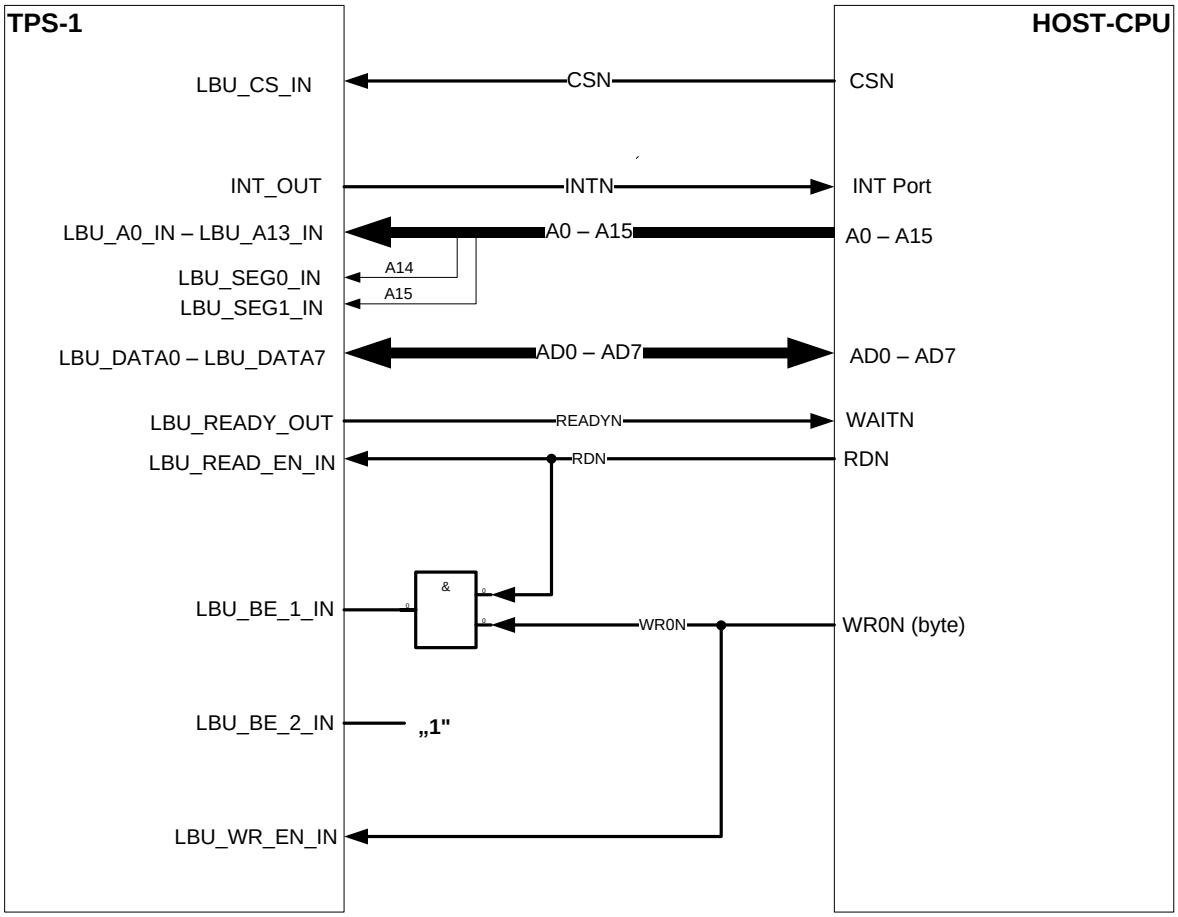

Figure 3-6: Connection example for an 8-bit data bus

3.2.5. Connection example for a 16-bit data bus

Figure 3 3-6 shows the connection of a 16-bit CPU to the TPS-1. The connection uses a 16-bit data bus and an address bus of 16 bit. Thus it is possible to access the entire address space of 64 KByte. Address line A0 should not be connected using the 16-bit data bus. The Address line LBU_A0_IN should be connected to a pull down.

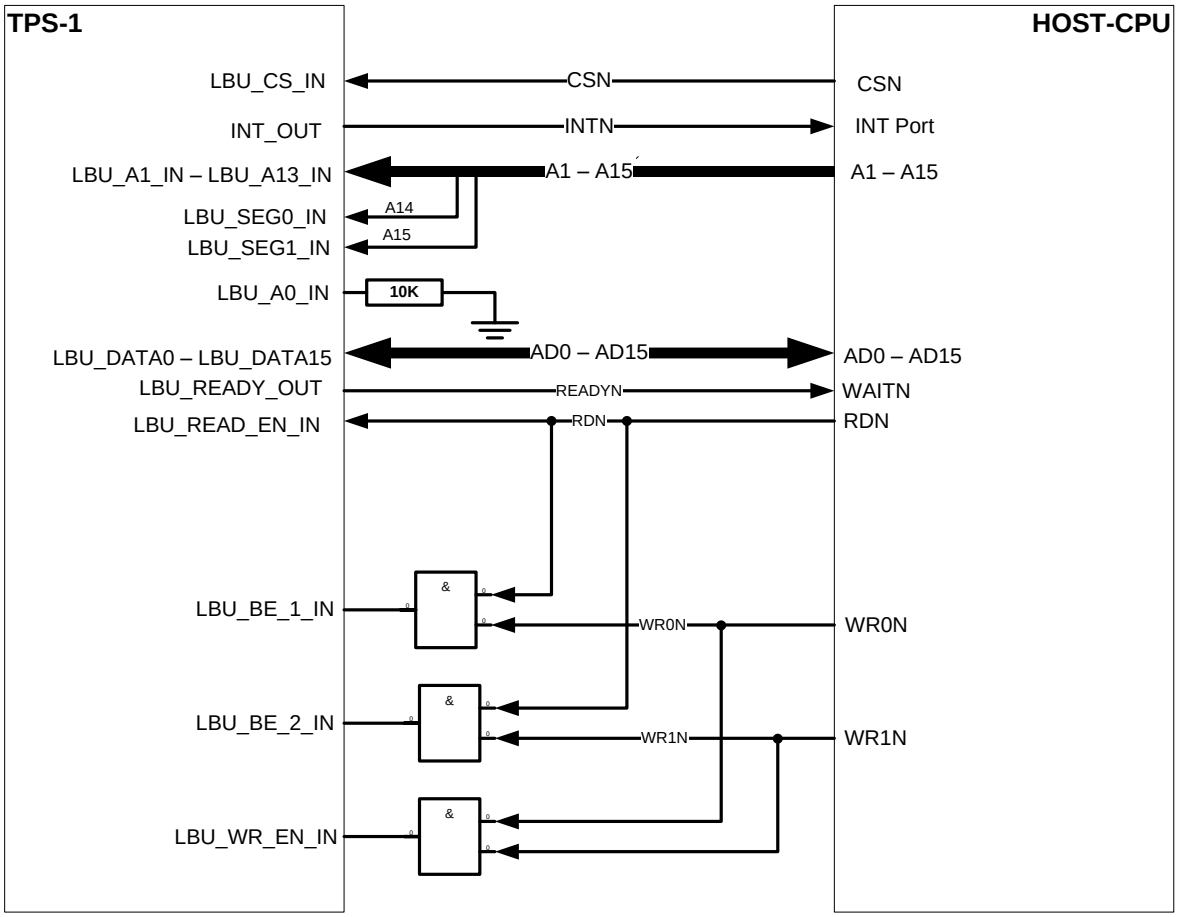

Figure 3-7: Connection of a V850 CPU with a 16-bit data bus

3.3. SPI Slave Interface

Another way to connect a host CPU is the SPI interface. The maximum speed for serial access to the shared memory is 25 MHz. The transmission clock frequency should range between 1 MHz and 25 MHz. A control unit for processing the SPI Master commands is implemented into the TPS-1.
The SPI Master commands are described in this chapter.

Table 3-6: SPI host interface signals

Pin	GPIO Pin	Signal designation	Function	Remarks
P3	GPIO_38	HOST_RESET_IN	Serial Reset	The SPI Slave interface can be reset by using this signal (signal is active high).
N3	GPIO_39	HOST_SFRN_IN	Serial Frame	The start of a new SPI transfer is signalized.
N2	GPIO_40	HOST_SRXD_IN	Serial Data Input	MOSI (Master out Slave in)
N4	GPIO_41	HOST_SCLK_IN	Serial Clock Input	Serial Clock driven by the SPI Master
M4	GPIO_42	HOST_STXD_OUT	Serial Data Output	MISO (Master in Slave out)
P4	GPIO_43	HOST_SHDR_OUT	Serial Header Information	header information available

An unknown or wrong SPI access causes an „Error-IRQ" that is reported to the host CPU by the event unit.
The clock phase and the CPOL (clock polarity) is adjustable (active low, active high).
The following figure shows the connection of a host CPU (V850ES/JG2) to the SPI Slave interface of the TPS-1. The **"chip select"** line is not connected. The data transfer is controlled by the status of the **"clock line"** (CSI-Master).
The pins HOST_RESET_IN, HOST_SFRN_IN and HOST_SHDR_OUT are not supported directly by the HOST-CPU. They have to be simulated by the pins P02, P03 and P04.

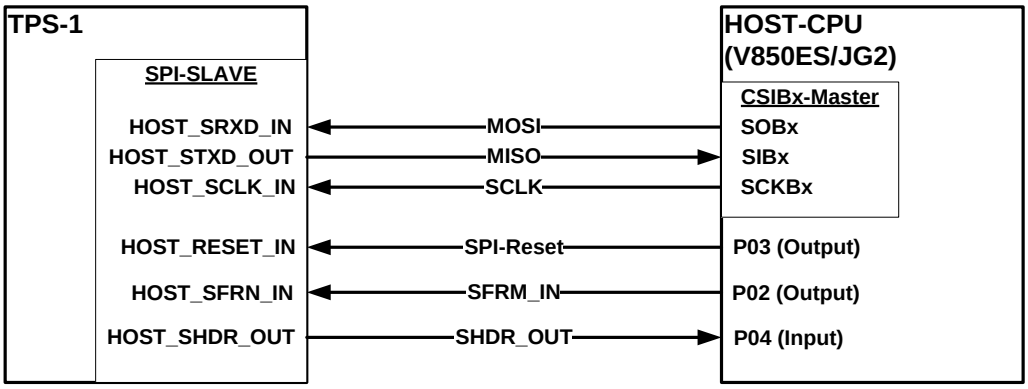

Figure 3-8: Connection of a V850 CPU to the SPI interface

3.3.1. Serial access to the shared memory

The access to the shared memory is processed with command bytes that are part of the SPI-Header. The command structure depends on the device.

Generally an SPI interface works like a shift register. The clock is driven by the SPI master. After processing the SPI command, the SPI slave sends the requested data to the host CPU (or data is only sent to the SPI slave). As long as the chip select signal is active, data are exchanged between the devices (master – slave).

3.3.1.1. Header structure

The content and meaning of SPI data is defined by the implementation of the SPI slave. The following chapter describes the structure of the SPI slave commands.

Table 3-7: SPI header structure

Header					Data
Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5 – max.
Command	Address	Address	Length	Length	
1 Byte	1 Byte	1 Byte	1 Byte	1 Byte	1 Byte .. max. length Shared Memory

An indirect command contains the length information in byte 3 and 4. A direct command contains the length information in the bits 0 to 3 of the command byte. The maximum address access is limited to 15 byte.

3.3.1.2. Structure of a command byte

Figure 3-8 shows the format of a command byte. A command byte can be followed by an address area, length area and data.

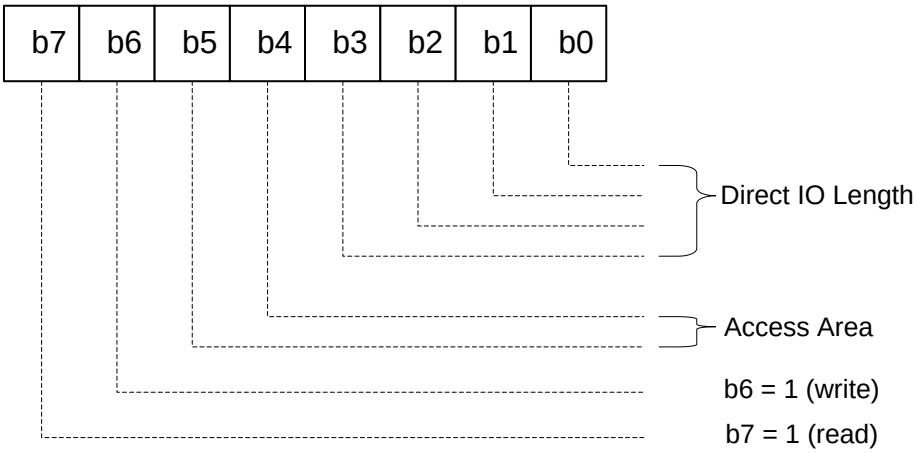

Figure 3-9: Command byte for SPI slaves (host interface)

The bits of the command byte have the following meaning:

- b7 indicates a read command,
- b6 indicates a write command,
- b5 and b4 describe the addressing range:
  „00": MEM access to the complete shared memory (64 Kbyte)
  „01": IO access to the input/output area
  „10": access to a multicast provider CR (only write)
  „11": fractional access to an I-CR (b6 = 1) or MC-CR (b6 = 0)
- b3 .. b0 contain the length for an optimized direct data access
  „= 0000": no direct access.
  „≠ 0000": direct access length information (maximum of 15 byte)

3.3.1.3. Command overview

The SPI commands are optimized for the use with PROFINET. The following table describes the implemented commands.

Table 3-8: Implemented SPI commands

DirectMEM-Access	**This gives the external host CPU access to the complete address space of 64 Kbyte. Each access transfers not more than 15 byte. The length is coded in the command byte.**				
Command	**Description**	**Command code**	**Number of address bytes**	**Number of length bytes**	**Number of data bytes**
Read MEM Direct	Reads from the transferred address. The length is coded in the command byte.	0b1000_nnnn (0x8n)	2	0	1 - 15
Write MEM Direct	Writes to the transferred address. The length is coded in the command byte.	0b0100_nnnn (0x4n)	2	0	1 - 15
MEM-Access	**With this command, the external host CPU can read from and write to the complete 64 Kbyte address space with a maximum data length of 64 Kbyte (access to cyclic and acyclic data).**				
Command	**Description**	**Command code**	**Number of address bytes**	**Number of length bytes**	**Number of data bytes**
Read MEM	Reads from the transferred address. The length is coded in the length byte.	0b1000_0000 (0x80)	2	2	1 – 32K (64K)
Write MEM	Writes to the transferred address. The length is coded in the length byte.	0b0100_0000 (0x40)	2	2	1 – 32K (64K)

3.3.2. SPI Slave Interface Timing

The SPI transfer is controlled by the signal HOST_SFRN_IN. A chip select signal is not used.

3.3.2.1. SPI Slave Interface Typical Timing

The following figure shows a typical SPI-Slave Timing (Motorola Mode).

Each transfer (a transmission of 8 bit) starts with a falling edge of the **HOST_SFRN_IN** signal. The transmission is controlled by the clock signal. All receive and transmit data is processed in the Little Endian format by the serial host interface. When connecting a Big Endian Host System, the format has to be changed into the correct order.

There is a maximum clock frequency of 25 MHz possible using this interface.

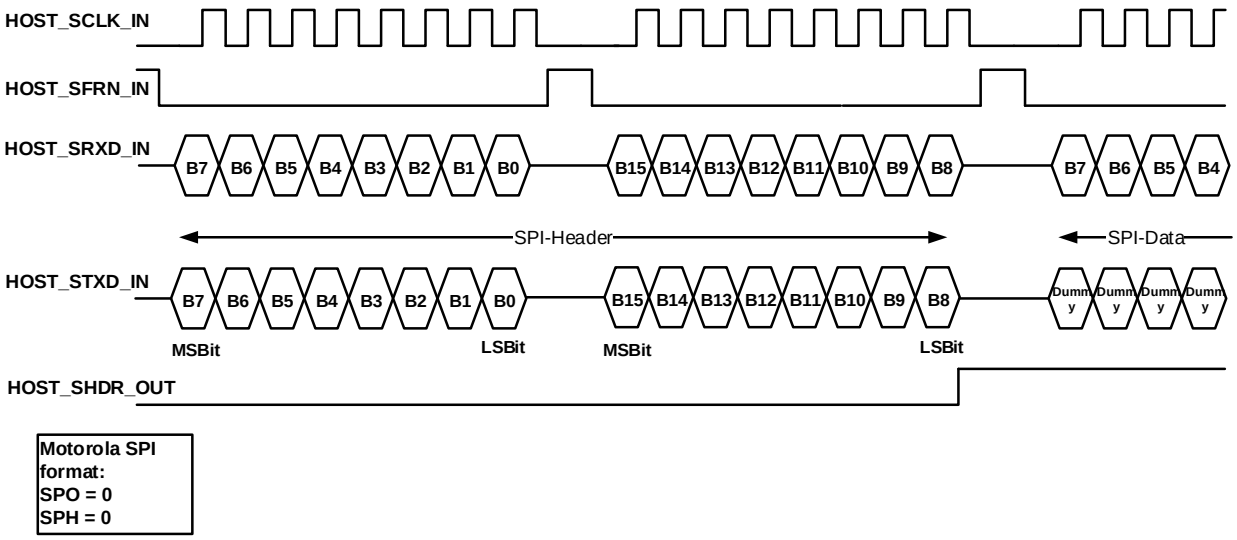

Figure 3-10: SPI Slave Timing

The signal **HOST_SHDR_OUT** is used to inform the SPI master, that header information has been received (**HOST_SHDR_OUT = 0**). When the signal goes to high level (**HOST_SHDR_OUT = 1**), payload data is expected.

3.3.2.2. SPI Slave Interface Handshake Mode

If the header contains a read or exchange command, it is necessary to wait for a short time after transferring the header in order to enable the slave interface to collect the data before transferring. There are two methods to do this.
You can enable the busy mode (polarity high or low) or use the wait mode.

3.3.2.2.1. SPI Slave Interface Handshake Busy Mode

The handshake mode and the polarity can be configured with the TPS Configurator.
After transmitting the header information, the Busy_Enable signal is set (no clock and HOST_SRXD_IN in high or low – depends on the Busy_POL). When the SPI slave interface can transmit the requested data the **HOST_STRX_OUT** signal is set to its active level. This indicates to the SPI master that it can start the next cycle and the master release the Busy_Enable signal. This forces the SPI slave to release the Busy level and the master starts the next clock cycle.

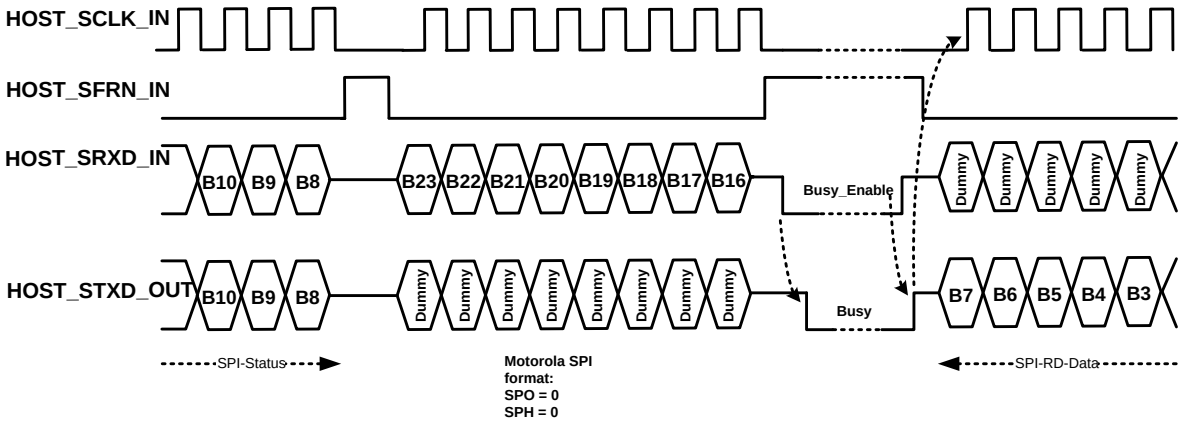

Figure 3-11: SPI Read-Timing (Busy_POL=0)

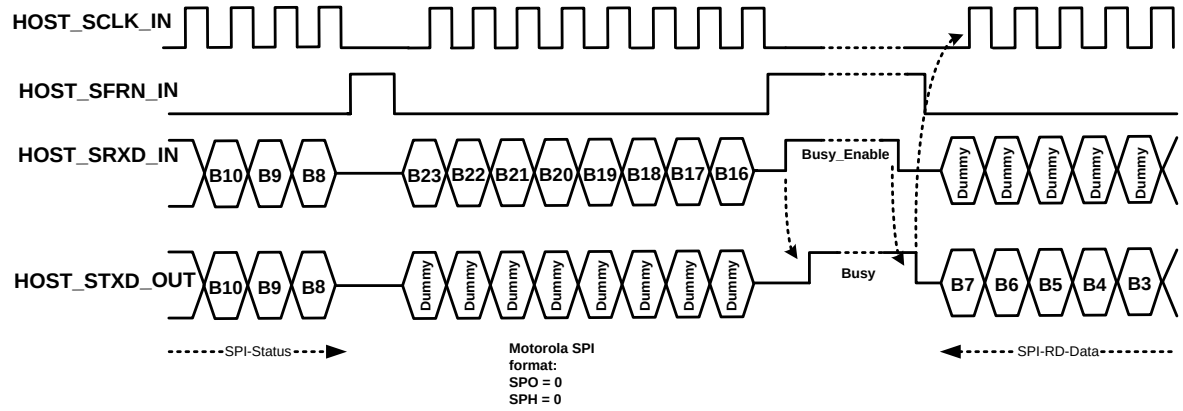

Figure 3-12: SPI Read-Timing (Busy_POL=1)

3.3.2.2.2. SPI Slave Interface Handshake Wait Mode

When using the Handshake Wait Mode, the SPI master deactivates the data transfer after the header has been transmitted and starts a wait time. During this time, the SPI Slave can provide the requested data.

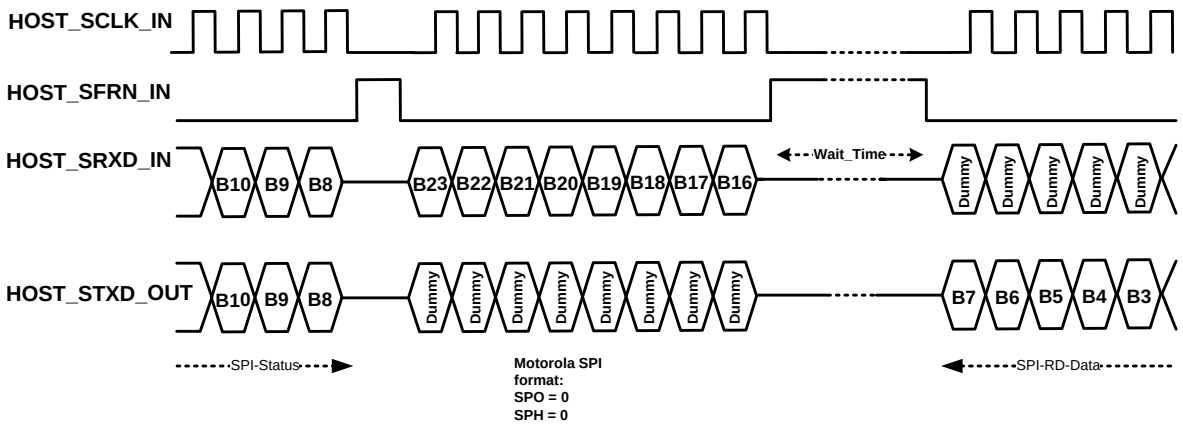

Figure 3-13: SPI Read-Timing Wait Mode

The following equation describes the Wait-Time after the command bytes, before starting the payload data:

$T_{Wait} = ((32 * f_{sys}/f_{SPI}) - 10)$; ($T_{Wait} * 1/f_{sys}$ = Wait-Time)

The time between two complete data transfers is calculated with the following equation:

$L = ((4 * (T_{Wait} + 10)) - 8 * f_{sys}/f_{SPI}))$; ($L * 1/f_{sys}$ = break between two cycles);

The following table shows a rough estimation for two frequencies:

Table 3-9: SPI Wait Time

SPI Clock (MHz)	Wait-Time (µs)
12.5	2.46 – 2.5
25	1.18 – 1.2

3.3.3. SPI Slave Interface Reset Timing

Figure 3-14 describes the behavior when a reset for the SPI Slave interface occurs. The communication process is interrupted and after a wait time of 4 system clocks (40 ns for the TPS-1), the next transfer can start.

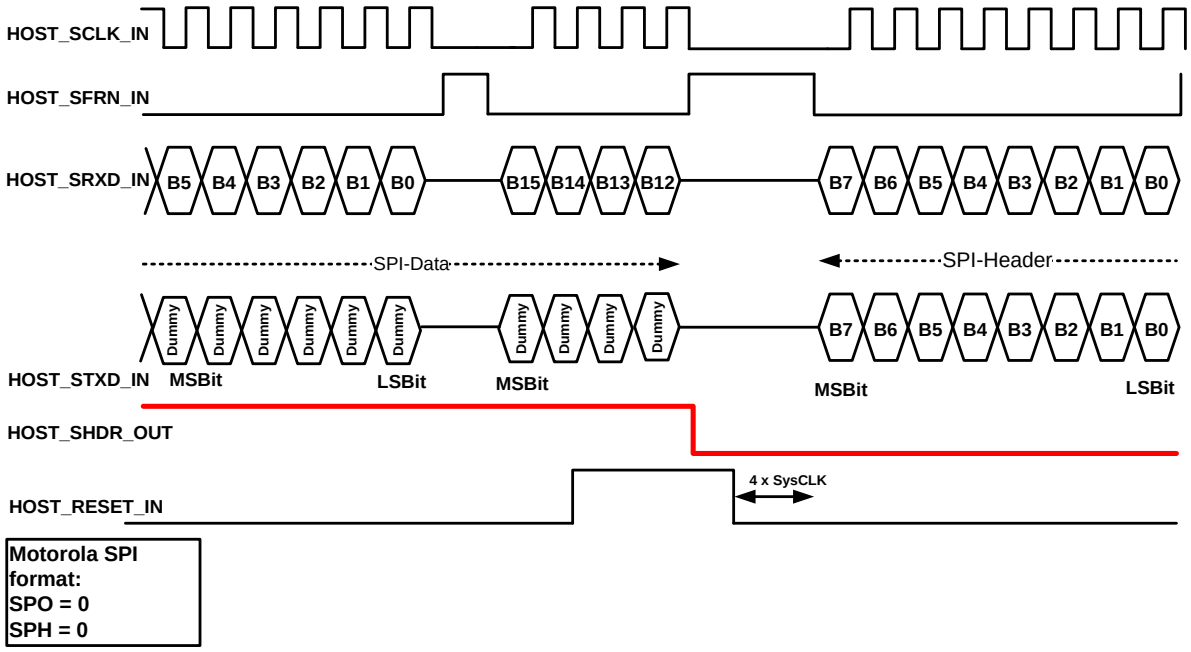

Figure 3-14: SPI Slave Reset Timing

The signal HOST_RESET_IN is the only way to set the slave interface to a defined status. The signal is active high. During the normal operation the signal is set to "low level".

4. Shared memory structure

Figure 4-1 describes the structure of the shared memory. The serial and parallel interfaces see the same memory image (64 Kbyte). If you use 4 kByte memory pages then you can only use the NRT Area up to 0x9FFF.

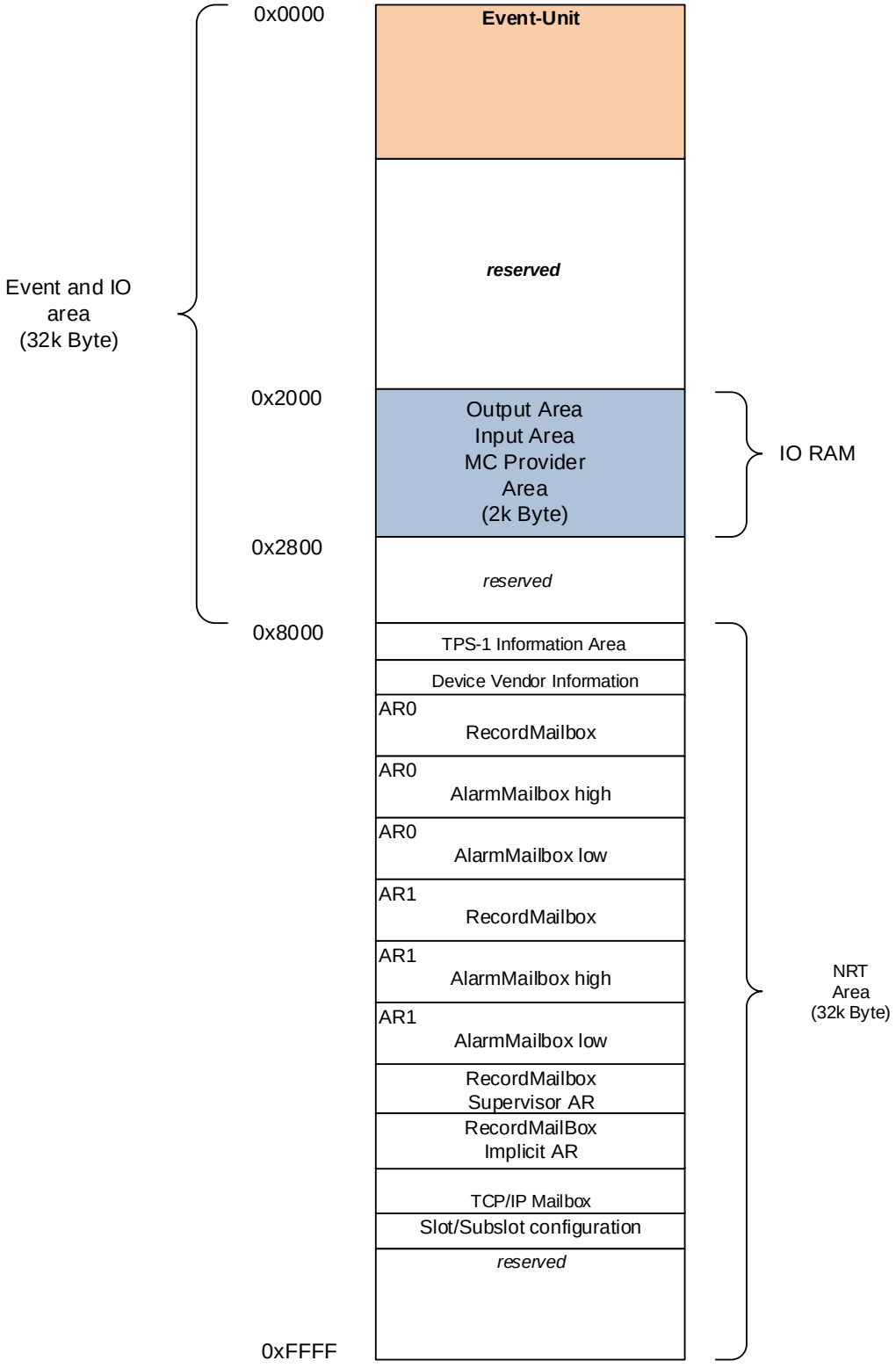

Figure 4-1: TPS-1 Shared Memory Structure (Dual Ported RAM)

The structure of the configuration written into the NRT area is checked by the TPS-1 firmware. If there are structure errors the TPS-1 firmware does not start.
The host interface and the NRT area are accessible in a continuous address space.

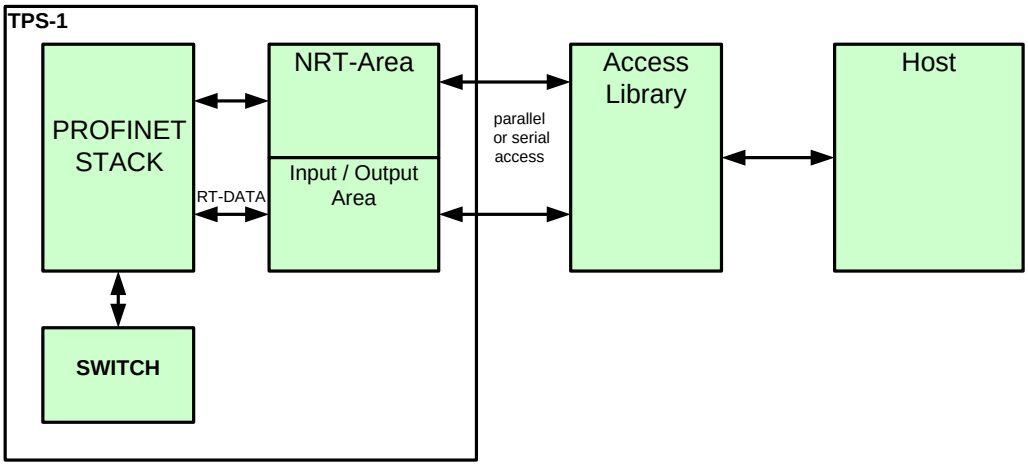

Figure 4-2: General overview host interface

Access to the NRT area and Input/Output area is processed with the support of a software library. The memory area (shared memory) is used for the access to acyclic and cyclic data. The size depends on the device.
Exchange of the cyclic data is managed in the peripheral interface (input / output area). The structure of this area is fixed. It is possible to manage one AR (Application Relations) in the first release.

- one I-Data-CR
- one O-Data CR

The IO data has a maximum size of 340 Byte (cyclic data).

4.1. Event communication with the TPS-1 Firmware

After system start up the communication between the TPS-1 and the host CPU is processed by the event register (one register for each direction). Each bit of the event register causes a special action.

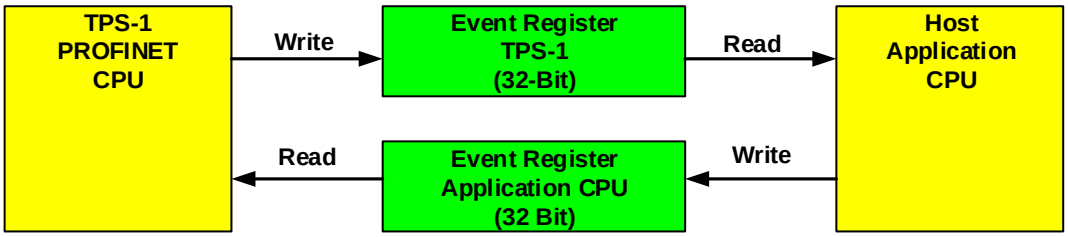

Figure 4-3: TPS-1 Event Communication

For process changes of the event register the TPS-1 and the host CPU has to poll these registers. You can also use an interrupt control mode if the host CPU supports this.

The event bits corresponding to the mail box access are not ambiguous. After receiving this event it is necessary to check each mail box. In the header of the respective mail box, the **READ_FLAG** is set.

The following tables describe the structure of the event register for each direction.

For each possible event bit in the event register a special callback function is implemented. For example the event "EVENT_ONCONNECT_REQ_REC_0" (bit 13) indicates a Connect.Req for the first AR (AR0). In this case the check function will call in the function OnConnect() and process the event.

4.2. Events from the TPS-1 firmware to the host

Table 4-1: TPS-1 Firmware Events

Name	Description
TPS_Event_Bits (Firmware Stack -> Host)	
TPS_EVENT_ONCONNECTDONE_AR0	Set when a connection for IOAR0 is established.
TPS_EVENT_ONCONNECTDONE_AR1	Set when a connection for IOAR1 is established.
TPS_EVENT_ONCONNECTDONE_AR2	Set when a connection for IOSAR is established.
TPS_EVENT_ON_PRM_END_DONE_IOAR0	All parameter available for IOAR0.
TPS_EVENT_ON_PRM_END_DONE_IOAR1	All parameter available for IOAR1.
TPS_EVENT_ON_PRM_END_DONE_IOSAR	All parameter available for IOSAR
TPS_EVENT_ONABORT_IOAR0	Connection for IOAR0 is disconnected.
TPS_EVENT_ONABORT_IOAR1	Connection for IOAR1 is disconnected.
TPS_EVENT_ONABORT_IOSAR	Connection for IOSAR is disconnected.
TPS_EVENT_ONREADRECORD	Set when a Record Read Request is available in a Record-Mailbox.
TPS_EVENT_ONWRITERECORD	Set when a Record Write Request is available in a Record-Mailbox.
TPS_EVENT_ONALARM_ACK_0	Set when an alarm (low priority) is acknowledged from the controller.
TPS_EVENT_ONDIAG_ACK	Set if a diagnostic alarm is acknowledged.
TPS_EVENT_ONCONNECT_REQ_REC_0	Set if a Connect.Req for the first AR (AR0) is received.
TPS_EVENT_ONCONNECT_REQ_REC_1	Set if a Connect.Req for the first AR (AR1) is received.
TPS_EVENT_ONCONNECT_REQ_REC_2	Set if a Connect.Req for the third AR (AR2) is received.
TPS_EVENT_ON_SET_DEVNAME	Device name is send to the host application.
TPS_EVENT_ON_SET_IP_PERM	IP address should be set permanent.
TPS_EVENT_ON_SET_IP_TEMP	IP address should only be set temporary.
TPS_EVENT_ONDCP_BLINK_START	Action LED flashing is should start.
TPS_EVENT_ONDCP_FACTORY_RESET	All settings are set to the factory settings.
TPS_EVENT_ONALARM_ACK_1	Set when an alarm (high priority) is acknowledged from the controller.
TPS_EVENT_RESET	A RESET of the Host CPU is forced.
TPS_EVENT_ETH_FRAME_REC	A TCP/IP Ethernet Frame is received.

4.3. Events from the host to the TPS-1 firmware

Table 4-2: Host Events

Name	Description
Host Event Bits (Host -> Firmware Stack)	
APP_EVENT_CONFIG_FINISHED	Set by TPS_StartDevice(). Configuration is valid.
APP_EVENT_APP_RDY_0	Set when the device is complete parameterized for AR0.
APP_EVENT_APP_RDY_1	Set when the device is complete parameterized for AR1.
APP_EVENT_APP_RDY_2	Set when the device is complete parameterized for AR2 (Supervisor AR).
APP_EVENT_RECORD_DONE	Set after processing a request of the Record Mailbox.
APP_EVENT_DIAG_CHANGED	Set when the status of the diagnostic mailbox changed.
APP_EVENT_ONCONNECT_OK_0	Connect AR0 ok. Is set after the host processes the Framelayout-Parameter out of a Connect Request of the AR0.
APP_EVENT_ONCONNECT_OK_1	Connect AR1 ok. Is set after the host processes the Framelayout-Parameter out of a Connect Request of the AR1.
APP_EVENT_ONCONNECT_OK_2	Connect AR2 ok. Is set after the host processes the Framelayout-Parameter out of a Connect Request of the AR2.
APP_EVENT_ABORT_AR_0	AR0 is disconnected by the host.
APP_EVENT_ABORT_AR_1	AR1 is disconnected by the host.
APP_EVENT_ABORT_AR_2	AR2 is disconnected by the host.
APP_EVENT_PULL_SUBMODULE	A submodule is pulled out of the device.
APP_EVENT_RETURN_SUBMODULE	A submodule returns in to the device.
APP_EVENT_ALARM_SEND_REQ_AR0	Set when an alarm for the AR0 is reported.
APP_EVENT_ALARM_SEND_REQ_AR1	Set when an alarm for the AR1 is reported.
APP_EVENT_ALARM_SEND_REQ_AR2	Set when an alarm for the AR2 is reported.
APP_EVENT_RESET_STACK_CONFIG	
APP_EVENT_ETH_FRAME_SEND	A TCP/IP Ethernet frame (MAC) should be send from the mailbox.
APP_EVENT_WRITE_INPUT_DATA	Process data written.
APP_EVENT_READ_OUTPUT_DATA	Process data read.
APP_EVENT_RESET_PN_STACK	Host CPU forces a software reset of the TPS-1

4.4. Interrupt Communication with the TPS-1

The communication between the TPS-1 and the Host CPU is processed by the Event-Unit. If you want to use the interrupt control, you need the registers shown in Table 4-3.

Table 4-3: Event Register List

Register Name:	Read / Write	Offset Address
Host_IRQ_low	R/-	0x0008
Host_IRQ_high	R/-	0x000C
Host_IRQmask_low	R/W	0x0010
Host_IRQmask_high	R/W	0x0014
Host_IRQack_low	-/W	0x0020
Host_IRQack_high	-/W	0x0024
Host_EOI	R/W	0x0028
PN_Event_low	R/W	0x003C
PN_Event_high	R/W	0x0040

4.4.1. How to generate an interrupt by an event

The following steps are necessary for generating an interrupt from an occurring event.

1. Set the mask register (low or high)
2. Acknowledge an Interrupt by deleting the event bits.
3. Write the Host_EOI register to reset the interrupt pin "INT_OUT".

It is only necessary to set the mask register during the start sequence of your device once. Each occurring event has to acknowledge by writing the **Host_IRQack_low** and **Host_IRQack_high** register.
After writing an acknowledge register the Host_EOI register must be written. The value written into this register disables the interrupt pin for the given period (period: **count * 10ns** – Wait_Time). The interrupt signal is active low.

Note: You must write the register Host_EOI during the initialization (program start) to set the signal line to its passive state (low level).

The register PN_Event_low and PN_Event_high is used to inform the external host about events. An ISR can check the event by reading these registers.

Table 4-4: Register PN_Event_low

Name	PN_Event_low		
Address	0x003C		
Access	r/ w		
Bits	Type of Event	Description	Init:
31:00	Event-Bit (HW-Events)	high active events Bit 0: Bit 1: Bit 2: Bit 3: Bit 4: Bit 5: Bit 6: Bit 7: Receive Output Data AR1 Bit 8: Receive Output Data AR0 Bit 9 – 15: reserved Bit 16 – 31: further use	0X00000000

Table 4-5: Register PN_Event_high

Name	PN_Event_high		
Address	0x0040		
Access	r/ w		
Bits	Type of Event	Description	Init:
31:00	Event-Bit (Stack Events)	high active events Bit 0: TPS_EVENT_ONCONNECTDONE_IOAR0 Bit 1: TPS_EVENT_ONCONNECTDONE_IOAR1 Bit 2: TPS_EVENT_ONCONNECTDONE_IOSAR Bit 3: TPS_EVENT_ON_PRM_END_DONE_IOAR0 Bit 4: TPS_EVENT_ON_PRM_END_DONE_IOAR1 Bit 5: TPS_EVENT_ON_PRM_END_DONE_IOSAR Bit 6: TPS_EVENT_ONABORT_IOAR0 Bit 7: TPS_EVENT_ONABORT_IOAR1 Bit 8: TPS_EVENT_ONABORT_IOSAR Bit 9: TPS_EVENT_ONREADRECORD Bit 10: TPS_EVENT_ONWRITERECORD Bit 11: TPS_EVENT_ONALARM_ACK_0 Bit 12: TPS_EVENT_ONDIAG_ACK Bit 13: TPS_EVENT_ONCONNECT_REQ_REC_0 Bit 14: TPS_EVENT_ONCONNECT_REQ_REC_1 Bit 15: TPS_EVENT_ONCONNECT_REQ_REC_2 Bit 16: TPS_EVENT_ON_SET_DEVNAME Bit 17: TPS_EVENT_ON_SET_IP_PERM Bit 18: TPS_EVENT_ON_SET_IP_TEMP Bit 19: TPS_EVENT_ONDCP_BLINK_START Bit 20: TPS_EVENT_ONDCP_FACTORY_RESET Bit 21: TPS_EVENT_ONALARM_ACK_1 Bit 22: TPS_EVENT_RESET Bit 23: TPS_EVENT_ETH_FRAME_REC Bit 24 – 31: reserved for further use	0X00000000

One or more bits written in to these registers (*_low and *_high) process an external interrupt event (INT_OUT). A new one will influence no bits set before.

Table 4-6 Register Host_IRQmask_low

Name	Host_IRQmask_low		
Address	0x0010		
Access	r/w		
Bits	Type of Event	Description	Init:
31:00	IRQ –Bits	"0": the Event is registered in PN_Event_low "1": the Event is not registered in PN_Event_low	0xFFFFFFFF

Table 4-7: Register Host_IRQmask_high

Name	Host_IRQmask_high		
Address	0x0014		
Access	r / w		
Bits	Type of Event	Description	Init:
31:00	IRQ –Bits	"0": the Event is registered in PN_Event_high "1": the Event is not registered in PN_Event_high	0xFFFFFFFF

After processing an event, the corresponding bit must be acknowledged by writing of acknowledgment register **Host_IRQack_low** and **Host_IRQack_high**.

Table 4-8: Register Host_IRQack_low

Name	Host_IRQack_low		
Address	0x0020		
Access	- / w		
Bits	Type of Event	Description	Init:
31:00	Ack –Bits	"0": the Event-Bit is not deleted in PN_Event_low "1": the Event-Bit is deleted in PN_Event_low	-

Table 4-9: Register Host_IRQack_high

Name	Host_IRQack_high		
Address	0x0024		
Access	- / w		
Bits	Type of Event	Description	Init:
31:00	Ack –Bits	"0": the Event-Bit is not deleted in PN_Event_high "1": the Event-Bit is deleted in PN_Event_high	-

You can verify the interrupt event sources by reading the Host_IRQ_low and Host_IRQ_high register. Each bit corresponds with a masked event. A bit set to "1" shows a masked bit.

Table 4-10: Register Host_IRQ_low

Name	Host_IRQ_low		
Address	0x0008		
Access	r/ -		
Bits	Type of Event	Description	Init:
31:00	IRQ –Bits	"0": PN_Event_low = "0" or Host_IRQMask_low = "1" "1": PN_Event_low = "1" and Host_IRQMask_low = "0"	0X00000000

Table 4-11: Register Host_IRQ_high

Name	Host_IRQ_high		
Address	0x000C		
Access	r/ -		
Bits	Type of Event	Description	Init:
31:00	IRQ –Bits	"0": PN_Event_low = "0" or Host_IRQMask_low = "1" "1": PN_Event_low = "1" and Host_IRQMask_low = "0"	0X00000000

The deactivation of the interrupt pin (INT_OUT) is processed by writing into the register "Host_EOI" (0x0028). A new activation of the interrupt pin depends on the written value (bits 17:00 – Wait_Time). The activated events can be identified by reading the register Host_IRQ_low and Host_IRQ_high.

Table 4-12: Register Host_EOI

Name	Host_EOI		
Address	0x0028		
Access	r/ w		
Bits	Type of Event	Description	Init:
17:00	Wait_Time	Period of deactivating of the interrupt pin (INT_OUT). (Number of entities * 10ns – max. value 2,6 ms)	0X00000
31:18	reserved		

4.5. Status LEDs of theTPS-1

The TPS-1 uses 4 GPIOs to indicate the device status. These GPIOs can be connected directly to LEDs to display the status.

Table 4-13: Status LEDs PROFINET

LED:	Color:	Pin:	State:	Description:
LED_BF_OUT	red	B13		Bus Communication:
			ON	No link status available.
			Flashing	Link status ok; no communication link to a PROFINET-Controller.
			OFF	The PROFINET -Controller has an active communication link to this PROFINET -Device.
LED_SF_OUT	red	B11		System Fail:
			ON	PROFINET diagnostic exists.
			OFF	No PROFINET diagnostic.
LED_MT_OUT	yellow	B10		Maintenance Required: Manufacturer specific – depends on the ability of the device.
LED_READY_OUT	green	C10		Device Ready:
			OFF	TPS-1 has not started correctly.
			Flashing	TPS-1 is waiting for the synchronization of the Host CPU (firmware start is complete).
			ON	TPS-1 has started correctly.

The status signals **LED_BF_OUT**, **LED_SF_OUT**, **LED_READY_OUT** and **LED_MT_OUT** are driven "active low".

5. TPS-1 boot subsystem

During each startup of the TPS-1, the firmware and the configuration are read from the boot Flash. The configuration contains also the MAC addresses for the network ports which connect the device to other PROFINET IO devices.

5.1. Hardware Structure for the Boot Operation

The TPS-1 uses a boot loader which reads all necessary data from the boot Flash and carries out the necessary settings. The boot loader is integrated into the ASIC and cannot be changed.

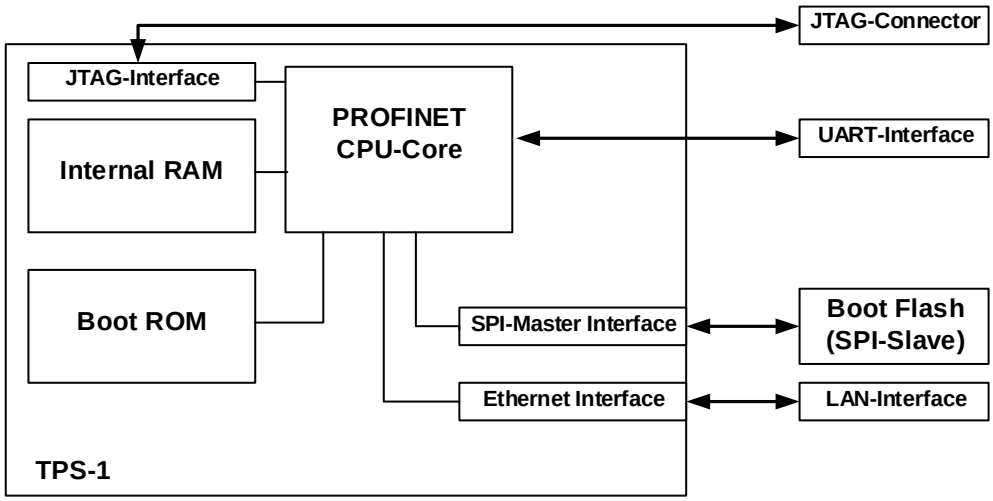

Figure 5-1: TPS-1 structure for the boot process

During the manufacturing process, the following data have to be written to the boot Flash:

- manufacturer information
- device data, device configuration
- I&M information
- operating mode of the TPS-1
- MAC addresses
- PROFINET CPU firmware (Target Host Image)

The necessary data for the boot Flash is assembled by the configuration tool **TPS Configurator.**

5.2. Loading and update of the firmware during the manufacturing process

The serial boot Flash can be written in several ways:

- before mounting with a programmer,
- via JTAG interface[Note1],
- via serial interface (UART)[Note1],
- via ETHERNET interface (BOOTP/TFTP)[Note2]

Note 1 Basically we recommend to use serial interface (UART) during the development phase to fill an empty Flash.

2 via ETHERNET is for firmware update only. If you have TPS-1 toolkit v1.1.0.2 or later, Please pre-program empty Flash with "default image" in the toolkit before the Flash is soldered. It allows to do all required setting via ETHERNET.

5.2.1. UART interface (UART boot)

The UART interface is used for basic communication with the TPS-1. The interface is reduced to a minimum and has no modem lines.

Table 5-1: Boot UART lines

Pin	Signal TPS-1	Description	
C14	UART6_TX	Boot UART "Transmit data"	
C13	UART6_RX	Boot UART "Receive data"	
P12	BOOT_1	Forced Boot	
		Value	**Function**
		0x0	BROM: Boot from Boot Flash is enabled (normal operating mode).
		0x1	UART: Boot via UART is enabled.

The signal line BOOT_1 (Forced Boot) forces a firmware update. For this update, the UART interface is used. In this case also a corrupt version can be updated.

The following parameters are set (fix) for the Interface:

- Baudrate: 115200 baud
- 8-bit data length
- 1 stop bit
- no parity check
- no hardware flow control

5.2.2. SPI master interface (Boot Flash)

The TPS-1 has one SPI master interface for connecting a serial Flash device. The Flash contains the TPS-1 firmware as well as the device configuration and the three required MAC addresses. The operation of this interface is managed by the boot loader.
The interface operates at a maximum speed of 25 MHz. This speed is necessary to realize the "device fast startup" function with the TPS-1.
It is necessary to have a delay time (clock low to data valid) not greater than 8 ns.
The Flash contains the TPS-1 firmware as well as the device configuration and the three required MAC addresses. The serial Flash must have a minimum size of **1 MByte** and must support the Motorola SPI-compatible interface. **The serial flash must be able to write sectors with a size of 4 kByte.**
The used SPI protocol configuration is as follows:

- Motorola SPI frame format;
- 8-bit data words;
- SPI clock out pin has a steady state high value, when data is not being transferred;
- Data is captured on the rising edges and propagated on the falling edges of the SPI clock signal.

You should avoid a device with write protection, particularly with a default setting after power up. The Flash ROM must support the SPI Commands listed in Table 5-3: SPI Boot Loader Driver Commands.

The following flash devices are recommended:

- M25PX32 V MW 3 (4M x 8) Numoyx (Micron)
- M25PX64 (8M x 8) Numoyx (Micron)
- M25PX80 (1M x 8) Numoyx (Micron)
- MX25L6406E (64M x 8) Macronix
- MX25L3206E (32M x 8) Macronix
- MX25L8006E (8M x 8) Macronix
-

Table 5-2: Boot Flash SPI Master Interface

Pin	Signal name	Typ	Function
M12	CS_FLASH_OUT	O	SPI-Master-Interface Firmware Flash: Chip Select (TPS-1) – active low
N13	SPI3_SCLK_OUT	O	SPI-Master-Interface Firmware Flash: CLOCK (TPS-1)
M13	SPI3_SRXD_IN	I	SPI-Master-Interface Firmware Flash: Receive Data (TPS-1) – MISO
M14	SPI3_STXD_OUT	O	SPI- Master-Interface Firmware Flash: Send Data (TPS-1) – MOSI

5.2.2.1. SPI Command Set

A SPI memory device must support the following commands. Writing to the flash requires the command Sector Erase (SE). **It must be possible to write sectors with a size of 4 Kbyte.**

Table 5-3: SPI Boot Loader Driver Commands

Instruction	Code	Address bytes	Dummy bytes	Data bytes
Write enable	0x06	0	0	0
Write disable	0x04	0	0	0
Read status register	0x05	0	0	1
Read Data	0x03	3	0	1 - ∞
Page Program	0x02	3	0	1 to 256
*Sector Erase (4KB)	0x20	3	0	0
Chip (Bulk) erase	0xC7	0	0	0
Read Identification	0x9F	0	0	3

(*) This command requires a sector size of 4 Kbyte.

5.2.2.2. SPI Flash Timing Requirements

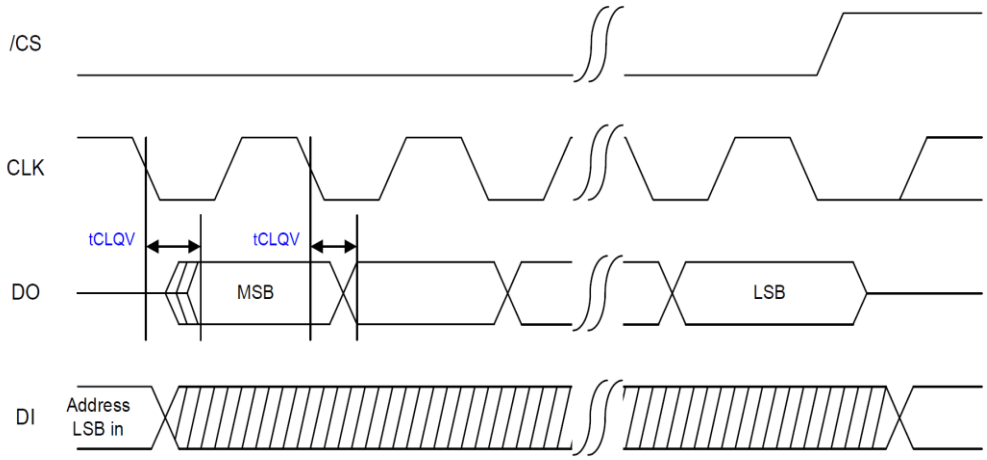

Figure 5-2: Serial Flash output timing requirement

/CS Chip-select input of serial Flash device
CLK Clock input of serial Flash device
DO Data output of serial Flash device
DI Data input of serial Flash device
tCLQV Clock low to output valid time (max. 8 ns).

6. IO Local GPIO Interface

For the development of small IO-Devices the TPS-1 offers the IO Parallel Interface with a maximum of 48 IO lines. These lines could be used for input, output and diagnostic purposes.
There are some restrictions when using the IO Local Parallel interface.

- You can have only **one** Application Identifier (API).
- It is only one module (slot) possible.
- It is only one submodule (subslot) possible.
- The input, output and diagnostic bits must be in a connected order.
- You must always choose groups in byte range (8, 16, 24, 32, etc.).

The TPS Configurator supports the configuration of the IO Local Parallel Interface. (Refer Appendix. A "Configuration of the IO Local Parallel Interface")

6.1. GPIO (digital input and output)

The I/O interface supports **48 GPIOs** (General Purpose Inputs/Outputs). The GPIOs can be used for digital IOs. Each pin can be used individually or in combination with other pins.
Parallel use of the GPIOs and the host interface is not possible!
Unused GPIO pins should be pulled up (10 kΩ to VCC33). Refer chapter2, note 2 to this.

7. TPS-1 Watchdog

The TPS-1 contains two watchdog controllers. One is used to control the PROFINET CPU. The other shall be used to control the connected Host CPU. The signals **WD_IN** and **WD_OUT** are used by the host CPU and the TPS-1 for mutual supervision and to force a restart if necessary.

Table 7-1: Watchdog signals

Pin	Signal TPS-1	Description	Remark
A11	WD_IN	Watchdog Input (from the Host)	This signal triggers the TPS-1 watchdog that monitors the Host CPU. A rising edge of this signal restarts the watchdog counter.
B12	WD_OUT	Watchdog Output (to the Host)	This signal is set when a watchdog trigger of the TPS-1 occurs (active low).

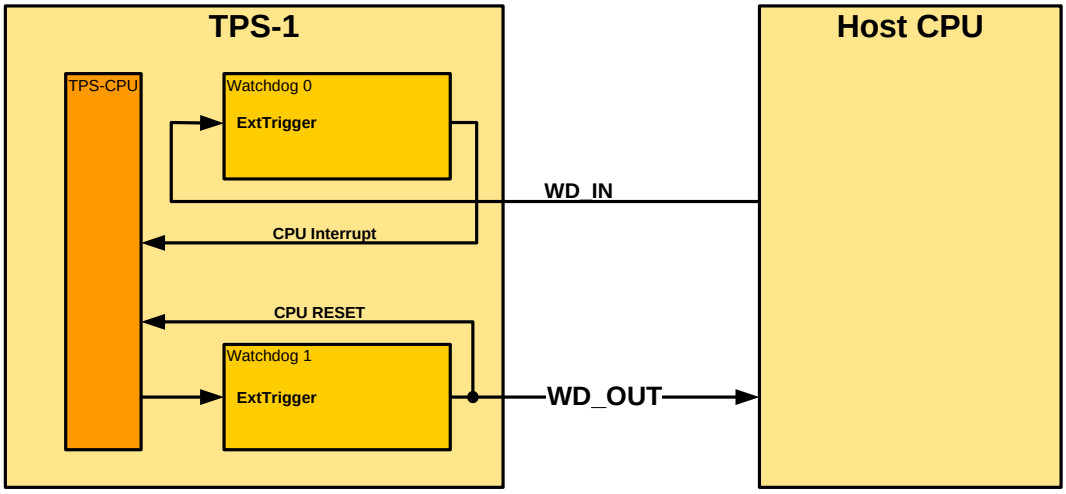

Figure 7-1: TPS-1 Watchdog Lines

7.1. Signal WD_OUT (pin B12)

The **WD_OUT** signal is processed by the TPS-1. The TPS-1 starts its watchdog during start up (the signal is set to high level during power up). This is done by the TPS-1 firmware

The signal WD_OUT indicates that a watchdog error occurs inside the TPS-1.

A watchdog error forces the TPS-1 to a reset. All communication connections to a controller are dropped down.
After a restart of the TPS-1, the host must configure the TPS-1 again.

If you are using the HOST-Interface, the external CPU must guarantee a **secure behavior** of the process output signals in case of a TPS-1 Watchdog.

In case of using the local IO interface, additional circuitry must avoid **insecure signals** for process outputs.

7.2. Signal WD_IN (pin A11)

The signal **WD_IN** is implemented as a watchdog trigger. When recognizing the host watchdog event, the TPS-1 generates a diagnostic alarm and sets the IOPS of the input data to the BAD state.

The watchdog start of the host CPU depends on the individual host. The TPS-1 starts checking the host watchdog when receiving the event **"APP_EVENT_CONFIG_FINISHED".**

The Watchdog Interval can be configured with the TPS Configurator. This information is written into the Boot Flash and is active after the next restart. The watchdog interval can be chosen between 1 ms and 512 ms. During the development you can disable the Host CPU watchdog by setting the interval value to **"0"** (TPS Configurator). Be aware that the watchdog must be activated to avoid unsecure operations of the device.

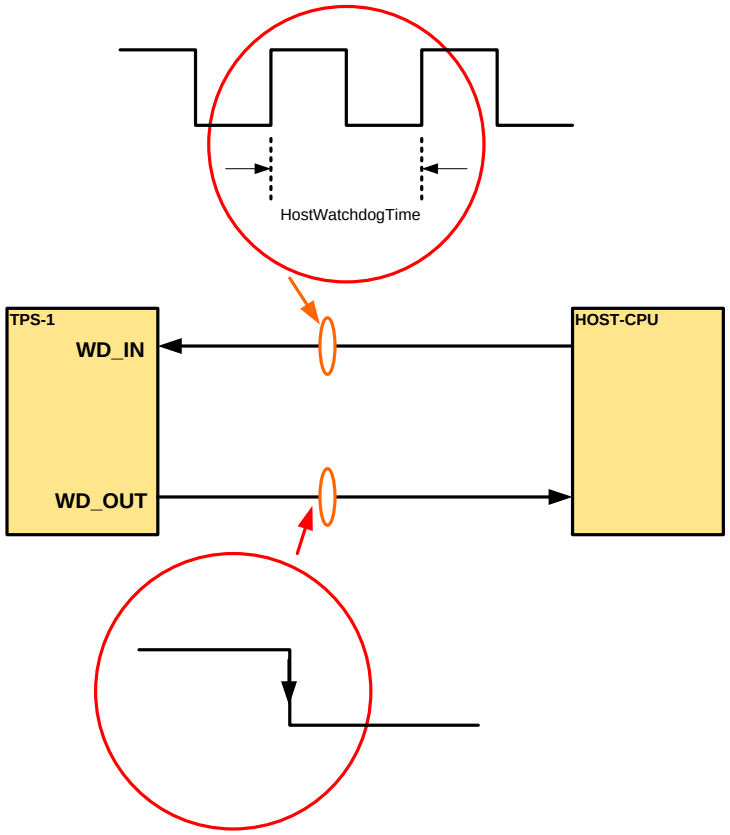

Figure 7-2: Watchdog Characteristics

8. PROFINET IO switch

The TPS-1 contains a PROFINET switch with 2 external ports. Thus, PNIO devices can be connected directly to each other without the need for external switching devices (line topology).

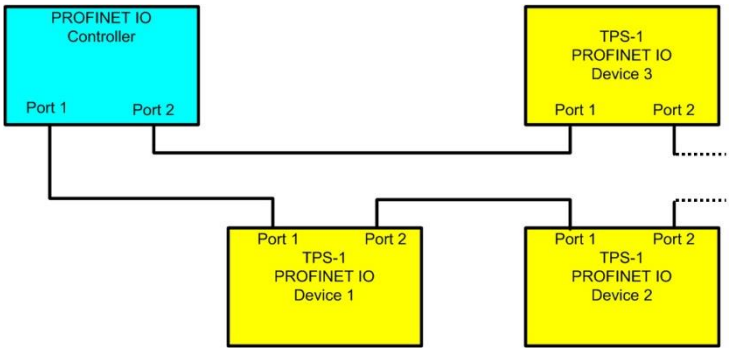

Figure 8-1: Network topologies with the TPS-1

All necessary PROFINET protocols are implemented (LLDP, PTCP, MRP, etc.). Additionally, the TPS-1 features 2 integrated PHY devices (IEEE 802.3, IEEE802.3u, ANSI X3.263-1995 and ISO/IEC9314).

Each port of the integrated PROFINET switch has its own MAC address. The MAC addresses are provided by the device manufacturer and stored in the Boot-Flash of the TPS-1.

The implemented hardware processes support all PROFINET communication channels (NRT, RT and IRT). The Ethernet standards 100BASE-TX and 100BASE-FX are supported.

Additionally, the PHYs support the following features:

- Auto-Negotiation,
- Auto-Crossing
- Auto-Polarity

In order to indicate network status and traffic, the TPS-1 provides respective signaling outputs:

Table 8-1: Status signals of the ETHERNET interface

Pin	Signal Name	Meaning
C12	Link_PHY1	LINK ETHERNET Port 1
D10	ACT_PHY1	Activity ETHERNET Port 1
C11	Link_PHY2	LINK ETHERNET Port 2
A10	ACT_PHY2	Activity ETHERNET Port 2

8.1. 100Base-TX interface

Physical transmission complies with the standard

- 100Base-TX: IEEE 802.3 Clause 25 (CAT 5)

For this interfaces, typically RJ45 plugs are used. However, it is recommended to use special connectors here that are suitable for industrial requirements. The interface hardware of the TPS-1 can be connected directly to the Ethernet transformer. The standard 100Base-TX requires CAT5 cables.
Interface activity is indicated by the signals LED *LINK_PHY1/(2)* and LED *ACTIVITY_PHY1/(2).*
The signal LED *LINK_PHY1/(2)* is also used to indicate the function "Search Device / Flashing".

8.1.1. 100Base-TX interface (Port 1)

Table 8-2: Signal lines 100Base-TX interface (Port 1)

Pin	Designation	Description
F13	P1_TX_P	Transmit data+
F14	P1_TX_N	Transmit data-
E13	P1_RX_P	Receive data+
E14	P1_RX_N	Receive data-

8.1.2. 100Base-TX interface (Port 2)

Table 8-3: Signal lines 100Base-TX interface (Port 2)

Pin	Designation	Description
J13	P2_TX_P	Transmit data+
J14	P2_TX_N	Transmit data-
K13	P2_RX_P	Receive data+
K14	P2_RX_N	Receive data-

8.2. 100Base-FX interface (Fiber Optic)

The physical transmission complies with the standard:

- IEEE 802.3 Clause 26 – 100.Mbit/s Ethernet for multimode fiber optic.

The connection of fiber optic wiring (POF und PCF) should be done with Fiber Optic Diagnostic Transceivers (**Avago Technologies QFBR-5978AZ – this transceiver fulfilled the requirements for the automation industry**). These devices provide the medium conversion and line diagnostics.

8.2.1. 100Base-FX interface (Port 1)

Table 8-4: Signal lines 100Base-FX interface (Port 1)

Pin	Designation	Description
C9	I2C_1_D_INOUT	I^2C data line
C6	SCLK_1_INOUT	I^2C clock line
B8	P1_SD_P	Signal detect (Difference +)
A8	P1_SD_N	Signal detect (Difference -)
A9	P1_RD_N	Receive signal (Difference -)
B9	P1_RD_P	Receive signal (Difference +)
A5	P1_FX_EN_OUT	Transmitter enable (transceiver output)
B6	P1_TD_OUT_P	Transmit signal (Difference +)
A6	P1_TD_OUT_N	Transmit signal (Difference -)

8.2.2. 100Base-FX interface (Port 2)

Table 8-5: Signal lines 100Base-FX interface (Port 2)

Pin	Designation	Description
M11	I2C_2_D_INOUT	I^2C data line
L11	SCLK_2_INOUT	I^2C clock line
N8	P2_SD_P	Signal detect (Difference +)
P8	P2_SD_N	Signal detect (Difference -)
P9	P2_RD_N	Receive signal (Difference -)
N9	P2_RD_P	Receive signal (Difference +)
P5	P2_FX_EN_OUT	Transmitter enable (transceiver output)
N6	P2_TD_OUT_P	Transmit signal (Difference +)
P6	P2_TD_OUT_N	Transmit signal (Difference -)

8.3. I2C-Bus – LWC Diagnostic

The TPS-1 provides two "**I^2C Interface Lines**" for fiber optics diagnostic purposes. The recommended AVAGO transceiver (AFBR-5978Z) features internal registers that can be read by the I^2C interface. The transceiver can deliver diagnostic information via the I^2C interface. If signal quality is dropping, an alarm indication can be sent to the controller.

Table 8-6: I^2C interface lines

Pin	Signal TPS-1	Description
C9	I2C_1_D_INOUT	Fiber Optic Port1 I^2C-Bus "Data"
C6	SCLK_1_INOUT	Fiber Optic Port1 I^2C-Bus "Clock"
M11	I2C_2_D_INOUT	Fiber Optic Port2 I^2C-Bus "Data"
L11	SCLK_2_INOUT	Fiber Optic Port2 I^2C-Bus "Clock"

8.4. Additional TPS-1 pins

The pins ATP and EXTRES are used for PHY1 and PHY2.

Table 8-7: Additional TPS-1 pins

Pin	Designation	I/O	Description
H12	ATP	AI/O (analog I/O)	Analog Test: This signal is used for the manufacturing process. Pin is left open.
H13	EXTRES	AI/O (analog I/O)	Reference resistor: Connect via a resistor 12.4KΩ / 1% to GND. This external resistor should be placed as close as possible to the chip. It must be terminated to analog GND.

8.5. Integrated voltage regulator 1.5 V

The integrated PHY components require a supply voltage of 3.3 V and 1.5 V. The supply voltage 1.5 V is supported by an internal voltage regulator. For a correct operation, some additional electronic components are necessary. Figure 8-2: Internal voltage regulator shows the design of the switching regulator.

During normal operation (Switching Regulator is running and POR is active), the pins TEST1, TEST2, and TEST3 are connected to GND via a pull-down resistor.

It is also possible to feed the TPS-1 with an external voltage of 1.5 V. Then you have to switch off the regulator (Pin **TEST1** set to 1 with a pull-up). The regulator output (Pin **LX**) changes to HiZ status.

The POR function must be in operation because this signal is used in combination with the external signal **RESETN** to enable the TPS-1 dies.

Caution: The 3.3 V supply voltage has to be connected to BVDD (pin J1) and AVDD_REG (pin F2). AVDD_REG is used to generate the internal POR signal of the TPS-1. If you are not using the internal regulator the pin AVDD_REG has also be connect to 3.3 V to prevent reset blocking.

The other combinations of the signals TEST1, TEST2 and TEST3 are used for the chip test at the factory process.

The switching regulator is designed to supply the PHY components. It is not allowed to connect additional components. You will find a recommendation for the circuitry of the switching regulator in the Chapter **"Board Design Information, Switching Regulator"**.

Table 8-8: Switching regulator operating modes describes the different modes of the switching regulator.

Table 8-8: Switching regulator operating modes

TEST3 (Pin E1)	TEST2 (Pin G3)	TEST1 (Pin H3)	Function
0	0	0	Normal mode: Regulator and POR **on**.
0	0	1	Only POR mode: Regulator **off**, POR **on**.
0	1	0	Regulator and POR circuitry switched **off (Note)**.
			Other options reserved for test

Note: This combination should be avoided, because you set the TPS-1 permanently into the reset state.

It is important that the input **FB** is connected to a smoothed 1.5 V voltage. The regulator adjusts the output voltage with negative feedback using this pin.

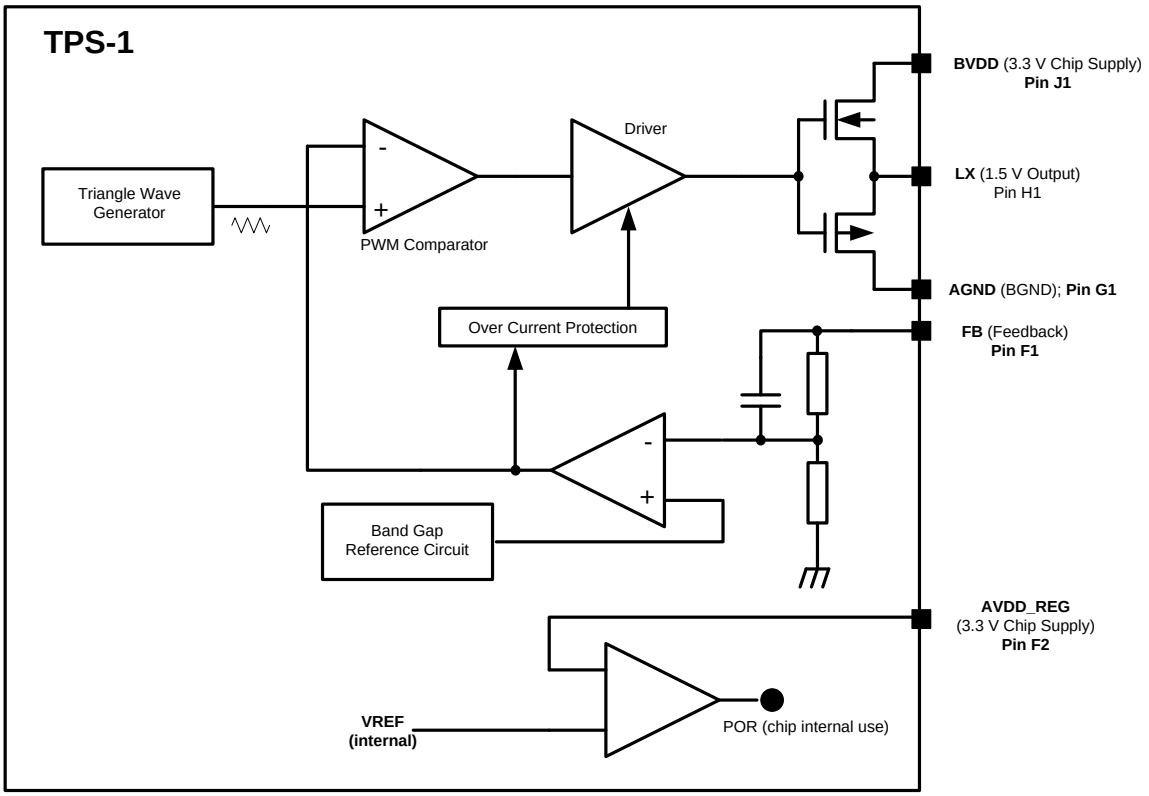

Figure 8-2: Internal voltage regulator

The time of power-supply rise to the point where all power supplies are stabilized must be reached within 100 ms.

The typical behavior of the power supplies is shown in Figure 8-3.

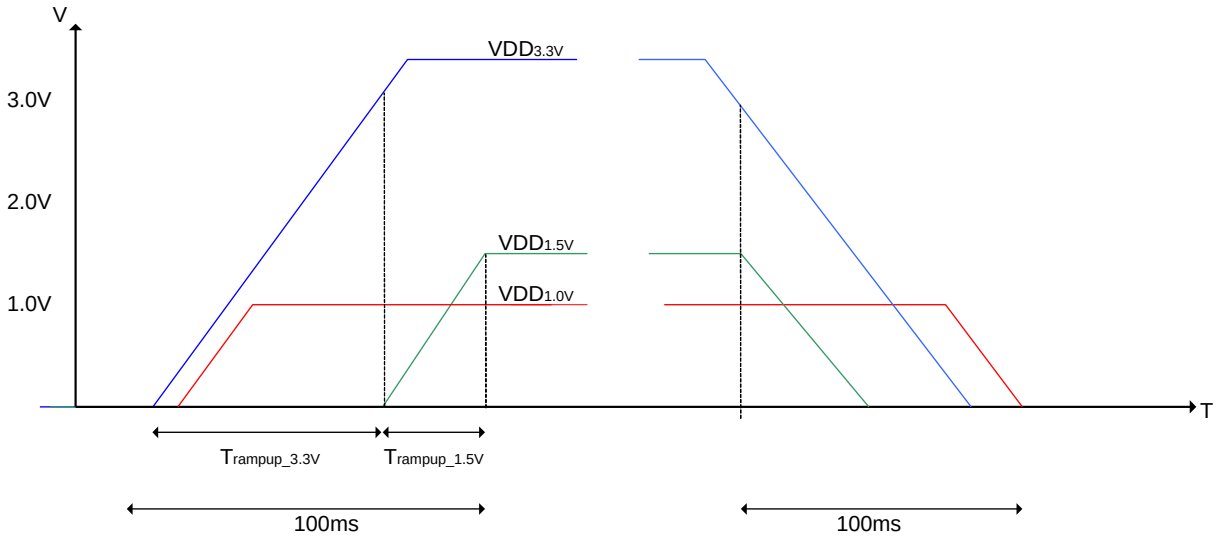

Figure 8-3: TPS-1 Power-up sequence

9. Clock circuit

The clock distribution of the TPS-1 requires an oscillator with 25 MHz (***XCLK1, XCLK2***). All necessary internal clock signals are derived from this external clock (internal clock unit).

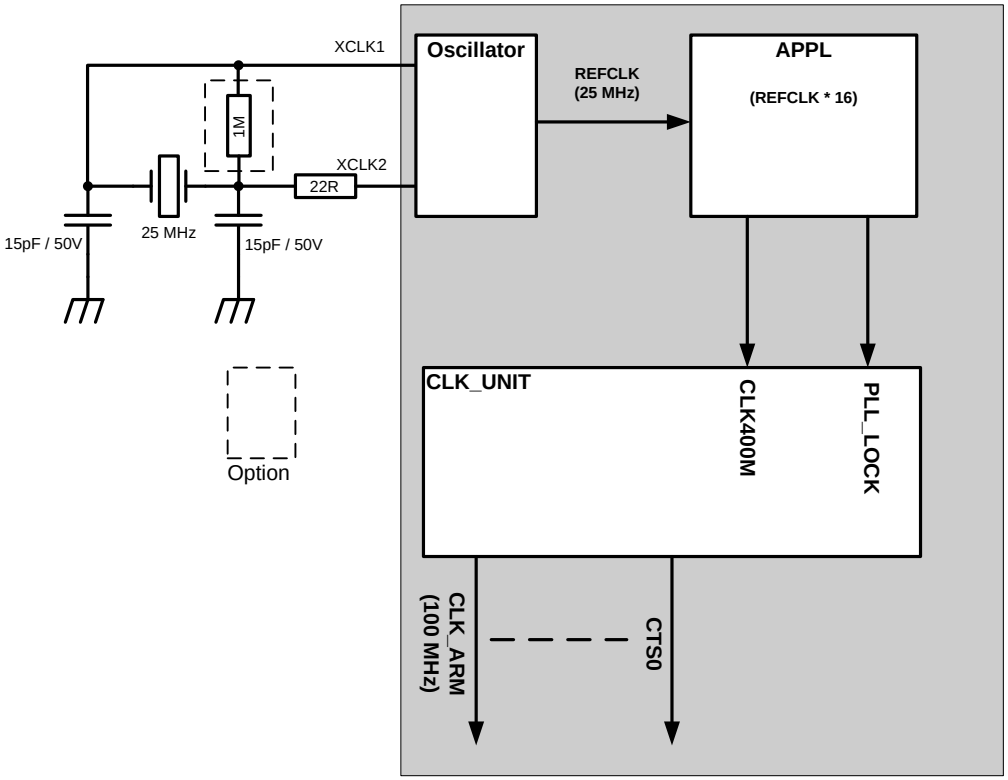

Figure 9-1: Wiring of the TPS-1 clock

The circuitry example (Figure 9-1) is based on the Epson Toyocom FA-238 Crystal Unit.

The crystal tolerance must not be more than ***+- 50 ppm*** at ***25 MHz.*** The duty cycle has to be 50% +- 10%. This tolerance must be preserved for the entire life span.

10. Reset of the TPS-1

An external reset is caused by a "low" level at the signal pin **RESETN**. This condition is held until the "low" level changes to a "high" level. During startup of the power supply the 3.3 V voltage is controlled by the TPS-1 (internal). The 1.5 V voltage (if fed from external) and the 1.0 V voltage must be controlled by an external circuitry.

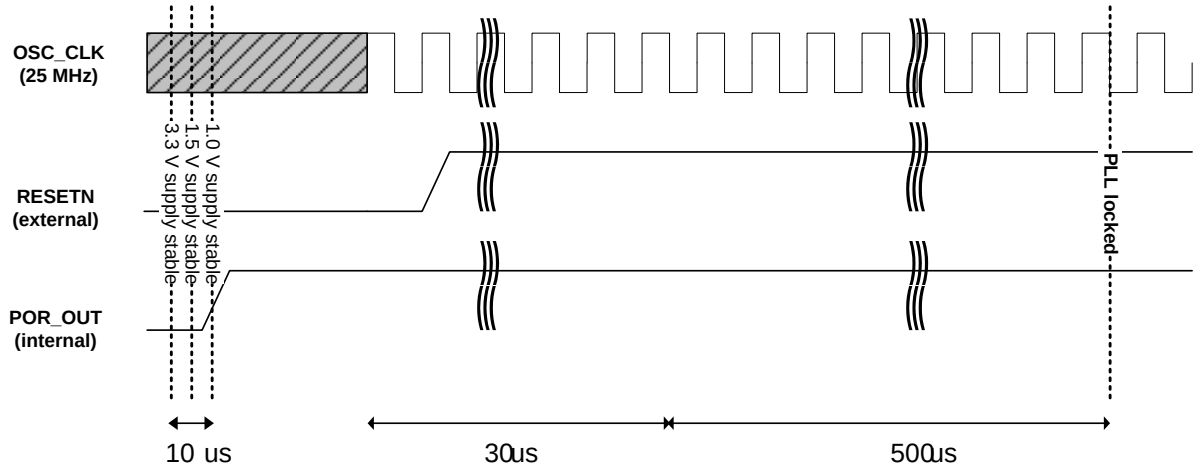

Figure 10-1: Reset behavior

The start-up time of the oscillator depends on the external components (quartz, RLC). As a general rule of thumb it is roughly in the range of 1 ms.

11. Boundary Scan Interface (JTAG)

The JTAG interface is used for the Boundary Scan test.

Table 11-1: JTAG interface pin definition

Pin	Designation	Type	Description	Remark
K5	TRSTN	I	Test Reset	JTAG Reset. Input: Reset signal of the target port. External pull-down (4K7 Ω to GND)
L6	TMS	I	Test Mode Select	JTAG interface is activated from the debug unit. pull-up (4K7 Ω to V_{DD})
L7	TDO	O	Test Data Output	
J5	TCK	I	Test Clock	JTAG clock signal to the TPS-1. It is recommended that this pin be set to a defined state on the target board. External pull-up (4K7 Ω to V_{DD})
L5	TDI	I	Test Data Input	External pull-up (4K7 Ω to V_{DD})

Table 11-2: JTAG interface pin definition

Pin TM0	Pin TM1	Function
0	0	normal operation mode
1	1	Boundary scan mode (see BSDL file)

11.1.1. Circuit recommendation of the JTAG Interface

If the JTAG interface is unused in the customer application the TRSTN input of the TPS-1 should be connected to digital GND via a 4.7kΩ resistor. The circuit recommendation for the interface looks as follows.

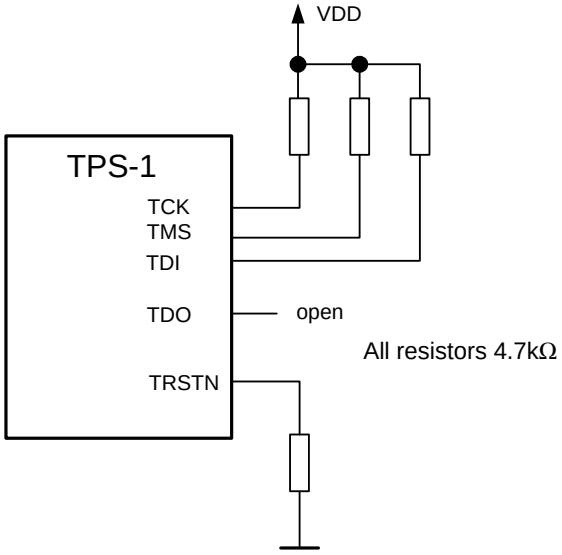

Figure 11-1: Unused JTAG Interface

If the customer wants to use the JTAG interface for boundary scan test, the customer has to check whether the boundary scan tool, that he intends to use, has specific requirements with respect to the TRSTN circuit in the target system. If the boundary scan tool has specific requirements, the circuit in the target system must be made configurable. The subsequent figure shows the situation, that the boundary scan tool requires a pull-up at the TRSTN input of TPS-1.

For using the JTAG interface with a boundary scan tool, you should implement the following.

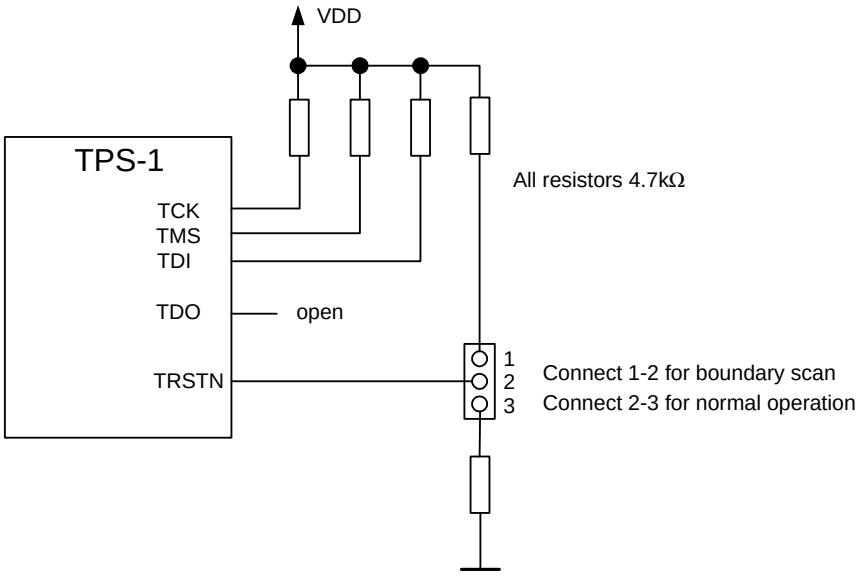

Figure 11-2: JTAG useable for boundary scan

Appendix.A Setting of operating modes

The basic configuration of the TPS-1 is managed with the "TPS Configurator" software. You can set the configuration of the host interface (serial, parallel) or the configuration of the Local IO Interface. There you can choose the IO interface (serial or parallel digital outputs).
When you choose one of the four operation modes from the **General Settings**, only that operation mode will be activated and the values can be modified. Other operation modes will be deactivated and their values can be viewed but not modified.
The configuration data and the firmware are stored into the serial boot Flash device. During each start-up the configuration is used to initialize the TPS-1. The necessary MAC-Addresses are permanently stored on the Flash Device. They cannot be changed after the initial setting (see ***"Ethernet Settings"*** *tab*).

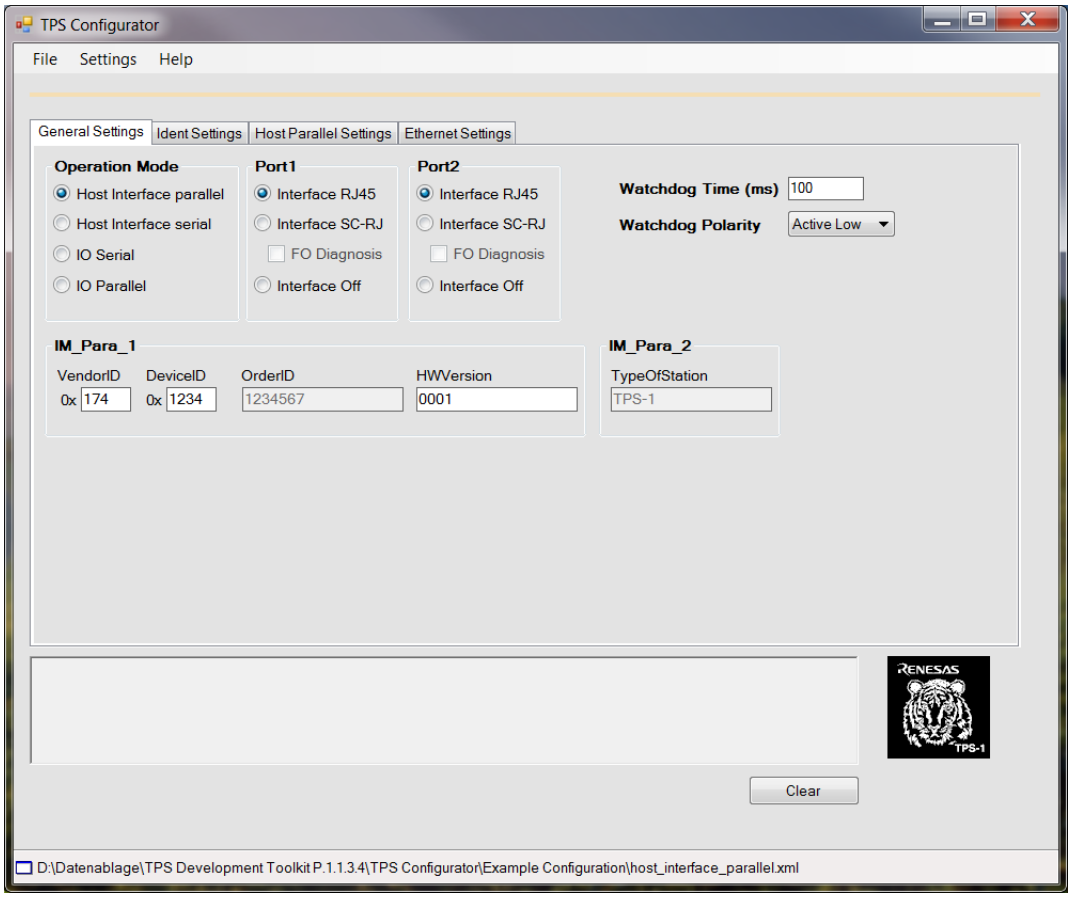

Figure A-1: First tab of the "TPS Configurator"

The configuration items on tab *"General Settings"* set the basic operation modes.

- Host Serial: A host CPU is connected via the SPI slave interface
- Host Parallel: A host CPU is connected via the parallel interface
- IO Serial: An IO device is connected via a simple SPI master interface
- IO Parallel: The GPIO pins are used in a user-specific order

By choosing a special operation mode, the corresponding configuration tabs are activated (label **"active"**). Only these tabs can be edited, all others are locked.

A.1 Host Interface

The host interface realizes the connection of external host CPUs. Data exchange is carried out via an internal ***Shared Memory*** area. Depending on the type of external host CPU, you can choose a serial (SPI slave) or a parallel interface.

A.1.1 Parallel Interface

The parallel host interface can be configured to work at 8-bit or 16-bit data width and in Motorola or Intel operating mode. Thus, the interface facilitates the connection of different processor types.

You find the respective parameters on the window tab "Host Parallel Settings".

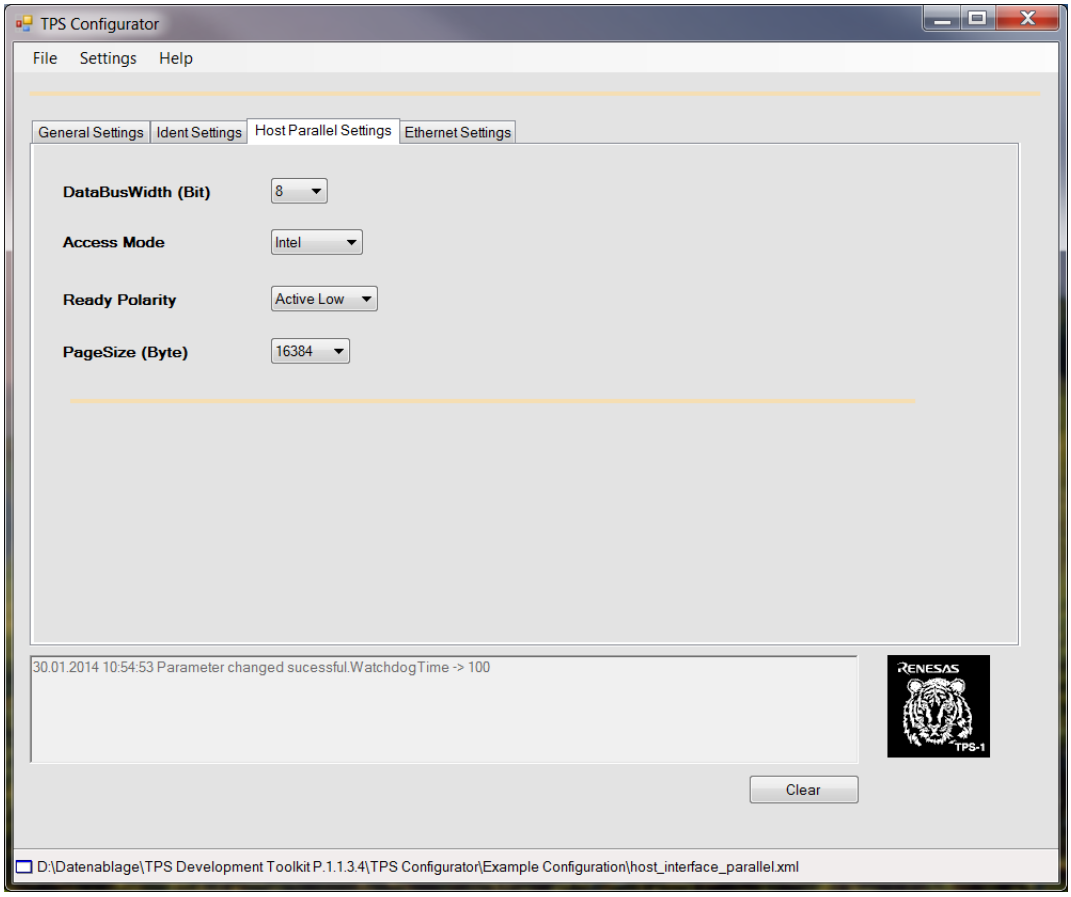

Figure A-2: Parallel host interface configuration

A.1.2 Serial Interface

The serial host interface is an SPI-Slave interface. The necessary hardware settings are available on tab ***"Host Serial Settings"***.
The watchdog function for the host CPU is configured below the headline ***"General Settings".*** You can choose watchdog time and activity level.

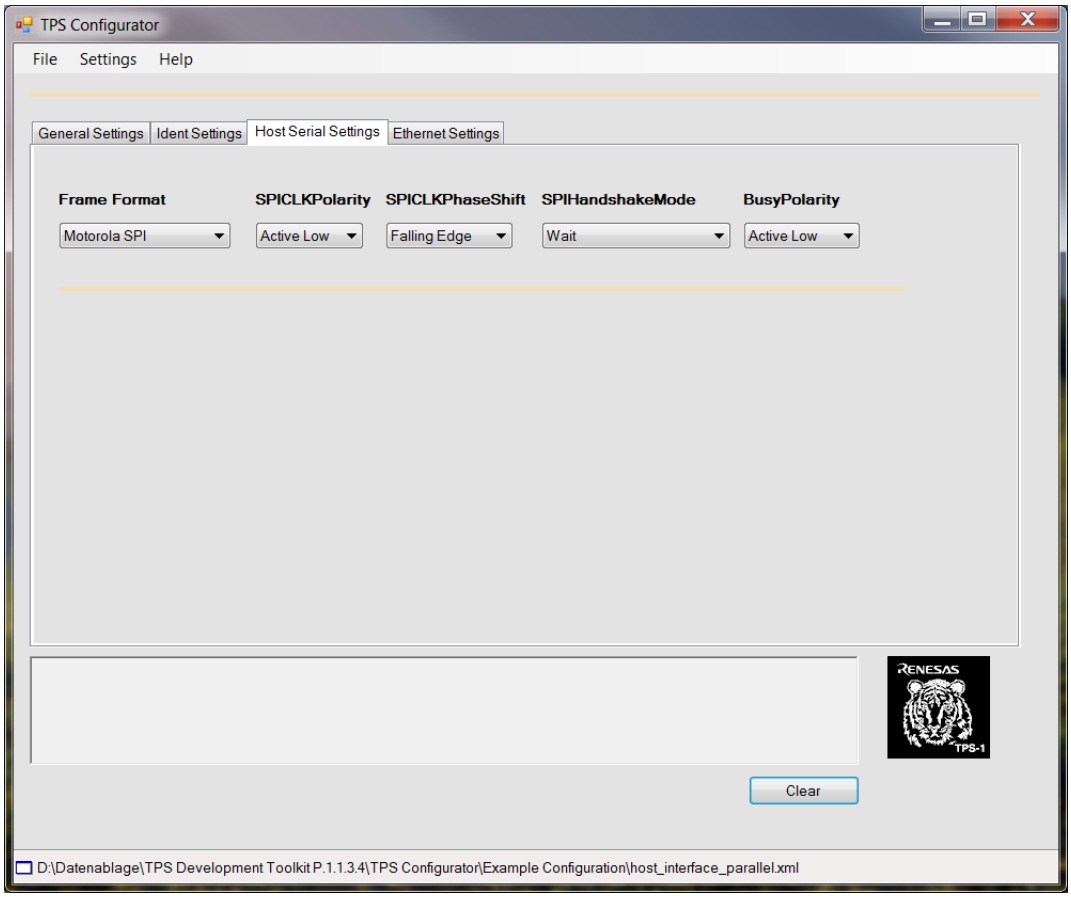

Figure A-3: Serial host interface configuration

Below the headline ***"Host Serial Settings"*** you find the settings for the SPI interface (MotorolaSPI, Microwire, etc.).

A.2 I/O-Configuration

These settings control the 48 GPIOs and the SPI master interface. GPIOs can be set individually or in groups.
Single or groups of GPIOs can be configured to work as inputs or outputs. On the tab ***"Channel"*** you can configure some GPIOs for diagnostic functions (PROFINET ChannelDiagList).

A.2.1 IO Parallel

At first you have to configure the basic addressing (e.g. API, SlotNo, et cetera).

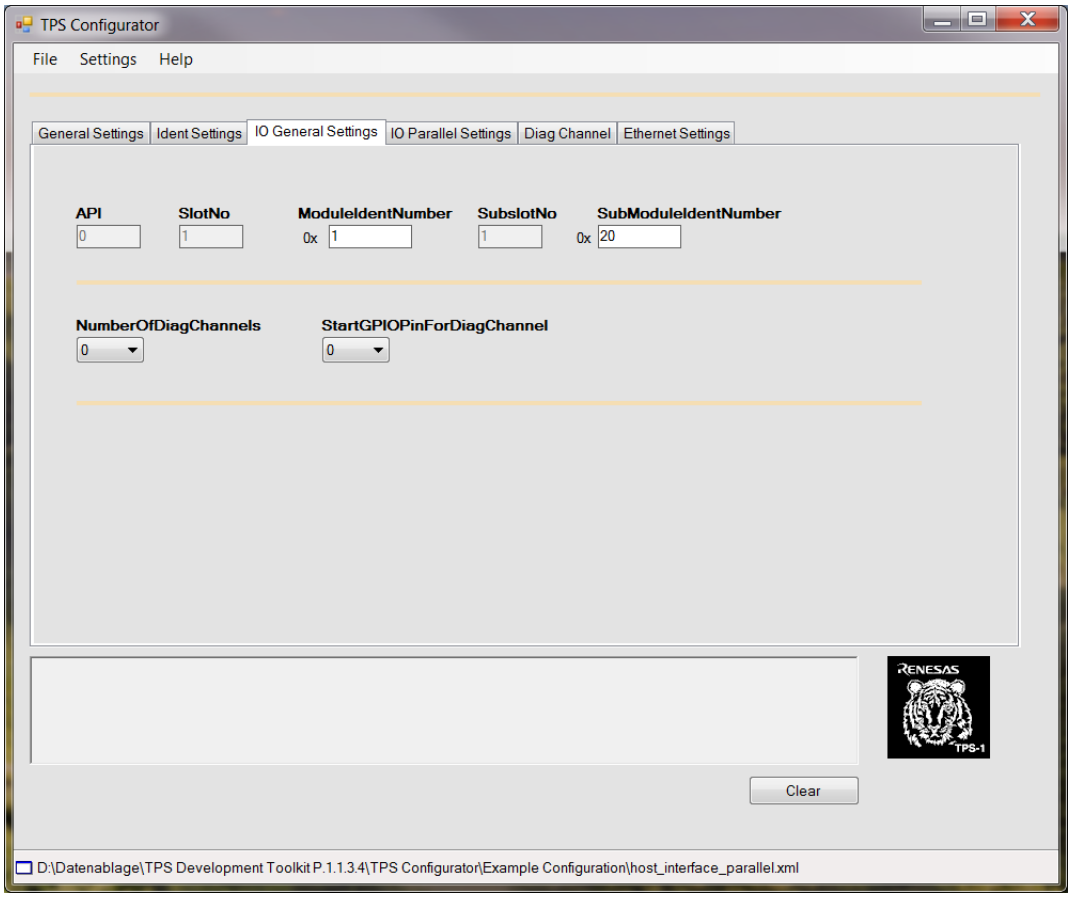

Figure A-4: Parallel Interface configuration part 1

After that, you configure the diagnosis channels (DiagChannels).

To configure the GPIO's you must refer to the part IO Parallel Settings.

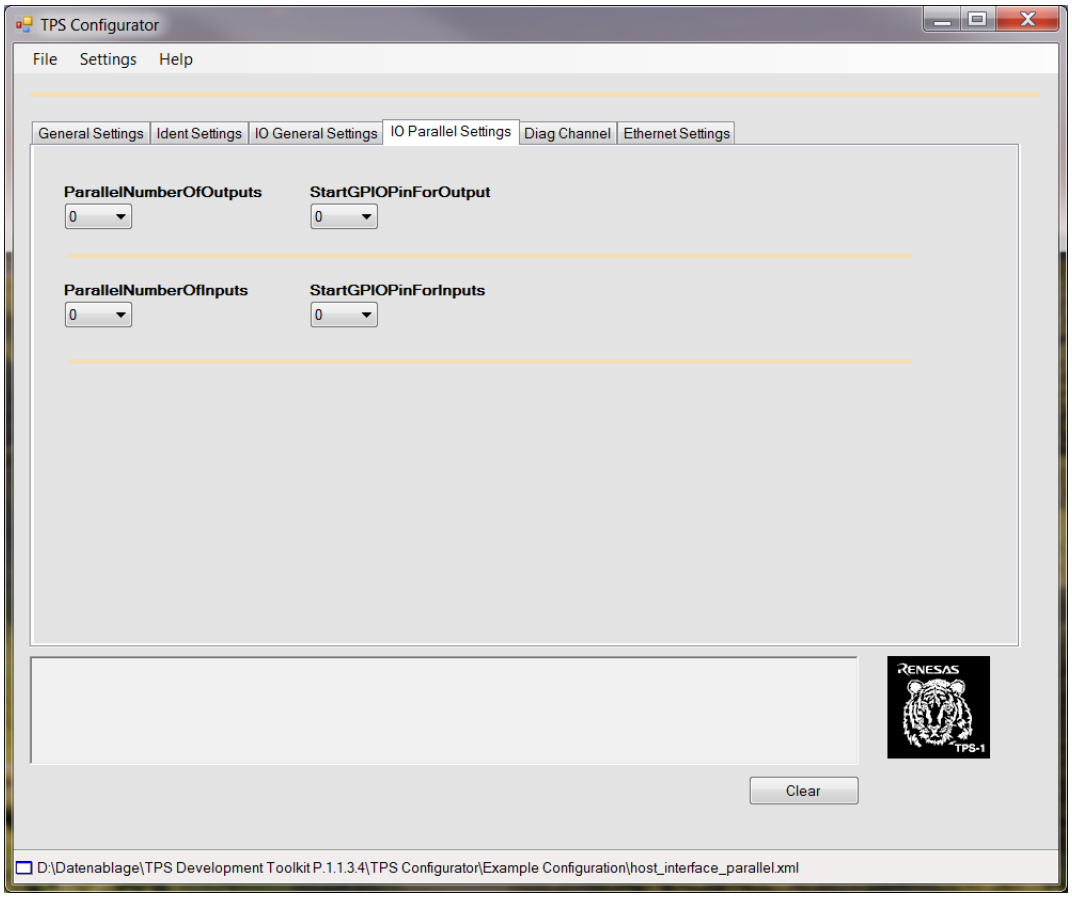

Figure A-5: Parallel Interface configuration part 2

A.2.2 IO Local Interface

For the development of small IO-Devices the TPS-1 offers the IO Parallel Interface with a maximum of 48 IO lines. These lines could be used for input, output and diagnostic purposes.

There are some restrictions when using the IO Local Parallel interface.

- You can have only one Application Identifier (API).
- It is only one module (slot) possible.
- It is only one submodule (subslot) possible.
- The input, output and diagnostic bits must be in a connected order.
- You must always choose groups in byte range (8, 16, 24, 32, etc.).

The TPS Configurator supports the configuration of the IO Local Parallel Interface.

You can set all necessary parameters for the IO Local Parallel Interface (e.g. API, SlotNumber, ModuleIdentNumber, etc.). On the next program tap you can configure the diagnostic channels.

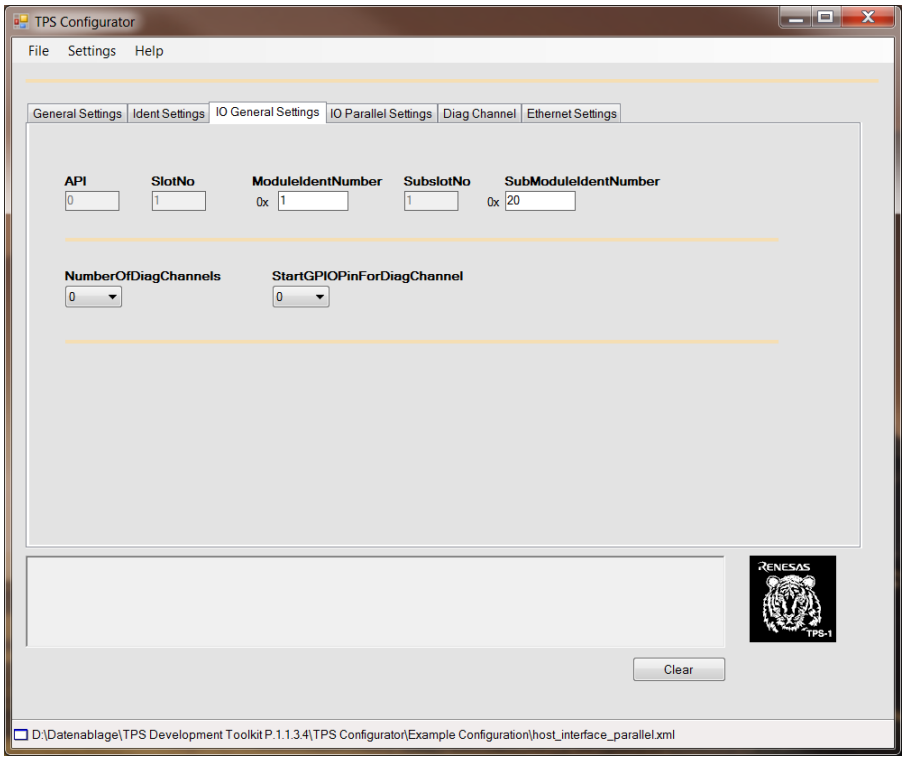

Figure A-6: IO Local Parallel Interface Mask

A.2.3 I&M0 Configuration (I&M0 data)

The provision of these parameter values is mandatory for every PROFINET device (I&M0 profile).

Table A-1: I&M0 Parameter

Parameter	Description
VENDOR ID	The parameter VENDOR_ID carries the ID of the respective device manufacturer. It is assigned by PI.
ORDER ID	This parameter contains the complete order number or at least a relevant part that allows unambiguous identification of the device/module within the manufacturer's web site.
SERIAL_NUMBER	A serial number is a unique production number of the device manufacturer even for devices with the same hardware, software or firmware edition.
Hardware-Revision	The content of this parameter characterizes the edition of the hardware only.
Software-Revision	The content of this parameter characterizes the edition of the software or firmware of a device or module.
REVISION_COUNTER	A changed value of the REVISION_COUNTER parameter of a given module marks a change of hardware or of its parameters.
PROFILE_ID	A module providing a special application profile may contain extended information (PROFILE_SPECIFIC_TYPE) about its function and/or sub devices, e.g. HART.
PROFILE_SPECIFIC_TYPE	In case a module provides a special application profile this parameter contain information about the usage of its channels and/or sub devices.
IM_VERSION	This parameter indicates the implemented version of the I&M functions.
IM_SUPORTED	This parameter indicates the availability of I&M records.

All parameters must be edited separately or can be copied as default values from the firmware. If you need more information regarding I&M0 parameters, please refer to the PROFINET specification.

A.3 Ethernet Interface Configuration

The Ethernet configuration is edited on tab ***"Ethernet Settings"***. This is also the window for configuring the factory settings (e.g. MAC addresses).

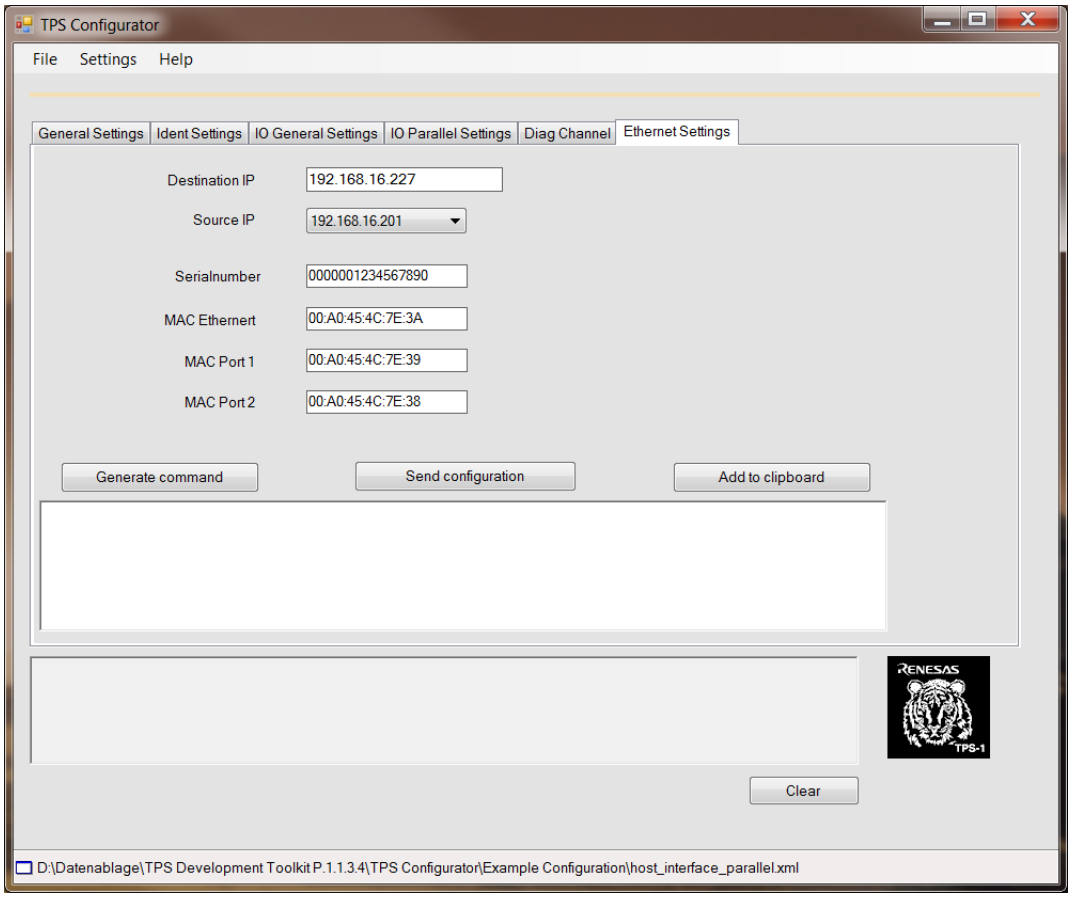

Figure A-7: Ethernet Interface Configuration

The TPS-1 needs three MAC addresses to operate. One is used for the TPS-1 itself; additionally, each of the two ports has an individual MAC address as well in order to support port-based communication services for e.g. LLDP.

The serial number of the device is edited in "S.N.". The IP addresses ***Destination IP*** and ***Source IP*** are needed for the transmission of configuration data via the Ethernet interface of the TPS-1.

The PC on which this tool is running represents the Source IP address. The Destination IP represents the PROFINET Device to configure. The configuration of the device is carried out in a subnet to which only the Source PC and the PROFINET Device belong (factory configuration). The device at first accepts any frame that contains the necessary MAC addresses. It is possible to program the MAC addresses one time (it is not allowed to change this initial configuration later).

A.4 Copying the configuration data into the Boot Flash

After the configuration data is complete, it has to be transferred to the PROFINET device. During the manufacturing process, the data can be copied into the Flash device with a special program (FS_Prog.exe). The TPS Configurator can generate a command with all the parameters ***(see "Generate Command")***.

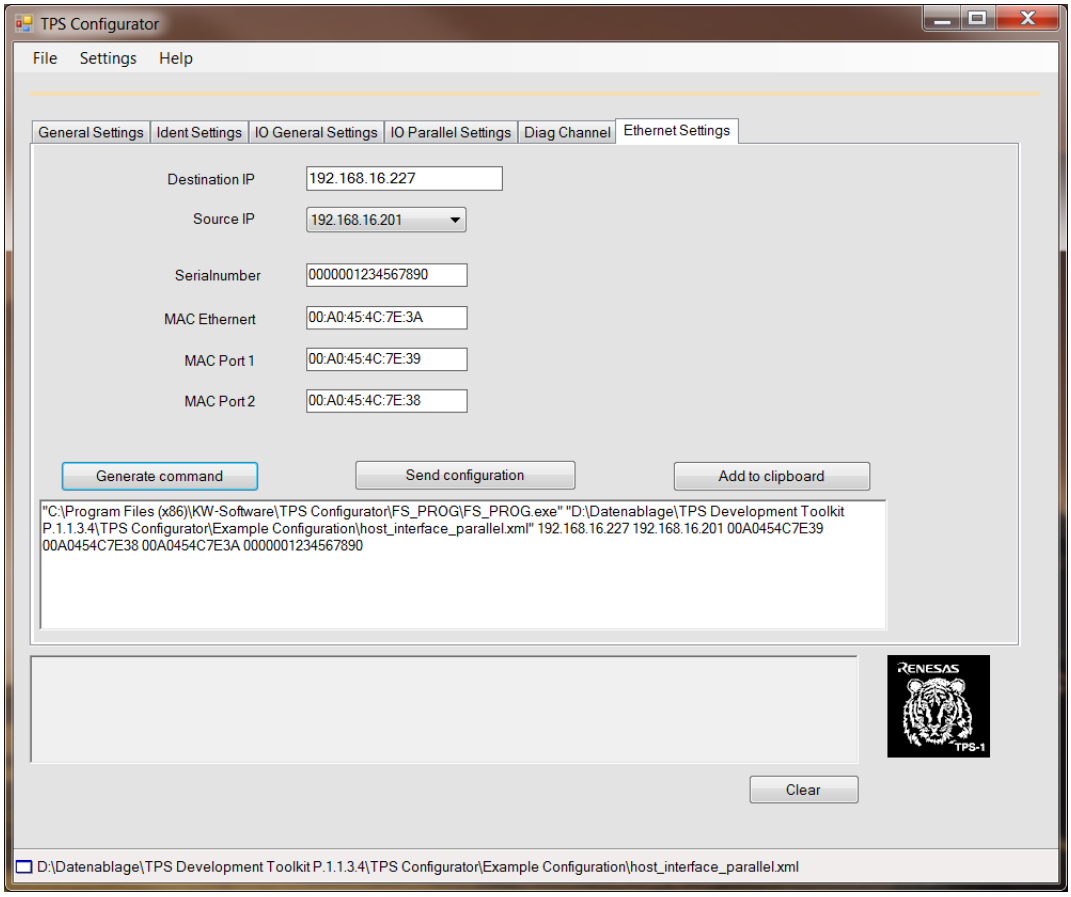

Figure A-8: Writing the TPS-1 configuration

By clicking "Send Configuration", the transfer of the configuration data to the PROPINET IO device is started.

A.5 Generating a complete serial boot Flash Image

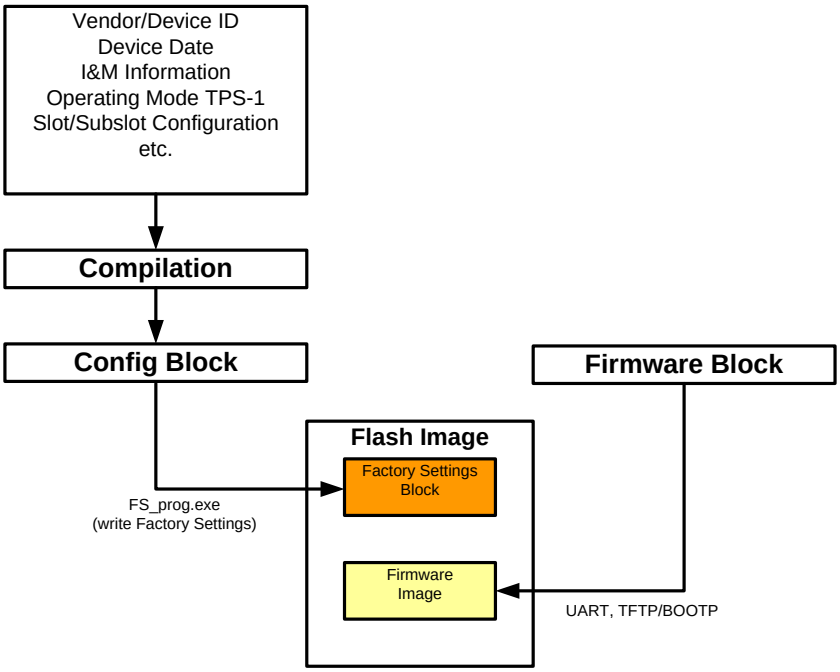

Figure A-9: Generating a Boot Flash Image

The generated XML file is compiled and assembled to a Configuration Block. (the TPS-Configurator build the Configuration Block that is transferred). The configuration data is then copied to the TPS-1 and stored into the serial boot Flash device (Factory Settings Block).
On the TPS-1 special software is running that enables you to copy a firmware image into the serial boot Flash device. The firmware block can be copied from every directory on your PC.

Appendix.B Board Design Information

This chapter provides useful information related to PCB design.

B.1 Voltage supply

The TPS-1 requires 3 supply voltages. The necessary supply voltages can be delivered directly from the power supply unit. In this case, the switching regulator is not needed (refer Chapter8.5). You can also use the integrated voltage regulator that is fed with 3.3 V. The recommended circuitry described in AppendixB.2

Necessary supply voltages of the TPS-1:

- 3.3 V nominal (between 3.0 V and 3.6 V)
- 1.5 V nominal (between 1.35 V and 1.65 V)
- 1.0 V nominal (between 0.9 V and 1.1 V, core voltage)

B.2 Switching Regulator

Switching regulator (features):

- Output voltage : 1.5V +/-5%
- Output current : 250 mA (max. DC)
- Power supply voltage : 3.3V +/- 0.3V
- Switching frequency : 1 MHz (typ)

B.2.1 Wiring for the Switching Regulator

The following figure gives the recommendation of the wiring.
The switching regulator output (LX) delivers the 1.5 V voltage, that is smoothed with the external devices. This voltage is connected to pin $V_{DD1.5V}$.
The following external devices are necessary for the switching regulator:

Figure B-1 shows the wiring for the external regulator circuit if the regulator is used to generate the 1.5 V for the PHYs.

Notes:

- All components should be placed as close as possible to the TPS-1.
- *Important*: The characteristic of C1 is mandatory. A lower ESR will cause problems with the regulator oscillation.

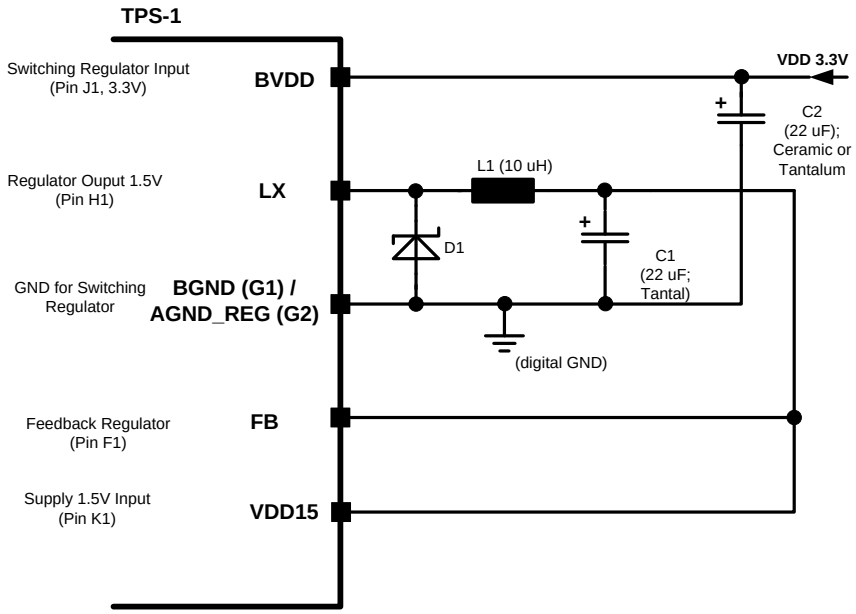

Figure B-1: Wiring of the switching regulator

Table B-1: Part Table for the Switching Regulator

Part	Type	Characteristics	Recommended components
C1*	Tantalum Capacitor	22 uF +/- 20% ESR: 150–350 mΩ	PSLB21A226M (NEC TOKIN) TCJB226M010R0300 (AVX) T494C226K016AT (KEMET)
C2	Capacitor	22uF +/- 20%	Ceramic or Tantalum
D1	Schottky Rectifier Diode	30 V, 1 A	SBS005 (Sanyo) STPS1L30UPBF (ST)
L1	Inductor	10 uH	VLCF5028T (TDK)
C1a*	Ceramic Capacitor	22 uF +/- 10%	Evaluated with (Murata): GRM32ER71A226KE20L
R1a*	Resistor	100 mΩ +/- 1%	Evaluated with: MCR18EZHFLR100 (ROHM)

To avoid the recommended tantalum capacitor it is possible to compose the needed characteristics with a series connection of a resistor and a ceramic capacitor. If you use ceramic capacitors only C1 has to be replaced by a ceramic capacitor in connection with a series resistor. C2 did not need a series resistor.

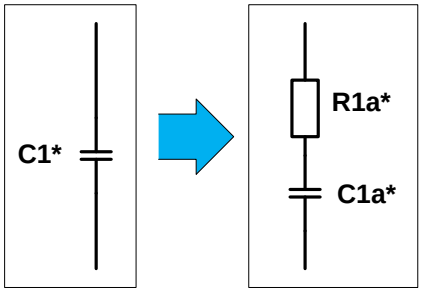

Figure B-2: Change Tantalum to Ceramic Capacitor

B.2.2 Layout Example for Switching Regulator

This chapter shows an example for the connection between the external output and regulator. The real design of the layout must be done on the PCB board.

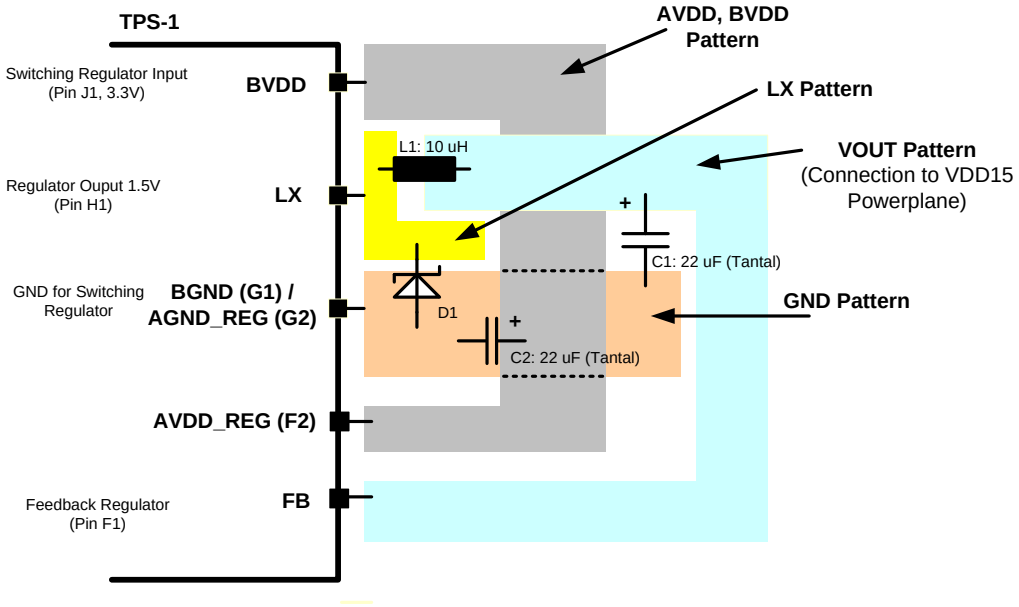

Figure B-3: Switching Regulator layout example

Instead of the tantalum capacitors you can also use ceramic capacitors. Please refer to chapter B2.1.

B.3 Board Design Recommendations for Ethernet PHY

B.3.1 Supply Voltage Circuitry

The on-chip PHYs of the TPS-1 require additional filtered operating voltages as shown in the table below.

Table B-2: Supply Voltages Circuitry for Ethernet PHY

Pin	Pin Name	Function	Supply Voltage Generation
D14	P1VDDARXTX	Analog port RX/TX power supply, 1.5 V (PHY port 1)	Must be generated from VDD15 (1.5 V) via a filter.
L14	P2VDDARXTX	Analog port RX/TX power supply, 1.5 V (PHY port 2)	
G14	VDDAPLL	Analog central power supply, 1.5 V	
H14	VDDACB	Analog central power supply, 3.3 V	Must be generated from VDD33 (3.3 V) via a filter.
E12	VDD33ESD	Analog test power supply, 3.3 V	
G13	VSSAPLLCB	Analog central GND	Must be derived from GND Core/IO via a filter or connected to GND Core/IO at the far end from TPS-1.
D12, D13, L12, L13	AGND	Analog GND for PHYs.	Must be generated from digital GND by filter.

Besides filtering, the PHY-specific supply voltages should be equipped with pairs of decoupling capacitors. 10 nF and 22 nF capacitors should be used for **VDD33ESD**, **VDDAPLL**, **VDDACB** and **P(2:1)VDDARXTX**. They should be placed as close as possible to the chip.

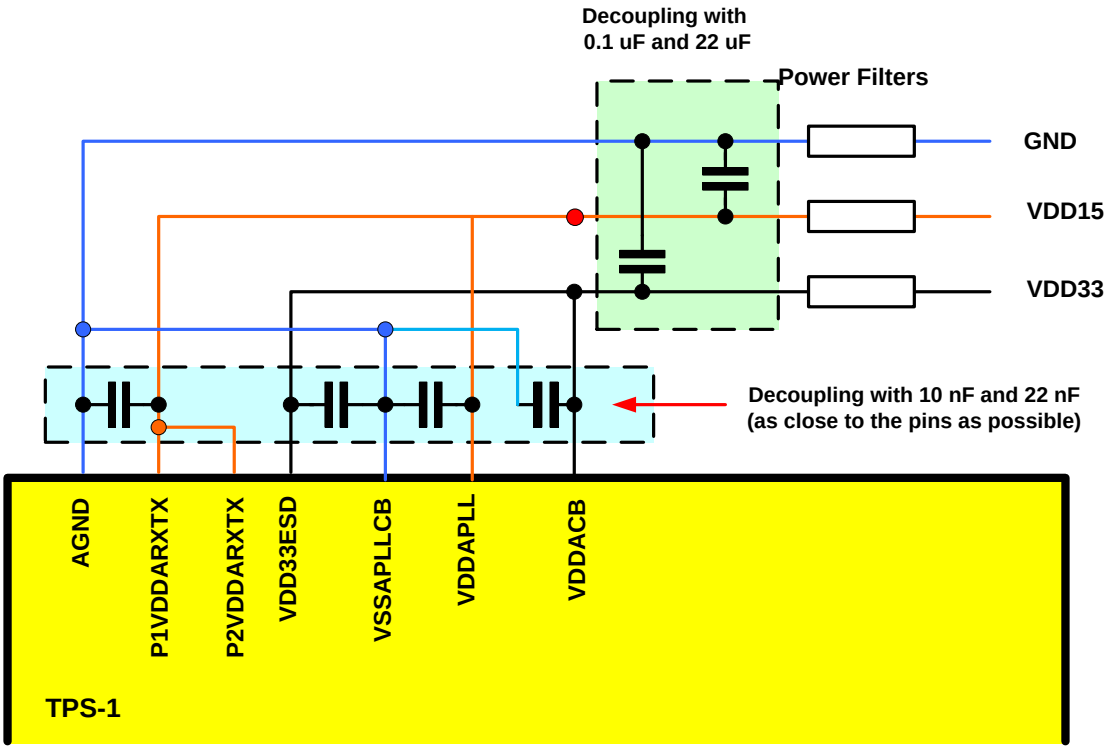

Figure B-4: Decoupling capacitors for supply voltage

Additional pairs of 0.1 µF and 22 µF capacitors should be applied to VDD33ESD and P(2:1)VDDARXTX.

Figure B-5 illustrates the power supply pins and their recommended connection. Digital supply and digital ground is not shown.

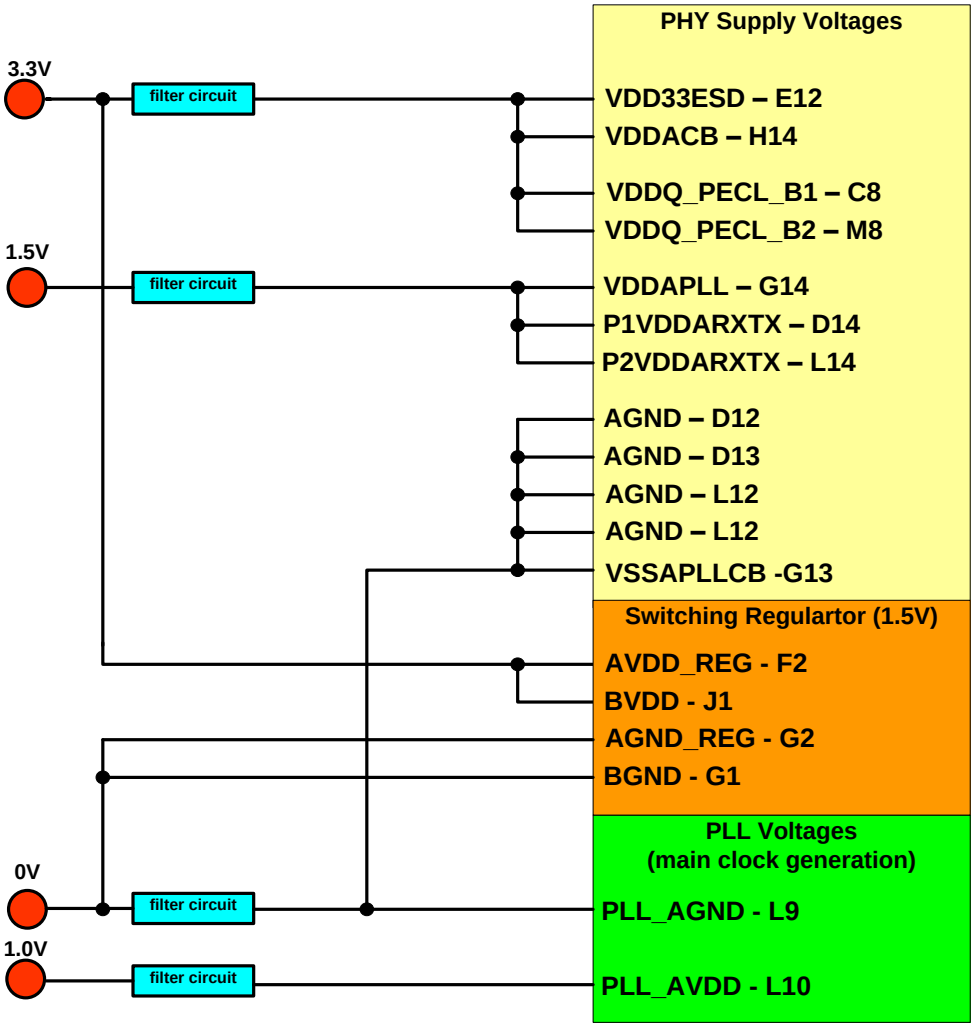

Figure B-5: Voltage Supply Concept

B.3.2 100BASE-TX Mode Circuitry

The analog input and output signals are very noise-sensitive and the PCB layout of these signals should be done very carefully. Transmit and receive lines must be routed with differential 100 Ω impedance and the trace length must be kept as short as possible.

The EXTRES input must be connected to analog GND with a 12.4 kΩ resistor (1% tolerance). See "Additional TPS-1 Pins".

The figure below shows a typical circuit example for a 100BASE-TX operation mode.

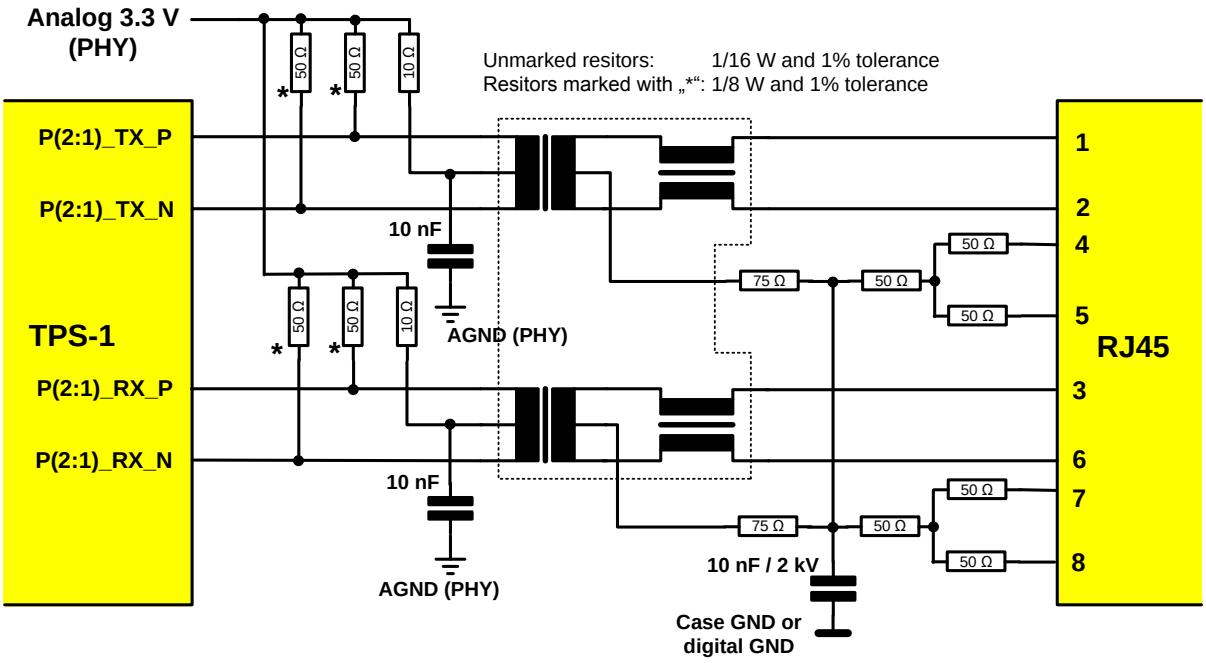

Figure B-6: 100BASE-TX Interface circuit Example

B.3.3 Unused 100Base-TX Interface

In applications that do not use the **100BASE-TX** mode, but only the **100BASE-FX** mode, the analog I/Os should be left open. Only **EXTRES** must still be connected with the 12.4 kΩ resistor to analog GND.

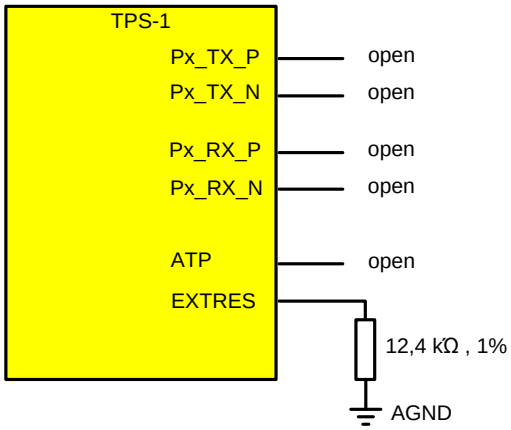

Figure B-7: Unused 100BASE-TX Interface

B.3.4 100BASE-FX Mode Circuitry

In case of 100BASE-FX operation, a PN-IO compliant optical transceiver module like **Avago AFBR-5978Z** or **QFBR-5978Z** is connected to the FX interface. The signals between the PHY and the transceiver module are 100 Ω differential respectively 50 Ω single-ended signals.

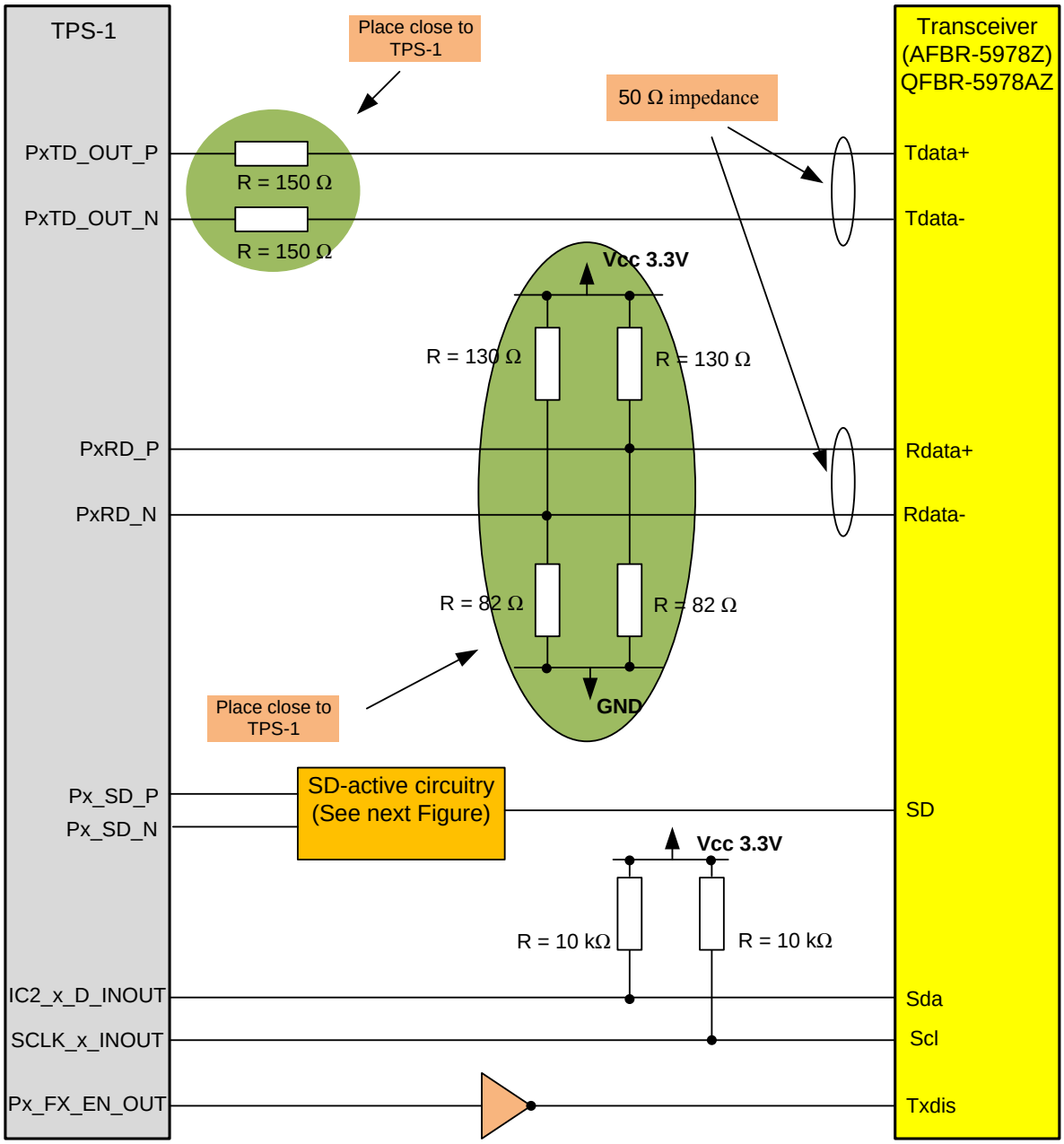

Figure B-8: 100BASE-FX Interface Example

Note: All resistors in this example should have a tolerance of 1%.

The circuitry for the connection of the SD-Pin of the transceiver to the SD_P/SD_N Pin of the TPS-1 is shown in Figure B-9. The active circuitry is necessary because the QFBR/AFBR transceiver provides no differential signal.

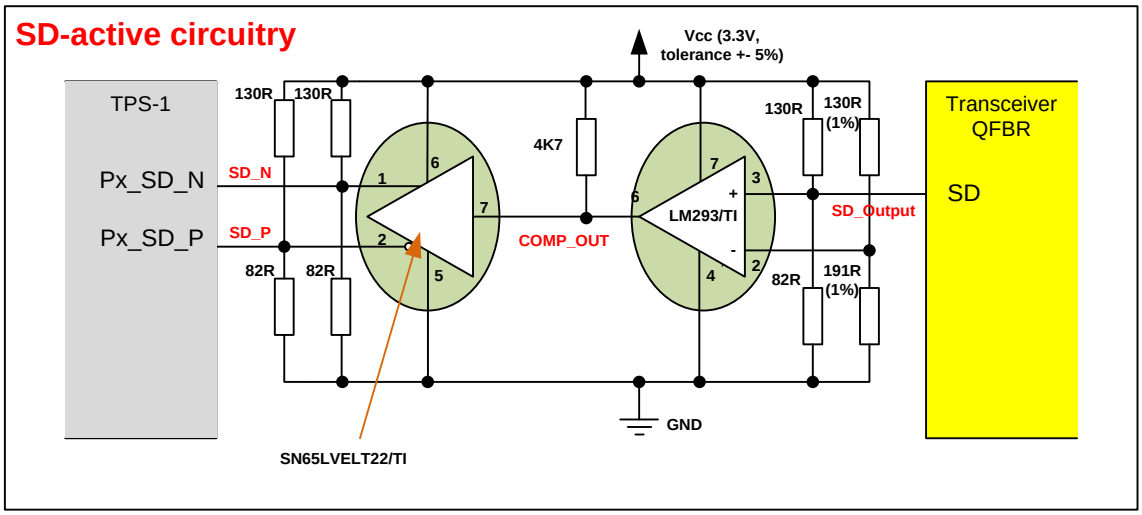

Figure B-9: Circuitry for the SD Signal

Table B-3: SD Signal for Transceiver

	SD_Output	COMP_OUT	SD_N	SD_P
No Link	0	0	1	0
Link	1	1	0	1

Using the AVAGO QFBR-5978Z or AFBR-5978Z Transceiver you must ensure the tolerance of the Supply Voltage (3.3V) between +- 5%.
Note: All resistors in this example should have a tolerance of 5% (see the exceptions).

If you want to use the FO diagnostic features, you can implement the AVAGO QFBR-5978AZ transceiver. For using the special features of this transceiver you must connect the TPS-1 to the transceiver by an I2C-bus.
Receive and transmit lines are compliant to the LVPECL technology. These lines must be routed carefully to avoid influence from e.g. the I^2C buses.
The power supply for the AVAGO transceiver is divided into the transmitter and receiver part. You need additional electronic components to reduce noise. It is important to take care in the layout of the device board to achieve optimum performance from the transceiver. It is recommended to add a filter to the power supply for the transmitter and receiver part.

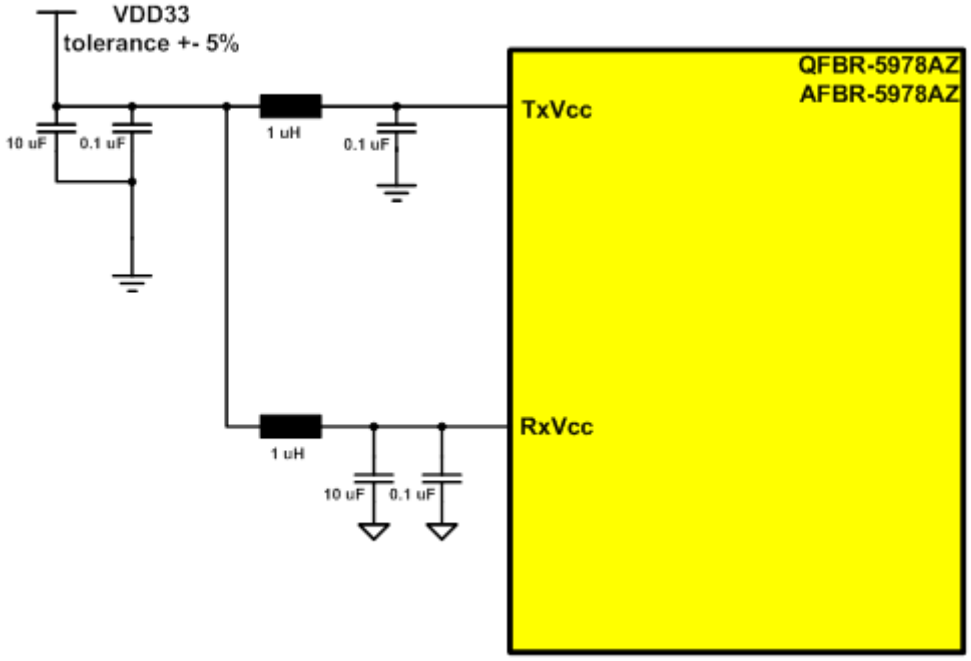

Figure B-10: Power Supply for AVAGO Transceiver

It is further recommended that a contiguous ground plane is provided in the device board directly under the transceiver to provide a low inductance ground for signal return current. The ground plane for the receiver and transmitter should also be divided and connected with a filter.
During the operation of the transceiver peaks on the supply voltage can occur so it is useful to add additional capacitors (see also the data sheet of the transceiver).

B.3.5 Unused 100Base-FX interface

Figure B-11 shows the wiring of an unused „Fiber Optic Transceiver". The interface uses PECL lines.
If a 100Base-FX interface is not used, the pins **Px_TD_OUT_P** and **Px_TD_OUT_N** can remain open (no Pull-Up or Pull-Down resistor necessary).
All other signals should be connected to GND level.

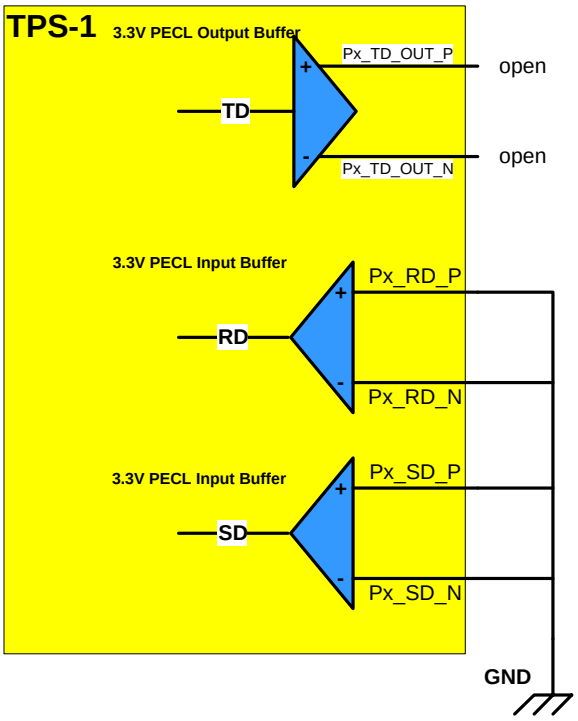

Figure B-11: Unused pins at 100Base-FX interface

Appendix.C Fast Start Up Requirements

Prioritized startup refers to the PROFINET function for accelerating the startup of IO devices in a PROFINET IO system with RT and IRT communication. It shortens the time that the respective configured IO device requires in order to reach the cyclic user data exchange.
The property prioritized startup demanded a startup time less than 500 ms.
If you want to realize this feature be aware that the complete device (TPS-1 and you own Application) must come up to this time requirement.
The function Autonegotiation is disabled and the system operates with a fixed transmission rate. To avoid the usage of crossover cables the Port 2 must get a crossover of the TX and RX lines

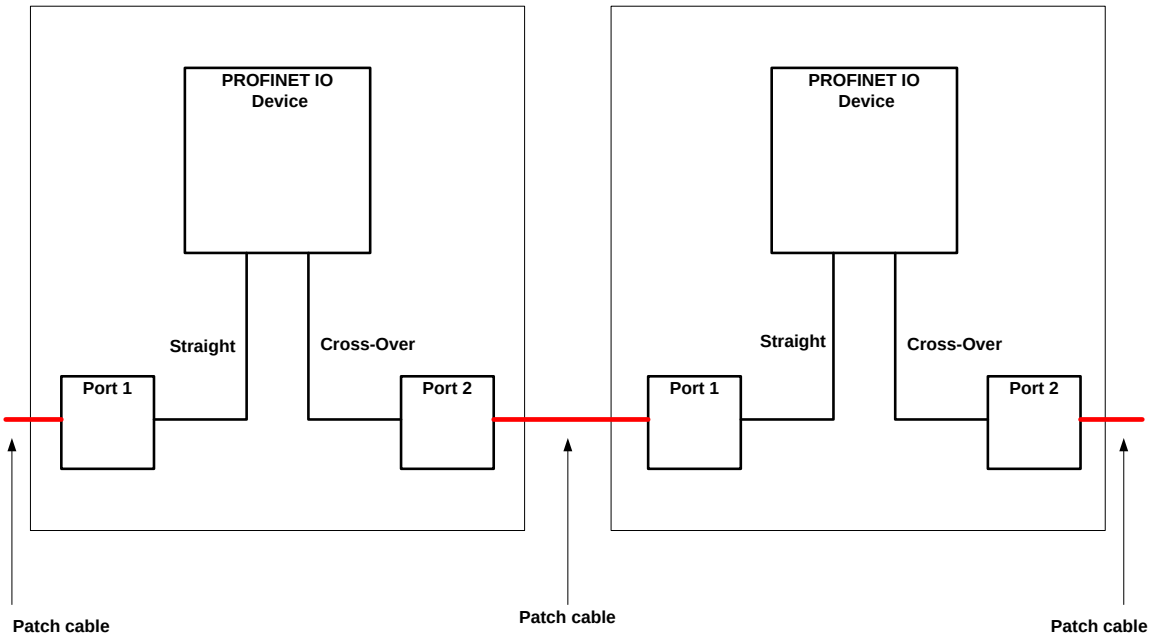

Figure C-1: Line Structure with crossover on board

The reset time of a device is very important for calculating the Start Up time. It is necessary to keep the reset time short.

REVISION HISTORY	TPS-1 User's Manual: Hardware

Rev.	Date	Description	
		Page	Summary
1.00	Sep 20, 2012	—	First Edition issued
1.01	Dec 12, 2012	8	1.1 Features added regarding TPS-1 Stack version 1.1
		19	3.1.3 Connection example for a 8bit data bus added.
		20	3.1.4 Connection example for a 16bit data bus, Figure 3-4 changed.
		34-37	4.4 Interrupt Communication with the TPS-1 added.
		40	5.2 add note 1 and 2 loading firmware to an empty Flash recommendation.
		71-73	B.3.4 100BASE-FX Mode Circuitry changed
		75	C Fast Start Up Requirements added
1.02	Jan 25, 2013	17-18	3.1.2 Signal description of the parallel interface corrected, Figure 3-1. Figure 3-2. corrected.
		40	5.2 Note1 changed.
		75	C Figure C-1. correct spelling errors
1.03	Jul 17, 2014	all	Changed - new printouts of the "TPS Configurator"
		all	Changed - Name PROFINET IO changed to PROFINET
		11-13	Chapter 2. , Table 2-1 : changed
		14	Chapter 2. , Table 2-2 : changed
		18	Chapter 3.3. , Table 3-3 : changed - LBU_BE(x)_IN in
		27	Chapter 3.2.2.1. , figure 3-9 : changed - HOST_SCLK_IN
		29	Chapter 3.2.2.2.2 : added - the equitation for calculating the wait- and latency-time for the TPS-1 SPI Wait Mode
		31	Chapter 4. , Figure 4-1 : changed
		43	Chapter 5.2.2. : added - Flash types
		55	Chapter 11. : changed
		68,69	Appendix.B.2.1. and B.2.2. : added - alternative description to avoid a tantalum capacitor.
1.04	Jul 13, 2015	16	Added chapter 3.1 Testing DPRAM Interface (additional information for testing the memory interface.
		75	Table B-3 added (FX interface)

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