Xylon d.o.o.

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Features

- Supports Xilinx® Zynq®-7000 All Programmable SoC, 7 Series and newer Xilinx FPGA families
- Older Xilinx FPGAs supported by previous IP core versions
- Supports perspective transformations of 2D quadrilaterals
- Programmable homographic transformation matrix enables:
  - cropping
  - resizing
  - rotating
  - translating
  - arbitrary combination of above operations
- Supports arbitrary transformation functions defined by MLUTs (Memory Look Up Table)
- Supports correction of fish eye lens distortions
- Suitable for extreme wide-angle lenses (fish-eye) with Field Of View (FOV) >180º
- High performance, i.e. up to 94 Mpix/s in 100 MHz operating systems
- Supports up to 2048x2048 input and output resolutions; 30 fps and higher frame rates
- Configurable number of video inputs (cameras) and video outputs
- Video De-interlacing
- Supports square and non-square pixels (pixel aspect ratio) at the video input

Core Facts

Provided with Core	
Documentation	User's Manual
Design File Formats	Encrypted VHDL
Constraints Files	Reference designs constraint files
Reference Designs & Application Notes	Xilinx Vivado® IP Integrator reference design
Additional Items	- Reference design for Xilinx ZC706 Evaluation Kit - standalone and Linux SW drivers and libraries

Simulation Tool Used
Mentor Graphics' Modelsim

Support
Support provided by Xylon

Table 1: Example Implementation Statistics for Xilinx® FPGAs

Family (Device)	Fmax (MHz)		LCs	Slices[1] (FFs/ LUTs)	IOB[2]	CMT	BRAM	MULT/ DSP48/E	DCM / CMT	GTx	Design Tools
	mclk	rclk									
Artix®-7 (XC7A35T-2)	140	150	15244	2382 (7979/5138)	0	0	17	27	0	0	Vivado 2014.4
Kintex®-7 (XC7K70T-3)	200	200	15257	2384 (7979/5136)	0	0	17	27	0	0	Vivado 2014.4
ZYNQ®-7000 (XC7Z010-2)	140	150	13715	2143 (7979/5136)	0	0	17	27	0	0	Vivado 2014.4

1) Assuming the Automotive Surround View Driver Assistance (DA) system's configuration: 4 input cameras, 4 output images, 32-bit AXI-Lite register interface, 64-bit AXI memory interface, lens correction and perspective transformation, YUV color space
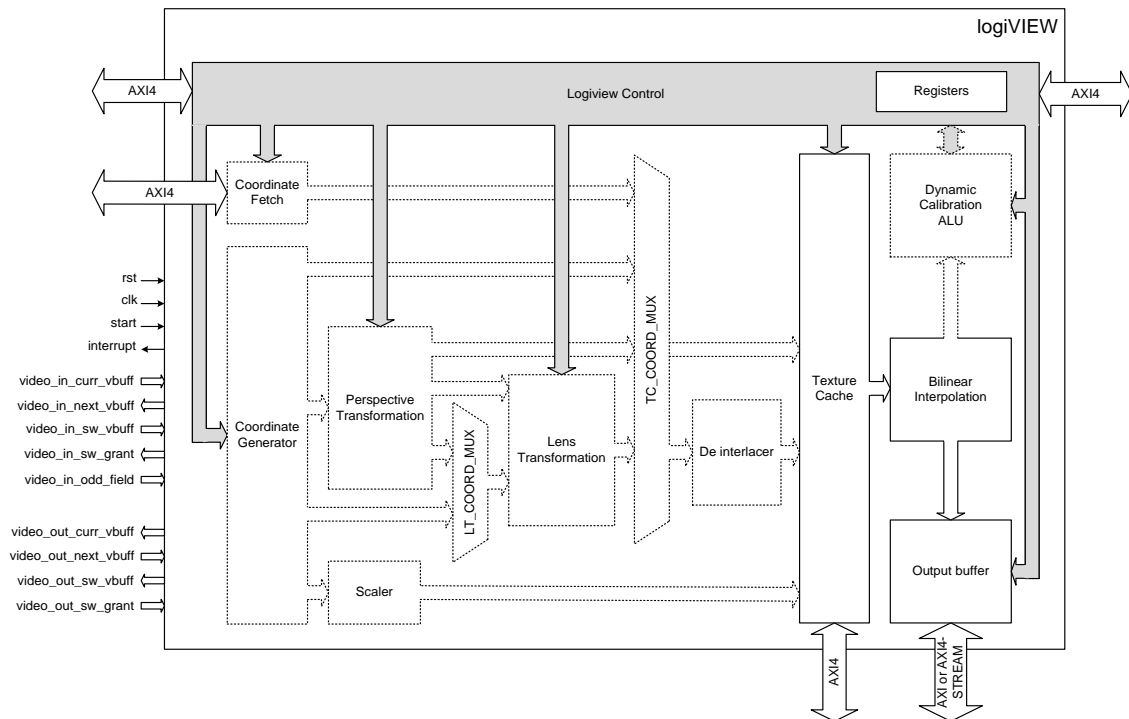2) Assuming register and memory interfaces are connected internally

Figure 1: logiVIEW Architecture

Features (cont)

- Supports native non-swizzled video inputs and swizzled (Xylon proprietary) for the highest efficiency
- Optional scaling-only module that reduces required programmable resources
- Supports line rendering (default is tile rendering) with AXI4-Stream output
- Supports input/output color spaces: RGB/RGB and YCbCr(4:2:2)/YCbCr(4:2:2)
- Double/triple buffering of video inputs and triple buffering of video outputs prevent video flickering
- Simple programming of control registers through ARM® AMBA® AXI4-Lite interface
- Configurable video memory interface type: AMBA AXI4 or AMBA AXI4-Stream
- Prepared for Xilinx Vivado® Design Suite implementation tool
- Older IP core's versions available in the Xilinx ISE® (Platform Studio) compatible format
- Parametrical VHDL design that allows tuning of features set and consumption of FPGA resources
- Simple Plug'n'Play other Xylon logicBRICKS IP cores, such as:

  - logiWIN Versatile Video Input
  - logiCVC-ML Compact Multilayer Video Controller
  - logiBITBLT Bit Block Transfer 2D Graphics Accelerator
  - logiISP Image Signal Processing (ISP) Pipeline

Applications

- Automotive Driver Assistance Systems: Surround View, Pedestrian Detection, Lane Departure Warning, Rear-View Camera, Heads-Up display (HUD)…
- Industrial systems: Surveillance Systems like Multi-Head 360° Panoramic Wide Camera with no blind spots, Industrial Pipe Inspection equipment, Test equipment…
- Medical Endoscopy and similar equipment
- Defense equipment, etc.

General Description

The logiVIEW Perspective Transformation and Lens Correction Image Processor is Xylon's logicBRICKS IP core optimized for Xilinx Zynq-7000 All Programmable SoC and FPGAs and designed to real-time process multiple still images or video streams. The logiVIEW IP core removes fish eye distortions caused by extreme wide-angle Field Of View (FOV) lenses, makes perspective corrections and other homographic transformations to the captured video, and executes arbitrary non-homographic transformation functions defined by MLUTs (Memory Look-up Table). The multiple corrected (processed) video or still image outputs can be stitched in a resulting single image by complementary logicBRICKS IP core – the logiCVC-ML Compact Multilayer Video Controller display controller IP core.
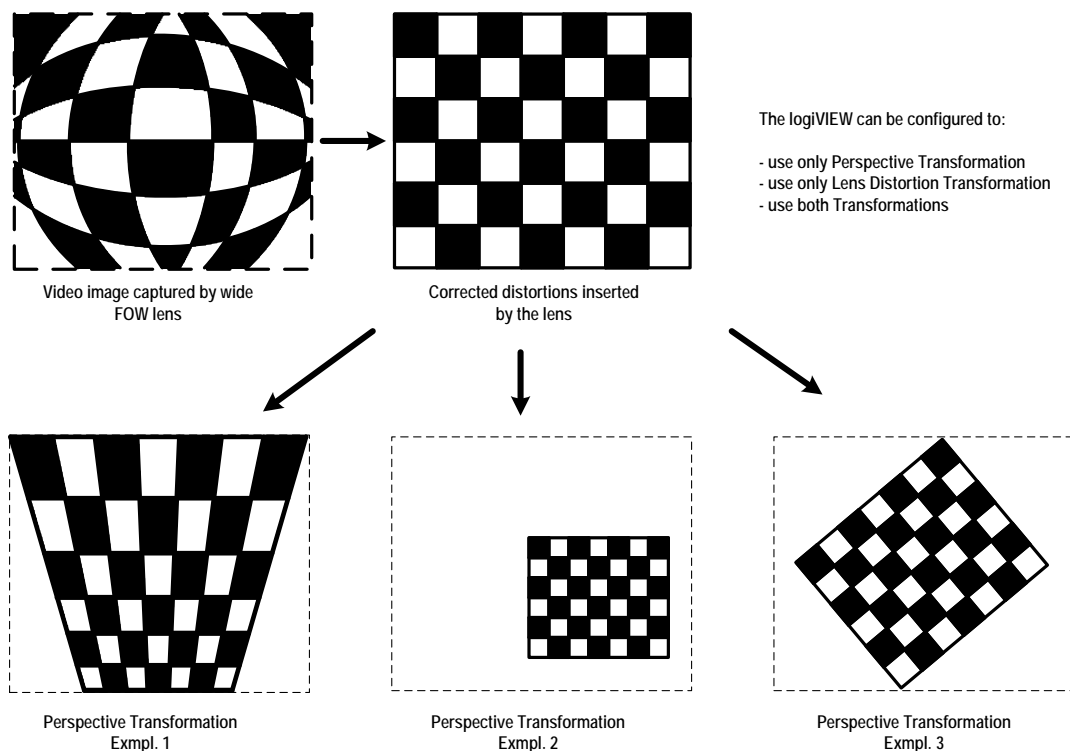
The logiVIEW can be configured to:

- use only Perspective Transformation
- use only Lens Distortion Transformation
- use both Transformations

Video image captured by wide FOW lens

Corrected distortions inserted by the lens

Perspective Transformation Exmpl. 1

Perspective Transformation Exmpl. 2

Perspective Transformation Exmpl. 3

Figure 2: logiVIEW Processing Flow with Lens Correction and Homographic Transformation Examples

The logiVIEW can be used in automotive Driver Assistance (DA) applications, such as the Four-Camera System for Surround View DA (Figure 4, 5 and 6), Heads-Up Displays (HUD), Lane Departure Warning, Rear-View (Back-Up) and others. Due to its high versatility and configurability, it can be also used in other single or multi-camera applications, such as medical endoscopy, surveillance systems (Panoramic 360° View camera - Figure 7), defense equipment, etc.

The image compensation for fish eye distortions inserted by wide-angle FOV lenses rectilinearly projects the camera captured images on the flat 2D surface suited for the LCD display. Perspective transformations calculated by a programmable homographic transformation matrix enable scaling, rotation, cropping, translation, as well as simultaneous combinations of all of these transformations. The Figure 2 shows several example outputs.

Additionally, the logiVIEW IP core can be configured to use an optional Memory Look-Up Table (MLUT) block at each video output. The MLUT can be programmed with an arbitrary transformation function to execute different transformations on input video picture's parts, for example gradual compensation of fisheye lens distortions at picture's edges and a full removal of all distortions in the picture's center (Figure 3). The MLUT transformations are key logiVIEW IP core's features for 3D Surround View applications (Figure 5 and 6).
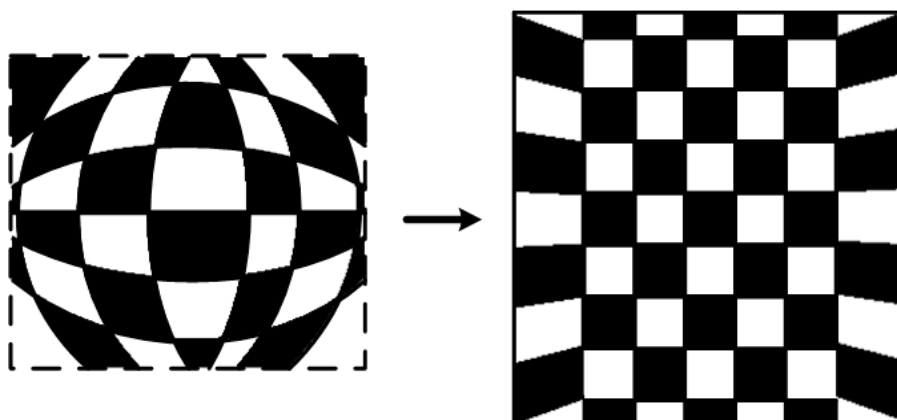
Figure 3: Example MLUT Transformation

The logiVIEW is a highly configurable IP core and can be used within Xilinx Vivado and ISE Design Suits. Xilinx implementation tools enable easy tuning of the logiVIEW's consumption of programmable logic resources and the features set setup through an easy-to-use GUI interface. Table 2 shows configuration parameters that can be setup prior to the core's synthesis time. IP configurations which utilize only the perspective, only the lens transformation, or only MLUT transformation are good examples of balancing between the required features set and used programmable logic resources.

The logiVIEW can handle an arbitrary number of video inputs and video outputs as long as the system architecture allows it. The available memory bandwidth, frame rates of input video cameras, and other system parameters determine the number of supported video inputs and outputs by a single logiVIEW IP core.

For example, the YCbCr video format requires lower memory bandwidth than the RGB video format, and the logiVIEW IP core configured to use the YCbCr can support more video channels and higher video resolutions with the same memory subsystem (SoC bus and memory controller IP core) and the memory connected to the FPGA. Video format can be setup through IP core's configuration GUI interface.

In video applications that require more processing power than offered by a single logiVIEW IP core instance, it is possible to implement parallel processing of video inputs' segments by multiple logiVIEW IP core instances and to achieve application goals.

The logiVIEW IP core uses linked list programming for maximum flexibility. Descriptor (a set of 32 words stored in memory) contains all data required to initialize logiVIEW for one output view. It has a programmable registers field accessible through the standard AMBA AXI4-Lite bus. Video memory interface can be selected to support AMBA AXI4 or AXI4-Stream bus interface.

Example logiVIEW Application - Automotive Surround View Driver Assistance

The Surround View DA provides an unmatched awareness of the situation by enabling the driver to see 360-degrees around the vehicle on the LCD instrument cluster or the Central information Display (CID). The surroundings can be seen from different perspectives, including the bird's eye view perspective typical for the first generation systems, which eliminates all blind spots during critical and precise maneuvers in crowded spaces. Xylon's Surround View solution based on the logiVIEW IP core is today used on the road in production automotive systems. The solution can be evaluated on the Xilinx Zynq-7000 AP SoC based logiADAK Automotive Driver Assistance Development Kit.
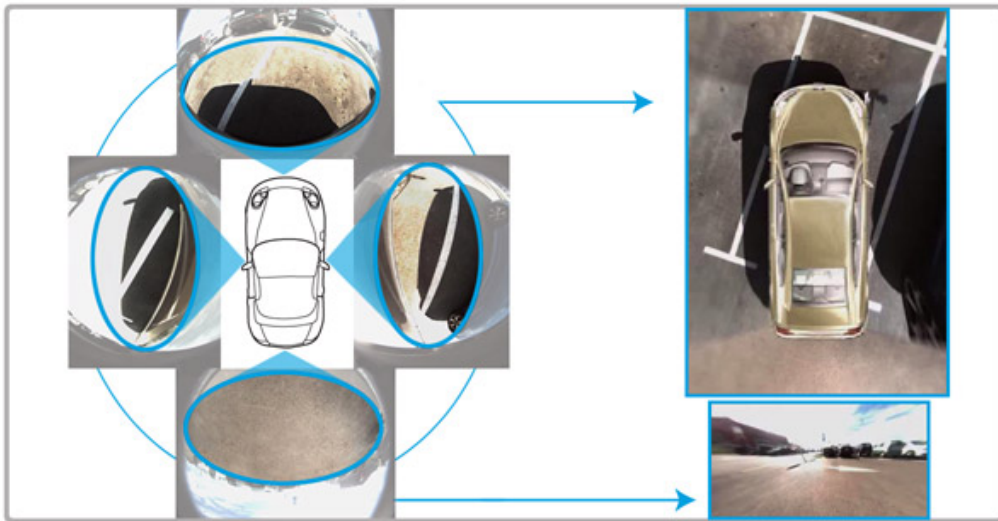
Figure 4: Xylon's Four-Camera Surround View DA Demo System – Camera Positioning and Example Video Outputs (Bird's View Perspective)

The Surround View DA system uses at least 4 cameras, furnished by extreme wide-angle fish eye lenses, which cover separated zones around the vehicle. The logiVIEW must remove the lens distortions, correct perspectives to four high-resolution input video streams, and stitch the corrected video images in a single display of vehicle's surroundings.
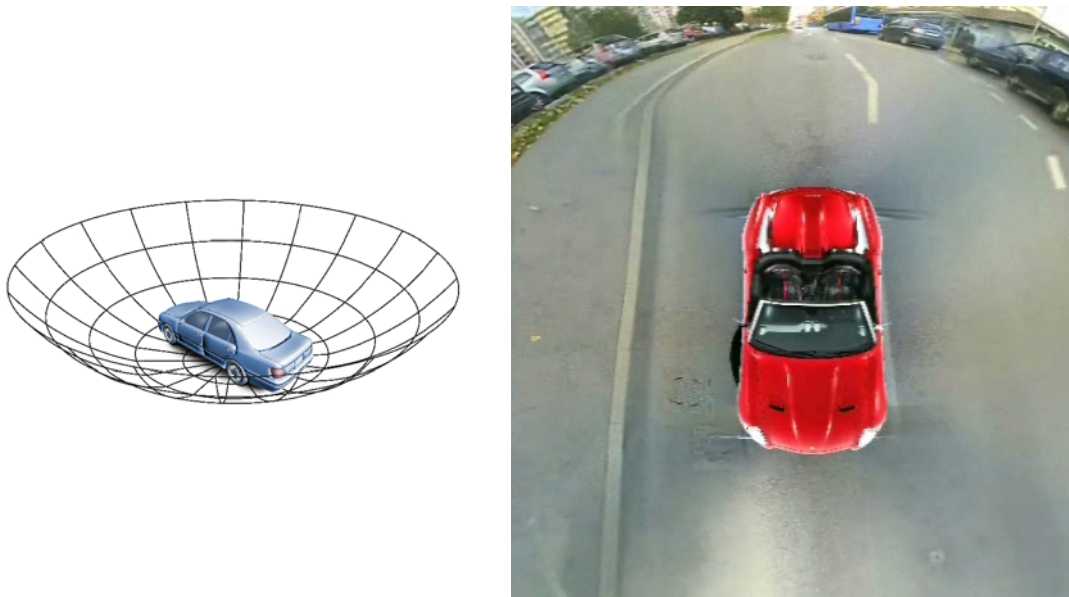

Figure 5: Xylon's Four-Camera Surround View DA Demo System – 3D View generated by logiVIEW MLUTs

Configurable logiVIEW MLUTs enable development of new generation Surround View automotive systems with the 3D visualization of vehicle's surrounding. The 3D visualization is achieved by projecting captured camera video images on the bowl-shaped ground surface – Figure 5. This type of visualization is more natural and easier to use. While bird's eye surround view systems have the POV (Point of View) defined orthogonally above the vehicle, new systems with the bowl-view capability can show vehicle's surroundings from different POVs.
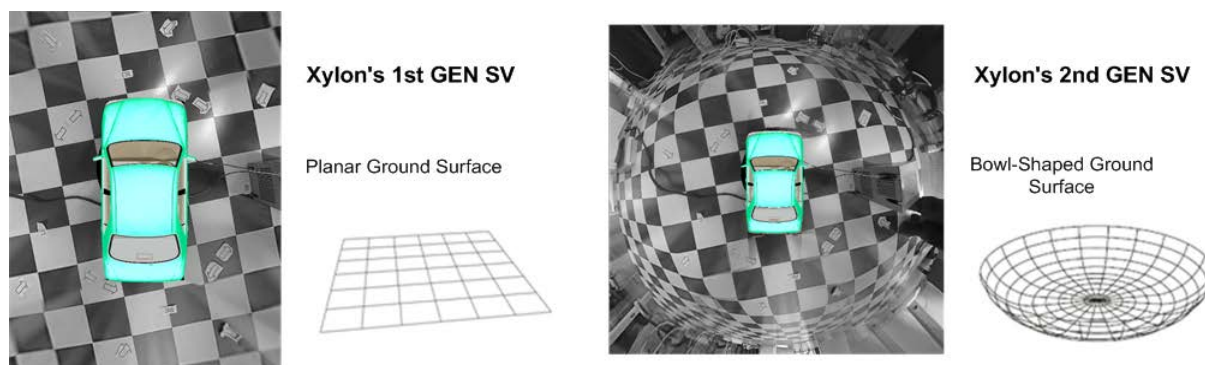
Figure 6: The difference between the 1ˢᵗ and the 2ⁿᵈ generation of Surround View ADAS

To learn more about Xylon's Surround View ADAS, please visit:
http://www.logicbricks.com/Solutions/Xylon-ADAS-Development-Kit.aspx

Example logiVIEW Application – Multi-Head 360° Video Camera for Surveillance Applications

Video surveillance multi-head camera with no blind spots that shows 360° view (Panoramic View) of the surroundings can be also based on the logiVIEW IP core. Xylon's demo setup uses 3x 1MP (Mega Pixel) imagers with wide angle lenses and Xylon logiCRAFT-CC development board based on Xilinx Spartan®-6 FPGA to fully process captured video streams in real time. Xylon logicBRICKS IP cores remove lens distortions (fish-eye), make perspective corrections and seamless stitching of three video streams with no dividing "borders", and finally display the resulting panoramic 2D video image.
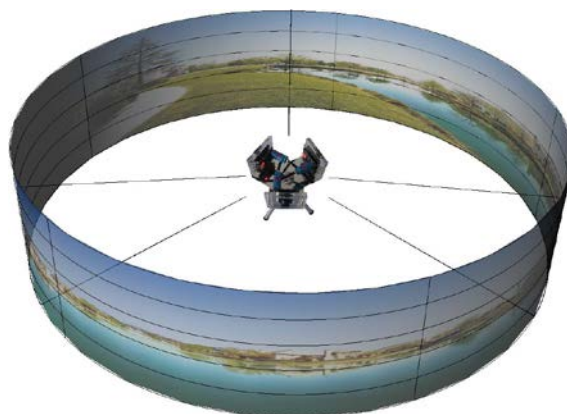

Figure 7: The difference between the Bird's View perspective and the Bowl View

The demo can be upgraded to support much higher video camera resolutions. To learn more about Xylon's Multi-Head Panoramic Camera, please visit:
http://www.logicbricks.com/Markets/Industrial/Video-Surveillance-Multi-Head-360-Panoramic-View-Camera.aspx

Example logiVIEW Application – Real-time Low Latency Video Rotation

Medical endoscopes, pipe inspection tools or various advanced defense systems are application examples that require real-time video rotation for an arbitrary angle, which can be dynamically changed in sub-degree steps, and very small video output latency.

To learn more about the video rotation by the logiVIEW IP core and to see Xylon demo in operation, please visit:
http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Low-Latency-Video-Rotation-for-Xilinx-SoC-FPGA.aspx

Functional Description

The Figure 1 presents the logiVIEW block diagram. The main logiVIEW functional blocks are: Perspective Transformation, Lens Transformation, Texture Cache, and logiVIEW Control.

Perspective Transformation

The Perspective Transformation calculates the desired perspective transformation defined by the programmable homographic matrix. Output coordinates from the Perspective Transformation can be supplied either to the Lens Transformation block or directly to the Texture Cache block if the Lens Transformation is not required.

Lens Transformation

The Lens Transformation can be used with the Perspective Transformation or without it. The generated output pixel coordinates match the calibrated lens parameters.

Scaler

The Scaler module calculates texture coordinates for input image scaling. Vertical and horizontal scaling factors can be programmed independently. This module can be used to save FPGA resources when scaling is the only required transformation type. The logiVIEW IP core configured with the Scaler module does not support lens and perspective transformations.

De-interlacer

The De-interlacer module generates coordinates for progressive rendering of the interlaced video. It uses video_in_odd_flag input signal to compensate image flickering between even and odd lines.

Texture Cache

The Texture Cache block uses texture coordinates from the Lens Transformation, Perspective Transformation, Coordinate Fetch (MLUT) or Coordinate Generator (no transformation) to retrieve pixels from the original (input) image stored in memory. Besides the pixel defined by input coordinates, the Texture Cache block retrieves the nearest neighboring pixels and uses caching for efficient memory bandwidth usage.

logiVIEW Control

The logiVIEW Control module fetches linked list elements from the memory and uses them to program all other logiVIEW modules. The programming is executed in defined timing intervals. Access to the memory is provided by the means of the 64-bit XMB or AXI4 bus.

Core Modifications

The logiVIEW IP core is supplied in an encrypted VHDL format compatible with the Xilinx Vivado IP Integrator tool. Older logiVIEW versions are available in the Xilinx ISE Platform Studio compatible format. Different logiVIEW configuration parameters are selectable prior to VHDL synthesis, and the following table presents a selection from a list of the available configuration parameters:

Table 2: logiVIEW VHDL configuration parameters

Parameter	Description
C_USE_PT	Use the Perspective Transformation block
C_USE_LT	Use the Lens Transformation block
C_USE_MLUT	Use the Memory Look-up Table block
C_USE_DCA	Use the Dynamic calibration block
C_USE_LT_COORD_MUX	Use Lens Transformation multiplexer: enables switching the source for input coordinates between Coordinate Generator and Perspective Transformation

Parameter	Description
	block.
C_USE_TC_COORD_MUX	Use Perspective Transformation multiplexer: enables switching the source for input coordinates between Coordinate Generator, Coordinate Fetch, Perspective Transformation or Lens transformation block.
C_USE_IN_BUFF	Enables input image's buffering to prevent video flickering.
C_USE_OUT_BUFF	Enables output image's buffering to prevent video flickering.
C_USE_YUV_4_2_2	Use YCbCr (4:2:2) format (RGB is default)
C_CAMERA_NUM	Number of input cameras

The logiVIEW is designed with regard to adaptability to various SoC designs. However, there may be instances where source code modification is necessary. Therefore, if you wish to reach the optimal use of the logiVIEW core in your specific implementation, or to supplement some of your specific functions, you can allow us to tailor the logiVIEW to your requirements.

Core I/O Signals

The core signals I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signals I/O are provided in Table 3.

Table 3: Core I/O Signals

Signal	Signal Direction	Description
Global Signals		
RST	Input	Global synchronous set/reset
CLK	Input	Memory clock
Memory Interface		
AXI4 Interface	Bus	Refer to AMBA AXI4specifications
Video Interface		
AXI-Stream Interface	Bus	Refer to AMBA AXI version 4 specification from ARM
Register Interface		
AXI4-Lite Interface	Bus	Refer to AMBA AXI4-Litespecifications
Auxiliary Signals		
HW_TRIGG	Input	Hardware trigger signal for start of processing, edge sensitive, active high
INTERRUPT	Out	Interrupt signal, level sensitive, active high
VIDEO_IN_CURR_VBUFF	Input	Video input double/triple buffering: Current video memory buffer
VIDEO_IN_NEXT_VBUFF	Out	Video input double/triple buffering: Next video memory buffer to write to
VIDEO_IN_SW_VBUFF	Input	Video input double/triple buffering: Request for buffer switching
VIDEO_IN_SW_GRANT	Out	Video input double/triple buffering: Buffer switching granted
VIDEO_IN_ODD_FIELD	Input	Video input odd field, for de-interlacing
VIDEO_OUT_CURR_VBUFF	Out	Video output double/triple buffering: Current video memory buffer
VIDEO_OUT_NEXT_VBUFF	Input	Video output double/triple buffering: Next video memory buffer to write to
VIDEO_OUT_SW_VBUFF	Out	Video output double/triple buffering: Request for buffer switching
VIDEO_OUT_SW_GRANT	Input	Video output double/triple buffering: Buffer switching granted

Verification Methods

The logiVIEW is fully supported by Xilinx Vivado IP Integrator and ISE Platform Studio integrated software solution. This tight integration tremendously shortens IP integration and verification. A full logiVIEW implementation does not require any particular skills beyond general Xilinx tools knowledge.

Recommended Design Experience

The user should have experience in the following areas:

- Xilinx design tools
- ModelSim

Available Support Products

logiREF-logiVIEW-ZC706 reference design showcases major logiVIEW IP features on Xilinx ZC706 Evaluation kit. The demo is simple to use and works on a still test image stored on the SD card. Demo users can program arbitrary test images, i.e. image captured from the proprietary video camera. Demonstrated features include: homographic perspective transformation, MLUT transformation, lens correction and lens correction with perspective transformation.

This demo is available on request only:

    Email: info@logicbricks.com

logiREF-VROT-FMC is a free and downloadable logicBRICKS reference design that showcases a real-time video rotation for an arbitrary angle, which can be dynamically changed in sub-degree steps. The video rotation works with a video output latency that can be as low as one frame time. Designed by standard off-the-shelf evaluation logicBRICKS IP cores, the demo SoC also demonstrates video frame grabbing, frame rate conversion, and display overlay with graphics touch screen HMI controls.

To learn more about and to download the logiREF-VROT-FMC reference design, visit the web:

    Email: support@logicbricks.com
    URL: http://www.logicbricks.com/logicBRICKS/Reference-logicBRICKS-Design/Low-Latency-Video-Rotation-for-Xilinx-SoC-FPGA.aspx

The logiADAK is a great programmable platform for upcoming automotive driver assistance applications that require intensive real-time video processing, parallel execution of multiple advanced algorithms and versatile interfacing with sensors and vehicle's communication backbones. The abundant performance and reprogrammability of the Zynq-7000 device enables ADAS designers to design SoCs that outperform competing solutions and achieve a new level of system differentiation through a combination of hardware-accelerated video inputs from multiple camera inputs and the ability to quickly adapt to ever changing sensor setups and interfacing.

To learn more about the logiADAK Automotive Driver Assistance Kit contact Xylon or visit the web:

    Email: support@logicbricks.com
    URL: www.logicbricks.com/Products/logiADAK.aspx

Ordering Information

This product is available directly from Xylon under the terms of the Xylon's IP License. Please contact Xylon for pricing and additional information:

Email:　　sales@logicbricks.com
URL:　　　www.logicbricks.com/Products/logiVIEW.aspx

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Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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Phone:　　+1 408-559-7778
Fax:　　　+1 408-559-7114
URL:　　　www.xilinx.com

Revision History

Version	Date	Note
2.00.	04.06.2010.	Preliminary Xylon release – new doc template
2.00.e	03.03.2011.	Changed data in the Table 2. Added description of new MLUT feature and YCrCB/RGB converter.
2.00.f	01.04.2011	The first public version. Added short Calibration Software description.
3.05	19.11.2012.	Support for bowl-shaped surface projections (3D visualization), dynamic stitching, new calibration software, and the second generation logiVIEW-SVK, updated resources
3.10	18.03.2015.	Initial Vivado version of IP core. Support for non-swizzled texture, non-square pixel size.
3.11	27.05.2015.	Pixel color calculation improved for YUV 4:2:2, added buffer registers and busy flag.