PC104-DAS16Jr/12 & PC104-DAS16Jr/16

User's Manual

MEASUREMENT
COMPUTING

Revision 4
August, 2001

HM PC104-DAS16Jr_##.lwp

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1 INSTALLATION

1.1 SOFTWARE

Before you open your computer and install the board, install and run *Insta*Cal™, the installation, calibration and test utility included with your board. *Insta*Cal™ will guide you through switch and jumper settings for your board. Detailed information regarding these settings can be found below. Refer to the *Software Installation* manual for *Insta*Cal™ installation instructions.

1.2 HARDWARE

The PC104-DAS16Jr/12 has one bank of switches, two single function switches and one jumper block which must be set before installation of the board inside your computer (Figure 1-1). The PC104-DAS16Jr/16 has one additional switch for selecting unipolar or bipolar ranges (Figure 1-2).
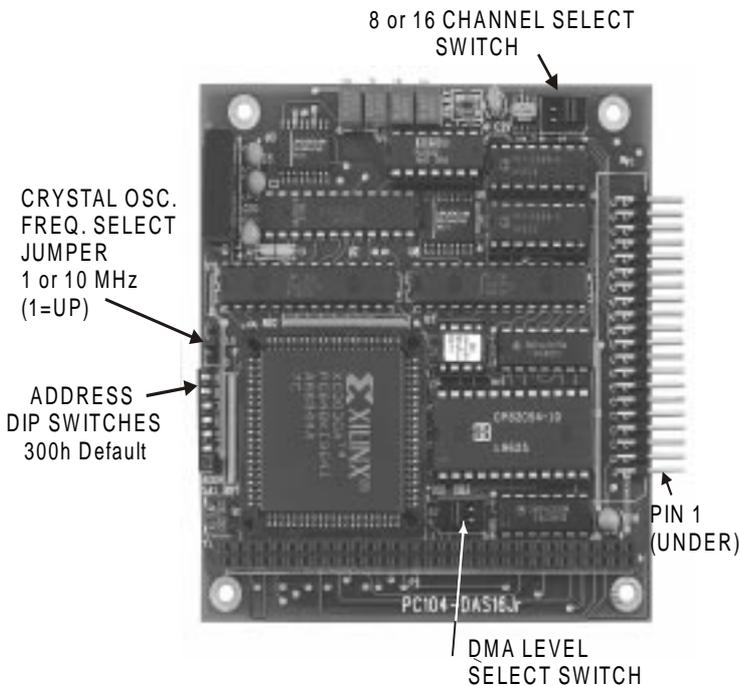
Figure 1-1. PC104-DAS16Jr/12 Switch & Jumper Locations

1

BIPOLAR or UNIPOLAR SELECT SWITCH (S3)

8 or 16 CHANNEL SELECT SWITCH (S1)

CRYSTAL OSC. FREQ. SELECT JUMPER (J1) 1 or 10 MHz (1=DOWN)

ADDRESS DIP SWITCHES 300h Default

PIN 1 (UNDER)

DMA LEVEL SELECT SWITCH (S2)
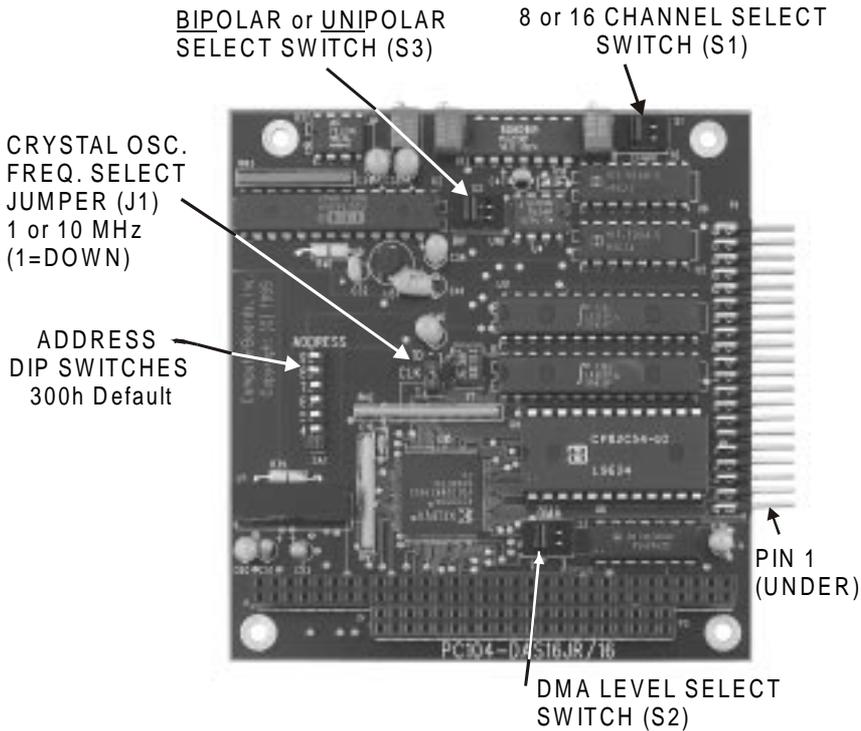
Figure 1-2. PC104-DAS16Jr/16 Switch and Jumper Locations

1.3 BASE ADDRESS

The base address switches are set at the factory to address 300h (768 decimal) as shown on Figure 1-3. Unless there is already a board in your system using this address, leave the switches as they are set at the factory.

In the example shown in Figure 1-3, the PC104-DAS16Jr/xx is set for base address 300h. See Figures 1-1 and 1-2 above for switch orientations and locations on the boards.

SW	HEX
A9	200
A8	100
A7	80
A6	40
A5	20
A4	10
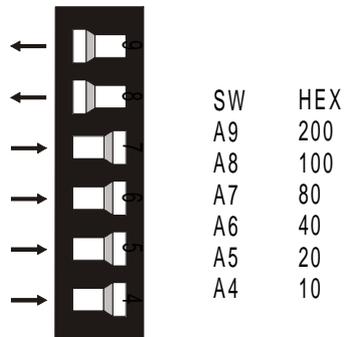
Figure 1-3. Base Address Switches

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1.4 DMA LEVEL SELECT

If using an XT PC there are only two DMA levels available and level 3 is probably used by the hard disk controller. Set the DMA level switch to the level 1 position (Figure 1-4). See Figure 1-1 or 1-2 for switch location.

If you have an AT or 386 type computer the hard disk controller is not at level 1 or 3 so either level may be used.

There are other boards that use DMA levels. Some network boards do and so do some IEEE-488 interface boards. If you have other boards in your computer with DMA level switches on them, make sure there are no conflicts
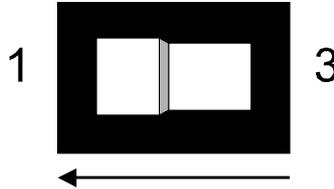
DMA LEVEL SELECT - DMA Level 1 is selected.

Figure 1-4. DMA Level Select Switch

1.5 1 OR 10 MHZ CRYSTAL OSCILLATOR JUMPER

The 1/10 (1 or 10) MHz XTAL jumper selects the frequency of the source applied to the on-board pacer. This pacer (counter 2) is used to pace the A/D start conversion trigger (Figure 1-5). See Figure 1-1 or 1-2 for jumper location.

This jumper is on the board because the original DAS-16, designed in 1984, had a 1 MHz crystal. When MetraByte redesigned the DAS-16 and added the faster 10 MHz crystal, a jumper was provided to maintain compatibility with older software.

The PC104-DAS16Jr/xx has the jumper because the DAS-16 has the jumper and some software requires the jumper to be in the 1 MHz position. However, some software requires the 10 MHz position.

The PC104-DAS16Jr/xx is shipped with the jumper in the 1 MHz position. InstaCal allows you to specify 1 or 10 MHz position in the setup. See Figure 1-1 or 1-2 for jumper location and orientation. Note the difference in orientation in Figures 1-1, 1-2, and 1-5.

CIO-DAS16JR-12   CIO-DAS16JR-16
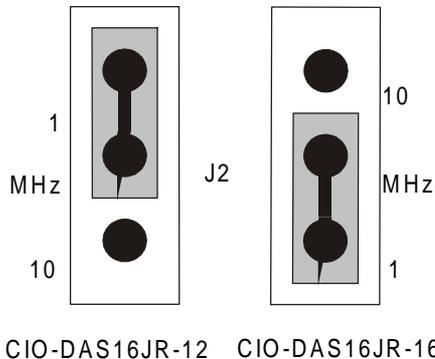
Figure 1-5. Frequency Select Jumpers

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Older software may require the 1 MHz setting for this jumper. Use the 10MHz setting for any new software development to get better resolution setting pacer frequencies.

1.6 8/16 CHANNEL SELECT

The PC104-DAS16Jr/xx can be configured for eight differential or 16 single-ended inputs. Using differential inputs allows up to 10 volts of common mode (ground loop) rejection and can be more noise immune.

8/16 CHANNEL SELECT - 8 Differential inputs selected.

The PC104-DAS16Jr/xx comes from the factory with the select switch set for 8 differential inputs as shown in Figure 1-6. Set it for the number of inputs you desire. See Figure 1-1 or 1-2 for switch location.

Figure 1-6. Channel Quantity Select Switch

1.7 INSTALLING THE BOARD

Having configured the board's switches and jumpers, it is now time to add the board to the PC104 bus in the PC.

1. Turn the power off.

2. Remove any covers, etc. so you can get access to the PC104 bus. Please be careful not to dislodge any of the cables installed on the boards in your computer.

3. Remove the retaining screws on the topmost PC104 card installed. Replace these screws with the threaded standoffs provided.

4. Push the PC104-DAS16Jr/xx board firmly down into the PC104 bus connector. Secure it in place with the screws removed in the previous step.

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2 SIGNAL CONNECTIONS

2.1 CONNECTOR DIAGRAM

The PC104-DAS16Jr/xx analog connector is a 40-pin in-line header connector (Figure 2-1). This connector accepts the C40FF-# cable which mates with the CIO-MINI40 screw terminal board.

```
        NC  40  ● ●  39  NC
        NC  38  ● ●  37  LL GND
    CH0 HI  36  ● ●  35  CH 8 HIGH\CH 0 LOW
    CH1 HI  34  ● ●  33  CH 9 HIGH\CH 1 LOW
    CH2 HI  32  ● ●  31  CH 10 HIGH\CH 2 LOW
    CH3 HI  30  ● ●  29  CH 11 HIGH\CH 3 LOW
    CH4 HI  28  ● ●  27  CH 12 HIGH\CH 4 LOW
    CH5 HI  26  ● ●  25  CH 13 HIGH\CH 5 LOW
    CH6 HI  24  ● ●  23  CH 14 HIGH\CH 6 LOW
    CH7 HI  22  ● ●  21  CH 15 HIGH\CH 7 LOW
     LLGND  20  ● ●  19  NC
     LLGND  18  ● ●  17  NC
        NC  16  ● ●  15  NC
       SSH  14  ● ●  13  DIGITAL GND
DIGITAL IN 0  12  ● ●  11  DIGITAL IN 1
DIGITAL IN 2  10  ● ●   9  DIGITAL IN 3
DIGITAL OUT 0   8  ● ●   7  DIGITAL OUT 1
DIGITAL OUT 2   6  ● ●   5  DIGITAL OUT 3
CTR 0 CLOCK   4  ● ●   3  CTR 0 OUT
  CTR 2 OUT   2  ● ●   1  +5V PC BUS
```

Figure 2-1. PC104-DAS16Jr/xx Board Connector Pinout

NOTE: On both board versions, pin 1 is the bottom (closest to the board) left-hand corner pin of the connector when the board is viewed edge - on from the connector side with the components facing up.

If compatibility with the CIO-DAS16 series connector is desired, you can convert to a compatible 37D connector using the C40-37F-# or C40-37M-# cables. If the BP40-37 Adapter Cable is used, is accessible from the rear of the PC through the expansion back plate (Figures 2-2 and 2-3). Using these adapters, the signals available are identical to the DAS-16 (with the exception of the missing D/A signals). An additional signal, SS&H OUT, can be accessed at pin 26.

LLGND 19	37 CH0 HI
CH 8 HIGH\CH 0 LOW 18	36 CH1 HI
CH 9 HIGH\CH 1 LOW 17	35 CH2 HI
CH 10 HIGH\CH 2 LOW 16	34 CH3 HI
CH 11 HIGH\CH 3 LOW 15	33 CH4 HI
CH 12 HIGH\CH 4 LOW 14	32 CH5 HI
CH 13 HIGH\CH 5 LOW 13	31 CH6 HI
CH 14 HIGH\CH 6 LOW 12	30 CH7 HI
CH 15 HIGH\CH 7 LOW 11	29 LLGND
NC 10	28 LLGND
NC 9	27 NC
NC 8	26 SSH
LLGND 7	25 DIGITAL IN 0 / TRIGGER
DIGITAL IN 1 6	24 DIGITAL IN 2
DIGITAL IN 3 5	23 DIGITAL OUT 0
DIGITAL OUT 1 4	22 DIGITAL OUT 2
DIGITAL OUT 3 3	21 CTR 0 CLOCK
CTR 0 OUT 2	20 CTR 2 OUT
+5V PC BUS 1	

Figure 2-2. BP40-37 Adapter Cable Pinout

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The BP40-37 Adapter connector accepts female 37-pin, D-type connectors, such as those on the C37FF-2, 2 foot cable with connectors (Figure 2-3). If frequent changes to signal connections or signal conditioning is required, please refer to the information on the CIO-MINI37, CIO-TERMINAL screw terminal board, CIO-EXP32, 32 channels analog MUX/AMP, CIO-SSH16, 16 channel simultaneous sample & hold board or the ISO-RACK16 5B module interface rack.
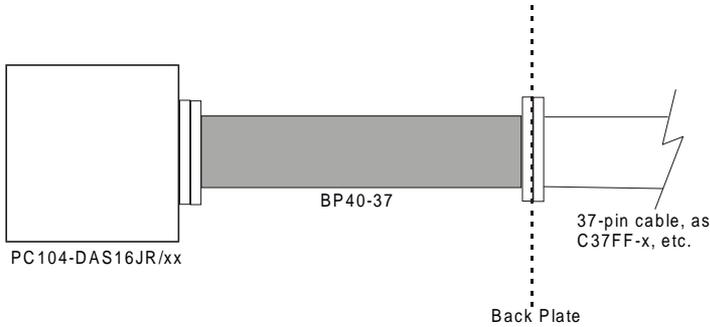
Figure 2-3. Cabling Using a BP40-37

2.2 ANALOG INPUTS

Analog inputs may be connected in three different configurations. These are Single Ended, Floating Differential and Differential.

WARNING - PLEASE READ

Measure the voltage between the ground signal at the signal source and the PC. If there is more than 10 volts, do not connect the board because you will not be able to make any reading. If the voltage is more than 30 volts, DO NOT connect to this signal because it will damage the board and possibly the computer.

2.3 SINGLE-ENDED

A single-ended input is two wires connected to the board, a channel high (CH# HIGH) and a Low Level Ground (LLGND). The LLGND signal must be the same ground the PC is on. The CH# HIGH is the voltage signal source (Figure 2-4).
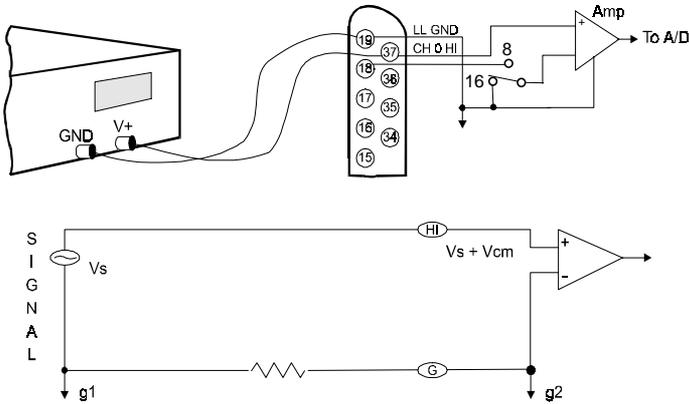
Figure 2-4. Single-Ended Input

2.4 FLOATING DIFFERENTIAL

A floating differential input is two wires from the signal source and a 10K ground reference resistor installed at the input. The two signals from the signal source are Signal High (CH# HIGH) and Signal Low (CH# LOW).

The reference resistor is connected between CH# LOW and LLGND pins.

A floating differential hookup is handy when the signal source is floating with respect to ground, such as a battery, 4-20 mA transmitter or and the lead lengths are long or subject to EMI interference (Figure 2-5).
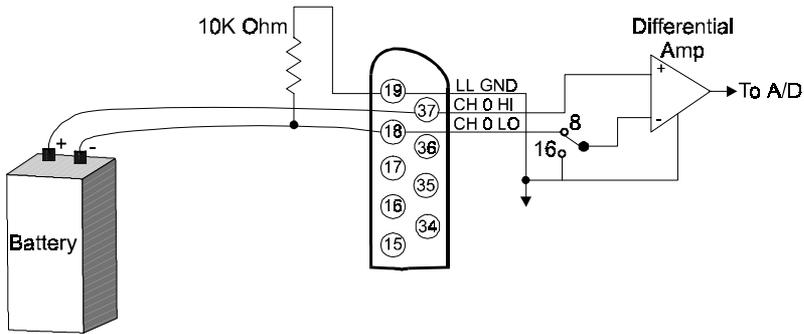
CIO-DAS16 CONNECTOR 8 CHANNEL DIFFERENTIAL

Figure 2-5. Floating Source Differential Input

The floating differential input will reject up to 10V of EMI energy on the signal wires.

WARNING

Check it with a ohmmeter to determine that the signal source really floating before risking the board and the PC!

2.5 DIFFERENTIAL INPUT

A differential signal has three wires from the signal source. The signals are Signal
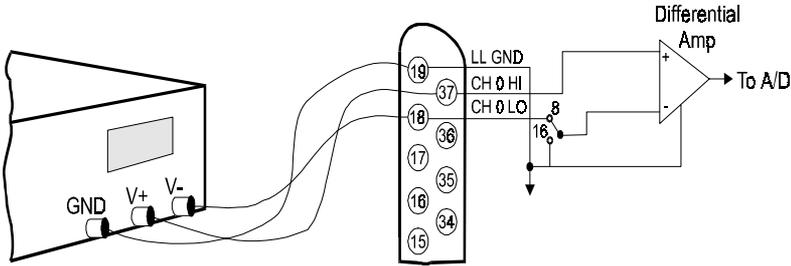
CIO-DAS16 CONNECTOR 8 CHANNEL DIFFERENTIAL

Figure 2-6. Differential Connections

High (CH# HIGH), Signal Low (CH# LOW) and Signal Ground (LLGND). See Figure 2-6.

A differential connection allows you to connect the board to a signal source with a ground that is different than the PC ground, but less than 10V difference, and still make a valid measurement of the signal between CH# HIGH and CH# LOW.

EXAMPLE:

A laboratory instrument with its own wall plug. There are sometimes differences in wall GND between outlets.

2.6 DIGITAL OUTPUTS & INPUTS

All the digital outputs inputs are TTL level. TTL is an electronics industry term, short for Transistor Transistor Logic, with describes a standard for digital signals which are either at 0V or 5V (nominal). The binary logic inside the PC is all TTL or LSTTL (Low power Schotky TTL). Both specifications are presented here.

3 REGISTER ARCHITECTURE

3.1 CONTROL & DATA REGISTERS

The PC104-DAS16Jr/xx is controlled and monitored by writing to and reading from 16 consecutive 8-bit I/O addresses. The first address, or BASE ADDRESS, is determined by setting a bank of switches on the board.

Most often, register manipulation is best left to experienced programmers with a specific need for low level control. If this is the case for you, use the information that follows to write your own code. Otherwise, we strongly suggest you consider using the Universal Library™ instead.

The register descriptions all follow the format:

7	6	5	4	3	2	1	0
A/D9	A/D10	A/D11	A/D12 LSB	CH8	CH4	CH2	CH1

The numbers along the top row are the bit positions within the 8-bit byte and the numbers and symbols in the bottom row are the functions associated with that bit.

To write to or read from a register in decimal or HEX, the following weights apply:

Table 3-1. Bit Weights

BIT POSITION	DECIMAL VALUE	HEX VALUE
0	1	1
1	2	2
2	4	4
3	8	8
4	16	10
5	32	20
6	64	40
7	128	80

To write control or data to a register, the individual bits must be set to 0 or 1 then combined to form a Byte.

The method of programming required to set/read bits from bytes is beyond the scope of this manual.

In summary form, the registers and their function are listed on Table 3-2.

Table 3-2. Register Summary

ADDRESS	READ FUNCTION	WRITE FUNCTION
BASE	A/D Bits 9 to 12 (LSB) & Chan. #	Start A/D Conversion
BASE + 1	A/D Bits 1 (MSB) to 8	None
BASE + 2	Channel MUX Read	Channel MUX Set
BASE + 3	Digital 4 Bit Input	Digital 4 Bit Output
BASE + 4	None	None
BASE + 5	None	None
BASE + 6	None	None
BASE + 7	None	None
BASE + 8	Status EOC, UNI/BIP etc.	None
BASE + 9	DMA, Interrupt & Trigger Control	Set DMA, INT etc.
BASE + 10	Pacer clock control register	None
BASE + 11	Gain setting read-back	Gain control
BASE + 12	Counter 0 Data	Counter 0 Data
BASE + 13	CTR 1 Data - A/D Pacer Clock	CTR 1 Data - A/D Pacer
BASE + 14	CTR 2 Data- A/D Pacer Clock	CTR 2 Data - A/D Pacer
BASE + 15	None. No read back on 8254.	Pacer Clock Control (8254)

3.2 A/D DATA & CHANNEL REGISTERS

BASE ADDRESS:

3.2.1 12-BIT BOARDS

7	6	5	4	3	2	1	0
A/D9	A/D10	A/D11	A/D12 LSB	CH8	CH4	CH2	CH1

Read/write register.

READ

On read, it contains two types of data. The least significant four digits of the analog input data and the channel number which the current data was taken from.

These four bits of analog input data must be combined with the eight bits of analog input data in BASE + 1, forming a complete 12 bit number. The data is in the format 0 = minus full scale. 4095 = +FS.

The channel number is binary. The weights are shown in Table 3-1. If the current channel were 5 then bits CH4 and CH1 would be high, CH8 and CH2 would be low.

WRITE

Writing any data to the register causes an immediate A/D conversion.

3.2.2 16-BIT BOARDS

7	6	5	4	3	2	1	0
A/D8	A/D9	A/D10	A/D11	A/D12	A/D13	A/D14	A/D15 LSB

A read/write register.

READ

On read, it contains the least significant eight digits of the Analog input data.

These eight bits of analog input data must be combined with the eight bits of analog input data in BASE + 1, forming a complete 16 bit number. The data is in the format 0 = minus full scale. 65,536 = +FS.

WRITE

Writing any data to the register causes an immediate A/D conversion.

BASE ADDRESS + 1

7	6	5	4	3	2	1	0
A/D0 MSB	A/D1	A/D2	A/D3	A/D4	A/D5	A/D6	A/D7

A Read-only register.

On read the most significant A/D byte is read.

3.3 CHANNEL MUX SCAN LIMITS REGISTER

BASE ADDRESS + 2

7	6	5	4	3	2	1	0
CH H8	CH H4	CH H2	CH H1	CH L8	CH L4	CH L2	CH L1

A read and write register.

READ

The current channel scan limits are read as one byte. The high channel number scan limit is in the most significant 4 bits. The low channel scan limit is in the least significant 4 bits.

WRITE

The channel scan limits desired are written as one byte. The high channel number scan limit is in the most significant 4 bits. The low channel scan limit is in the least significant 4 bits.

Bits 3-0 contain the starting channel number and bits 7-4 contain the ending channel number. If you wanted to scan channels 1, 2, 3 in that order, do so by placing the 3 in bits 7-4 and the 1 in bits 3-0.

NOTE

Every write to this register sets the current A/D channel MUX setting to the number in bits 0-3. See BASE + 8.

3.4 4-BIT DIGITAL I/O REGISTERS

BASE ADDRESS + 3

7	6	5	4	3	2	1	0
0	0	0	0	DI3	DI2, CTR 0 GATE	DI1	DI0, TRIG

When read...

READ

The signals present at the inputs are read as one byte, the most significant 4 bits of which are always zero. The pins 25 (digital input 0) and 24 (digital input 2) digital inputs have two functions each.

The TRIG function of digital input 0 may be used to hold of the first sample of an A/D set by holding it low (0V) until you are ready to take samples, which are then paced by the 8254. It can also be used as the source of an external start conversion pulse, synchronizing A/D conversions to some external event.

When written to..

7	6	5	4	3	2	1	0
X	X	X	X	DO3	DO2	DO1	DO0

WRITE

The upper four bits are ignored. The lower four bits are latched TTL outputs. Once written, the state of the inputs cannot be read back because a read back would read the separate digital input lines (see above).

3.5 STATUS REGISTER

BASE ADDRESS + 8

7	6	5	4	3	2	1	0
EOC	U/B	MUX	INT	CH8	CH4	CH2	CH1

A read mostly, one-function-write register.

READ

EOC = 1, the A/D converter is busy. EOC = 0, it is free.

U/B = 1, the amplifier is in Unipolar mode. U/B = 0, is bipolar.

MUX = 1, Channels are configured 16 single ended. MUX = 0, 8 differential.

INT = 1, an external pulse has been received. INT = 0, the flip-flop is ready to receive a pulse..

There is a flip-flop on the TRIGGER input (pin 25) which will latch a pulse as short as 200 nanoseconds. Once triggered, this flip-flop must be reset by a write to this register. Your interrupts service routine must do this before another interrupt trigger can be received.

CH8, CH4, CH2 & CH1 are a binary number between 0 and 15 indicating the channel number that the MUX is currently set to and is valid only when EOC = 0. The channel MUX increments shortly after EOC = 1 so may be in a state of transition when EOC = 1. The binary weight of each bit is shown in the table above.

WRITE

A write of any data to this register resets the flip-flop on the pin 25 input and sets the INT bit to 0.

3.6 DMA, INTERRUPT & TRIGGER CONTROL

BASE ADDRESS + 9

7	6	5	4	3	2	1	0
INTE	IR4	IR2	IR1	Don't Care	DMA	TS1	TS0

A read and write register.

READ

INTE = 1, Interrupts are enabled. An interrupt generated will be placed on the PC bus interrupt level selected by IR4, IR2 & IR1. INTE = 0, interrupts are disabled.

IR4, IR2, IR1 are bits in a binary number between 0 and 7 which map interrupts onto the PC bus interrupt levels 2 - 7. Interrupts 0 & 1 may not be asserted by the PC104-DAS16Jr/xx.

DMA = 1, DMA transfers are enabled. DMA = 0, DMA transfers are disabled. It is worth noting that this bit only allows the PC104-DAS16Jr/xx to assert a DMA request to the PC on the DMA request level selected by the DMA switch on the PC104-DAS16Jr/xx. Before this bit is set to 1, the PC's 8237 (or appropriate) DMA controller chip must be set up.

TS1 & TS0 control the source of the A/D start conversion trigger according to Table 4-4 below.

Table 3-3. A/D Start Conversion Source Coding

TS1	TS0	
0	X	Software triggered A/D only.
1	0	Start on rising TRIGGER (Digital input 0, Pin 25)
1	1	Start on Pacer Clock Pulse (CTR 2 OUT, no external access)

3.7 PACER CLOCK CONTROL REGISTER

BASE ADDRESS + 10

7	6	5	4	3	2	1	0
X	X	X	X	X	X	CTR0	TRIG0

WRITE only

CTR0 = 1. When CTR0 = 1, an on-board 100 kHz clock signal is ANDed with the COUNTER 0 CLOCK INPUT (pin 21). A high on pin 21 will allow pulses from the on-board source into the 8254 Counter 0 input.

CTR0 = 0. When CTR0 = 0, the input to 8254 Counter 0 is entirely dependent on pulses at pin 21, COUNTER 0 CLOCK INPUT.

TRIG0 = 1. When TRIG0 = 1, the TRIGGER input at pin 25 is ANDed with TRIG0 which must be high for the pulses from the on-board pacer clock (8254) to start A/D conversions. The input at pin 25 is pulled up and will always be high unless pulled low externally.

TRIG0 = 0. When = 0, the GATEs of counter 1 & 2 are held high, preventing the gating of the pacer externally from pin 25.

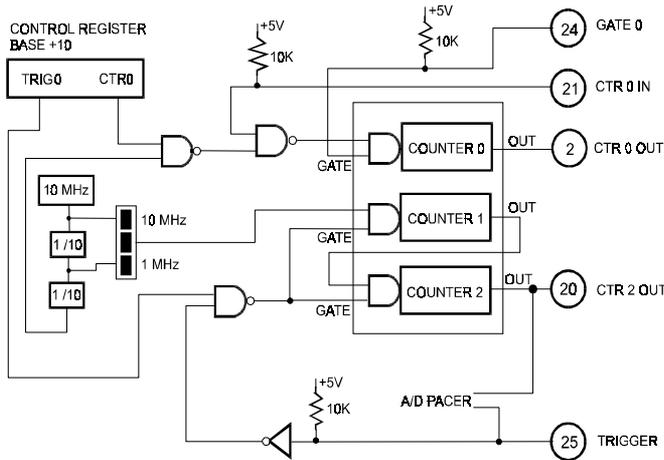Figure 3-1 shows the relationship of this register to the pacer counters and associated logic..

Figure 3-1. Pacing Control Counters

3.8 ANALOG INPUT RANGE REGISTER

BASE ADDRESS + 11

7	6	5	4	3	2	1	0
X	X	X	X	Range	Uni/Bip	G1	G0

Table 3-4. Input Range Codes PC104-DAS16Jr/12

RANGE	UNI/BIP	G1	G0	INPUT RANGE	DECIMAL
1	0	0	0	±10V	8
0	0	0	0	±5V	0
0	0	0	1	±2.5V	1
0	0	1	0	±1.25V	2
0	0	1	1	±0.625V	3
0	1	0	0	0 to 10V	4
0	1	0	1	0 to 5V	5
0	1	1	0	0 to 2.5V	6
0	1	1	1	0 to 1.25V	7

Table 3-5. Input Range Codes PC104-DAS16Jr/16

RANGE	UNI/BIP	G1	G0	INPUT RANGE	DECIMAL
0	0	0	0	±10V	0
0	0	0	1	±5V	1
0	0	1	0	±2.5V	2
0	0	1	1	±1.25V	3
0	1	0	0	0 to 10V	4
0	1	0	1	0 to 5V	5
0	1	1	0	0 to 2.5V	6
0	1	1	1	0 to 1.25V	7

A write to this register sets the analog input range for all 8/16 analog inputs. For the PC104-DAS16Jr/12, range is programmable; the lower four bits set the analog input range. For the PC104-DAS16Jr/16, the lower two bits set the range; the Uni/Bip bit is set by hardware and the Range bit is not used. The upper four bits are not used for either board. The current range is determined by reading this register.

3.9 PACER CLOCK DATA & CONTROL REGISTERS

8254 COUNTER 0 DATA

BASE ADDRESS + 12

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

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8254 COUNTER 1 DATA

BASE ADDRESS + 13   30Dh, 781 decimal

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

8254 COUNTER 2 DATA

BASE ADDRESS + 14   30Eh, 782 decimal

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

Because each counter will count as high as 65,535, loading or reading the counter data is a multi-step process. Refer to the 82C54 data sheet for details regarding its programming. The data sheet is available at:
http://www.measurementcomputing.com/PDFmanuals/82C54.pdf

8254 COUNTER CONTROL

BASE ADDRESS + 15   30Fh, 783 decimal

7	6	5	4	3	2	1	0
D8	D7	D6	D5	D4	D3	D2	D1

This register controls the operation and loading/reading of the counters. Refer to the 82C54 data sheet for programming details.

3.10 ANALOG INPUTS

Analog signals connected to the analog inputs are first fed into the two HI-0508 analog multiplexers (MUXs). A MUX's function is to select one of the inputs and connect that input to the MUX output. One of these MUX chips connects CH0-CH7 high inputs. The other connects CH0-CH7 Low input (differential input mode) or CH8-CH15 High inputs (single ended mode) depending on the state of the channel configuration switch marked 8/16.

From the output of the MUX, the analog signal is fed into a programmable differential amplifier.

The A/D converter chip has an integral sample & hold circuit, greatly simplifying design and improving signal integrity. The A/D converter is capable of sampling rates to 330 kHz but the DMA transfer circuitry of the personal computer's 8-bit bus is limited to a maximum synchronous transfer rate of less than the maximum A/D rate.

Therefore the maximum sampling rate of the PC104-DAS16Jr/xx is dependent on the computer.

3.11 DIGITAL INPUT & OUTPUT

There are four bits of output only and four bits of input only on the analog connector. From the original DAS-16 design these were the only eight bits of digital I/O.

4 SPECIFICATIONS

Power consumption

+5VDC quiescent

PC104-DAS16Jr/12	140 mA typical, 230 mA max
PC104-DAS16Jr/16	145 mA typical, 205 mA max

+ 5VDC Operating (A/D converting to FIFO)

PC104-DAS16Jr/12	250 mA typical, 375 mA max
PC104-DAS16Jr/16	235 mA typical, 350 mA max

Analog input section

A/D converter type	
PC104-DAS16Jr/16	AD7805
PC104-DAS16Jr/12	AD7800
Resolution	
PC104-DAS16Jr/12	12 bits
PC104-DAS16Jr/16	16 bits
Number of channels	8 differential or 16 single-ended, switch-selectable
Input ranges	
PC104-DAS16Jr/12	$\pm$10V, $\pm$5V, $\pm$2.5V, $\pm$1.25V, $\pm$0.625V, 0 to 10V, 0 to 5V, 0 to 2.5V, 0 to 1.25V fully programmable
PC104-DAS16Jr/16	$\pm$10V, $\pm$5V, $\pm$2.5V, $\pm$1.25V programmable in Bipolar mode OR 0 to 10V, 0 to 5V, 0 to 2.5V, 0 to 1.25V programmable in Unipolar mode
Polarity	Unipolar/Bipolar switch-selectable
A/D Pacing	Programmable: internal counter, external source (Din 0 / Trigger) or software polled
A/D Trigger sources	External polled gate trigger (DIn 0)
A/D Triggering Modes	
Digital:	Gated pacer, software polled. (Gate must be disabled by software after trigger event.)
Data transfer	From 512 sample FIFO via interrupt, DMA or software polled
DMA	Channel 1 or 3, switch-selectable
DMA enable	Programmable

A/D conversion time
    PC104-DAS16Jr/12   3.3 μs
    PC104-DAS16Jr/16   10 μs
Throughput
    PC104-DAS16Jr/12   150 kHz
    PC104-DAS16Jr/16   100 kHz
Accuracy
    PC104-DAS16Jr/12   0.01% of reading, ±1LSB
    PC104-DAS16Jr/16   0.003% of reading, ±1LSB
Integral Linearity error
    PC104-DAS16Jr/12   ±1 LSB
    PC104-DAS16Jr/16   ±1.5 LSB (±3LSB on 1.25V ranges)
Differential Linearity   ±1 LSB
No missing codes guaranteed
    PC104-DAS16Jr/12   12 bits
    PC104-DAS16Jr/16   16 bits
Gain drift (A/D specs)
    PC104-DAS16Jr/12   ±6 ppm/°C
    PC104-DAS16Jr/16   ±7 ppm/°C
Zero drift (A/D specs)
    PC104-DAS16Jr/12   ±1 ppm/°C
    PC104-DAS16Jr/16   ±2 ppm/°C

Common Mode Range   ±10V
CMRR @ 60 Hz   70 dB
Input leakage current (@ 25 deg C)   ±20 nA
Input impedance   10 Mohms min
Absolute maximum input voltage   ±35V

Digital I/O section

Digital type   FPGA
Configuration   Two ports, 4 bits each, 4 input and
                                4 output
Input low voltage   0.8V max
Input high voltage   2.0V min
Output low voltage (IOL = 4 mA)   0.32V max
Output high voltage (IOH = −4 mA)   3.86V min
Absolute maximum input voltage   −0.5V , +5.5V
Interrupts   Programmable: levels 2 to 7
Interrupt enable   Programmable
Interrupt sources   End-of-conversion, DMA terminal
                                count

Counter section

Counter type	82C54
Configuration	3 down-counters, 16 bits each

Counter 0 - Independent user counter
    Source: Programmable (external or 100 kHz internal source)
    Gate: Available at connector (DIn 2)
    Output: Available at connector (Ctr 0 Out)

Counter 1 - ADC Pacer Lower Divider
    Source: Jumper-selectable 1/10 MHz
    Gate: Tied to Counter 2 gate, can be program-enabled at user connector (DIn 0 / Trigger).
    Output: Chained to Counter 2 Clock.

Counter 2 - ADC Pacer Upper Divider
    Source: Counter 1 Output.
    Gate: Tied to Counter 1 gate, programmable source.
    Output: Programmable as ADC Pacer clock, hardwired to user connector (Ctr 2 Out)

Clock input frequency	10 MHz max
High pulse width (clock input)	30 ns min
Low pulse width (clock input)	50 ns min
Gate width high	50 ns min
Gate width low	50 ns min
Input low voltage	0.8V max
Input high voltage	2.0V min
Output low voltage	0.4V max
Output high voltage	3.0V min

Crystal oscillator
Frequency	10 MHz
Frequency accuracy	100 ppm

Environmental

Operating temperature range	0 to 50°C
Storage temperature range	−40 to 100°C
Humidity	0 to 90% non-condensing

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For your notes.

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EC Declaration of Conformity

We, Measurement Computing Corporation., declare under sole responsibility that the product:

PC104-DAS16Jr/12
PC104-DAS16Jr/16   Analog input boards for PC104 bus

Part Number   Description

to which this declaration relates, meets the essential requirements, is in conformity with, and CE marking has been applied according to the relevant EC Directives listed below using the relevant section of the following EC standards and other normative documents:

EU EMC Directive 89/336/EEC: Essential requirements relating to electromagnetic compatibility.

EU 55022 Class B: Limits and methods of measurements of radio interference characteristics of information technology equipment.

EN 50082-1: EC generic immunity requirements.

IEC 801-2: Electrostatic discharge requirements for industrial process measurement and control equipment.

IEC 801-3: Radiated electromagnetic field requirements for industrial process measurements and control equipment.

IEC 801-4: Electrically fast transients for industrial process measurement and control equipment.

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