Tektronix Logic Analyzers

TLA7000 Series Data Sheet

Features & Benefits

- 68/102/136 Channel Logic Analyzers with up to 512 Mb Record Length
- MagniVu™ Acquisition Technology provides up to 20 ps (50 GHz) Timing Resolution to Find and Measure Elusive Timing Problems Quickly
- Up to 156 ps (6.4 GHz)/512 Mb Record Length Timing Analysis
- Up to 1.4 GHz Clock with up to 3.0 Gb/s Data with a Data Valid Window of 180 ps for State Acquisition Analysis of High-performance Synchronous Buses
- Glitch and Setup/Hold Triggering and Display Finds and Displays Elusive Hardware Problems
- Transitional Storage Extends the Signal Analysis Capture Time for Signals that Transition Infrequently
- Simultaneous State, High-speed Timing, and Analog Analysis through the Same Probe Pinpoints Elusive Faults
- Compression Probing System with 0.5 pF Capacitive Loading Eliminates Need for Onboard Connectors, Minimizes Intrusion on Circuits, and is Ideal for Differential Signal Applications
- Trace Problems from Symptom back to Root Cause in Real Time across Multiple Modules by Viewing Time-correlated Data in a Wide Variety of Display Formats
- PCI Express Gen1 through Gen3 including Gen3 Protocol to Physical Layer Analysis for Link Widths from x1 through x16 with up to 8.0 GT/s Acquisition Rates and up to 16 GB Deep Memory (for x16 Link)
- Comprehensive PCI Express Probing Solutions, including Midbus, Slot Interposer, and Solder-down Connectors
- Modular Mainframes provide Flexibility and Expandability
- Supports up to 6,528 Logic Analyzer Channels, 48 Independent Buses
- Broad Processor and Bus Support

Applications

- FPGA Debug and Verification
- MIPI Protocol Analysis
- DDR2 and DDR3 Debug and Verification
- Signal Integrity
- PCI Express Debug from Protocol Layer to Physical Layer
  - Silicon Validation
  - Computer System Validation
  - Embedded System Debug and Validation
- Processor/Bus Debug and Verification
- Embedded Software Integration, Debug, and Verification

Breakthrough Solutions for Real-time Digital Systems Analysis

Tektronix provides breakthrough digital systems analysis tools that enable digital hardware and software designers to capture and analyze the source of elusive problems that threaten product development schedules. The TLA7000 Series provides the speed you need to capture the source of those elusive problems, plus the visibility you want with large displays and fast system data throughput, while protecting your investment with compatibility with all TLA modules.

Tektronix®

TLA7012 and TLA7016 Mainframes

The TLA7012 Portable and TLA7016 Benchtop mainframes are modular mainframes that accept TLA logic analyzer and pattern generator modules. The TLA7012 and TLA7016 can be configured as either master or expansion mainframes to provide solutions for large numbers of buses and high channel-count requirements.

The TLA7012 Portable Mainframe and TLA7016 Benchtop Mainframe along with the TLAPC1 Benchtop Controller are built on a Microsoft Windows XP Professional PC platform that offers a familiar work environment for the TLA application software. They provide multiple display capability for extended desktop viewing, in addition to an internal DVD-RW, hard drive, and multiple USB 2.0 ports for expansion. A replaceable hard drive is standard on both mainframes, ideal for security or enabling individual team members to store personal setups and data. Trigger in/out connections provide an interface to other external instrumentation, such as DPO oscilloscopes, for correlating measurement results.

P6800 and P6900 Series Probes

No test and measurement solution is complete without probing. With the industry's lowest capacitance, the P6800 and P6900 Series logic analyzer probes protect the integrity of your signal – critical for connecting to fast buses like DDR2 and DDR3 where low intrusion is key to the proper operation of your design. Select from single-ended and differential probes and a variety of attachment mechanisms, including the "connectorless" compression connection that eliminates the need for onboard connectors.

For applications where circuit board space is at a premium, the high-density P6900 Series with D-Max® Probing Technology offers the industry's smallest available footprint. For debugging the signal integrity glitches common on fast buses, the P6900 Series works with the TLA7BBx and TLA7ACx modules and their iLink™ Tool Set capability to provide iCapture™ simultaneous digital-analog acquisition. This allows you to clearly see the time-correlated digital and analog behavior of your design, without the extra capacitance and setup time of double-probing.

For differential signaling applications where signal integrity is critical, the high-fidelity P6980 and P6982 are perfect for those applications where noise performance is critical. In addition, the P6980 and P6982 can support the small voltage swings that differential signaling often requires. The P6962DBL, when used with a TLA7000 Series logic analyzer with the TLA7BBx module, supports digital validation and debug of DDR3 memory with data rates up to 1600 mega-transfers per second. For board designs that do not include high-density probe footprints, the P6960 with its companion flying leadset provides the flexibility required to meet many different debug needs.

P6700 Series Probes for PCI Express

The P6700 Series probes provide validation engineers with a comprehensive set of PCI Express probing solutions, including midbus, slot interposer, and solder-down connectors. With support for PCI Express Gen3 channel lengths up to 24 in. with 2 connectors, these probes offer minimal electrical loading with the highest signal fidelity and active equalization to ensure accurate data recovery of closed eyes. All P6700 Series probes feature a graphical lane swizzling capability for maximum flexibility to accommodate unique circuit board layouts.

TLA7ACx and TLA7BBx Modules

Today's digital design engineers face daily pressures to speed new products to the marketplace. The TLA7ACx and TLA7BBx Series logic analyzer modules answer the need with breakthrough solutions for the entire design team, providing the ability to quickly monitor, capture, and analyze real-time digital system operation in order to debug, verify, optimize, and validate digital systems. Hardware developers, hardware/software integrators, and embedded software developers will appreciate the range of capabilities of the TLA7ACx and TLA7BBx Series logic analyzer modules. Its broad feature set includes capturing and correlating elusive hardware and software faults; providing simultaneous state, high-speed timing, and analog analysis through the same probe; using deep state acquisition to find the cause of complex problems; real-time, nonintrusive software execution tracing that correlates to source code and to hardware events; and nonintrusive connectorless probing.

The TLA7BBx Series logic analyzer modules offer breakthrough MagniVu™ technology by Tektronix for providing high-speed sampling (up to 50 GHz) that dramatically changes the way logic analyzers work and enables them to provide startling new measurement capabilities. The TLA7BBx modules offer high-speed state synchronous capture, high-speed timing capture, and analog capture through the same set of probes. They capitalize on MagniVu technology to offer up to 20 ps timing on all channels, glitch and setup/hold triggering, and display and time stamp that is always on at up to 20 ps resolution.

To compliment the high-performance logic analyzer modules, the TLA7ACx Series logic analyzer modules offer all the same debug and verification functionality, but with performance levels more suited to the embedded designer. The TLA7ACx modules offer high-speed state synchronous capture, high-speed timing capture, and analog capture through the same set of probes. MagniVu technology offering up to 125 ps timing on all channels, glitch and setup/hold triggering, and display and time stamp that is always on at 125 ps resolution is available as standard on all models.

Module	Timing Resolution	State Speed	Memory
TLA7ACx	125 ps (8 GHz)	Up to 800 MHz	Up to 128 Mb
TLA7BBx	20 ps (50 GHz)	Up to 1.4 GHz	Up to 64 Mb

TLA7SAxx PCI Express Logic Protocol Analyzer Modules

PCI Express 3.0 introduces new challenges for validation engineers. Time-to-market pressures require a solution that can quickly pinpoint problems. The TLA7SAxx Series logic protocol analyzer modules provide an innovative approach to PCI Express validation that spans all layers of the protocol from the physical layer to the transaction layer.

Reduce your time to information by viewing and searching up to 16 GB deep memory in just seconds with rapid display updates enabled by our industry-leading hardware acceleration. With improved information density you can then quickly ascertain the health of the system and identify patterns of interest (errors, specific transactions, ordered sets, etc.) with statistics using the Summary Profile window. Protocol behavior can be viewed at the packet and transaction level interspersed with physical layer activity in a single innovative Transaction window. Further insight into physical layer details can be gained with the unique Listing window showing packet details at the symbol level by lane and you can view individual lane activity correlated with analog waveforms from your high-bandwidth oscilloscope in the Waveform window.

Hardware developers, hardware/software integrators, and embedded system designers will appreciate the tight integration with the Tektronix Logic Analyzer. This provides visibility of complete system interactions with time-correlated, multibus analysis on a single display. Cross triggering and a common global time stamp enables accurate and efficient debugging by showing exactly what was happening on one bus relative to another at any given instant of time. Coupled with the P6700 Series probing solutions, engineers have flexible options for platform accessibility.

TLA7012 and TLA7016 Characteristics

General

Characteristic	Description
Instrument Slots	TLA7012: Holds 2 TLA modules TLA7016: Holds 6 TLA modules
Expansion Capability	The TLA7000 Series mainframes can be used as either master or expansion mainframes (TL708EX 8-port Instrument Hub and Expander is required for 3-8 mainframes connected together using TekLink™ cable) TLA7012: Up to eight TLA7012 mainframes can be used, providing support for up to 16 TLA modules (2,176 channels) TLA7016: Up to eight TLA7016 mainframes can be used, providing support for up to 48 TLA modules (6,528 channels)

TLA7012 PC Characteristics

Characteristic	Description
Operating System	Microsoft® Windows® XP Professional and Multilingual User Interface Pack
Processor	2 GHz Intel® Pentium® M-760
Chipset	Intel® 915GM
Memory	1 GB DDR PC 533 MHz (SODIMM), expandable to 2 GB DDR memory
Sound	Line In and Mic Out connectors
Removable Hard Drive	3.5 in., ≥80 GB Serial ATA, 7200 RPM
Optical Drive	Internal 4.7 GB DVD±R/RW
External Display Port Type	One (1) DVI-D (primary – digital only) and one (1) DVI-I (secondary – digital and analog) connectors
External Display Resolution	Up to 1600×1200 noninterlaced at 32-bit color, each for both primary and secondary displays
Network Port	One (1) 10/100/1000 LAN with RJ-45 connector
USB 2.0 Port	Seven (7); three (3) in front and four (4) in rear

TLA7012 Integral Controls

Characteristic	Description
Front-panel Display	Size: 15 in. (38.1 cm) diagonal Type: Active-matrix color TFT LCD with backlight Resolution: 1024×768
Simultaneous Display Capability	Both the front-panel and one external display can be used simultaneously at 1024×768 resolution
Front Panel	General-purpose knob with dedicated hotkeys and knobs for horizontal and vertical scaling and scrolling
Touch Screen	Available with Option 18

Integrated View (iView™) Capability

Characteristic	Description
TLA Mainframe Configuration Requirements	GPIB-iView (Opt. 1C) requires TLA Application Software V5.0 or greater USB-iView (Opt. 2C) requires TLA Application Software V5.8 or greater
Number of Tektronix Oscilloscopes that can be Connected to a TLA System	1
External Oscilloscopes Supported	More than 100. For a complete listing of currently supported oscilloscopes, please visit our website http://www.tektronix.com/iview
TLA Connections	USB, Trigger In, Trigger Out, Clock Out
Oscilloscope Connections	
GPIB-iView (Opt. 1C)	GPIB, Trigger In, Trigger Out, Clock In (when available)
USB-iView (Opt. 2C)	USB Device Port, Trigger In, Trigger Out
Setup	iView™ external oscilloscope wizard automates setup
Data Correlation	After oscilloscope acquisition is complete, the data is automatically transferred to the TLA and time correlated with the TLA acquisition data
Deskew	The oscilloscope and TLA data is automatically deskewed and time correlated when using the iView™ external oscilloscope cable
GPIB-iView™ (Opt. 2C) External Oscilloscope Cable Length	2 m (6.6 ft.)
USB-iView (Opt. 2C) External Oscilloscope Cable Length	1.8 m (6 ft.)

Symbolic Support

Characteristic	Description
Number of Symbols/Ranges	Unlimited (limited only by amount of virtual memory available on TLA)
Object File Formats Supported	IEEE695, OMF 51, OMF 86, OMF 166, OMF 286, OMF 386, COFF, Elf/Dwarf 1 and 2, Elf/Stabs, TSF (If your software development tools do not generate output in one of the above formats, TSF, or the Tektronix symbol file, a generic ASCII file format is supported. The generic ASCII file format is documented in the TLA User Manual). If a format is not listed, please contact your local Tektronix representative

TLA7012 and TLA7016 External Instrumentation Interfaces

Characteristic	Description
System Trigger Output	Asserted whenever a system trigger occurs (TTL-compatible output, back-terminated into 50 Ω)
System Trigger Input	Forces a system trigger (triggers all modules) when asserted (adjustable threshold between 0.5 V and 1.5 V, edge-sensitive, falling-edge latched)
External Signal Output	Can be used to drive external circuitry from a module's trigger mechanism (TTL-compatible output, back-terminated into 50 Ω)
External Signal Input	Can be used to provide an external signal to arm or trigger any or all modules (adjustable threshold between 0.5 V and 1.5 V, level sensitive)

Power

Product	Characteristics
TLA7012	Voltage Range/Frequency: 90-250 V AC at 45-66 Hz 100-132 V AC at 360-440 Hz Input Current: 7 A maximum at 90 V AC (70 A surge) Power Consumption: 750 W maximum
TLA7016	Voltage Range/Frequency: 90-250 V AC at 45-66 Hz, 100-132 V AC at 360-440 Hz Input Current: 16.5 A maximum at 90 V AC (70 A surge) Power Consumption: 1,450 W maximum
TL708EX	Voltage Range/Frequency: 100-240 V AC at 50-60 Hz Input Current: 2 A maximum at 100 V AC Power Consumption: 200 W maximum

Environmental

Characteristic	Description
Temperature	Operating: +5 °C to +45 °C Nonoperating: –20 °C to +60 °C
Humidity	20% to 80% Operating: ≤30 °C; 80% relative humidity (29 °C maximum wet-bulb temperature) Nonoperating: 8% to 80% (29 °C maximum wet-bulb temperature)
Altitude	Operating: –1,000 ft. to 10,000 ft. (–305 meters to 3,050 meters)
Safety	UL3111-1, CSA1010.1, EN61010-1, IEC61010-1

Physical Characteristics

TLA7012 Portable

Dimensions	mm	in.
Height	295	11.6
Width	451	17.75
Depth	460	18.1
Weight	**kg**	**lb.**
Net (w/o modules)	14	30
Shipping (Typical)	27	59

TLA7016 Benchtop

Dimensions	mm	in.
Height	350	13.7
Width	425	16.7
Depth	673	26.5
Weight	**kg**	**lb.**
Net (w/o modules)	25	55
Shipping (Typical)	51.8	115

TL708EX 8-port Instrument Hub and Expander

Dimensions	mm	in.
Height	51	2
Width	445	17.5
Depth	305	12
Weight	**kg**	**lb.**
Net	3	6
Shipping	5	11

TLA7ACx Characteristics

General

Characteristic	Description
Number of Channels (All channels are acquired including clocks)	
TLA7AC2	68 channels (4 are clock channels)
TLA7AC3	102 channels (4 are clock and 2 are qualifier channels)
TLA7AC4	136 channels (4 are clock and 4 are qualifier channels)
Channel grouping	No limit to number of groups or number of channels per group (all channels can be reused in multiple groups)
Module "Merging"	Up to five 102-channel or 136-channel modules can be "merged" to make up to a 680-channel module. Merged modules exhibit the same depth as the lesser of the five individual modules. Word/setup-and-hold/glitch/transition recognizers span all five modules. Range recognizers limited to three-module merge. Only one set of clock connections is required.
Time Stamp	51 bits at 125 ps resolution (3.25 days duration)
Clocking/Acquisition Modes	Asynchronous/Synchronous 8 GHz MagniVu high-speed timing is available simultaneous with all modes
Number of Mainframe Instrument Slots Required per TLA Series Module	1

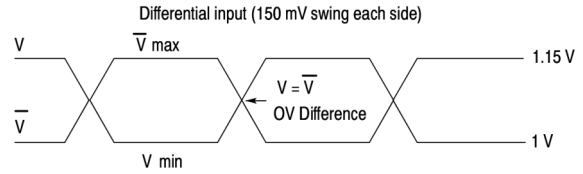
Input Characteristics (with P6800 or P6900 Series probes)

Characteristic	Description
Capacitive Loading	0.5 pF clock/data (P6900 Series) <0.7 pF clock/data (P6800 Series) (1.0 pF for P6810 in group configuration)
Threshold Selection Range	From –2.0 V to +4.5 V in 5 mV increments Threshold presets include TTL (1.5 V), CMOS (1.65 V), ECL (–1.3 V), PECL (3.7 V), LVPECL (2.0 V), LVCMOS 1.5 V (0.75 V), LVCMOS 1.8 V (0.9 V), LVCMOS 2.5 V (1.25 V), LVCMOS 3.3 V (1.65 V), LVDS (0 V), and user defined
Threshold Selection Channel Granularity	Separate selection for each of the clock/qualifier channels and one per group of 16 data channels for each 34-channel probe
Threshold Accuracy (including probe)	±(35 mV + 1%)
Input Voltage Range	
Operating	–2.5 V to 5.0 V
Nondestructive	±15 V
Minimum Input Signal Swing	300 mV (single ended) $V_{MAX} – V_{MIN}$ > 150 mV (differential)
Input Signal Minimum Slew Rate	200 mV/ns typical

State Acquisition Characteristics (with P6800 or P6900 Series probes)

Full Channel	Half Channel	Quarter Channel
235 MHz	450 MHz / 450 Mb/s or 470 Mb/s (DDR)	450 MHz / 900 Mb/s
450 MHz Optional	800 MHz / 800 Mb/s or 900 Mb/s (DDR)	625 MHz / 1.25 Gb/s

Characteristic	Description
State Record Length with Time Stamps	(Quarter/Half/Full channels) 8/4/2 Mb, 32/16/8 Mb, 128/64/32 Mb, 512/256/128 Mb per channel
Setup-and-Hold Time Selection Range	From 16 ns before, to 8 ns after clock edge in 125 ps increments. Range may be shifted towards the setup region by 0 ns [+8, –8] ns, 4 ns [+12, –4] ns, or 8 ns [+16, 0] ns
Setup-and-Hold Window	
All channels	625 ps typical
Single channel	500 ps typical
Minimum Clock Pulse Width	500 ps (P6960, P6964, P6980, P6982, P6860, P6864, P6880), 700 ps (P6810)
Active Clock Edge Separation	400 ps
Demux Channel Selection	Channels can be demultiplexed to other channels through user interface with 8-channel granularity
Source Synchronous Clocking	Up to four "Fast Latches" per module (20 max per 5-way merge) to strobe source-synchronous buses into TLA7ACx modules. Four sets of any predefined "Fast Latches" may be combined with qualification data and data pipelining to store four independent source-synchronous data buses. Two "Fast Latches" may be combined to address DDR applications.



Differential equivalent signal input (300 mV swing) as viewed by the logic analyzer and the analog probe output**.

* Note: For differential inputs, the module threshold should be set to OV (assuming no common mode error).

** Note: See online help for further analog output details.

Timing Acquisition Characteristics (with P6800 or P6900 Series probes)

Characteristic	Description
MagniVu™ Timing	125 ps max, adjustments to 250 ps, 500 ps, 1 ns, and 2 ns
MagniVu Timing Record Length	16 Kb per channel, with adjustable trigger position
Deep Timing Resolution (Quarter/Half/Full channels)	500 ps / 1 ns / 2 ns to 50 ms
Deep Timing Resolution with Glitch Storage Enabled	4 ns to 50 ms
Deep Timing Record Length (Quarter/Half/Full channels with time stamps and with or without transitional storage)	8/4/2 Mb, 32/16/8 Mb,128/64/32 Mb, 512/256/128 Mb per channel
Deep Timing Record Length with Glitch Storage Enabled	Half of default main memory depth
Channel-to-Channel Skew	300 ps typical
Minimum Recognizable Pulse/Glitch Width (Single channel)	500 ps (P6960, P6964, P6980, P6982, P6860, P6864, P6880), 750 ps (P6810)
Minimum Detectable Setup/Hold Violation	250 ps
Minimum Recognizable Multichannel Trigger Event	Sample period + channel-to-channel skew

Analog Acquisition Characteristics (with P6800 or P6900 Series probes)

Characteristic	Description
Bandwidth	2 GHz typical
Attenuation	10X, ±1%
Offset and Gain (Accuracy)	±50 mV, ±2% of signal amplitude
Channels Demultiplexed	4
Run/Stop Requirements	None, analog outputs are always active
iCapture™ Analog Outputs	Compatible with any supported Tektronix oscilloscope
iCapture Analog Output BNC Cable	Low loss, 10X, 36 in. Basic Analog Multiplexer functionality is offered standard on all TLA7ACx modules. This routes 4 fixed channels to the iCapture Analog Output BNCs. The outputs cannot be switched to other logic analyzer channels. Option AM enables full analog multiplexer control and allows the routing of any 4 logic analyzer channels to the iCapture Analog Output BNCs

Trigger Characteristics

Characteristic	Description
Independent Trigger States	16
Maximum Independent If/Then Clauses per State	16
Maximum Number of Events per If/Then Clause	8
Maximum Number of Actions per If/Then Clause	8
Maximum Number of Trigger Events	18 (2 counters/timers plus any 16 other resources)
Number of Word Recognizers	16
Number of Transition Recognizers	16
Number of Range Recognizers	4
Number of Counters/Timers	2
Trigger Event Types	Word, Group, Channel, Transition, Range, Anything, Counter Value, Timer Value, Signal, Glitch, Setup-and-Hold Violation, Snapshot
Trigger Action Types	Trigger Module, Trigger All Modules, Trigger Main, Trigger MagniVu, Store, Don't Store, Store Sample, Increment Counter, Decrement Counter, Reset Counter, Start Timer, Stop Timer, Reset Timer, Snapshot Current Sample, Goto State, Set/Clear Signal, Do Nothing
Maximum Triggerable Data Rate	1250 Mb/s (4X clocking mode)
Trigger Sequence Rate	DC to 500 MHz (2 ns)
Counter/Timer Range	51 bits each (>50 days at 2 ns)
Counter Rate	DC to 500 MHz (2 ns)
Timer Clock Rate	500 MHz (2 ns)
Counter/Timer Latency	2 ns
Range Recognizers	Double bounded (408 channel max). Can be as wide as any group, must be grouped according to specified order of significance
Setup-and-Hold Violation Recognizer Setup Time Range	From 8 ns before to 7 ns after clock edge in 125 ps increments. This range may be shifted towards the positive region by 0 ns, 4 ns, or 8 ns
Setup-and-Hold Violation Recognizer Hold Time Range	From 7 ns before to 8 ns after clock edge in 125 ps increments. This range may be shifted towards the positive region by 0 ns [+8, –8] ns, 4 ns [+12, –4] ns, or 8 ns [+16, 0] ns
Trigger Position	Any data sample
MagniVu Trigger Position	MagniVu position can be set from 0% to 60% centered around the MagniVu trigger
Storage Control (Data qualification)	Global (conditional), by state (start/stop), block, by trigger action, or transitional. Also force main prefill selection available

Physical Characteristics

Dimensions	mm	in.
Height	262	10.3
Width	61	2.4
Depth	381	15
Weight	**kg**	**lb.**
Net	3.1	6.7
Shipping	6.3	13.7

TLA7BBx Characteristics

General

Characteristic	Description
Number of Channels (All channels are acquired including clocks)	
TLA7BB2	68 channels (4 are clock channels)
TLA7BB3	102 channels (4 are clock, 2 are qualifier channels)
TLA7BB4	136 channels (4 are clock, 4 are qualifier channels)
Channel grouping	No limit to number of groups or number of channels per group (all channels can be reused in multiple groups)
Module "Merging"	Up to five 68-channel, 102-channel, or 136-channel modules can be "merged" to make up to a 680-channel module. Merged modules exhibit the same depth as the lesser of the five individual modules. Word/setup-and-hold/glitch/transition recognizers span all five modules. Range recognizers limited to three module merge. Only one set of clock connections is required.
Time Stamp	54 bits at 20 ps resolution (>4 days duration)
Clocking/Acquisition Modes	Asynchronous and Synchronous. 20 ps (50 GHz) MagniVu, high-speed timing is available simultaneous with all modes
Number of Mainframe Instrument Slots Required per TLA Series Module	1

Input Characteristics (with P6800 or P6900 Series probes)

Characteristic	Description
Capacitive Loading	0.5 pF clock/data (P6900 Series)
	<0.7 pF clock/data (P6800 Series); 1.0 pF for P6810 when 8-channel podlet grouper is used
Threshold Selection Range	From –2.0 V to +4.5 V in 5 mV increments Threshold presets include TTL (1.5 V), CMOS (2.5 V), ECL (–1.3 V), PECL (3.7 V), LVPECL (2.0 V), LVCMOS 1.5 V (0.75 V), LVCMOS 1.8 V (0.9 V), LVCMOS 2.5 V (1.25 V), LVCMOS 3.3 V (1.65 V), LVDS (0 V), and user defined
Threshold Selection Channel Granularity	Separate selection for each of the clock/qualifier and individual channels
Threshold Accuracy (including probe)	±(35 mV + 1%)
Input Voltage Range	
Operating	–2.5 V to 5.0 V
Nondestructive	±15 V
Minimum Input Signal Swing	200 mV (single ended)
	$V_{MAX} – V_{MIN}$ > 100 mV (differential)
Input Signal Minimum Slew Rate	200 mV/ns typical

State Acquisition Characteristics (with P6800 or P6900 Series probes)

Configuration	Full Channel	Half Channel
750 MHz Standard	750 MHz / 750 Mb/s (1 sample/clock) 750 MHz / 1.5 Gb/s (2 samples/clock)	750 MHz / 3 Gb/s (4 samples/clock)
1.4 GHz Optional	1.4 GHz / 1.4 Gb/s (1 sample/clock)	1.4 GHz / 2.8 Gb/s (2 samples/clock)

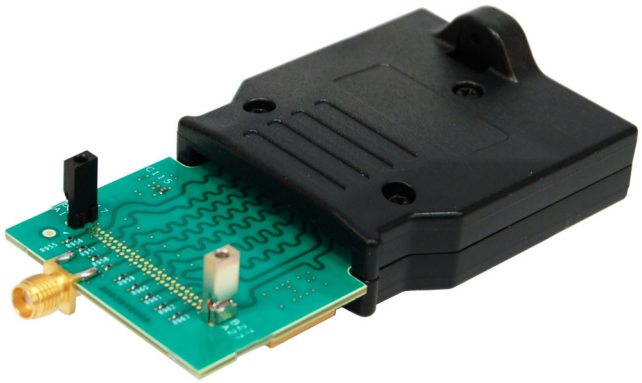
Characteristic	Description
State Record Length with Time Stamps (Half/Full channels)	4/2 Mb, 8/4 Mb, 16/8 Mb, 32/16 Mb, 64/32 Mb, 128/64 Mb per channel
Setup-and-Hold Time Selection Range	From 15 ns before, to 7.5 ns after clock edge in 20 ps increments. Range may be shifted towards the setup region by 0 ns [+7.5, –7.5] ns, 2.5 ns [+10, –5] ns, or 7.5 ns [+15, 0] ns
Setup-and-Hold Window, Single Channel	180 ps typical
Minimum Clock Pulse Width	200 ps (P6960, P6964, P6980, P6982, P6860, P6864, P6880), 250 ps (P6810)
Demux Channel Selection	Channels can be demultiplexed to other channels through user interface with 8-channel granularity

Timing Acquisition Characteristics (with P6800 or P6900 Series probes)

Characteristic	Description
MagniVu™ Timing	20 ps max, adjustments to 40 ps, 80 ps, 160 ps, 320 ps, and 640 ps
MagniVu Timing Record Length	128 Kb per channel, with adjustable trigger position
Deep Timing Resolution (Quarter/Half/Full channels)	156.25 ps / 312.5 ps / 625 ps to 50 ms
Deep Timing Resolution with Glitch Storage Enabled	1.25 ns to 50 ms
Deep Timing Record Length (Quarter/Half/Full channels)	8/4/2 Mb, 16/8/4 Mb, 32/16/8 Mb, 64/32/16 Mb, 128/64/32 Mb, 256/128/64 Mb per channel
Deep Timing Record Length with Glitch Storage Enabled	Half of default main memory depth
Channel-to-Channel Skew (module + probes)	
Before customer deskew	±80 ps typical
After customer deskew *(see AutoDeskew information below)*	±20 ps typical
Minimum Recognizable Pulse/Glitch Width (Single channel)	200 ps (P6960, P6964, P6980, P6982, P6860, P6864, P6880) 250 ps (P6810)
Minimum Detectable Setup/Hold Violation	40 ps
Minimum Recognizable Multichannel Trigger Event	Sample period + channel-to-channel skew

AutoDeskew and Customer Deskew Fixture

Tektronix recommends **AutoDeskew**, a standard feature available within the TLA Application, for deskewing probe channels and setting the sample point for synchronous applications. However, for tight time alignment in both synchronous and asynchronous applications (including MagniVu), Tektronix recommends the **Customer Deskew Fixture**. This is an optional accessory to the TLA7BBx modules that is used to perform a “channel-to-channel deskew” of the probes connected to



the TLA7BBx module to ensure tight time alignment between all channels across all probes. Two different fixtures are available:

- Customer Deskew Fixture for P6800 Series Probes
- Customer Deskew Fixture for P6900 Series Probes

For ordering details, please see the Ordering Information section.

Analog Acquisition Characteristics (with P6800 or P6900 Series probes)

Characteristic	Description
Bandwidth	3 GHz (typical)
Attenuation	10X, ±1%
Offset and Gain (Accuracy)	±50 mV, ±2% of signal amplitude
Channels Demultiplexed	4
Run/Stop Requirements	None, analog outputs are always active
iCapture™ Analog Outputs	Compatible with any supported external Tektronix oscilloscope
iCapture Analog Output BNC Cables	Four (4) low loss, 10X, 36 in.

Physical Characteristics

Dimensions	mm	in.
Height	262	10.3
Width	61	2.4
Depth	381	15
Weight	**kg**	**lb.**
Net	3.1	6.7
Shipping	6.3	13.7

Trigger Characteristics

Characteristic	Description
Independent Trigger States	16
Maximum Independent If/Then Clauses per State	16
Maximum Number of Events per If/Then Clause	8
Maximum Number of Actions per If/Then Clause	8
Maximum Number of Trigger Events	26 (2 counters/timers plus any 24 other resources)
Number of Word Recognizers	24
Number of Transition Recognizers	24
Number of Range Recognizers	8
Number of Counters/Timers	2
Trigger Event Types	Word, Group, Channel, Transition, Range, Anything, Counter Value, Timer Value, Signal, Glitch, Setup-and-Hold Violation, Snapshot
Trigger Action Types	Trigger Module, Trigger All Modules, Trigger Main, Trigger MagniVu, Store, Don't Store, Start Store, Stop Store, Increment Counter, Decrement Counter, Reset Counter, Start Timer, Stop Timer, Reset Timer, Snapshot Current Sample, Goto State, Set/Clear Signal, Do Nothing
Maximum Triggerable Data Rate	3.0 Gb/s
Trigger Sequence Rate	DC to 800 MHz (1.25 ns)
Counter/Timer Range	48 bits each (~4 days at 1.25 ns)
Counter Rate	DC to 800 MHz (1.25 ns)
Timer Clock Rate	800 MHz (1.25 ns)
Counter/Timer Test Latency	0 ns
Range Recognizers	Double bounded (408 channel max). Can be as wide as any group, must be grouped according to specified order of significance
Setup-and-Hold Violation Recognizer	
Setup time range	From 7.5 ns before to 7.5 ns after clock edge in 20 ps increments. This range may be shifted towards the positive region by 0 ns, 2.5 ns, 5 ns, or 7.5 ns
Hold time range	
Trigger Position	Any data sample
MagniVu Trigger Position	MagniVu position can be set from 0% to 60% centered around the MagniVu trigger
Storage Control (Data qualification)	All, Global (conditional), by state (start/stop), block, by trigger action, or transitional. Also force main prefill selection available

TLA7SAxx Characteristics

General

Characteristic	Description
Number of Lanes	
TLA7SA08	8 differential inputs, x4
TLA7SA16	16 differential inputs, x8
Record Length	TLA7SA16: 160M Symbols per differential input, 8 GB physical memory total (16 GB physical memory for a x16 configuration) TLA7SA08: 160M Symbols per differential input, 4 GB physical memory total 160M Symbols translates into 160 ms at 8 GT/s, 320 ms at 5 GT/s, or 640 ms at 2.5 GT/s at 100% bus utilization
Time Stamp Range	292 hours
Time Stamp	50 bits at 936 ps resolution
Clocking/Acquisition Modes	TLA module without SSC (Spread Spectrum Clocking) , External Reference Clock (100 MHz ±10%) with or without SSC
External reference clock frequency tolerance	±300 ppm
Number of Mainframe Instrument Slots Required per TLA Series Module	2

Module Configuration Requirements

Module	Bi-Directional Link Width			
	X1	X4	X8	X16
TLA7SA08	1	1	0	0
TLA7SA16	1	1	1	2

Input Characteristics (with P67SA00 Series probes)

Characteristic	Description
Capacitive Loading	See P67SA00 Series Probe Manual
Minimum Data Eye	See P67SA00 Series Probe Manual

Acquisition Characteristics (with P67SA00 Series probes)

Characteristic	Description
Dynamic Link-width Switch Latency	Consumes up to 48 symbols (typical)
Dynamic Link-rate Switch Latency	<200 ns EIDLE time (typical) (with either internal reference clock or spread spectrum using external reference clock)
Maximum time to change to Gen1 rate	2 TS1
Maximum time to change to Gen2 rate	1 EIEOS + 3 TS1
Maximum time to change to Gen3 rate	1 EIEOS + 6 TS1
Number of FTS Packets Required to Re-sync Following L0s Exit	Gen1*[1]: 4 FTS (typical) Gen2*[1]: 1 EIEOS + 6 FTS (typical) Gen3*[1]: 1 EIEOS + 4 FTS (typical)

*[1] Assumes an EIDLE ranging from 20 ns to 2 ms, with either internal reference clock or spread spectrum using external reference clock.

Filter Characteristics

Characteristic	Description
Ordered Sets	TS1, TS2, SKP, EIOS, FTS, EIEOS, SDS
DLLPs	Ack, Nak, PM, Vendor Specific, FC1, FC2, UpdateFC
TLPs	MRd, MRdL, MWr, IORd, IOWr, CfgRd0, CfgWr0, CfgRd1, CfgWr1, Msg, MsgD, Cpl, CplD, CPlLk, CPlDLk, FetchAdd, Swap, CAS, LPrfx, EPrfx

Trigger Characteristics

Characteristic	Description
Independent Trigger States	8
Trigger Sequencer Rate	Operates at symbol rate time (Gen1, Gen2, Gen3)
Maximum Independent If/Then Clauses per State	8
Maximum Number of Events per If/Then Clause	8
Maximum Number of Actions per If/Then Clause	8
Maximum Number of Event Counters per State	2
Event Counter Range	31 bit
Number of TLP Packet Recognizers per Link Direction	4
Number of DLLP Packet Recognizers per Link Direction	4
Number of Sequence Recognizers	4
Number of Symbols per Sequence Recognizer	16
Number of Link Event Recognizers	4
Number of Global Counters/Timers	4
Trigger Event Types	Anything, TLP, DLLP, Sequence, Link Event, Counter, Timer
Trigger Action Types	Trigger, Trigger All Modules, Wait for System Trigger, Goto, Increment Counter, Decrement Counter, Reset Counter, Start Timer, Reset Timer, Reset and Start Timer, Stop Timer, Reset and Stop Timer, Set Signal Out, Clear Signal Out, Arm Module, Start Storage, Stop Storage, Do Nothing
Counter/Timer Range	48 bit (~5 days with 3.6 ns resolution)
Counter/Timer Test Latency	68 ns
Storage Control (Data qualification)	By state (start/stop)

Physical Characteristics

	TLA7SA16		TLA7SA08	
Dimensions	**mm**	**in.**	**mm**	**in.**
Height	262	10.3	262	10.3
Width	61	2.4	61	2.4
Depth	381	15	381	15
Weight	**kg**	**lb.**	**kg**	**lb.**
Net	3.20	7.06	2.84	6.25
Shipping	7.30	16.1	6.94	15.3

Ordering Information

TLA7012

Portable Logic Analyzer Mainframe, holds two TLA modules.
Includes: Mini Keyboard (119-7275-xx), Optical Wheel Mouse (119-7054-xx), Front-panel cover (200-4939-xx), One dual-wide panel filler for empty slots (333-4206-xx), TLA Application Software CD (063-3881-xx), Certificate of Traceable Calibration.
Note: Please specify power cord, language, and service options when ordering.

TLA7012 Options

Option	Description	Order Number
Opt. 18	Add touch screen	N/A
Opt. 1C	Add GPIB-iView™ external oscilloscope interface kit (requires TLA Application SW V5.0 or greater)	012-1614-xx
Opt. 2C	Add USB-iView external oscilloscope interface kit (requires TLA Application SW V5.8 or greater)	
Opt. PO	Add Accessory Pouch for TLA7012	016-1441-xx
Opt. TL	Add Teklink Cable	174-5019-xx
Opt. 1K	Add LACART logic analyzer cart	LACART
Opt. 88	Factory install of module	N/A

TLA7012 Optional Accessories

Order Number	Accessory
650-4815-xx	Additional Removable Hard Drive Assembly (no SW)
020-2664-xx	Rackmount Kit
016-1522-xx	Wheeled Transport Case

TLA7016

Benchtop Logic Analyzer Mainframe, holds six TLA modules.
Includes: Five (5) dual-wide panel fillers for empty slots (333-4206-xx), LAN cable, straight-through, RJ-45 (174-5225-xx), TLA Application Software CD (063-3881-xx), Certificate of Traceable Calibration.
Note: Please specify power cord, language, and service options when ordering.

TLA7016 Options

Option	Description	Order Number
Opt. 1C	Add GPIB-iView™ external oscilloscope interface kit (requires TLA Application SW V5.0 or greater)	012-1614-xx
Opt. 2C	Add USB-iView external oscilloscope interface kit (requires TLA Application SW V5.8 or greater)	N/A
Opt. TL	Add Teklink Cable	174-5019-xx
Opt. BTB	Add Benchtop System Mounting Brackets	407-5127-xx (Left) 407-5132-xx (Right)
Opt. 1K	Add K4000 logic analyzer cart	K4000
Opt. 88	Factory install of module	N/A

TLA7016 Optional Accessories

Order Number	Accessory
020-2369-xx	Rackmount Kit
016-1651-xx	Wheeled Transport Case

TL708EX

TekLink™ 8-port Instrument Hub and Expander (Used for connecting 3-to-8 TLA7012 or TLA7016 mainframes).
Includes: Instruction sheet (071-1765-xx, English only).
Note: Please specify power cord and service options when ordering.

TLA7000 Series Power Cord Options

Option	Description
Opt. A0	North America power
Opt. A1	Universal Euro power
Opt. A2	United Kingdom power
Opt. A3	Australia power
Opt. A4	240 V, North America power
Opt. A5	Switzerland power
Opt. A6	Japan power
Opt. A10	China power
Opt. A11	India power
Opt. A12	Brazil power
Opt. A99	No power cord or AC adapter

TLA7000 Series Language Options

Option	Description
Opt. L0	English Manual
Opt. L5	Japanese Manual
Opt. L10	Russian Manual
Opt. L99	No Manual

TLA7000 Series Installation Service

Option	Description
LAINSTAL-SM	Installation of single mainframe and up to 3 modules or 1 to 3 modules in existing mainframe
LAINSTAL-LG	Installation of single mainframe and 4 to 6 modules

Gigabit LAN (GbE) Switch

Order Number	Description
020-2666-xx	16-port Gigabit LAN (GbE) Switch with U.S. Standard (120 V, 60 Hz) Power Cord

Power Cords for Gigabit LAN (GbE) Switch

Order Number	Description
161-0066-00	Power Cord, IEC320 C13, North American, Straight
161-0066-09	Power Cord, IEC320 C13, Universal Euro, Straight
161-0066-10	Power Cord, IEC320 C13, Universal Euro, Straight
161-0066-11	Power Cord, IEC320 C13, Australian, Straight
161-0066-12	Power Cord, IEC320 C13, North American, Straight
161-0154-00	Power Cord, IEC320 C13, Switzerland, Straight
161-0298-00	Power Cord, IEC320 C13, Japan, Straight
161-0304-00	Power Cord, IEC320 C13, China, Straight

TLA7ACx Modules

Includes: Certificate of calibration, and one-year warranty (return to Tektronix).
Note: Probes must be ordered separately.

TLA7ACx Logic Analyzer Modules

Module	Description
TLA7AC2	68-channel Logic Analyzer module, 8 GHz timing, 235 MHz state, 2 Mb record length. Options for up to 128 Mb record length and/or up to 450 MHz state
TLA7AC3	102-channel Logic Analyzer module, 8 GHz timing, 235 MHz state, 2 Mb record length. Options for up to 128 Mb record length and/or up to 450 MHz state
TLA7AC4	136-channel Logic Analyzer module, 8 GHz timing, 235 MHz state, 2 Mb record length. Options for up to 128 Mb record length and/or up to 450 MHz state

TLA7ACx Module Options

Base configuration is 2 Mb record length at 235 MHz state with basic Analog Multiplexer capability.

Option	Description
Opt. 1S	Increase to 8 Mb Record Length at 235 MHz State
Opt. 2S	Increase to 32 Mb Record Length at 235 MHz State
Opt. 3S	Increase to 128 Mb Record Length at 235 MHz State
Opt. 4S	Increase to 2 Mb Record Length at 450 MHz State
Opt. 5S	Increase to 8 Mb Record Length at 450 MHz State
Opt. 6S	Increase to 32 Mb Record Length at 450 MHz State
Opt. 7S	Increase to 128 Mb Record Length at 450 MHz State
Opt. AM	Enable Full Analog Multiplexer
Opt. 88	Factory Install

TLA7ACx Language Options

Option	Description
Opt. LG1	Global Manual
Opt. L99	No Manual

Please refer to the Service section at the rear of this document for details about Calibration and Repair options.

TLA7BBx Modules

Includes: Certificate of calibration, and one-year warranty (return to Tektronix).
Note: Probes must be ordered separately.

TLA7BBx Logic Analyzer Modules

Module	Description
TLA7BB2	68-channel Logic Analyzer module, 50 GHz MagniVu timing, 750 MHz state clock, 2 Mb record length. Options for up to 64 Mb record length and/or up to 1.4 GHz state clock
TLA7BB3	102-channel Logic Analyzer module, 50 GHz MagniVu timing, 750 MHz state clock, 2 Mb record length. Options for up to 64 Mb record length and/or up to 1.4 GHz state clock
TLA7BB4	136-channel Logic Analyzer module, 50 GHz MagniVu timing, 750 MHz state clock, 2 Mb record length. Options for up to 64 Mb record length and/or up to 1.4 GHz state clock

TLA7BBx Module Options

Base configuration is 2 Mb record length at 750 MHz state clock with full Analog Multiplexer capability.

Option	Description
Opt. 1S	Increase to 4 Mb Record Length at 750 MHz State Clock
Opt. 2S	Increase to 8 Mb Record Length at 750 MHz State Clock
Opt. 3S	Increase to 16 Mb Record Length at 750 MHz State Clock
Opt. 4S	Increase to 32 Mb Record Length at 750 MHz State Clock
Opt. 5S	Increase to 64 Mb Record Length at 750 MHz State Clock
Opt. 6S	Increase to 2 Mb Record Length at 1.4 GHz State Clock
Opt. 7S	Increase to 4 Mb Record Length at 1.4 GHz State Clock
Opt. 8S	Increase to 8 Mb Record Length at 1.4 GHz State Clock
Opt. 9S	Increase to 16 Mb Record Length at 1.4 GHz State Clock
Opt. AS	Increase to 32 Mb Record Length at 1.4 GHz State Clock
Opt. BS	Increase to 64 Mb Record Length at 1.4 GHz State Clock
Opt. 88	Factory Install

TLA Series Module Upgrades

Please refer to the Service section at the rear of this document for details about Calibration and Repair options.

TLA7BBx Customer Deskew Fixture

Option	Description
020-2942-00	TLA7BBx Customer Deskew Fixture for P6800 Series Probes
020-2940-00	TLA7BBx Customer Deskew Fixture for P6900 Series Probes

TLA7BBx Language Options

Option	Description
Opt. L0	English Manual
Opt. L5	Japanese Manual
Opt. L10	Russian Manual
Opt. L99	No Manual

TLA7SAxx PCI Express Logic Protocol Analyzer Modules

Includes: Statement of Compliance, one-year warranty (return to Tektronix), reference clock cable (672-6285-xx), and reference clock jumper cable (174-5392-xx).
Note: Probes, mainframes, and software must be ordered separately.

Module	Description
TLA7SA16	16 Differential Inputs, x8 Logic Protocol Analyzer module, 8 GT/s acquisition, 8 GB physical memory
TLA7SA08	8 Differential Inputs, x4 Logic Protocol Analyzer module, 8 GT/s acquisition, 4 GB physical memory

TLA7SAxx PCI Express Software

Software	Description
TMS160PCIE3	TLA protocol software for PCIe 3.0

Logic Analyzer TLA7SAxx Module Options

Option	Description
Opt. 88	Factory Install
Opt. L0	English Manual
Opt. L5	Japanese Manual
Opt. L10	Russian Manual
Opt. L99	No Manual

Service Options

The following service options are offered for the TLA logic analyzer products.

Option	TLA7000 Mainframes	TL7ACx Modules	TLA7BBx Modules	TLA7SAxx Modules
Opt. C3 Calibration Service 3 Years	X	X	X	X
Opt. C5 Calibration Service 5 Years	X	X	X	X
Opt. D1 Calibration Data Report	X	X	X	
Opt. D3 Calibration Data Report 3 Years (with Opt. C3)	X	X	X	
Opt. D5 Calibration Data Report 5 Years (with Opt. C5)	X	X	X	
Opt. G3 Complete Care 3 Years (includes loaner, scheduled calibration and more). TLA7012, TLA7BB2, TLA7BB3, TLA7BB4, TLA7S08, TLA7S16 only			X	X
Opt. G5 Complete Care 5 Years (includes loaner, scheduled calibration and more). TLA7012, TLA7BB2, TLA7BB3, TLA7BB4, TLA7S08, TLA7S16 only			X	X
Opt. R3 Repair Service 3 Years	X	X	X	X
Opt. R5 Repair Service 5 Years	X	X	X	X
Opt. S1 On-site Service 1 Year	X			
Opt. S3 On-site Service 3 Years (with R or C options)	X			
Opt. R3DW Repair Service Coverage 3 Years (includes product warranty period). 3-year period starts at time of instrument purchase	X	X	X	X
Opt. R5DW Repair Service Coverage 5 Years (includes product warranty period). 5-year period starts at time of instrument purchase	X	X	X	X

TLA7000 Series Upgrades

You can add new capabilities to your existing TLA mainframe or increase the state speed, memory depth, or add full analog multiplexer capability (TLA7ACx only) to existing TLA modules by ordering the appropriate upgrade kit. Please refer to the TLA Family Upgrade Guide for further details.

CE

Tektronix is registered to ISO 9001 and ISO 14001 by SRI Quality System Registrar.

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Updated 10 February 2011

For Further Information. Tektronix maintains a comprehensive, constantly expanding collection of application notes, technical briefs and other resources to help engineers working on the cutting edge of technology. Please visit **www.tektronix.com**

02 Oct 2011 52W-15053-15