

DA-3GHD-8-MkII

1x8 non-inverting 3GHD-SDI and ASI Distribution Amplifier

User manual

Rev. A



Nevion Support

Nevion Europe

Nevion USA

P.O. Box 1020 3204 Sandefjord, Norway Support phone 1: +47 33 48 99 97 Support phone 2: +47 90 60 99 99 1600 Emerson Avenue Oxnard, CA 93033, USA Toll free North America: (866) 515-0811 Outside North America: +1 (805) 247-8560

E-mail: support@nevion.com

See http://www.nevion.com/support/ for service hours for customer support globally.

Revision history

Current revision of this document is the uppermost in the table below.

Rev.	Repl.	Date	Sign	Change description
Α	-	2015-05-21	MR	Initial version

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1 Product overview

The Flashlink DA-3GHD-8-MkII is a multi bit-rate distribution amplifier module providing high performance media distribution for various signal formats from 19.4Mbps up to 2970Mbps. The unit can be configured to do cable equalizing and reclocking of SMPTE 424M, SMPTE 292 and SMPTE 259M signal formats.

The product provides 8 reclocked non-inverting outputs. It will detect 3G/HD and SD rates and automatically switch to correct output slew-rate. The reclocker supports the bit-rates 270Mbps, 1483.5Mbps, 1485Mbps, 2967Mbps and 2970Mbps. For other rates the reclocker can automatically switch to bypass mode and DA-3GHD-8-MkII will work as a non-reclocking distribution amplifier with cable equalization. DA-3GHD-8 also supports reclocking of DVB-ASI at 270Mbps, enabling all possible rates including empty transport streams with only K28.5 padding packets. All 8 outputs are non-inverting and suitable for DVB-ASI.

DA-3GHD-8-MkII is designed for all distribution purposes in studio, duplication and Broadcast applications.

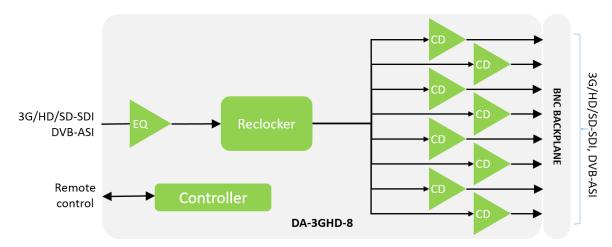


Figure 1: DA-3GHD-8-MkII

2 Specifications

2.1 Electrical Outputs

Number of outputs

75 Ohm BNC Connectors

Output Return loss < -15dB, 5MHz -1.5GHz < -10dB, 1.5GHz - 3GHz

Output signal level 800mV +/- 10%

Output signal rise / fall time

SD limit: [0.4ns – 1.5ns]; <0.5ns rise/fall var. 20% - 80% HD limit: < 270ps, <100ps rise/fall var.

3G HD limit: <135ps, <50ps rise/fall var.

Amplitude overshoot <10%

Non-inverting **Polarity** Output timing jitter SD: <0.2 UI

HD: <1 UI 3G HD: <1UI SD: <0.15 UI

Output alignment jitter HD: <0.15 UI 3G HD: <0.2UI

2.2 Electrical Inputs

Number of inputs 1

75 Ohm BNC Connectors

Input Return loss < -15dB, 5MHz -1.5GHz

< -10dB, 1.5GHz - 3GHz

Jitter tolerance SD limit:

> 10Hz-10kHz: >1 UI 10kHz-10MHz: >0.2 UI

HD limit:

10Hz-100kHz: >1 UI 100kHz-150MHz: >0.2 UI

3G HD limit:

- 10Hz-100kHz: >2 UI 100kHz-300MHz: >0.3 UI

	Cable equalization, DA-3GHD-8-MkII.			
Format	Min.	Typical	Comments	
SD-SDI	325m		Belden 8281	
		375m	BER< 10E-12	
			Total length of cable	
			included patching between	
			modules	
HD-SDI	170m		Belden 1694A	
		190m	BER< 10E-12	
3GHD-SDI	80m		Total length of cable	
		100m	included patching between	
			modules	

2.3 Features

Re-clocking: Automatic SD, HD, 3G detection

Automatic output slew rate adjustment according to SMPTE-259M and SMPTE-292M/ SMPTE424M

Supported clock rates: 270, 1483.5, 1485, 2967, 2970Mbps

Input equalizer: Eq. bypass for non-video formats or low bit rates

2.4 Supported standards

SMPTE: SMPTE424M, SMPTE292M, SMPTE259M, SMPTE305M,

SMPTE310M

DVB-ASI: EN50083-9

2.5 General

DC power consumption: +5V / 1.4W

3 Configuration

The DA-3GHD-8 supports a number of different formats. The correct configuration can either be set with a DIP switch or with GYDA Control System. The layout of the main module is shown in the drawing below with the DIP switch to the upper left position.

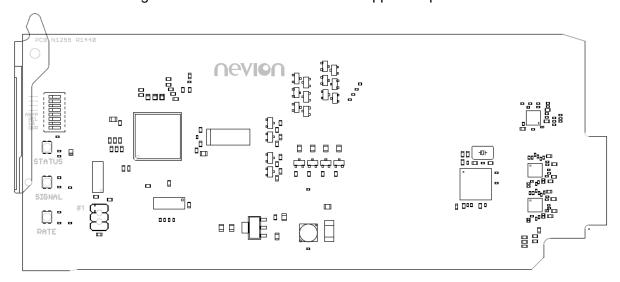


Figure 2: DA-3GHD-8-MkII module layout

DIP switch configuration must be set according to Table 1:

Switch #	Label	Function DIP=OFF	Function DIP=ON	Comment
1				
2				
3				
4	CD	Cable detect OFF	Cable detect ON	Cable driver function for extended cable length
5	ABYP	No auto bypass	Reclocker bypass if unsupported bitrate	Auto bypass of reclocker
6	RCL	Reclocker Bypass	Reclocker ON	Reclocker mode
7	EQ	Cable equalizer Bypass	Cable equalizer ON	Equalizer mode
8	OVR	GYDA control Config. with GYDA	Override GYDA control Config. with DIP switch	Select GYDA config. mode

Table 1: DA-3GHD-8-mkll DIP switches

All DIP switches are off when pointing towards the release handle.

3.1 Configuration Examples

Typical configurations for DA-3GHD-8-mkII:

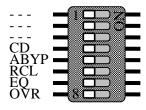


Figure 3: Default all off; Gyda controls the card

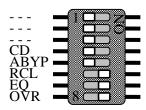


Figure 4: DIP control; Equalizing and reclocking turned on



Figure 5: Same as above, but if the input signal is something else than the supported bitrates, the reclocker will automatically enter bypass mode

4 Connections

The backplane layout is shown in Figure 6.

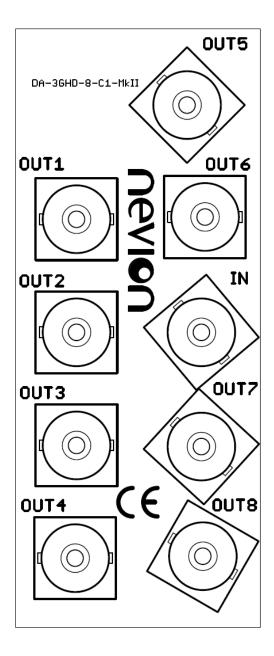


Figure 6: Layout of the backplane DA-3GHD-8-C1-MkII

The electrical input signal is connected to the IN BNC. All OUT1 to OUT8 BNC's provide non-inverted signals and can be used for all formats, included DVB-ASI. Unused outputs should be terminated with 75ohm.

5 Operation

The status of the module can be easily monitored visually by LED's at the front of the module. The LED's are visible through the front panel as shown in Figure 10.

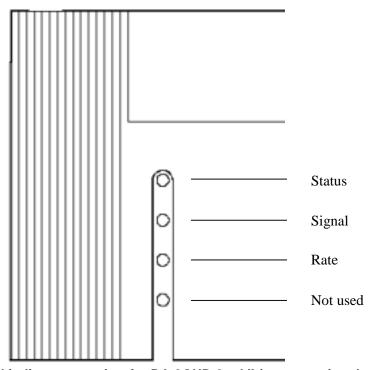


Figure 7: Panel indicator overview for DA-3GHD-8-mkll (text not printed on the front panel).

The functions of the different LED's are described in Table 2.

Diode \ state	Red LED	Yellow LED	Green LED	No light
Status	Module is faulty		Module is OK Module has power	Module has no power
Signal	No input signal	EQ bypassed or muted	Input signal present	
Rate	Rate not detected	Recl. bypassed	Reclocker locked	
Fourth LED not used				

Table 2: LED status description

General environmental requirements for Nevion equipment

1. The equipment will meet the guaranteed performance specification under the following environmental conditions:

- Operating room temperature 0°C to 50°C

range:

- Operating relative humidity range: <90% (non-condensing)

2. The equipment will operate without damage under the following environmental conditions:

- Temperature range: -5°C to 55°C

- Relative humidity range: <95% (non-condensing)

Product Warranty

The warranty terms and conditions for the product(s) covered by this manual follow the General Sales Conditions by Nevion, which are available on the company web site:

www.nevion.com

Appendix A Materials declaration and recycling information

A.1 Materials declaration

For product sold into China after 1st March 2007, we comply with the "Administrative Measure on the Control of Pollution by Electronic Information Products". In the first stage of this legislation, content of six hazardous materials has to be declared. The table below shows the required information.

	Toxic or hazardous substances and elements					
組成名稱 Part Name	鉛 Lead (Pb)	汞 Mercury (Hg)	镉 Cadmium (Cd)	六价铬 Hexavalent Chromium (Cr(VI))	多溴联苯 Polybrominated biphenyls (PBB)	多溴二苯醚 Polybrominated diphenyl ethers (PBDE)
DA-3GHD-8-MkII	0	0	0	0	0	0
<power delivered="" if="" supply,="" unit="" with=""></power>	0	0	0	0	0	0

O: Indicates that this toxic or hazardous substance contained in all of the homogeneous materials for this part is below the limit requirement in SJ/T11363-2006.

This is indicated by the product marking:



A.2 Recycling information

Nevion provides assistance to customers and recyclers through our web site http://www.nevion.com/. Please contact Nevion's Customer Support for assistance with recycling if this site does not show the information you require.

Where it is not possible to return the product to Nevion or its agents for recycling, the following general information may be of assistance:

- Before attempting disassembly, ensure the product is completely disconnected from power and signal connections.
- All major parts are marked or labeled to show their material content.
- Depending on the date of manufacture, this product may contain lead in solder.
- Some circuit boards may contain battery-backed memory devices.

X: Indicates that this toxic or hazardous substance contained in at least one of the homogeneous materials used for this part is above the limit requirement in SJ/T11363-2006.