SAMSUNG ELECTRONICS

USER'S MANUAL

S3F84NB

8-BIT CMOS MICROCONTROLLERS

Dec, 2007

REV 1.00

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REVISION HISTORY

Revision No	Description of Change	Refer to	Author(s)	Date
0.00	Preliminary Spec for internal release only	–	–	Aug, 2006
1.00	First revision	–	HwiTaek. Chung	Dec, 2007

REVISION DESCRIPTIONS FOR REVISION 1.00

Chapter		Subjects (Major changes comparing with last version)
Chapter Name	**Page**	
01. Product Overview	1-3	'Operating Voltage Range' is changed form '2.0 V to 5.5 V at 10MHz fOSC (LVR disabled) ' to '2.0 V to 5.5 V @ 1-4MHz (LVR disabled)' and '3.0 to 5.5 V @ 1-10MHz'.
02. Address Space	2-3	Figure 2-2 Smart Option: LVR level is changed from 3.9V to 4.0V when 'LVR Level Selection Bits' is set to '01'. Modified default LVR state from 'enable' to 'disable'.
	2-20	Added sentence 'However, if an overflow or underflow condition occurs as a result of increasing or decreasing the stack address value in the SPL register during normal stack operations, the value in the SPL register will overflow (or underflow) to the SPH register, overwriting any other data that is currently stored there. To avoid overwriting data in the SPH register, you can initialize the SPL value to "FFH" instead of "00H".'
04. Control Registers	4-6	Modified ADCON.7 to be 'Keep Always Logic 0'.
05. Interrupt Structure	5-11	Added a note in Figure 5-6.
15. A/D Converter	15-2	Modified ADCON.7 to be 'Keep Always Logic 0'.
19. Embedded Flash Memory Interface	19-4	Figure 19-2 Smart Option: LVR level is changed from 3.9V to 4.0V when 'LVR Level Selection Bits' is set to '01'.
20. Electrical Data	20-4	Changed the pull-up resistor value to 50kΩ in Table 20-3.
	20-8	Deleted the 'strong mode' in Table 20-8.

Preface

The S3F84NB *Microcontroller User's Manual* is designed for application designers and programmers who are using the S3F84NB microcontroller for application development. It is organized in two main parts:

Part I Programming Model

Part II Hardware Descriptions

Part I contains software-related information to familiarize you with the microcontroller's architecture, programming model, instruction set, and interrupt structure. It has six chapters:

Chapter 1	Product Overview	Chapter 4	Control Registers
Chapter 2	Address Spaces	Chapter 5	Interrupt Structure
Chapter 3	Addressing Modes	Chapter 6	Instruction Set

Chapter 1, "Product Overview," is a high-level introduction to S3F84NB with general product descriptions, as well as detailed information about individual pin characteristics and pin circuit types.

Chapter 2, "Address Spaces," describes program and data memory spaces, the internal register file, and register addressing. Chapter 2 also describes working register addressing, as well as system stack and user-defined stack operations.

Chapter 3, "Addressing Modes," contains detailed descriptions of the addressing modes that are supported by the S3F8-series CPU.

Chapter 4, "Control Registers," contains overview tables for all mapped system and peripheral control register values, as well as detailed one-page descriptions in a standardized format. You can use these easy-to-read, alphabetically organized, register descriptions as a quick-reference source when writing programs.

Chapter 5, "Interrupt Structure," describes the S3F84NB interrupt structure in detail and further prepares you for additional information presented in the individual hardware module descriptions in Part II.

Chapter 6, "Instruction Set," describes the features and conventions of the instruction set used for all S3F8-series microcontrollers. Several summary tables are presented for orientation and reference. Detailed descriptions of each instruction are presented in a standard format. Each instruction description includes one or more practical examples of how to use the instruction when writing an application program.

A basic familiarity with the information in Part I will help you to understand the hardware module descriptions in Part II. If you are not yet familiar with the S3F8-series microcontroller family and are reading this manual for the first time, we recommend that you first read Chapters 1–3 carefully. Then, briefly look over the detailed information in Chapters 4, 5, and 6. Later, you can reference the information in Part I as necessary.

Part II "hardware Descriptions," has detailed information about specific hardware components of the S3F84NB microcontroller. Also included in Part II are electrical, mechanical data. It has 16 chapters:

Chapter 7	Clock Circuit	Chapter 15	A/D Converter
Chapter 8	RESET and Power-Down	Chapter 16	Watch Timer
Chapter 9	I/O Ports	Chapter 17	Pattern Generation Module
Chapter 10	Basic Timer	Chapter 18	Low Voltage Reset
Chapter 11	8-Bit Timer A/B/C (0, 1)	Chapter 19	Embedded Flash Memory Interface
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1 PRODUCT OVERVIEW

S3C8-SERIES MICROCONTROLLERS

Samsung's S3C8-series of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU, a wide range of integrated peripherals, and various mask-programmable ROM sizes. The major CPU features are:

- Efficient register-oriented architecture
- Selectable CPU clock sources
- Idle and Stop power-down mode released by interrupt or reset
- Built-in basic timer with watchdog function

A sophisticated interrupt structure recognizes up to eight-interrupt levels. Each level can have one or more interrupt sources and vectors. Fast interrupt processing (within a minimum of four CPU clocks) can be assigned to specific interrupt levels.

S3F84NB MICROCONTROLLER

The S3F84NB single-chip CMOS microcontrollers are fabricated using the highly advanced CMOS process technology based on Samsung's latest CPU architecture.

The S3F84NB is a microcontroller with 64K-byte flash memory embedded.

Using a proven modular design approach, Samsung engineers have successfully developed the S3F84NB by integrating the following peripheral modules with the powerful SAM8 core:

- Seven programmable I/O ports, including seven 8-bit ports for a total of 56 pins.
- Fourteen bit-programmable pins for external interrupt.
- One 8-bit basic timer for oscillation stabilization and watchdog function (system reset).
- Four 8-bit timer/counter and two 16-bit timer/counter with selectable operating modes.
- Two asynchronous UART
- One synchronous SIO
- One Watch timer for real-time clock
- One Pattern generation Module
- 10-bit 8-channel A/D converter

The S3F84NB is versatile microcontroller for home appliances and ADC applications, etc. They are currently available in 64-pin QFP and 64-pin SDIP package.

FEATURES

CPU

- SAM8RC CPU core

Memory

- Program memory:
  - 64-Kbyte Internal Flash Memory
  - Sector size: 128Bytes
  - 10years data retention
  - Fast Programming Time: Sector Erase: 10ms
    Byte Program: 32us
  - Byte Programmable
  - User programmable by 'LDC' instruction
  - Sector (128-bytes) Erase available
  - External serial programming support
  - Endurance: 10,000 Erase/Program cycles
  - Expandable OBPTM (On Board Program)
- Data memory: 2064-byte general purpose RAM

Oscillation Sources.

- Crystal, or ceramic for main clock
- Crystal for sub clock (32.768 kHz)

Instruction Set

- 78 instructions.
- IDLE and STOP instructions added for power-down modes

Instruction Execution Time

- 400 ns at 10-MHz f_{OSC} (minimum)

Interrupts

- 29 interrupt sources with 29 vectors/8 levels.
- Fast interrupt processing feature

I/O Ports

- Total 56 bit-programmable pins.

8-Bit Basic Timer

- One programmable 8-bit basic timer for oscillation stabilization control
- Watchdog timer function

Timers

- 8-bit timer/counter (**Timer A**) with three operating modes; Interval mode, capture mode and PWM mode
- 8-bit timer/counter (**Timer B**) could also be used as a carrier frequency or PWM generator.
- 8-bit timer/counter (**timer C (0,1)**) with two operating modes; interval mode and PWM mode
- 16-bit timer/counter (**Timer 1(0,1)**) with three operating modes; Interval mode, Capture mode, and PWM mode..

Watch timer

- Interval Time: 3.19ms, 0.25s, 0.5s, 1.0s at 32.768 kHz
- 0.5/1/2/4 kHz buzzer output selectable

A/D Converter

- Eight-analog input channels
- 10-bit conversion resolution
- 20us conversion speed at 10MHz clock.

Asynchronous UART

- Programmable baud rate generator
- Supports serial data transmit/receive operations with 8-bit, 9-bit in UART module

Synchronous SIO

- 8-bit transmit/receive mode
- 8-bit receive mode
- Selectable baud rate or external clock source

Pattern Generation Module

- Pattern generation module triggered by timer match signal and Software.

Built-in RESET circuit (LVR)

- Low-Voltage detector for safe reset

Operating Temperature Range

- –40°C to + 85°C

Operating Voltage Range

- 2.0 V to 5.5 V @ 1-4MHz (LVR disabled)
- LVR to 5.5 V @ 1-4MHz (LVR enabled)
- 3.0 to 5.5 V @ 1-10MHz

Package Type

- 64 pin QFP, 64 pin SDIP

BLOCK DIAGRAM

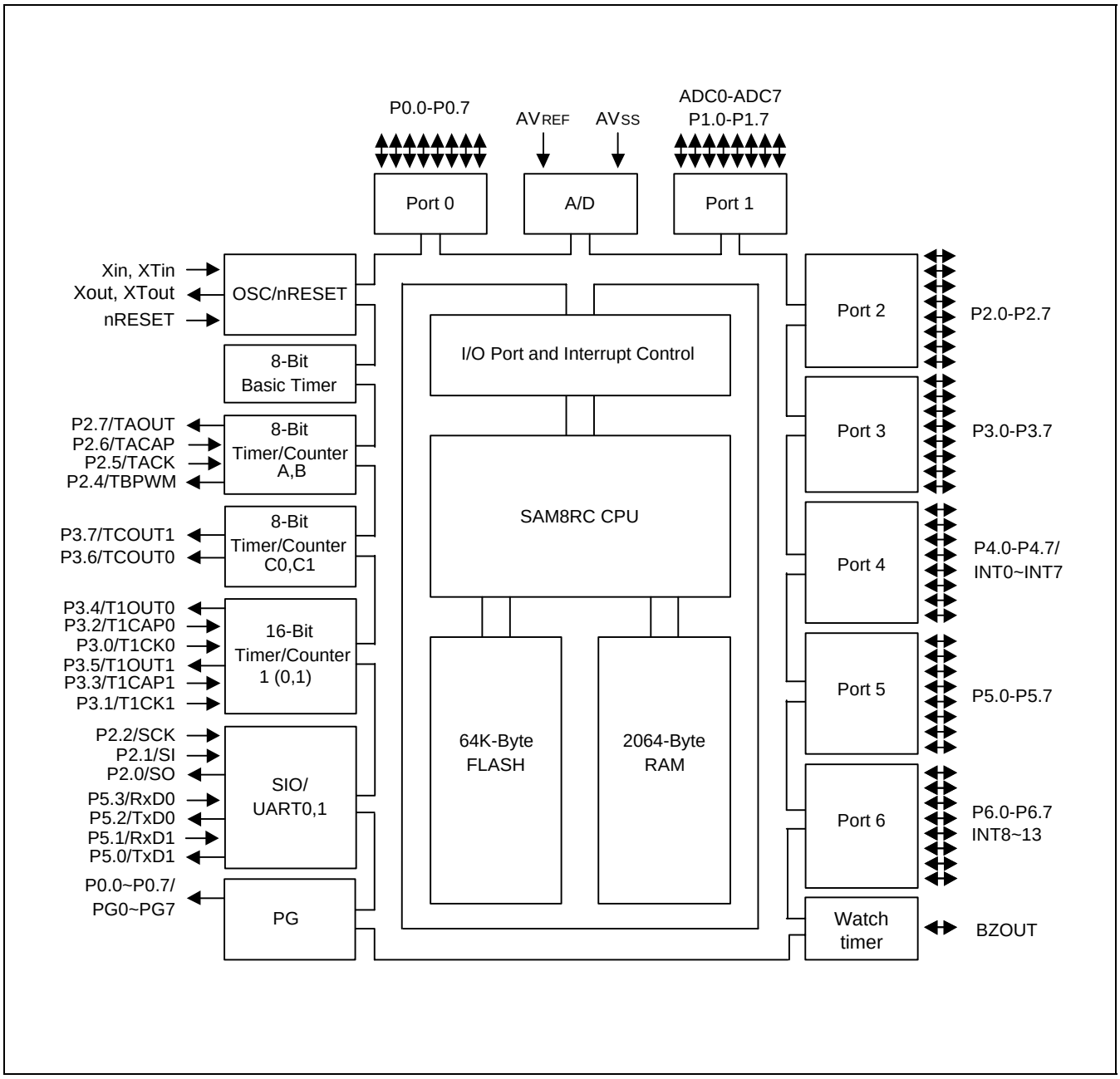


Figure 1-1. S3F84NB Block Diagram

PIN ASSIGNMENT

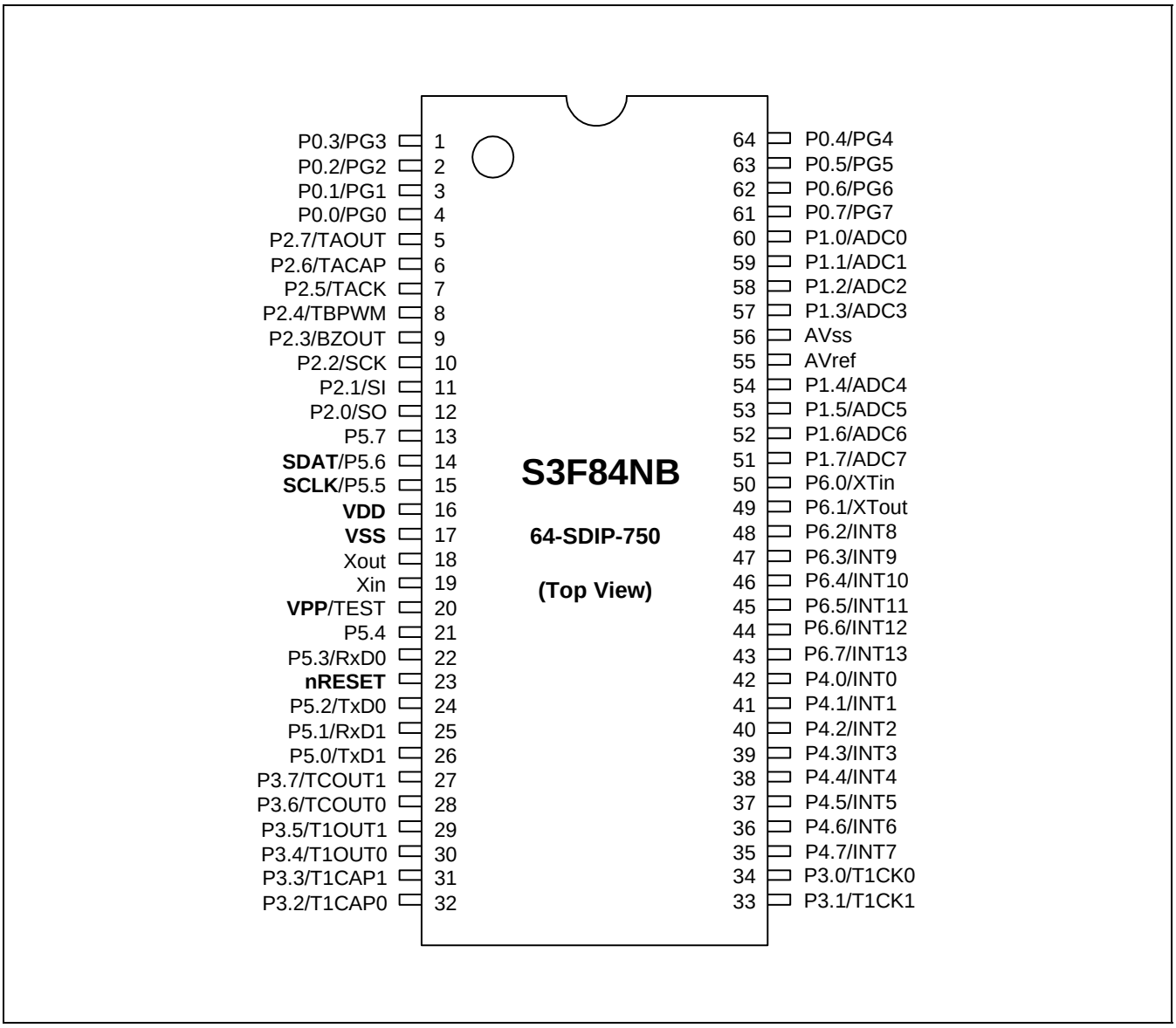


Figure 1-2. S3F84NB Pin Assignment (64-pin SDIP)

PIN ASSIGNMENT

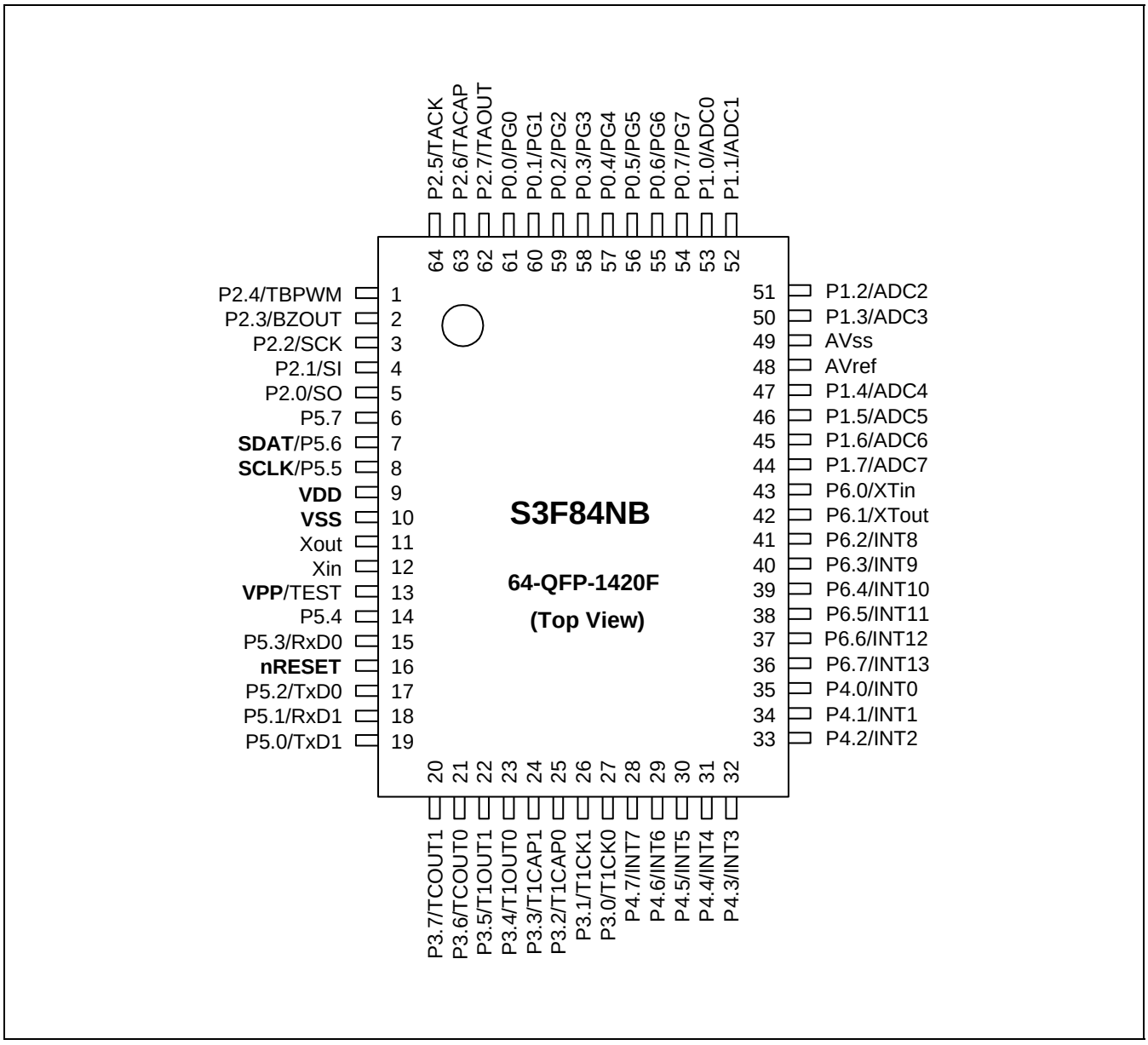


Figure 1-3. S3F84NB Pin Assignment (64-QFP)

PIN DESCRIPTIONS

Table 1-1. S3F84NB Pin Descriptions

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Number	Share Pins
P0.0–P0.7	I/O	Bit programmable port; input or output mode selected by software; input or push-pull output. Software assignable pull-up. Alternately, P0.0–P0.7 can be used as the PG output port (PG0–PG7).	D	1-4, 64-61 (61-54)	PG0–PG7
P1.0–P1.7	I/O	Bit programmable port; input or output mode selected by software; input or push-pull output. Software assignable pull-up. Alternatively used as analog input pins for A/D converter modules.	E	60-57, 54-51 (53-50, 47-44)	ADC0–ADC7
P2.0–P2.7	I/O	Bit programmable port; input or output mode selected by software; input or push-pull output. Software assignable pull-up. Alternately, P2.0~P2.7 can be used as I/O for TIMER A, TIMER B, SIO and Buzzer output.	D	12-5 (5-1, 64-62)	SO SI SCK BZOUT TBPWM TACK TACAP TAOUT
P3.0–P3.7	I/O	Bit programmable port; input or output mode selected by software; input or push-pull output. Software assignable pull-up. Alternately, P3.0~P3.7 can be used as I/O for TIMER C(0,1), TIMER 1(0,1)	D	34-27 (27-20)	T1CK0 T1CK1 T1CAP0 T1CAP1 T1OUT0 T1OUT1 TCOUT0 TCOUT1

NOTE: Pin numbers shown in parentheses “( )” are for the 64-pin QFP package.

Table 1-1. S3F84NB Pin Descriptions (64-SDIP) (Continued)

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Number	Share Pins
P4.0–P4.7	I/O	Bit programmable port; input or output mode selected by software; input or push-pull output. Software assignable pull-up. P4.0–P4.7 can alternately be used as inputs for external interrupts INT0–INT7, respectively (with noise filters and interrupt controller)	D-1	42-35 (35-28)	INT0–INT7
P5.0–P5.7	I/O	Bit programmable port; input or output mode selected by software; input or push-pull output. Software assignable pull-up. Alternately, P5.0–P5.3 can be used as I/O for serial port, UART0, UART1, respectively.	G	26-24, 22,21, 15-13 (19-17, 15,14,8-6)	TxD1 RxD1 TxD0 RxD0
P6.0–P6.7	I/O	P6.0, P6.1 are bit programmable port; input or output mode selected by software; input or push-pull output. Software assignable pull-up. P6.0 and P6.1 can alternately be used for subsystem oscillator in/out mode selected by software.	F	50-43 (43-36)	XT_{IN}, XT_{OUT}
		P6.2–P6.7 are bit programmable port; input or output mode selected by software; input or push-pull output. Software assignable pull-up. P6.2–P6.7 can alternately be used as inputs for external interrupts INT8–INT13, respectively (with noise filters and interrupt controller)	D-1		INT8–INT13

NOTE: Pin numbers shown in parentheses "( )" are for the 64-pin QFP package.

Table 1-1. S3F84NB Pin Descriptions (Continued)

Pin Name	Pin Type	Pin Description	Circuit Type	Pin Number	Share Pins
ADC0–ADC7	I	Analog input pins for A/D converter module. Alternatively used as general-purpose digital input/output port 1.	E	60-57, 54-51 (53-50, 47-44)	P1.0–P1.7
PG0–PG7	O	Pattern generator Output. Alternatively used as general-purpose digital input/output port 0.	D	4-1, 64-61 (61-54)	P0.0–P0.7
AVREF, AVSS	–	A/D converter reference voltage and ground	–	55, 56 (48,49)	–
RxD0, RxD1	I/O	Serial data RxD pin for receive input and transmit output (mode 0)	G	22, 25 (15,18)	P5.3, P5.1
TxD0, TxD1	O	Serial data TxD pin for transmit output and shift clock input (mode 0)	D	24, 26 (17,19)	P5.2, P5.0
TACK	I	External clock input pins for timer A	D	7(64)	P2.5
TACAP	I	Capture input pins for timer A	D	6(63)	P2.6
TAOUT	O	Pulse width modulation output pins for timer A	D	5(62)	P2.7
BZOUT	O	Buzzer output pin	D	9(2)	P2.3
TBPWM	O	Carrier frequency output pins for timer B	D	8(1)	P2.4
TCOUT0 TCOUT1	O	Timer C 8-bit PWM mode output or counter match toggle output pins	D	28,27 (21,20)	P3.6, P3.7
T1CK0 T1CK1	I	External clock input pins for timer 1	D	34,33 (27,26)	P3.0, P3.1
T1CAP0 T1CAP1	I	Capture input pins for timer 1	D	32,31 (25,24)	P3.2, P3.3
T1OUT0 T1OUT1	O	Timer 1 16-bit PWM mode output or counter match toggle output pins	D	30,29 (23,22)	P3.4, P3.5
SI, SO, SCK	I/O	Synchronous SIO pins	D	11,12,10 (4,5,3)	P2.1, P2.0, P2.2
nRESET	I	System reset pin (pull-up resistor: 240kΩ)	B	23(16)	–
TEST (V_{PP})	I	Pull-down resistor connected internally	–	20(13)	–
V_{DD}, V_{SS}	–	Power input pins	–	16,17 (9,10)	–
XT_{IN}, XT_{OUT}	I, O	Subsystem oscillator pins	F	50,49 (43,42)	P6.0, P6.1
X_{IN}, X_{OUT}	I,O	Main oscillator pins	–	19,18 (12,11)	–

NOTE: Pin numbers shown in parentheses "( )" are for the 64-pin QFP package.

PIN CIRCUITS

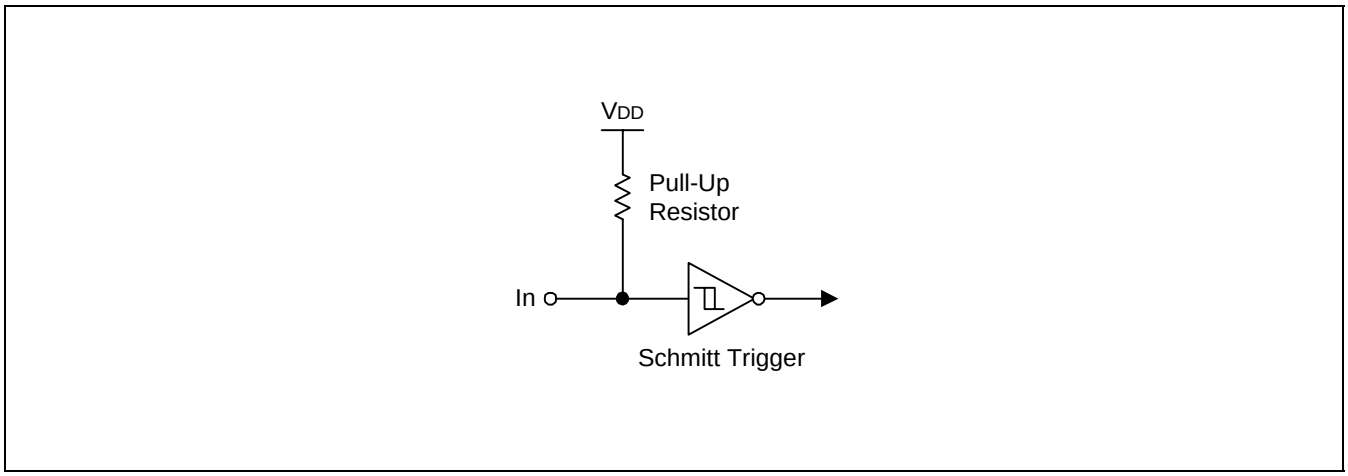


Figure 1-4. Pin Circuit Type B (nRESET)

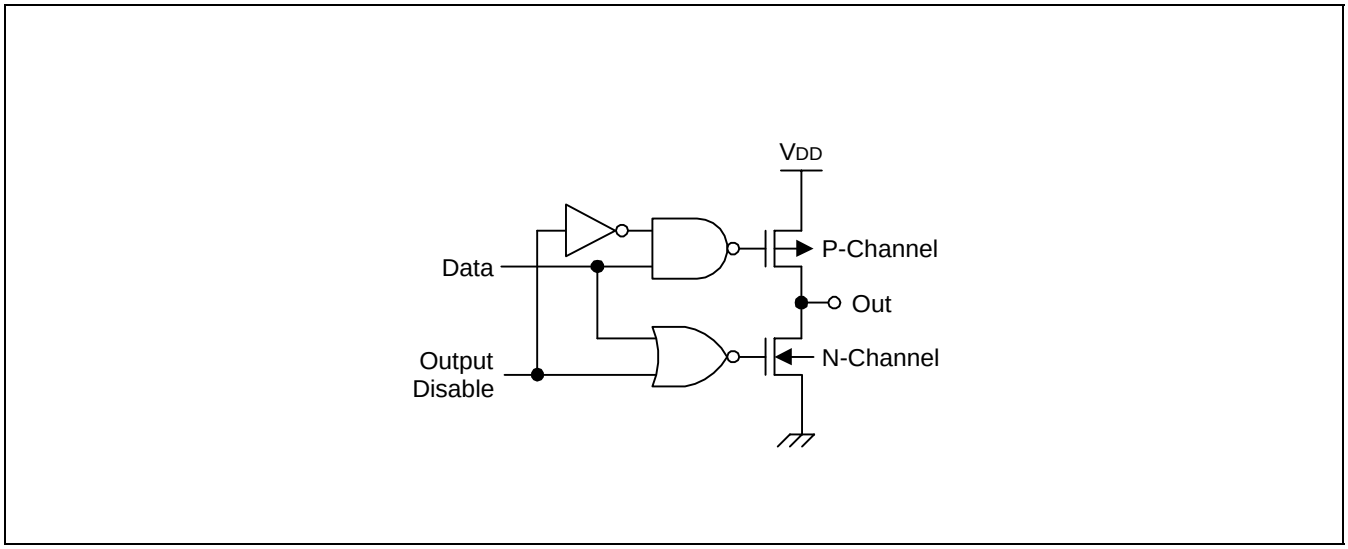


Figure 1-5. Pin Circuit Type C

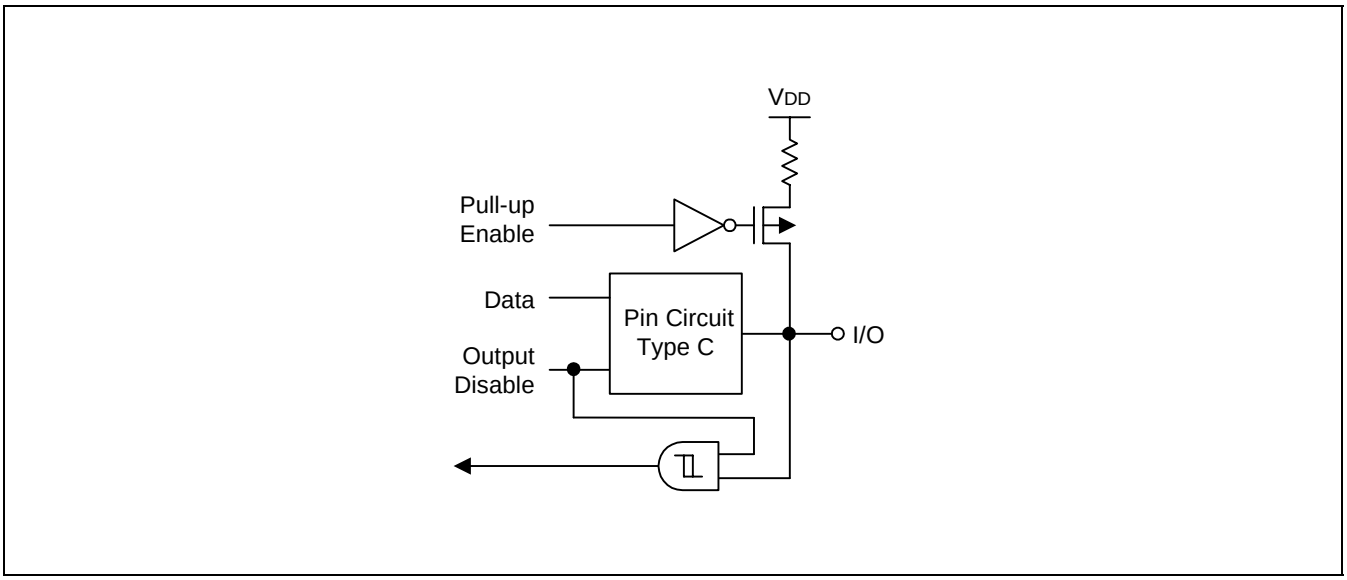


Figure 1-6. Pin Circuit Type D (Port 0, 2, 3 and P5.0-P5.3)

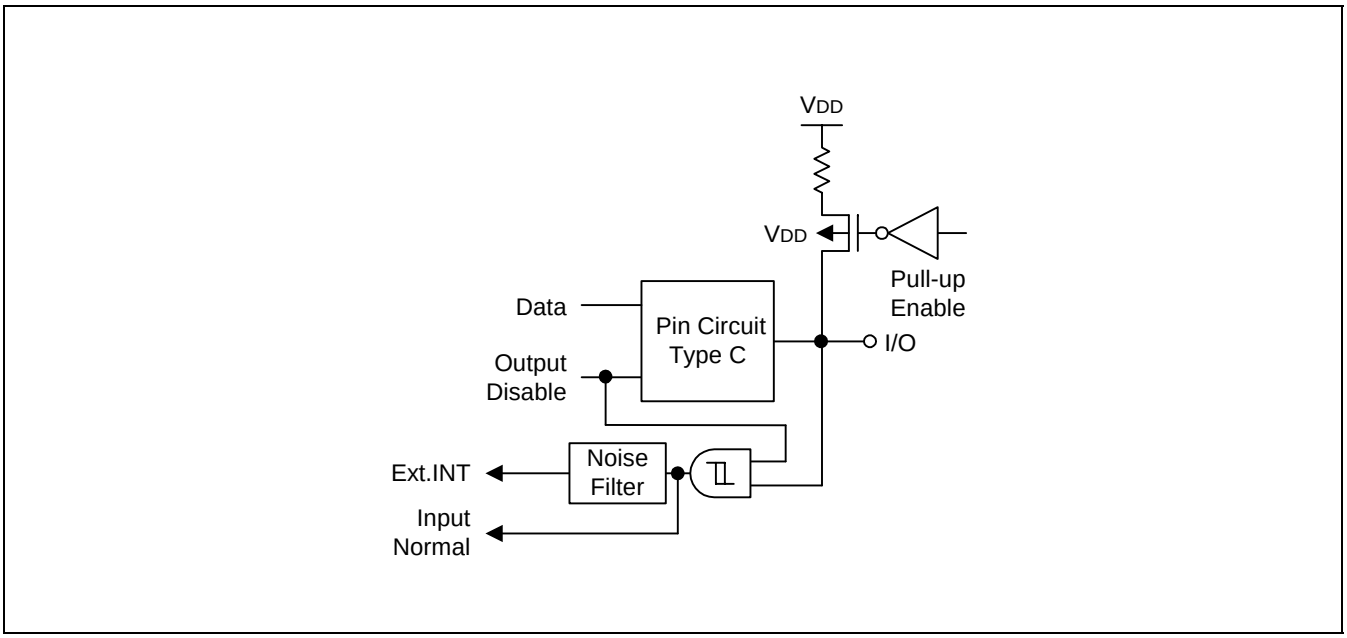


Figure 1-7. Pin Circuit Type D-1 (Port 4, and P6.2-P6.7)

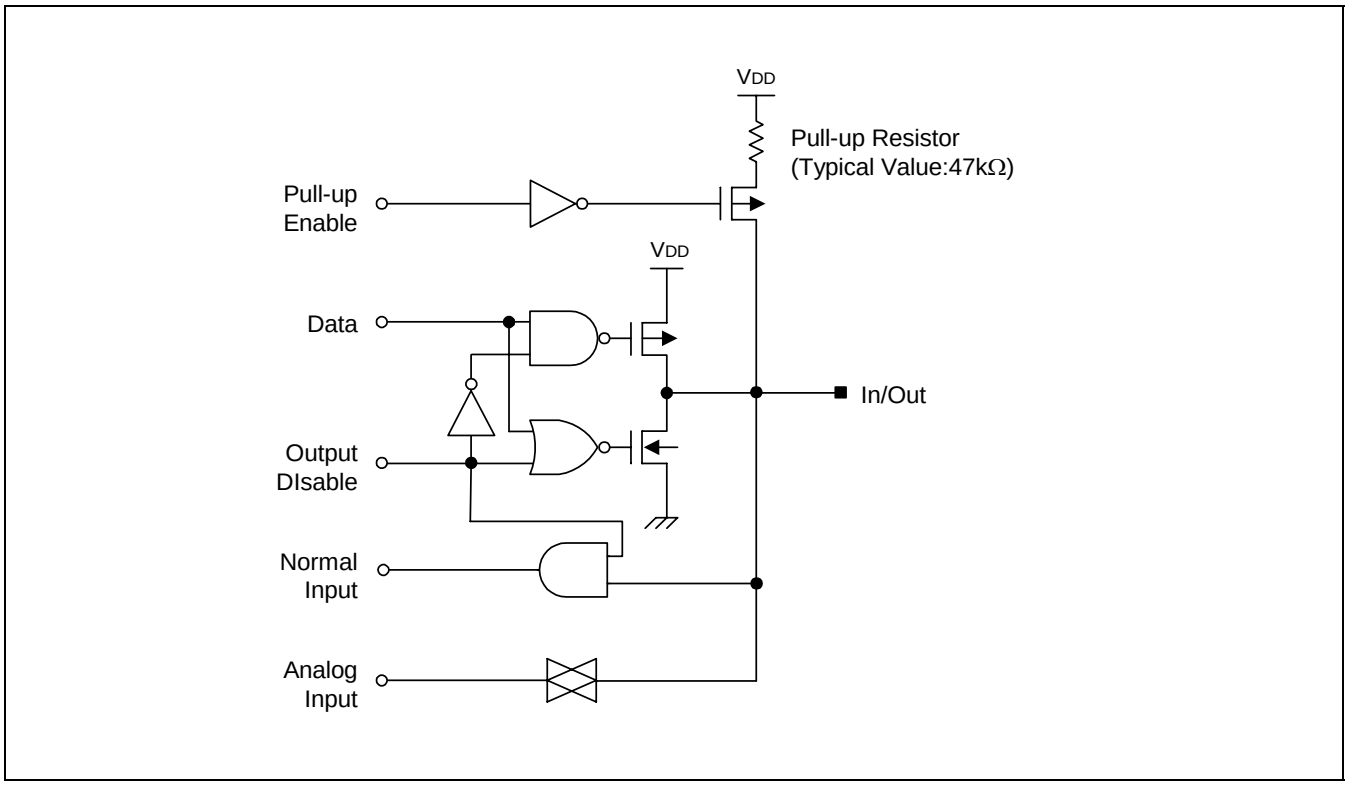


Figure 1-8. Pin Circuit Type E (Port 1)

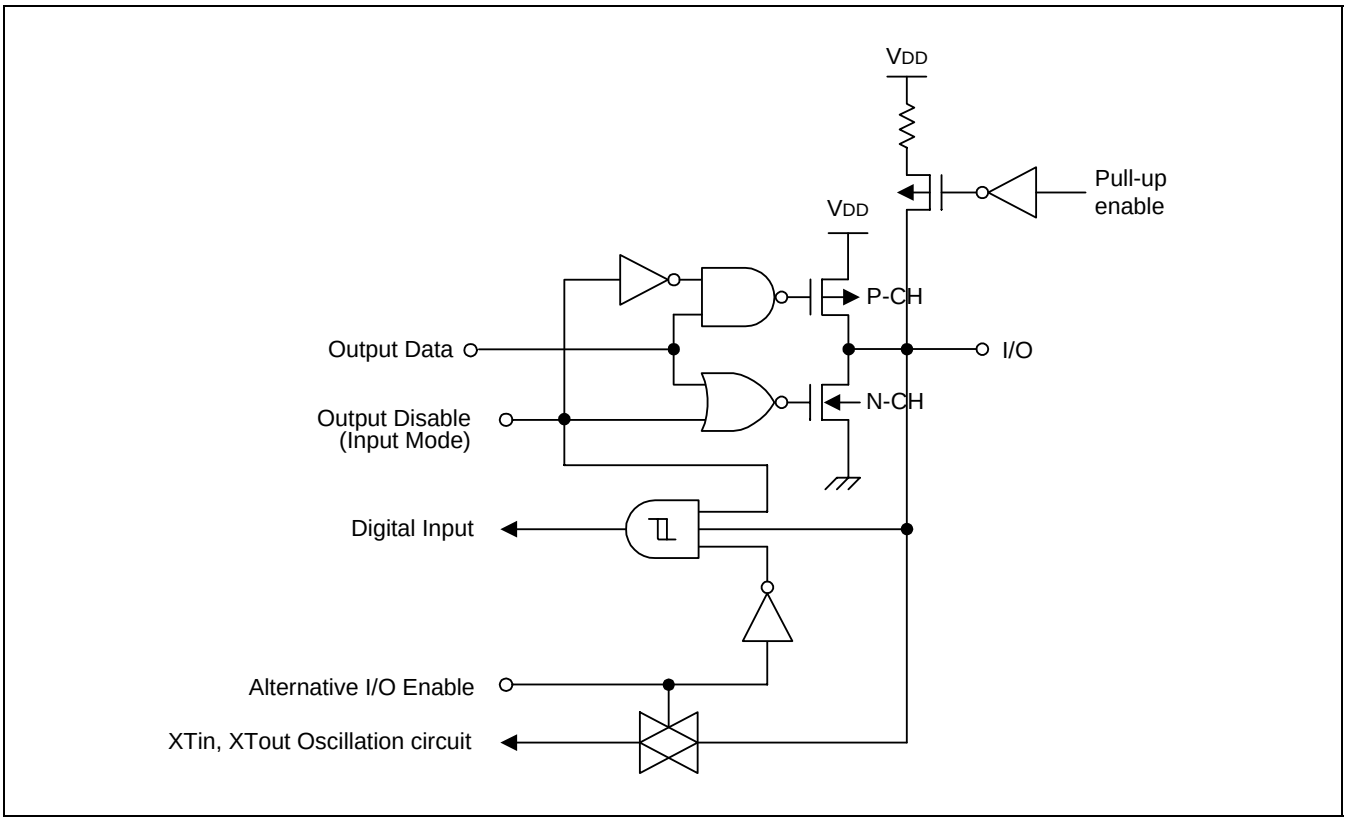


Figure 1-9. Pin Circuit Type F (P6.0, P6.1)

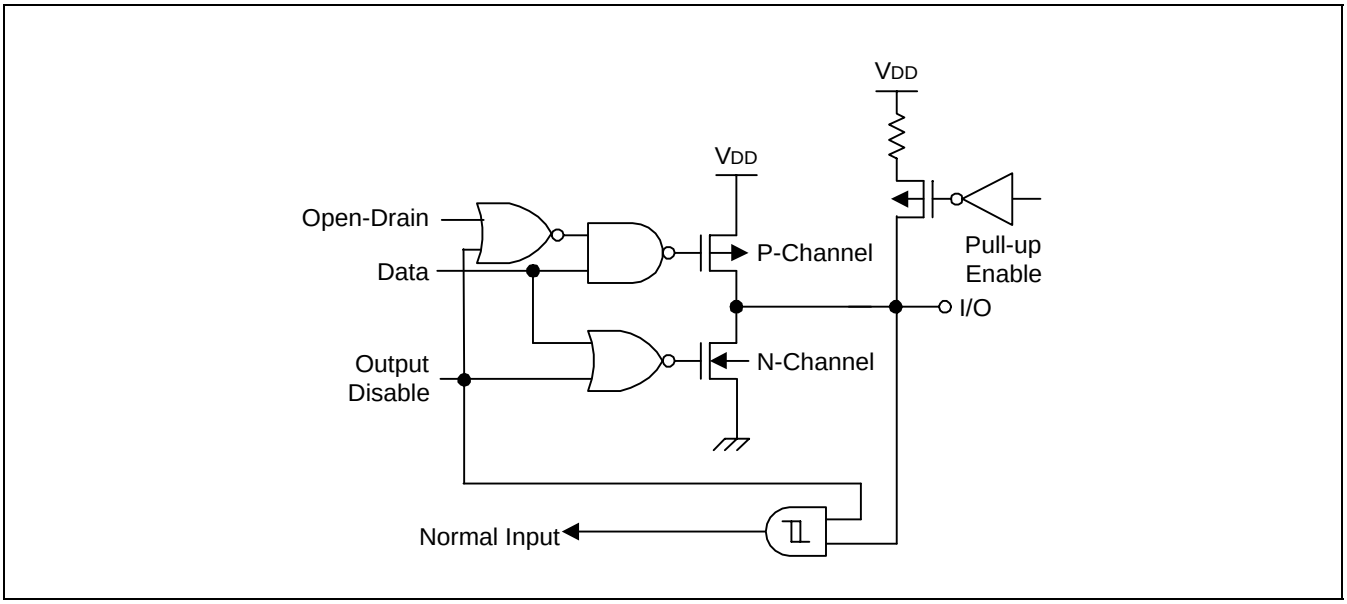


Figure 1-10. Pin Circuit Type G (P5.4-P5.7)

2 ADDRESS SPACES

OVERVIEW

The S3F84NB microcontroller has two types of address space:

- Internal program memory (Flash memory)
- Internal register file

A 16-bit address bus supports program memory operations. A separate 8-bit register bus carries addresses and data between the CPU and the register file.

The S3F84NB has a programmable internal 64-Kbytes Flash ROM. An external memory interface is not implemented.

PROGRAM MEMORY

Program memory (Flash memory) stores program code or table data. The S3F84NB has 64-Kbyte of internal programmable Flash memory. The program memory address range is therefore 0000H–FFFFH of Flash memory (See Figure 2-1).

The first 256 bytes of the program memory (0H–0FFH) are reserved for interrupt vector addresses. Unused locations (0000H – 00FFH except 03CH, 03DH, 03EH and 03FH) in this address range can be used as normal program memory. The location 03CH, 03DH, 03EH and 03FH is used as smart option ROM cell. If you use the vector address area to store program code, be careful to avoid overwriting vector addresses stored in these locations.

The program memory address at which program execution starts after reset is 0100H(default). If you use ISP^{TM} sectors as the ISP^{TM} software storage, the reset vector address can be changed by setting the Smart Option. (Refer to Figure 2-2).

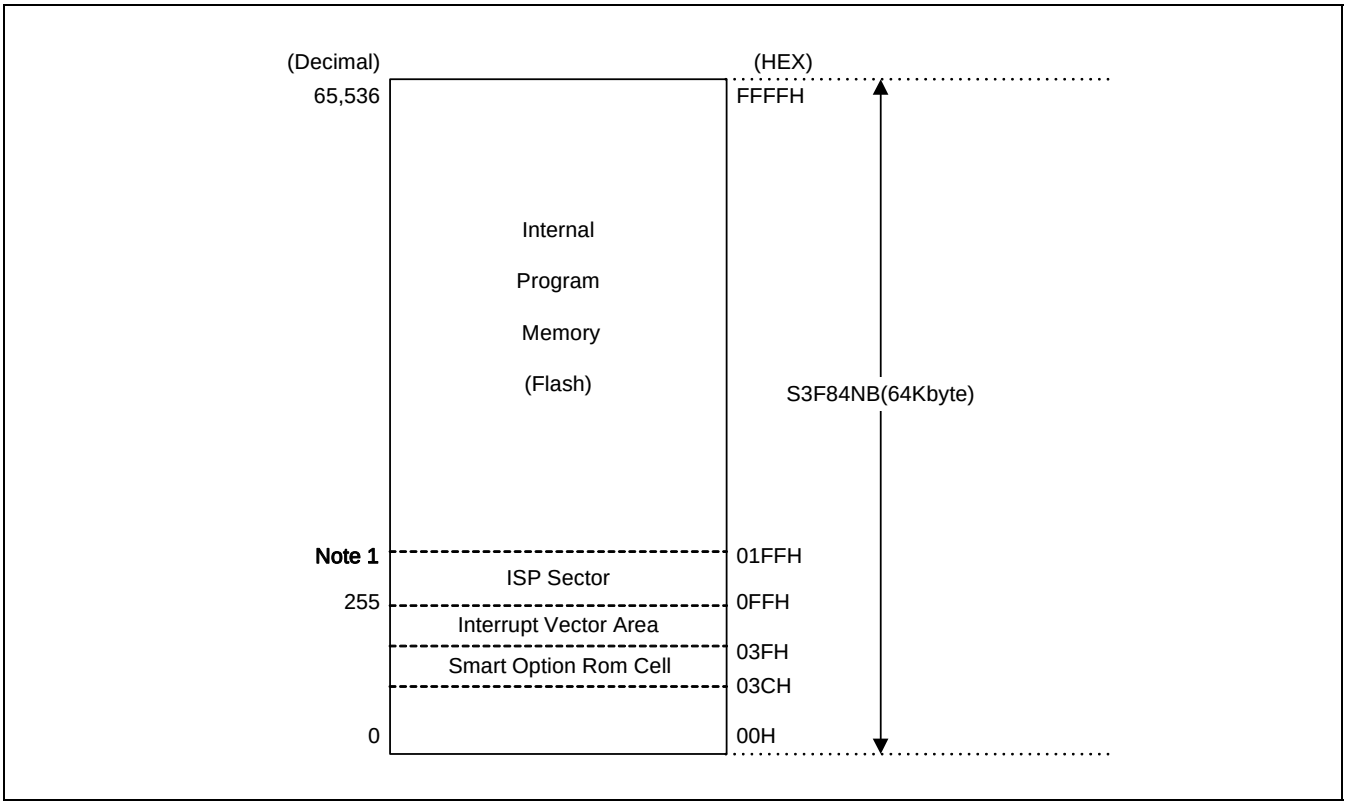


Figure 2-1. Program Memory Address Space

NOTES:

1. The size of ISP^{TM} sector can be varied by Smart Option. (Refer to Figure 2-2). According to the smart option setting related to the ISP, ISP reset vector address can be changed one of addresses to be select (200H, 300H, 500H or 900H).
2. ISP^{TM} sector can store On Board Program Software (Refer to chapter 15. Embedded Flash Memory Interface).

SMART OPTION

Smart option is the program memory option for starting condition of the chip. The program memory addresses used by smart option are from 003CH to 003FH. The S3F84NB only use 003EH and 003FH. User can write any value in the not used addresses (003CH and 003DH). The default value of smart option bits in program memory is 0FFH (LVR disable, Normal reset vector address 100H, ISP protection disable). Before execution the program memory code, user can set the smart option bits according to the hardware option for user to want to select.

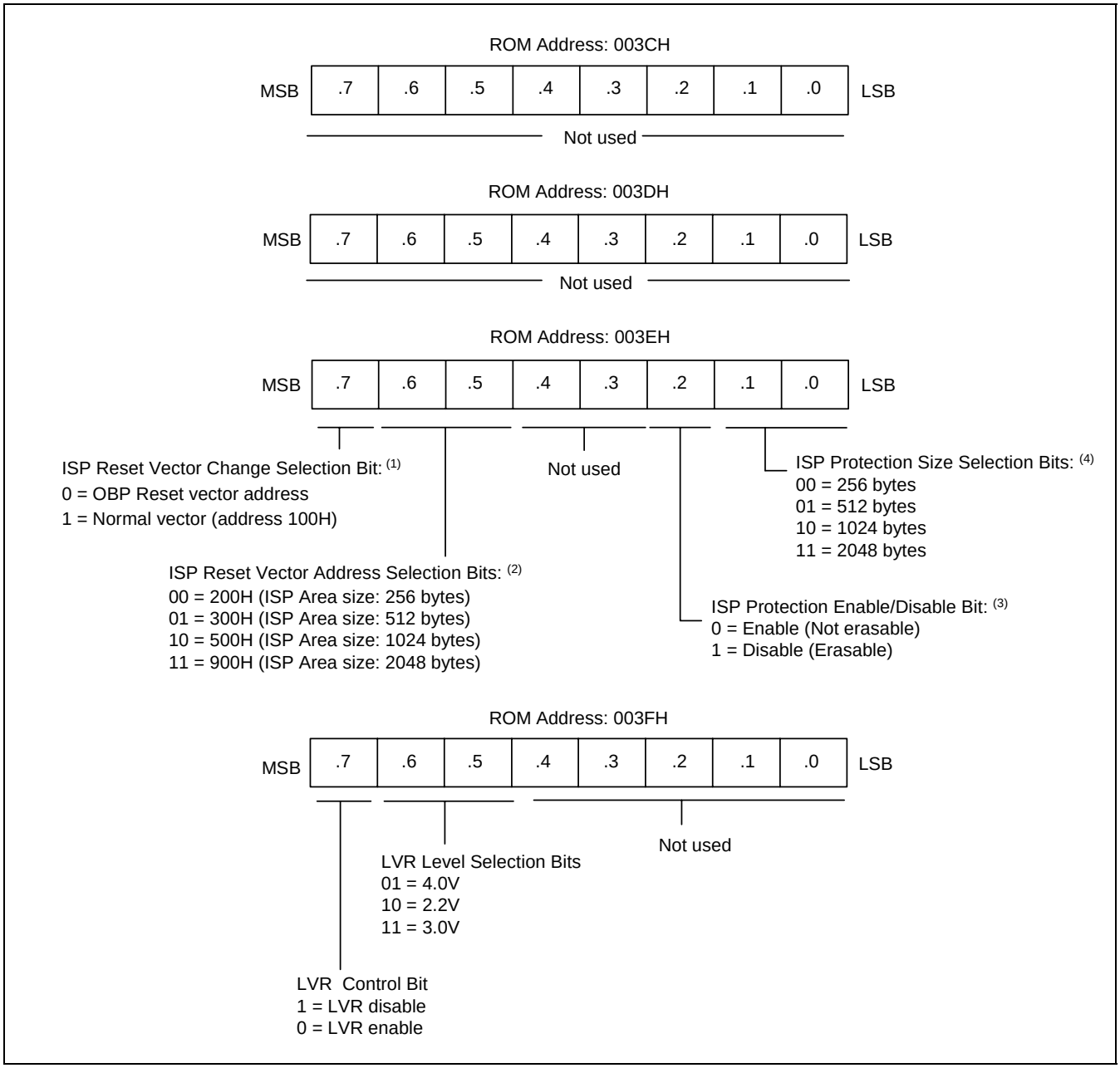


Figure 2-2. Smart Option

NOTES

1. By setting ISP Reset Vector Change Selection Bit (3EH.7) to ‘0’, user can have the available ISP area.
   If ISP Reset Vector Change Selection Bit (3EH.7) is ‘1’, 3EH.6 and 3EH.5 are meaningless.

2. If ISP Reset Vector Change Selection Bit (3EH.7) is ‘0’, user must change ISP reset vector address from 0100H to some address which user want to set reset address (0200H, 0300H, 0500H or 0900H).
   If the reset vector address is 0200H, the ISP area can be assigned from 0100H to 01FFH (256bytes). If 0300H, the ISP area can be assigned from 0100H to 02FFH (512bytes). If 0500H, the ISP area can be assigned from 0100H to 04FFH (1024bytes). If 0900H, the ISP area can be assigned from 0100H to 08FFH (2048bytes).

3. If ISP Protection Enable/Disable Bit is ‘0’, user can’t erase or program the ISP area selected by 3EH.1 and 3EH.0 in flash memory.

4. User can select suitable ISP protection size by 3EH.1 and 3EH.0. If ISP Protection Enable/Disable Bit (3EH.2) is ‘1’, 3EH.1 and 3EH.0 are meaningless.

5. Although user can write any value in the not used bits of 3CH, 3DH, 3EH and 03FH, we recommend the value of not used bits is ‘1’.

REGISTER ARCHITECTURE

In the S3F84NB implementation, the upper 64-byte area of register files is expanded two 64-byte areas, called *set 1* and *set 2*. The upper 32-byte area of set 1 is further expanded two 32-byte register banks (bank 0 and bank 1), and the lower 32-byte area is a single 32-byte common area. Set 2 is logically expanded 8 separately addressable register pages, page 0–page 8. Only page 8 is 6byte.

In case of S3F84NB the total number of addressable 8-bit registers is 2,150. Of these 2,150 registers, 16 bytes are for CPU and system control registers, 64 bytes are for peripheral control and data registers, 16 bytes are used as shared working registers, and 2,048 registers are for general-purpose use.

You can always address set 1 register location, regardless of which of the 8 register pages is currently selected. The set 1 locations, however, can only be addressed using direct addressing modes.

The extension of register space into separately addressable areas (sets, banks, and pages) is supported by various addressing mode restrictions, the bank selection instructions: SB0 and SB1, and the register page pointer (PP).

Specific register types and the area (in bytes) that they occupy in the register file are summarized in Table 2-1.

Table 2-1. S3F84NB Register Type Summary

Register Type	Number of Bytes
General-purpose registers (including 16-byte common working register area, the 192-byte prime register area, and the 64-byte set 2 area)	2,064
CPU and system control registers	16
Mapped clock, peripheral, I/O control, and data registers	64
Mapped peripheral registers (page 8)	6
Total Addressable Bytes	2,150

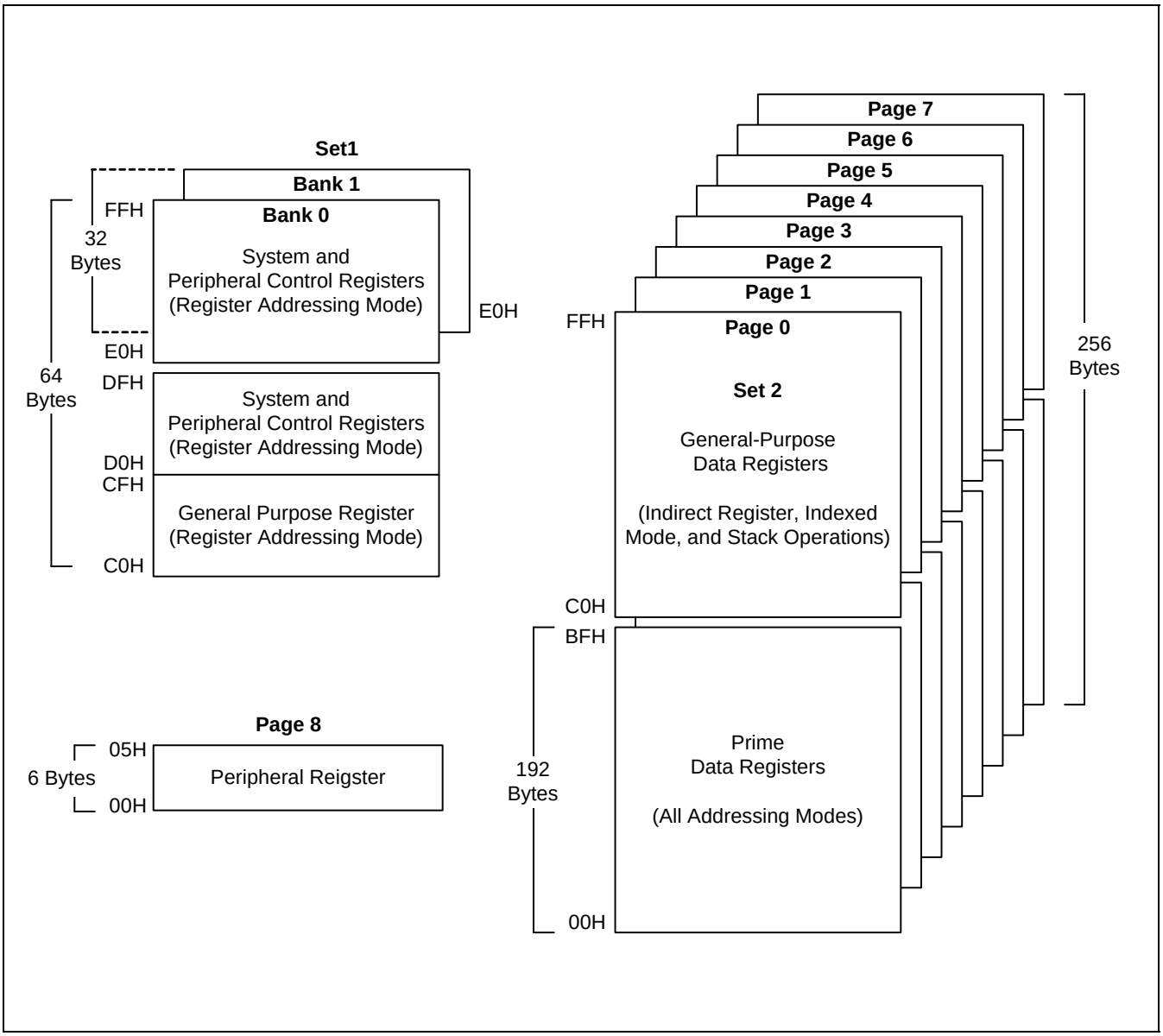


Figure 2-3. Internal Register File Organization

REGISTER PAGE POINTER (PP)

The S3C8-series architecture supports the logical expansion of the physical 2,064-byte internal register file (using an 8-bit data bus) into as many as 16 separately addressable register pages. Page addressing is controlled by the register page pointer (PP, DFH). In the S3F84NB microcontroller, a paged register file expansion is implemented for data registers, and the register page pointer must be changed to address other pages.

After a reset, the page pointer's source value (lower nibble) and the destination value (upper nibble) are always "0000", automatically selecting page 0 as the source and destination page for register addressing.

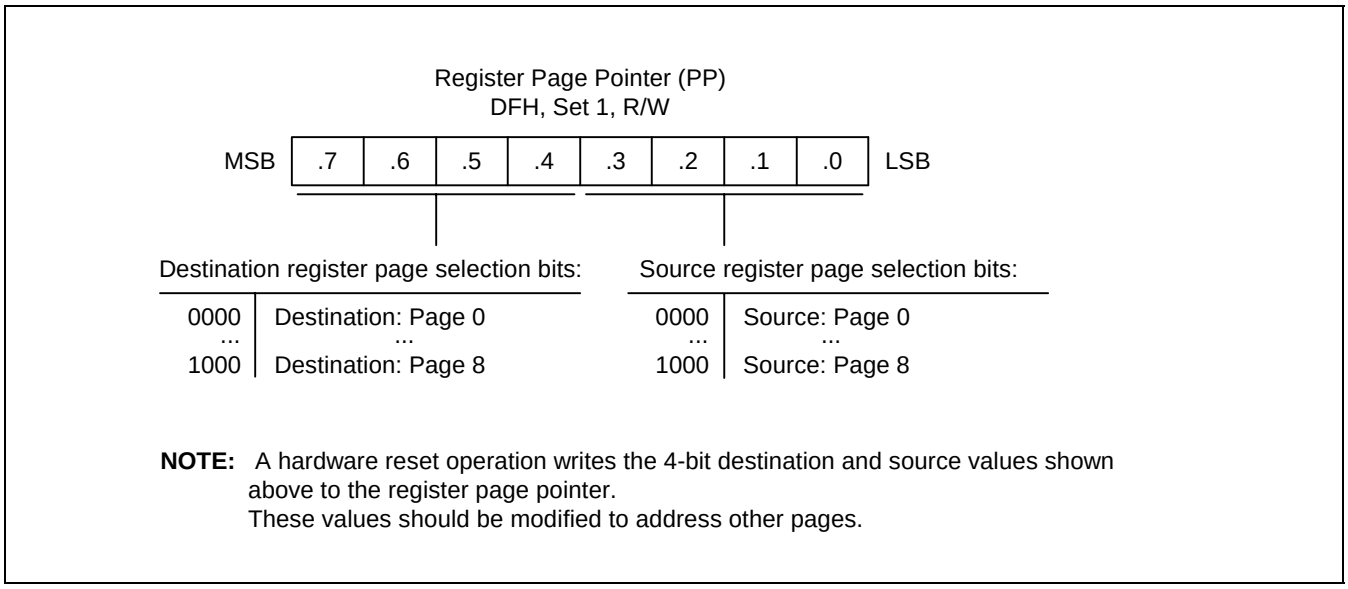


Figure 2-4. Register Page Pointer (PP)

☞ PROGRAMMING TIP – Using the Page Pointer for RAM clear (Page 0, Page 1)

```
        LD      PP,#00H         ;  Destination ← 0, Source ← 0
        SRP     #0C0H
        LD      R0,#0FFH        ;  Page 0 RAM clear starts
RAMCL0  CLR     @R0
        DJNZ    R0,RAMCL0
        CLR     @R0             ;  R0 = 00H

        LD      PP,#10H         ;  Destination ← 1, Source ← 0
        LD      R0,#0FFH        ;  Page 1 RAM clear starts
RAMCL1  CLR     @R0
        DJNZ    R0,RAMCL1
        CLR     @R0             ;  R0 = 00H
```

REGISTER SET 1

The term *set 1* refers to the upper 64 bytes of the register file, locations C0H–FFH.

The upper 32-byte area of this 64-byte space (E0H–FFH) is expanded two 32-byte register banks, *bank 0* and *bank 1*. The set register bank instructions, SB0 or SB1, are used to address one bank or the other. A hardware reset operation always selects bank 0 addressing.

The upper two 32-byte areas (bank 0 and bank 1) of set 1 (E0H–FFH) contain 64 mapped system and peripheral control registers. The lower 32-byte area contains 16 system registers (D0H–DFH) and a 16-byte common working register area (C0H–CFH). You can use the common working register area as a “scratch” area for data operations being performed in other areas of the register file.

Registers in set 1 locations are directly accessible at all times using Register addressing mode. The 16-byte working register area can only be accessed using working register addressing (For more information about working register addressing, please refer to Chapter 3, “Addressing Modes.”)

REGISTER SET 2

The same 64-byte physical space that is used for set 1 locations C0H–FFH is logically duplicated to add another 64 bytes of register space. This expanded area of the register file is called set *2*. For the S3F84NB, the set 2 address range (C0H–FFH) is accessible on pages 0-8.

The logical division of set 1 and set 2 is maintained by means of addressing mode restrictions. You can use only Register addressing mode to access set 1 location. In order to access registers in set 2, you must use Register Indirect addressing mode or Indexed addressing mode.

The set 2 register area is commonly used for stack operations.

PRIME REGISTER SPACE

The lower 192 bytes (00H–BFH, but page8 is 6byte) of the S3F84NB's eight 256-byte register pages is called *prime register area.* Prime registers can be accessed using any of the seven addressing modes (see Chapter 3, "Addressing Modes.")

The prime register area on page 0 is immediately addressable following a reset. In order to address prime registers on pages 0, or 1 you must set the register page pointer (PP) to the appropriate source and destination values.

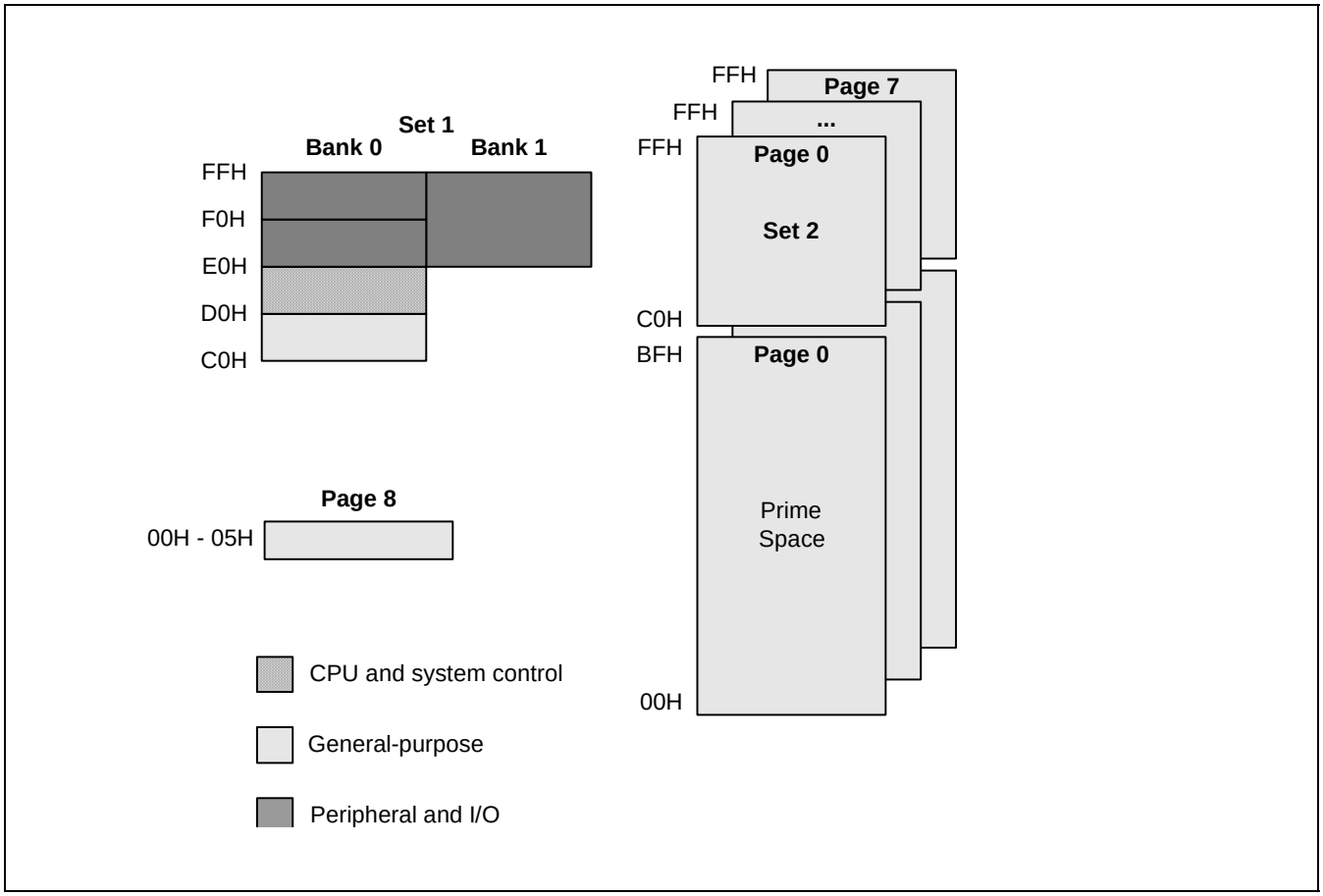


Figure 2-5. Set 1, Set 2, Prime Area Register

WORKING REGISTERS

Instructions can access specific 8-bit registers or 16-bit register pairs using either 4-bit or 8-bit address fields. When 4-bit working register addressing is used, the 256-byte register file can be seen by the programmer as one that consists of 32 8-byte register groups or "slices." Each slice comprises of eight 8-bit registers.

Using the two 8-bit register pointers, RP1 and RP0, two working register slices can be selected at any one time to form a 16-byte working register block. Using the register pointers, you can move this 16-byte register block anywhere in the addressable register file, except for the set 2 area.

The terms slice and block are used in this manual to help you visualize the size and relative locations of selected working register spaces:

- One working register *slice* is 8 bytes (eight 8-bit working registers, R0–R7 or R8–R15)
- One working register *block* is 16 bytes (sixteen 8-bit working registers, R0–R15)

All the registers in an 8-byte working register slice have the same binary value for their five most significant address bits. This makes it possible for each register pointer to point to one of the 24 slices in the register file other than set 2. The base addresses for the two selected 8-byte register slices are contained in register pointers RP0 and RP1.

After a reset, RP0 and RP1 always point to the 16-byte common area in set 1 (C0H–CFH).

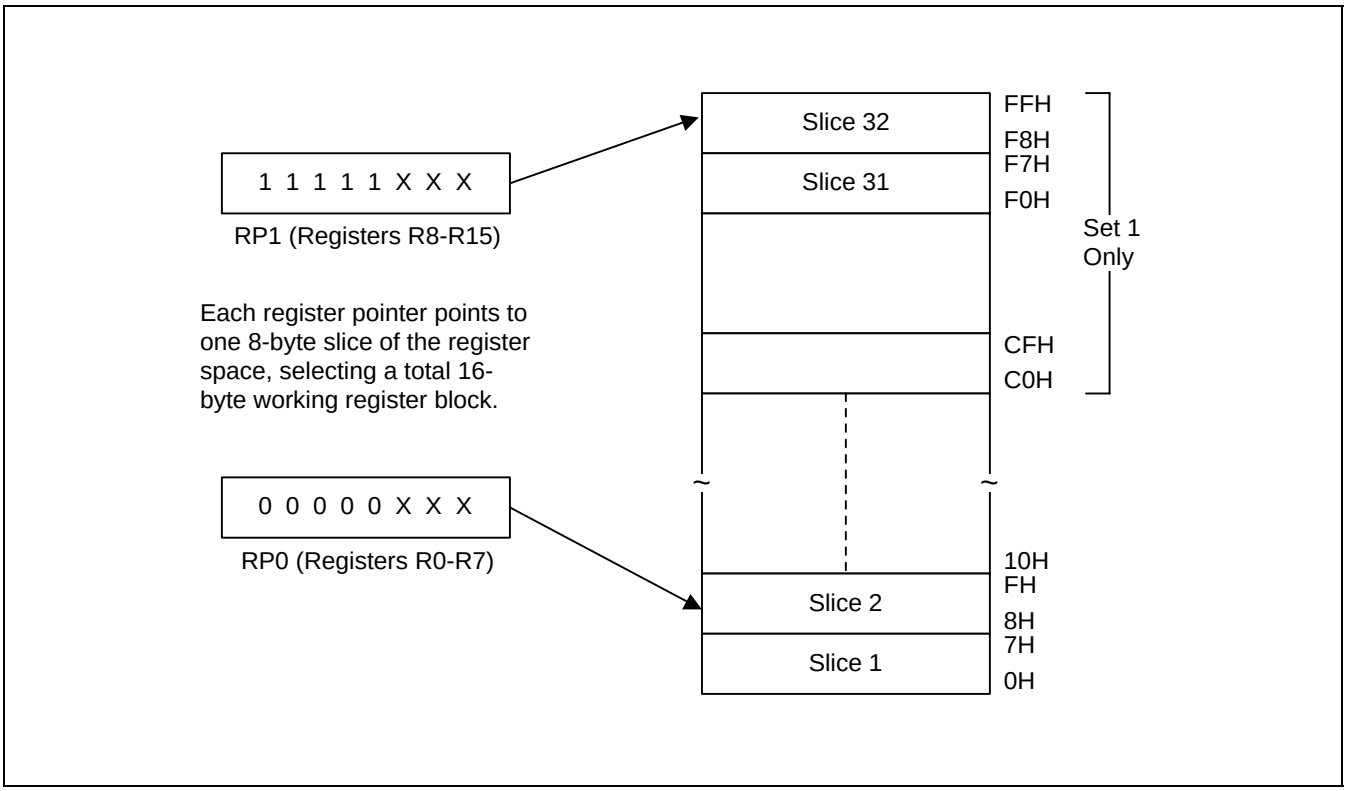


Figure 2-6. 8-Byte Working Register Areas (Slices)

USING THE REGISTER POINTERS

Register pointers RP0 and RP1, mapped to addresses D6H and D7H in set 1, are used to select two movable 8-byte working register slices in the register file. After a reset, RP# point to the working register common area: RP0 points to addresses C0H–C7H, and RP1 points to addresses C8H–CFH.

To change a register pointer value, you load a new value to RP0 and/or RP1 using an SRP or LD instruction. (See Figures 2-7 and 2-8).

With working register addressing, you can only access those two 8-bit slices of the register file that are currently pointed to by RP0 and RP1. You cannot, however, use the register pointers to select a working register space in set 2, C0H–FFH, because these locations can be accessed only using the Indirect Register or Indexed addressing modes.

The selected 16-byte working register block usually consists of two contiguous 8-byte slices. As a general programming guideline, it is recommended that RP0 point to the "lower" slice and RP1 point to the "upper" slice (see Figure 2-7).). In some cases, it may be necessary to define working register areas in different (non-contiguous) areas of the register file. In Figure 2-8, RP0 points to the "upper" slice and RP1 to the "lower" slice.

Because a register pointer can point to either of the two 8-byte slices in the working register block, you can flexibly define the working register area to support program requirements.

☞ PROGRAMMING TIP – Setting the Register Pointers

```
SRP     #70H          ;  RP0 ← 70H, RP1 ← 78H
SRP1    #48H          ;  RP0 ← no change, RP1 ← 48H,
SRP0    #0A0H         ;  RP0 ← 0A0H, RP1 ← no change
CLR     RP0           ;  RP0 ← 00H, RP1 ← no change
LD      RP1,#0F8H     ;  RP0 ← no change, RP1 ← 0F8H
```

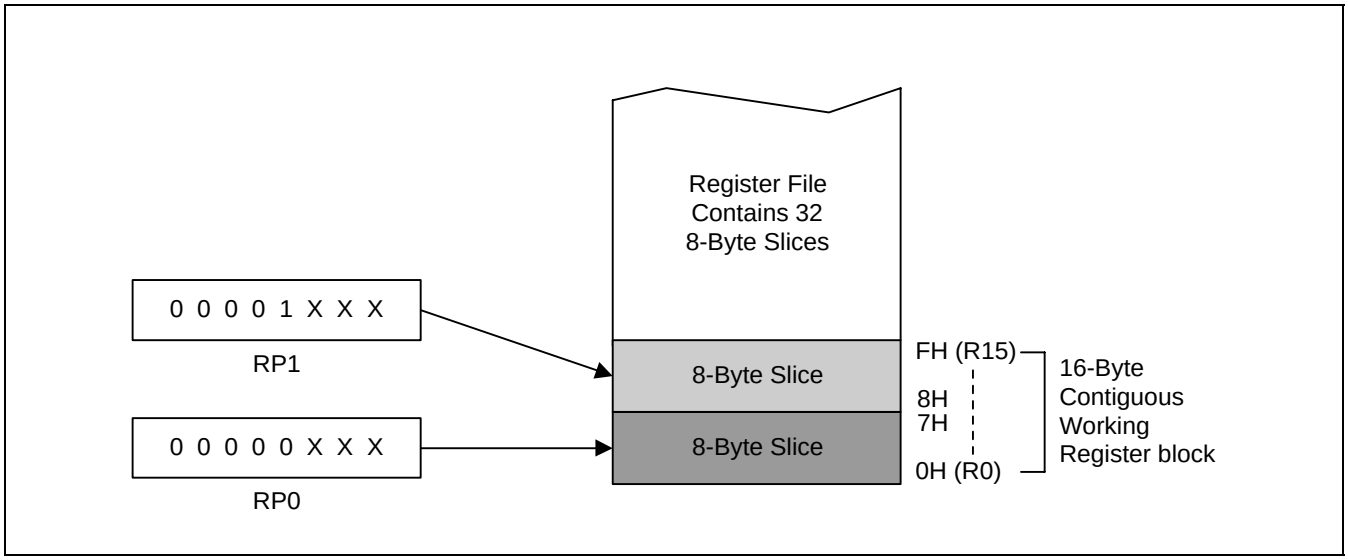


Figure 2-7. Contiguous 16-Byte Working Register Block

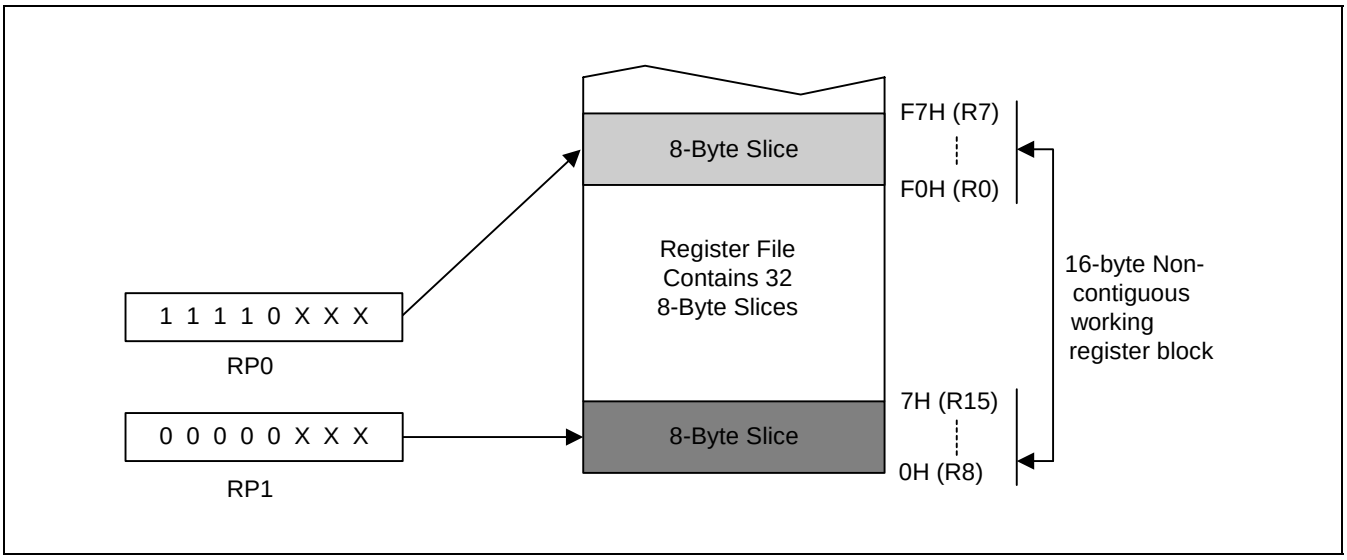


Figure 2-8. Non-Contiguous 16-Byte Working Register Block

☞ PROGRAMMING TIP – Using the RPs to Calculate the Sum of a Series of Registers

Calculate the sum of registers 80H–85H using the register pointer. The register addresses from 80H through 85H contain the values 10H, 11H, 12H, 13H, 14H, and 15 H, respectively:

```
SRP0    #80H        ;  RP0 ← 80H
ADD     R0,R1       ;  R0 ← R0 + R1
ADC     R0,R2       ;  R0 ← R0 + R2 + C
ADC     R0,R3       ;  R0 ← R0 + R3 + C
ADC     R0,R4       ;  R0 ← R0 + R4 + C
ADC     R0,R5       ;  R0 ← R0 + R5 + C
```

The sum of these six registers, 6FH, is located in the register R0 (80H). The instruction string used in this example takes 12 bytes of instruction code and its execution time is 36 cycles. If the register pointer is not used to calculate the sum of these registers, the following instruction sequence would have to be used:

```
ADD     80H,81H     ;  80H ← (80H) + (81H)
ADC     80H,82H     ;  80H ← (80H) + (82H) + C
ADC     80H,83H     ;  80H ← (80H) + (83H) + C
ADC     80H,84H     ;  80H ← (80H) + (84H) + C
ADC     80H,85H     ;  80H ← (80H) + (85H) + C
```

Now, the sum of the six registers is also located in register 80H. However, this instruction string takes 15 bytes of instruction code rather than 12 bytes, and its execution time is 50 cycles rather than 36 cycles.

REGISTER ADDRESSING

The S3C8-series register architecture provides an efficient method of working register addressing that takes full advantage of shorter instruction formats to reduce execution time.

With Register (R) addressing mode, in which the operand value is the content of a specific register or register pair, you can access any location in the register file except for set 2. With working register addressing, you use a register pointer to specify an 8-byte working register space in the register file and an 8-bit register within that space.

Registers are addressed either as a single 8-bit register or as a paired 16-bit register space. In a 16-bit register pair, the address of the first 8-bit register is always an even number and the address of the next register is always an odd number. The most significant byte of the 16-bit data is always stored in the even-numbered register, and the least significant byte is always stored in the next (+1) odd-numbered register.

Working register addressing differs from Register addressing as it uses a register pointer to identify a specific 8-byte working register space in the internal register file and a specific 8-bit register within that space.

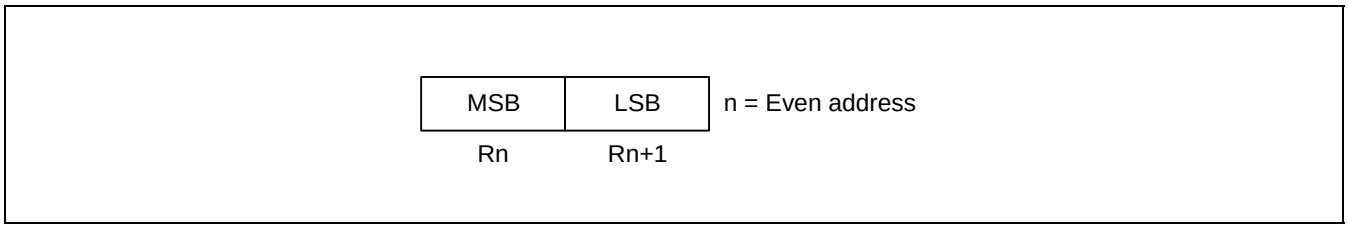


Figure 2-9. 16-Bit Register Pair

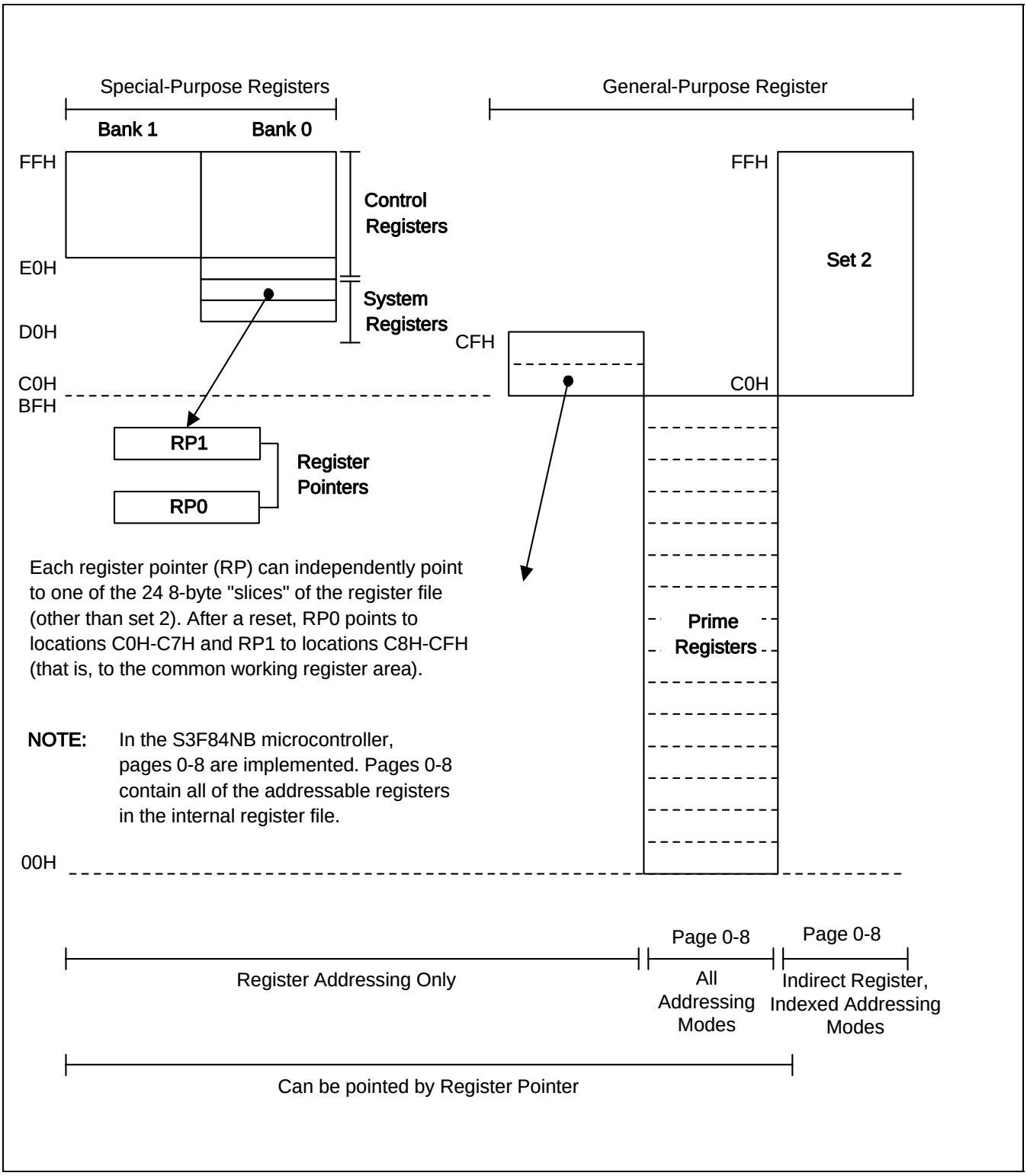


Figure 2-10. Register File Addressing

COMMON WORKING REGISTER AREA (C0H–CFH)

After a reset, register pointers RP0 and RP1 automatically select two 8-byte register slices in set 1, locations C0H–CFH, as the active 16-byte working register block:

RP0 → C0H–C7H

RP1 → C8H–CFH

This 16-byte address range is called *common area*. That is, locations in this area can be used as working registers by operations that address any location on any page in the register file. Typically, these working registers serve as temporary buffers for data operations between different pages.

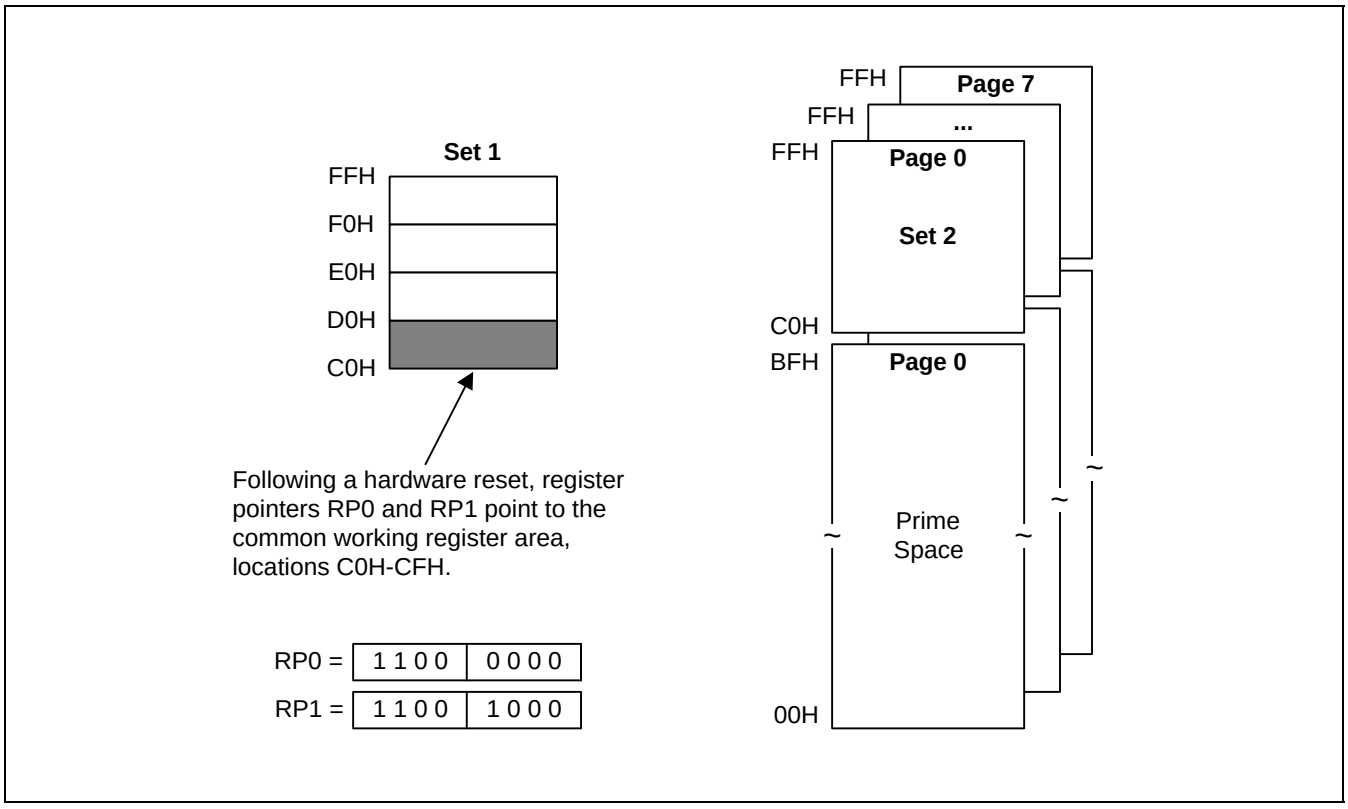


Figure 2-11. Common Working Register Area

☞ PROGRAMMING TIP – Addressing the Common Working Register Area

As the following examples show, you should access working registers in the common area, locations C0H–CFH, using working register addressing mode only.

Examples 1:

```
1. LD      0C2H,40H          ;  Invalid addressing mode!
```

Use working register addressing instead:

```
SRP        #0C0H
LD         R2,40H            ;  R2 (C2H) ← the value in location 40H
```

Example 2:

```
ADD        0C3H,#45H         ;  Invalid addressing mode!
```

Use working register addressing instead:

```
SRP        #0C0H
ADD        R3,#45H           ;  R3 (C3H) ← R3 + 45H
```

4-BIT WORKING REGISTER ADDRESSING

Each register pointer defines a movable 8-byte slice of working register space. The address information stored in a register pointer serves as an addressing "window" that makes it possible for instructions to access working registers very efficiently using short 4-bit addresses. When an instruction addresses a location in the selected working register area, the address bits are concatenated in the following way to form a complete 8-bit address:

- The high-order bit of the 4-bit address selects one of the register pointers ("0" selects RP0, "1" selects RP1).
- The five high-order bits in the register pointer select an 8-byte slice of the register space.
- The three low-order bits of the 4-bit address select one of the eight registers in the slice.

As shown in Figure 2-12, the result of this operation is that the five high-order bits from the register pointer are concatenated with the three low-order bits from the instruction address to form the complete address. As long as the address stored in the register pointer remains unchanged, the three bits from the address will always point to an address in the same 8-byte register slice.

Figure 2-13 shows a typical example of 4-bit working register addressing. The high-order bit of the instruction "INC R6" is "0", which selects RP0. The five high-order bits stored in RP0 (01110B) are concatenated with the three low-order bits of the instruction's 4-bit address (110B) to produce the register address 76H (01110110B).

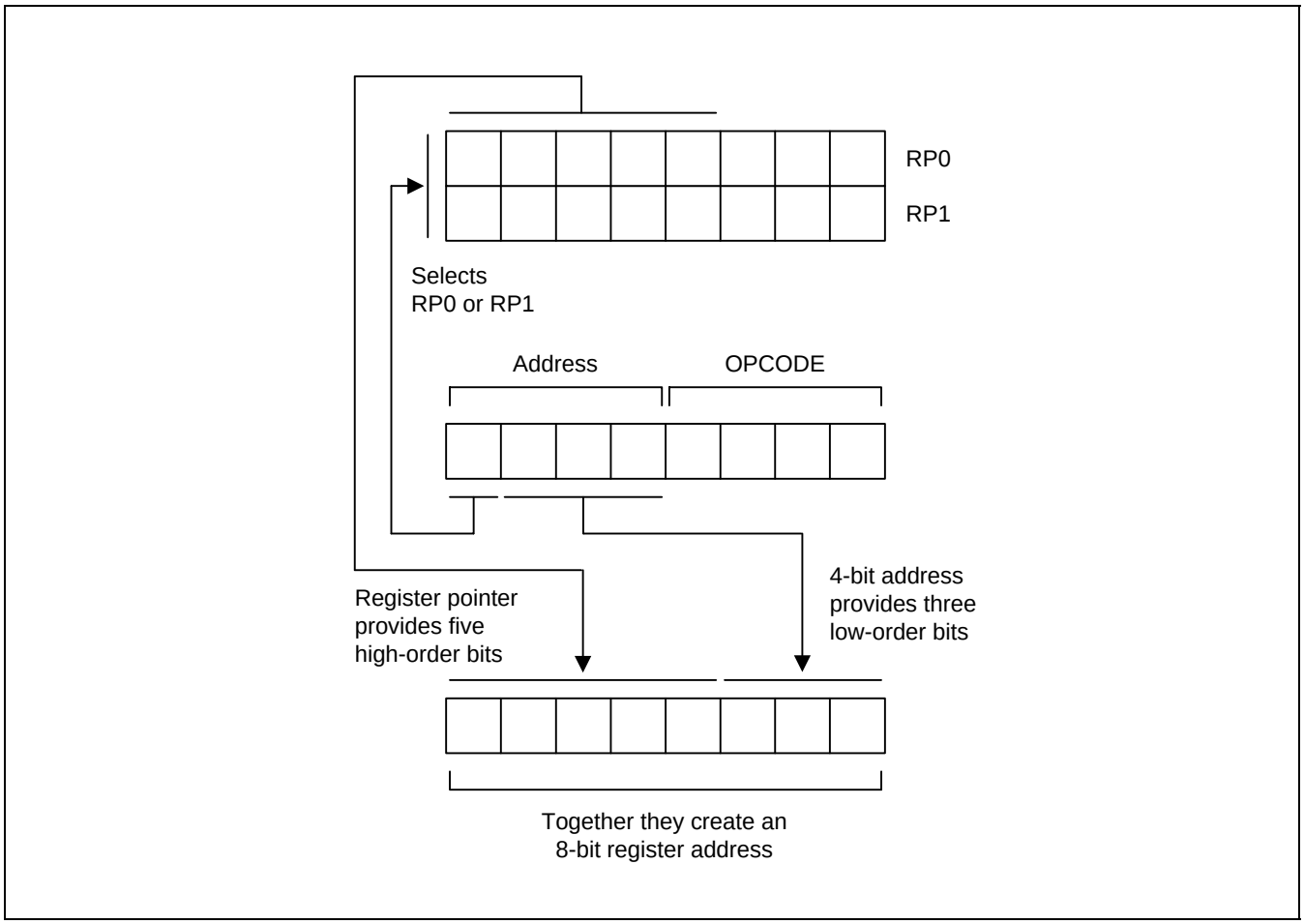


Figure 2-12. 4-Bit Working Register Addressing

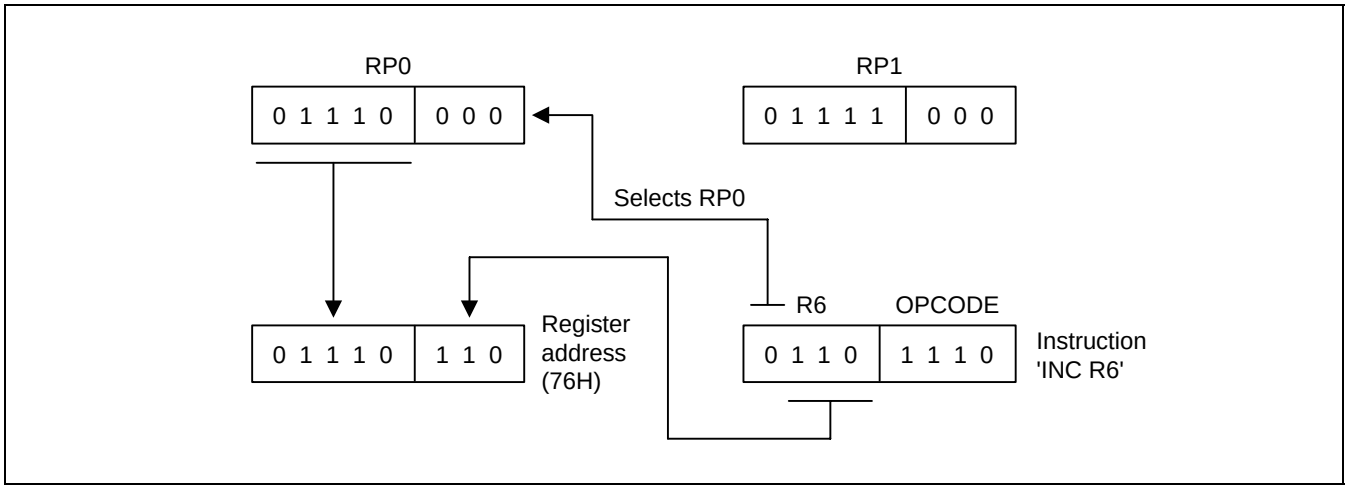


Figure 2-13. 4-Bit Working Register Addressing Example

8-BIT WORKING REGISTER ADDRESSING

You can also use 8-bit working register addressing to access registers in a selected working register area. To initiate 8-bit working register addressing, the upper four bits of the instruction address must contain the value "1100B." This 4-bit value (1100B) indicates that the remaining four bits have the same effect as 4-bit working register addressing.

As shown in Figure 2-14, the lower nibble of the 8-bit address is concatenated in much the same way as for 4-bit addressing. Bit 3 selects either RP0 or RP1, which then supplies the five high-order bits of the final address. The three low-order bits of the complete address are provided by the original instruction.

Figure 2-15 shows an example of 8-bit working register addressing. The four high-order bits of the instruction address (1100B) specify 8-bit working register addressing. Bit 3 ("1") selects RP1 and the five high-order bits in RP1 (10101B) become the five high-order bits of the register address. The three low-order bits of the register address (011) are provided by the three low-order bits of the 8-bit instruction address. The five-address bits from RP1 and the three address bits from the instruction are concatenated to form the complete register address, 0ABH (10101011B).

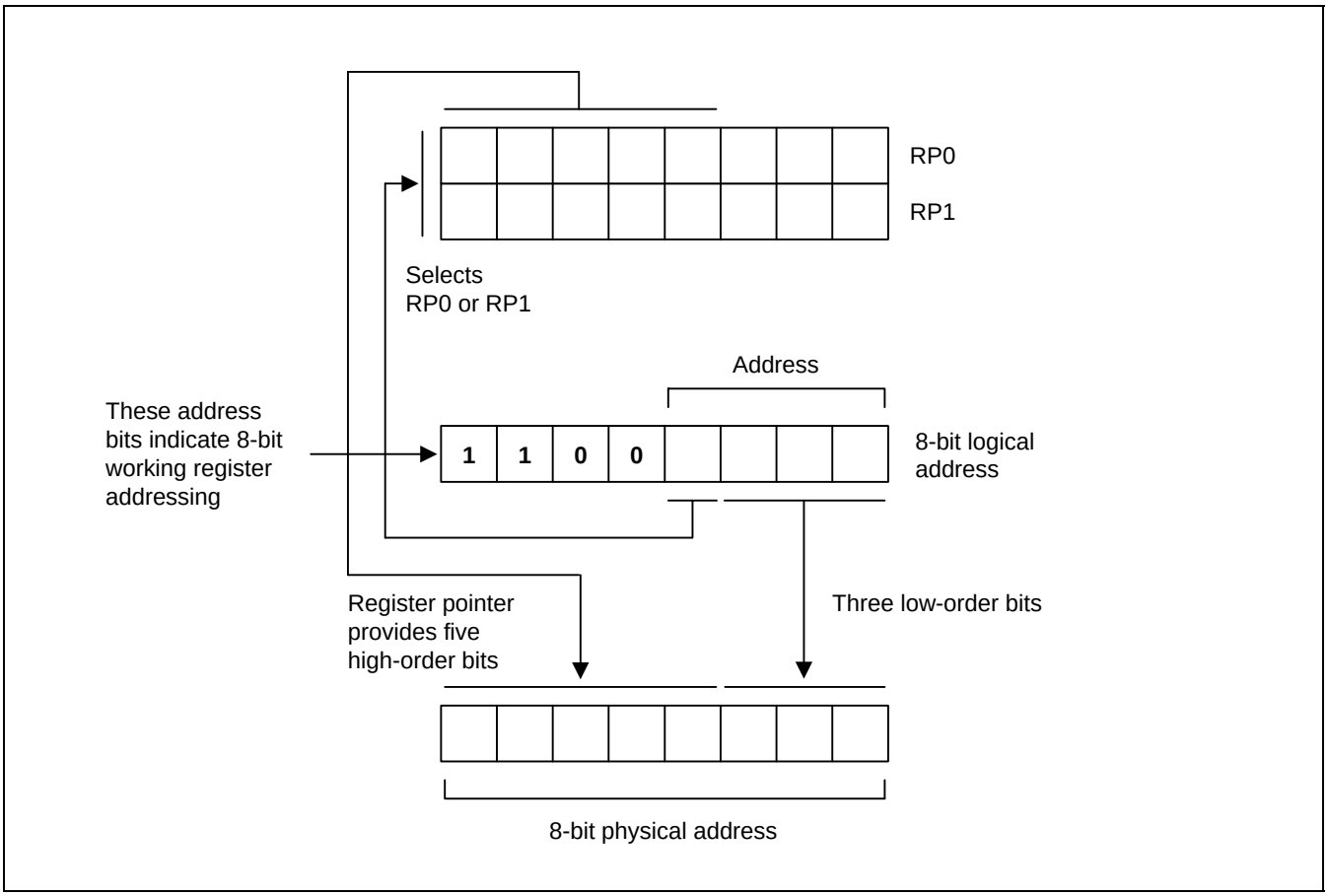


Figure 2-14. 8-Bit Working Register Addressing

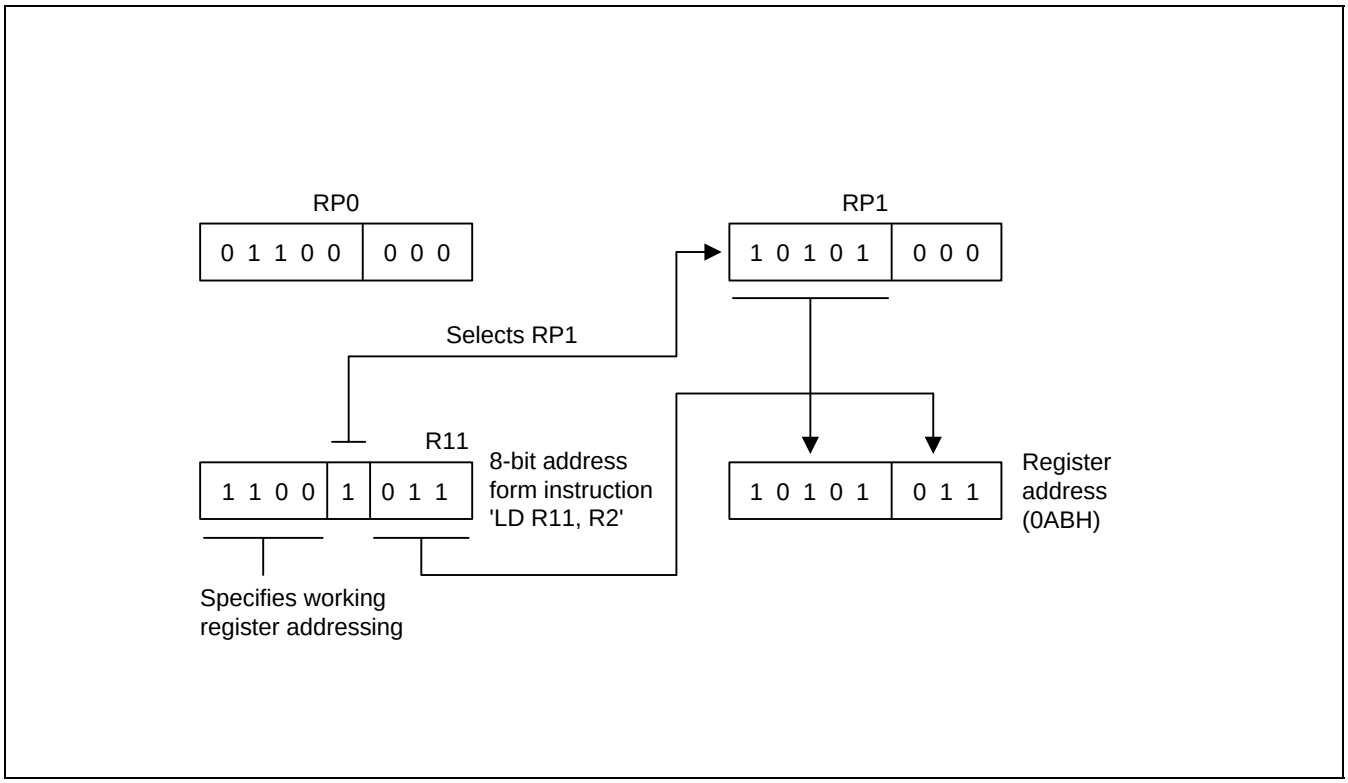


Figure 2-15. 8-Bit Working Register Addressing Example

SYSTEM AND USER STACK

The S3C8-series microcontrollers use the system stack for data storage, subroutine calls and returns. The PUSH and POP instructions are used to control system stack operations. The S3F84NB architecture supports stack operations in the internal register file.

Stack Operations

Return addresses for procedure calls, interrupts, and data are stored on the stack. The contents of the PC are saved to stack by a CALL instruction and restored by the RET instruction. When an interrupt occurs, the contents of the PC and the FLAGS register are pushed to the stack. The IRET instruction then pops these values back to their original locations. The stack address value is always decreased by one before a push operation and increased by one *after* a pop operation. The stack pointer (SP) always points to the stack frame stored on the top of the stack, as shown in Figure 2-16.

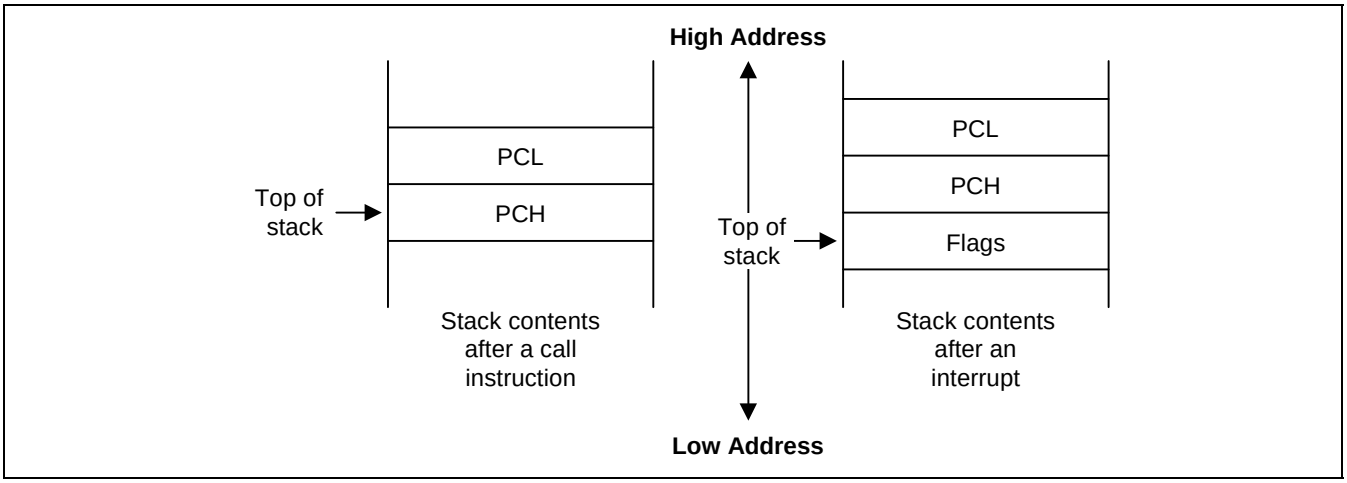


Figure 2-16. Stack Operations

User-Defined Stacks

You can freely define stacks in the internal register file as data storage locations. The instructions PUSHUI, PUSHUD, POPUI, and POPUD support user-defined stack operations.

Stack Pointers (SPL, SPH)

Register locations D8H and D9H contain the 16-bit stack pointer (SP) that is used for system stack operations. The most significant byte of the SP address, SP15–SP8, is stored in the SPH register (D8H), and the least significant byte, SP7–SP0, is stored in the SPL register (D9H). After a reset, the SP value is undetermined.

Because only internal memory space is implemented in the S3F84NB, the SPL must be initialized to an 8-bit value in the range 00H–FFH. The SPH register is not needed and can be used as a general-purpose register, if necessary.

When the SPL register contains the only stack pointer value (that is, when it points to a system stack in the register file), you can use the SPH register as a general-purpose data register. However, if an overflow or underflow condition occurs as a result of increasing or decreasing the stack address value in the SPL register during normal stack operations, the value in the SPL register will overflow (or underflow) to the SPH register, overwriting any other data that is currently stored there. To avoid overwriting data in the SPH register, you can initialize the SPL value to "FFH" instead of "00H".

☞ PROGRAMMING TIP – Standard Stack Operations Using PUSH and POP

The following example shows you how to perform stack operations in the internal register file using PUSH and POP instructions:

```
LD      SPL,#0FFH       ;  SPL ← FFH
                        ;  (Normally, the SPL is set to 0FFH by the initialization
                        ;  routine)
•
•
•
PUSH    PP              ;  Stack address 0FEH ← PP
PUSH    RP0             ;  Stack address 0FDH ← RP0
PUSH    RP1             ;  Stack address 0FCH ← RP1
PUSH    R3              ;  Stack address 0FBH ← R3
•
•
•
POP     R3              ;  R3 ← Stack address 0FBH
POP     RP1             ;  RP1 ← Stack address 0FCH
POP     RP0             ;  RP0 ← Stack address 0FDH
POP     PP              ;  PP ← Stack address 0FEH
```

3 ADDRESSING MODES

OVERVIEW

Instructions that are stored in program memory are fetched for execution using the program counter. Instructions indicate the operation to be performed and the data to be operated on. Addressing mode is the method used to determine the location of the data operand. The operands specified in SAM88RC instructions may be condition codes, immediate data, or a location in the register file, program memory, or data memory.

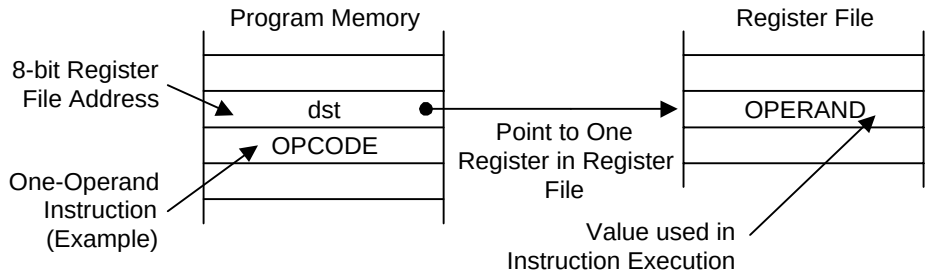
The S3C8-series instruction set supports seven explicit addressing modes. Not all of these addressing modes are available for each instruction. The seven addressing modes and their symbols are:

- Register (R)
- Indirect Register (IR)
- Indexed (X)
- Direct Address (DA)
- Indirect Address (IA)
- Relative Address (RA)
- Immediate (IM)

REGISTER ADDRESSING MODE (R)

In Register addressing mode (R), the operand value is the content of a specified register or register pair (see Figure 3-1).

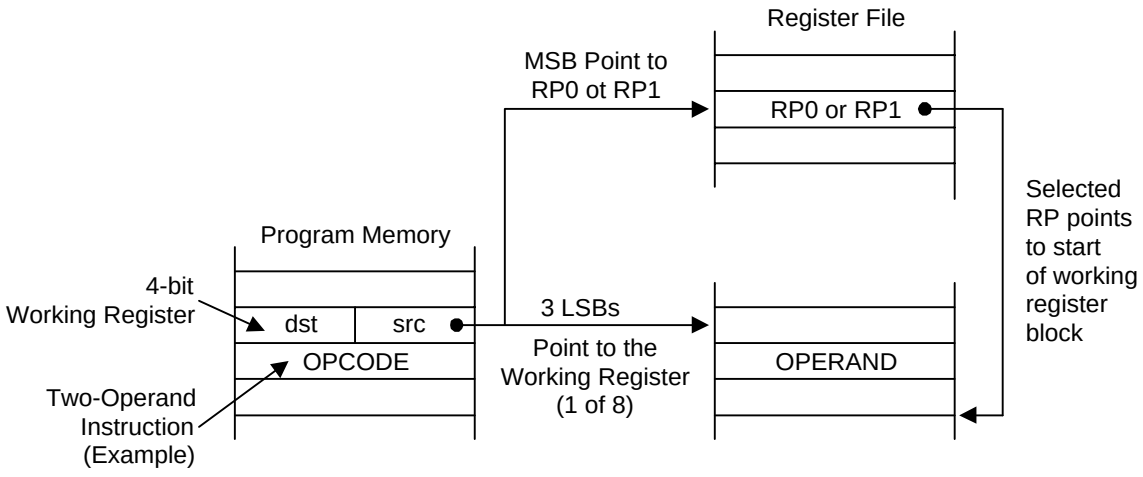
Working register addressing differs from Register addressing in that it uses a register pointer to specify an 8-byte working register space in the register file and an 8-bit register within that space (see Figure 3-2).



Sample Instruction:

```
DEC     CNTR            ;   Where CNTR is the label of an 8-bit register address
```

Figure 3-1. Register Addressing



Sample Instruction:

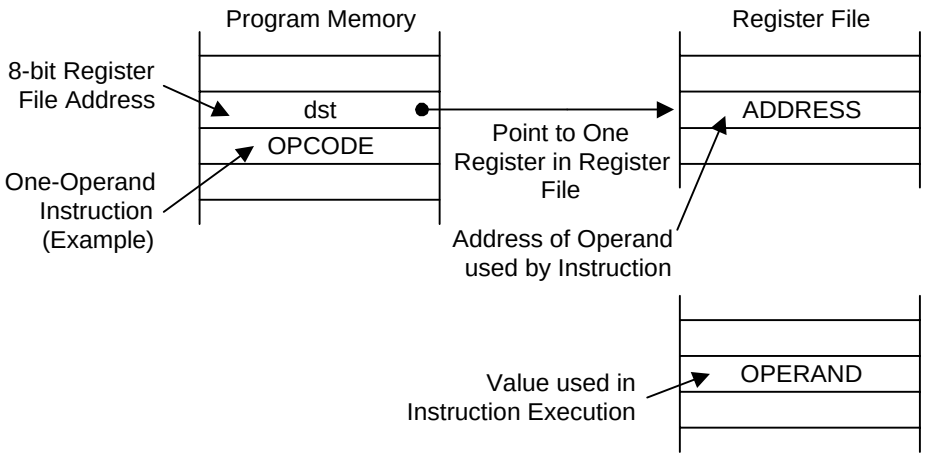
```
ADD     R1, R2          ;   Where R1 and R2 are registers in the currently
                            selected working register area.
```

Figure 3-2. Working Register Addressing

INDIRECT REGISTER ADDRESSING MODE (IR)

In Indirect Register (IR) addressing mode, the content of the specified register or register pair is the address of the operand. Depending on the instruction used, the actual address may point to a register in the register file, to program memory (ROM), or to an external memory space (see Figures 3-3 through 3-6).

You can use any 8-bit register to indirectly address another register. Any 16-bit register pair can be used to indirectly address another memory location. Please note, however, that you cannot access locations C0H–FFH in set 1 using the Indirect Register addressing mode.



Sample Instruction:

```
RL      @SHIFT          ;   Where SHIFT is the label of an 8-bit register address
```

Figure 3-3. Indirect Register Addressing to Register File

INDIRECT REGISTER ADDRESSING MODE (Continued)

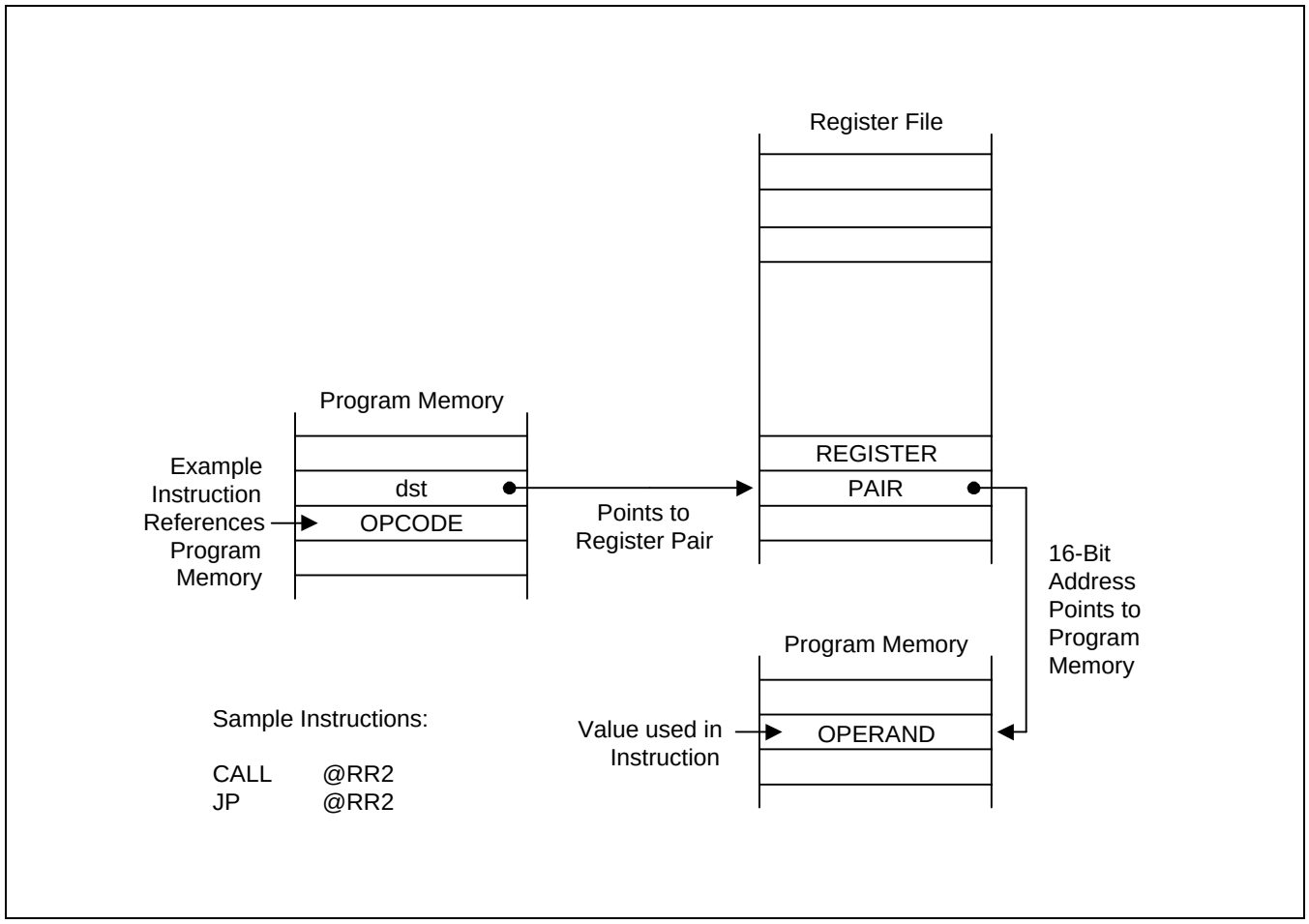


Figure 3-4. Indirect Register Addressing to Program Memory

INDIRECT REGISTER ADDRESSING MODE (Continued)

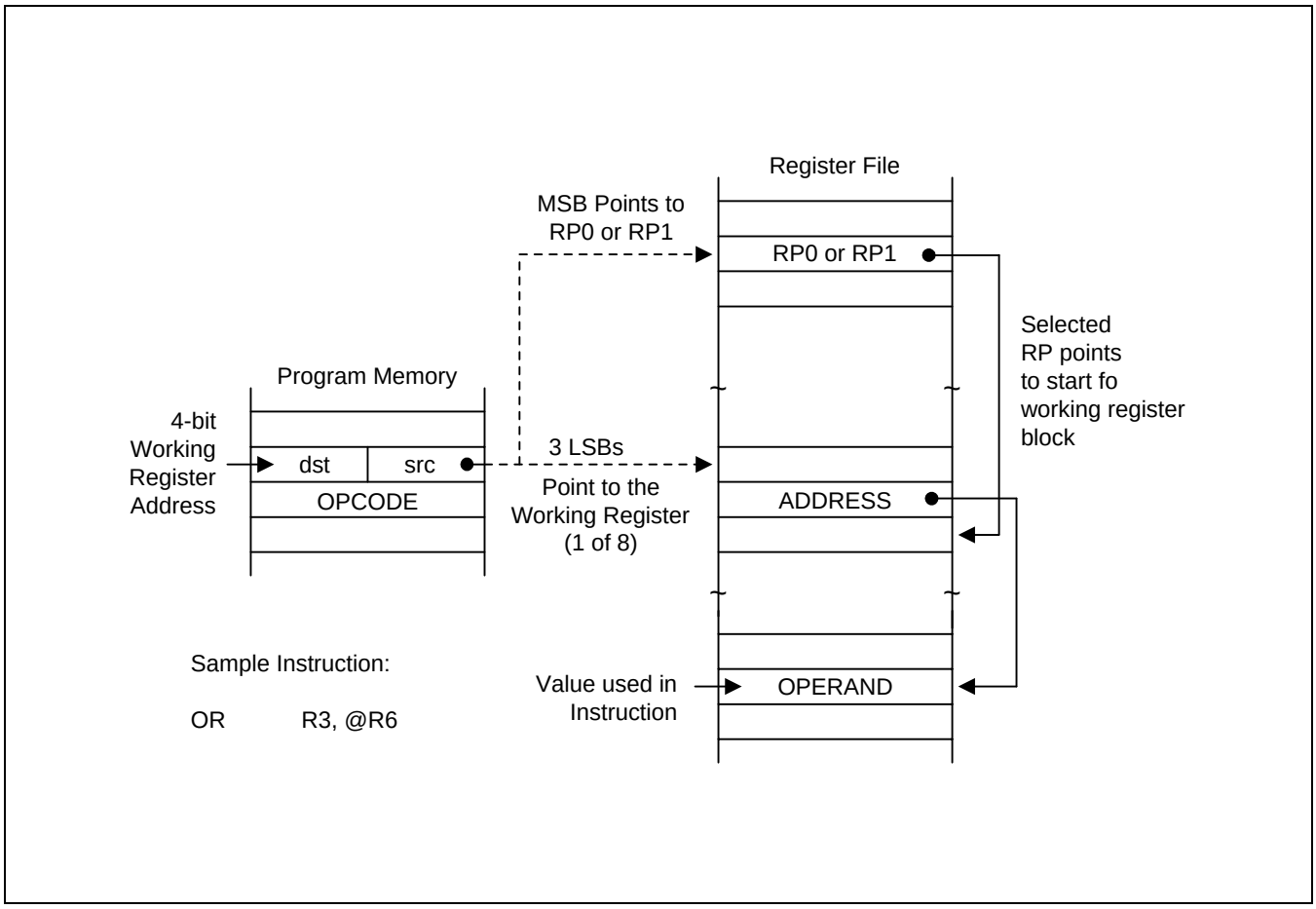
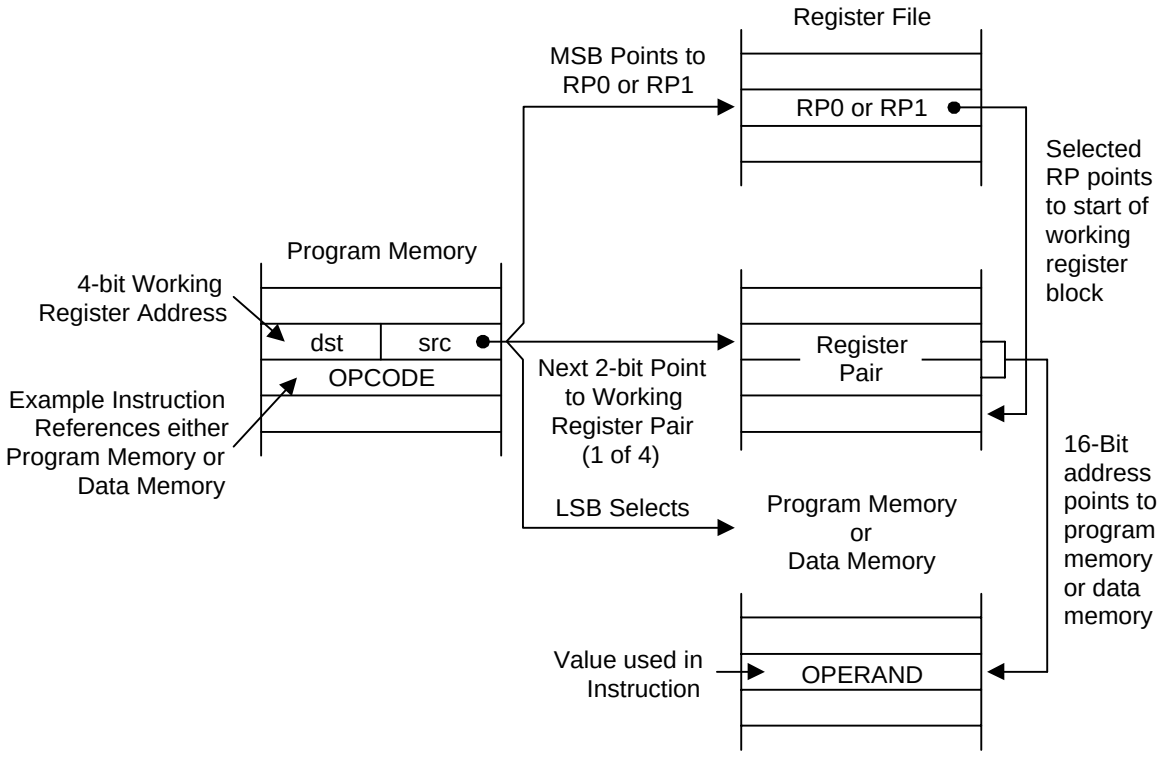


Figure 3-5. Indirect Working Register Addressing to Register File

INDIRECT REGISTER ADDRESSING MODE (Continued)



Sample Instructions:

```
LCD     R5,@RR6       ;  Program memory access
LDE     R3,@RR14      ;  External data memory access
LDE     @RR4, R8      ;  External data memory access
```

Figure 3-6. Indirect Working Register Addressing to Program or Data Memory

INDEXED ADDRESSING MODE (X)

Indexed (X) addressing mode adds an offset value to a base address during instruction execution in order to calculate the effective operand address (see Figure 3-7). You can use Indexed addressing mode to access locations in the internal register file or in external memory. Please note, however, that you cannot access locations C0H–FFH in set 1 using indexed addressing mode.

In short offset Indexed addressing mode, the 8-bit displacement is treated as a signed integer in the range –128 to +127. This applies to external memory accesses only (see Figure 3-8.)

For register file addressing, an 8-bit base address provided by the instruction is added to an 8-bit offset contained in a working register. For external memory accesses, the base address is stored in the working register pair designated in the instruction. The 8-bit or 16-bit offset given in the instruction is then added to that base address (see Figure 3-9).

The only instruction that supports indexed addressing mode for the internal register file is the Load instruction (LD). The LDC and LDE instructions support indexed addressing mode for internal program memory and for external data memory, when implemented.

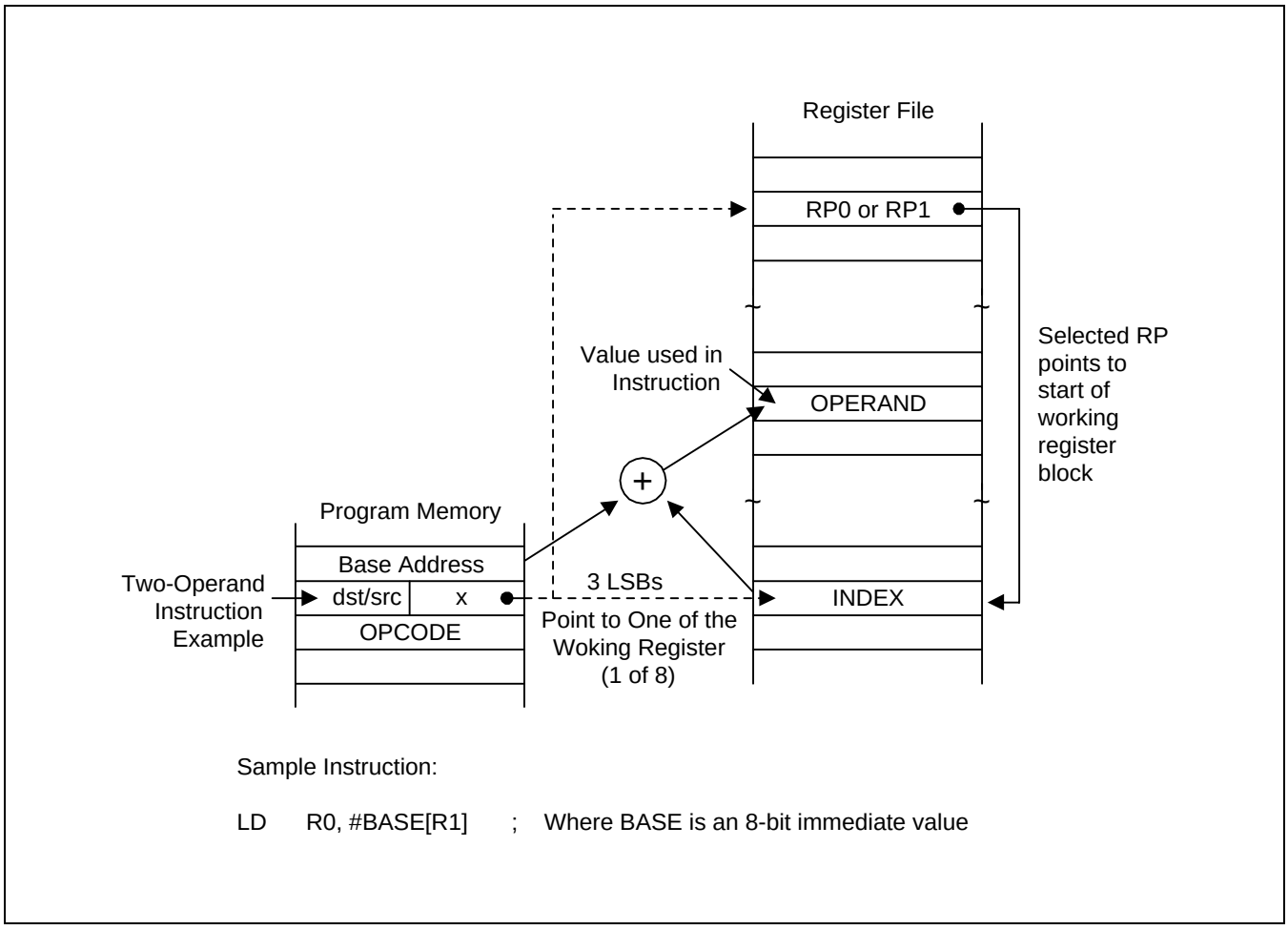
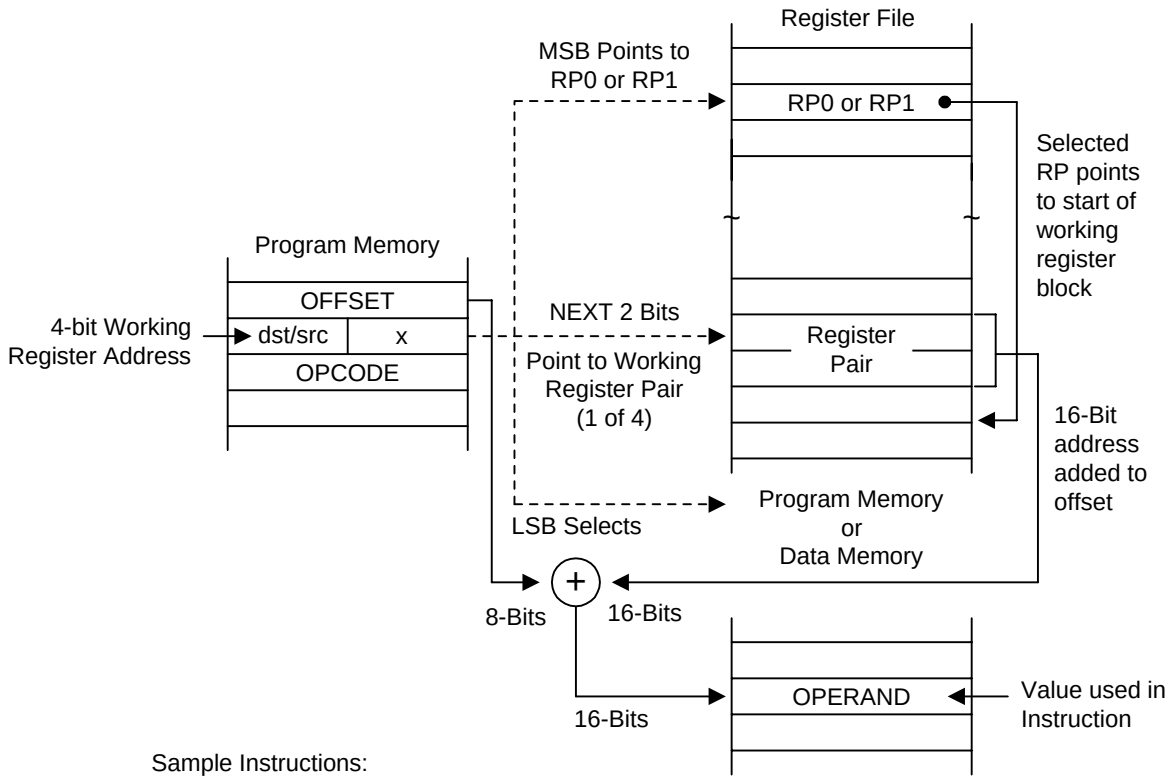


Figure 3-7. Indexed Addressing to Register File

INDEXED ADDRESSING MODE (Continued)

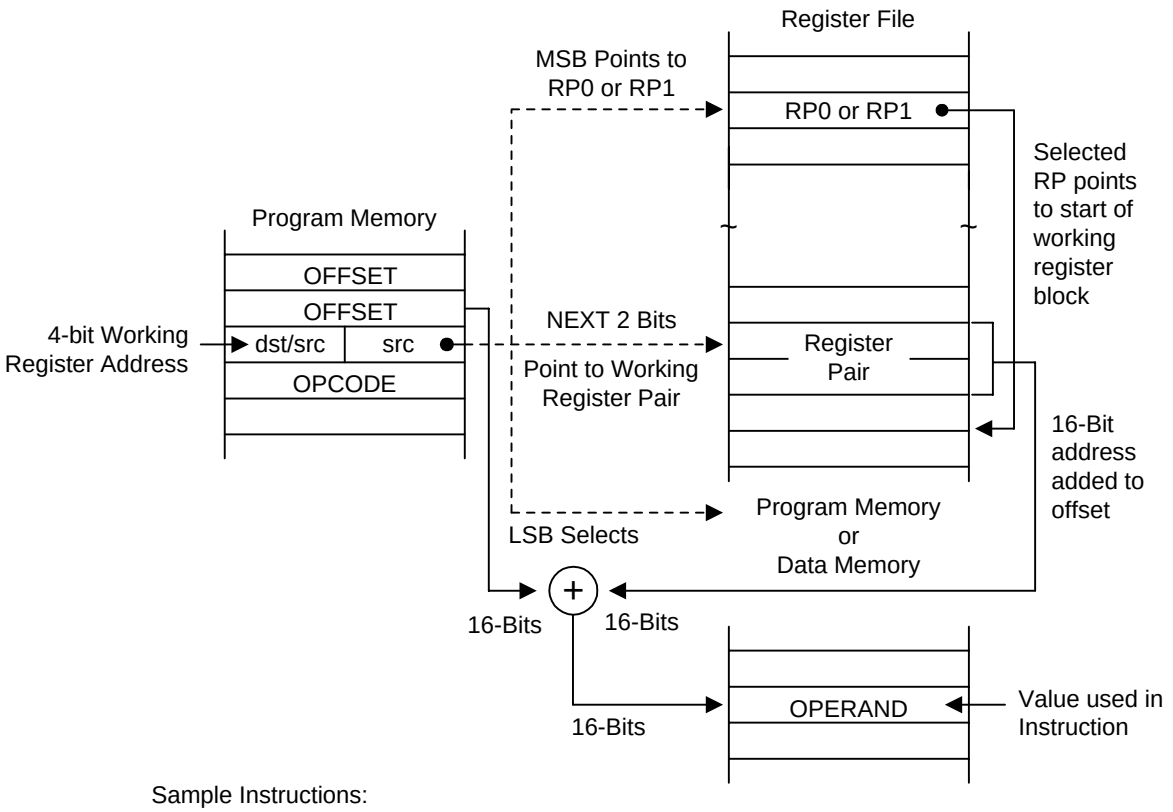


Sample Instructions:

```
LDC     R4, #04H[RR2]     ; The values in the program address (RR2 + 04H)
                          ; are loaded into register R4.
LDE     R4,#04H[RR2]      ; Identical operation to LDC example, except that
                          ; external program memory is accessed.
```

Figure 3-8. Indexed Addressing to Program or Data Memory with Short Offset

INDEXED ADDRESSING MODE (Continued)



Sample Instructions:

```
LDC     R4, #1000H[RR2]     ; The values in the program address (RR2 + 1000H)
                              are loaded into register R4.
LDE     R4,#1000H[RR2]      ; Identical operation to LDC example, except that
                              external program memory is accessed.
```

Figure 3-9. Indexed Addressing to Program or Data Memory

DIRECT ADDRESS MODE (DA)

In Direct Address (DA) mode, the instruction provides the operand's 16-bit memory address. Jump (JP) and Call (CALL) instructions use this addressing mode to specify the 16-bit destination address that is loaded into the PC whenever a JP or CALL instruction is executed.

The LDC and LDE instructions can use Direct Address mode to specify the source or destination address for Load operations to program memory (LDC) or to external data memory (LDE), if implemented.

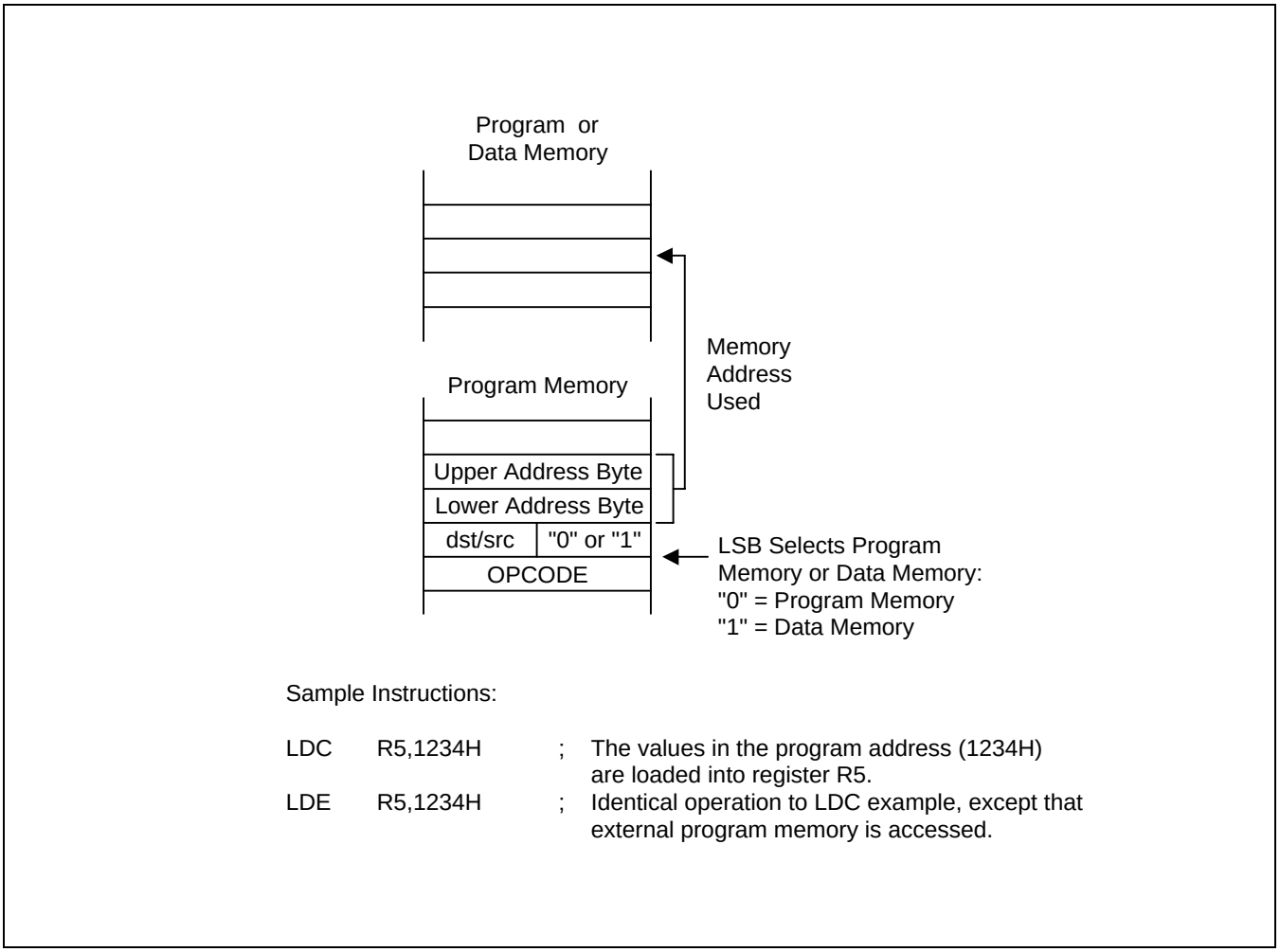
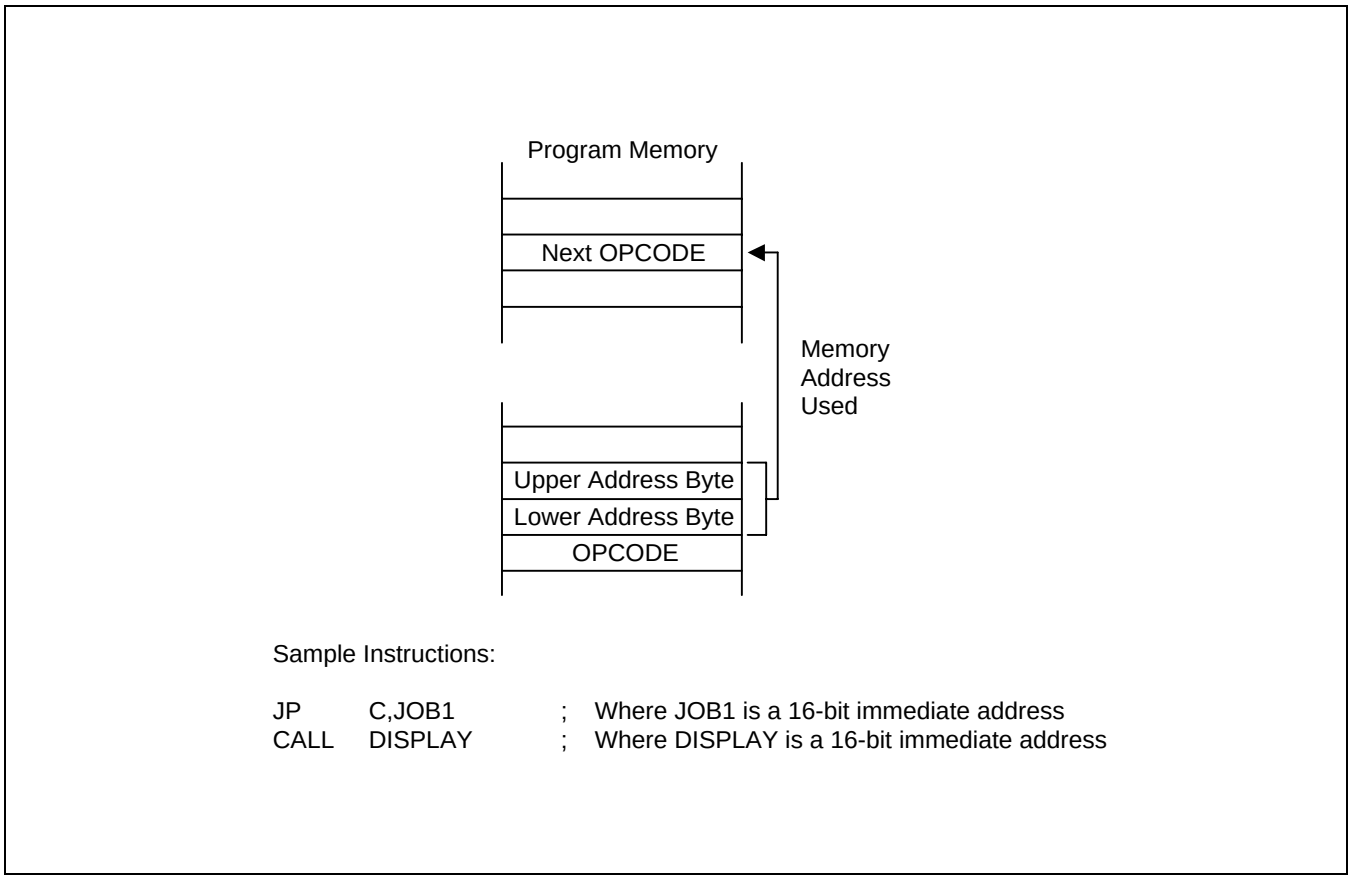


Figure 3-10. Direct Addressing for Load Instructions

DIRECT ADDRESS MODE (Continued)



Sample Instructions:

```
JP      C,JOB1      ;  Where JOB1 is a 16-bit immediate address
CALL    DISPLAY     ;  Where DISPLAY is a 16-bit immediate address
```

Figure 3-11. Direct Addressing for Call and Jump Instructions

INDIRECT ADDRESS MODE (IA)

In Indirect Address (IA) mode, the instruction specifies an address located in the lowest 256 bytes of the program memory. The selected pair of memory locations contains the actual address of the next instruction to be executed. Only the CALL instruction can use the Indirect Address mode.

Because the Indirect Address mode assumes that the operand is located in the lowest 256 bytes of program memory, only an 8-bit address is supplied in the instruction; the upper bytes of the destination address are assumed to be all zeros.

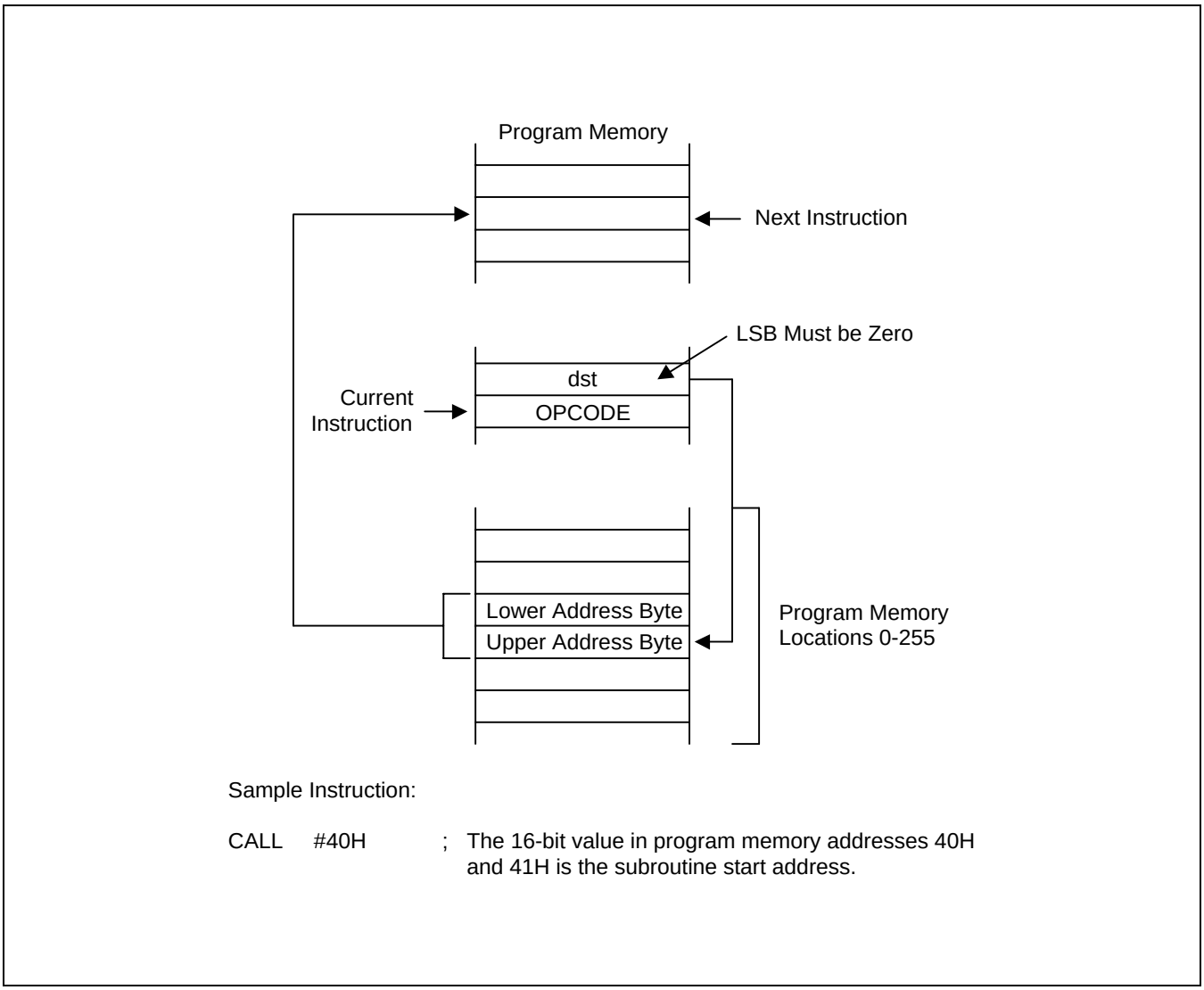


Figure 3-12. Indirect Addressing

RELATIVE ADDRESS MODE (RA)

In Relative Address (RA) mode, a twos-complement signed displacement between – 128 and + 127 is specified in the instruction. The displacement value is then added to the current PC value. The result is the address of the next instruction to be executed. Before this addition occurs, the PC contains the address of the instruction immediately following the current instruction.

Several program control instructions use the Relative Address mode to perform conditional jumps. The instructions that support RA addressing are BTJRF, BTJRT, DJNZ, CPIJE, CPIJNE, and JR.

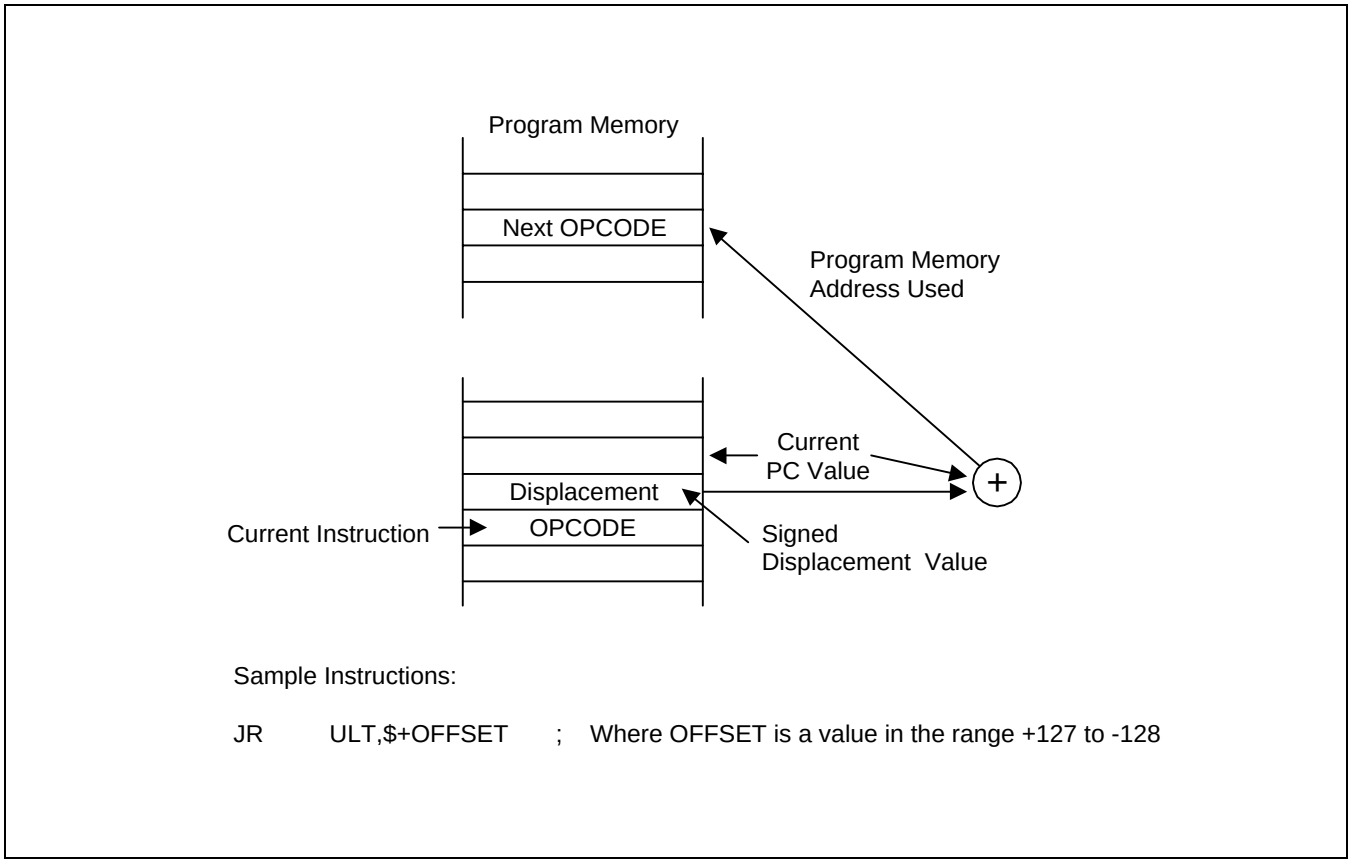


Figure 3-13. Relative Addressing

IMMEDIATE MODE (IM)

In Immediate (IM) addressing mode, the operand value used in the instruction is the value supplied in the operand field itself. The operand may be one byte or one word in length, depending on the instruction used. Immediate addressing mode is useful for loading constant values into registers.

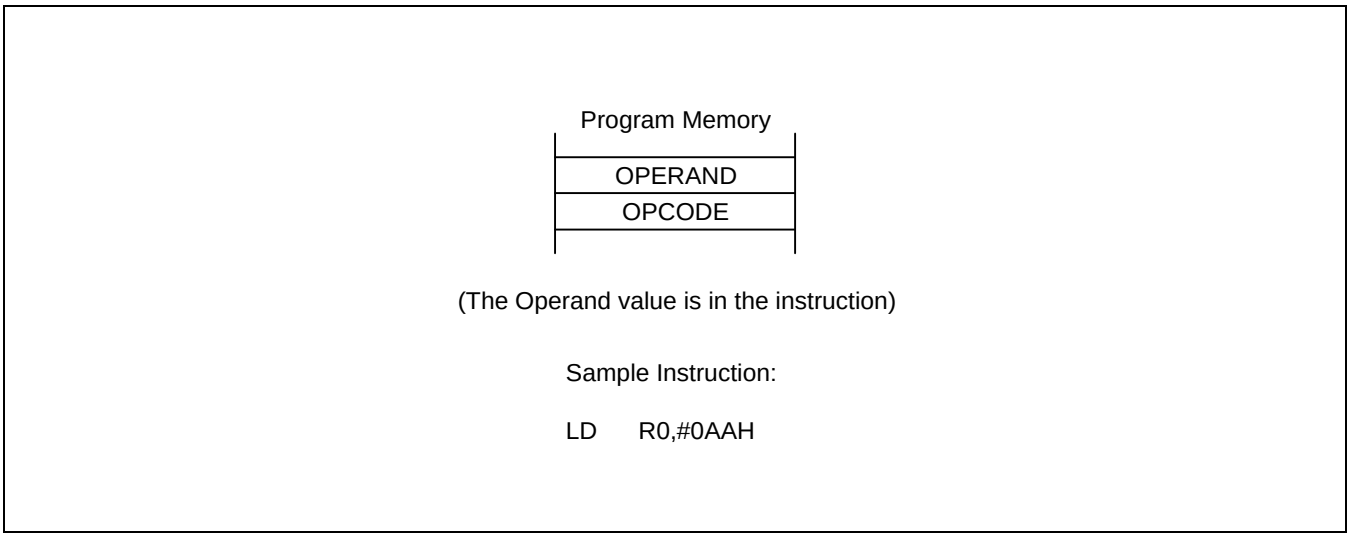


Figure 3-14. Immediate Addressing

4 CONTROL REGISTERS

OVERVIEW

Control register descriptions are arranged in alphabetical order according to register mnemonic. More detailed information about control registers is presented in the context of the specific peripheral hardware descriptions in Part II of this manual.

The locations and read/write characteristics of all mapped registers in the S3F84NB register file are listed in Table 4-1. The hardware reset value for each mapped register is described in Chapter 8, “RESET and Power-Down."

Table 4-1. Set 1 Registers

Register Name	Mnemonic	Decimal	Hex	R/W
Timer B control register	TBCON	208	D0H	R/W
Timer B data register (High Byte)	TBDATAH	209	D1H	R/W
Timer B data register (Low Byte)	TBDATAL	210	D2H	R/W
Basic timer control register	BTCON	211	D3H	R/W
Clock control register	CLKCON	212	D4H	R/W
System flags register	FLAGS	213	D5H	R/W
Register pointer 0	RP0	214	D6H	R/W
Register pointer 1	RP1	215	D7H	R/W
Stack pointer (High Byte)	SPH	216	D8H	R/W
Stack pointer (Low Byte)	SPL	217	D9H	R/W
Instruction pointer (High Byte)	IPH	218	DAH	R/W
Instruction pointer (Low Byte)	IPL	219	DBH	R/W
Interrupt request register	IRQ	220	DCH	R
Interrupt mask register	IMR	221	DDH	R/W
System mode register	SYM	222	DEH	R/W
Register page pointer	PP	223	DFH	R/W

Table 4-2. Set 1, Bank 0 Registers

Register Name	Mnemonic	Decimal	Hex	R/W
Port 0 data register	P0	224	E0H	R/W
Port 1 data register	P1	225	E1H	R/W
Port 2 data register	P2	226	E2H	R/W
Port 3 data register	P3	227	E3H	R/W
Port 4 data register	P4	228	E4H	R/W
Port 5 data register	P5	229	E5H	R/W
Port 6 data register	P6	230	E6H	R/W
Timer A, Timer 1 interrupt pending register	TINTPND	231	E7H	R/W
Port 6 control register (High Byte)	P6CONH	232	E8H	R/W
Port 6 control register (Low Byte)	P6CONL	233	E9H	R/W
Timer A control register	TACON	234	EAH	R/W
Timer A data register	TADATA	235	EBH	R/W
Timer A counter register	TACNT	236	ECH	R
Port 6 interrupt control register	P6INT	237	EDH	R/W
Port 6 interrupt/pending register	P6INTPND	238	EEH	R/W
Port 0 control register	P0CON	239	EFH	R/W
Port 1 control register (High Byte)	P1CONH	240	F0H	R/W
Port 1 control register (Low Byte)	P1CONL	241	F1H	R/W
Port 2 control register (High Byte)	P2CONH	242	F2H	R/W
Port 2 control register (Low Byte)	P2CONL	243	F3H	R/W
Port 3 control register (High Byte)	P3CONH	244	F4H	R/W
Port 3 control register (Low Byte)	P3CONL	245	F5H	R/W
Port 4 control register (High Byte)	P4CONH	246	F6H	R/W
Port 4 control register (Low Byte)	P4CONL	247	F7H	R/W
Port 5 control register (High Byte)	P5CONH	248	F8H	R/W
Port 5 control register (Low Byte)	P5CONL	249	F9H	R/W
Port 4 interrupt control register	P4INT	250	FAH	R/W
Port 4 interrupt/pending register	P4INTPND	251	FBH	R/W
Location FCH is factory use only				
Basic timer counter data register	BTCNT	253	FDH	R
Location FEH is not mapped.				
Interrupt priority register	IPR	255	FFH	R/W

Table 4-3. Set 1, Bank 1 Registers

Register Name	Mnemonic	Decimal	Hex	R/W
SIO data register	SIODATA	224	E0H	R/W
SIO Control register	SIOCON	225	E1H	R/W
UART0 data register	UDATA0	226	E2H	R/W
UART0 control register	UARTCON0	227	E3H	R/W
UART0 baud rate data register	BRDATAH0	228	E4H	R/W
UART0 baud rate data register	BRDATAL0	229	E5H	R/W
Timer 1(0) data register (High Byte)	T1DATAH0	230	E6H	R/W
Timer 1(0) data register (Low Byte)	T1DATAL0	231	E7H	R/W
Timer 1(1) data register (High Byte)	T1DATAH1	232	E8H	R/W
Timer 1(1) data register (Low Byte)	T1DATAL1	233	E9H	R/W
Timer 1(0) control register	T1CON0	234	EAH	R/W
Timer 1(1) control register	T1CON1	235	EBH	R/W
Timer 1(0) counter register (High Byte)	T1CNTH0	236	ECH	R
Timer 1(0) counter register (Low Byte)	T1CNTL0	237	EDH	R
Timer 1(1) counter register (High Byte)	T1CNTH1	238	EEH	R
Timer 1(1) counter register (Low Byte)	T1CNTL1	239	EFH	R
Timer C(0) data register	TCDATA0	240	F0H	R/W
Timer C(1) data register	TCDATA1	241	F1H	R/W
Timer C(0) control register	TCCON0	242	F2H	R/W
Timer C(1) control register	TCCON1	243	F3H	R/W
SIO prescaler control register	SIOPS	244	F4H	R/W
Watch timer control register	WTCON	245	F5H	R/W
Oscillator control register	OSCCON	246	F6H	R/W
A/D converter control register	ADCON	247	F7H	R/W
A/D converter data register (High Byte)	ADDATAH	248	F8H	R
A/D converter data register (Low Byte)	ADDATAL	249	F9H	R
UART1 data register	UDATA1	250	FAH	R/W
UART1 control register	UARTCON1	251	FBH	R/W
UART pending register	UARTPND	252	FCH	R/W
STOP control register	STPCON	253	FDH	R/W
Pattern generation control register	PGCON	254	FEH	R/W
Pattern generation data register	PGDATA	255	FFH	R/W

Table 4-4. Page 8 Registers

Register Name	Mnemonic	Decimal	Hex	R/W
UART1 baud rate data register	BRDATAH1	0	00H	R/W
UART1 baud rate data register	BRDATAL1	1	01H	R/W
Flash memory sector address register (High byte)	FMSECH	2	02H	R/W
Flash memory sector address register (Low byte)	FMSECL	3	03H	R/W
Flash memory user programming enable register	FMUSR	4	04H	R/W
Flash memory control register	FMCON	5	05H	R/W

NOTE: When you use the SK-1000 (SK-8xx) MDS, The BRDATAH/BRDATAL of mnemonic isn't showed on the system register window of MDS application program. Because the BRDATAH/BRDATAL is located on the general register page 8.

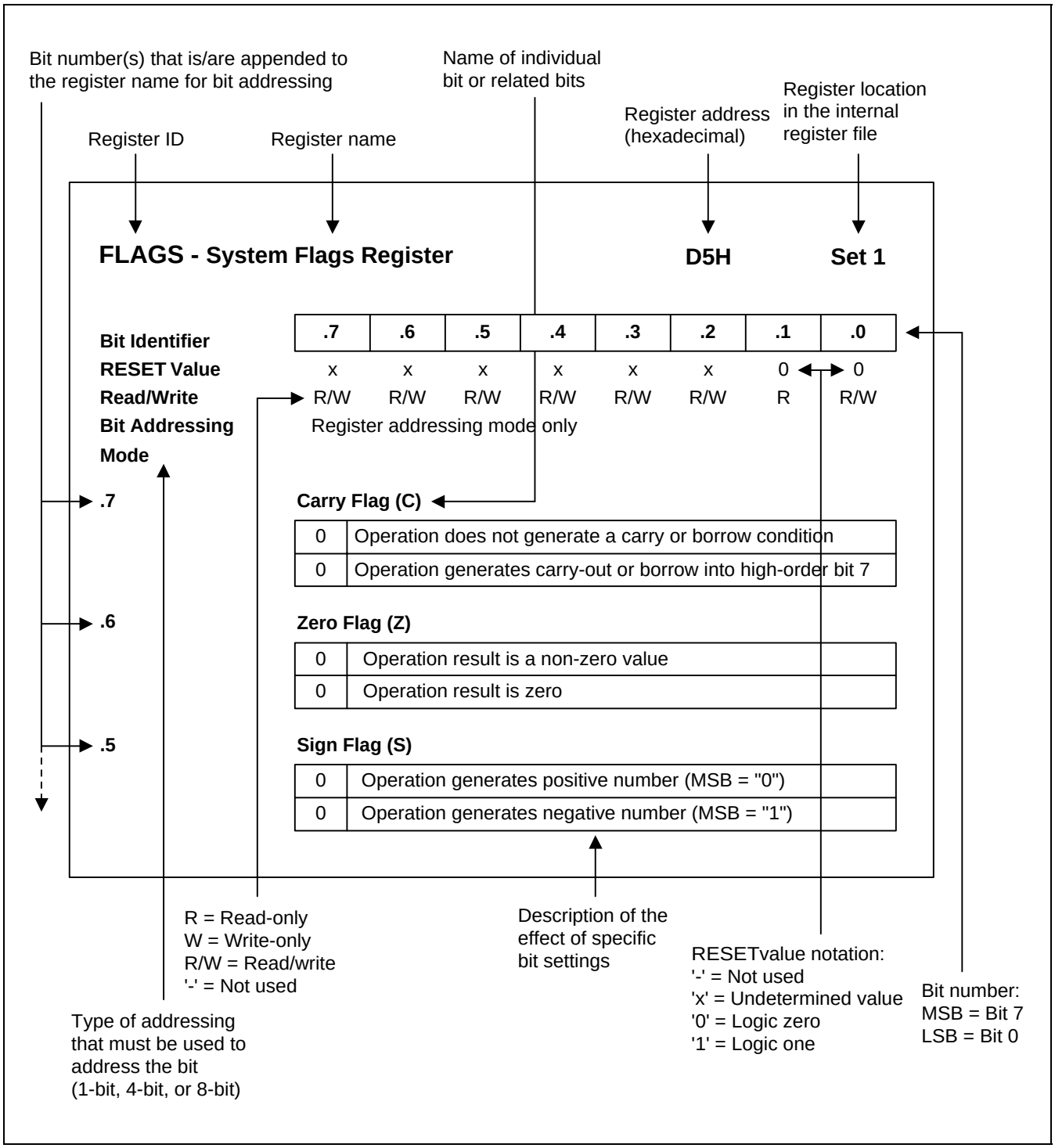


Figure 4-1. Register Description Format

ADCON – A/D Converter Control Register F7H Set 1, Bank 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	–	0	0	0	0	0	0	0
Read/Write	–	R/W	R/W	R/W	R	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7

Not used for the S3F84NB (must keep always 0)

.6- .4 A/D Input Pin Selection Bits

0	0	0	ADC0
0	0	1	ADC1
0	1	0	ADC2
0	1	1	ADC3
1	0	0	ADC4
1	0	1	ADC5
1	1	0	ADC6
1	1	1	ADC7

.3 End-of-Conversion Bit (Read-only)

0	A/D conversion opration is in progress
1	A/D conversion opration is complete

.2- .1 Clock Source Selection Bits

0	0	fxx/16
0	1	fxx/8
1	0	fxx/4
1	1	fxx

.0 Start or Enable Bit

0	Disable operation
1	Start operation

BTCON – Basic Timer Control Register D3H Set 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .4 Watchdog Timer Function Disable Code (for System Reset)

1	0	1	0	Disable watchdog timer function
Others				Enable watchdog timer function

.3- .2 Basic Timer Input Clock Selection Bits

0	0	fxx/4096 (3)
0	1	fxx/1024
1	0	fxx/128
1	1	fxx/16

.1 Basic Timer Counter Clear Bit (1)

0	No effect
1	Clear the basic timer counter value

.0 Clock Frequency Divider Clear Bit for Basic Timer (2)

0	No effect
1	Clear both clock frequency dividers

NOTES:

1. When you write a “1” to BTCON.1, the basic timer counter value is cleared to "00H". Immediately following the write operation, the BTCON.1 value is automatically cleared to “0”.
2. When you write a "1" to BTCON.0, the corresponding frequency divider is cleared to "00H". Immediately following the write operation, the BTCON.0 value is automatically cleared to "0".
3. The fxx is selected clock for system (main OSC. or sub OSC.).

CLKCON – System Clock Control Register D4H Set 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	–	–	–	R/W	R/W	–	–	–
Addressing Mode	Register addressing mode only							

.7- .5 Not used for the S3F84NB (must keep always 0)

.4- .3 **CPU Clock (System Clock) Selection Bits (note)**

0	0	fxx/16
0	1	fxx/8
1	0	fxx/2
1	1	fxx/1 (non-divided)

.2- .0 Not used for the S3F84NB (must keep always 0)

NOTE: After a reset, the slowest clock (divided by 16) is selected as the system clock. To select faster clock speeds, load the appropriate values to CLKCON.3 and CLKCON.4.

FLAGS – System Flags Register D5H Set 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	x	x	x	x	x	x	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Addressing Mode	Register addressing mode only							

.7 Carry Flag (C)

0	Operation does not generate a carry or underflow condition
1	Operation generates a carry-out or underflow into high-order bit 7

.6 Zero Flag (Z)

0	Operation result is a non-zero value
1	Operation result is zero

.5 Sign Flag (S)

0	Operation generates a positive number (MSB = "0")
1	Operation generates a negative number (MSB = "1")

.4 Overflow Flag (V)

0	Operation result is $\leq$ +127 or $\geq$ –128
1	Operation result is > +127 or < –128

.3 Decimal Adjust Flag (D)

0	Add operation completed
1	Subtraction operation completed

.2 Half-Carry Flag (H)

0	No carry-out of bit 3 or no underflow into bit 3 by addition or subtraction
1	Addition generated carry-out of bit 3 or subtraction generated underflow into bit 3

.1 Fast Interrupt Status Flag (FIS)

0	Interrupt return (IRET) in progress (when read)
1	Fast interrupt service routine in progress (when read)

.0 Bank Address Selection Flag (BA)

0	Bank 0 is selected
1	Bank 1 is selected

FMCON – Flash Memory Control Register 05H Page 8

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	–	–	–	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .4 **Flash Memory Mode Selection Bits**

0101	Programming mode
1010	Erase mode
0110	Hard Lock mode
Others	Not used for S3F84NB

.3- .1

Not used for S3F84NB

.0 **Flash operation Start Bit** (available for Erase and Hard Lock mode only)

0	Operation stop bit
1	Operation start bit (auto cleared)

FMSECH – Flash Memory Sector Address Register (High byte) 02H Page 8

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .0 **Flash Memory Sector Address (High Byte)**

Note : The high-byte flash memory sector address pointer value is the higher eight bits of the 16-bit pointer address.

FMSECL – Flash Memory Sector Address Register (Low byte) 03H Page 8

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .0 **Flash Memory Sector Address (Low Byte)**

Note : The low-byte flash memory sector address pointer value is the lower eight bits of the 16-bit pointer address.

FMUSR – Flash Memory User Programming Enable Register 04H Page 8

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .0 **Flash Memory User Programming Enable Bits**

1	0	1	0	0	1	0	1	Enable user programming mode
Other values								Disable user programming mode

NOTES:

1. To enable flash memory user programming, write 10100101b to FMUSR.
2. To disable flash memory operation, write other value except “10100101b” into FMUSR.

IMR – Interrupt Mask Register DDH Set 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	x	x	x	x	x	x	x	x
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7 Interrupt Level 7 (IRQ7) Enable Bit

0	Disable (mask)
1	Enable (un-mask)

.6 Interrupt Level 6 (IRQ6) Enable Bit

0	Disable (mask)
1	Enable (un-mask)

.5 Interrupt Level 5 (IRQ5) Enable Bit

0	Disable (mask)
1	Enable (un-mask)

.4 Interrupt Level 4 (IRQ4) Enable Bit

0	Disable (mask)
1	Enable (un-mask)

.3 Interrupt Level 3 (IRQ3) Enable Bit

0	Disable (mask)
1	Enable (un-mask)

.2 Interrupt Level 2 (IRQ2) Enable Bit

0	Disable (mask)
1	Enable (un-mask)

.1 Interrupt Level 1 (IRQ1) Enable Bit

0	Disable (mask)
1	Enable (un-mask)

.0 Interrupt Level 0 (IRQ0) Enable Bit

0	Disable (mask)
1	Enable (un-mask)

NOTE: When an interrupt level is masked, any interrupt requests that may be issued are not recognized by the CPU.

IPH – Instruction Pointer (High Byte) DAH Set 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	x	x	x	x	x	x	x	x
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .0 Instruction Pointer Address (High Byte)

The high-byte instruction pointer value is the upper eight bits of the 16-bit instruction pointer address (IP15–IP8). The lower byte of the IP address is located in the IPL register (DBH).

IPL – Instruction Pointer (Low Byte) DBH Set 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	x	x	x	x	x	x	x	x
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .0 Instruction Pointer Address (Low Byte)

The low-byte instruction pointer value is the lower eight bits of the 16-bit instruction pointer address (IP7–IP0). The upper byte of the IP address is located in the IPH register (DAH).

IPR – Interrupt Priority Register FFH Set 1, Bank 0

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	x	x	x	x	x	x	x	x
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7, .4, and .1 Priority Control Bits for Interrupt Groups A, B, and C

0	0	0	Group priority undefined
0	0	1	B > C > A
0	1	0	A > B > C
0	1	1	B > A > C
1	0	0	C > A > B
1	0	1	C > B > A
1	1	0	A > C > B
1	1	1	Group priority undefined

.6 Interrupt Subgroup C Priority Control Bit

0	IRQ6 > IRQ7
1	IRQ7 > IRQ6

.5 Interrupt Group C Priority Control Bit

0	IRQ5 > (IRQ6, IRQ7)
1	(IRQ6, IRQ7) > IRQ5

.3 Interrupt Subgroup B Priority Control Bit

0	IRQ3 > IRQ4
1	IRQ4 > IRQ3

.2 Interrupt Group B Priority Control Bit

0	IRQ2 > (IRQ3, IRQ4)
1	(IRQ3, IRQ4) > IRQ2

.0 Interrupt Group A Priority Control Bit

0	IRQ0 > IRQ1
1	IRQ1 > IRQ0

IRQ – Interrupt Request Register DCH Set 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R	R	R	R	R	R	R	R
Addressing Mode	Register addressing mode only							

.7 Interrupt Level 7 (IRQ7) Request Pending Bit

0	Not pending
1	Pending

.6 Interrupt Level 6 (IRQ6) Request Pending Bit

0	Not pending
1	Pending

.5 Interrupt Level 5 (IRQ5) Request Pending Bit

0	Not pending
1	Pending

.4 Interrupt Level 4 (IRQ4) Request Pending Bit

0	Not pending
1	Pending

.3 Interrupt Level 3 (IRQ3) Request Pending Bit

0	Not pending
1	Pending

.2 Interrupt Level 2 (IRQ2) Request Pending Bit

0	Not pending
1	Pending

.1 Interrupt Level 1 (IRQ1) Request Pending Bit

0	Not pending
1	Pending

.0 Interrupt Level 0 (IRQ0) Request Pending Bit

0	Not pending
1	Pending

OSCCON – Oscillator Control Register F6H Set 1, Bank 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	–	–	–	–	0	0	–	0
Read/Write	–	–	–	–	R/W	R/W	–	R/W
Addressing Mode	Register addressing mode only							

.7- .4

Not used for the S3F84NB

.3 Main System Oscillator Control Bit

0	Main System Oscillator RUN
1	Main System Oscillator STOP

.2 Sub System Oscillator Control Bit

0	Sub system oscillator RUN
1	Sub system oscillator STOP

.1

Not used for the S3F84NB

.0 System Clock Selection Bit

0	Main oscillator select
1	Subsystem oscillator select

P0CON – Port 0 Control Register EFH Set 1, Bank 0

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .6 **P0.7/P0.6/P0.5/P0.4**

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	Alternative function mode (PGOUT<7:4>)

.5–.4 **P0.3/P0.2**

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	Alternative function mode (PGOUT<3:2>)

.3- .2 **P0.1**

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	Alternative function mode (PGOUT<1>)

.1- .0 **P0.0**

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	Alternative function mode (PGOUT<0>)

P1CONH – Port 1 Control Register (High Byte) F0H Set 1, Bank 0

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .6 P1.7/ADC7 Configration Bits

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	ADC input

.5- .4 P1.6/ADC6 Configration Bits

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	ADC input

.3- .2 P1.5/ADC5 Configration Bits

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	ADC input

.1- .0 P1.4/ADC4 Configration Bits

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	ADC input

P1CONL – Port 1 Control Register (Low Byte) F1H Set 1, Bank 0

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .6 **P1.3/ADC3 Configration Bits**

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	ADC input

.5- .4 **P1.2/ADC2 Configration Bits**

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	ADC input

.3- .2 **P1.1/ADC1 Configration Bits**

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	ADC input

.1- .0 **P1.0/ADC0 Configration Bits**

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	ADC input

P2CONH – Port 2 Control Register (High Byte) F2H Set 1, Bank 0

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .6 **P2.7/TAOUT**

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	Alternative output mode (TAOUT)

.5- .4 **P2.6/TACAP**

0	0	Input mode (TACAP)
0	1	Input mode, pull-up (TACAP)
1	0	Push-pull output
1	1	Alternative output mode (Not used)

.3- .2 **P2.5/TACK**

0	0	Input mode (TACK)
0	1	Input mode, pull-up (TACK)
1	0	Push-pull output
1	1	Alternative output mode (Not used)

.1- .0 **P2.4/ TBPWM**

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	Alternative output mode (TBPWM)

P2CONL – Port 2 Control Register (Low Byte) F3H Set 1, Bank 0

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .6 **P2.3/BUZOUT**

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	Alternative output mode (BUZOUT)

.5- .4 **P2.2/SCK**

0	0	Input mode (SCK input)
0	1	Input mode, pull-up (SCK input)
1	0	Push-pull output
1	1	Alternative output mode (SCK output)

.3- .2 **P2.1/SI**

0	0	Input mode (SI)
0	1	Input mode, pull-up (SI)
1	0	Push-pull output
1	1	Alternative output mode (Not used)

.1- .0 **P2.0/SO**

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	Alternative output mode (SO)

P3CONH – Port 3 Control Register (High Byte) F4H Set 1, Bank 0

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .6 **P3.7/TCOUT1**

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	Alternative output mode(TCOUT1)

.5- .4 **P3.6/TCOUT0**

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	Alternative output mode(TCOUT0)

.3- .2 **P3.5/ T1OUT1**

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	Alternative output mode(T1OUT1)

.1- .0 **P3.4/ T1OUT0**

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	Alternative output mode(T1OUT0)

P3CONL – Port 3 Control Register (Low Byte) F5H Set 1, Bank 0

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .6 **P3.3/T1CAP1**

0	0	Input mode (T1CAP1)
0	1	Input mode, pull-up (T1CAP1)
1	x	Push-pull output

.5- .4 **P3.2/ T1CAP0**

0	0	Input mode (T1CAP0)
0	1	Input mode, pull-up (T1CAP0)
1	x	Push-pull output

.3- .3 **P3.1/T1CK1**

0	0	Input mode (T1CK1)
0	1	Input mode, pull-up (T1CK1)
1	x	Push-pull output

.1- .0 **P3.0/T1CK0**

0	0	Input mode (T1CK0)
0	1	Input mode, pull-up (T1CK0)
1	x	Push-pull output

P4CONH – Port 4 Control Register (High Byte) F6H Set 1, Bank 0

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .6 **P4.7/INT7**

0	0	Input mode; falling edge interrupt
0	1	Input mode; rising edge interrupt
1	0	Input mode, pull-up; falling edge interrupt
1	1	Push-pull output

.5- .4 **P4.6/ INT6**

0	0	Input mode; falling edge interrupt
0	1	Input mode; rising edge interrupt
1	0	Input mode, pull-up; falling edge interrupt
1	1	Push-pull output

.3- .2 **P4.5/ INT5**

0	0	Input mode; falling edge interrupt
0	1	Input mode; rising edge interrupt
1	0	Input mode, pull-up; falling edge interrupt
1	1	Push-pull output

.1- .0 **P4.4/ INT4**

0	0	Input mode; falling edge interrupt
0	1	Input mode; rising edge interrupt
1	0	Input mode, pull-up; falling edge interrupt
1	1	Push-pull output

P4CONL – Port 4 Control Register (Low Byte) F7H Set 1, Bank 0

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .6 **P4.3/INT3**

0	0	Input mode; falling edge interrupt
0	1	Input mode; rising edge interrupt
1	0	Input mode, pull-up; falling edge interrupt
1	1	Push-pull output

.5- .4 **P4.2/INT2**

0	0	Input mode; falling edge interrupt
0	1	Input mode; rising edge interrupt
1	0	Input mode, pull-up; falling edge interrupt
1	1	Push-pull output

.3- .2 **P4.1/INT1**

0	0	Input mode; falling edge interrupt
0	1	Input mode; rising edge interrupt
1	0	Input mode, pull-up; falling edge interrupt
1	1	Push-pull output

.1- .0 **P4.0/INT0**

0	0	Input mode; falling edge interrupt
0	1	Input mode; rising edge interrupt
1	0	Input mode, pull-up; falling edge interrupt
1	1	Push-pull output

P4INT – Port 4 Interrupt Control Register FAH Set 1, Bank 0

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7 P4.7 External Interrupt (INT7) Enable Bit

0	Disable interrupt
1	Enable interrupt

.6 P4.6 External Interrupt (INT6) Enable Bit

0	Disable interrupt
1	Enable interrupt

.5 P4.5 External Interrupt (INT5) Enable Bit

0	Disable interrupt
1	Enable interrupt

.4 P4.4 External Interrupt (INT4) Enable Bit

0	Disable interrupt
1	Enable interrupt

.3 P4.3 External Interrupt (INT3) Enable Bit

0	Disable interrupt
1	Enable interrupt

.2 P4.2 External Interrupt (INT2) Enable Bit

0	Disable interrupt
1	Enable interrupt

.1 P4.1 External Interrupt (INT1) Enable Bit

0	Disable interrupt
1	Enable interrupt

.0 P4.0 External Interrupt (INT0) Enable Bit

0	Disable interrupt
1	Enable interrupt

P4INTPND – Port 4 Interrupt Pending Register FBH Set 1, Bank 0

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7 P4.7/PND7 Interrupt Pending Bit

0	Interrupt request is not pending, pending bit clear when write 0
1	Interrupt request is pending

.6 P4.6/PND6 Interrupt Pending Bit

0	Interrupt request is not pending, pending bit clear when write 0
1	Interrupt request is pending

.5 P4.5/PND5 Interrupt Pending Bit

0	Interrupt request is not pending, pending bit clear when write 0
1	Interrupt request is pending

.4 P4.4/PND4 Interrupt Pending Bit

0	Interrupt request is not pending, pending bit clear when write 0
1	Interrupt request is pending

.3 P4.3/PND3 Interrupt Pending Bit

0	Interrupt request is not pending, pending bit clear when write 0
1	Interrupt request is pending

.2 P4.2/PND2 Interrupt Pending Bit

0	Interrupt request is not pending, pending bit clear when write 0
1	Interrupt request is pending

.1 P4.1/PND1 Interrupt Pending Bit

0	Interrupt request is not pending, pending bit clear when write 0
1	Interrupt request is pending

.0 P4.0/PND0 Interrupt Pending Bit

0	Interrupt request is not pending, pending bit clear when write 0
1	Interrupt request is pending

P5CONH – Port 5 Control Register (High Byte) F8H Set 1, Bank 0

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .6 **P5.7**

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	Open-drain output

.5- .4 **P5.6**

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	Open-drain output

.3- .2 **P5.5**

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	Open-drain output

.1- .0 **P5.4**

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	Open-drain output

P5CONL – Port 5 Control Register (Low Byte) F9H Set 1, Bank 0

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .6 **P5.3/RxD0**

0	0	Input mode (RxD0 input)
0	1	Input mode, pull-up (RxD0 input)
1	0	Push-pull output
1	1	Alternative output (RxD0 output)

.5- .4 **P5.2/TxD0**

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	Alternative output (TxD0 output)

.3- .2 **P5.1/RxD1**

0	0	Input mode (RxD1 input)
0	1	Input mode, pull-up (RxD1 input)
1	0	Push-pull output
1	1	Alternative output (RxD1 output)

.1- .0 **P5.0/TxD1**

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	Alternative output (TxD1 output)

P6CONH – Port 6 Control Register (High Byte) E8H Set 1, Bank 0

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .6 **P6.7/INT13**

0	0	Input mode; falling edge interrupt
0	1	Input mode; rising edge interrupt
1	0	Input mode, pull-up; falling edge interrupt
1	1	Push-pull output

.5- .4 **P6.6/ INT12**

0	0	Input mode; falling edge interrupt
0	1	Input mode; rising edge interrupt
1	0	Input mode, pull-up; falling edge interrupt
1	1	Push-pull output

.3- .2 **P6.5/ INT11**

0	0	Input mode; falling edge interrupt
0	1	Input mode; rising edge interrupt
1	0	Input mode, pull-up; falling edge interrupt
1	1	Push-pull output

.1- .0 **P6.4/ INT10**

0	0	Input mode; falling edge interrupt
0	1	Input mode; rising edge interrupt
1	0	Input mode, pull-up; falling edge interrupt
1	1	Push-pull output

P6CONL – Port 6 Control Register (Low Byte) E9H Set 1, Bank 0

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	1	1	1	1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .6 **P6.3/INT9**

0	0	Input mode; falling edge interrupt
0	1	Input mode; rising edge interrupt
1	0	Input mode, pull-up; falling edge interrupt
1	1	Push-pull output

.5- .4 **P6.2/INT8**

0	0	Input mode; falling edge interrupt
0	1	Input mode; rising edge interrupt
1	0	Input mode, pull-up; falling edge interrupt
1	1	Push-pull output

.3- .2 **P6.1/XT_{OUT}**

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	Alternative function (Sub-Clock Oscillator Output, XT_{OUT})

.1- .0 **P6.0/XT_{IN}**

0	0	Input mode
0	1	Input mode, pull-up
1	0	Push-pull output
1	1	Alternative function (Sub-Clock Oscillator Input, XT_{IN})

P6INT – Port 6 Interrupt Control Register EDH Set 1, Bank 0

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	–	–
Addressing Mode	Register addressing mode only							

.7 P6.7 External Interrupt (INT13) Enable Bit

0	Disable interrupt
1	Enable interrupt

.6 P6.6 External Interrupt (INT12) Enable Bit

0	Disable interrupt
1	Enable interrupt

.5 P6.5 External Interrupt (INT11) Enable Bit

0	Disable interrupt
1	Enable interrupt

.4 P6.4 External Interrupt (INT10) Enable Bit

0	Disable interrupt
1	Enable interrupt

.3 P6.3 External Interrupt (INT9) Enable Bit

0	Disable interrupt
1	Enable interrupt

.2 P6.2 External Interrupt (INT8) Enable Bit

0	Disable interrupt
1	Enable interrupt

.1- .0

Not used for the S3F84NB (must keep always 0)

P6INTPND – Port 6 Interrupt Pending Register EEH Set 1, Bank 0

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	–	–
Addressing Mode	Register addressing mode only							

.7 P6.7/PND13 Interrupt Pending Bit

0	Interrupt request is not pending, pending bit clear when write 0
1	Interrupt request is pending

.6 P6.6/PND12 Interrupt Pending Bit

0	Interrupt request is not pending, pending bit clear when write 0
1	Interrupt request is pending

.5 P6.5/PND11 Interrupt Pending Bit

0	Interrupt request is not pending, pending bit clear when write 0
1	Interrupt request is pending

.4 P6.4/PND10 Interrupt Pending Bit

0	Interrupt request is not pending, pending bit clear when write 0
1	Interrupt request is pending

.3 P6.3/PND9 Interrupt Pending Bit

0	Interrupt request is not pending, pending bit clear when write 0
1	Interrupt request is pending

.2 P6.2/PND8 Interrupt Pending Bit

0	Interrupt request is not pending, pending bit clear when write 0
1	Interrupt request is pending

.1- .0

Not used for the S3F84NB (must keep always 0)

PGCON – Pattern Generation Control Register FEH Set 1, Bank 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	–	–	–	–	0	0	0	0
Read/Write	–	–	–	–	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .4

Not used for the S3F84NB

.3 Software Trigger Start Bit

0	No effect
1	Software trigger start (will be automatically clear)

.2 PG Operation Disable/Enable Selection Bit

0	PG operation disable
1	PG operation enable

.1- .0 PG Operation Trigger Mode Selection Bits

0	0	Timer A match siganal triggering
0	1	Timer B underflow siganal triggering
1	0	Timer 1(0) match siganal triggering
1	1	Software triggering mode

PP – Register Page Pointer DFH Set 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7– .4 Destination Register Page Selection Bits

0	0	0	0	Destination: page 0
0	0	0	1	Destination: page 1
0	0	1	0	Destination: page 2
0	0	1	1	Destination: page 3
0	1	0	0	Destination: page 4
0	1	0	1	Destination: page 5
0	1	1	0	Destination: page 6
0	1	1	1	Destination: page 7
1	0	0	0	Destination: page 8
Other values				Don't care

.3- .0 Source Register Page Selection Bits

0	0	0	0	Source: page 0
0	0	0	1	Source: page 1
0	0	1	0	Source: page 2
0	0	1	1	Source: page 3
0	1	0	0	Source: page 4
0	1	0	1	Source: page 5
0	1	1	0	Source: page 6
0	1	1	1	Source: page 7
1	0	0	0	Source: page 8
Other values				Don't care

NOTES:

1. In the S3F84NB microcontroller, the internal register file is configured as eight pages (Pages 0-7). The pages 0-1 are used for the general-purpose register file, and page 2-7 is used for data register or general purpose registers.
2. When you used the SK-1000(SK-8xx) MDS , The BRDATAH1/BRDATAL1 of mnemonic isn't showed on the system register window of MDS application program. Because the BRDATAH1/BRDATAL1 is located on the general register page 8.

RP0 – Register Pointer 0 D6H Set 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	1	1	0	0	0	–	–	–
Read/Write	R/W	R/W	R/W	R/W	R/W	–	–	–
Addressing Mode	Register addressing only							

.7- .3 **Register Pointer 0 Address Value**

Register pointer 0 can independently point to one of the 256-byte working register areas in the register file. Using the register pointers RP0 and RP1, you can select two 8-byte register slices at one time as active working register space. After a reset, RP0 points to address C0H in register set 1, selecting the 8-byte working register slice C0H–C7H.

.2- .0 Not used for the S3F84NB

RP1 – Register Pointer 1 D7H Set 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	1	1	0	0	1	–	–	–
Read/Write	R/W	R/W	R/W	R/W	R/W	–	–	–
Addressing Mode	Register addressing only							

.7- .3 **Register Pointer 1 Address Value**

Register pointer 1 can independently point to one of the 256-byte working register areas in the register file. Using the register pointers RP0 and RP1, you can select two 8-byte register slices at one time as active working register space. After a reset, RP1 points to address C8H in register set 1, selecting the 8-byte working register slice C8H–CFH.

.2- .0 Not used for the S3F84NB

SIOCON – SIO Control Register E1H Set 1, Bank 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7 SIO Shift Clock Selection Bit

0	Internal clock (P.S clock)
1	External clock (SCK)

.6 Data Direction Control Bit

0	MSB first mode
1	LSB first mode

.5 SIO Mode Selection Bit

0	Receive only mode
1	Transmit/receive mode

.4 Shift Start Edge Selection Bit

0	Tx at falling edges, Rx at rising edges
1	Tx at rising edges, Rx at falling edges

.3 SIO Counter Clear and Shift Start Bit

0	No action
1	Clear 3-bit counter and start shifting (Auto clear bit)

.2 SIO Shift Operation Enable Bit

0	Disable shifter and clock counter
1	Enable shifter and clock counter

.1 SIO Interrupt Enable Bit

0	Disable SIO interrupt
1	Enable SIO interrupt

.0 SIO Interrupt Pending Bit

0	No interrupt pending
0	*Clear pending condition (when write)*
1	Interrupt is pending

SIOPS – SIO Prescaler Register F4H Set 1, Bank 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .0 Baud rate = Input clock (fxx)/[(SIOPS + 1) × 4] or SCK input clock

SPH – Stack Pointer (High Byte D8H Set 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	x	x	x	x	x	x	x	x
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .0 **Stack Pointer Address (High Byte)**

The high-byte stack pointer value is the upper eight bits of the 16-bit stack pointer address (SP15–SP8). The lower byte of the stack pointer value is located in register SPL (D9H). The SP value is undefined following a reset.

SPL – Stack Pointer (Low Byte) D9H Set 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	x	x	x	x	x	x	x	x
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .0 **Stack Pointer Address (Low Byte)**

The low-byte stack pointer value is the lower eight bits of the 16-bit stack pointer address (SP7–SP0). The upper byte of the stack pointer value is located in register SPH (D8H). The SP value is undefined following a reset.

STPCON – Stop Control Register FDH Set 1, Bank 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .0 STOP Control Bits

1 0 1 0 0 1 0 1	Enable stop instruction
Other values	Disable stop instruction

NOTE: Before execute the STOP instruction, You must set this STPCON register as “10100101b”. Otherwise the STOP instruction will not be executed.

SYM – System Mode Register DEH Set 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	–	–	x	x	x	0	0
Read/Write	–	–	–	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7 Not used, But you must keep always 0

.6 and .5 Not used for S3F84NB

.4- .2 **Fast Interrupt Level Selection Bits**

0	0	0	IRQ0
0	0	1	IRQ1
0	1	0	IRG2
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

.1 **Fast Interrupt Enable Bit**

0	Disable fast interrupt processing
1	Enable fast interrupt processing

.0 **Global Interrupt Enable Bit** (note)

0	Disable global interrupt processing
1	Enable global interrupt processing

NOTE: Following a reset, you enable global interrupt processing by executing an EI instruction (not by writing a "1" to SYM.0).

T1CON0 – Timer 1(0) Control Register EAH Set 1, Bank 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .5 Timer 1(0) Input Clock Selection Bits

0	0	0	fxx/1024
0	0	1	fxx/256
0	1	0	fxx/64
0	1	1	fxx/8
1	0	0	fxx
1	0	1	External clock falling edge
1	1	0	External clock rising edge
1	1	1	Counter stop

.4- .3 Timer 1(0) Operating Mode Selection Bits

0	0	Interval mode
0	1	Capture mode (Capture on rising edge, OVF can occur)
1	0	Capture mode (Capture on falling edge, OVF can occur)
1	1	PWM mode

.2 Timer 1(0) Counter Enable Bit

0	No effect
1	Clear the timer 1(0) counter (Auto-clear bit)

.1 Timer 1(0) Match/Capture Interrupt Enable Bit

0	Disable interrupt
1	Enable interrupt

.0 Timer 1(0) Overflow Interrupt Enable

0	Disable overflow interrupt
1	Enable overflow interrupt

T1CON1 – Timer 1(1) Control Register EBH Set 1, Bank 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .5 Timer 1(1) Input Clock Selection Bits

0	0	0	fxx/1024
0	0	1	fxx/256
0	1	0	fxx/64
0	1	1	fxx/8
1	0	0	fxx
1	0	1	External clock falling edge
1	1	0	External clock rising edge
1	1	1	Counter stop

.4- .3 Timer 1(1) Operating Mode Selection Bits

0	0	Interval mode
0	1	Capture mode (Capture on rising edge, OVF can occur)
1	0	Capture mode (Capture on falling edge, OVF can occur)
1	1	PWM mode

.2 Timer 1(1) Counter Enable Bit

0	No effect
1	Clear the timer 1(1) counter (Auto-clear bit)

.1 Timer 1(1) Match/Capture Interrupt Enable Bit

0	Disable interrupt
1	Enable interrupt

.0 Timer 1(1) Overflow Interrupt Enable

0	Disable overflow interrupt
1	Enable overflow interrupt

TACON – Timer A Control Register EAH Set 1, Bank 0

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .6 Timer A Input Clock Selection Bits

0	0	fxx/1024
0	1	fxx/256
1	0	fxx/64
1	1	External clock (TACK)

.5- .4 Timer A Operating Mode Selection Bits

0	0	Interval mode (TAOUT mode)
0	1	Capture mode (capture on rising edge, counter running, OVF can occur)
1	0	Capture mode (capture on falling edge, counter running, OVF can occur)
1	1	PWM mode (OVF interrupt can occur)

.3 Timer A Counter Clear Bit

0	No effect
1	Clear the timer A counter (Auto-clear bit)

.2 Timer A Overflow Interrupt Enable Bit

0	Disable overflow interrupt
1	Enable overflow interrupt

.1 Timer A Match/Capture Interrupt Enable Bit

0	Disable interrupt
1	Enable interrupt

.0 Timer A Start/Stop Bit

0	Stop Timer A
1	Start Timer A

TBCON – Timer B Control Register D0H Set 1, Bank 0

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .6 Timer B Input Clock Selection Bits

0	0	fxx/4
0	1	fxx/8
1	0	fxx/64
1	1	fxx/256

.5- .4 Timer B Interrupt Time Selection Bits

0	0	Elapsed time for low data value
0	1	Elapsed time for high data value
1	0	Elapsed time for low and high data values
1	1	Not Used

.3 Timer B Interrupt Enable Bit

0	Disable Interrupt
1	Enable Interrupt

.2 Timer B Start/Stop Bit

0	Stop timer B
1	Start timer B

.1 Timer B Mode Selection Bit

0	One-shot mode
1	Repeating mode

.0 Timer B Output flip-flop Control Bit

0	T-FF is low
1	T-FF is high

NOTE: fxx is selected clock for system.

TCCON0 – Timer C(0) Control Register F2H Set 1, Bank 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7 Timer C(0) Start/Stop Bit

0	Stop Timer C(0)
1	Start Timer C(0)

.6- .4 Timer C(0) 3-bits Prescaler Bits

0	0	0	Non devided
0	0	1	Divided by 2
0	1	0	Divided by 3
0	1	1	Divided by 4
1	0	0	Divided by 5
1	0	1	Divided by 6
1	1	0	Divided by 7
1	1	1	Divided by 8

.3 Timer C(0) Counter Clear Bit

0	No effect
1	Clear the timer C(0) counter (Auto-clear bit)

.2 Timer C(0) Mode Selection Bit

0	fxx/1 & PWM mode
1	fxx/64 & interval mode

.1 Timer C(0) Interrupt Enable Bit

0	Disable interrupt
1	Enable interrupt

.0 Timer C(0) Pending Bit

0	No interrupt pending
0	*Clear pending bit when write*
1	Interrupt pending

TCCON1 – Timer C(1) Control Register F3H Set 1, Bank 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7 Timer C(1) Start/Stop Bit

0	Stop Timer C(1)
1	Start Timer C(1)

.6- .4 Timer C(1) 3-bits Prescaler Bits

0	0	0	Non devided
0	0	1	Divided by 2
0	1	0	Divided by 3
0	1	1	Divided by 4
1	0	0	Divided by 5
1	0	1	Divided by 6
1	1	0	Divided by 7
1	1	1	Divided by 8

.3 Timer C(1) Counter Clear Bit

0	No effect
1	Clear the timer C(1) counter (Auto-clear bit)

.2 Timer C(1) Mode Selection Bit

0	fxx/1 & PWM mode
1	fxx/64 & interval mode

.1 Timer C(1) Interrupt Enable Bit

0	Disable interrupt
1	Enable interrupt

.0 Timer C(1) Pending Bit

0	No interrupt pending
0	*Clear pending bit when write*
1	Interrupt pending

TINTPND – Timer A, Timer 1 Interrupt Pending Register E7H Set 1, Bank 0

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	–	–	0	0	0	0	0	0
Read/Write	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .6 Not used for the S3F84NB

.5 Timer 1(1) Overflow Interrupt Pending Bit

0	No interrupt pending
0	*Clear pending bit when write*
1	Interrupt pending

.4 Timer 1(1) Match/Capture Interrupt Pending Bit

0	No interrupt pending
0	*Clear pending bit when write*
1	Interrupt pending

.3 Timer 1(0) Overflow Interrupt Pending Bit

0	No interrupt pending
0	*Clear pending bit when write*
1	Interrupt pending

.2 Timer 1(0) Match/Capture Interrupt Pending Bit

0	No interrupt pending
0	*Clear pending bit when write*
1	Interrupt pending

.1 Timer A Overflow Interrupt Pending Bit

0	No interrupt pending
0	*Clear pending bit when write*
1	Interrupt pending

.0 Timer A Match/Capture Interrupt Pending Bit

0	No interrupt pending
0	*Clear pending bit when write*
1	Interrupt pending

UARTCON0 – UART0 Control Register E3H Set 1, Bank 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .6 Operating Mode and Baud Rate Selection Bits

0	0	Mode 0: Shite register [fxx/(16 × (16bit BRDATA + 1))]
0	1	Mode 1: 8-bit UART [fxx/(16 × (16bit BRDATA + 1))]
1	0	Mode 2: 9-bit UART [fxx/(16 × (16bit BRDATA + 1))]
1	1	Mode 3: 9-bit UART [fxx/(16 × (16bit BRDATA + 1))]

.5 Multiprocessor Communication(1) Enable Bit (for modes 2 and 3 only)

0	Disable
1	Enable

.4 Serial Data Receive Enable Bit

0	Disable
1	Enable

.3

If Parity disable mode (PEN0 = 0),
location of the 9th data bit to be transmitted in UART0 mode 2 or 3 ("0" or "1").

If Parity enable mode (PEN0 = 1),
even/odd parity selection bit for transmit data in UART0 mode 2 or 3.
0: Even parity bit generation for transmit data
1: Odd parity bit generation for transmit data

.2

If Parity disable (PEN0 = 0),
location of the 9th data bit that was received in UART0 mode 2 or 3 ("0" or "1").

If Parity enable mode (PEN0 = 1),
even/odd parity selection bit for receive data in UART0 mode 2 or 3.
0: Even parity check for the received data
1: Odd parity check for the received data

A result of parity error will be saved in PER0 bit of the UARTPND register after parity checking of the received data.

UARTCON0 – UART0 Control Register (Continued) E3H Set 1, Bank 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.1 Receive Interrupt Enable Bit

0	Disable Receive interrupt
1	Enable Receive interrupt

.0 Transmit Interrupt Enable Bit

0	Disable Transmit interrupt
1	Enable Transmit Interrupt

NOTES:

1. In mode 2 or 3, if the MCE (UARTCON.5) bit is set to "1", then the receive interrupt will not be activated if the received 9^{th} data bit is "0". In mode 1, if MCE = "1", then the receive interrupt will not be activated if a valid stop bit was not received. In mode 0, the MCE (UARTCON.5) bit should be "0".
2. The descriptions for 8-bit and 9-bit UART mode do not include start and stop bits for serial data receive and transmit.
3. Parity enable bits, PEN0 and PEN1, are located in the UARTPND register at address FCH, Bank 1.
4. Parity enable and parity error check can be available in 9-bit UART mode (Mode 2, 3) only.

UARTCON1 – UART1 Control Register FBH Set 1, Bank 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7- .6 Operating Mode and Baud Rate Selection Bits

0	0	Mode 0: Shift Register [fxx/(16 × (16bit BRDATA + 1))]
0	1	Mode 1: 8-bit UART [fxx/(16 × (16bit BRDATA + 1))]
1	0	Mode 2: 9-bit UART [fxx/(16 × (16bit BRDATA + 1))]
1	1	Mode 3: 9-bit UART [fxx/(16 × (16bit BRDATA + 1))]

.5 Multiprocessor Communication(1) Enable Bit (for modes 2 and 3 only)

0	Disable
1	Enable

.4 Serial Data Receive Enable Bit

0	Disable
1	Enable

.3

If Parity disable mode (PEN1 = 0),
location of the 9th data bit to be transmitted in UART1 mode 2 or 3 ("0" or "1").

If Parity enable mode (PEN1 = 1),
even/odd parity selection bit for transmit data in UART1 mode 2 or 3.
0: Even parity bit generation for transmit data
1: Odd parity bit generation for transmit data

.2

If Parity disable (PEN1 = 0),
location of the 9th data bit that was received in UART1 mode 2 or 3 ("0" or "1").

If Parity enable mode (PEN1 = 1),
even/odd parity selection bit for receive data in UART1 mode 2 or 3.
0: Even parity check for the received data
1: Odd parity check for the received data

A result of parity error will be saved in PER1 bit of the UARTPND register after parity checking of the received data.

UARTCON1 – UART1 Control Register (Continued) FBH Set 1, Bank 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.1 Receive Interrupt Enable Bit

0	Disable receive interrupt
1	Enable receive interrupt

.0 Transmit Interrupt Enable Bit

0	Disable transmit interrupt
1	Enable transmit Interrupt

NOTES:

1. In mode 2 or 3, if the MCE (UARTCON.5) bit is set to "1", then the receive interrupt will not be activated if the received 9th data bit is "0". In mode 1, if MCE = "1", then the receive interrupt will not be activated if a valid stop bit was not received. In mode 0, the MCE (UARTCON.5) bit should be "0".
2. The descriptions for 8-bit and 9-bit UART mode do not include start and stop bits for serial data receive and transmit.
3. Parity enable bits, PEN0 and PEN1, are located in the UARTPND register at address FCH, Bank 1.
4. Parity enable and parity error check can be available in 9-bit UART mode (Mode 2, 3) only.

UARTPND – UART0,1 Pending and parity control FCH Set 1, Bank 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7 UART1 Parity Enable/Disable (PEN1)

0	Disable
1	Enable

.6 UART1 Receive Parity Error (RPE1)

0	No error
1	Parity error

.5 UART0 Parity Enable/Disable (PEN0)

0	Disable
1	Enable

.4 UART0 Receive Parity Error (RPE0)

0	No error
1	Parity error

.3 UART1 Receive Interrupt Pending Flag

0	Not pending
0	*Clear pending bit (when write)*
1	Interrupt pending

.2 UART1 Transmit Interrupt Pending Flag

0	Not pending
0	*Clear pending bit (when write)*
1	Interrupt pending

.1 UART0 Receive Interrupt Pending Flag

0	Not pending
0	*Clear pending bit (when write)*
1	Interrupt pending

UARTPND – UART0,1 Pending and parity control(Continued) FCH Set 1, Bank 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.0 UART0 Transmit Interrupt Pending Flag

0	Not pending
0	*Clear pending bit (when write)*
1	Interrupt pending

NOTES:

1. In order to clear a data transmit or receive interrupt pending flag, you must write a "0" to the appropriate pending bit.
2. To avoid programming errors, we recommend using load instruction (except for LDB), when manipulating UARTPND values.
3. Parity enable and parity error check can be available in 9-bit UART mode (Mode 2, 3) only.
4. Parity error bit (RPE0, RPE1) will be refreshed whenever 8th receive data bit has been shifted.

WTCON – Watch Timer Control Register F5H Set 1, Bank 1

Bit Identifier	.7	.6	.5	.4	.3	.2	.1	.0
RESET Value	0	0	0	0	0	0	0	0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addressing Mode	Register addressing mode only							

.7 Watch Timer Clock Selection Bit

0	Main system clock divided by 256 (fxx/256)
1	Sub system clock (fxt)

.6 Watch Timer Interrupt Enable Bit

0	Disable watch timer interrupt
1	Enable watch timer interrupt

.5- .4 Buzzer Signal Selection Bits

0	0	0.5 kHz buzzer (BUZ) signal output
0	1	1 kHz buzzer (BUZ) signal output
1	0	2 kHz buzzer (BUZ) signal output
1	1	4 kHz buzzer (BUZ) signal output

.3- .2 Watch Timer Speed Selection Bits

0	0	0.5 s Interval
0	1	0.25 s Interval
1	0	0.125 s Interval
1	1	1.955 ms Interval

.1 Watch Timer Enable Bit

0	Disable watch timer; Clear frequency dividing circuits
1	Enable watch timer

.0 Watch Timer Interrupt Pending Bit

0	Interrupt is not pending
1	*Clear pending bit when write*
1	Interrupt is pending

5 INTERRUPT STRUCTURE

OVERVIEW

The S3C8-series interrupt structure has three basic components: levels, vectors, and sources. The SAM8 CPU recognizes up to eight interrupt levels and supports up to 128 interrupt vectors. When a specific interrupt level has more than one vector address, the vector priorities are established in hardware. A vector address can be assigned to one or more sources.

Levels

Interrupt levels are the main unit for interrupt priority assignment and recognition. All peripherals and I/O blocks can issue interrupt requests. In other words, peripheral and I/O operations are interrupt-driven. There are eight possible interrupt levels: IRQ0–IRQ7, also called level 0–level 7. Each interrupt level directly corresponds to an interrupt request number (IRQn). The total number of interrupt levels used in the interrupt structure varies from device to device. The S3F84NB interrupt structure recognizes eight interrupt levels.

The interrupt level numbers 0 through 7 do not necessarily indicate the relative priority of the levels. They are just identifiers for the interrupt levels that are recognized by the CPU. The relative priority of different interrupt levels is determined by settings in the interrupt priority register, IPR. Interrupt group and subgroup logic controlled by IPR settings lets you define more complex priority relationships between different levels.

Vectors

Each interrupt level can have one or more interrupt vectors, or it may have no vector address assigned at all. The maximum number of vectors that can be supported for a given level is 128 (The actual number of vectors used for S3C8-series devices is always much smaller). If an interrupt level has more than one vector address, the vector priorities are set in hardware. S3F84NB uses twenty-nine vectors.

Sources

A source is any peripheral that generates an interrupt. A source can be an external pin or a counter overflow. Each vector can have several interrupt sources. In the S3F84NB interrupt structure, there are twenty-nine possible interrupt sources.

When a service routine starts, the respective pending bit should be either cleared automatically by hardware or cleared "manually" by program software. The characteristics of the source's pending mechanism determine which method would be used to clear its respective pending bit.

INTERRUPT TYPES

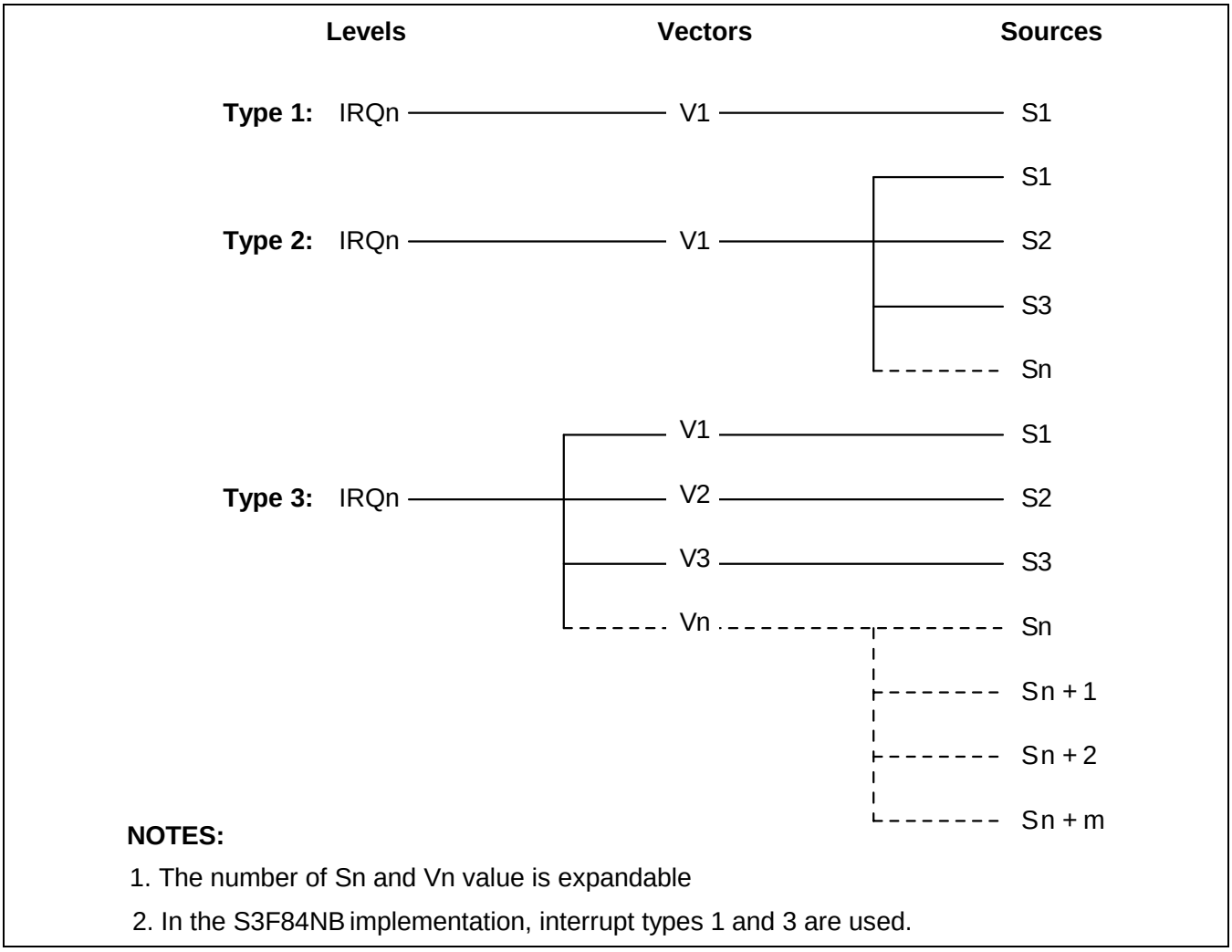
The three components of the S3C8 interrupt structure described before – levels, vectors, and sources – are combined to determine the interrupt structure of an individual device and to make full use of its available interrupt logic. There are three possible combinations of interrupt structure components, called interrupt types 1, 2, and 3. The types differ in the number of vectors and interrupt sources assigned to each level (see Figure 5-1):

Type 1: One level (IRQn) + one vector (V_1) + one source (S_1)

Type 2: One level (IRQn) + one vector (V_1) + multiple sources ($S_1 – S_n$)

Type 3: One level (IRQn) + multiple vectors ($V_1 – V_n$) + multiple sources ($S_1 – S_n$, $S_{n+1} – S_{n+m}$)

In the S3F84NB microcontroller, two interrupt types are implemented.



NOTES:

1. The number of Sn and Vn value is expandable
2. In the S3F84NB implementation, interrupt types 1 and 3 are used.

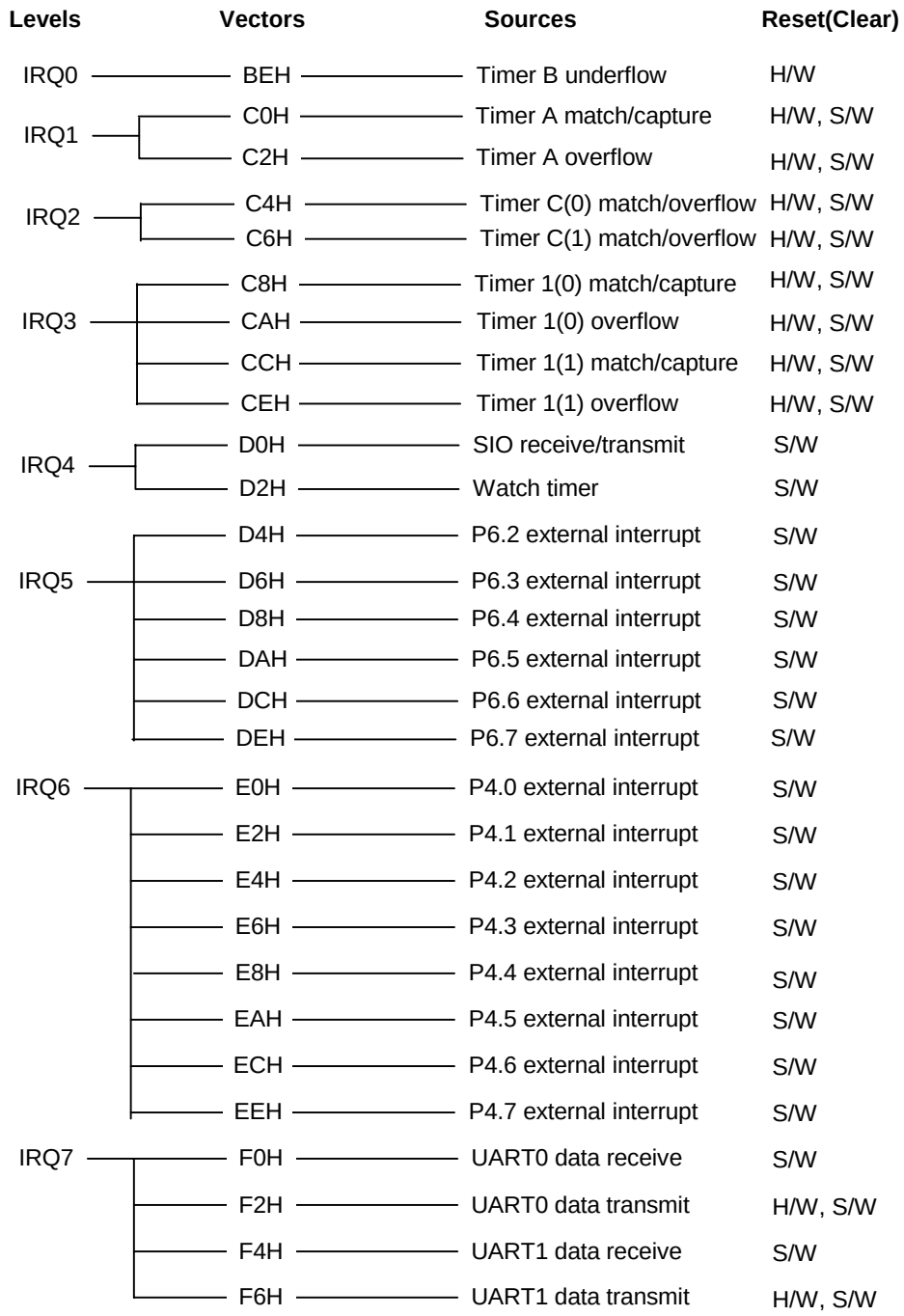
Figure 5-1. S3C8-Series Interrupt Types

S3F84NB INTERRUPT STRUCTURE

The S3F84NB microcontroller supports twenty-nine interrupt sources. All of the interrupt sources have a corresponding interrupt vector address. Eight interrupt levels are recognized by the CPU in this device-specific interrupt structure, as shown in Figure 5-2.

When multiple interrupt levels are active, the interrupt priority register (IPR) determines the order in which contending interrupts are to be serviced. If multiple interrupts occur within the same interrupt level, the interrupt with the lowest vector address is usually processed first (The relative priorities of multiple interrupts within a single level are fixed in hardware).

When the CPU grants an interrupt request, interrupt processing starts. All other interrupts are disabled and the program counter value and status flags are pushed to stack. The starting address of the service routine is fetched from the appropriate vector address (plus the next 8-bit value to concatenate the full 16-bit address) and the service routine is executed.



NOTES:

1. Within a given interrupt level, the lower vector address has high priority. For example, DCH has higher priority than DEH within the level IRQ5 the priorities within each level are set at the factory.
2. External interrupts are triggered by a rising or falling edge, depending on the corresponding control register setting.

Figure 5-2. S3F84NB Interrupt Structure

INTERRUPT VECTOR ADDRESSES

All interrupt vector addresses for the S3F84NB interrupt structure are stored in the vector address area of the internal 64-Kbyte flash memory, 0H–FFFFH (see Figure 5-3).

You can allocate unused locations in the vector address area as normal program memory. If you do so, please be careful not to overwrite any of the stored vector addresses (Table 5-1 lists all vector addresses).

The program reset address in the flash memory is 0100H.

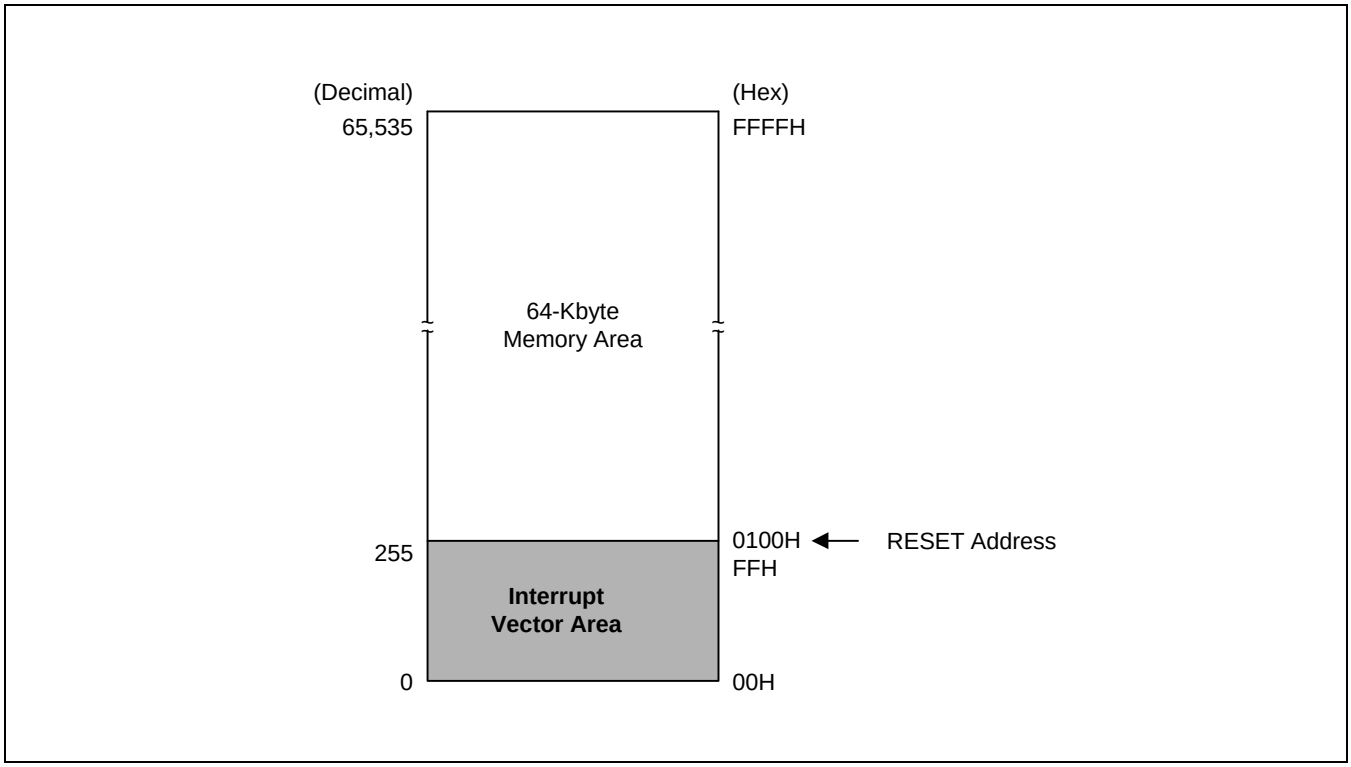


Figure 5-3. ROM Vector Address Area

Table 5-1. Interrupt Vectors

Vector Address		Interrupt Source	Request		Reset/Clear	
Decimal Value	Hex Value		Interrupt Level	Priority in Level	H/W	S/W
256	100H	Basic timer(WDT) overflow	RESETB	–	√	
246	F6H	UART1 transmit	IRQ7	3	√	
244	F4H	UART1 receive		2		√
242	F2H	UART0 transmit		1	√	
240	F0H	UART0 receive		0		√
238	EEH	P4.7 external interrupt	IRQ6	7		√
236	ECH	P4.6 external interrupt		6		√
234	EAH	P4.5 external interrupt		5		√
232	E8H	P4.4 external interrupt		4		√
230	E6H	P4.3 external interrupt		3		√
228	E4H	P4.2 external interrupt		2		√
226	E2H	P4.1 external interrupt		1		√
224	E0H	P4.0 external interrupt		0		√
222	DEH	P6.7 external interrupt	IRQ5	5		√
220	DCH	P6.6 external interrupt		4		√
218	DAH	P6.5 external interrupt		3		√
216	D8H	P6.4 external interrupt		2		√
214	D6H	P6.3 external interrupt		1		√
212	D4H	P6.2 external interrupt		0		√
210	D2H	Watch timer	IRQ4	1		√
208	D0H	SIO receive/transmit		0		√
206	CEH	Timer 1(1) overflow	IRQ3	3	√	√
204	CCH	Timer 1(1) match/capture		2	√	√
202	CAH	Timer 1(0) overflow		1	√	√
200	C8H	Timer 1(0) match/capture		0	√	√
198	C6H	Timer C(1) match/overflow	IRQ2	1	√	√
196	C4H	Timer C(0) match/overflow		0	√	√
194	C2H	Timer A overflow	IRQ1	1	√	√
192	C0H	Timer A match/capture		0	√	√
190	BEH	Timer B underflow	IRQ0	–	√	

NOTES:

1. Interrupt priorities are identified in inverse order: "0" is the highest priority, "1" is the next highest, and so on.
2. If two or more interrupts within the same level contend, the interrupt with the lowest vector address usually has priority over one with a higher vector address. The priorities within a given level are fixed in hardware.

ENABLE/DISABLE INTERRUPT INSTRUCTIONS (EI, DI)

Executing the Enable Interrupts (EI) instruction globally enables the interrupt structure. All interrupts are then serviced as they occur according to the established priorities.

NOTE

The system initialization routine executed after a reset must always contain an EI instruction to globally enable the interrupt structure.

During the normal operation, you can execute the DI (Disable Interrupt) instruction at any time to globally disable interrupt processing. The EI and DI instructions change the value of bit 0 in the SYM register.

SYSTEM-LEVEL INTERRUPT CONTROL REGISTERS

In addition to the control registers for specific interrupt sources, four system-level registers control interrupt processing:

- The interrupt mask register, IMR, enables (un-masks) or disables (masks) interrupt levels.
- The interrupt priority register, IPR, controls the relative priorities of interrupt levels.
- The interrupt request register, IRQ, contains interrupt pending flags for each interrupt level (as opposed to each interrupt source).
- The system mode register, SYM, enables or disables global interrupt processing (SYM settings also enable fast interrupts and control the activity of external interface, if implemented).

Table 5-2. Interrupt Control Register Overview

Control Register	ID	R/W	Function Description
Interrupt mask register	IMR	R/W	Bit settings in the IMR register enable or disable interrupt processing for each of the eight interrupt levels: IRQ0–IRQ7.
Interrupt priority register	IPR	R/W	Controls the relative processing priorities of the interrupt levels. The seven levels of S3F84NB are organized into three groups: A, B, and C. Group A is IRQ0 and IRQ1, group B is IRQ2, IRQ3 and IRQ4, and group C is IRQ5, IRQ6, and IRQ7.
Interrupt request register	IRQ	R	This register contains a request pending bit for each interrupt level.
System mode register	SYM	R/W	This register enables/disables fast interrupt processing, dynamic global interrupt processing.

NOTE: Before IMR register is changed to any value, all interrupts must be disable.
Using DI instruction is recommended.

INTERRUPT PROCESSING CONTROL POINTS

Interrupt processing can therefore be controlled in two ways: globally or by specific interrupt level and source. The system-level control points in the interrupt structure are:

- Global interrupt enable and disable (by EI and DI instructions or by direct manipulation of SYM.0)
- Interrupt level enable/disable settings (IMR register)
- Interrupt level priority settings (IPR register)
- Interrupt source enable/disable settings in the corresponding peripheral control registers

NOTE

When writing an application program that handles interrupt processing, be sure to include the necessary register file address (register pointer) information.

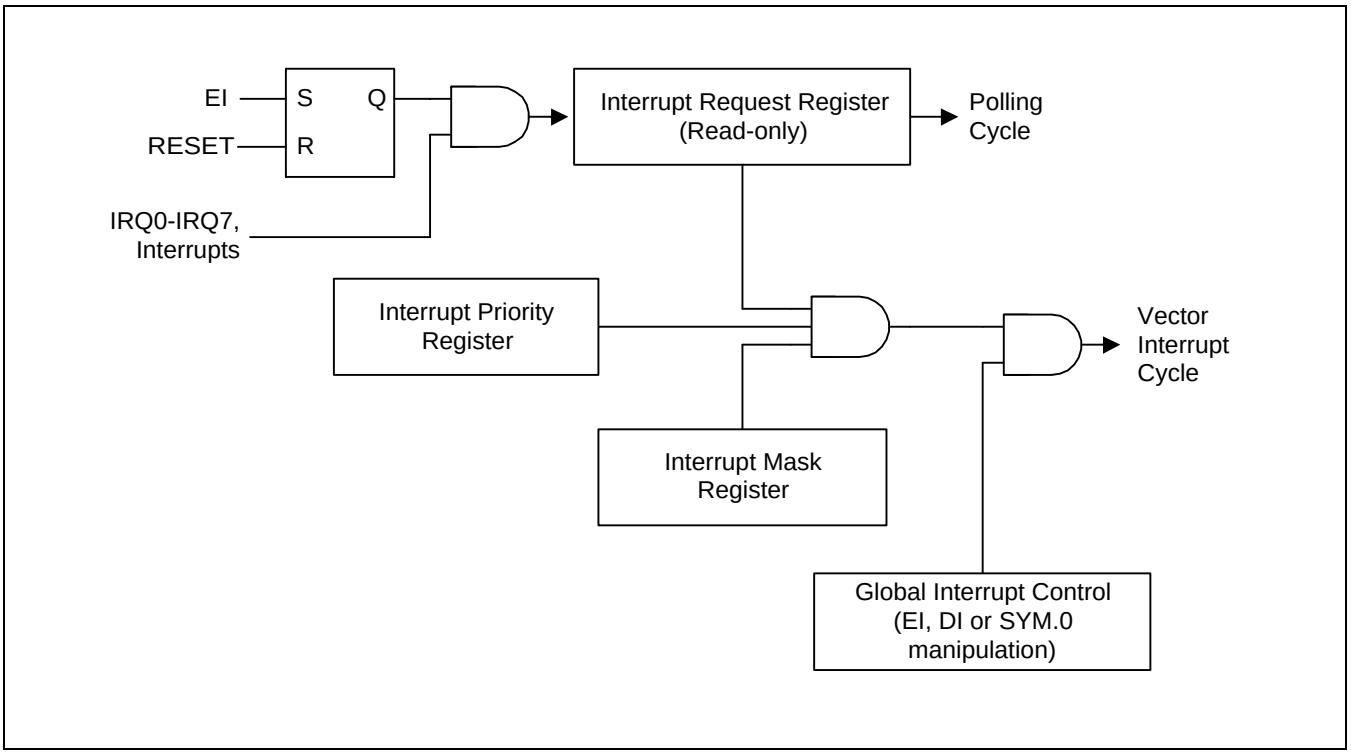


Figure 5-4. Interrupt Function Diagram

PERIPHERAL INTERRUPT CONTROL REGISTERS

For each interrupt source there is one or more corresponding peripheral control registers that let you control the interrupt generated by the related peripheral (see Table 5-3).

Table 5-3. Interrupt Source Control and Data Registers

Interrupt Source	Interrupt Level	Register(s)	Location(s) in Set 1
Timer B underflow	IRQ0	TBCON	D0H, bank 0
		TBDATAH, TBDATAL	D1H, D2H, bank 0
Timer A overflow	IRQ1	TINTPND	E7H, bank 0
Timer A match/capture		TACON	EAH, bank 0
		TADATA	EBH, bank 0
		TACNT	ECH, bank 0
Timer C(0) match/overflow	IRQ2	TCCON0	F2H, bank 1
Timer C(1) match/overflow		TCCON1	F3H, bank 1
		TCDATA0	F0H, bank 1
		TCDATA1	F1H, bank 1
Timer 1(0) match/capture	IRQ3	T1DATAH0,T1DATAL0	E6H, E7H, bank 1
Timer 1(0) overflow		T1DATAH1,T1DATAL1	E8H, E9H, bank 1
Timer 1(1) match/capture		T1CON0, T1CON1	EAH, EBH, bank1
Timer 1(1) overflow		T1CNTH0, T1CNTL0	ECH, EDH, bank1
		T1CNTH1, T1CNTL1	EEH, EFH, bank1
SIO receive/transmit	IRQ4	SIOCON, SIODATA	E1H, E0H, bank1
Watch timer		WTCON	F5H, bank1
P6.7 external interrupt	IRQ5	P6CONH	E8H, bank0
P6.6 external interrupt		P6CONL	E9H, bank0
P6.5 external interrupt		P6INT	EDH, bank0
P6.4 external interrupt		P6INTPND	EEH, bank0
P6.3 external interrupt			
P6.2 external interrupt			
P4.7 external interrupt	IRQ6	P4CONH	F6H, bank 0
P4.6 external interrupt		P4CONL	F7H, bank 0
P4.5 external interrupt		P4INT	FAH, bank 0
P4.4 external interrupt		P4INTPND	FBH, bank 0
P4.3 external interrupt			
P4.2 external interrupt			
P4.1 external interrupt			
P4.0 external interrupt			
UART0 receive/transmit	IRQ7	UARTCON0	E3H, bank 1
UART1 receive/transmit		UARTCON1	FBH, bank 1
		UDATA0, UDATA1	E2H, FAH, bank 1
		UARTPND	E5H, bank 1

SYSTEM MODE REGISTER (SYM)

The system mode register, SYM (set 1, DEH), is used to globally enable and disable interrupt processing (see Figure 5-5).

A reset clears SYM.0 to "0".

The instructions EI and DI enable and disable global interrupt processing, respectively, by modifying the bit 0 value of the SYM register. In order to enable interrupt processing an Enable Interrupt (EI) instruction must be included in the initialization routine, which follows a reset operation. Although you can manipulate SYM.0 directly to enable and disable interrupts during the normal operation, it is recommended to use the EI and DI instructions for this purpose.

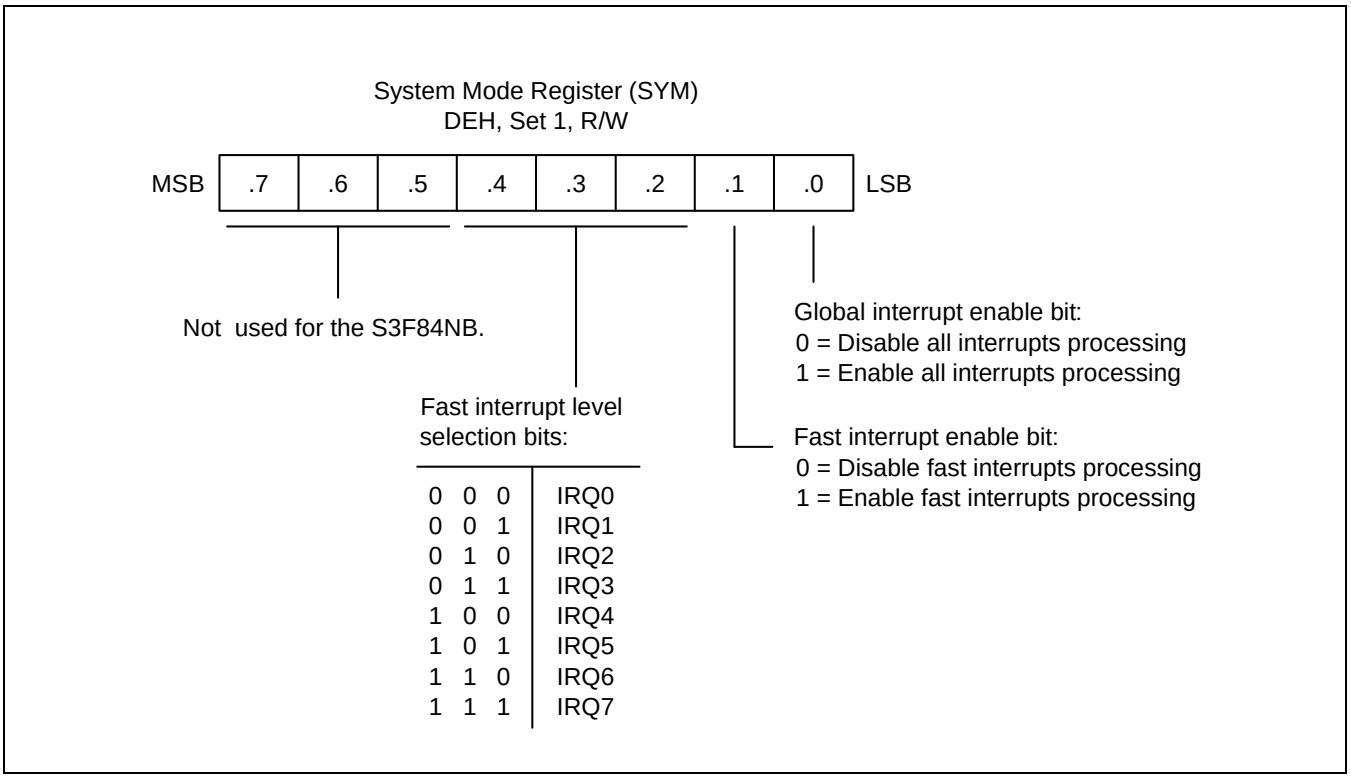


Figure 5-5. System Mode Register (SYM)

INTERRUPT MASK REGISTER (IMR)

The interrupt mask register, IMR (set 1, DDH) is used to enable or disable interrupt processing for individual interrupt levels. After a reset, all IMR bit values are undetermined and must therefore be written to their required settings by the initialization routine.

Each IMR bit corresponds to a specific interrupt level: bit 1 to IRQ1, bit 2 to IRQ2, and so on. When the IMR bit of an interrupt level is cleared to "0", interrupt processing for that level is disabled (masked). When you set a level's IMR bit to "1", interrupt processing for the level is enabled (not masked).

The IMR register is mapped to register location DDH in set 1. Bit values can be read and written by instructions using the Register addressing mode.

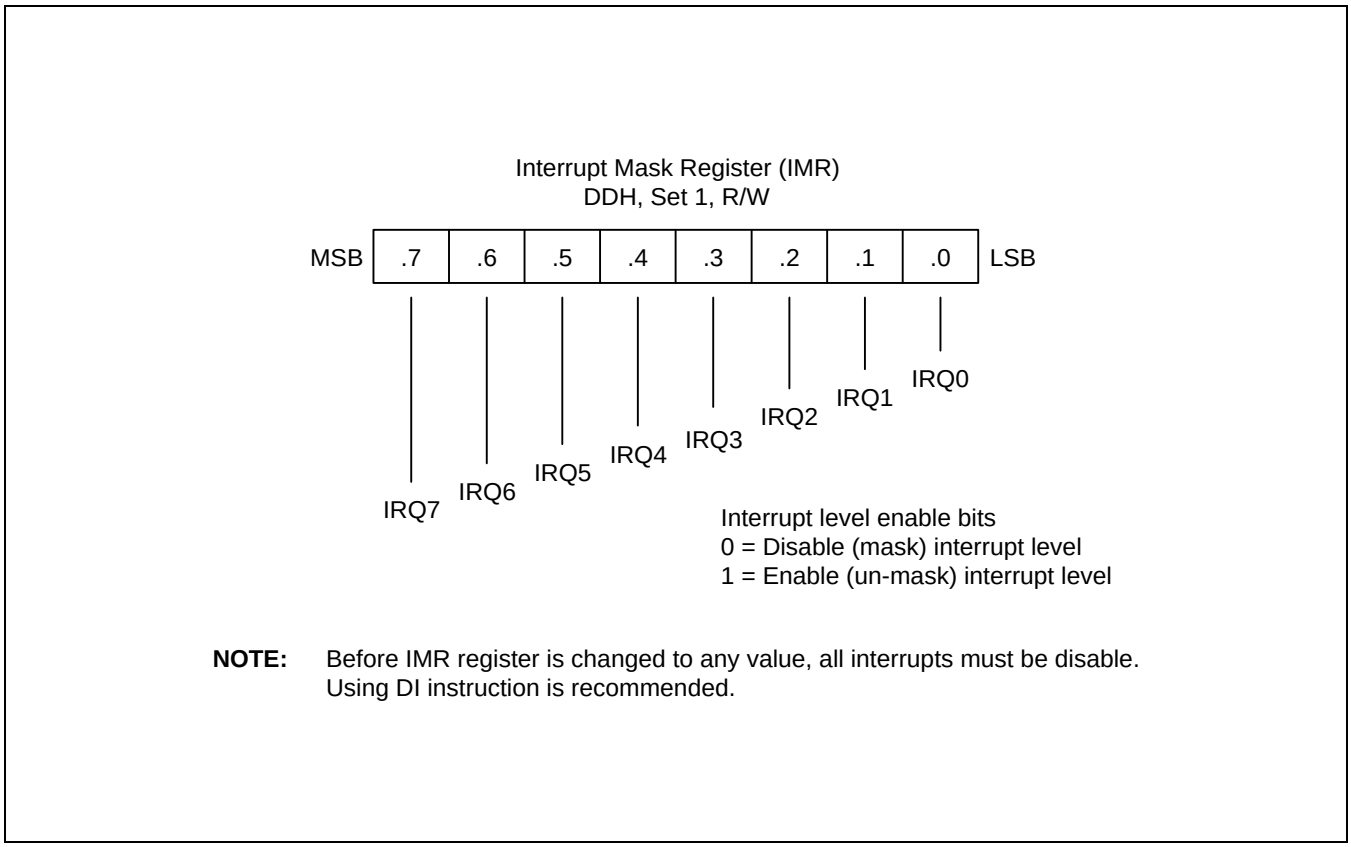


Figure 5-6. Interrupt Mask Register (IMR)

INTERRUPT PRIORITY REGISTER (IPR)

The interrupt priority register, IPR (set 1, bank 0, FFH), is used to set the relative priorities of the interrupt levels in the microcontroller's interrupt structure. After a reset, all IPR bit values are undetermined and must therefore be written to their required settings by the initialization routine.

When more than one interrupt sources are active, the source with the highest priority level is serviced first. If two sources belong to the same interrupt level, the source with the lower vector address usually has the priority (This priority is fixed in hardware).

To support programming of the relative interrupt level priorities, they are organized into groups and subgroups by the interrupt logic. Please note that these groups (and subgroups) are used only by IPR logic for the IPR register priority definitions (see Figure 5-7):

Group A IRQ0, IRQ1

Group B IRQ2, IRQ3, IRQ4

Group C IRQ5, IRQ6, IRQ7

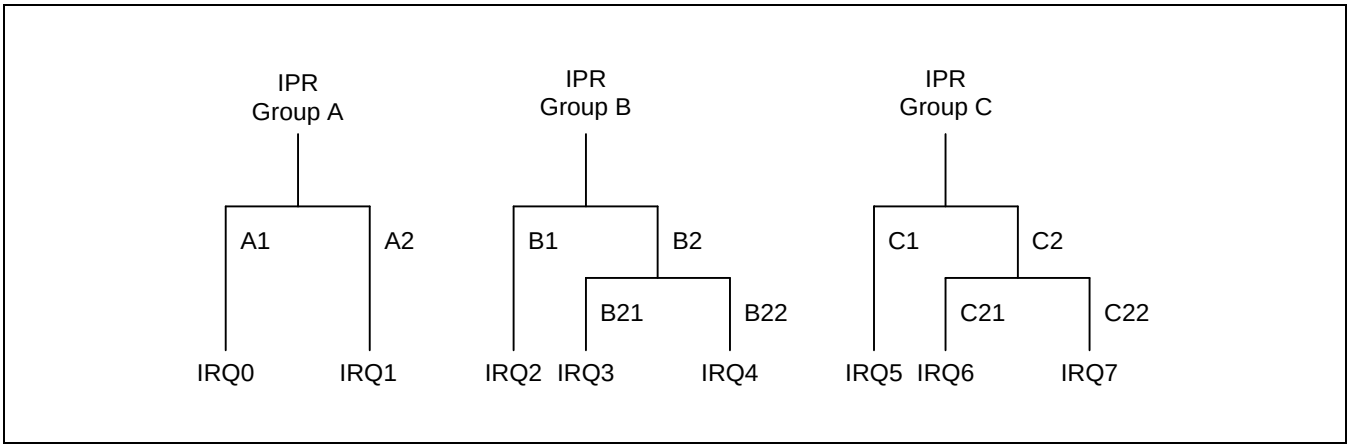


Figure 5-7. Interrupt Request Priority Groups

As you can see in Figure 5-8, IPR.7, IPR.4, and IPR.1 control the relative priority of interrupt groups A, B, and C. For example, the setting "001B" for these bits would select the group relationship B > C > A. The setting "101B" would select the relationship C > B > A.

The functions of the other IPR bit settings are as follows:

- IPR.5 controls the relative priorities of group C interrupts.
- Interrupt group C includes a subgroup that has an additional priority relationship among the interrupt levels 5, 6, and 7. IPR.6 defines the subgroup C relationship. IPR.5 controls the interrupt group C.
- IPR.0 controls the relative priority setting of IRQ0 and IRQ1 interrupts.

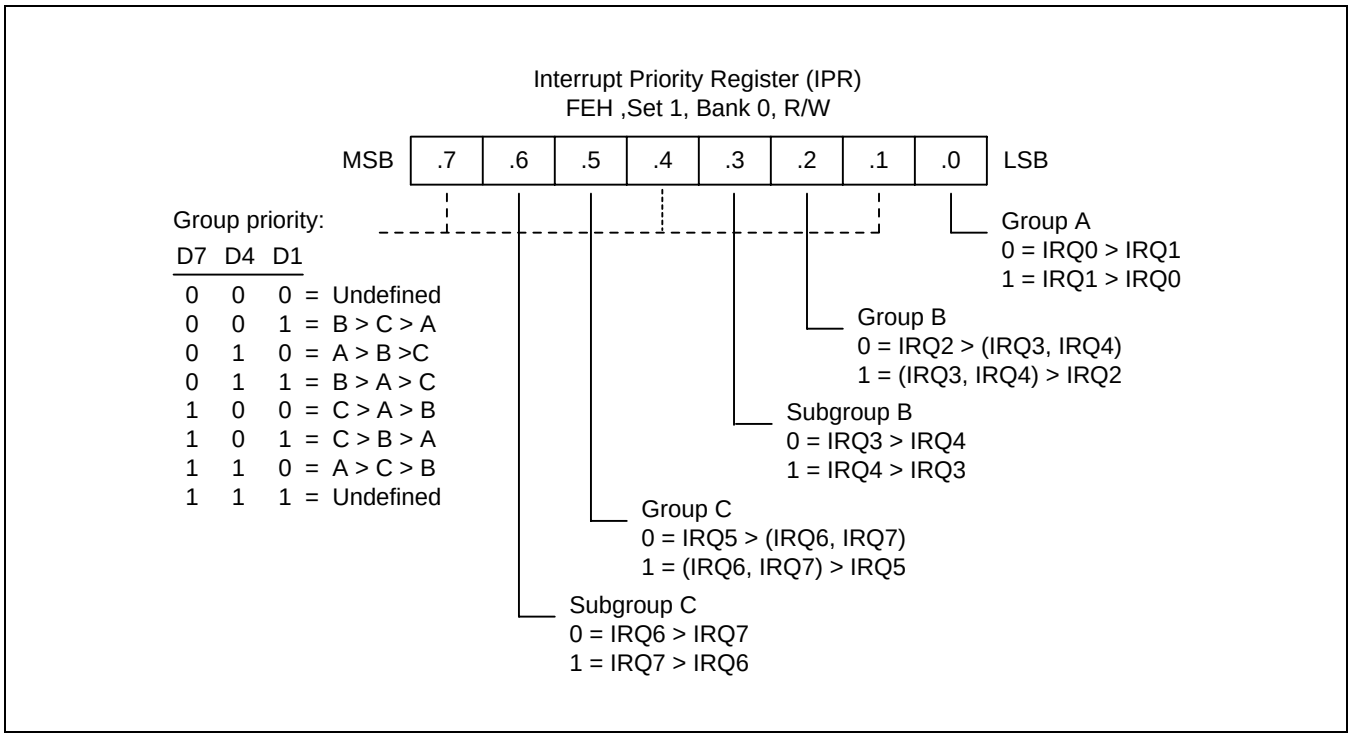


Figure 5-8. Interrupt Priority Register (IPR)

INTERRUPT REQUEST REGISTER (IRQ)

You can poll bit values in the interrupt request register, IRQ (set 1, DCH), to monitor interrupt request status for all levels in the microcontroller's interrupt structure. Each bit corresponds to the interrupt level of the same number: bit 0 to IRQ0, bit 1 to IRQ1, and so on. A "0" indicates that no interrupt request is currently being issued for that level. A "1" indicates that an interrupt request has been generated for that level.

IRQ bit values are read-only addressable using Register addressing mode. You can read (test) the contents of the IRQ register at any time using bit or byte addressing to determine the current interrupt request status of specific interrupt levels. After a reset, all IRQ status bits are cleared to "0".

You can poll IRQ register values even if a DI instruction has been executed (that is, if global interrupt processing is disabled). If an interrupt occurs while the interrupt structure is disabled, the CPU will not service it. You can, however, still detect the interrupt request by polling the IRQ register. In this way, you can determine which events occurred while the interrupt structure was globally disabled.

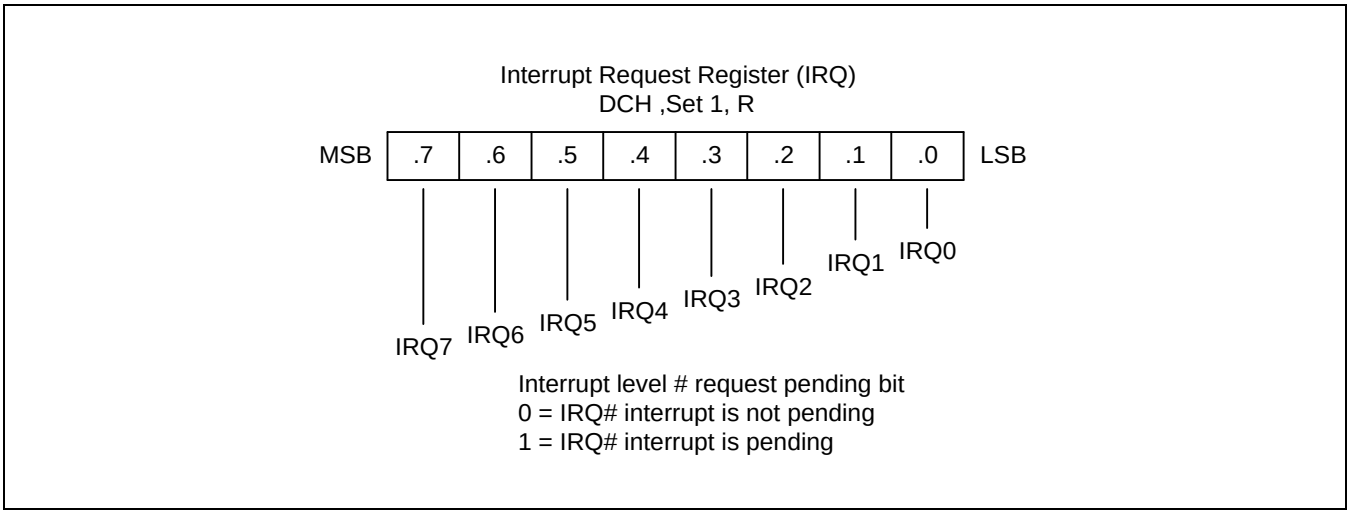


Figure 5-9. Interrupt Request Register (IRQ)

INTERRUPT PENDING FUNCTION TYPES

Overview

There are two types of interrupt pending bits: one type that is automatically cleared by hardware after the interrupt service routine is acknowledged and executed; the other that must be cleared in the interrupt service routine.

Pending Bits Cleared Automatically by Hardware

For interrupt pending bits that are cleared automatically by hardware, interrupt logic sets the corresponding pending bit to "1" when a request occurs. It then issues an IRQ pulse to inform the CPU that an interrupt is waiting to be serviced. The CPU acknowledges the interrupt source by sending an IACK, executes the service routine, and clears the pending bit to "0". This type of pending bit is not mapped and cannot, therefore, be read or written by application software.

In the S3F84NB interrupt structure, the timer B underflow interrupt (IRQ1) belongs to this category of interrupts in which pending condition is cleared automatically by hardware.

Pending Bits Cleared by the Service Routine

The second type of pending bit is the one that should be cleared by program software. The service routine must clear the appropriate pending bit before a return-from-interrupt subroutine (IRET) occurs. To do this, a "0" must be written to the corresponding pending bit location in the source's mode or control register.

In the S3F84NB interrupt structure, pending conditions for IRQ4, IRQ5, IRQ6, and IRQ7 must be cleared in the interrupt service routine.

INTERRUPT SOURCE POLLING SEQUENCE

The interrupt request polling and servicing sequence is as follows:

1. A source generates an interrupt request by setting the interrupt request bit to "1".
2. The CPU polling procedure identifies a pending condition for that source.
3. The CPU checks the source's interrupt level.
4. The CPU generates an interrupt acknowledge signal.
5. Interrupt logic determines the interrupt's vector address.
6. The service routine starts and the source's pending bit is cleared to "0" (by hardware or by software).
7. The CPU continues polling for interrupt requests.

INTERRUPT SERVICE ROUTINES

Before an interrupt request is serviced, the following conditions must be met:

- Interrupt processing must be globally enabled (EI, SYM.0 = "1")
- The interrupt level must be enabled (IMR register)
- The interrupt level must have the highest priority if more than one level is currently requesting service
- The interrupt must be enabled at the interrupt's source (peripheral control register)

When all the above conditions are met, the interrupt request is acknowledged at the end of the instruction cycle. The CPU then initiates an interrupt machine cycle that completes the following processing sequence:

1. Reset (clear to "0") the interrupt enable bit in the SYM register (SYM.0) to disable all subsequent interrupts.
2. Save the program counter (PC) and status flags to the system stack.
3. Branch to the interrupt vector to fetch the address of the service routine.
4. Pass control to the interrupt service routine.

When the interrupt service routine is completed, the CPU issues an Interrupt Return (IRET). The IRET restores the PC and status flags, setting SYM.0 to "1". It allows the CPU to process the next interrupt request.

GENERATING INTERRUPT VECTOR ADDRESSES

The interrupt vector area in the ROM (00H–FFH) contains the addresses of interrupt service routines that correspond to each level in the interrupt structure. Vectored interrupt processing follows this sequence:

1. Push the program counter's low-byte value to the stack.
2. Push the program counter's high-byte value to the stack.
3. Push the FLAG register values to the stack.
4. Fetch the service routine's high-byte address from the vector location.
5. Fetch the service routine's low-byte address from the vector location.
6. Branch to the service routine specified by the concatenated 16-bit vector address.

NOTE

A 16-bit vector address always begins at an even-numbered ROM address within the range of 00H–FFH.

NESTING OF VECTORED INTERRUPTS

It is possible to nest a higher-priority interrupt request while a lower-priority request is being serviced. To do this, you must follow these steps:

1. Push the current 8-bit interrupt mask register (IMR) value to the stack (PUSH IMR).
2. Load the IMR register with a new mask value that enables only the higher priority interrupt.
3. Execute an EI instruction to enable interrupt processing (a higher priority interrupt will be processed if it occurs).
4. When the lower-priority interrupt service routine ends, restore the IMR to its original value by returning the previous mask value from the stack (POP IMR).
5. Execute an IRET.

Depending on the application, you may be able to simplify the procedure above to some extent.

6 INSTRUCTION SET

OVERVIEW

The SAM8 instruction set is specifically designed to support the large register files that are typical of most SAM8 microcontrollers. There are 78 instructions. The powerful data manipulation capabilities and features of the instruction set include:

- A full complement of 8-bit arithmetic and logic operations, including multiply and divide
- No special I/O instructions (I/O control/data registers are mapped directly into the register file)
- Decimal adjustment included in binary-coded decimal (BCD) operations
- 16-bit (word) data can be incremented and decremented
- Flexible instructions for bit addressing, rotate, and shift operations

Data Types

The SAM8 CPU performs operations on bits, bytes, BCD digits, and two-byte words. Bits in the register file can be set, cleared, complemented, and tested. Bits within a byte are numbered from 7 to 0, where bit 0 is the least significant (right-most) bit.

Register Addressing

To access an individual register, an 8-bit address in the range 0-255 or the 4-bit address of a working register is specified. Paired registers can be used to construct 16-bit data or 16-bit program memory or data memory addresses. For detailed information about register addressing, please refer to Section 2, "Address Spaces."

Addressing Modes

There are seven explicit addressing modes: Register (R), Indirect Register (IR), Indexed (X), Direct (DA), Relative (RA), Immediate (IM), and Indirect (IA). For detailed descriptions of these addressing modes, please refer to Section 3, "Addressing Modes."

Table 6-1. Instruction Group Summary

Mnemonic	Operands	Instruction
Load Instructions		
CLR	dst	Clear
LD	dst,src	Load
LDB	dst,src	Load bit
LDE	dst,src	Load external data memory
LDC	dst,src	Load program memory
LDED	dst,src	Load external data memory and decrement
LDCD	dst,src	Load program memory and decrement
LDEI	dst,src	Load external data memory and increment
LDCI	dst,src	Load program memory and increment
LDEPD	dst,src	Load external data memory with pre-decrement
LDCPD	dst,src	Load program memory with pre-decrement
LDEPI	dst,src	Load external data memory with pre-increment
LDCPI	dst,src	Load program memory with pre-increment
LDW	dst,src	Load word
POP	dst	Pop from stack
POPUD	dst,src	Pop user stack (decrementing)
POPUI	dst,src	Pop user stack (incrementing)
PUSH	src	Push to stack
PUSHUD	dst,src	Push user stack (decrementing)
PUSHUI	dst,src	Push user stack (incrementing)

Table 6-1. Instruction Group Summary (Continued)

Mnemonic	Operands	Instruction
Arithmetic Instructions		
ADC	dst,src	Add with carry
ADD	dst,src	Add
CP	dst,src	Compare
DA	dst	Decimal adjust
DEC	dst	Decrement
DECW	dst	Decrement word
DIV	dst,src	Divide
INC	dst	Increment
INCW	dst	Increment word
MULT	dst,src	Multiply
SBC	dst,src	Subtract with carry
SUB	dst,src	Subtract
Logic Instructions		
AND	dst,src	Logical AND
COM	dst	Complement
OR	dst,src	Logical OR
XOR	dst,src	Logical exclusive OR

Table 6-1. Instruction Group Summary (Continued)

Mnemonic	Operands	Instruction
Program Control Instructions		
BTJRF	dst,src	Bit test and jump relative on false
BTJRT	dst,src	Bit test and jump relative on true
CALL	dst	Call procedure
CPIJE	dst,src	Compare, increment and jump on equal
CPIJNE	dst,src	Compare, increment and jump on non-equal
DJNZ	r,dst	Decrement register and jump on non-zero
ENTER		Enter
EXIT		Exit
IRET		Interrupt return
JP	cc,dst	Jump on condition code
JP	dst	Jump unconditional
JR	cc,dst	Jump relative on condition code
NEXT		Next
RET		Return
WFI		Wait for interrupt
Bit Manipulation Instructions		
BAND	dst,src	Bit AND
BCP	dst,src	Bit compare
BITC	dst	Bit complement
BITR	dst	Bit reset
BITS	dst	Bit set
BOR	dst,src	Bit OR
BXOR	dst,src	Bit XOR
TCM	dst,src	Test complement under mask
TM	dst,src	Test under mask

Table 6-1. Instruction Group Summary (Concluded)

Mnemonic	Operands	Instruction
Rotate and Shift Instructions		
RL	dst	Rotate left
RLC	dst	Rotate left through carry
RR	dst	Rotate right
RRC	dst	Rotate right through carry
SRA	dst	Shift right arithmetic
SWAP	dst	Swap nibbles
CPU Control Instructions		
CCF		Complement carry flag
DI		Disable interrupts
EI		Enable interrupts
IDLE		Enter Idle mode
NOP		No operation
RCF		Reset carry flag
SB0		Set bank 0
SB1		Set bank 1
SCF		Set carry flag
SRP	src	Set register pointers
SRP0	src	Set register pointer 0
SRP1	src	Set register pointer 1
STOP		Enter Stop mode

FLAGS REGISTER (FLAGS)

The flags register FLAGS contains eight bits that describe the current status of CPU operations. Four of these bits, FLAGS.7–FLAGS.4, can be tested and used with conditional jump instructions; two others FLAGS.3 and FLAGS.2 are used for BCD arithmetic.

The FLAGS register also contains a bit to indicate the status of fast interrupt processing (FLAGS.1) and a bank address status bit (FLAGS.0) to indicate whether bank 0 or bank 1 is currently being addressed. FLAGS register can be set or reset by instructions as long as its outcome does not affect the flags, such as, Load instruction.

Logical and Arithmetic instructions such as, AND, OR, XOR, ADD, and SUB can affect the Flags register. For example, the AND instruction updates the Zero, Sign and Overflow flags based on the outcome of the AND instruction. If the AND instruction uses the Flags register as the destination, then simultaneously, two write will occur to the Flags register producing an unpredictable result.

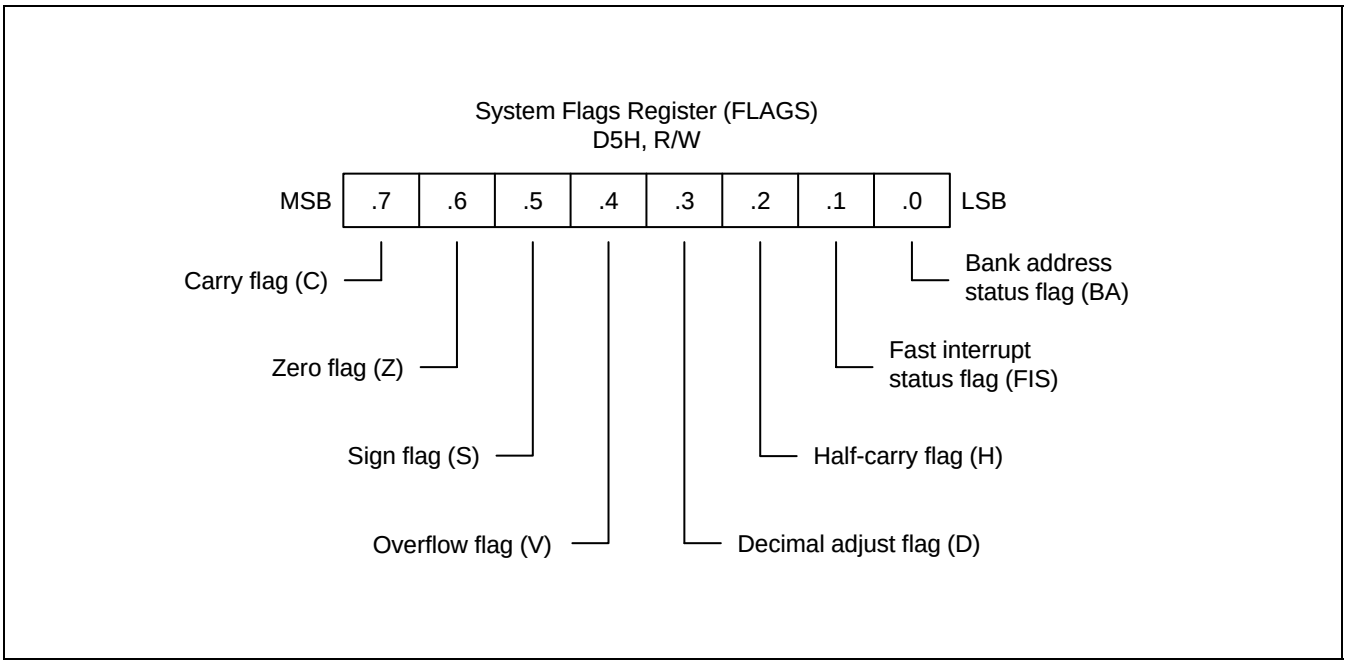


Figure 6-1. System Flags Register (FLAGS)

FLAG DESCRIPTIONS

C Carry Flag (FLAGS.7)

The C flag is set to "1" if the result from an arithmetic operation generates a carry-out from or a borrow to the bit 7 position (MSB). After rotate and shift operations, it contains the last value shifted out of the specified register. Program instructions can set, clear, or complement the carry flag.

Z Zero Flag (FLAGS.6)

For arithmetic and logic operations, the Z flag is set to "1" if the result of the operation is zero. For operations that test register bits, and for shift and rotate operations, the Z flag is set to "1" if the result is logic zero.

S Sign Flag (FLAGS.5)

Following arithmetic, logic, rotate, or shift operations, the sign bit identifies the state of the MSB of the result. A logic zero indicates a positive number and a logic one indicates a negative number.

V Overflow Flag (FLAGS.4)

The V flag is set to "1" when the result of a two's-complement operation is greater than + 127 or less than – 128. It is also cleared to "0" following logic operations.

D Decimal Adjust Flag (FLAGS.3)

The DA bit is used to specify what type of instruction was executed last during BCD operations, so that a subsequent decimal adjust operation can execute correctly. The DA bit is not usually accessed by programmers, and cannot be used as a test condition.

H Half-Carry Flag (FLAGS.2)

The H bit is set to "1" whenever an addition generates a carry-out of bit 3, or when a subtraction borrows out of bit 4. It is used by the Decimal Adjust (DA) instruction to convert the binary result of a previous addition or subtraction into the correct decimal (BCD) result. The H flag is seldom accessed directly by a program.

FIS Fast Interrupt Status Flag (FLAGS.1)

The FIS bit is set during a fast interrupt cycle and reset during the IRET following interrupt servicing. When set, it inhibits all interrupts and causes the fast interrupt return to be executed when the IRET instruction is executed.

BA Bank Address Flag (FLAGS.0)

The BA flag indicates which register bank in the set 1 area of the internal register file is currently selected, bank 0 or bank 1. The BA flag is cleared to "0" (select bank 0) when you execute the SB0 instruction and is set to "1" (select bank 1) when you execute the SB1 instruction.

INSTRUCTION SET NOTATION

Table 6-2. Flag Notation Conventions

Flag	Description
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag
0	Cleared to logic zero
1	Set to logic one
*	Set or cleared according to operation
–	Value is unaffected
x	Value is undefined

Table 6-3. Instruction Set Symbols

Symbol	Description
dst	Destination operand
src	Source operand
@	Indirect register address prefix
PC	Program counter
IP	Instruction pointer
FLAGS	Flags register (D5H)
RP	Register pointer
#	Immediate operand or register address prefix
H	Hexadecimal number suffix
D	Decimal number suffix
B	Binary number suffix
opc	Opcode

Table 6-4. Instruction Notation Conventions

Notation	Description	Actual Operand Range
cc	Condition code	See list of condition codes in Table 6-6.
r	Working register only	Rn (n = 0–15)
rb	Bit (b) of working register	Rn.b (n = 0–15, b = 0–7)
r0	Bit 0 (LSB) of working register	Rn (n = 0–15)
rr	Working register pair	RRp (p = 0, 2, 4, ..., 14)
R	Register or working register	reg or Rn (reg = 0–255, n = 0–15)
Rb	Bit 'b' of register or working register	reg.b (reg = 0–255, b = 0–7)
RR	Register pair or working register pair	reg or RRp (reg = 0–254, even number only, where p = 0, 2, ..., 14)
IA	Indirect addressing mode	addr (addr = 0–254, even number only)
Ir	Indirect working register only	@Rn (n = 0–15)
IR	Indirect register or indirect working register	@Rn or @reg (reg = 0–255, n = 0–15)
Irr	Indirect working register pair only	@RRp (p = 0, 2, ..., 14)
IRR	Indirect register pair or indirect working register pair	@RRp or @reg (reg = 0–254, even only, where p = 0, 2, ..., 14)
X	Indexed addressing mode	#reg [Rn] (reg = 0–255, n = 0–15)
XS	Indexed (short offset) addressing mode	#addr [RRp] (addr = range –128 to +127, where p = 0, 2, ..., 14)
XL	Indexed (long offset) addressing mode	#addr [RRp] (addr = range 0–65535, where p = 0, 2, ..., 14)
DA	Direct addressing mode	addr (addr = range 0–65535)
RA	Relative addressing mode	addr (addr = number in the range +127 to –128 that is an offset relative to the address of the next instruction)
IM	Immediate addressing mode	#data (data = 0–255)
IML	Immediate (long) addressing mode	#data (data = range 0–65535)

Table 6-5. Opcode Quick Reference

OPCODE MAP									
		LOWER NIBBLE (HEX)							
	–	0	1	2	3	4	5	6	7
U	0	DEC R1	DEC IR1	ADD r1,r2	ADD r1,Ir2	ADD R2,R1	ADD IR2,R1	ADD R1,IM	BOR r0–Rb
P	1	RLC R1	RLC IR1	ADC r1,r2	ADC r1,Ir2	ADC R2,R1	ADC IR2,R1	ADC R1,IM	BCP r1.b, R2
P	2	INC R1	INC IR1	SUB r1,r2	SUB r1,Ir2	SUB R2,R1	SUB IR2,R1	SUB R1,IM	BXOR r0–Rb
E	3	JP IRR1	SRP/0/1 IM	SBC r1,r2	SBC r1,Ir2	SBC R2,R1	SBC IR2,R1	SBC R1,IM	BTJR r2.b, RA
R	4	DA R1	DA IR1	OR r1,r2	OR r1,Ir2	OR R2,R1	OR IR2,R1	OR R1,IM	LDB r0–Rb
	5	POP R1	POP IR1	AND r1,r2	AND r1,Ir2	AND R2,R1	AND IR2,R1	AND R1,IM	BITC r1.b
N	6	COM R1	COM IR1	TCM r1,r2	TCM r1,Ir2	TCM R2,R1	TCM IR2,R1	TCM R1,IM	BAND r0–Rb
I	7	PUSH R2	PUSH IR2	TM r1,r2	TM r1,Ir2	TM R2,R1	TM IR2,R1	TM R1,IM	BIT r1.b
B	8	DECW RR1	DECW IR1	PUSHUD IR1,R2	PUSHUI IR1,R2	MULT R2,RR1	MULT IR2,RR1	MULT IM,RR1	LD r1, x, r2
B	9	RL R1	RL IR1	POPUD IR2,R1	POPUI IR2,R1	DIV R2,RR1	DIV IR2,RR1	DIV IM,RR1	LD r2, x, r1
L	A	INCW RR1	INCW IR1	CP r1,r2	CP r1,Ir2	CP R2,R1	CP IR2,R1	CP R1,IM	LDC r1, Irr2, xL
E	B	CLR R1	CLR IR1	XOR r1,r2	XOR r1,Ir2	XOR R2,R1	XOR IR2,R1	XOR R1,IM	LDC r2, Irr2, xL
	C	RRC R1	RRC IR1	CPIJE Ir,r2,RA	LDC r1,Irr2	LDW RR2,RR1	LDW IR2,RR1	LDW RR1,IML	LD r1, Ir2
H	D	SRA R1	SRA IR1	CPIJNE Irr,r2,RA	LDC r2,Irr1	CALL IA1		LD IR1,IM	LD Ir1, r2
E	E	RR R1	RR IR1	LDCD r1,Irr2	LDCI r1,Irr2	LD R2,R1	LD R2,IR1	LD R1,IM	LDC r1, Irr2, xs
X	F	SWAP R1	SWAP IR1	LDCPD r2,Irr1	LDCPI r2,Irr1	CALL IRR1	LD IR2,R1	CALL DA1	LDC r2, Irr1, xs

Table 6-5. Opcode Quick Reference (Continued)

OPCODE MAP									
LOWER NIBBLE (HEX)									
	–	8	9	A	B	C	D	E	F
U	0	LD r1,R2	LD r2,R1	DJNZ r1,RA	JR cc,RA	LD r1,IM	JP cc,DA	INC r1	NEXT
P	1	↓	↓	↓	↓	↓	↓	↓	ENTER
P	2								EXIT
E	3								WFI
R	4								SB0
	5								SB1
N	6								IDLE
I	7	↓	↓	↓	↓	↓	↓	↓	STOP
B	8								DI
B	9								EI
L	A								RET
E	B								IRET
	C								RCF
H	D	↓	↓	↓	↓	↓	↓	↓	SCF
E	E								CCF
X	F	LD r1,R2	LD r2,R1	DJNZ r1,RA	JR cc,RA	LD r1,IM	JP cc,DA	INC r1	NOP

CONDITION CODES

The opcode of a conditional jump always contains a 4-bit field called the condition code (cc). This specifies under which conditions it is to execute the jump. For example, a conditional jump with the condition code for "equal" after a compare operation only jumps if the two operands are equal. Condition codes are listed in Table 6-6.

The carry (C), zero (Z), sign (S), and overflow (V) flags are used to control the operation of conditional jump instructions.

Table 6-6. Condition Codes

Binary	Mnemonic	Description	Flags Set
0000	F	Always false	–
1000	T	Always true	–
0111 (note)	C	Carry	C = 1
1111 (note)	NC	No carry	C = 0
0110 (note)	Z	Zero	Z = 1
1110 (note)	NZ	Not zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No overflow	V = 0
0110 (note)	EQ	Equal	Z = 1
1110 (note)	NE	Not equal	Z = 0
1001	GE	Greater than or equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater than	(Z OR (S XOR V)) = 0
0010	LE	Less than or equal	(Z OR (S XOR V)) = 1
1111 (note)	UGE	Unsigned greater than or equal	C = 0
0111 (note)	ULT	Unsigned less than	C = 1
1011	UGT	Unsigned greater than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned less than or equal	(C OR Z) = 1

NOTES:

1. It indicates condition codes that are related to two different mnemonics but which test the same flag. For example, Z and EQ are both true if the zero flag (Z) is set, but after an ADD instruction, Z would probably be used; after a CP instruction, however, EQ would probably be used.
2. For operations involving unsigned numbers, the special condition codes UGE, ULT, UGT, and ULE must be used.

INSTRUCTION DESCRIPTIONS

This section contains detailed information and programming examples for each instruction in the SAM8 instruction set. Information is arranged in a consistent format for improved readability and for fast referencing. The following information is included in each instruction description:

- Instruction name (mnemonic)
- Full instruction name
- Source/destination format of the instruction operand
- Shorthand notation of the instruction's operation
- Textual description of the instruction's effect
- Specific flag settings affected by the instruction
- Detailed description of the instruction's format, execution time, and addressing mode(s)
- Programming example(s) explaining how to use the instruction

ADC – Add with carry

ADC dst,src

Operation: dst ← dst + src + c

The source operand, along with the setting of the carry flag, is added to the destination operand and the sum is stored in the destination. The contents of the source are unaffected. Two's-complement addition is performed. In multiple precision arithmetic, this instruction permits the carry from the addition of low-order operands to be carried into the addition of high-order operands.

Flags:

C: Set if there is a carry from the most significant bit of the result; cleared otherwise.

Z: Set if the result is "0"; cleared otherwise.

S: Set if the result is negative; cleared otherwise.

V: Set if arithmetic overflow occurs, that is, if both operands are of the same sign and the result is of the opposite sign; cleared otherwise.

D: Always cleared to "0".

H: Set if there is a carry from the most significant bit of the low-order four bits of the result; cleared otherwise.

Format:

			Bytes	Cycles	Opcode (Hex)	Addr Mode dst	Addr Mode src
opc	dst | src		2	4	12	r	r
				6	13	r	lr
opc	src	dst	3	6	14	R	R
				6	15	R	IR
opc	dst	src	3	6	16	R	IM

Examples: Given: R1 = 10H, R2 = 03H, C flag = "1", register 01H = 20H, register 02H = 03H, and register 03H = 0AH:

ADC	R1,R2	→	R1 = 14H, R2 = 03H
ADC	R1,@R2	→	R1 = 1BH, R2 = 03H
ADC	01H,02H	→	Register 01H = 24H, register 02H = 03H
ADC	01H,@02H	→	Register 01H = 2BH, register 02H = 03H
ADC	01H,#11H	→	Register 01H = 32H

In the first example, destination register R1 contains the value 10H, the carry flag is set to "1", and the source working register R2 contains the value 03H. The statement "ADC R1,R2" adds 03H and the carry flag value ("1") to the destination value 10H, leaving 14H in register R1.

ADD – Add

ADD dst,src

Operation: dst ← dst + src

The source operand is added to the destination operand and the sum is stored in the destination. The contents of the source are unaffected. Two's-complement addition is performed.

Flags:
C: Set if there is a carry from the most significant bit of the result; cleared otherwise.
Z: Set if the result is "0"; cleared otherwise.
S: Set if the result is negative; cleared otherwise.
V: Set if arithmetic overflow occurred, that is, if both operands are of the same sign and the result is of the opposite sign; cleared otherwise.
D: Always cleared to "0".
H: Set if a carry from the low-order nibble occurred.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst	src
opc | dst | src	2	4	02	r	r
		6	03	r	lr
opc | src | dst	3	6	04	R	R
		6	05	R	IR
opc | dst | src	3	6	06	R	IM

Examples: Given: R1 = 12H, R2 = 03H, register 01H = 21H, register 02H = 03H, register 03H = 0AH:

ADD R1,R2 → R1 = 15H, R2 = 03H
ADD R1,@R2 → R1 = 1CH, R2 = 03H
ADD 01H,02H → Register 01H = 24H, register 02H = 03H
ADD 01H,@02H → Register 01H = 2BH, register 02H = 03H
ADD 01H,#25H → Register 01H = 46H

In the first example, destination working register R1 contains 12H and the source working register R2 contains 03H. The statement "ADD R1,R2" adds 03H to 12H, leaving the value 15H in register R1.

AND – Logical AND

AND dst, src

Operation: dst ← dst AND src

The source operand is logically ANDed with the destination operand. The result is stored in the destination. The AND operation results in a "1" bit being stored whenever the corresponding bits in the two operands are both logic ones; otherwise a "0" bit value is stored. The contents of the source are unaffected.

Flags:
C: Unaffected.
Z: Set if the result is "0"; cleared otherwise.
S: Set if the result bit 7 is set; cleared otherwise.
V: Always cleared to "0".
D: Unaffected.
H: Unaffected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst	Addr Mode src
opc | dst | src	2	4	52	r	r
		6	53	r	lr
opc | src | dst	3	6	54	R	R
		6	55	R	IR
opc | dst | src	3	6	56	R	IM

Examples: Given: R1 = 12H, R2 = 03H, register 01H = 21H, register 02H = 03H, register 03H = 0AH:

AND R1,R2 → R1 = 02H, R2 = 03H
AND R1,@R2 → R1 = 02H, R2 = 03H
AND 01H,02H → Register 01H = 01H, register 02H = 03H
AND 01H,@02H → Register 01H = 00H, register 02H = 03H
AND 01H,#25H → Register 01H = 21H

In the first example, destination working register R1 contains the value 12H and the source working register R2 contains 03H. The statement "AND R1,R2" logically ANDs the source operand 03H with the destination operand value 12H, leaving the value 02H in register R1.

BAND – Bit AND

BAND dst,src.b

BAND dst.b,src

Operation: dst(0) ← dst(0) AND src(b)

or

dst(b) ← dst(b) AND src(0)

The specified bit of the source (or the destination) is logically ANDed with the zero bit (LSB) of the destination (or source). The resultant bit is stored in the specified bit of the destination. No other bits of the destination are affected. The source is unaffected.

Flags:
C: Unaffected.
Z: Set if the result is "0"; cleared otherwise.
S: Cleared to "0".
V: Undefined.
D: Unaffected.
H: Unaffected.

Format:

			Bytes	Cycles	Opcode (Hex)	Addr Mode dst	src
opc	dst | b | 0	src	3	6	67	r0	Rb
opc	src | b | 1	dst	3	6	67	Rb	r0

NOTE: In the second byte of the 3-byte instruction formats, the destination (or source) address is four bits, the bit address 'b' is three bits, and the LSB address value is one bit in length.

Examples: Given: R1 = 07H and register 01H = 05H:

BAND R1,01H.1 → R1 = 06H, register 01H = 05H

BAND 01H.1,R1 → Register 01H = 05H, R1 = 07H

In the first example, source register 01H contains the value 05H (00000101B) and destination working register R1 contains 07H (00000111B). The statement "BAND R1,01H.1" ANDs the bit 1 value of the source register ("0") with the bit 0 value of register R1 (destination), leaving the value 06H (00000110B) in register R1.

BCP – Bit Compare

BCP dst,src.b

Operation: dst(0) – src(b)

The specified bit of the source is compared to (subtracted from) bit zero (LSB) of the destination. The zero flag is set if the bits are the same; otherwise it is cleared. The contents of both operands are unaffected by the comparison.

Flags:
C: Unaffected.
Z: Set if the two bits are the same; cleared otherwise.
S: Cleared to "0".
V: Undefined.
D: Unaffected.
H: Unaffected.

Format:

			Bytes	Cycles	Opcode (Hex)	Addr Mode dst	src
opc	dst | b | 0	src	3	6	17	r0	Rb

NOTE: In the second byte of the instruction format, the destination address is four bits, the bit address 'b' is three bits, and the LSB address value is one bit in length.

Example: Given: R1 = 07H and register 01H = 01H:

BCP R1,01H.1 → R1 = 07H, register 01H = 01H

If destination working register R1 contains the value 07H (00000111B) and the source register 01H contains the value 01H (00000001B), the statement "BCP R1,01H.1" compares bit one of the source register (01H) and bit zero of the destination register (R1). Because the bit values are not identical, the zero flag bit (Z) is cleared in the FLAGS register (0D5H).

BITC – Bit Complement

BITC dst.b

Operation: dst(b) ← NOT dst(b)

This instruction complements the specified bit within the destination without affecting any other bits in the destination.

Flags:
C: Unaffected.
Z: Set if the result is "0"; cleared otherwise.
S: Cleared to "0".
V: Undefined.
D: Unaffected.
H: Unaffected.

Format:

		Bytes	Cycles	Opcode (Hex)	Addr Mode dst
opc	dst | b | 0	2	4	57	rb

NOTE: In the second byte of the instruction format, the destination address is four bits, the bit address 'b' is three bits, and the LSB address value is one bit in length.

Example: Given: R1 = 07H

BITC R1.1 → R1 = 05H

If working register R1 contains the value 07H (00000111B), the statement "BITC R1.1" complements bit one of the destination and leaves the value 05H (00000101B) in register R1. Because the result of the complement is not "0", the zero flag (Z) in the FLAGS register (0D5H) is cleared.

BITR – Bit Reset

BITR dst.b

Operation: dst(b) ← 0

The BITR instruction clears the specified bit within the destination without affecting any other bits in the destination.

Flags: No flags are affected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst
opc | dst | b | 0	2	4	77	rb

NOTE: In the second byte of the instruction format, the destination address is four bits, the bit address 'b' is three bits, and the LSB address value is one bit in length.

Example: Given: R1 = 07H:

BITR R1.1 → R1 = 05H

If the value of working register R1 is 07H (00000111B), the statement "BITR R1.1" clears bit one of the destination register R1, leaving the value 05H (00000101B).

BITS – Bit Set

BITS dst.b

Operation: dst(b) ← 1

The BITS instruction sets the specified bit within the destination without affecting any other bits in the destination.

Flags: No flags are affected.

Format:

		Bytes	Cycles	Opcode (Hex)	Addr Mode dst
opc	dst | b | 1	2	4	77	rb

NOTE: In the second byte of the instruction format, the destination address is four bits, the bit address 'b' is three bits, and the LSB address value is one bit in length.

Example: Given: R1 = 07H:

BITS R1.3 → R1 = 0FH

If working register R1 contains the value 07H (00000111B), the statement "BITS R1.3" sets bit three of the destination register R1 to "1", leaving the value 0FH (00001111B).

BOR – Bit OR

BOR dst,src.b

BOR dst.b,src

Operation: dst(0) ← dst(0) OR src(b)

or

dst(b) ← dst(b) OR src(0)

The specified bit of the source (or the destination) is logically ORed with bit zero (LSB) of the destination (or the source). The resulting bit value is stored in the specified bit of the destination. No other bits of the destination are affected. The source is unaffected.

Flags:
C: Unaffected.
Z: Set if the result is "0"; cleared otherwise.
S: Cleared to "0".
V: Undefined.
D: Unaffected.
H: Unaffected.

Format:

			Bytes	Cycles	Opcode (Hex)	Addr Mode dst	Addr Mode src
opc	dst | b | 0	src	3	6	07	r0	Rb
opc	src | b | 1	dst	3	6	07	Rb	r0

NOTE: In the second byte of the 3-byte instruction formats, the destination (or source) address is four bits, the bit address 'b' is three bits, and the LSB address value is one bit.

Examples: Given: R1 = 07H and register 01H = 03H:

BOR R1, 01H.1 → R1 = 07H, register 01H = 03H

BOR 01H.2, R1 → Register 01H = 07H, R1 = 07H

In the first example, destination working register R1 contains the value 07H (00000111B) and source register 01H the value 03H (00000011B). The statement "BOR R1,01H.1" logically ORs bit one of register 01H (source) with bit zero of R1 (destination). This leaves the same value (07H) in working register R1.

In the second example, destination register 01H contains the value 03H (00000011B) and the source working register R1 the value 07H (00000111B). The statement "BOR 01H.2,R1" logically ORs bit two of register 01H (destination) with bit zero of R1 (source). This leaves the value 07H in register 01H.

BTJRF – Bit Test, Jump Relative on False

BTJRF dst,src.b

Operation: If src(b) is a "0", then PC ← PC + dst

The specified bit within the source operand is tested. If it is a "0", the relative address is added to the program counter and control passes to the statement whose address is now in the PC; otherwise, the instruction following the BTJRF instruction is executed.

Flags: No flags are affected.

Format:

(Note 1)

opc	src | b | 0	dst

Bytes	Cycles	Opcode (Hex)	Addr Mode dst	Addr Mode src
3	10	37	RA	rb

NOTE: In the second byte of the instruction format, the source address is four bits, the bit address 'b' is three bits, and the LSB address value is one bit in length.

Example: Given: R1 = 07H:

BTJRF SKIP,R1.3 → PC jumps to SKIP location

If working register R1 contains the value 07H (00000111B), the statement "BTJRF SKIP,R1.3" tests bit 3. Because it is "0", the relative address is added to the PC and the PC jumps to the memory location pointed to by the SKIP. (Remember that the memory location must be within the allowed range of + 127 to – 128.)

BTJRT – Bit Test, Jump Relative on True

BTJRT dst,src.b

Operation: If src(b) is a "1", then PC ← PC + dst

The specified bit within the source operand is tested. If it is a "1", the relative address is added to the program counter and control passes to the statement whose address is now in the PC; otherwise, the instruction following the BTJRT instruction is executed.

Flags: No flags are affected.

Format:

(Note 1)

opc	src | b | 1	dst

Bytes	Cycles	Opcode (Hex)	Addr Mode dst	Addr Mode src
3	10	37	RA	rb

NOTE: In the second byte of the instruction format, the source address is four bits, the bit address 'b' is three bits, and the LSB address value is one bit in length.

Example: Given: R1 = 07H:

```
BTJRT    SKIP,R1.1
```

If working register R1 contains the value 07H (00000111B), the statement "BTJRT SKIP,R1.1" tests bit one in the source register (R1). Because it is a "1", the relative address is added to the PC and the PC jumps to the memory location pointed to by the SKIP. (Remember that the memory location must be within the allowed range of + 127 to – 128.)

BXOR – Bit XOR

BXOR dst,src.b

BXOR dst.b,src

Operation: dst(0) ← dst(0) XOR src(b)

or

dst(b) ← dst(b) XOR src(0)

The specified bit of the source (or the destination) is logically exclusive-ORed with bit zero (LSB) of the destination (or source). The result bit is stored in the specified bit of the destination. No other bits of the destination are affected. The source is unaffected.

Flags:
C: Unaffected.
Z: Set if the result is "0"; cleared otherwise.
S: Cleared to "0".
V: Undefined.
D: Unaffected.
H: Unaffected.

Format:

			Bytes	Cycles	Opcode (Hex)	Addr Mode dst	src
opc	dst | b | 0	src	3	6	27	r0	Rb
opc	src | b | 1	dst	3	6	27	Rb	r0

NOTE: In the second byte of the 3-byte instruction formats, the destination (or source) address is four bits, the bit address 'b' is three bits, and the LSB address value is one bit in length.

Examples: Given: R1 = 07H (00000111B) and register 01H = 03H (00000011B):

BXOR R1,01H.1 → R1 = 06H, register 01H = 03H

BXOR 01H.2,R1 → Register 01H = 07H, R1 = 07H

In the first example, destination working register R1 has the value 07H (00000111B) and source register 01H has the value 03H (00000011B). The statement "BXOR R1,01H.1" exclusive-ORs bit one of register 01H (source) with bit zero of R1 (destination). The result bit value is stored in bit zero of R1, changing its value from 07H to 06H. The value of source register 01H is unaffected.

CALL – Call Procedure

CALL dst

Operation:
SP ← SP – 1
@SP ← PCL
SP ← SP – 1
@SP ← PCH
PC ← dst

The current contents of the program counter are pushed onto the top of the stack. The program counter value used is the address of the first instruction following the CALL instruction. The specified destination address is then loaded into the program counter and points to the first instruction of a procedure. At the end of the procedure the return instruction (RET) can be used to return to the original program flow. RET pops the top of the stack back into the program counter.

Flags: No flags are affected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst
opc | dst	3	14	F6	DA
opc | dst	2	12	F4	IRR
opc | dst	2	14	D4	IA

Examples: Given: R0 = 35H, R1 = 21H, PC = 1A47H, and SP = 0002H:

CALL 3521H → SP = 0000H
(Memory locations 0000H = 1AH, 0001H = 4AH, where 4AH is the address that follows the instruction.)

CALL @RR0 → SP = 0000H (0000H = 1AH, 0001H = 49H)

CALL #40H → SP = 0000H (0000H = 1AH, 0001H = 49H)

In the first example, if the program counter value is 1A47H and the stack pointer contains the value 0002H, the statement "CALL 3521H" pushes the current PC value onto the top of the stack. The stack pointer now points to memory location 0000H. The PC is then loaded with the value 3521H, the address of the first instruction in the program sequence to be executed.

If the contents of the program counter and stack pointer are the same as in the first example, the statement "CALL @RR0" produces the same result except that the 49H is stored in stack location 0001H (because the two-byte instruction format was used). The PC is then loaded with the value 3521H, the address of the first instruction in the program sequence to be executed. Assuming that the contents of the program counter and stack pointer are the same as in the first example, if program address 0040H contains 35H and program address 0041H contains 21H, the statement "CALL #40H" produces the same result as in the second example.

CCF – Complement Carry Flag

CCF

Operation: C ← NOT C

The carry flag (C) is complemented. If C = "1", the value of the carry flag is changed to logic zero; if C = "0", the value of the carry flag is changed to logic one.

Flags: **C:** Complemented.

No other flags are affected.

Format:

	Bytes	Cycles	Opcode (Hex)
opc	1	4	EF

Example: Given: The carry flag = "0":

CCF

If the carry flag = "0", the CCF instruction complements it in the FLAGS register (0D5H), changing its value from logic zero to logic one.

CLR – Clear

CLR dst

Operation: dst ← "0"

The destination location is cleared to "0".

Flags: No flags are affected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst
opc | dst	2	4	B0	R
		4	B1	IR

Examples: Given: Register 00H = 4FH, register 01H = 02H, and register 02H = 5EH:

CLR 00H → Register 00H = 00H

CLR @01H → Register 01H = 02H, register 02H = 00H

In Register (R) addressing mode, the statement "CLR 00H" clears the destination register 00H value to 00H. In the second example, the statement "CLR @01H" uses Indirect Register (IR) addressing mode to clear the 02H register value to 00H.

COM – Complement

COM dst

Operation: dst ← NOT dst

The contents of the destination location are complemented (one's complement); all "1s" are changed to "0s", and vice-versa.

Flags:
C: Unaffected.
Z: Set if the result is "0"; cleared otherwise.
S: Set if the result bit 7 is set; cleared otherwise.
V: Always reset to "0".
D: Unaffected.
H: Unaffected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst
opc | dst	2	4	60	R
		4	61	IR

Examples: Given: R1 = 07H and register 07H = 0F1H:

COM R1 → R1 = 0F8H
COM @R1 → R1 = 07H, register 07H = 0EH

In the first example, destination working register R1 contains the value 07H (00000111B). The statement "COM R1" complements all the bits in R1: all logic ones are changed to logic zeros, and vice-versa, leaving the value 0F8H (11111000B).

In the second example, Indirect Register (IR) addressing mode is used to complement the value of destination register 07H (11110001B), leaving the new value 0EH (00001110B).

CP – Compare

CP dst,src

Operation: dst – src

The source operand is compared to (subtracted from) the destination operand, and the appropriate flags are set accordingly. The contents of both operands are unaffected by the comparison.

Flags:
C: Set if a "borrow" occurred (src > dst); cleared otherwise.
Z: Set if the result is "0"; cleared otherwise.
S: Set if the result is negative; cleared otherwise.
V: Set if arithmetic overflow occurred; cleared otherwise.
D: Unaffected.
H: Unaffected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst	src
opc | dst | src	2	4	A2	r	r
		6	A3	r	lr
opc | src | dst	3	6	A4	R	R
		6	A5	R	IR
opc | dst | src	3	6	A6	R	IM

Examples: 1. Given: R1 = 02H and R2 = 03H:

```
        CP      R1,R2   →   Set the C and S flags
```

Destination working register R1 contains the value 02H and source register R2 contains the value 03H. The statement "CP R1,R2" subtracts the R2 value (source/subtrahend) from the R1 value (destination/minuend). Because a "borrow" occurs and the difference is negative, C and S are "1".

2. Given: R1 = 05H and R2 = 0AH:

```
        CP      R1,R2
        JP      UGE,SKIP
        INC     R1
SKIP    LD      R3,R1
```

In this example, destination working register R1 contains the value 05H which is less than the contents of the source working register R2 (0AH). The statement "CP R1,R2" generates C = "1" and the JP instruction does not jump to the SKIP location. After the statement "LD R3,R1" executes, the value 06H remains in working register R3.

CPIJE – Compare, Increment, and Jump on Equal

CPIJE dst,src,RA

Operation: If dst – src = "0", PC ← PC + RA

Ir ← Ir + 1

The source operand is compared to (subtracted from) the destination operand. If the result is "0", the relative address is added to the program counter and control passes to the statement whose address is now in the program counter. Otherwise, the instruction immediately following the CPIJE instruction is executed. In either case, the source pointer is incremented by one before the next instruction is executed.

Flags: No flags are affected.

Format:

				Bytes	Cycles	Opcode (Hex)	Addr Mode dst	Addr Mode src
opc	src	dst	RA	3	12	C2	r	Ir

NOTE: Execution time is 18 cycles if the jump is taken or 16 cycles if it is not taken.

Example: Given: R1 = 02H, R2 = 03H, and register 03H = 02H:

CPIJE R1,@R2,SKIP → R2 = 04H, PC jumps to SKIP location

In this example, working register R1 contains the value 02H, working register R2 the value 03H, and register 03 contains 02H. The statement "CPIJE R1,@R2,SKIP" compares the @R2 value 02H (00000010B) to 02H (00000010B). Because the result of the comparison is *equal*, the relative address is added to the PC and the PC then jumps to the memory location pointed to by SKIP. The source register (R2) is incremented by one, leaving a value of 04H. (Remember that the memory location must be within the allowed range of + 127 to – 128.)

CPIJNE – Compare, Increment, and Jump on Non-Equal

CPIJNE dst,src,RA

Operation: If dst – src _ "0", PC ← PC + RA

Ir ← Ir + 1

The source operand is compared to (subtracted from) the destination operand. If the result is not "0", the relative address is added to the program counter and control passes to the statement whose address is now in the program counter; otherwise the instruction following the CPIJNE instruction is executed. In either case the source pointer is incremented by one before the next instruction.

Flags: No flags are affected.

Format:

				Bytes	Cycles	Opcode (Hex)	Addr Mode dst	src
opc	src	dst	RA	3	12	D2	r	Ir

NOTE: Execution time is 18 cycles if the jump is taken or 16 cycles if it is not taken.

Example: Given: R1 = 02H, R2 = 03H, and register 03H = 04H:

CPIJNE R1,@R2,SKIP → R2 = 04H, PC jumps to SKIP location

Working register R1 contains the value 02H, working register R2 (the source pointer) the value 03H, and general register 03 the value 04H. The statement "CPIJNE R1,@R2,SKIP" subtracts 04H (00000100B) from 02H (00000010B). Because the result of the comparison is *non-equal*, the relative address is added to the PC and the PC then jumps to the memory location pointed to by SKIP. The source pointer register (R2) is also incremented by one, leaving a value of 04H. (Remember that the memory location must be within the allowed range of + 127 to – 128.)

DA – Decimal Adjust

DA dst

Operation: dst ← DA dst

The destination operand is adjusted to form two 4-bit BCD digits following an addition or subtraction operation. For addition (ADD, ADC) or subtraction (SUB, SBC), the following table indicates the operation performed. (The operation is undefined if the destination operand was not the result of a valid addition or subtraction of BCD digits):

Instruction	Carry Before DA	Bits 4–7 Value (Hex)	H Flag Before DA	Bits 0–3 Value (Hex)	Number Added to Byte	Carry After DA
	0	0–9	0	0–9	00	0
	0	0–8	0	A–F	06	0
	0	0–9	1	0–3	06	0
ADD	0	A–F	0	0–9	60	1
ADC	0	9–F	0	A–F	66	1
	0	A–F	1	0–3	66	1
	1	0–2	0	0–9	60	1
	1	0–2	0	A–F	66	1
	1	0–3	1	0–3	66	1
	0	0–9	0	0–9	00 = – 00	0
SUB	0	0–8	1	6–F	FA = – 06	0
SBC	1	7–F	0	0–9	A0 = – 60	1
	1	6–F	1	6–F	9A = – 66	1

Flags:
C: Set if there was a carry from the most significant bit; cleared otherwise (see table).
Z: Set if result is "0"; cleared otherwise.
S: Set if result bit 7 is set; cleared otherwise.
V: Undefined.
D: Unaffected.
H: Unaffected.

Format:

opc	dst

Bytes	Cycles	Opcode (Hex)	Addr Mode dst
2	4	40	R
	4	41	IR

DA – Decimal Adjust

DA (Continued)

Example: Given: Working register R0 contains the value 15 (BCD), working register R1 contains 27 (BCD), and address 27H contains 46 (BCD):

```
ADD     R1,R0       ;       C ← "0", H ← "0", Bits 4–7 = 3, bits 0–3 = C, R1 ← 3CH
DA      R1          ;       R1 ← 3CH + 06
```

If addition is performed using the BCD values 15 and 27, the result should be 42. The sum is incorrect, however, when the binary representations are added in the destination location using standard binary arithmetic:

```
    0 0 0 1   0 1 0 1       15
+   0 0 1 0   0 1 1 1       27
    0 0 1 1   1 1 0 0   =   3CH
```

The DA instruction adjusts this result so that the correct BCD representation is obtained:

```
    0 0 1 1   1 1 0 0
+   0 0 0 0   0 1 1 0
    0 1 0 0   0 0 1 0   =   42
```

Assuming the same values given above, the statements

```
SUB     27H,R0      ;       C ← "0", H ← "0", Bits 4–7 = 3, bits 0–3 = 1
DA      @R1         ;       @R1 ← 31–0
```

leave the value 31 (BCD) in address 27H (@R1).

DEC – Decrement

DEC dst

Operation: dst ← dst – 1

The contents of the destination operand are decremented by one.

Flags:
C: Unaffected.
Z: Set if the result is "0"; cleared otherwise.
S: Set if result is negative; cleared otherwise.
V: Set if arithmetic overflow occurred; cleared otherwise.
D: Unaffected.
H: Unaffected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst
opc dst	2	4	00	R
		4	01	IR

Examples: Given: R1 = 03H and register 03H = 10H:

```
DEC   R1     →   R1 = 02H
DEC   @R1    →   Register 03H = 0FH
```

In the first example, if working register R1 contains the value 03H, the statement "DEC R1" decrements the hexadecimal value by one, leaving the value 02H. In the second example, the statement "DEC @R1" decrements the value 10H contained in the destination register 03H by one, leaving the value 0FH.

DECW – Decrement Word

DECW dst

Operation: dst ← dst – 1

The contents of the destination location (which must be an even address) and the operand following that location are treated as a single 16-bit value that is decremented by one.

Flags:
C: Unaffected.
Z: Set if the result is "0"; cleared otherwise.
S: Set if the result is negative; cleared otherwise.
V: Set if arithmetic overflow occurred; cleared otherwise.
D: Unaffected.
H: Unaffected.

Format:

		Bytes	Cycles	Opcode (Hex)	Addr Mode dst
opc	dst	2	8	80	RR
			8	81	IR

Examples: Given: R0 = 12H, R1 = 34H, R2 = 30H, register 30H = 0FH, and register 31H = 21H:

```
DECW    RR0     →   R0 = 12H, R1 = 33H
DECW    @R2     →   Register 30H = 0FH, register 31H = 20H
```

In the first example, destination register R0 contains the value 12H and register R1 the value 34H. The statement "DECW RR0" addresses R0 and the following operand R1 as a 16-bit word and decrements the value of R1 by one, leaving the value 33H.

NOTE: A system malfunction may occur if you use a Zero flag (FLAGS.6) result together with a DECW instruction. To avoid this problem, we recommend that you use DECW as shown in the following example:

```
LOOP:   DECW    RR0
        LD      R2,R1
        OR      R2,R0
        JR      NZ,LOOP
```

DI – Disable Interrupts

DI

Operation: SYM (0) ← 0

Bit zero of the system mode control register, SYM.0, is cleared to "0", globally disabling all interrupt processing. Interrupt requests will continue to set their respective interrupt pending bits, but the CPU will not service them while interrupt processing is disabled.

Flags: No flags are affected.

Format:

	Bytes	Cycles	Opcode (Hex)
opc	1	4	8F

Example: Given: SYM = 01H:

DI

If the value of the SYM register is 01H, the statement "DI" leaves the new value 00H in the register and clears SYM.0 to "0", disabling interrupt processing.

Before changing IMR, interrupt pending and interrupt source control register, be sure DI state.

DIV – Divide (Unsigned)

DIV dst,src

Operation: dst ÷ src

dst (UPPER) ← REMAINDER

dst (LOWER) ← QUOTIENT

The destination operand (16 bits) is divided by the source operand (8 bits). The quotient (8 bits) is stored in the lower half of the destination. The remainder (8 bits) is stored in the upper half of the destination. When the quotient is $\geq 2^8$, the numbers stored in the upper and lower halves of the destination for quotient and remainder are incorrect. Both operands are treated as unsigned integers.

Flags:
C: Set if the V flag is set and quotient is between 2^8 and $2^9 - 1$; cleared otherwise.
Z: Set if divisor or quotient = "0"; cleared otherwise.
S: Set if MSB of quotient = "1"; cleared otherwise.
V: Set if quotient is $\geq 2^8$ or if divisor = "0"; cleared otherwise.
D: Unaffected.
H: Unaffected.

Format:

opc	src	dst

Bytes	Cycles	Opcode (Hex)	Addr Mode dst	src
3	26/10	94	RR	R
	26/10	95	RR	IR
	26/10	96	RR	IM

NOTE: Execution takes 10 cycles if the divide-by-zero is attempted; otherwise it takes 26 cycles.

Examples: Given: R0 = 10H, R1 = 03H, R2 = 40H, register 40H = 80H:

DIV RR0,R2 → R0 = 03H, R1 = 40H

DIV RR0,@R2 → R0 = 03H, R1 = 20H

DIV RR0,#20H → R0 = 03H, R1 = 80H

In the first example, destination working register pair RR0 contains the values 10H (R0) and 03H (R1), and register R2 contains the value 40H. The statement "DIV RR0,R2" divides the 16-bit RR0 value by the 8-bit value of the R2 (source) register. After the DIV instruction, R0 contains the value 03H and R1 contains 40H. The 8-bit remainder is stored in the upper half of the destination register RR0 (R0) and the quotient in the lower half (R1).

DJNZ – Decrement and Jump if Non-Zero

DJNZ r,dst

Operation: r ← r – 1

If r ≠ 0, PC ← PC + dst

The working register being used as a counter is decremented. If the contents of the register are not logic zero after decrementing, the relative address is added to the program counter and control passes to the statement whose address is now in the PC. The range of the relative address is +127 to –128, and the original value of the PC is taken to be the address of the instruction byte following the DJNZ statement.

NOTE: In case of using DJNZ instruction, the working register being used as a counter should be set at the one of location 0C0H to 0CFH with SRP, SRP0, or SRP1 instruction.

Flags: No flags are affected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst
r | opc | dst	2	8 (jump taken)	rA	RA
		8 (no jump)	r = 0 to F	

Example: Given: R1 = 02H and LOOP is the label of a relative address:

```
SRP     #0C0H
DJNZ    R1,LOOP
```

DJNZ is typically used to control a "loop" of instructions. In many cases, a label is used as the destination operand instead of a numeric relative address value. In the example, working register R1 contains the value 02H, and LOOP is the label for a relative address.

The statement "DJNZ R1, LOOP" decrements register R1 by one, leaving the value 01H. Because the contents of R1 after the decrement are non-zero, the jump is taken to the relative address specified by the LOOP label.

EI – Enable Interrupts

EI

Operation: SYM (0) ← 1

An EI instruction sets bit zero of the system mode register, SYM.0 to "1". This allows interrupts to be serviced as they occur (assuming they have highest priority). If an interrupt's pending bit was set while interrupt processing was disabled (by executing a DI instruction), it will be serviced when you execute the EI instruction.

Flags: No flags are affected.

Format:

	Bytes	Cycles	Opcode (Hex)
opc	1	4	9F

Example: Given: SYM = 00H:

EI

If the SYM register contains the value 00H, that is, if interrupts are currently disabled, the statement "EI" sets the SYM register to 01H, enabling all interrupts. (SYM.0 is the enable bit for global interrupt processing.)

ENTER – Enter

ENTER

Operation:

SP ← SP – 2
@SP ← IP
IP ← PC
PC ← @IP
IP ← IP + 2

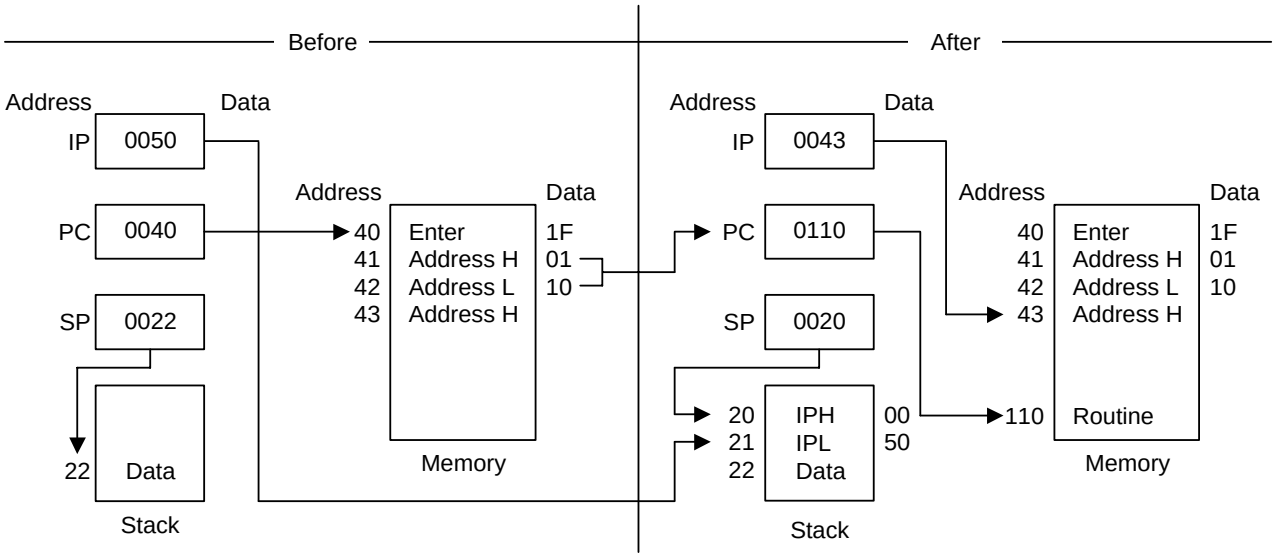
This instruction is useful when implementing threaded-code languages. The contents of the instruction pointer are pushed to the stack. The program counter (PC) value is then written to the instruction pointer. The program memory word that is pointed to by the instruction pointer is loaded into the PC, and the instruction pointer is incremented by two.

Flags: No flags are affected.

Format:

	Bytes	Cycles	Opcode (Hex)
opc	1	14	1F

Example: The diagram below shows one example of how to use an ENTER statement.



EXIT – Exit

EXIT

Operation:

IP ← @SP
SP ← SP + 2
PC ← @IP
IP ← IP + 2

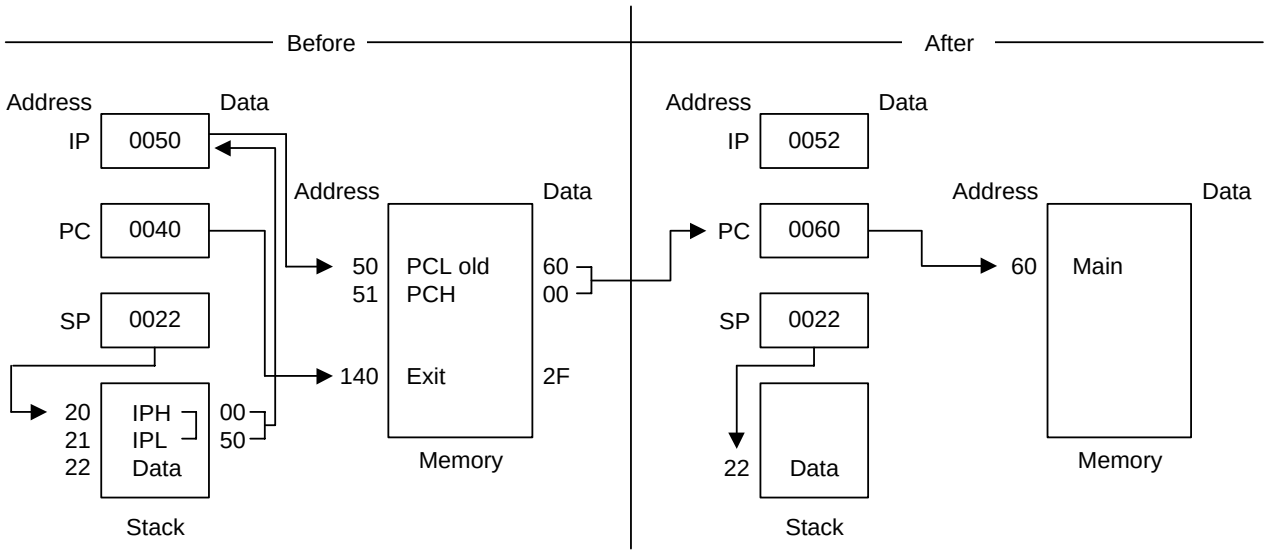
This instruction is useful when implementing threaded-code languages. The stack value is popped and loaded into the instruction pointer. The program memory word that is pointed to by the instruction pointer is then loaded into the program counter, and the instruction pointer is incremented by two.

Flags: No flags are affected.

Format:

	Bytes	Cycles	Opcode (Hex)
opc	1	14 (internal stack) 16 (internal stack)	2F

Example: The diagram below shows one example of how to use an EXIT statement.



IDLE – Idle Operation

IDLE

Operation:

The IDLE instruction stops the CPU clock while allowing system clock oscillation to continue. Idle mode can be released by an interrupt request (IRQ) or an external reset operation.

Flags: No flags are affected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst	src
opc	1	4	6F	–	–

Example: The instruction

IDLE

stops the CPU clock but not the system clock.

INC – Increment

INC dst

Operation: dst ← dst + 1

The contents of the destination operand are incremented by one.

Flags:
C: Unaffected.
Z: Set if the result is "0"; cleared otherwise.
S: Set if the result is negative; cleared otherwise.
V: Set if arithmetic overflow occurred; cleared otherwise.
D: Unaffected.
H: Unaffected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst
dst | opc	1	4	rE	r
			r = 0 to F	
opc | dst	2	4	20	R
		4	21	IR

Examples: Given: R0 = 1BH, register 00H = 0CH, and register 1BH = 0FH:

INC R0 → R0 = 1CH
INC 00H → Register 00H = 0DH
INC @R0 → R0 = 1BH, register 01H = 10H

In the first example, if destination working register R0 contains the value 1BH, the statement "INC R0" leaves the value 1CH in that same register.

The next example shows the effect an INC instruction has on register 00H, assuming that it contains the value 0CH.

In the third example, INC is used in Indirect Register (IR) addressing mode to increment the value of register 1BH from 0FH to 10H.

INCW – Increment Word

INCW dst

Operation: dst ← dst + 1

The contents of the destination (which must be an even address) and the byte following that location are treated as a single 16-bit value that is incremented by one.

Flags:
C: Unaffected.
Z: Set if the result is "0"; cleared otherwise.
S: Set if the result is negative; cleared otherwise.
V: Set if arithmetic overflow occurred; cleared otherwise.
D: Unaffected.
H: Unaffected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst
opc | dst	2	8	A0	RR
		8	A1	IR

Examples: Given: R0 = 1AH, R1 = 02H, register 02H = 0FH, and register 03H = 0FFH:

INCW RR0 → R0 = 1AH, R1 = 03H
INCW @R1 → Register 02H = 10H, register 03H = 00H

In the first example, the working register pair RR0 contains the value 1AH in register R0 and 02H in register R1. The statement "INCW RR0" increments the 16-bit destination by one, leaving the value 03H in register R1. In the second example, the statement "INCW @R1" uses Indirect Register (IR) addressing mode to increment the contents of general register 03H from 0FFH to 00H and register 02H from 0FH to 10H.

NOTE: A system malfunction may occur if you use a Zero (Z) flag (FLAGS.6) result together with an INCW instruction. To avoid this problem, we recommend that you use INCW as shown in the following example:

```
LOOP:   INCW    RR0
        LD      R2,R1
        OR      R2,R0
        JR      NZ,LOOP
```

IRET – Interrupt Return

IRET IRET (Normal) IRET (Fast)

Operation:

IRET (Normal)	IRET (Fast)
FLAGS ← @SP	PC ↔ IP
SP ← SP + 1	FLAGS ← FLAGS'
PC ← @SP	FIS ← 0
SP ← SP + 2	
SYM(0) ← 1	

This instruction is used at the end of an interrupt service routine. It restores the flag register and the program counter. It also re-enables global interrupts. A "normal IRET" is executed only if the fast interrupt status bit (FIS, bit one of the FLAGS register, 0D5H) is cleared (= "0"). If a fast interrupt occurred, IRET clears the FIS bit that was set at the beginning of the service routine.

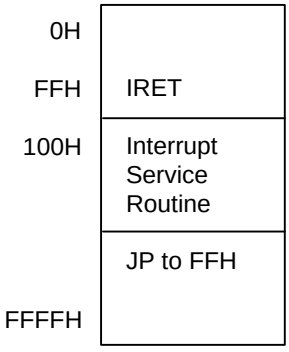
Flags: All flags are restored to their original settings (that is, the settings before the interrupt occurred).

Format:

IRET (Normal)	Bytes	Cycles	Opcode (Hex)
opc	1	10 (internal stack) 12 (internal stack)	BF

IRET (Fast)	Bytes	Cycles	Opcode (Hex)
opc	1	6	BF

Example: In the figure below, the instruction pointer is initially loaded with 100H in the main program before interrupts are enabled. When an interrupt occurs, the program counter and instruction pointer are swapped. This causes the PC to jump to address 100H and the IP to keep the return address. The last instruction in the service routine normally is a jump to IRET at address FFH. This causes the instruction pointer to be loaded with 100H "again" and the program counter to jump back to the main program. Now, the next interrupt can occur and the IP is still correct at 100H.



NOTE: In the fast interrupt example above, if the last instruction is not a jump to IRET, you must pay attention to the order of the last two instructions. The IRET cannot be immediately proceeded by a clearing of the interrupt status (as with a reset of the IPR register).

JP – Jump

JP cc,dst (Conditional)

JP dst (Unconditional)

Operation: If cc is true, PC ← dst

The conditional JUMP instruction transfers program control to the destination address if the condition specified by the condition code (cc) is true; otherwise, the instruction following the JP instruction is executed. The unconditional JP simply replaces the contents of the PC with the contents of the specified register pair. Control then passes to the statement addressed by the PC.

Flags: No flags are affected.

Format: (1)

(2)		Bytes	Cycles	Opcode (Hex)	Addr Mode dst
cc | opc	dst	3	8	ccD cc = 0 to F	DA
opc	dst	2	8	30	IRR

NOTES:
1. The 3-byte format is used for a conditional jump and the 2-byte format for an unconditional jump.
2. In the first byte of the three-byte instruction format (conditional jump), the condition code and the opcode are both four bits.

Examples: Given: The carry flag (C) = "1", register 00 = 01H, and register 01 = 20H:

JP C,LABEL_W → LABEL_W = 1000H, PC = 1000H

JP @00H → PC = 0120H

The first example shows a conditional JP. Assuming that the carry flag is set to "1", the statement "JP C,LABEL_W" replaces the contents of the PC with the value 1000H and transfers control to that location. Had the carry flag not been set, control would then have passed to the statement immediately following the JP instruction.

The second example shows an unconditional JP. The statement "JP @00" replaces the contents of the PC with the contents of the register pair 00H and 01H, leaving the value 0120H.

JR – Jump Relative

JR cc,dst

Operation: If cc is true, PC ← PC + dst

If the condition specified by the condition code (cc) is true, the relative address is added to the program counter and control passes to the statement whose address is now in the program counter; otherwise, the instruction following the JR instruction is executed. (See list of condition codes).

The range of the relative address is +127, –128, and the original value of the program counter is taken to be the address of the first instruction byte following the JR statement.

Flags: No flags are affected.

Format:

(1)	Bytes	Cycles	Opcode (Hex)	Addr Mode dst
cc | opc | dst	2	6	ccB	RA
			cc = 0 to F	

NOTE: In the first byte of the two-byte instruction format, the condition code and the opcode are each four bits.

Example: Given: The carry flag = "1" and LABEL_X = 1FF7H:

JR C,LABEL_X → PC = 1FF7H

If the carry flag is set (that is, if the condition code is true), the statement "JR C,LABEL_X" will pass control to the statement whose address is now in the PC. Otherwise, the program instruction following the JR would be executed.

LD – Load

LD dst, src

Operation: dst ← src

The contents of the source are loaded into the destination. The source's contents are unaffected.

Flags: No flags are affected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst	Addr Mode src
dst | opc / src	2	4	rC	r	IM
		4	r8	r	R
src | opc / dst	2	4	r9	R	r
			r = 0 to F		
opc / dst | src	2	4	C7	r	lr
		4	D7	lr	r
opc / src / dst	3	6	E4	R	R
		6	E5	R	IR
opc / dst / src	3	6	E6	R	IM
		6	D6	IR	IM
opc / src / dst	3	6	F5	IR	R
opc / dst | src / x	3	6	87	r	x [r]
opc / src | dst / x	3	6	97	x [r]	r

LD – Load

LD (Continued)

Examples: Given: R0 = 01H, R1 = 0AH, register 00H = 01H, register 01H = 20H, register 02H = 02H, LOOP = 30H, and register 3AH = 0FFH:

LD	R0,#10H	→	R0 = 10H
LD	R0,01H	→	R0 = 20H, register 01H = 20H
LD	01H,R0	→	Register 01H = 01H, R0 = 01H
LD	R1,@R0	→	R1 = 20H, R0 = 01H
LD	@R0,R1	→	R0 = 01H, R1 = 0AH, register 01H = 0AH
LD	00H,01H	→	Register 00H = 20H, register 01H = 20H
LD	02H,@00H	→	Register 02H = 20H, register 00H = 01H
LD	00H,#0AH	→	Register 00H = 0AH
LD	@00H,#10H	→	Register 00H = 01H, register 01H = 10H
LD	@00H,02H	→	Register 00H = 01H, register 01H = 02, register 02H = 02H
LD	R0,#LOOP[R1]	→	R0 = 0FFH, R1 = 0AH
LD	#LOOP[R0],R1	→	Register 31H = 0AH, R0 = 01H, R1 = 0AH

LDB – Load Bit

LDB dst,src.b

LDB dst.b,src

Operation: dst(0) ← src(b)

or

dst(b) ← src(0)

The specified bit of the source is loaded into bit zero (LSB) of the destination, or bit zero of the source is loaded into the specified bit of the destination. No other bits of the destination are affected. The source is unaffected.

Flags: No flags are affected.

Format:

			Bytes	Cycles	Opcode (Hex)	Addr Mode dst	Addr Mode src
opc	dst | b | 0	src	3	6	47	r0	Rb
opc	src | b | 1	dst	3	6	47	Rb	r0

NOTE: In the second byte of the instruction formats, the destination (or source) address is four bits, the bit address 'b' is three bits, and the LSB address value is one bit in length.

Examples: Given: R0 = 06H and general register 00H = 05H:

LDB R0, 00H.2 → R0 = 07H, register 00H = 05H

LDB 00H.0,R0 → R0 = 06H, register 00H = 04H

In the first example, destination working register R0 contains the value 06H and the source general register 00H the value 05H. The statement "LD R0,00H.2" loads the bit two value of the 00H register into bit zero of the R0 register, leaving the value 07H in register R0.

In the second example, 00H is the destination register. The statement "LD 00H.0,R0" loads bit zero of register R0 to the specified bit (bit zero) of the destination register, leaving 04H in general register 00H.

LDC/LDE – Load Memory

LDC/LDE dst,src

Operation: dst ← src

This instruction loads a byte from program or data memory into a working register or vice-versa. The source values are unaffected. LDC refers to program memory and LDE to data memory. The assembler makes 'Irr' or 'rr' values an even number for program memory and odd an odd number for data memory.

Flags: No flags are affected.

Format:

					Bytes	Cycles	Opcode (Hex)	Addr Mode dst	Addr Mode src
1.	opc	dst | src			2	10	C3	r	Irr
2.	opc	src | dst			2	10	D3	Irr	r
3.	opc	dst | src	XS		3	12	E7	r	XS [rr]
4.	opc	src | dst	XS		3	12	F7	XS [rr]	r
5.	opc	dst | src	XL_L	XL_H	4	14	A7	r	XL [rr]
6.	opc	src | dst	XL_L	XL_H	4	14	B7	XL [rr]	r
7.	opc	dst | 0000	DA_L	DA_H	4	14	A7	r	DA
8.	opc	src | 0000	DA_L	DA_H	4	14	B7	DA	r
9.	opc	dst | 0001	DA_L	DA_H	4	14	A7	r	DA
10.	opc	src | 0001	DA_L	DA_H	4	14	B7	DA	r

NOTES:

1. The source (src) or working register pair [rr] for formats 5 and 6 cannot use register pair 0–1.
2. For formats 3 and 4, the destination address 'XS [rr]' and the source address 'XS [rr]' are each one byte.
3. For formats 5 and 6, the destination address 'XL [rr] and the source address 'XL [rr]' are each two bytes.
4. The DA and r source values for formats 7 and 8 are used to address program memory; the second set of values, used in formats 9 and 10, are used to address data memory.

LDC/LDE – Load Memory

LDC/LDE (Continued)

Examples: Given: R0 = 11H, R1 = 34H, R2 = 01H, R3 = 04H; Program memory locations 0103H = 4FH, 0104H = 1A, 0105H = 6DH, and 1104H = 88H. External data memory locations 0103H = 5FH, 0104H = 2AH, 0105H = 7DH, and 1104H = 98H:

```
LDC     R0,@RR2          ;  R0 ← contents of program memory location 0104H
                         ;  R0 = 1AH, R2 = 01H, R3 = 04H

LDE     R0,@RR2          ;  R0 ← contents of external data memory location 0104H
                         ;  R0 = 2AH, R2 = 01H, R3 = 04H

LDC (note) @RR2,R0       ;  11H (contents of R0) is loaded into program memory
                         ;  location 0104H (RR2),
                         ;  working registers R0, R2, R3 → no change

LDE     @RR2,R0          ;  11H (contents of R0) is loaded into external data memory
                         ;  location 0104H (RR2),
                         ;  working registers R0, R2, R3 → no change

LDC     R0,#01H[RR2]     ;  R0 ← contents of program memory location 0105H
                         ;  (01H + RR2),
                         ;  R0 = 6DH, R2 = 01H, R3 = 04H

LDE     R0,#01H[RR2]     ;  R0 ← contents of external data memory location 0105H
                         ;  (01H + RR2), R0 = 7DH, R2 = 01H, R3 = 04H

LDC (note) #01H[RR2],R0  ;  11H (contents of R0) is loaded into program memory location
                         ;  0105H (01H + 0104H)

LDE     #01H[RR2],R0     ;  11H (contents of R0) is loaded into external data memory
                         ;  location 0105H (01H + 0104H)

LDC     R0,#1000H[RR2]   ;  R0 ← contents of program memory location 1104H
                         ;  (1000H + 0104H), R0 = 88H, R2 = 01H, R3 = 04H

LDE     R0,#1000H[RR2]   ;  R0 ← contents of external data memory location 1104H
                         ;  (1000H + 0104H), R0 = 98H, R2 = 01H, R3 = 04H

LDC     R0,1104H         ;  R0 ← contents of program memory location 1104H, R0 = 88H

LDE     R0,1104H         ;  R0 ← contents of external data memory location 1104H,
                         ;  R0 = 98H

LDC (note) 1105H,R0      ;  11H (contents of R0) is loaded into program memory location
                         ;  1105H, (1105H) ← 11H

LDE     1105H,R0         ;  11H (contents of R0) is loaded into external data memory
                         ;  location 1105H, (1105H) ← 11H
```

NOTE: These instructions are not supported by masked ROM type devices.

LDCD/LDED – Load Memory and Decrement

LDCD/LDED dst,src

Operation: dst ← src

rr ← rr – 1

These instructions are used for user stacks or block transfers of data from program or data memory to the register file. The address of the memory location is specified by a working register pair. The contents of the source location are loaded into the destination location. The memory address is then decremented. The contents of the source are unaffected.

LDCD references program memory and LDED references external data memory. The assembler makes 'Irr' an even number for program memory and an odd number for data memory.

Flags: No flags are affected.

Format:

		Bytes	Cycles	Opcode (Hex)	Addr Mode dst	src
opc	dst | src	2	10	E2	r	Irr

Examples: Given: R6 = 10H, R7 = 33H, R8 = 12H, program memory location 1033H = 0CDH, and external data memory location 1033H = 0DDH:

```
LDCD    R8,@RR6     ;  0CDH (contents of program memory location 1033H) is loaded
                    ;  into R8 and RR6 is decremented by one
                    ;  R8 = 0CDH, R6 = 10H, R7 = 32H (RR6 ← RR6 – 1)

LDED    R8,@RR6     ;  0DDH (contents of data memory location 1033H) is loaded
                    ;  into R8 and RR6 is decremented by one (RR6 ← RR6 – 1)
                    ;  R8 = 0DDH, R6 = 10H, R7 = 32H
```

LDCI/LDEI – Load Memory and Increment

LDCI/LDEI dst,src

Operation: dst ← src

rr ← rr + 1

These instructions are used for user stacks or block transfers of data from program or data memory to the register file. The address of the memory location is specified by a working register pair. The contents of the source location are loaded into the destination location. The memory address is then incremented automatically. The contents of the source are unaffected.

LDCI refers to program memory and LDEI refers to external data memory. The assembler makes 'Irr' even for program memory and odd for data memory.

Flags: No flags are affected.

Format:

		Bytes	Cycles	Opcode (Hex)	Addr Mode dst	src
opc	dst | src	2	10	E3	r	Irr

Examples: Given: R6 = 10H, R7 = 33H, R8 = 12H, program memory locations 1033H = 0CDH and 1034H = 0C5H; external data memory locations 1033H = 0DDH and 1034H = 0D5H:

```
LDCI    R8,@RR6     ;  0CDH (contents of program memory location 1033H) is loaded
                    ;  into R8 and RR6 is incremented by one (RR6 ← RR6 + 1)
                    ;  R8 = 0CDH, R6 = 10H, R7 = 34H

LDEI    R8,@RR6     ;  0DDH (contents of data memory location 1033H) is loaded
                    ;  into R8 and RR6 is incremented by one (RR6 ← RR6 + 1)
                    ;  R8 = 0DDH, R6 = 10H, R7 = 34H
```

LDCPD/LDEPD – Load Memory with Pre-Decrement

LDCPD/

LDEPD dst,src

Operation: rr ← rr – 1

dst ← src

These instructions are used for block transfers of data from program or data memory from the register file. The address of the memory location is specified by a working register pair and is first decremented. The contents of the source location are then loaded into the destination location. The contents of the source are unaffected.

LDCPD refers to program memory and LDEPD refers to external data memory. The assembler makes 'Irr' an even number for program memory and an odd number for external data memory.

Flags: No flags are affected.

Format:

		Bytes	Cycles	Opcode (Hex)	Addr Mode dst	src
opc	src | dst	2	14	F2	Irr	r

Examples: Given: R0 = 77H, R6 = 30H, and R7 = 00H:

```
LDCPD   @RR6,R0     ; (RR6 ← RR6 – 1)
                    ; 77H (contents of R0) is loaded into program memory location
                    ; 2FFFH (3000H – 1H)
                    ; R0 = 77H, R6 = 2FH, R7 = 0FFH

LDEPD   @RR6,R0     ; (RR6 ← RR6 – 1)
                    ; 77H (contents of R0) is loaded into external data memory
                    ; location 2FFFH (3000H – 1H)
                    ; R0 = 77H, R6 = 2FH, R7 = 0FFH
```

LDCPI/LDEPI – Load Memory with Pre-Increment

LDCPI/

LDEPI dst,src

Operation: rr ← rr + 1

dst ← src

These instructions are used for block transfers of data from program or data memory from the register file. The address of the memory location is specified by a working register pair and is first incremented. The contents of the source location are loaded into the destination location. The contents of the source are unaffected.

LDCPI refers to program memory and LDEPI refers to external data memory. The assembler makes 'Irr' an even number for program memory and an odd number for data memory.

Flags: No flags are affected.

Format:

		Bytes	Cycles	Opcode (Hex)	Addr Mode dst	src
opc	src | dst	2	14	F3	Irr	r

Examples: Given: R0 = 7FH, R6 = 21H, and R7 = 0FFH:

```
LDCPI   @RR6,R0     ; (RR6 ← RR6 + 1)
                    ; 7FH (contents of R0) is loaded into program memory
                    ; location 2200H (21FFH + 1H)
                    ; R0 = 7FH, R6 = 22H, R7 = 00H

LDEPI   @RR6,R0     ; (RR6 ← RR6 + 1)
                    ; 7FH (contents of R0) is loaded into external data memory
                    ; location 2200H (21FFH + 1H)
                    ; R0 = 7FH, R6 = 22H, R7 = 00H
```

LDW – Load Word

LDW dst,src

Operation: dst ← src

The contents of the source (a word) are loaded into the destination. The contents of the source are unaffected.

Flags: No flags are affected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst	Addr Mode src
opc | src | dst	3	8	C4	RR	RR
		8	C5	RR	IR
opc | dst | src	4	8	C6	RR	IML

Examples: Given: R4 = 06H, R5 = 1CH, R6 = 05H, R7 = 02H, register 00H = 1AH, register 01H = 02H, register 02H = 03H, and register 03H = 0FH:

LDW RR6,RR4 → R6 = 06H, R7 = 1CH, R4 = 06H, R5 = 1CH

LDW 00H,02H → Register 00H = 03H, register 01H = 0FH, register 02H = 03H, register 03H = 0FH

LDW RR2,@R7 → R2 = 03H, R3 = 0FH,

LDW 04H,@01H → Register 04H = 03H, register 05H = 0FH

LDW RR6,#1234H → R6 = 12H, R7 = 34H

LDW 02H,#0FEDH → Register 02H = 0FH, register 03H = 0EDH

In the second example, please note that the statement "LDW 00H,02H" loads the contents of the source word 02H, 03H into the destination word 00H, 01H. This leaves the value 03H in general register 00H and the value 0FH in register 01H.

The other examples show how to use the LDW instruction with various addressing modes and formats.

MULT – Multiply (Unsigned)

MULT dst,src

Operation: dst ← dst ∞ src

The 8-bit destination operand (even register of the register pair) is multiplied by the source operand (8 bits) and the product (16 bits) is stored in the register pair specified by the destination address. Both operands are treated as unsigned integers.

Flags:
C: Set if result is > 255; cleared otherwise.
Z: Set if the result is "0"; cleared otherwise.
S: Set if MSB of the result is a "1"; cleared otherwise.
V: Cleared.
D: Unaffected.
H: Unaffected.

Format:

opc	src	dst

Bytes	Cycles	Opcode (Hex)	Addr Mode dst	src
3	22	84	RR	R
	22	85	RR	IR
	22	86	RR	IM

Examples: Given: Register 00H = 20H, register 01H = 03H, register 02H = 09H, register 03H = 06H:

MULT 00H, 02H → Register 00H = 01H, register 01H = 20H, register 02H = 09H
MULT 00H, @01H → Register 00H = 00H, register 01H = 0C0H
MULT 00H, #30H → Register 00H = 06H, register 01H = 00H

In the first example, the statement "MULT 00H,02H" multiplies the 8-bit destination operand (in the register 00H of the register pair 00H, 01H) by the source register 02H operand (09H). The 16-bit product, 0120H, is stored in the register pair 00H, 01H.

NEXT – Next

NEXT

Operation: PC ← @ IP

IP ← IP + 2

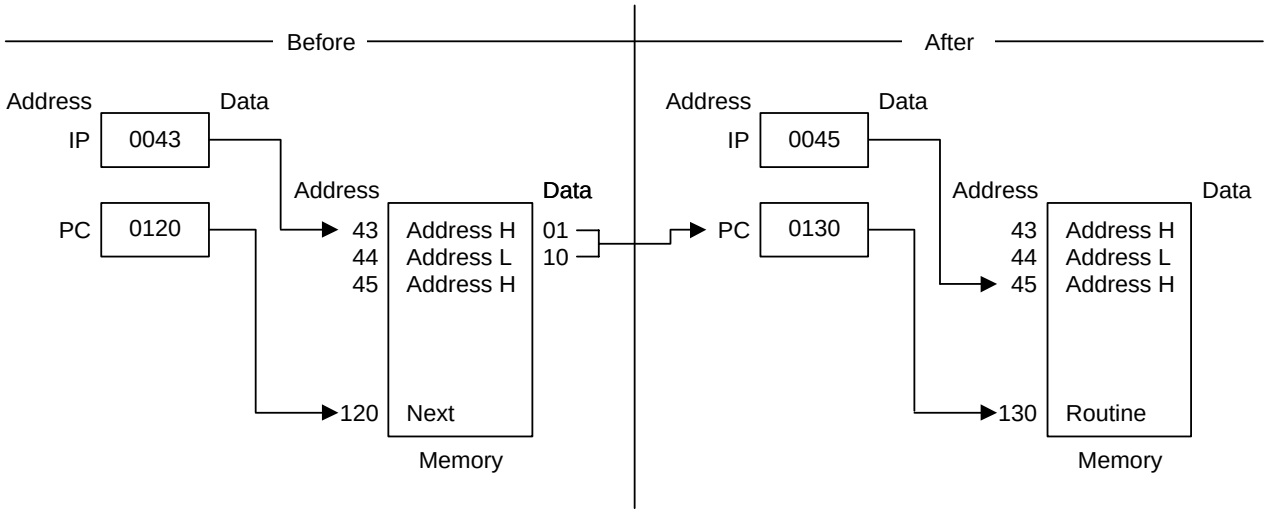
The NEXT instruction is useful when implementing threaded-code languages. The program memory word that is pointed to by the instruction pointer is loaded into the program counter. The instruction pointer is then incremented by two.

Flags: No flags are affected.

Format:

	Bytes	Cycles	Opcode (Hex)
opc	1	10	0F

Example: The following diagram shows one example of how to use the NEXT instruction.



NOP – No Operation

NOP

Operation: No action is performed when the CPU executes this instruction. Typically, one or more NOPs are executed in sequence in order to effect a timing delay of variable duration.

Flags: No flags are affected.

Format:

	Bytes	Cycles	Opcode (Hex)
opc	1	4	FF

Example: When the instruction

NOP

is encountered in a program, no operation occurs. Instead, there is a delay in instruction execution time.

OR – Logical OR

OR dst,src

Operation: dst ← dst OR src

The source operand is logically ORed with the destination operand and the result is stored in the destination. The contents of the source are unaffected. The OR operation results in a "1" being stored whenever either of the corresponding bits in the two operands is a "1"; otherwise a "0" is stored.

Flags:
C: Unaffected.
Z: Set if the result is "0"; cleared otherwise.
S: Set if the result bit 7 is set; cleared otherwise.
V: Always cleared to "0".
D: Unaffected.
H: Unaffected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst	Addr Mode src
opc | dst | src	2	4	42	r	r
		6	43	r	lr
opc | src | dst	3	6	44	R	R
		6	45	R	IR
opc | dst | src	3	6	46	R	IM

Examples: Given: R0 = 15H, R1 = 2AH, R2 = 01H, register 00H = 08H, register 01H = 37H, and register 08H = 8AH:

OR R0,R1 → R0 = 3FH, R1 = 2AH
OR R0,@R2 → R0 = 37H, R2 = 01H, register 01H = 37H
OR 00H,01H → Register 00H = 3FH, register 01H = 37H
OR 01H,@00H → Register 00H = 08H, register 01H = 0BFH
OR 00H,#02H → Register 00H = 0AH

In the first example, if working register R0 contains the value 15H and register R1 the value 2AH, the statement "OR R0,R1" logical-ORs the R0 and R1 register contents and stores the result (3FH) in destination register R0.

The other examples show the use of the logical OR instruction with the various addressing modes and formats.

POP – Pop From Stack

POP dst

Operation: dst ← @SP

SP ← SP + 1

The contents of the location addressed by the stack pointer are loaded into the destination. The stack pointer is then incremented by one.

Flags: No flags affected.

Format:

opc	dst

Bytes	Cycles	Opcode (Hex)	Addr Mode dst
2	8	50	R
	8	51	IR

Examples: Given: Register 00H = 01H, register 01H = 1BH, SPH (0D8H) = 00H, SPL (0D9H) = 0FBH, and stack register 0FBH = 55H:

POP 00H → Register 00H = 55H, SP = 00FCH

POP @00H → Register 00H = 01H, register 01H = 55H, SP = 00FCH

In the first example, general register 00H contains the value 01H. The statement "POP 00H" loads the contents of location 00FBH (55H) into destination register 00H and then increments the stack pointer by one. Register 00H then contains the value 55H and the SP points to location 00FCH.

POPUD – Pop User Stack (Decrementing)

POPUD dst,src

Operation: dst ← src

IR ← IR – 1

This instruction is used for user-defined stacks in the register file. The contents of the register file location addressed by the user stack pointer are loaded into the destination. The user stack pointer is then decremented.

Flags: No flags are affected.

Format:

			Bytes	Cycles	Opcode (Hex)	Addr Mode dst	src
opc	src	dst	3	8	92	R	IR

Example: Given: Register 00H = 42H (user stack pointer register), register 42H = 6FH, and register 02H = 70H:

POPUD 02H,@00H → Register 00H = 41H, register 02H = 6FH, register 42H = 6FH

If general register 00H contains the value 42H and register 42H the value 6FH, the statement "POPUD 02H,@00H" loads the contents of register 42H into the destination register 02H. The user stack pointer is then decremented by one, leaving the value 41H.

POPUI – Pop User Stack (Incrementing)

POPUI dst,src

Operation: dst ← src

IR ← IR + 1

The POPUI instruction is used for user-defined stacks in the register file. The contents of the register file location addressed by the user stack pointer are loaded into the destination. The user stack pointer is then incremented.

Flags: No flags are affected.

Format:

			Bytes	Cycles	Opcode (Hex)	Addr Mode dst	Addr Mode src
opc	src	dst	3	8	93	R	IR

Example: Given: Register 00H = 01H and register 01H = 70H:

POPUI 02H,@00H → Register 00H = 02H, register 01H = 70H, register 02H = 70H

If general register 00H contains the value 01H and register 01H the value 70H, the statement "POPUI 02H,@00H" loads the value 70H into the destination general register 02H. The user stack pointer (register 00H) is then incremented by one, changing its value from 01H to 02H.

PUSH – Push To Stack

PUSH src

Operation: SP ← SP – 1

@SP ← src

A PUSH instruction decrements the stack pointer value and loads the contents of the source (src) into the location addressed by the decremented stack pointer. The operation then adds the new value to the top of the stack.

Flags: No flags are affected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst
opc | src	2	8 (internal clock)	70	R
		8 (external clock)		
		8 (internal clock)		
		8 (external clock)	71	IR

Examples: Given: Register 40H = 4FH, register 4FH = 0AAH, SPH = 00H, and SPL = 00H:

PUSH 40H → Register 40H = 4FH, stack register 0FFH = 4FH, SPH = 0FFH, SPL = 0FFH

PUSH @40H → Register 40H = 4FH, register 4FH = 0AAH, stack register 0FFH = 0AAH, SPH = 0FFH, SPL = 0FFH

In the first example, if the stack pointer contains the value 0000H, and general register 40H the value 4FH, the statement "PUSH 40H" decrements the stack pointer from 0000 to 0FFFFH. It then loads the contents of register 40H into location 0FFFFH and adds this new value to the top of the stack.

PUSHUD – Push User Stack (Decrementing)

PUSHUD dst,src

Operation: IR ← IR – 1

dst ← src

This instruction is used to address user-defined stacks in the register file. PUSHUD decrements the user stack pointer and loads the contents of the source into the register addressed by the decremented stack pointer.

Flags: No flags are affected.

Format:

			Bytes	Cycles	Opcode (Hex)	Addr Mode dst	src
opc	dst	src	3	8	82	IR	R

Example: Given: Register 00H = 03H, register 01H = 05H, and register 02H = 1AH:

PUSHUD @00H,01H → Register 00H = 02H, register 01H = 05H, register 02H = 05H

If the user stack pointer (register 00H, for example) contains the value 03H, the statement "PUSHUD @00H,01H" decrements the user stack pointer by one, leaving the value 02H. The 01H register value, 05H, is then loaded into the register addressed by the decremented user stack pointer.

PUSHUI – Push User Stack (Incrementing)

PUSHUI dst,src

Operation: IR ← IR + 1

dst ← src

This instruction is used for user-defined stacks in the register file. PUSHUI increments the user stack pointer and then loads the contents of the source into the register location addressed by the incremented user stack pointer.

Flags: No flags are affected.

Format:

			Bytes	Cycles	Opcode (Hex)	Addr Mode dst	src
opc	dst	src	3	8	83	IR	R

Example: Given: Register 00H = 03H, register 01H = 05H, and register 04H = 2AH:

PUSHUI @00H,01H → Register 00H = 04H, register 01H = 05H, register 04H = 05H

If the user stack pointer (register 00H, for example) contains the value 03H, the statement "PUSHUI @00H,01H" increments the user stack pointer by one, leaving the value 04H. The 01H register value, 05H, is then loaded into the location addressed by the incremented user stack pointer.

RCF – Reset Carry Flag

RCF RCF

Operation: C ← 0

The carry flag is cleared to logic zero, regardless of its previous value.

Flags: **C:** Cleared to "0".

No other flags are affected.

Format:

	Bytes	Cycles	Opcode (Hex)
opc	1	4	CF

Example: Given: C = "1" or "0":

The instruction RCF clears the carry flag (C) to logic zero.

RET – Return

RET

Operation: PC ← @SP

SP ← SP + 2

The RET instruction is normally used to return to the previously executing procedure at the end of a procedure entered by a CALL instruction. The contents of the location addressed by the stack pointer are popped into the program counter. The next statement that is executed is the one that is addressed by the new program counter value.

Flags: No flags are affected.

Format:

	Bytes	Cycles	Opcode (Hex)
opc	1	8 (internal stack) 10 (internal stack)	AF

Example: Given: SP = 00FCH, (SP) = 101AH, and PC = 1234:

RET → PC = 101AH, SP = 00FEH

The statement "RET" pops the contents of stack pointer location 00FCH (10H) into the high byte of the program counter. The stack pointer then pops the value in location 00FEH (1AH) into the PC's low byte and the instruction at location 101AH is executed. The stack pointer now points to memory location 00FEH.

RL – Rotate Left

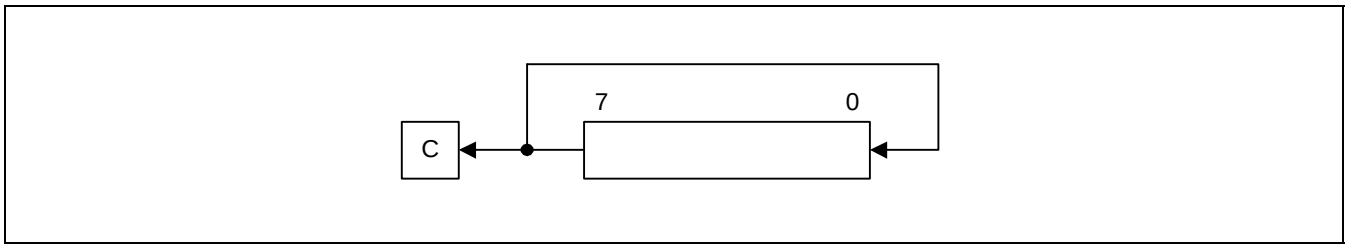
RL dst

Operation: C ← dst (7)

dst (0) ← dst (7)

dst (n + 1) ← dst (n), n = 0–6

The contents of the destination operand are rotated left one bit position. The initial value of bit 7 is moved to the bit zero (LSB) position and also replaces the carry flag.



Flags:
C: Set if the bit rotated from the most significant bit position (bit 7) was "1".
Z: Set if the result is "0"; cleared otherwise.
S: Set if the result bit 7 is set; cleared otherwise.
V: Set if arithmetic overflow occurred; cleared otherwise.
D: Unaffected.
H: Unaffected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst
opc dst	2	4	90	R
		4	91	IR

Examples: Given: Register 00H = 0AAH, register 01H = 02H and register 02H = 17H:

RL 00H → Register 00H = 55H, C = "1"

RL @01H → Register 01H = 02H, register 02H = 2EH, C = "0"

In the first example, if general register 00H contains the value 0AAH (10101010B), the statement "RL 00H" rotates the 0AAH value left one bit position, leaving the new value 55H (01010101B) and setting the carry and overflow flags.

RLC – Rotate Left Through Carry

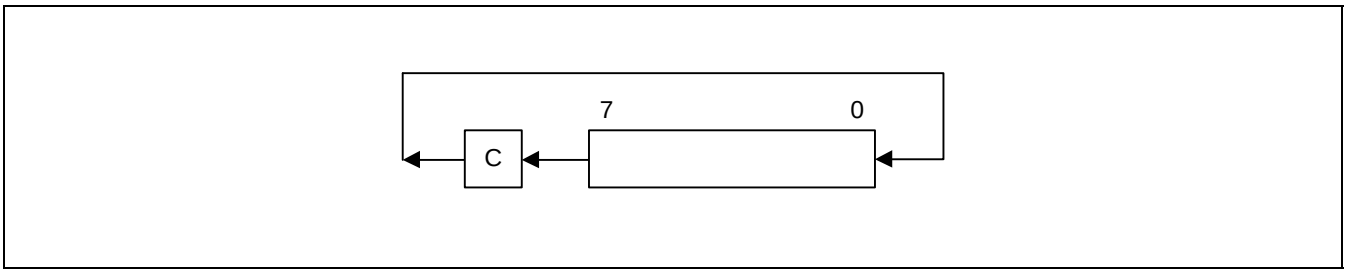
RLC dst

Operation: dst (0) ← C

C ← dst (7)

dst (n + 1) ← dst (n), n = 0–6

The contents of the destination operand with the carry flag are rotated left one bit position. The initial value of bit 7 replaces the carry flag (C); the initial value of the carry flag replaces bit zero.



Flags:
- **C:** Set if the bit rotated from the most significant bit position (bit 7) was "1".
- **Z:** Set if the result is "0"; cleared otherwise.
- **S:** Set if the result bit 7 is set; cleared otherwise.
- **V:** Set if arithmetic overflow occurred, that is, if the sign of the destination changed during rotation; cleared otherwise.
- **D:** Unaffected.
- **H:** Unaffected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst
opc | dst	2	4	10	R
		4	11	IR

Examples: Given: Register 00H = 0AAH, register 01H = 02H, and register 02H = 17H, C = "0":

RLC 00H → Register 00H = 54H, C = "1"

RLC @01H → Register 01H = 02H, register 02H = 2EH, C = "0"

In the first example, if general register 00H has the value 0AAH (10101010B), the statement "RLC 00H" rotates 0AAH one bit position to the left. The initial value of bit 7 sets the carry flag and the initial value of the C flag replaces bit zero of register 00H, leaving the value 55H (01010101B). The MSB of register 00H resets the carry flag to "1" and sets the overflow flag.

RR – Rotate Right

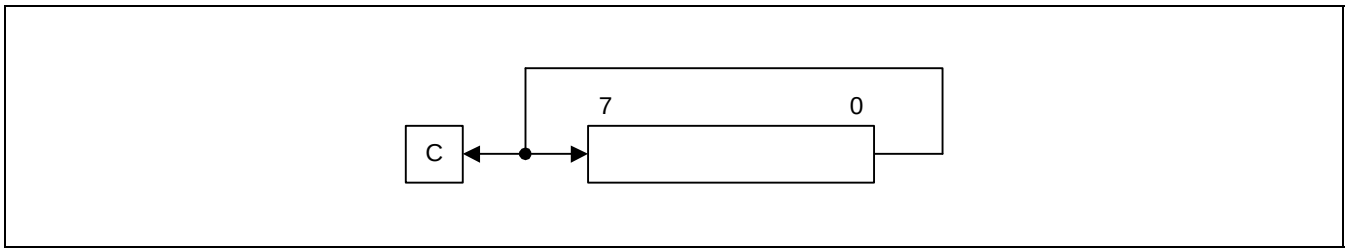
RR dst

Operation: C ← dst (0)

dst (7) ← dst (0)

dst (n) ← dst (n + 1), n = 0–6

The contents of the destination operand are rotated right one bit position. The initial value of bit zero (LSB) is moved to bit 7 (MSB) and also replaces the carry flag (C).



Flags:
- **C:** Set if the bit rotated from the least significant bit position (bit zero) was "1".
- **Z:** Set if the result is "0"; cleared otherwise.
- **S:** Set if the result bit 7 is set; cleared otherwise.
- **V:** Set if arithmetic overflow occurred, that is, if the sign of the destination changed during rotation; cleared otherwise.
- **D:** Unaffected.
- **H:** Unaffected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst
opc | dst	2	4	E0	R
		4	E1	IR

Examples: Given: Register 00H = 31H, register 01H = 02H, and register 02H = 17H:

RR 00H → Register 00H = 98H, C = "1"

RR @01H → Register 01H = 02H, register 02H = 8BH, C = "1"

In the first example, if general register 00H contains the value 31H (00110001B), the statement "RR 00H" rotates this value one bit position to the right. The initial value of bit zero is moved to bit 7, leaving the new value 98H (10011000B) in the destination register. The initial bit zero also resets the C flag to "1" and the sign flag and overflow flag are also set to "1".

RRC – Rotate Right Through Carry

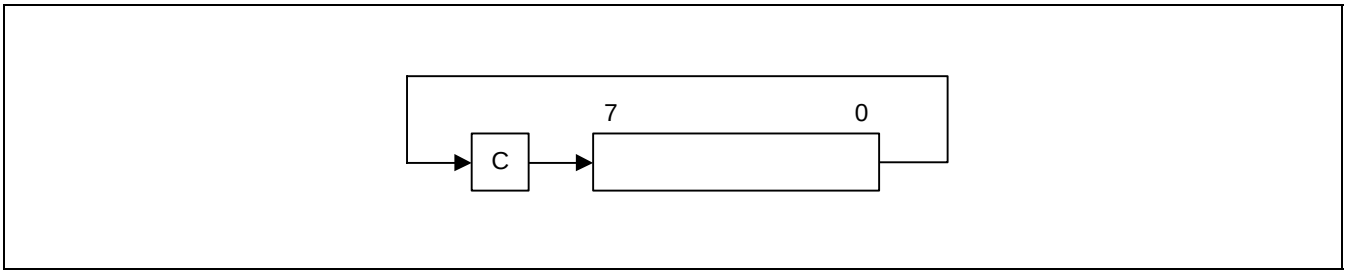
RRC dst

Operation: dst (7) ← C

C ← dst (0)

dst (n) ← dst (n + 1), n = 0–6

The contents of the destination operand and the carry flag are rotated right one bit position. The initial value of bit zero (LSB) replaces the carry flag; the initial value of the carry flag replaces bit 7 (MSB).



Flags:
C: Set if the bit rotated from the least significant bit position (bit zero) was "1".
Z: Set if the result is "0" cleared otherwise.
S: Set if the result bit 7 is set; cleared otherwise.
V: Set if arithmetic overflow occurred, that is, if the sign of the destination changed during rotation; cleared otherwise.
D: Unaffected.
H: Unaffected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst
opc dst	2	4	C0	R
		4	C1	IR

Examples: Given: Register 00H = 55H, register 01H = 02H, register 02H = 17H, and C = "0":

RRC 00H → Register 00H = 2AH, C = "1"
RRC @01H → Register 01H = 02H, register 02H = 0BH, C = "1"

In the first example, if general register 00H contains the value 55H (01010101B), the statement "RRC 00H" rotates this value one bit position to the right. The initial value of bit zero ("1") replaces the carry flag and the initial value of the C flag ("1") replaces bit 7. This leaves the new value 2AH (00101010B) in destination register 00H. The sign flag and overflow flag are both cleared to "0".

SB0 – Select Bank 0

SB0

Operation: BANK ← 0

The SB0 instruction clears the bank address flag in the FLAGS register (FLAGS.0) to logic zero, selecting bank 0 register addressing in the set 1 area of the register file.

Flags: No flags are affected.

Format:

	Bytes	Cycles	Opcode (Hex)
opc	1	4	4F

Example: The statement

SB0

clears FLAGS.0 to "0", selecting bank 0 register addressing.

SB1 – Select Bank 1

SB1

Operation: BANK ← 1

The SB1 instruction sets the bank address flag in the FLAGS register (FLAGS.0) to logic one, selecting bank 1 register addressing in the set 1 area of the register file. (Bank 1 is not implemented in some KS88-series microcontrollers.)

Flags: No flags are affected.

Format:

	Bytes	Cycles	Opcode (Hex)
opc	1	4	5F

Example: The statement

SB1

sets FLAGS.0 to "1", selecting bank 1 register addressing, if implemented.

SBC – Subtract With Carry

SBC dst,src

Operation: dst ← dst – src – c

The source operand, along with the current value of the carry flag, is subtracted from the destination operand and the result is stored in the destination. The contents of the source are unaffected. Subtraction is performed by adding the two's-complement of the source operand to the destination operand. In multiple precision arithmetic, this instruction permits the carry ("borrow") from the subtraction of the low-order operands to be subtracted from the subtraction of high-order operands.

Flags:

C: Set if a borrow occurred (src > dst); cleared otherwise.
Z: Set if the result is "0"; cleared otherwise.
S: Set if the result is negative; cleared otherwise.
V: Set if arithmetic overflow occurred, that is, if the operands were of opposite sign and the sign of the result is the same as the sign of the source; cleared otherwise.
D: Always set to "1".
H: Cleared if there is a carry from the most significant bit of the low-order four bits of the result; set otherwise, indicating a "borrow".

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst	src
opc | dst | src	2	4	32	r	r
		6	33	r	lr
opc | src | dst	3	6	34	R	R
		6	35	R	IR
opc | dst | src	3	6	36	R	IM

Examples: Given: R1 = 10H, R2 = 03H, C = "1", register 01H = 20H, register 02H = 03H, and register 03H = 0AH:

SBC	R1,R2	→	R1 = 0CH, R2 = 03H
SBC	R1,@R2	→	R1 = 05H, R2 = 03H, register 03H = 0AH
SBC	01H,02H	→	Register 01H = 1CH, register 02H = 03H
SBC	01H,@02H	→	Register 01H = 15H,register 02H = 03H, register 03H = 0AH
SBC	01H,#8AH	→	Register 01H = 95H; C, S, and V = "1"

In the first example, if working register R1 contains the value 10H and register R2 the value 03H, the statement "SBC R1,R2" subtracts the source value (03H) and the C flag value ("1") from the destination (10H) and then stores the result (0CH) in register R1.

SCF – Set Carry Flag

SCF

Operation: C ← 1

The carry flag (C) is set to logic one, regardless of its previous value.

Flags: **C:** Set to "1".

No other flags are affected.

Format:

	Bytes	Cycles	Opcode (Hex)
opc	1	4	DF

Example: The statement

SCF

sets the carry flag to logic one.

SRA – Shift Right Arithmetic

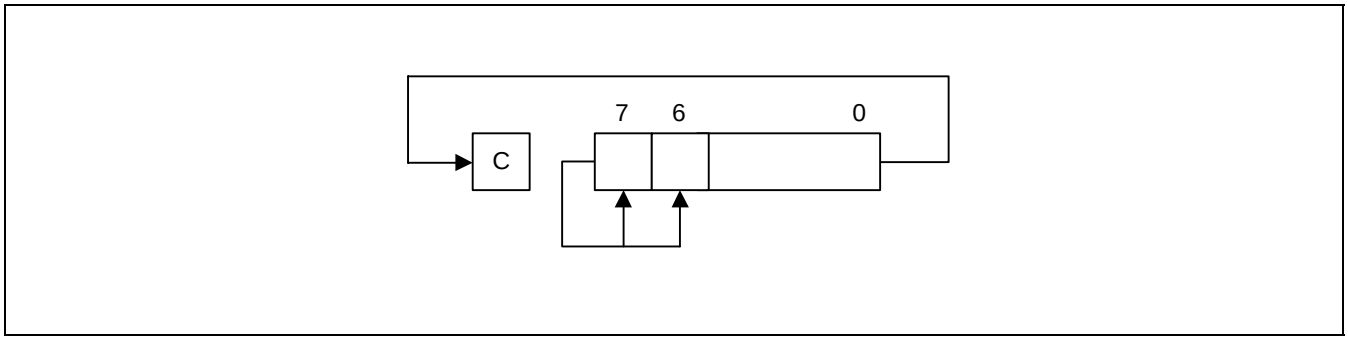
SRA dst

Operation: dst (7) ← dst (7)

C ← dst (0)

dst (n) ← dst (n + 1), n = 0–6

An arithmetic shift-right of one bit position is performed on the destination operand. Bit zero (the LSB) replaces the carry flag. The value of bit 7 (the sign bit) is unchanged and is shifted into bit position 6.



Flags:
C: Set if the bit shifted from the LSB position (bit zero) was "1".
Z: Set if the result is "0"; cleared otherwise.
S: Set if the result is negative; cleared otherwise.
V: Always cleared to "0".
D: Unaffected.
H: Unaffected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst
opc dst	2	4	D0	R
		4	D1	IR

Examples: Given: Register 00H = 9AH, register 02H = 03H, register 03H = 0BCH, and C = "1":

SRA 00H → Register 00H = 0CD, C = "0"

SRA @02H → Register 02H = 03H, register 03H = 0DEH, C = "0"

In the first example, if general register 00H contains the value 9AH (10011010B), the statement "SRA 00H" shifts the bit values in register 00H right one bit position. Bit zero ("0") clears the C flag and bit 7 ("1") is then shifted into the bit 6 position (bit 7 remains unchanged). This leaves the value 0CDH (11001101B) in destination register 00H.

SRP/SRP0/SRP1 – Set Register Pointer

SRP src

SRP0 src

SRP1 src

Operation:

If src (1) = 1 and src (0) = 0 then: RP0 (3–7) ← src (3–7)
If src (1) = 0 and src (0) = 1 then: RP1 (3–7) ← src (3–7)
If src (1) = 0 and src (0) = 0 then: RP0 (4–7) ← src (4–7),
RP0 (3) ← 0
RP1 (4–7) ← src (4–7),
RP1 (3) ← 1

The source data bits one and zero (LSB) determine whether to write one or both of the register pointers, RP0 and RP1. Bits 3–7 of the selected register pointer are written unless both register pointers are selected. RP0.3 is then cleared to logic zero and RP1.3 is set to logic one.

Flags: No flags are affected.

Format:

		Bytes	Cycles	Opcode (Hex)	Addr Mode src
opc	src	2	4	31	IM

Examples: The statement

SRP #40H

sets register pointer 0 (RP0) at location 0D6H to 40H and register pointer 1 (RP1) at location 0D7H to 48H.

The statement "SRP0 #50H" sets RP0 to 50H, and the statement "SRP1 #68H" sets RP1 to 68H.

STOP – Stop Operation

STOP

Operation:

The STOP instruction stops the both the CPU clock and system clock and causes the microcontroller to enter Stop mode. During Stop mode, the contents of on-chip CPU registers, peripheral registers, and I/O port control and data registers are retained. Stop mode can be released by an external reset operation or by external interrupts. For the reset operation, the RESET pin must be held to Low level until the required oscillation stabilization interval has elapsed.

Flags: No flags are affected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst	src
opc	1	4	7F	–	–

Example: The statement

STOP

halts all microcontroller operations.

SUB – Subtract

SUB dst,src

Operation: dst ← dst – src

The source operand is subtracted from the destination operand and the result is stored in the destination. The contents of the source are unaffected. Subtraction is performed by adding the two's complement of the source operand to the destination operand.

Flags:
- **C:** Set if a "borrow" occurred; cleared otherwise.
- **Z:** Set if the result is "0"; cleared otherwise.
- **S:** Set if the result is negative; cleared otherwise.
- **V:** Set if arithmetic overflow occurred, that is, if the operands were of opposite signs and the sign of the result is of the same as the sign of the source operand; cleared otherwise.
- **D:** Always set to "1".
- **H:** Cleared if there is a carry from the most significant bit of the low-order four bits of the result; set otherwise indicating a "borrow".

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst	Addr Mode src
opc | dst | src	2	4	22	r	r
		6	23	r	lr
opc | src | dst	3	6	24	R	R
		6	25	R	IR
opc | dst | src	3	6	26	R	IM

Examples: Given: R1 = 12H, R2 = 03H, register 01H = 21H, register 02H = 03H, register 03H = 0AH:

SUB	R1,R2	→	R1 = 0FH, R2 = 03H
SUB	R1,@R2	→	R1 = 08H, R2 = 03H
SUB	01H,02H	→	Register 01H = 1EH, register 02H = 03H
SUB	01H,@02H	→	Register 01H = 17H, register 02H = 03H
SUB	01H,#90H	→	Register 01H = 91H; C, S, and V = "1"
SUB	01H,#65H	→	Register 01H = 0BCH; C and S = "1", V = "0"

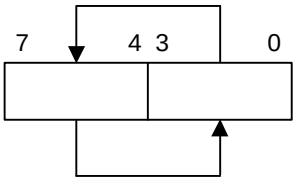
In the first example, if working register R1 contains the value 12H and if register R2 contains the value 03H, the statement "SUB R1,R2" subtracts the source value (03H) from the destination value (12H) and stores the result (0FH) in destination register R1.

SWAP – Swap Nibbles

SWAP dst

Operation: dst (0 – 3) ↔ dst (4 – 7)

The contents of the lower four bits and upper four bits of the destination operand are swapped.



Flags:
C: Undefined.
Z: Set if the result is "0"; cleared otherwise.
S: Set if the result bit 7 is set; cleared otherwise.
V: Undefined.
D: Unaffected.
H: Unaffected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst
opc dst	2	4	F0	R
		4	F1	IR

Examples: Given: Register 00H = 3EH, register 02H = 03H, and register 03H = 0A4H:

SWAP 00H → Register 00H = 0E3H

SWAP @02H → Register 02H = 03H, register 03H = 4AH

In the first example, if general register 00H contains the value 3EH (00111110B), the statement "SWAP 00H" swaps the lower and upper four bits (nibbles) in the 00H register, leaving the value 0E3H (11100011B).

TCM – Test Complement Under Mask

TCM dst,src

Operation: (NOT dst) AND src

This instruction tests selected bits in the destination operand for a logic one value. The bits to be tested are specified by setting a "1" bit in the corresponding position of the source operand (mask). The TCM statement complements the destination operand, which is then ANDed with the source mask. The zero (Z) flag can then be checked to determine the result. The destination and source operands are unaffected.

Flags:
C: Unaffected.
Z: Set if the result is "0"; cleared otherwise.
S: Set if the result bit 7 is set; cleared otherwise.
V: Always cleared to "0".
D: Unaffected.
H: Unaffected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst	src
opc | dst | src	2	4	62	r	r
		6	63	r	lr
opc | src | dst	3	6	64	R	R
		6	65	R	IR
opc | dst | src	3	6	66	R	IM

Examples: Given: R0 = 0C7H, R1 = 02H, R2 = 12H, register 00H = 2BH, register 01H = 02H, and register 02H = 23H:

TCM	R0,R1	→	R0 = 0C7H, R1 = 02H, Z = "1"
TCM	R0,@R1	→	R0 = 0C7H, R1 = 02H, register 02H = 23H, Z = "0"
TCM	00H,01H	→	Register 00H = 2BH, register 01H = 02H, Z = "1"
TCM	00H,@01H	→	Register 00H = 2BH, register 01H = 02H, register 02H = 23H, Z = "1"
TCM	00H,#34	→	Register 00H = 2BH, Z = "0"

In the first example, if working register R0 contains the value 0C7H (11000111B) and register R1 the value 02H (00000010B), the statement "TCM R0,R1" tests bit one in the destination register for a "1" value. Because the mask value corresponds to the test bit, the Z flag is set to logic one and can be tested to determine the result of the TCM operation.

TM – Test Under Mask

TM dst,src

Operation: dst AND src

This instruction tests selected bits in the destination operand for a logic zero value. The bits to be tested are specified by setting a "1" bit in the corresponding position of the source operand (mask), which is ANDed with the destination operand. The zero (Z) flag can then be checked to determine the result. The destination and source operands are unaffected.

Flags:
C: Unaffected.
Z: Set if the result is "0"; cleared otherwise.
S: Set if the result bit 7 is set; cleared otherwise.
V: Always reset to "0".
D: Unaffected.
H: Unaffected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst	Addr Mode src
opc | dst | src	2	4	72	r	r
		6	73	r	lr
opc | src | dst	3	6	74	R	R
		6	75	R	IR
opc | dst | src	3	6	76	R	IM

Examples: Given: R0 = 0C7H, R1 = 02H, R2 = 18H, register 00H = 2BH, register 01H = 02H, and register 02H = 23H:

TM	R0,R1	→	R0 = 0C7H, R1 = 02H, Z = "0"
TM	R0,@R1	→	R0 = 0C7H, R1 = 02H, register 02H = 23H, Z = "0"
TM	00H,01H	→	Register 00H = 2BH, register 01H = 02H, Z = "0"
TM	00H,@01H	→	Register 00H = 2BH, register 01H = 02H, register 02H = 23H, Z = "0"
TM	00H,#54H	→	Register 00H = 2BH, Z = "1"

In the first example, if working register R0 contains the value 0C7H (11000111B) and register R1 the value 02H (00000010B), the statement "TM R0,R1" tests bit one in the destination register for a "0" value. Because the mask value does not match the test bit, the Z flag is cleared to logic zero and can be tested to determine the result of the TM operation.

WFI – Wait For Interrupt

WFI

Operation:

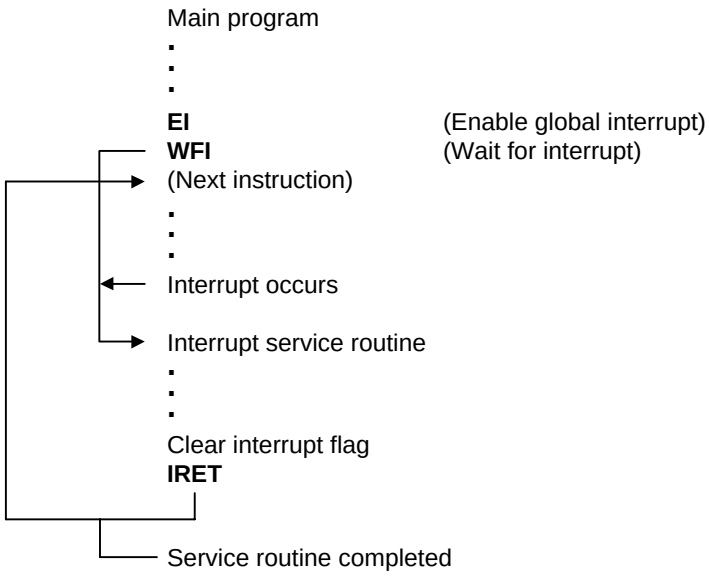
The CPU is effectively halted until an interrupt occurs, except that DMA transfers can still take place during this wait state. The WFI status can be released by an internal interrupt, including a fast interrupt .

Flags: No flags are affected.

Format:

	Bytes	Cycles	Opcode (Hex)
opc	1	4n	3F
		(n = 1, 2, 3, ...)	

Example: The following sample program structure shows the sequence of operations that follow a "WFI" statement:



XOR – Logical Exclusive OR

XOR dst,src

Operation: dst ← dst XOR src

The source operand is logically exclusive-ORed with the destination operand and the result is stored in the destination. The exclusive-OR operation results in a "1" bit being stored whenever the corresponding bits in the operands are different; otherwise, a "0" bit is stored.

Flags:
C: Unaffected.
Z: Set if the result is "0"; cleared otherwise.
S: Set if the result bit 7 is set; cleared otherwise.
V: Always reset to "0".
D: Unaffected.
H: Unaffected.

Format:

	Bytes	Cycles	Opcode (Hex)	Addr Mode dst	src
opc | dst | src	2	4	B2	r	r
		6	B3	r	lr
opc | src | dst	3	6	B4	R	R
		6	B5	R	IR
opc | dst | src	3	6	B6	R	IM

Examples: Given: R0 = 0C7H, R1 = 02H, R2 = 18H, register 00H = 2BH, register 01H = 02H, and register 02H = 23H:

XOR R0,R1 → R0 = 0C5H, R1 = 02H
XOR R0,@R1 → R0 = 0E4H, R1 = 02H, register 02H = 23H
XOR 00H,01H → Register 00H = 29H, register 01H = 02H
XOR 00H,@01H → Register 00H = 08H, register 01H = 02H, register 02H = 23H
XOR 00H,#54H → Register 00H = 7FH

In the first example, if working register R0 contains the value 0C7H and if register R1 contains the value 02H, the statement "XOR R0,R1" logically exclusive-ORs the R1 value with the R0 value and stores the result (0C5H) in the destination register R0.

7 CLOCK CIRCUIT

OVERVIEW

The clock frequency generated for the Main clock of S3F84NB by an external crystal can range from 1 MHz to 12 MHz. The maximum CPU clock frequency is 12 MHz. The X_{IN} and X_{OUT} pins connect the external oscillator or clock source to the on-chip clock circuit. Also the subsystem clock frequency for the Watch timer by an external crystal can range from 30 kHz to 35 kHz. The XT_{IN} and XT_{OUT} pins connect the external oscillator or clock source to the on-chip clock circuit. The sub-system oscillation pins, XT_{IN} and XT_{OUT} can be used for normal digital I/O pins (P6.0, P6.1) if they are not used for oscillation pins.

SYSTEM CLOCK CIRCUIT

The system clock circuit has the following components:

- External crystal or ceramic resonator oscillation source (or an external clock source)
- Oscillator stop and wake-up functions
- Programmable frequency divider for the CPU clock (fxx divided by 1, 2, 8, or 16)
- System clock control register, CLKCON
- Oscillator control register, OSCCON and STOP control register, STPCON

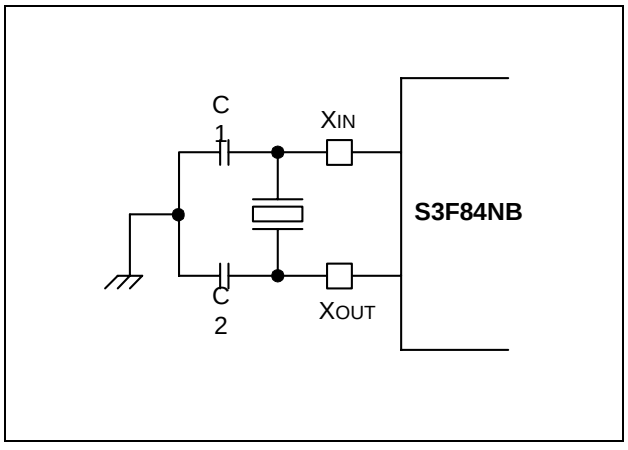


Figure 7-1. Main Oscillator Circuit (Crystal or Ceramic Oscillator)

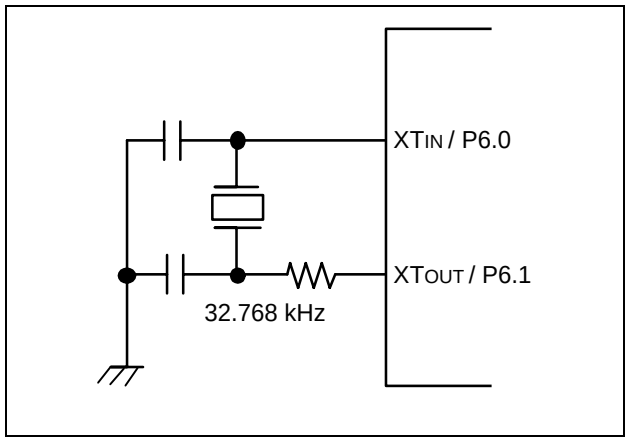


Figure 7-2. Sub-System Oscillator Circuit (Crystal Oscillator)

CLOCK STATUS DURING POWER-DOWN MODES

The two power-down modes, Stop mode and Idle mode, affect the system clock as follows:

- In Stop mode, the main oscillator is halted. Stop mode is released, and the oscillator is started, by a reset operation or an external interrupt (with RC delay noise filter), and can be released by internal interrupt too when the sub-system oscillator is running and watch timer is operating with sub-system clock.
- In Idle mode, the internal clock signal is gated to the CPU, but not to interrupt structure, timers and timer/ counters. Idle mode is released by a reset or by an external or internal interrupt.

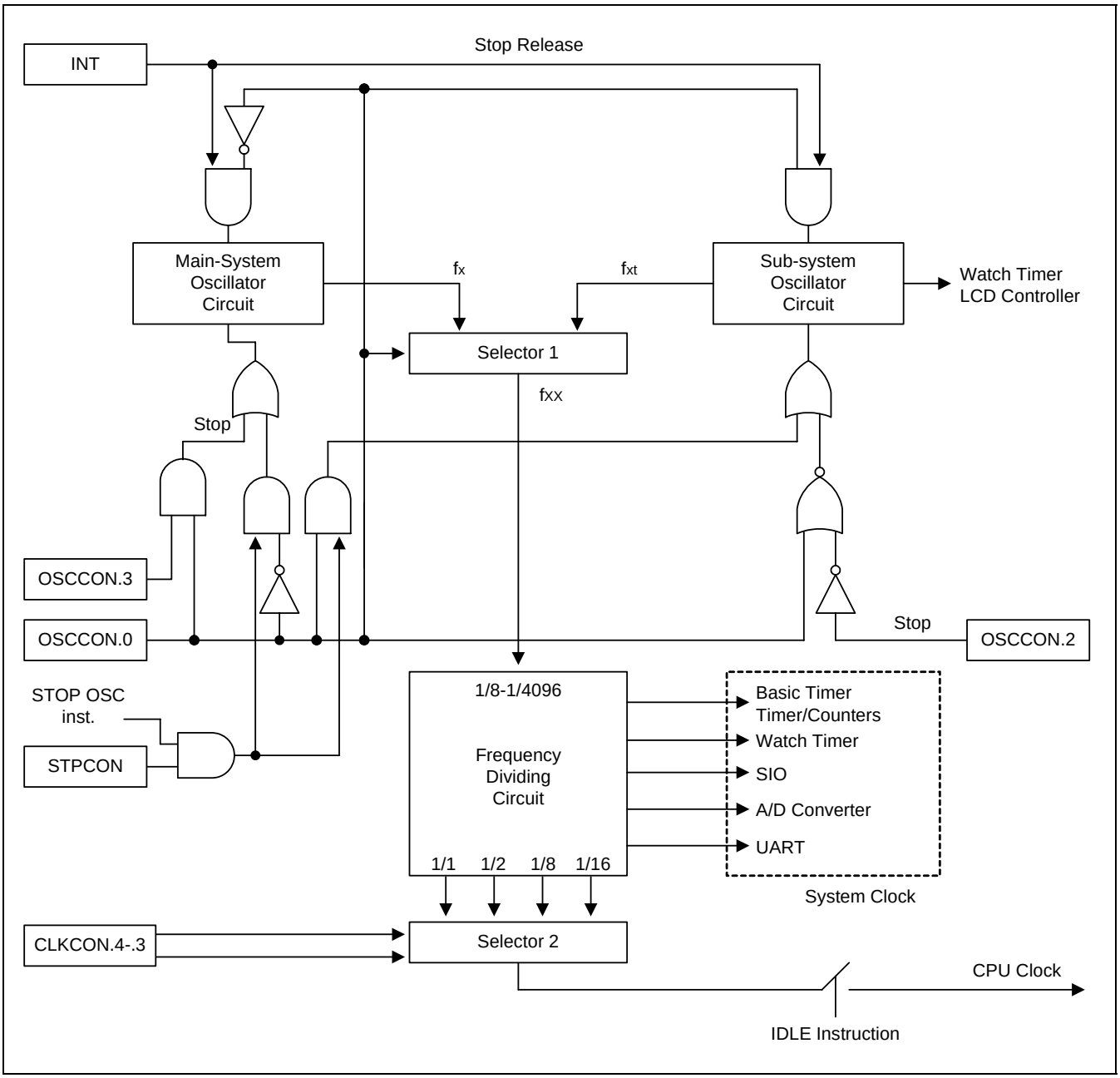


Figure 7-3. System Clock Circuit Diagram

SYSTEM CLOCK CONTROL REGISTER (CLKCON)

The system clock control register, CLKCON, is located in the bank 0 of set 1, address D4H. It is read/write addressable and has the following functions:

- Oscillator frequency divide-by value

After the main oscillator is activated, and the fxx/16 (the slowest clock speed) is selected as the CPU clock. If necessary, you can then increase the CPU clock speed fxx/8, fxx/2, or fxx/1.

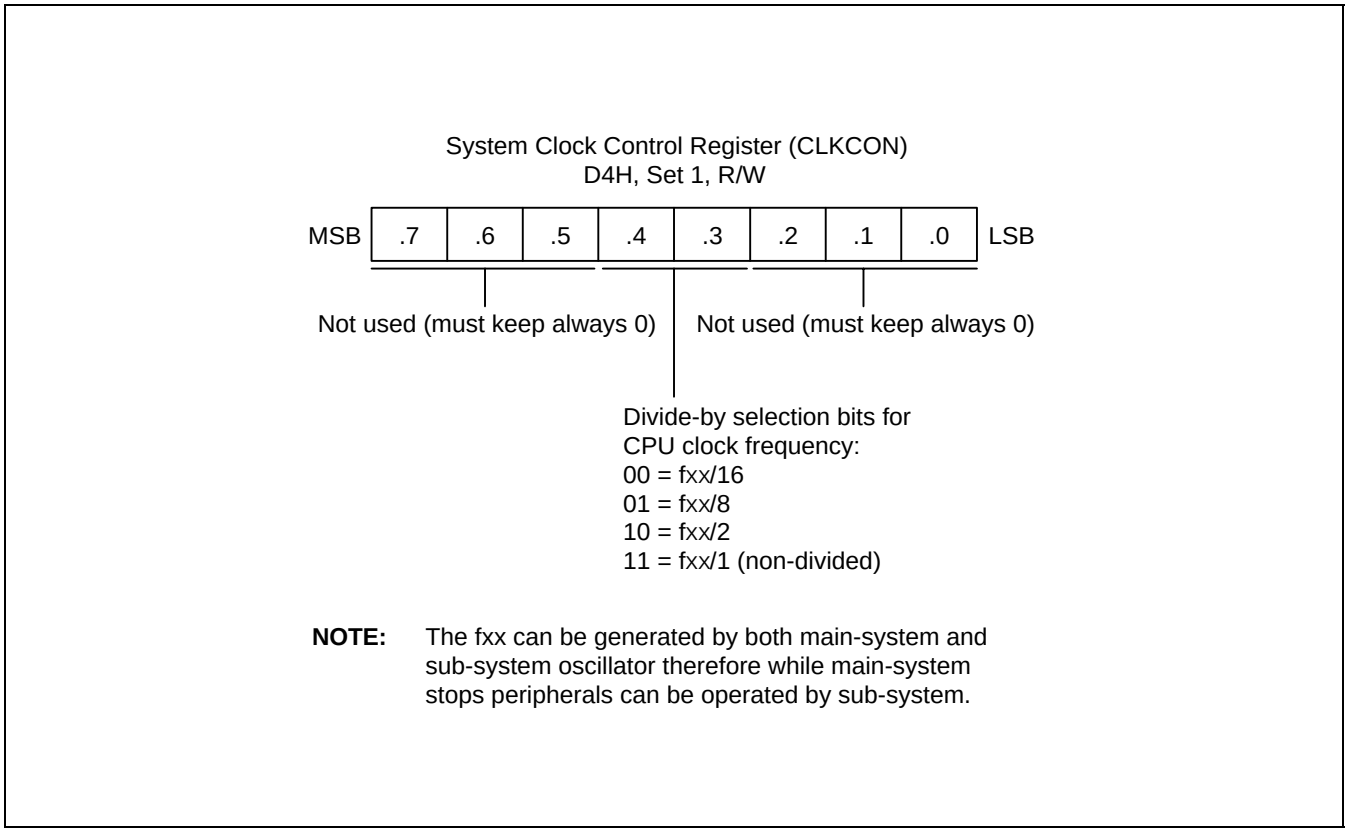
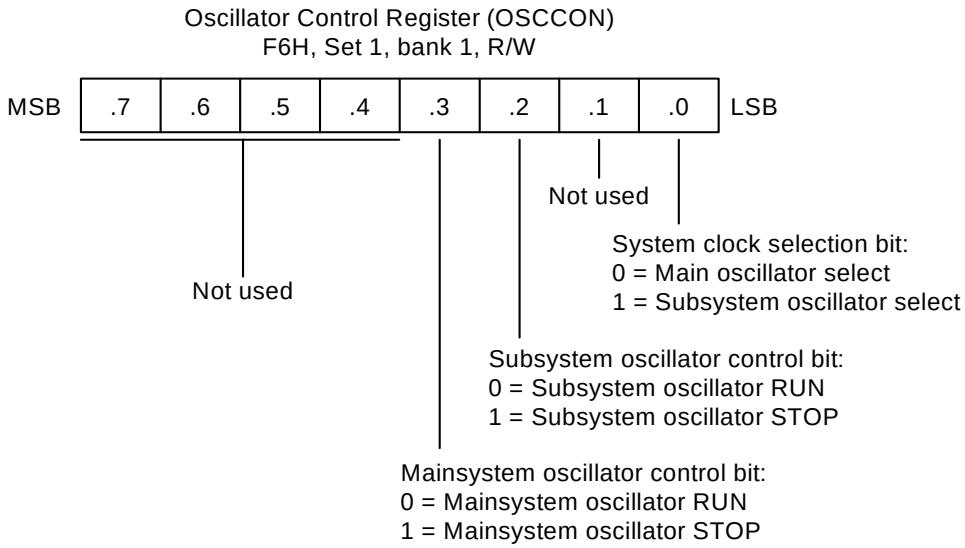


Figure 7-4. System Clock Control Register (CLKCON)



NOTE: When the CPU is operated with fxt (sub-oscillation clock), it is possible to use the stop instruction but in this case before using stop instruction, you must select fxx/128 for basic timer counter clock input.
Then the oscillation stabilization time is 62.5 ((1/32768) x 128 x 16) ms + 100 ms.
Here the warm-up time is from the time that the stop release signal activates to the time that basic timer starts counting.

Figure 7-5. Oscillator Control Register (OSCCON)

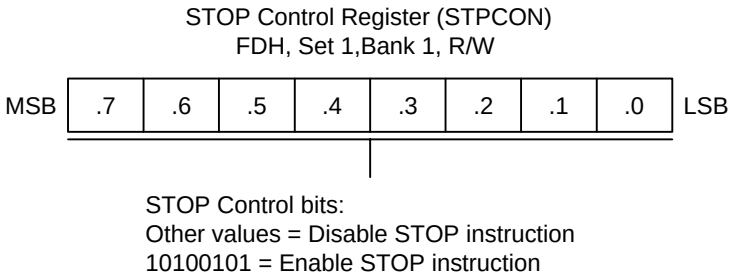


Figure 7-6. STOP Control Register (STPCON)

8 RESET and POWER-DOWN

SYSTEM RESET

OVERVIEW

During a power-on reset, the voltage at V_{DD} goes to High level and the nRESET pin is forced to Low level. The RESET signal is input through a Schmitt trigger circuit where it is then synchronized with the CPU clock. This procedure brings S3F84NB into a known operating status.

To allow time for internal CPU clock oscillation to stabilize, the nRESET pin must be held to Low level for a minimum time interval after the power supply comes within tolerance. The minimum required oscillation stabilization time for a reset operation is 1 millisecond.

Whenever a reset occurs during normal operation (that is, when both V_{DD} and nRESET are High level), the nRESET pin is forced Low and the reset operation starts. All system and peripheral control registers are then reset to their default hardware values

In summary, the following sequence of events occurs during a reset operation:

- Interrupt is disabled.
- The watchdog function (basic timer) is enabled.
- Ports 0-6 are set to input mode, P6.0 and P6.1 are set to XTin and XTout respectively.
- Peripheral control and data registers are disabled and reset to their default hardware values.
- The program counter (PC) is loaded with the program reset address in the ROM, 0100H.
- When the programmed oscillation stabilization time interval has elapsed, the instruction stored in ROM location 0100H (and 0101H) is fetched and executed.

NORMAL MODE RESET OPERATION

In normal (masked ROM) mode, the TEST pin is tied to V_{SS}. A reset enables access to the 48-Kbyte on-chip ROM.

NOTE

To program the duration of the oscillation stabilization interval, you make the appropriate settings to the basic timer control register, BTCON, *before* entering Stop mode. Also, if you do not want to use the basic timer watchdog function (which causes a system reset if a basic timer counter overflow occurs), you can disable it by writing '1010B' to the upper nibble of BTCON.

HARDWARE RESET VALUES

Table 8-1, 8-2, and 8-3 list the reset values for CPU and system registers, peripheral control registers, and peripheral data registers following a reset operation. The following notation is used to represent reset values:

- A "1" or a "0" shows the reset bit value as logic one or logic zero, respectively.
- An "x" means that the bit value is undefined after a reset.
- A dash ("–") means that the bit is either not used or not mapped, but read 0 is the bit value.

Table 8-1. S3F84NB Set 1 Register values after RESET

Register Name	Mnemonic	Address		Bit Values After RESET							
		Dec	Hex	7	6	5	4	3	2	1	0
Timer B control register	TBCON	208	D0H	0	0	0	0	0	0	0	0
Timer B data register (high byte)	TBDATAH	209	D1H	1	1	1	1	1	1	1	1
Timer B data register (low byte)	TBDATAL	210	D2H	1	1	1	1	1	1	1	1
Basic timer control register	BTCON	211	D3H	0	0	0	0	0	0	0	0
Clock Control register	CLKCON	212	D4H	0	0	0	0	0	0	0	0
System flags register	FLAGS	213	D5H	x	x	x	x	x	x	0	0
Register pointer 0	RP0	214	D6H	1	1	0	0	0	–	–	–
Register pointer 1	RP1	215	D7H	1	1	0	0	1	–	–	–
Stack pointer (high byte)	SPH	216	D8H	x	x	x	x	x	x	x	x
Stack pointer (low byte)	SPL	217	D9H	x	x	x	x	x	x	x	x
Instruction pointer (high byte)	IPH	218	DAH	x	x	x	x	x	x	x	x
Instruction pointer (low byte)	IPL	219	DBH	x	x	x	x	x	x	x	x
Interrupt request register	IRQ	220	DCH	0	0	0	0	0	0	0	0
Interrupt mask register	IMR	221	DDH	x	x	x	x	x	x	x	x
System mode register	SYM	222	DEH	0	–	–	x	x	x	0	0
Register page pointer	PP	223	DFH	0	0	0	0	0	0	0	0

Table 8-2. S3F84NB Set 1, Bank 0 Register values after RESET

Register Name	Mnemonic	Address		Bit values after Reset							
		Dec	Hex	7	6	5	4	3	2	1	0
Port 0 data register	P0	224	E0H	0	0	0	0	0	0	0	0
Port 1 data register	P1	225	E1H	0	0	0	0	0	0	0	0
Port 2 data register	P2	226	E2H	0	0	0	0	0	0	0	0
Port 3 data register	P3	227	E3H	0	0	0	0	0	0	0	0
Port 4 data register	P4	228	E4H	0	0	0	0	0	0	0	0
Port 5 data register	P5	229	E5H	0	0	0	0	0	0	0	0
Port 6 data register	P6	230	E6H	0	0	0	0	0	0	0	0
Timer A,1 interrupt pending register	TINTPND	231	E7H	–	–	0	0	0	0	0	0
Port 6 control register (high byte)	P6CONH	232	E8H	0	0	0	0	0	0	0	0
Port 6 control register (low byte)	P6CONL	233	E9H	0	0	0	0	1	1	1	1
Timer A control register	TACON	234	EAH	0	0	0	0	0	0	0	0
Timer A data register	TADATA	235	EBH	1	1	1	1	1	1	1	1
Timer A counter register	TACNT	236	ECH	0	0	0	0	0	0	0	0
Port 6 interrupt control register	P6INT	237	EDH	0	0	0	0	0	0	0	0
Port 6 interrupt/pending register	P6INTPND	238	EEH	0	0	0	0	0	0	0	0
Port 0 control register	P0CON	239	EFH	0	0	0	0	0	0	0	0
Port 1 control register (high byte)	P1CONH	240	F0H	0	0	0	0	0	0	0	0
Port 1 control register (low byte)	P1CONL	241	F1H	0	0	0	0	0	0	0	0
Port 2 control register (high byte)	P2CONH	242	F2H	0	0	0	0	0	0	0	0
Port 2 control register (low byte)	P2CONL	243	F3H	0	0	0	0	0	0	0	0
Port 3 control register (high byte)	P3CONH	244	F4H	0	0	0	0	0	0	0	0
Port 3 control register (low byte)	P3CONL	245	F5H	0	0	0	0	0	0	0	0
Port 4 control register (high byte)	P4CONH	246	F6H	0	0	0	0	0	0	0	0
Port 4 control register (low byte)	P4CONL	247	F7H	0	0	0	0	0	0	0	0
Port 5 control register (high byte)	P5CONH	248	F8H	0	0	0	0	0	0	0	0
Port 5 control register (low byte)	P5CONL	249	F9H	0	0	0	0	0	0	0	0
Port 4 interrupt control register	P4INT	250	FAH	0	0	0	0	0	0	0	0
Port 4 interrupt/pending register	P4INTPND	251	FBH	0	0	0	0	0	0	0	0
Location FCH is factory use only											
Basic timer data register	BTCNT	253	FDH	0	0	0	0	0	0	0	0
Location FEH is not mapped											
Interrupt priority register	IPR	255	FFH	x	x	x	x	x	x	x	x

Table 8-3. S3F84NB Set 1, Bank 1 Register values after RESET

Register Name	Mnemonic	Address		Bit values after Reset							
		Dec	Hex	7	6	5	4	3	2	1	0
SIO data register	SIODATA	224	E0H	0	0	0	0	0	0	0	0
SIO Control register	SIOCON	225	E1H	0	0	0	0	0	0	0	0
UART0 data register	UDATA0	226	E2H	1	1	1	1	1	1	1	1
UART0 control register	UARTCON0	227	E3H	0	0	0	0	0	0	0	0
UART0 baud rate data register (high)	BRDATAH0	228	E4H	1	1	1	1	1	1	1	1
UART0 baud rate data register (low)	BRDATAL0	229	E5H	1	1	1	1	1	1	1	1
Timer 1(0) data register (high byte)	T1DATAH0	230	E6H	1	1	1	1	1	1	1	1
Timer 1(0) data register (low byte)	T1DATAL0	231	E7H	1	1	1	1	1	1	1	1
Timer 1(1) data register (high byte)	T1DATAH1	232	E8H	1	1	1	1	1	1	1	1
Timer 1(1) data register (low byte)	T1DATAL1	233	E9H	1	1	1	1	1	1	1	1
Timer 1(0) control register	T1CON0	234	EAH	0	0	0	0	0	0	0	0
Timer 1(1) control register	T1CON1	235	EBH	0	0	0	0	0	0	0	0
Timer 1(0) counter register(high byte)	T1CNTH0	236	ECH	0	0	0	0	0	0	0	0
Timer 1(0) counter register(low byte)	T1CNTL0	237	EDH	0	0	0	0	0	0	0	0
Timer 1(1) counter register(high byte)	T1CNTH1	238	EEH	0	0	0	0	0	0	0	0
Timer 1(1) counter register(low byte)	T1CNTL1	239	EFH	0	0	0	0	0	0	0	0
Timer C(0) data register	TCDATA0	240	F0H	1	1	1	1	1	1	1	1
Timer C(1) data register	TCDATA1	241	F1H	1	1	1	1	1	1	1	1
Timer C(0) control register	TCCON0	242	F2H	0	0	0	0	0	0	0	0
Timer C(1) control register	TCCON1	243	F3H	0	0	0	0	0	0	0	0
SIO prescaler control register	SIOPS	244	F4H	0	0	0	0	0	0	0	0
Watch timer control register	WTCON	245	F5H	0	0	0	0	0	0	0	0
Oscillator control register	OSCCON	246	F6H	–	–	–	0	0	0	–	0
A/D converter control register	ADCON	247	F7H	0	0	0	0	0	0	0	0
A/D converter data register(high byte)	ADDATAH	248	F8H	0	0	0	0	0	0	0	0
A/D converter data register(low byte)	ADDATAL	249	F9H	0	0	0	0	0	0	0	0
UART1 data register	UDATA1	250	FAH	1	1	1	1	1	1	1	1
UART1 control register	UARTCON1	251	FBH	0	0	0	0	0	0	0	0
UART pending register	UARTPND	229	FCH	0	0	0	0	0	0	0	0
STOP control register	STPCON	253	FDH	0	0	0	0	0	0	0	0
Pattern generation control register	PGCON	254	FEH	–	–	–	–	0	0	0	0
Pattern generation data register	PGDATA	255	FFH	0	0	0	0	0	0	0	0

Table 8-4. S3F84NB Page8 Register Values After RESET

Register Name	Mnemonic	Address		Bit Values After Reset							
		Dec	Hex	7	6	5	4	3	2	1	0
UART1 baud rate data register	BRDATAH1	0	00H	1	1	1	1	1	1	1	1
UART1 baud rate data register	BRDATAL1	1	01H	1	1	1	1	1	1	1	1
Flash memory sector address register (High byte)	FMSECH	2	02H	0	0	0	0	0	0	0	0
Flash memory sector address register (Low byte)	FMSECL	3	03H	0	0	0	0	0	0	0	0
Flash memory user programming enable register	FMUSR	4	04H	0	0	0	0	0	0	0	0
Flash memory control register	FMCON	5	05H	0	0	0	0	0	0	0	0

POWER-DOWN MODES

STOP MODE

Stop mode is invoked by the instruction STOP (opcode 7FH). In Stop mode, the operation of the CPU and all peripherals is halted. That is, the on-chip main oscillator stops and the supply current is reduced to less than 3 µA except for the current consumption of LVR (Low voltage Reset) circuit. All system functions stop when the clock "freezes," but data stored in the internal register file is retained. Stop mode can be released in one of two ways: by a reset or by interrupts.

NOTE

Do not use stop mode if you are using an external clock source because X_{IN} input must be restricted internally to V_{SS} to reduce current leakage.

Using RESET to Release Stop Mode

Stop mode is released when the RESET signal is released and returns to high level: all system and peripheral control registers are reset to their default hardware values and the contents of all data registers are retained. A reset operation automatically selects a slow clock (1/16) because CLKCON.3 and CLKCON.4 are cleared to '00B'. After the programmed oscillation stabilization interval has elapsed, the CPU starts the system initialization routine by fetching the program instruction stored in ROM location 0100H (and 0101H).

Using an External Interrupt to Release Stop Mode

External interrupts with an RC-delay noise filter circuit can be used to release Stop mode. Which interrupt you can use to release Stop mode in a given situation depends on the microcontroller's current internal operating mode. The external interrupts in the S3F84NB interrupt structure that can be used to release Stop mode are:

- External interrupts P4.0–P4.7 (INT0–INT7) and P6.2–P6.7 (INT8–INT13)

Please note the following conditions for Stop mode release:

- If you release Stop mode using an external interrupt, the current values in system and peripheral control registers are unchanged.
- If you use an external interrupt for Stop mode release, you can also program the duration of the oscillation stabilization interval. To do this, you must make the appropriate control and clock settings *before* entering Stop mode.
- When the Stop mode is released by external interrupt, the CLKCON.4 and CLKCON.3 bit-pair setting remains unchanged and the currently selected clock value is used.
- The external interrupt is serviced when the Stop mode release occurs. Following the IRET from the service routine, the instruction immediately following the one that initiated Stop mode is executed.

Using an internal Interrupt to Release Stop Mode

Activate any enabled interrupt, causing stop mode to be released. Other things are same as using external interrupt.

How to Enter into Stop Mode

There are two ways to enter into Stop mode:

1. Handling OSCCON register.
2. Handling STPCON register then writing Stop instruction (keep the order).

IDLE MODE

Idle mode is invoked by the instruction IDLE (opcode 6FH). In idle mode, CPU operations are halted while some peripherals remain active. During idle mode, the internal clock signal is gated away from the CPU, but all peripherals timers remain active. Port pins retain the mode (input or output) they had at the time idle mode was entered.

There are two ways to release idle mode:

1. Execute a reset. All system and peripheral control registers are reset to their default values and the contents of all data registers are retained. The reset automatically selects the slow clock fxx/16 because CLKCON.4 and CLKCON.3 are cleared to '00B'. If interrupts are masked, a reset is the only way to release idle mode.
2. Activate any enabled interrupt, causing idle mode to be released. When you use an interrupt to release idle mode, the CLKCON.4 and CLKCON.3 register values remain unchanged, and the currently selected clock value is used. The interrupt is then serviced. When the return-from-interrupt (IRET) occurs, the instruction immediately following the one that initiated idle mode is executed.

9 I/O PORTS

OVERVIEW

The S3F84NB microcontroller has seven bit-programmable I/O ports, P0-P6. This gives a total of 56 I/O pins. Each port can be flexibly configured to meet application design requirements. The CPU accesses ports by directly writing or reading port registers. No special I/O instructions are required.

Table 9-1 gives you a general overview of the S3F84NB I/O port functions.

Table 9-1. S3F84NB Port Configuration Overview

Port	Configuration Options
0	Bit programmable port; input or output mode selected by software; input or push-pull output. Software assignable pull-up. Alternately, P0.0–P0.7 can be used as the PG output port (PG0–PG7).
1	Bit programmable port; input or output mode selected by software; input or push-pull output. Software assignable pull-up. Alternatively used as analog input pins for A/D converter modules.
2	Bit programmable port; input or output mode selected by software; input or push-pull output. Software assignable pull-up. Alternately, P2.0–P2.7 can be used as I/O for TIMERA, TIMERB, BZOUT, SIO
3	Bit programmable port; input or output mode selected by software; input or push-pull output. Software assignable pull-up. Alternately, P3.0–P3.7 can be used as I/O for TIMER C(0),TIMER C(1), TIMER 1(0), TIMER 1(1)
4	Bit programmable port; input or output mode selected by software; input or push-pull output. Software assignable pull-up. P4.0–P4.7 can alternately be used as inputs for external interrupts INT0–INT7, respectively (with noise filters and interrupt controller)
5	Bit programmable port; input or output mode selected by software; input or push-pull output. Software assignable pull-up. Alternately, P5.0–P5.3 can be used as I/O for serial port, UART0, UART1, respectively.
6	Bit programmable port; input or output mode selected by software; input or push-pull output. Software assignable pull-up. P6.0–P6.1 can alternately be used as Subsystem oscillator XT_{IN}, XT_{OUT} pins and P6.2–P6.7 can alternately be used as inputs for external interrupts INT8–INT13, respectively (with noise filters and interrupt controller).

PORT DATA REGISTERS

Table 9-2 gives you an overview of the register locations of all seven S3F84NB I/O port data registers. Data registers for ports 0, 1, 2, 3, 4, 5 and 6 have the general format shown in Table 9-2.

Table 9-2. Port Data Register Summary

Register Name	Mnemonic	Decimal	Hex	Location	R/W
Port 0 data register	P0	224	E0H	Set 1, Bank 0	R/W
Port 1 data register	P1	225	E1H	Set 1, Bank 0	R/W
Port 2 data register	P2	226	E2H	Set 1, Bank 0	R/W
Port 3 data register	P3	227	E3H	Set 1, Bank 0	R/W
Port 4 data register	P4	228	E4H	Set 1, Bank 0	R/W
Port 5 data register	P5	229	E5H	Set 1, Bank 0	R/W
Port 6 data register	P6	230	E6H	Set 1, Bank 0	R/W

PORT 0

Port 0 is an 8-bit I/O port that you can use two ways:

- General-purpose digital I/O
- Alternative function: PGOUT7–PGOUT0

Port 0 is accessed directly by writing or reading the port 0 data register, P0 at location E0H in set 1, bank 0.

Port 0 Control Register (P0CON)

Port 0 pins are configured individually by bit-pair settings in the control register located in set 1, bank 0: P0CON (EFH). A reset clears the P0CON registers to “00H”, configuring all pins to input modes.

When programming the port, please remember that any alternative peripheral I/O function you configure using the port 0 control registers must also be enabled in the associated peripheral module.

Port 0 Control Register (P0CON)
EFH, Set 1, Bank 0, R/W

MSB	.7	.6	.5	.4	.3	.2	.1	.0	LSB
	P0.7-P0.4 PGOUT[7:4]		P0.3/P0.2 PGOUT[3:2]		P0.1 PGOUT[1]		P0.0 PGOUT[0]		

.7 .6 bit : P0.7/P0.6/P0.5/P0.4

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Alternative function mode(PGOUT[7:4])

.5 .4 bit : P0.3/P0.2

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Alternative function mode(PGOUT[3:2])

.3 .2 bit : P0.1

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Alternative function mode(PGOUT[1])

.1 .0 bit : P0.0

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Alternative function mode(PGOUT[0])

Figure 9-1. Port 0 Control Register (P0CON)

PORT 1

Port 1 is an 8-bit I/O port with individually configurable pins that you can use two ways:

- General-purpose digital I/O
- Alternative function: ADC0–ADC7

Port 1 is accessed directly by writing or reading the port 1 data register, P1 at location E1H in set 1, bank 0.

Port 1 Control Register (P1CONH, P1CONL)

Port 1 has two 8-bit control registers: P1CONH for P1.4–P1.7 and P1CONL for P1.0–P1.3. A reset clears the P1CONH and P1CONL registers to “00H”, configuring all pins to input modes. You use control registers settings to select input or output mode (push-pull) and enable the alternative functions.

When programming the port, please remember that any alternative peripheral I/O function you configure using the port 1 control registers must also be enabled in the associated peripheral module.

Port 1 Control Register, High Byte (P1CONH)
F0H, Set 1, Bank 0, R/W

MSB	.7	.6	.5	.4	.3	.2	.1	.0	LSB

P1.7/ADC7
P1.6/ADC6
P1.5/ADC5
P1.4/ADC4

.7 .6 bit : P1.7/ADC7

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Alternative function(ADC7)

.5 .4 bit : P1.6/ADC6

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Alternative function(ADC6)

.3 .2 bit : P1.5/ADC5

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Alternative function(ADC5)

.1 .0 bit : P1.4/ADC4

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Alternative function(ADC4)

NOTE: When use this port 1, user must be care of the pull-up resistance status.

Figure 9-2. Port 1 High-Byte Control Register (P1CONH)

Port 1 Control Register, Low Byte (P1CONL)
F1H, Set 1, Bank 0, R/W

MSB	.7	.6	.5	.4	.3	.2	.1	.0	LSB

P1.3/ADC3 P1.2/ADC2 P1.1/ADC1 P1.0/ADC0

.7 .6 bit : P1.3/ADC3

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Alternative function(ADC3)

.5 .4 bit : P1.2/ADC2

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Alternative function(ADC2)

.3 .2 bit : P1.1/ADC1

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Alternative function(ADC1)

.1 .0 bit : P1.0/ADC0

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Alternative function(ADC0)

NOTE: When use this port 1, user must be care of the pull-up resistance status.

Figure 9-3. Port 1 Low-Byte Control Register (P1CONL)

PORT 2

Port 2 is an 8-bit I/O port with individually configurable pins. Port 2 pins are accessed directly by writing or reading the port 2 data register, P2 at location E2H in set 1, bank 0. P2.0–P2.7 can serve as digital inputs, outputs (push pull) or you can configure the following alternative functions:

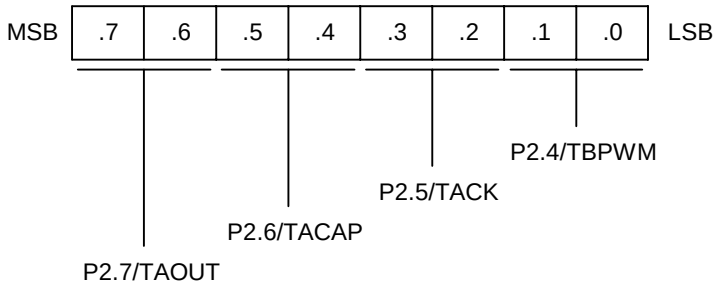
- Low-byte pins (P2.0–P2.3): BZOUT, SCK, SI, SO
- High-byte pins (P2.4–P2.7): TAOUT, TACAP, TACK, TBPWM

Port 2 Control Register (P2CONH, P2CONL)

Port 2 has two 8-bit control registers: P2CONH for P2.4–P2.7 and P2CONL for P2.0–P2.3. A reset clears the P2CONH and P2CONL registers to “00H”, configuring all pins to input mode. You use control registers settings to select input or output mode (push-pull) and enable the alternative functions.

When programming the port, please remember that any alternative peripheral I/O function you configure using the port 2 control registers must also be enabled in the associated peripheral module.

Port 2 Control Register, High Byte (P2CONH)
F2H, Set 1, Bank 0, R/W



.7 .6 bit : P2.7/TAOUT

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Alternative function(TAOUT)

.5 .4 bit : P2.6/TACAP

00	Input mode(TACAP)
01	Input mode, pull-up(TACAP)
10	Push-pull output
11	Alternative function (Not used)

.3 .2 bit : P2.5/TACK

00	Input mode(TACK)
01	Input mode, pull-up(TACK)
10	Push-pull output
11	Alternative function (Not used)

.1 .0 bit : P2.4/TBPWM

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Alternative function(TBPWM)

NOTE: When use this port 2, user must be care of the pull-up resistance status.

Figure 9-4. Port 2 High-Byte Control Register (P2CONH)

Port 2 Control Register, Low Byte (P2CONL)
F3H, Set 1, Bank 0, R/W

MSB	.7	.6	.5	.4	.3	.2	.1	.0	LSB

P2.3/BUZOUT
P2.2/SCK
P2.1/SI
P2.0/SO

.7 .6 bit : P2.3/BZOUT

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Alternative output mode(BZOUT)

.5 .4 bit : P2.2/SCK

00	Input mode(SCK input)
01	Input mode, pull-up(SCK input)
10	Push-pull output
11	Alternative output mode(SCK output)

.3 .2 bit : P2.1/SI

00	Input mode(SI)
01	Input mode, pull-up(SI)
10	Push-pull output
11	Alternative output mode (Not used)

.1 .0 bit : P2.0/SO

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Alternative output mode(SO)

NOTE: When use this port 2, user must be care of the pull-up resistance status.

Figure 9-5. Port 2 Low-Byte Control Register (P2CONL)

PORT 3

Port 3 is an 8-bit I/O port that can be used for general-purpose digital I/O. The pins are accessed directly by writing or reading the port 3 data register, P3 at location E3H in set 1, bank 0. P3.7–P3.0 can serve as inputs, outputs
(push pull) or you can configure the following alternative functions:

- Low-byte pins (P3.0–P3.3): T1CAP1, T1CAP0, T1CK1, T1CK0
- High-byte pins (P3.4–P3.7): TCOUT1, TCOUT0, T1OUT1, T1OUT0

To individually configure the port 3 pins P3.0–P3.7, you make bit-pair settings in two control registers located in set 1, bank 0: P3CONL (low byte, F5H) and P3CONH (high byte, F4H).

Port 3 Control Registers (P3CONH, P3CONL)

Two 8-bit control registers are used to configure port 3 pins: P3CONL (F5H, set 1, Bank 0) for pins P3.0–P3.3 and P3CONH (F4H, set 1, Bank 0) for pins P3.4–P3.7. Each byte contains four bit-pairs and each bit-pair configures one pin of port 3.

Port 3 Control Register, High Byte (P3CONH)
F4H, Set 1, Bank 0, R/W

MSB	.7	.6	.5	.4	.3	.2	.1	.0	LSB

P3.7/TCOUT1
P3.6/TCOUT0
P3.5/T1OUT1
P3.4/T1OUT0

.7 .6 bit : P3.7/TCOUT1

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Alternative function(TCOUT1)

.5 .4 bit : P3.6/TCOUT0

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Alternative function(TCOUT0)

.3 .2 bit : P3.5/T1OUT1

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Alternative function(T1OUT1)

.1 .0 bit : P3.4/T1OUT0

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Alternative function(T1OUT0)

Figure 9-6. Port 3 High-Byte Control Register (P3CONH)

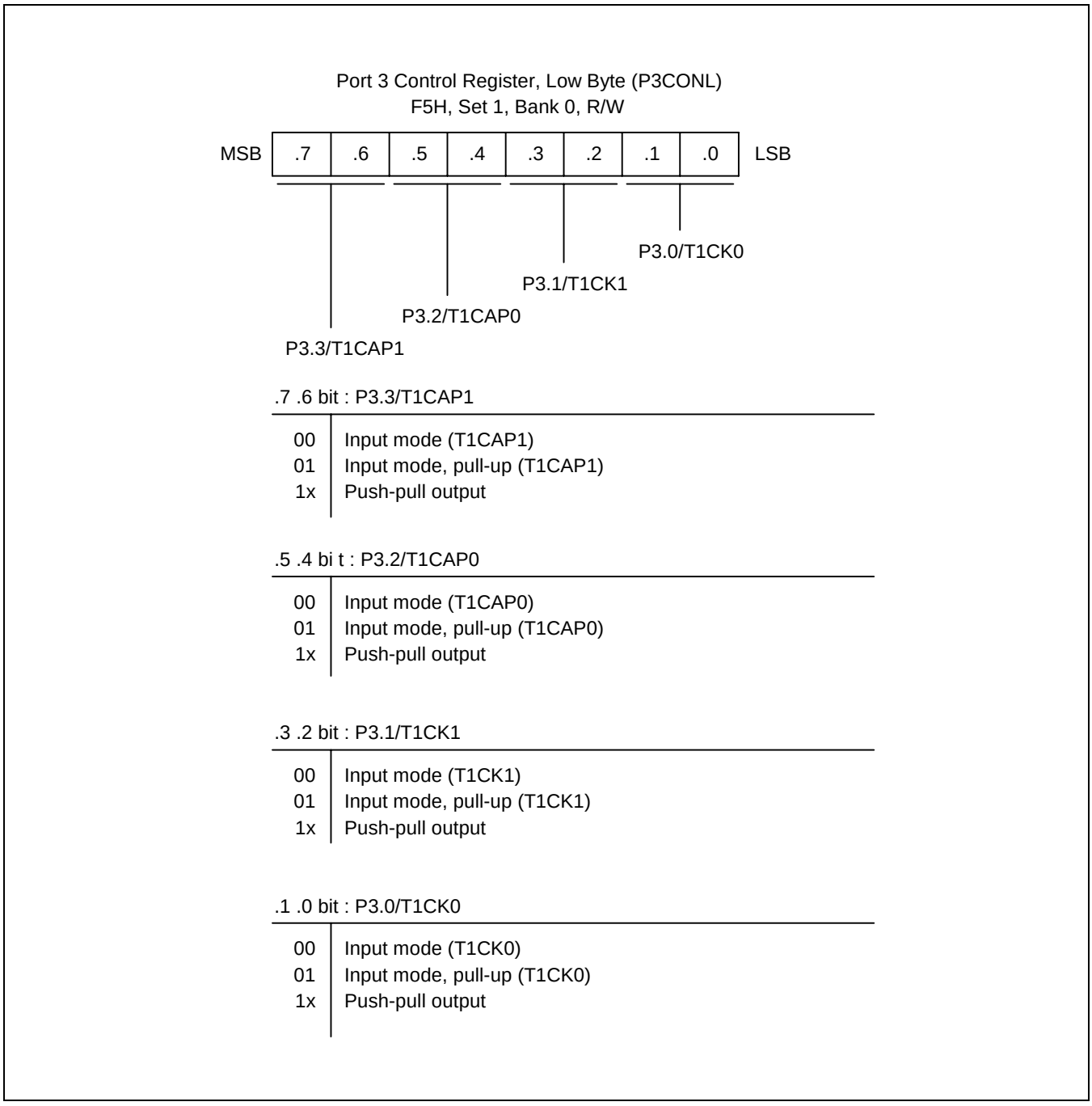


Figure 9-7. Port 3 Low-Byte Control Register (P3CONL)

PORT 4

Port 4 is an 8-bit I/O port that you can use two ways:

- General-purpose digital I/O
- External interrupt inputs for INT0–INT7

Port 4 is accessed directly by writing or reading the port 4 data register, P4 at location E4H in set 1, bank 0.

Port 4 Control Register (P4CONH, P4CONL)

Port 4 pins are configured individually by bit-pair settings in two control registers located in set 1, bank 0: P4CONL (low byte, F7H) and P4CONH (high byte, F6H).

When you select output mode, a push-pull circuit is configured. In input mode, three different selections are available:

- Schmitt trigger input and interrupt generation on falling signal edges.
- Schmitt trigger input and interrupt generation on rising signal edges.
- Schmitt trigger input with pull up resister and interrupt generation on falling signal edges.

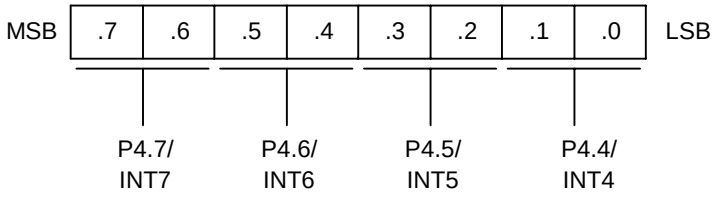
Port 4 Interrupt Enable and Pending Registers (P4INT, P4INTPND)

To process external interrupts at the port 4 pins, two additional control registers are provided: the port 4 interrupt enable register P4INT (FAH, set 1, bank 0) and the port 4 interrupt pending register P4INTPND (FBH, set 1, bank 0).

The port 4 interrupt pending register P4INTPND lets you check for interrupt pending conditions and clear the pending condition when the interrupt service routine has been initiated. The application program detects interrupt requests by polling the P4INTPND register at regular intervals.

When the interrupt enable bit of any port 4 pin is “1”, a rising or falling signal edge at that pin will generate an interrupt request. The corresponding P4INTPND bit is then automatically set to “1” and the IRQ level goes low to signal the CPU that an interrupt request is waiting. When the CPU acknowledges the interrupt request, application software must clear the pending condition by writing a “0” to the corresponding P4INTPND bit.

Port 4 Control Register, High Byte (P4CONH)
F6H, Set 1, Bank 0, R/W



.7 .6 bit : P4.7/INT7

00	Input mode; (falling edge interrupt)
01	Input mode; (rising edge interrupt)
10	Input mode, pull-up; (falling edge interrupt)
11	Push-pull output

.5 .4 bit : P4.6/INT6

00	Input mode; (falling edge interrupt)
01	Input mode; (rising edge interrupt)
10	Input mode, pull-up; (falling edge interrupt)
11	Push-pull output

.3 .2 bit : P4.5/INT5

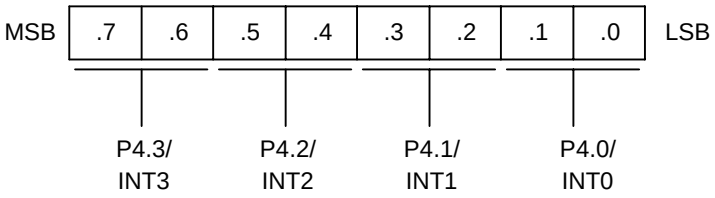
00	Input mode; (falling edge interrupt)
01	Input mode; (rising edge interrupt)
10	Input mode, pull-up; (falling edge interrupt)
11	Push-pull output

.1 .0 bit : P4.4/INT4

00	Input mode; (falling edge interrupt)
01	Input mode; (rising edge interrupt)
10	Input mode, pull-up; (falling edge interrupt)
11	Push-pull output

Figure 9-8. Port 4 High-Byte Control Register (P4CONH)

Port 4 Control Register, Low Byte (P4CONL)
F7H, Set 1, Bank 0, R/W



.7 .6 bit : P4.3/INT3

00	Input mode; (falling edge interrupt)
01	Input mode; (rising edge interrupt)
10	Input mode, pull-up; (falling edge interrupt)
11	Push-pull output

.5 .4 bit : P4.2/INT2

00	Input mode; (falling edge interrupt)
01	Input mode; (rising edge interrupt)
10	Input mode, pull-up; (falling edge interrupt)
11	Push-pull output

.3 .2 bit : P4.1/INT1

00	Input mode; (falling edge interrupt)
01	Input mode; (rising edge interrupt)
10	Input mode, pull-up; (falling edge interrupt)
11	Push-pull output

.1 .0 bit : P4.0/INT0

00	Input mode; (falling edge interrupt)
01	Input mode; (rising edge interrupt)
10	Input mode, pull-up; (falling edge interrupt)
11	Push-pull output

Figure 9-9. Port 4 Low-Byte Control Register (P4CONL)

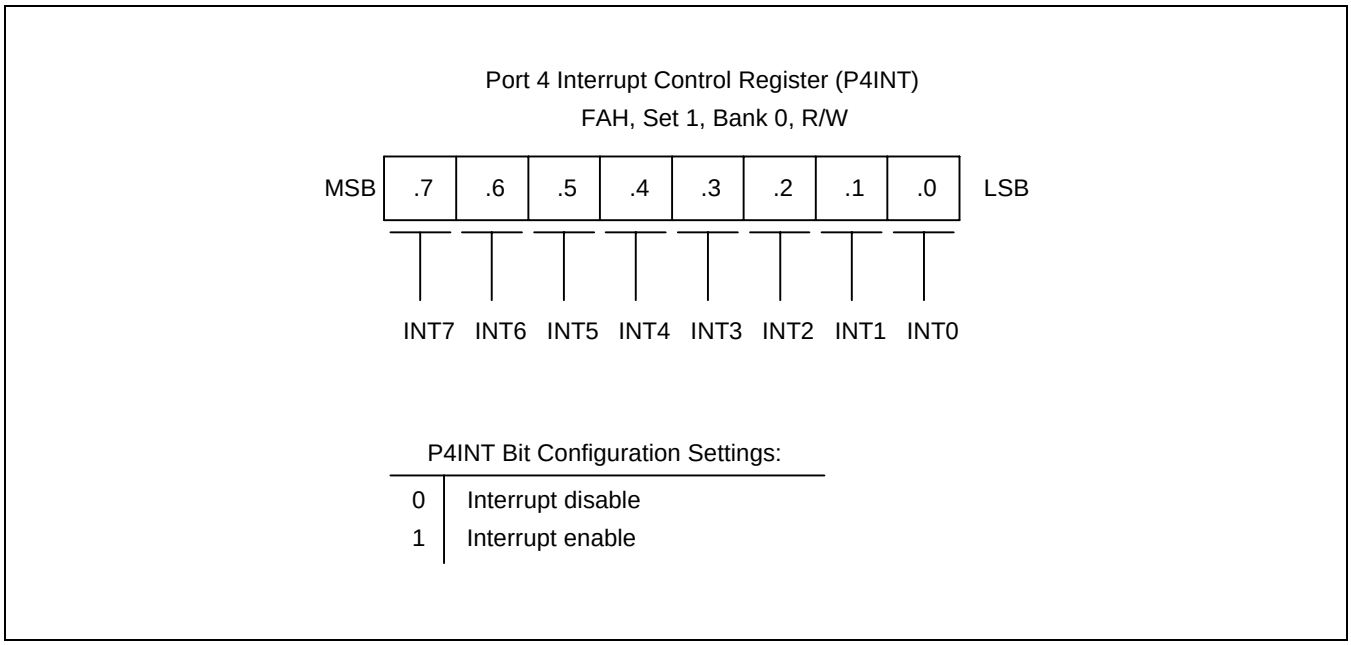


Figure 9-10. Port 4 Interrupt Control Register (P4INT)

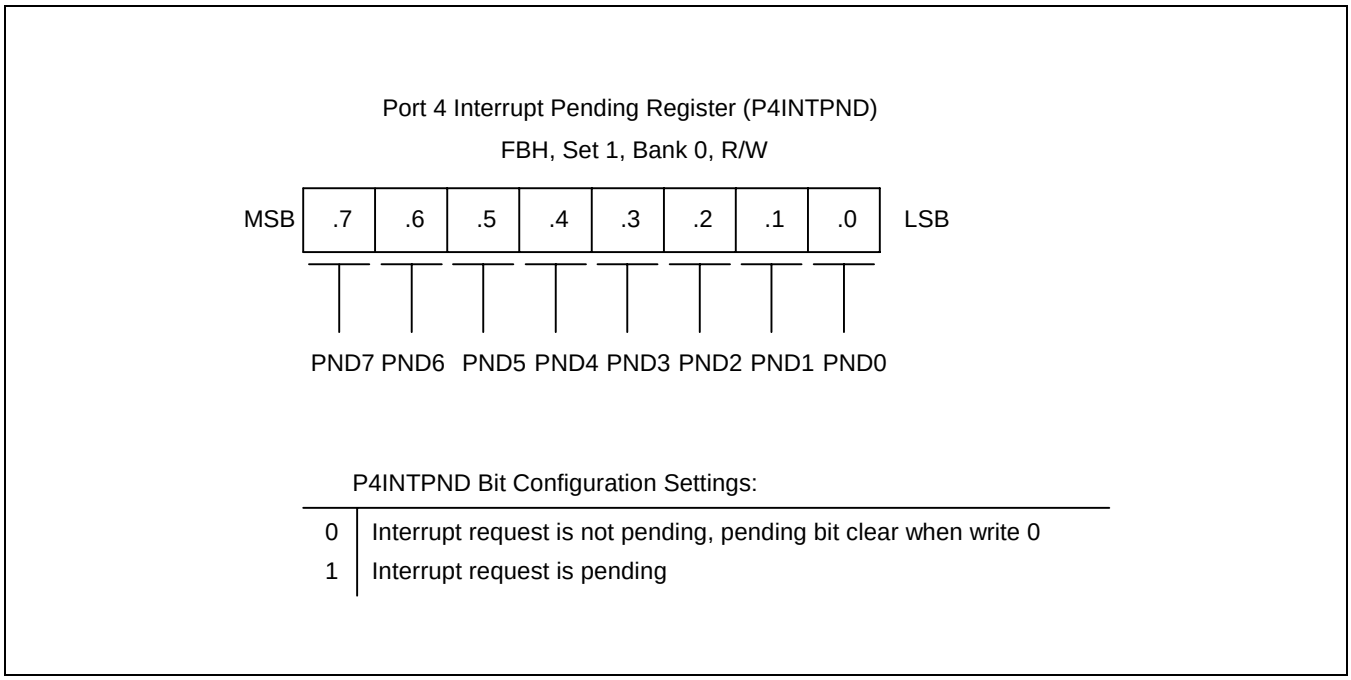


Figure 9-11. Port 4 Interrupt Pending Register (P4INTPND)

PORT 5

Port 5 is an 8-bit digital I/O port with individually configurable pins. Port 5 pins are accessed directly by writing or reading the port 5 data register, P5 at location E5H in set 1, bank 0. P5.7–P5.4 can serve as inputs, outputs (push pull, open-drain). P5.3–P5.0 can serve as inputs, outputs (push pull) or you can configure the following alternative functions:

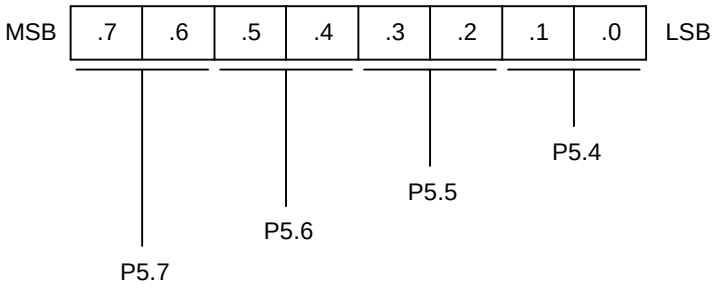
- Low-byte pins (P5.3–P5.0): RxD0, TxD0, RxD1, TxD1

Port 5 Control Register (P5CONH, P5CONL)

Port 5 has two 8-bit control registers: P5CONH for P5.4–P5.7 and P5CONL for P5.0–P5.3. A reset clears the P5CONH and P5CONL registers to “00H”, configuring all pins to input mode. You use control registers settings to select input or output mode (push-pull, open-drain) and enable the alternative functions.

When programming the port, please remember that any alternative peripheral I/O function you configure using the port 5 control registers must also be enabled in the associated peripheral module.

Port 5 Control Register, High Byte (P5CONH)
F8H, Set 1, Bank 0, R/W



.7 .6 bit : P5.7

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Open-drain output mode

.5 .4 bit : P5.6

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Open-drain ouput mode

.3 .2 bit : P5.5

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Open-drain output mode

.1 .0 bit : P5.4

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Open-drain output mode

Figure 9-12. Port 5 High-Byte Control Register (P5CONH)

Port 5 Control Register, Low Byte (P5CONL)
F9H, Set 1, Bank 0, R/W

MSB	.7	.6	.5	.4	.3	.2	.1	.0	LSB

P5.3/ RxD0 — P5.2/ TxD0 — P5.1/ RxD1 — P5.0/ TxD1

.7 .6 bit : P5.3/RxD0

00	Input mode(RxD0 input)
01	Input mode, pull-up(RxD0 input)
10	Push-pull output
11	Alternative output mode(RxD0 output)

.5 .4 bit : P5.2/TxD0

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Alternative output mode(TxD0 output)

.3 .2 bit : P5.1/RxD1

00	Input mode(RxD1 input)
01	Input mode, pull-up(RxD1 input)
10	Push-pull output
11	Alternative output mode(RxD1 output)

.1 .0 bit : P5.0/TxD1

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Alternative output mode(TxD1 output)

Figure 9-13. Port 5 Low-Byte Control Register (P5CONL)

PORT 6

Port 6 is an 8-bit digital I/O port that you can use three ways:

- General-purpose digital I/O
- External interrupt inputs for INT8–INT13
- Subsystem oscillator input (XT_{IN}), output (XT_{OUT}) pins

Port 6 is accessed directly by writing or reading the port 6 data register, P6 at location E6H in set 1, bank 0.

Port 6 Control Register (P6CONH, P6CONL)

Port 6 pins are configured individually by bit-pair settings in two control registers located in set 1, bank 0: P6CONL (low byte, E9H) and P6CONH (high byte, E8H).

When you select output mode, a push-pull circuit is configured. In input mode, three different selections are available for P6.2–P6.7:

- Schmitt trigger input and interrupt generation on falling signal edges.
- Schmitt trigger input and interrupt generation on rising signal edges.
- Schmitt trigger input with pull up resister and interrupt generation on falling signal edges.

Port 6 Interrupt Enable and Pending Registers (P6INT, P6INTPND)

To process external interrupts at the port 6 pins, two additional control registers are provided: the port 6 interrupt enable register P6INT (EDH, set 1, bank 0) and the port 6 interrupt pending register P6INTPND (EEH, set 1, bank 0).

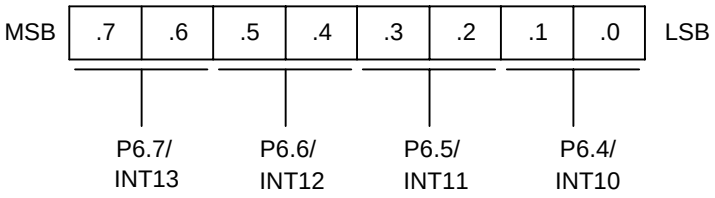
The port 6 interrupt pending register P6INTPND lets you check for interrupt pending conditions and clear the pending condition when the interrupt service routine has been initiated. The application program detects interrupt requests by polling the P6INTPND register at regular intervals.

When the interrupt enable bit of any port 6 pin is “1”, a rising or falling signal edge at that pin will generate an interrupt request. The corresponding P6INTPND bit is then automatically set to “1” and the IRQ level goes low to signal the CPU that an interrupt request is waiting. When the CPU acknowledges the interrupt request, application software must clear the pending condition by writing a “0” to the corresponding P6INTPND bit.

Subsystem Oscillator Input (XTin), Output (XTout)

The reset value of P6CONL register is “0FH” so that P6.0 and P6.1 pins are set to the subsystem oscillation mode after CPU Reset. This allows fast oscillation starting. If you don’t use subsystem oscillation mode in your applications, it is recommended to set these pins as Push-up output mode for protecting current leakage.

Port 6 Control Register, High Byte (P6CONH)
E8H, Set 1, Bank 0, R/W



.7 .6 bit : P6.7/INT13

00	Input mode; (falling edge interrupt)
01	Input mode; (rising edge interrupt)
10	Input mode, pull-up; (falling edge interrupt)
11	Push-pull output

.5 .4 bit : P6.6/INT12

00	Input mode; (falling edge interrupt)
01	Input mode; (rising edge interrupt)
10	Input mode, pull-up; (falling edge interrupt)
11	Push-pull output

.3 .2 bit : P6.5/INT11

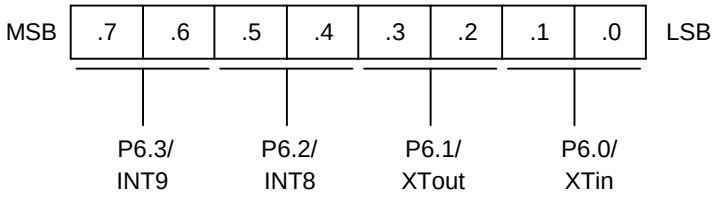
00	Input mode; (falling edge interrupt)
01	Input mode; (rising edge interrupt)
10	Input mode, pull-up; (falling edge interrupt)
11	Push-pull output

.1 .0 bit : P6.4/INT10

00	Input mode; (falling edge interrupt)
01	Input mode; (rising edge interrupt)
10	Input mode, pull-up; (falling edge interrupt)
11	Push-pull output

Figure 9-14. Port 6 High-Byte Control Register (P6CONH)

Port 6 Control Register, Low Byte (P6CONL)
E9H , Set 1, Bank 0, R/W



.7 .6 bit : P6.3/INT9

00	Input mode; (falling edge interrupt)
01	Input mode; (rising edge interrupt)
10	Input mode, pull-up; (falling edge interrupt)
11	Push-pull output

.5 .4 bit : P6.2/INT8

00	Input mode; (falling edge interrupt)
01	Input mode; (rising edge interrupt)
10	Input mode, pull-up; (falling edge interrupt)
11	Push-pull output

.3 .2 bit : P6.1/XTout

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Alternative function (Sub-Clock Oscillator Output, XTout)

.1 .0 bit : P6.0/XTin

00	Input mode
01	Input mode, pull-up
10	Push-pull output
11	Alternative function (Sub-Clock Oscillator Input, XTin)

Figure 9-15. Port 6 Low-Byte Control Register (P6CONL)

Port 6 Interrupt Control Register (P6INT)

EDH, Set 1, Bank 0, R/W

MSB	.7	.6	.5	.4	.3	.2	.1	.0	LSB
	INT13	INT12	INT11	INT10	INT9	INT8	Not used (must keep always 0)		

P6INT Bit Configuration Settings:

0	Interrupt disable
1	Interrupt enable

Figure 9-16. Port 6 Interrupt Control Register (P6INT)

Port 6 Interrupt Pending Register (P6INTPND)

EEH, Set 1, Bank 0, R/W

MSB	.7	.6	.5	.4	.3	.2	.1	.0	LSB
	PND13	PND12	PND11	PND10	PND9	PND8	Not used (must keep always 0)		

P6INTPND Bit Configuration Settings:

0	Interrupt request is not pending, pending bit clear when write 0
1	Interrupt request is pending

Figure 9-17. Port 6 Interrupt Pending Register (P6INTPND)

10 BASIC TIMER

OVERVIEW

BASIC TIMER (BT)

You can use the basic timer (BT) in two different ways:

- As a watchdog timer to provide an automatic reset mechanism in the event of a system malfunction.
- To signal the end of the required oscillation stabilization interval after a reset or a Stop mode release.

The functional components of the basic timer block are:

- Clock frequency divider (fxx divided by 4096, 1024, 128 or 16) with multiplexer
- 8-bit basic timer counter, BTCNT (set 1, bank 0, FDH, read-only)
- Basic timer control register, BTCON (set 1, D3H, read/write)

BASIC TIMER CONTROL REGISTER (BTCON)

The basic timer control register, BTCON, is used to select the input clock frequency, to clear the basic timer counter and frequency dividers, and to enable or disable the watchdog timer function. It is located in set 1, address D3H, and is read/write addressable using register addressing mode.

A reset clears BTCON to '00H'. This enables the watchdog function and selects a basic timer clock frequency of $f_{XX}/4096$. To disable the watchdog function, write the signature code '1010B' to the basic timer register control bits BTCON.7–BTCON.4.

The 8-bit basic timer counter, BTCNT (set 1, bank 0, FDH), can be cleared at any time during normal operation by writing a "1" to BTCON.1. To clear the frequency dividers, write a "1" to BTCON.0.

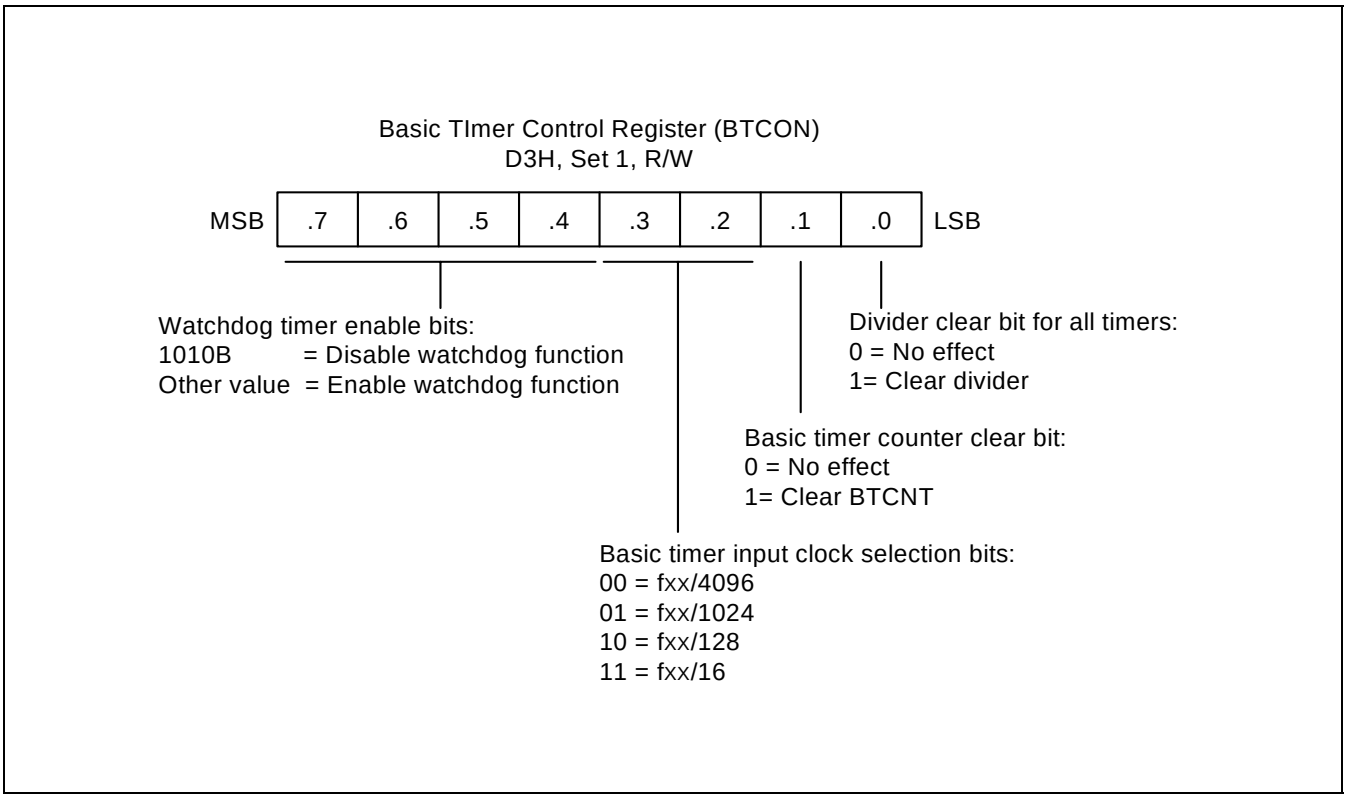


Figure 10-1. Basic Timer Control Register (BTCON)

BASIC TIMER FUNCTION DESCRIPTION

Watchdog Timer Function

You can program the basic timer overflow signal (BTOVF) to generate a reset by setting BTCON.7–BTCON.4 to any value other than "1010B". (The "1010B" value disables the watchdog function.) A reset clears BTCON to "00H", automatically enabling the watchdog timer function. A reset also selects the CPU clock (as determined by the current CLKCON register setting), divided by 4096, as the BT clock.

The CPU is reset whenever a basic timer counter overflow occurs, During normal operation, the application program must prevent the overflow, and the accompanying reset operation, from occurring. To do this, the BTCNT value must be cleared (by writing a “1” to BTCON.1) at regular intervals.

If a system malfunction occurs due to circuit noise or some other error condition, the BT counter clear operation will not be executed and a basic timer overflow will occur, initiating a reset. In other words, during the normal operation, the basic timer overflow loop (a bit 7 overflow of the 8-bit basic timer counter, BTCNT) is always broken by a BTCNT clear instruction. If a malfunction does occur, a reset is triggered automatically.

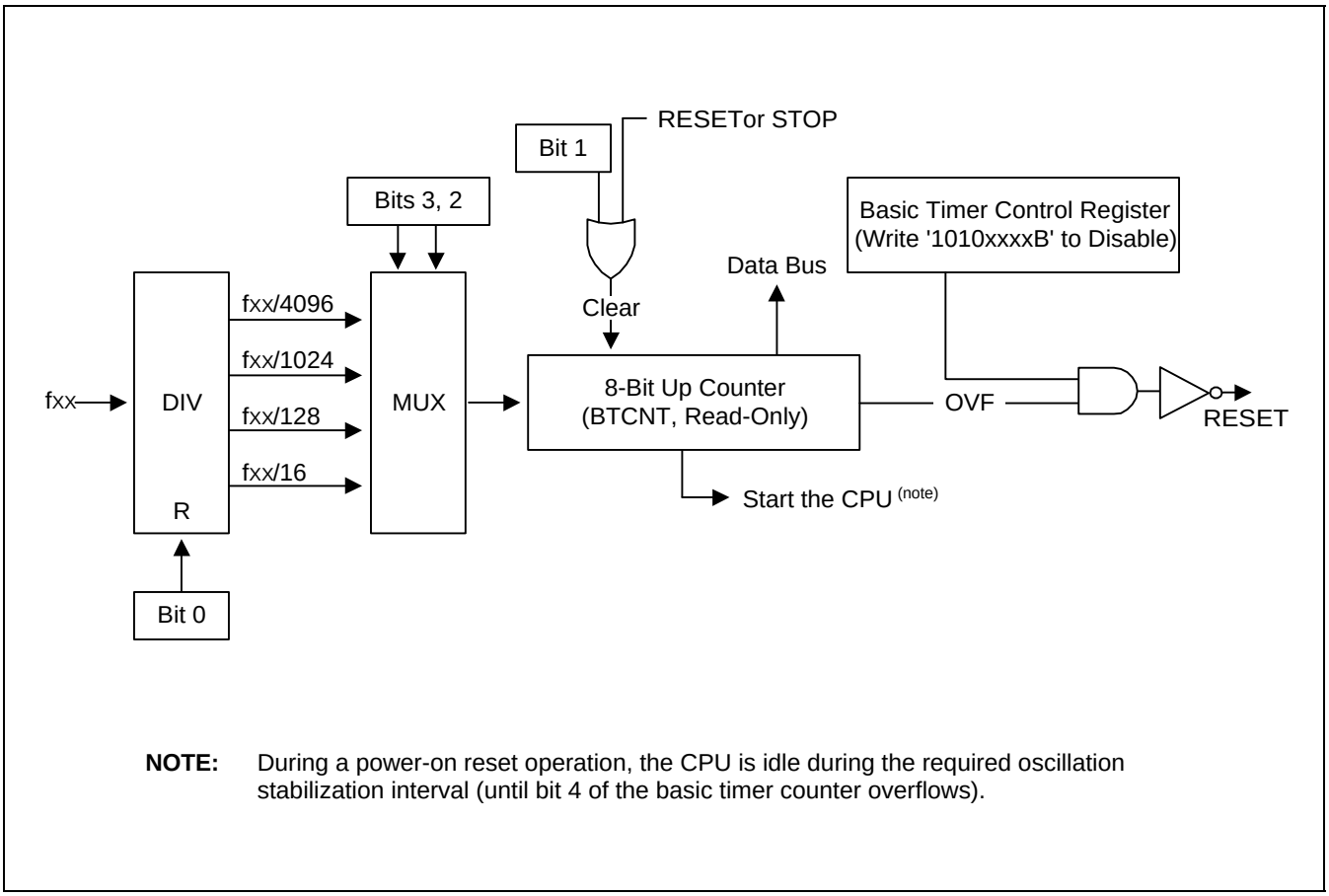
Oscillation Stabilization Interval Timer Function

You can also use the basic timer to program a specific oscillation stabilization interval following a reset or when Stop mode has been released by an external interrupt.

In Stop mode, whenever a reset or an external interrupt occurs, the oscillator starts. The BTCNT value then starts increasing at the rate of fxx/4096 (for reset), or at the rate of the preset clock source (for an external interrupt). When BTCNT.4 overflows, a signal is generated to indicate that the stabilization interval has elapsed and to gate the clock signal off to the CPU so that it can resume normal operation.

In summary, the following events occur when stop mode is released:

1. During stop mode, a power-on reset or an interrupt occurs to trigger the Stop mode release and oscillation starts.
2. If a power-on reset occurred, the basic timer counter will increase at the rate of fxx/4096. If an external interrupt is used to release stop mode, the BTCNT value increases at the rate of the preset clock source.
3. Clock oscillation stabilization interval begins and continues until bit 4 of the basic timer counter overflows.
4. When a BTCNT.4 overflow occurs, normal CPU operation resumes.



NOTE: During a power-on reset operation, the CPU is idle during the required oscillation stabilization interval (until bit 4 of the basic timer counter overflows).

Figure 10-2. Basic Timer Block Diagram

11 8-BIT TIMER A/B/C(0,1)

8-BIT TIMER A

OVERVIEW

The 8-bit timer A is an 8-bit general-purpose timer/counter. Timer A has three operating modes, you can select one of them using the appropriate TACON setting:

- Interval timer mode (Toggle output at TAOUT pin)
- Capture input mode with a rising or falling edge trigger at the TACAP pin
- PWM mode (TAPWM)

Timer A has the following functional components:

- Clock frequency divider (fxx divided by 1024, 256, or 64) with multiplexer
- External clock input pin (TACK)
- 8-bit counter (TACNT), 8-bit comparator, and 8-bit reference data register (TADATA)
- I/O pins for capture input (TACAP) or PWM or match output (TAOUT)
- Timer A overflow interrupt (IRQ1, vector C2H) and match/capture interrupt (IRQ1, vector C0H) generation
- Timer A control register, TACON (set 1, bank0, EAH, read/write)

FUNCTION DESCRIPTION

Timer A Interrupts (IRQ1, Vectors C0H and C2H)

The timer A module can generate two interrupts: the timer A overflow interrupt (TAOVF), and the timer A match/ capture interrupt (TAINT). TAOVF is interrupt level IRQ1, vector C2H. TAINT also belongs to interrupt level IRQ1, but is assigned the separate vector address, C0H.

A timer A overflow interrupt pending condition is automatically cleared by hardware when it has been serviced. A timer A match/capture interrupt, TAINT pending condition is also cleared by hardware when it has been serviced.

Interval Timer Function

The timer A module can generate an interrupt: the timer A match interrupt (TAINT). TAINT belongs to interrupt level IRQ1, and is assigned the separate vector address, C0H.

When the timer A match interrupt occurs and is serviced by the CPU, the pending condition is cleared automatically by hardware.

In interval timer mode, a match signal is generated and TAOUT is toggled when the counter value is identical to the value written to the timer A reference data register, TADATA. The match signal generates a timer A match interrupt (TAINT, vector C0H) and clears the counter.

If, for example, you write the value 10H to TADATA and 0AH to TACON, the counter will increment until it reaches 10H. At this point, the Timer A interrupt request is generated, the counter value is reset, and counting resumes.

Pulse Width Modulation Mode

Pulse width modulation (PWM) mode lets you program the width (duration) of the pulse that is output at the TAOUT pin. As in interval timer mode, a match signal is generated when the counter value is identical to the value written to the Timer A data register, TADATA. In PWM mode, however, the match signal does not clear the counter. Instead, it runs continuously, overflowing at FFH, and then continues incrementing from 00H.

Although you can use the match signal to generate a timer A overflow interrupt, interrupts are not typically used in PWM-type applications. Instead, the pulse at the TAOUT pin is held to Low level as long as the reference data value is *less than or equal to* (≤) the counter value and then the pulse is held to High level for as long as the data value is *greater than* (>) the counter value. One pulse width is equal to t_{CLK} • 256.

Capture Mode

In capture mode, a signal edge that is detected at the TACAP pin opens a gate and loads the current counter value into the Timer A data register. You can select rising or falling edges to trigger this operation.

Timer A also gives you capture-input source: the signal edge at the TACAP pin. You select the capture input by setting the value of the Timer A capture input selection bit in the port 2 control register, P2CONH, (set 1, bank 0, F2H). When P2CONH.5-.4 is 00, the TACAP input or normal input is selected. When P2CONH.5-.4 is set to 10, normal output is selected.

Both kinds of timer A interrupts can be used in capture mode: the timer A overflow interrupt is generated whenever a counter overflow occurs; the timer A match/capture interrupt is generated whenever the counter value is loaded into the Timer A data register.

By reading the captured data value in TADATA, and assuming a specific value for the timer A clock frequency, you can calculate the pulse width (duration) of the signal that is being input at the TACAP pin.

TIMER A CONTROL REGISTER (TACON)

You use the timer A control register, TACON, to:

- Select the timer A operating mode (interval timer, capture mode and PWM mode)
- Select the timer A input clock frequency
- Clear the timer A counter, TACNT
- Enable the timer A overflow interrupt or timer A match/capture interrupt
- Clear timer A match/capture interrupt pending conditions

TACON is located in set 1, Bank 0 at address EAH, and is read/write addressable using Register addressing mode. A reset clears TACON to '00H'. This sets timer A to normal interval timer mode, selects an input clock frequency of fxx/1024, and disables all timer A interrupts. You can clear the timer A counter at any time during normal operation by writing a "1" to TACON.3.

The timer A overflow interrupt (TAOVF) is interrupt level IRQ1 and has the vector address C2H. When a timer A overflow interrupt occurs and is serviced by the CPU, the pending condition is cleared automatically by hardware.

To enable the timer A match/capture interrupt (IRQ1, vector C0H), you must write TACON.1 to "1". To generate the exact time interval, you should write TACON.3 and .0 to “1”, which cleared counter and interrupt pending bit. When interrupt service routine is served, the pending condition must be cleared by software by writing a ‘0’ to the interrupt pending bit (TINTPND.0 or TINTPND.1).

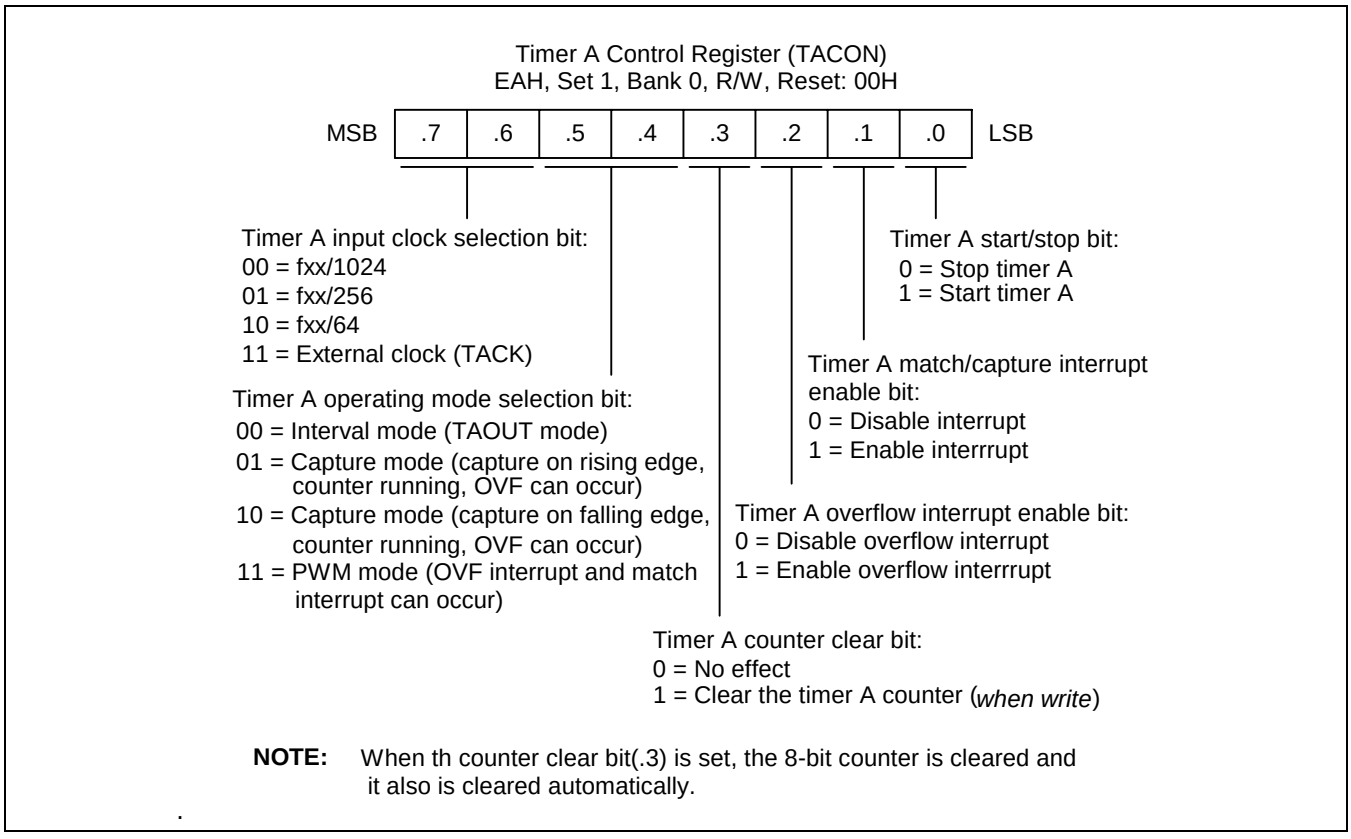
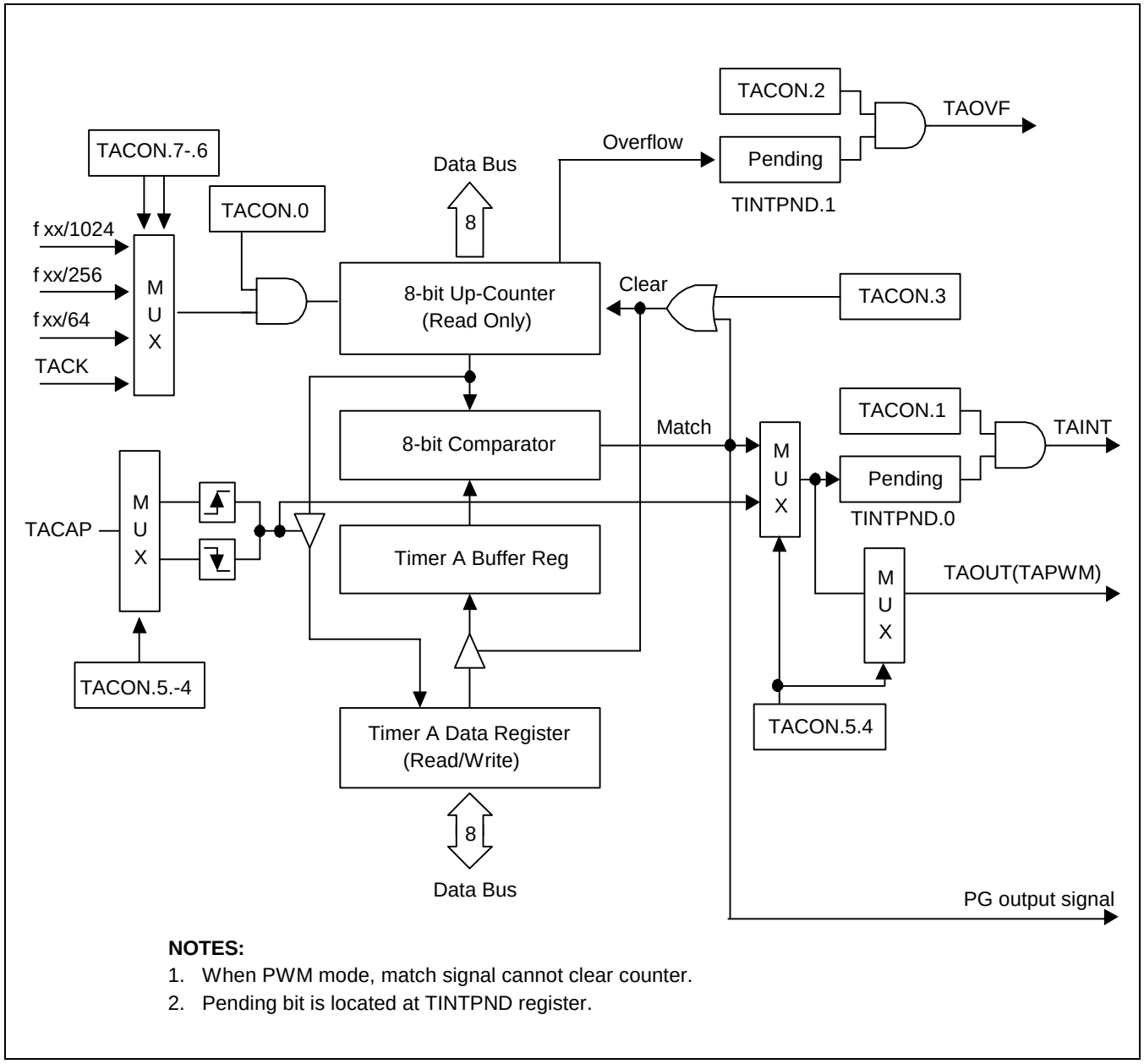


Figure 11-1. Timer A Control Register (TACON)

BLOCK DIAGRAM



NOTES:

1. When PWM mode, match signal cannot clear counter.
2. Pending bit is located at TINTPND register.

Figure 11-2. Timer A Functional Block Diagram

8-BIT TIMER B

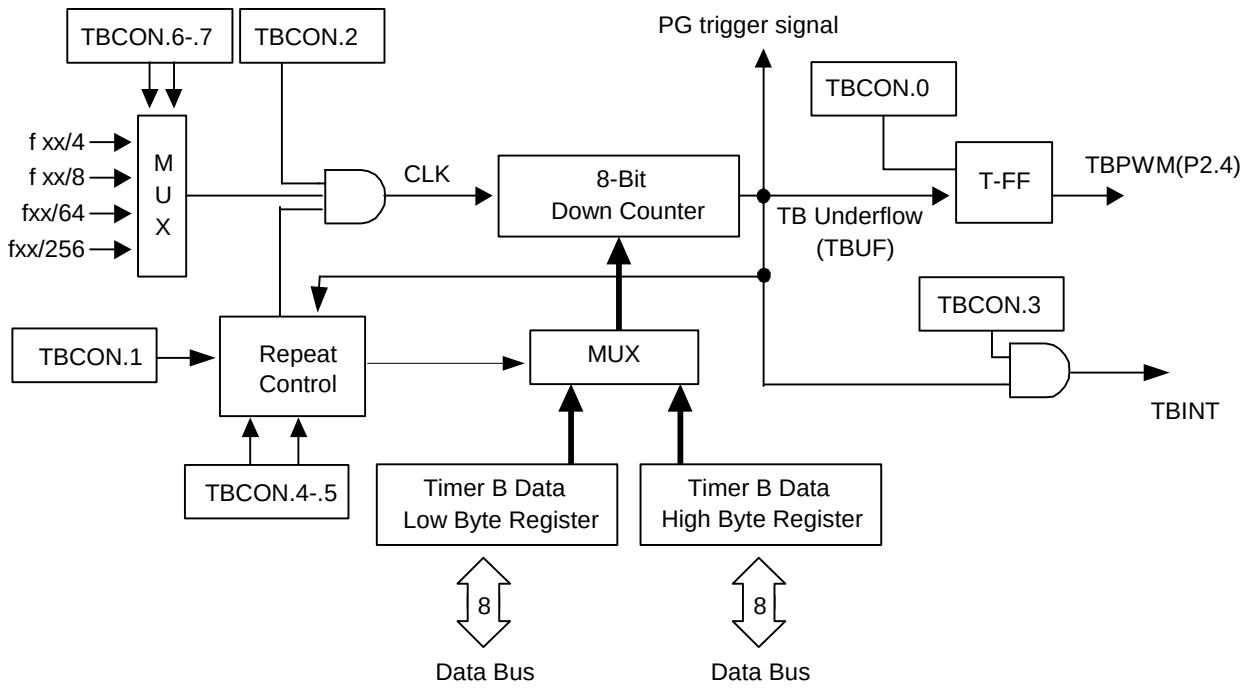
OVERVIEW

The S3F84NB micro-controller has an 8-bit timer called timer B. Timer B, which can be used to generate the carrier frequency of a remote controller signal. Also, it can be used as the programmable buzz signal generator that makes a sound with a various frequency from 200Hz to 20kHz. These various frequencies can be used to generate a melody sound.

Timer B has two functions:

- As a normal interval timer, generating a timer B interrupt at programmed time intervals.
- To generate a programmable carrier pulse for a remote control signal at P2.4.

BLOCK DIAGRAM



NOTE: In case of setting TBCON.5-.4 at '10', the value of the TBDATAL register is loaded into the 8-bit counter when the operation of the timer B starts. And then if a underflow occurs in the counter, the value of the TBDATAH register is loaded into the value of the 8-bit counter. However, if the next borrow occurs, the value of the TBDATAL register is loaded into the value of the 8-bit counter. To output TBPWM as carrier wave, you have to set P2CONH.1-.0 as "11".

Figure 11-3. Timer B Functional Block Diagram

TIMER B CONTROL REGISTER (TBCON)

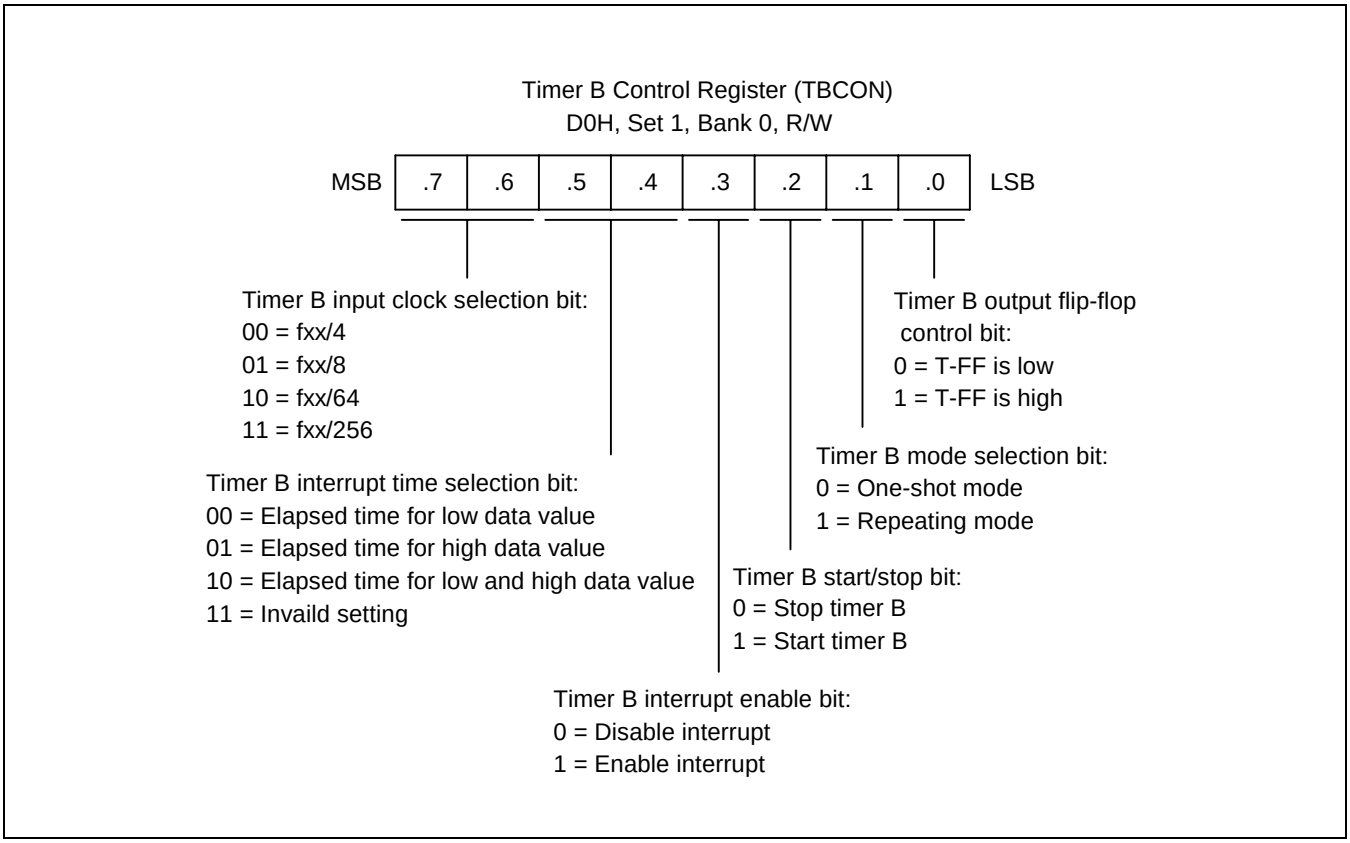


Figure 11-4. Timer B Control Register (TBCON)

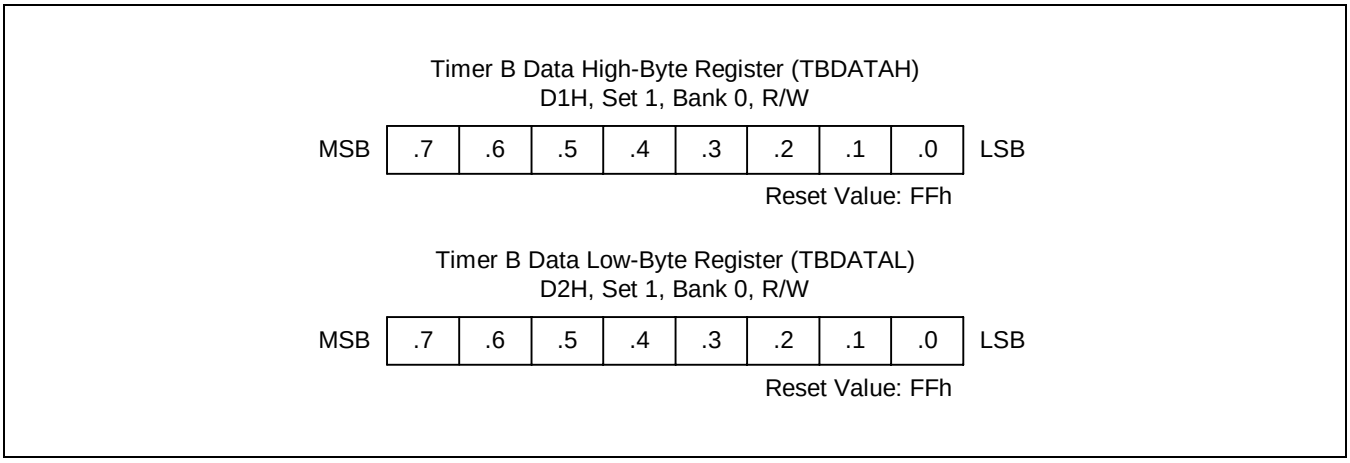
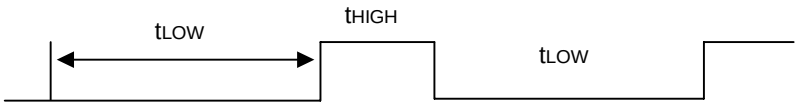


Figure 11-5. Timer B Data Registers (TBDATAH, TBDATAL)

TIMER B PULSE WIDTH CALCULATIONS



To generate the above repeated waveform consisted of low period time, t_{LOW}, and high period time, t_{HIGH}.

When T-FF = 0,

t_{LOW} = (TBDATAL + 1) x 1/fx, 0H < TBDATAL < 100H, where fx = The selected clock.

t_{HIGH} = (TBDATAH + 1) x 1/fx, 0H < TBDATAH < 100H, where fx = The selected clock.

When T-FF = 1,

t_{LOW} = (TBDATAH + 1) x 1/fx, 0H < TBDATAH < 100H, where fx = The selected clock.

t_{HIGH} = (TBDATAL + 1) x 1/fx, 0H < TBDATAL < 100H, where fx = The selected clock.

To make t_{LOW} = 24 us and t_{HIGH} = 15 us. f_{OSC} = 4 MHz, fx = 4 MHz/4 = 1 MHz

When T-FF = 0,

t_{LOW} = 24 us = (TBDATAL + 1) /fx = (TBDATAL + 1) x 1us, TBDATAL = 23.

t_{HIGH} = 15 us = (TBDATAH + 1) /fx = (TBDATAH + 1) x 1us, TBDATAH = 14.

When T-FF = 1,

t_{HIGH} = 15 us = (TBDATAL + 1) /fx = (TBDATAL + 1) x 1us, TBDATAL = 14.

t_{LOW} = 24 us = (TBDATAH + 1) /fx = (TBDATAH + 1) x 1us, TBDATAH = 23.

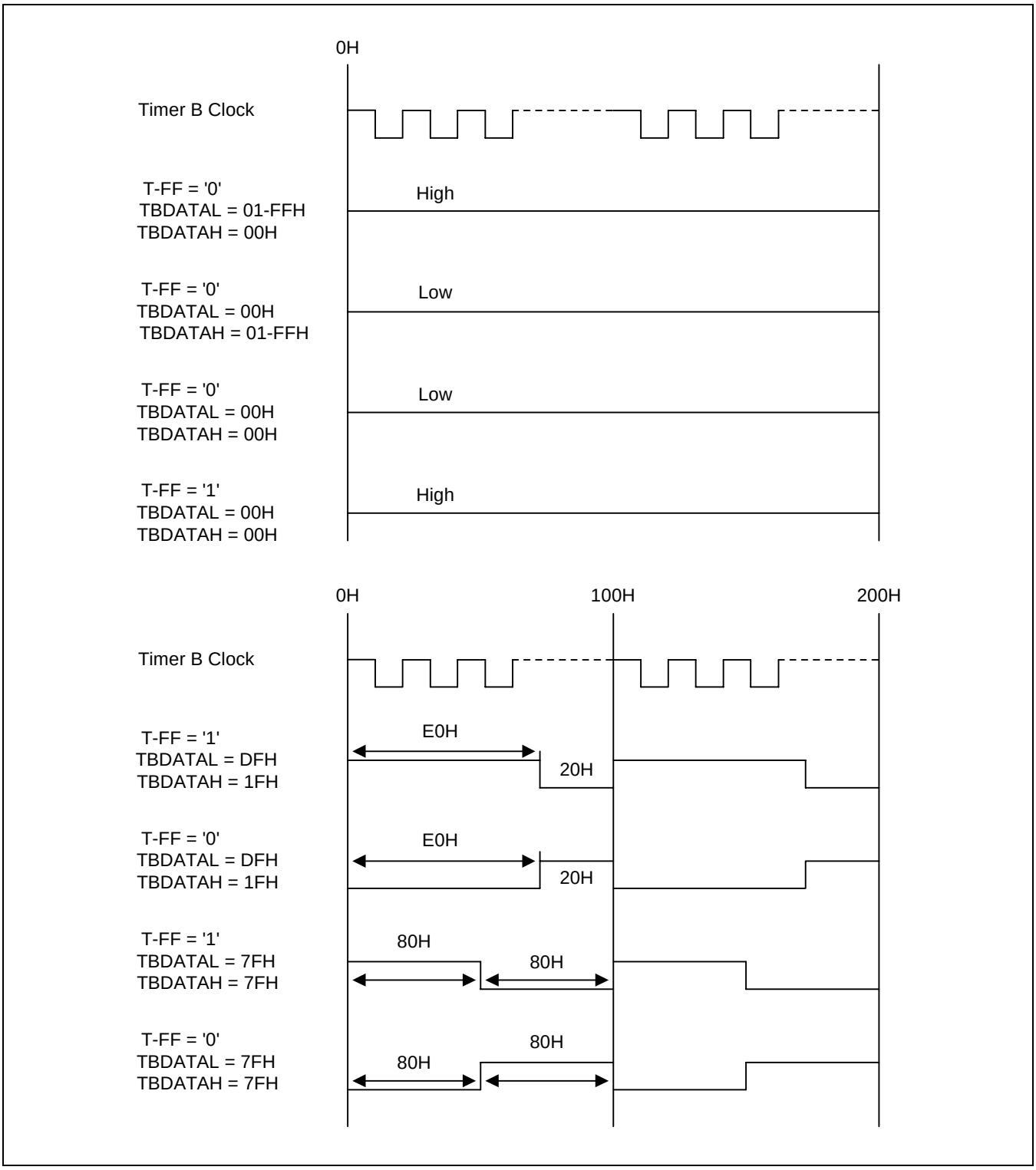
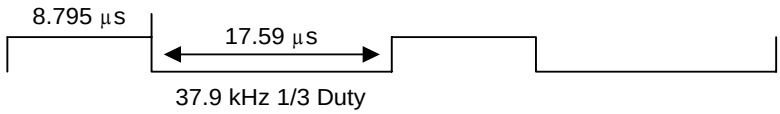


Figure 11-6. Timer B Output Flip Flop Waveforms in Repeat Mode

☞ PROGRAMMING TIP – To generate 38 kHz, 1/3duty signal through P2.4

This example sets Timer B to the repeat mode, sets the oscillation frequency as the Timer B clock source, and TBDATAH and TBDATAL to make a 38 kHz, 1/3 Duty carrier frequency. The program parameters are:



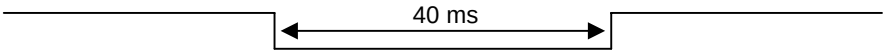
- Timer B is used in repeat mode
- Oscillation frequency is 16 MHz (0.0625 μs), fx=fxx/4=4MHz (0.25 μs)
- TBDATAH = 8.795 μs/0.25 μs = 35.18, TBDATAL = 17.59 μs/0.25 μs = 70.36
- Set P2.4 to TBPWM mode.

```
        ORG     0100H                   ;  Reset address
START   DI
        •
        •
        •
        LD      TBDATAL,#(35-1)         ;  Set 17.5 μs
        LD      TBDATAH,#(70-1)         ;  Set 8.75 μs
        LD      TBCON,#00100111B        ;  Clock Source ← fxx/4
                                        ;  Disable Timer B interrupt.
                                        ;  Select repeat mode for Timer B.
                                        ;  Start Timer B operation.
                                        ;  Set Timer B Output flip-flop (T-FF) high.

        LD      P2CONH,#03H             ;  Set P2.4 to TBPWM mode.
                                        ;  This command generates 38 kHz, 1/3 duty pulse signal
                                           through P2.4.
        •
        •
        •
```

☞ PROGRAMMING TIP – To generate a one pulse signal through P2.4

This example sets Timer B to the one shot mode, sets the oscillation frequency as the Timer B clock source, and TBDATAH and TBDATAL to make a 40μs width pulse. The program parameters are:



- Timer B is used in one shot mode
- Oscillation frequency is 4 MHz (fx=1/4 clock = 1 μs)
- TBDATAH = 40 μs / 1 μs = 40, TBDATAL = 1
- Set P2.4 to TBPWM mode

```
            ORG     0100H               ;  Reset address
START       DI
            •
            •
            •
            LD      TBDATAH,# (40-1)    ;  Set 40 μs
            LD      TBDATAL,# 1         ;  Set any value except  00H
            LD      TBCON,#00010001B    ;  Clock Source ← fxx/4
                                        ;  Disable Timer B interrupt.
                                        ;  Select one shot mode for Timer B.
                                        ;  Stop Timer B operation.
                                        ;  Set Timer B output flip-flop (T-FF) high
            LD      P2CONH, #03H        ;  Set P2.4 to TBPWM mode.
            •
            •
PULSE_OUT:  LD      TBCON,#00000101B    ;  Start Timer B operation
                                        ;  to make the pulse at  this point.
            •                           ;  After the instruction is executed, 0.75 μs is required
            •                           ;  before the falling edge of the pulse starts.
            •
```

8-BIT TIMER C(0,1)

OVERVIEW

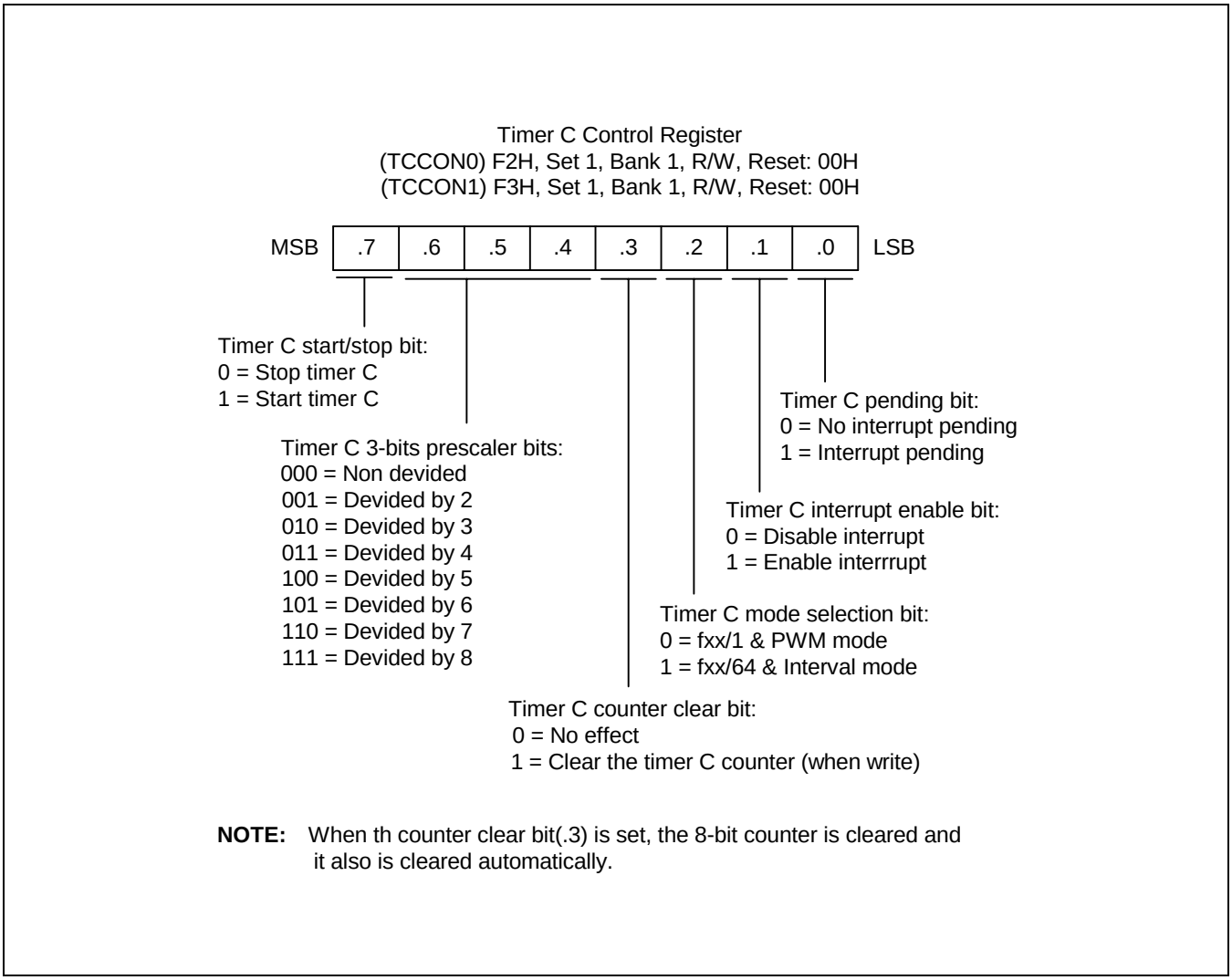
The 8-bit timer C(0,1) is an 8-bit general-purpose timer/counter. Timer C(0,1) has two operating modes, you can select one of them using the appropriate TCCON0, TCCON1 setting:

- Interval timer mode (Toggle output at TCOUT0, TCOUT1 pin), only match interrupt occurs
- PWM mode (TCOUT0, TCOUT1 pin), match and overflow interrupt can occur

Timer C(0,1) has the following functional components:

- Clock frequency divider with multiplexer
- 8-bit counter, 8-bit comparator, and 8-bit reference data register (TCDATA0, TCDATA1)
- PWM or match output (TCOUT0, TCOUT1)
- Timer C(0) match/overflow interrupt (IRQ2, vector C4H) generation
- Timer C(1) match/overflow interrupt (IRQ2, vector C6H) generation
- Timer C(0) control register, TCCON0 (set 1, bank1, F2H, read/write)
- Timer C(1) control register, TCCON1 (set 1, bank1, F3H, read/write)

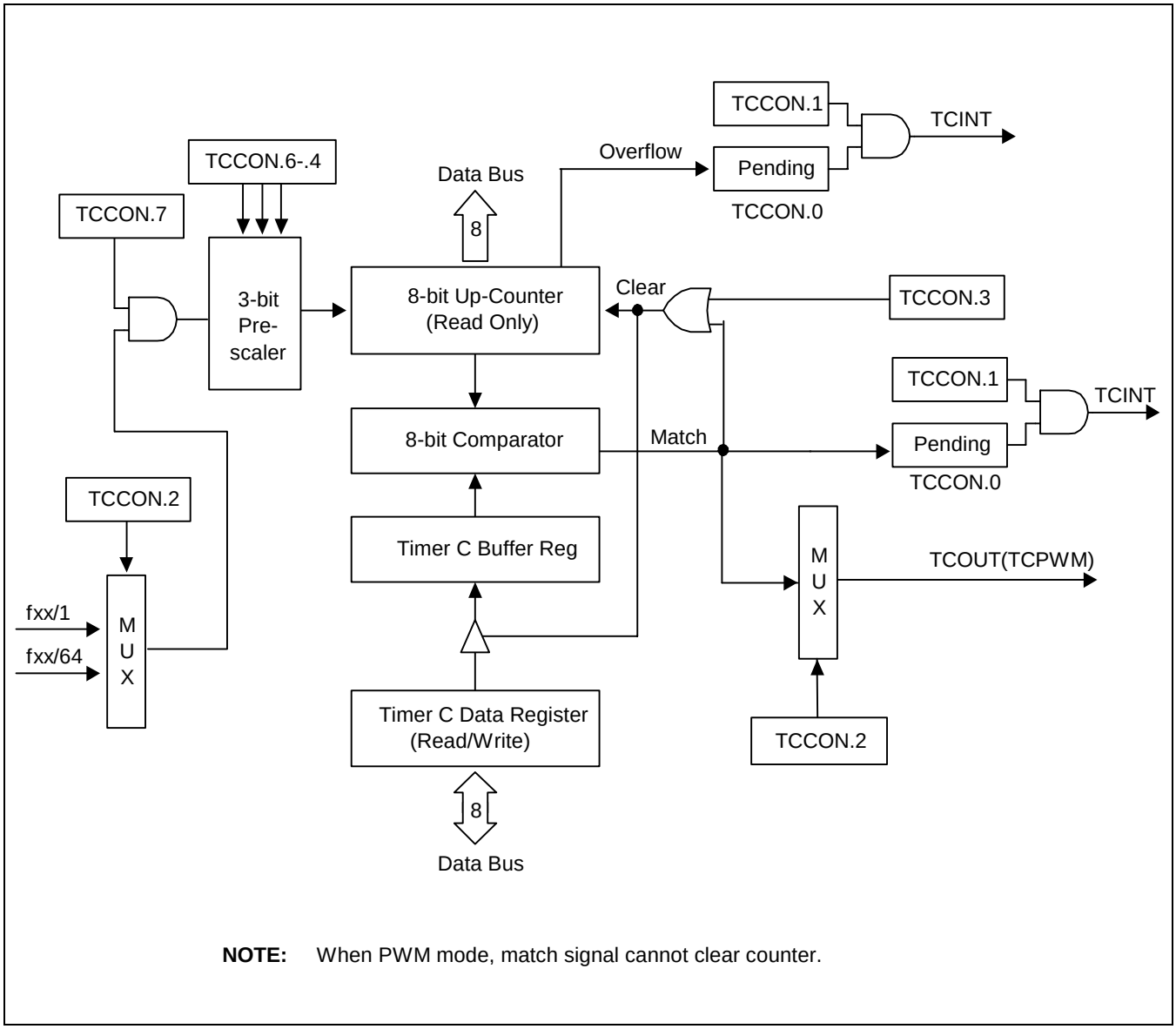
TIMER C (0,1) CONTROL REGISTER (TCCON0, TCCON1)



NOTE: When th counter clear bit(.3) is set, the 8-bit counter is cleared and it also is cleared automatically.

Figure 11-7. Timer C0, C1 Control Register (TCCON0, TCCON1)

BLOCK DIAGRAM



NOTE: When PWM mode, match signal cannot clear counter.

Figure 11-8. Timer C0, C1 Functional Block Diagram

☞ PROGRAMMING TIP – Using the Timer A

```
                ORG         0000h

                VECTOR      0C0h,TAMC_INT
                VECTOR      0C2h,TAOV_INT

                ORG         0100h

INITIAL:
                LD          SYM,#00h            ;  Disable Global/Fast interrupt → SYM
                LD          IMR,#00000010b      ;  Enable IRQ1 interrupt
                LD          SPH,#00000000b      ;  Set stack area
                LD          SPL,#00000000b
                LD          BTCON,#10100011b    ;  Disable watch-dog

                LD          TADATA,#80h
                LD          TACON,#01001010b    ;  Match interrupt enable
                                                ;  6.55 ms duration (10 MHz x'tal)

                EI

MAIN:
                •
                •
                MAIN ROUTINE
                •
                •

                JR          T,MAIN

TAMC_INT:
                •
                •
                Interrupt service routine
                •
                •
                IRET

TAOV_INT:
                •
                Interrupt service routine
                •
                IRET


                .END
```

☞ PROGRAMMING TIP – Using the Timer B

```
                ORG         0000h

                VECTOR      0BEh,TBUN_INT

                ORG         0100h

INITIAL:
                LD          SYM,#00h            ;  Disable Global/Fast interrupt
                LD          IMR,#00000001b      ;  Enable IRQ0 interrupt
                LD          SPH,#00000000b      ;  Set stack area
                LD          SPL,#00000000b
                LD          BTCON,#10100011b    ;  Disable Watch-dog

                LD          P2CONH,#00000011b   ;  Enable TBPWM output

                LD          TBDATAH,#80h
                LD          TBDATAL,#80h
                LD          TBCON,#11101110b    ;  Enable interrupt, fxx/256, Repeat
                                                ;  Duration 6.605ms (10 MHz x'tal)

                EI

MAIN:
                •
                •
                •
                MAIN ROUTINE
                •
                •
                •

                JR          T,MAIN

TBUN_INT:
                •
                •
                •
                Interrupt service routine
                •
                •
                •
                IRET

                .END
```

☞ PROGRAMMING TIP – Using the Timer C(0)

```
                ORG         0000h

                VECTOR      0C4h, TCUN_INT

                ORG         0100h

INITIAL:
                LD          SYM, #00h               ;  Disable Global/Fast interrupt
                LD          IMR,#00000100b          ;  Enable IRQ2 interrupt
                LD          SPH,#00000000b          ;  Set stack area
                LD          SPL,#00000000b
                LD          BTCON,#10100011b        ;  Disable Watch-dog

                LD          P3CONH,#00110000b       ;  Enable TCOUT0 output
                SB1
                LD          TCDATA0,#80h
                LD          TCCON0,#10001110b       ;  Enable interrupt , non-div, fxx/64
                                                    ;  Duration 1.638ms (10 MHz x'tal)
                SB0
                EI

MAIN:
                •
                •
                •
                MAIN ROUTINE
                •
                •
                •

                JR          T,MAIN

TCUN_INT:
                •
                •
                •
                Interrupt service routine
                •
                •
                •
                IRET

                .END
```

12 16-BIT TIMER 1(0,1)

OVERVIEW

The S3F84NB has two 16-bit timer/counters. The 16-bit timer 1(0,1) is an 16-bit general-purpose timer/counter. Timer 1(0,1) has three operating modes, one of which you select using the appropriate T1CON0, T1CON1 setting is

- Interval timer mode (Toggle output at T1OUT0, T1OUT1 pin)
- Capture input mode with a rising or falling edge trigger at the T1CAP0, T1CAP1 pin
- PWM mode (T1PWM0, T1PWM1); PWM output shares their output port with T1OUT0, T1OUT1 pin

Timer 1(0,1) has the following functional components:

- Clock frequency divider (fxx divided by 1024, 256, 64, 8, 1) with multiplexer
- External clock input pin (T1CK0, T1CK1)
- A 16-bit counter (T1CNTH0/L0, T1CNTH1/L1), a 16-bit comparator, and two 16-bit reference data register (T1DATAH0/L0, T1DATAH1/L1)
- I/O pins for capture input (T1CAP0, T1CAP1), or match output (T1OUT0, T1OUT1)
- Timer 1(0) overflow interrupt (IRQ3, vector CAH) and match/capture interrupt (IRQ3, vector C8H) generation
- Timer 1(1) overflow interrupt (IRQ3, vector CEH) and match/capture interrupt (IRQ3, vector CCH) generation
- Timer 1(0) control register, T1CON0 (set 1, EAH, Bank 1, read/write)
- Timer 1(1) control register, T1CON1 (set 1, EBH, Bank 1, read/write)

FUNCTION DESCRIPTION

Timer 1(0,1) Interrupts (IRQ3, Vectors CEH, CCH, CAH and C8H)

The timer 1(0) module can generate two interrupts, the timer 1(0) overflow interrupt (T1OVF0), and the timer 1(0) match/capture interrupt (T1INT0). T1OVF0 is interrupt level IRQ3, vector CAH. T1INT0 also belongs to interrupt level IRQ3, but is assigned the separate vector address, C8H.

A timer 1(0) overflow interrupt pending condition is automatically cleared by hardware when it has been serviced. A timer 1(0) match/capture interrupt, T1INT0 pending condition is also cleared by hardware when it has been serviced.

The timer 1(1) module can generate two interrupts, the timer 1(1) overflow interrupt (T1OVF1), and the timer 1(1) match/capture interrupt (T1INT1). T1OVF1 is interrupt level IRQ3, vector CEH. T1INT1 also belongs to interrupt level IRQ3, but is assigned the separate vector address, CCH.

A timer 1(1) overflow interrupt pending condition is automatically cleared by hardware when it has been serviced. A timer 1(1) match/capture interrupt, T1INT1 pending condition is also cleared by hardware when it has been serviced.

Interval Mode (match)

The timer 1(0) module can generate an interrupt: the timer 1(0) match interrupt (T1INT0). T1INT0 belongs to interrupt level IRQ3, and is assigned the separate vector address, C8H. In interval timer mode, a match signal is generated and T1OUT0 is toggled when the counter value is identical to the value written to the Timer 1 reference data registers, T1DATAH0 and T1DATAL0. The match signal generates a timer 1(0) match interrupt (T1INT0, vector C8H) and clears the counter value.

The timer 1(1) module can generate an interrupt: the timer 1(1) match interrupt (T1INT1). T1INT1 belongs to interrupt level IRQ3, and is assigned the separate vector address, CCH. In interval timer mode, a match signal is generated and T1OUT1 is toggled when the counter value is identical to the value written to the Timer 1 reference data register, T1DATAH1 and T1DATAL1. The match signal generates a timer 1(1) match interrupt (T1INT1, vector CCH) and clears the counter value.

Capture Mode

In capture mode for timer 1(0), a signal edge that is detected at the T1CAP0 pin opens a gate and loads the current counter value into the timer 1 data registers (T1DATAH0, T1DATAL0 for rising edge, or falling edge). You can select rising or falling edge to trigger this operation. The timer 1(0) also gives you capture input source, the signal edge at the T1CAP0 pin. You select the capture input by setting the value of the timer 1(0) capture input selection bit in the port 3 control register low, P3CONL, (set 1 bank 0, F5H).

Both kinds of timer 1(0) interrupts (T1OVF0, T1INT0) can be used in capture mode, the timer 1(0) overflow interrupt is generated whenever a counter overflow occurs, the timer 1(0) capture interrupt is generated whenever the counter value is loaded into the timer 1 data register.

By reading the captured data value in T1DATAH0, T1DATAL0, and assuming a specific value for the timer 1(0) clock frequency, you can calculate the pulse width (duration) of the signal that is being input at the T1CAP0 pin.

In capture mode for Timer 1(1), a signal edge that is detected at the T1CAP1 pin opens a gate and loads the current counter value into the timer 1 data register (T1DATAH1, T1DATAL1 for rising edge, or falling edge). You can select rising or falling edges to trigger this operation. The timer 1(1) also gives you capture input source, the signal edge at the T1CAP1 pin. You select the capture input by setting the value of the timer 1(1) capture input selection bit in the port 3 control register low, P3CONL, (set 1 bank 0, F5H).

Both kinds of timer 1(1) interrupts (T1OVF1, T1INT1) can be used in capture mode, the timer 1(1) overflow

interrupt is generated whenever a counter overflow occurs, the timer 1(1) capture interrupt is generated whenever the counter value is loaded into the timer 1 data register.

By reading the captured data value in T1DATAH1, T1DATAL1, and assuming a specific value for the timer 1(1) clock frequency, you can calculate the pulse width (duration) of the signal that is being input at the T1CAP1 pin.

PWM Mode

Pulse width modulation (PWM) mode lets you program the width (duration) of the pulse that is output at the T1OUT0, T1OUT1 pin. As in interval timer mode, a match signal is generated when the counter value is identical to the value written to the timer 1(0,1) data registers. In PWM mode, however, the match signal does not clear the counter but can generate a match interrupt. Instead, it runs continuously, overflowing at FFFFH, and then continuous increasing from 0000H. Whenever an overflow occur, an overflow (T1OVF0,1) interrupt can be generated.

Although you can use the match or overflow interrupts in the PWM mode, these interrupts are not typically used in PWM-type applications. Instead, the pulse at the T1OUT0, T1OUT1 pin is held to low level as long as the reference data value is less than or equal to(≤) the counter value and then the pulse is held to high level for as long as the data value is greater than(>) the counter value. One pulse width is equal to $t_{CLK.}$

TIMER 1(0,1) CONTROL REGISTER (T1CON0, T1CON1)

You use the timer 1(0,1) control register, T1CON0, T1CON1, to:

- Select the timer 1(0,1) operating mode (Interval timer, Capture mode, PWM mode)
- Select the timer 1(0,1) input clock frequency
- Clear the timer 1(0,1) counter, T1CNTH0/L0, T1CNTH1/L1
- Enable the timer 1(0,1) overflow interrupt
- Enable the timer 1(0,1) match/capture interrupt

T1CON0 is located in set 1 and Bank 1 at address EAH, and is read/write addressable using Register addressing mode. T1CON1 is located in set 1 and Bank 1 at address EBH, and is read/write addressable using Register addressing mode.

A reset clears T1CON0, T1CON1 to '00H'. This sets timer 1(0,1) to normal interval timer mode, selects an input clock frequency of fxx/1024, and disables all timer 1(0,1) interrupts. To disable the counter operation, please set T1CON (0,1).7-.5 to 111B. You can clear the timer 1(0,1) counter at any time during normal operation by writing a "1" to T1CON (0,1).3.

The timer 1(0) overflow interrupt (T1OVF0) is interrupt level IRQ3 and has the vector address CAH. And, the timer 1(1) overflow interrupt (T1OVF1) is interrupt level IRQ3 and has the vector address CEH. To generate the exact time interval, you should write "1" to T1CON (0,1).2 and clear appropriate pending bits of the TINTPND register.

To detect a match/capture or overflow interrupt pending condition when T1INT0, T1INT1 or T1OVF0, T1OVF1 is disabled, the application program should poll the pending bit TINTPND register, bank 0, address E9H. When a "1" is detected, a timer 1(0,1) match/capture or overflow interrupt is pending. When the sub-routine has been serviced, the pending condition must be cleared by software by writing a "0" to the interrupt pending bit. If interrupts (match/capture or overflow) are enabled, the pending bit is cleared automatically by hardware.

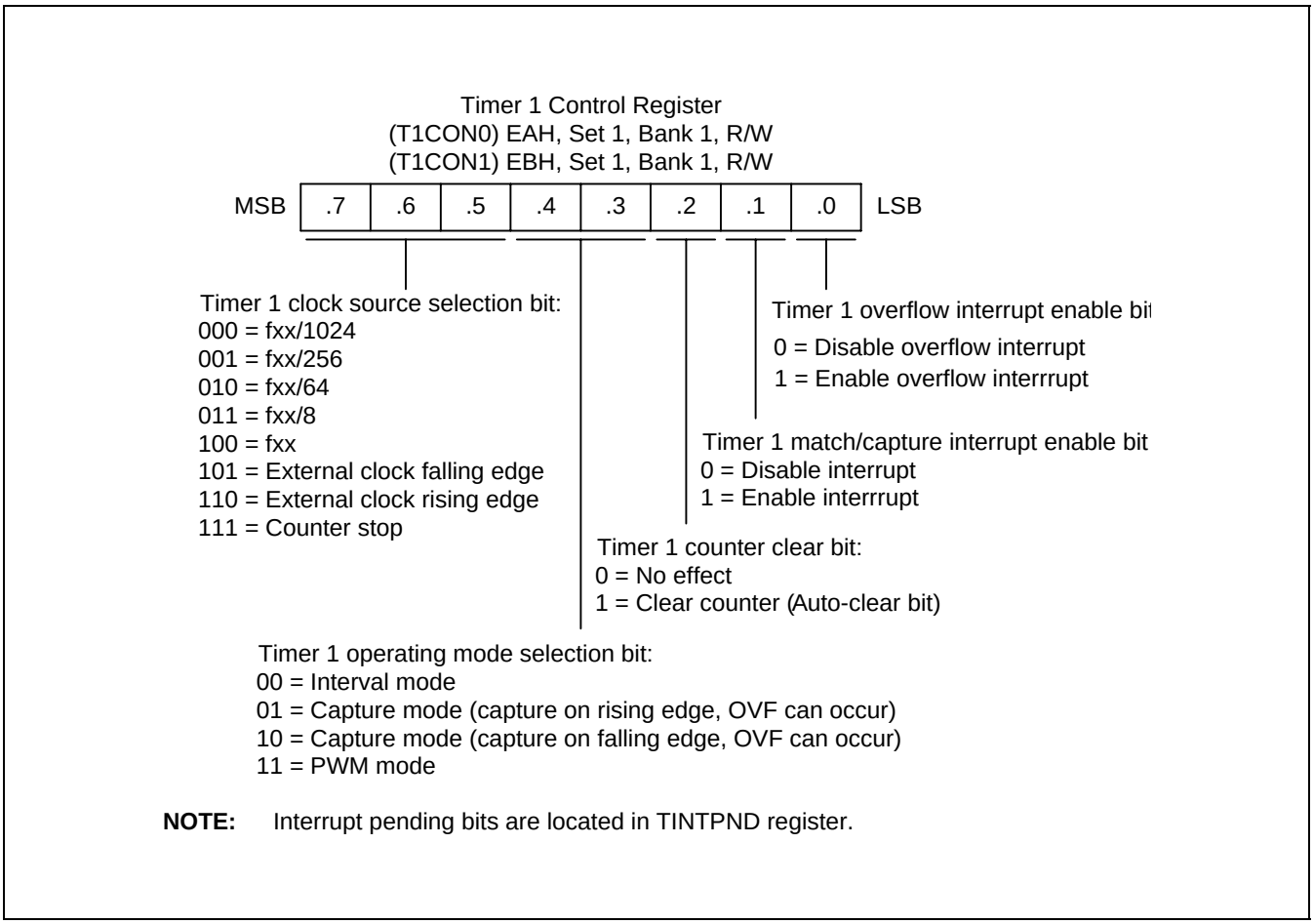


Figure 12-1. Timer 1(0,1) Control Register (T1CON0, T1CON1)

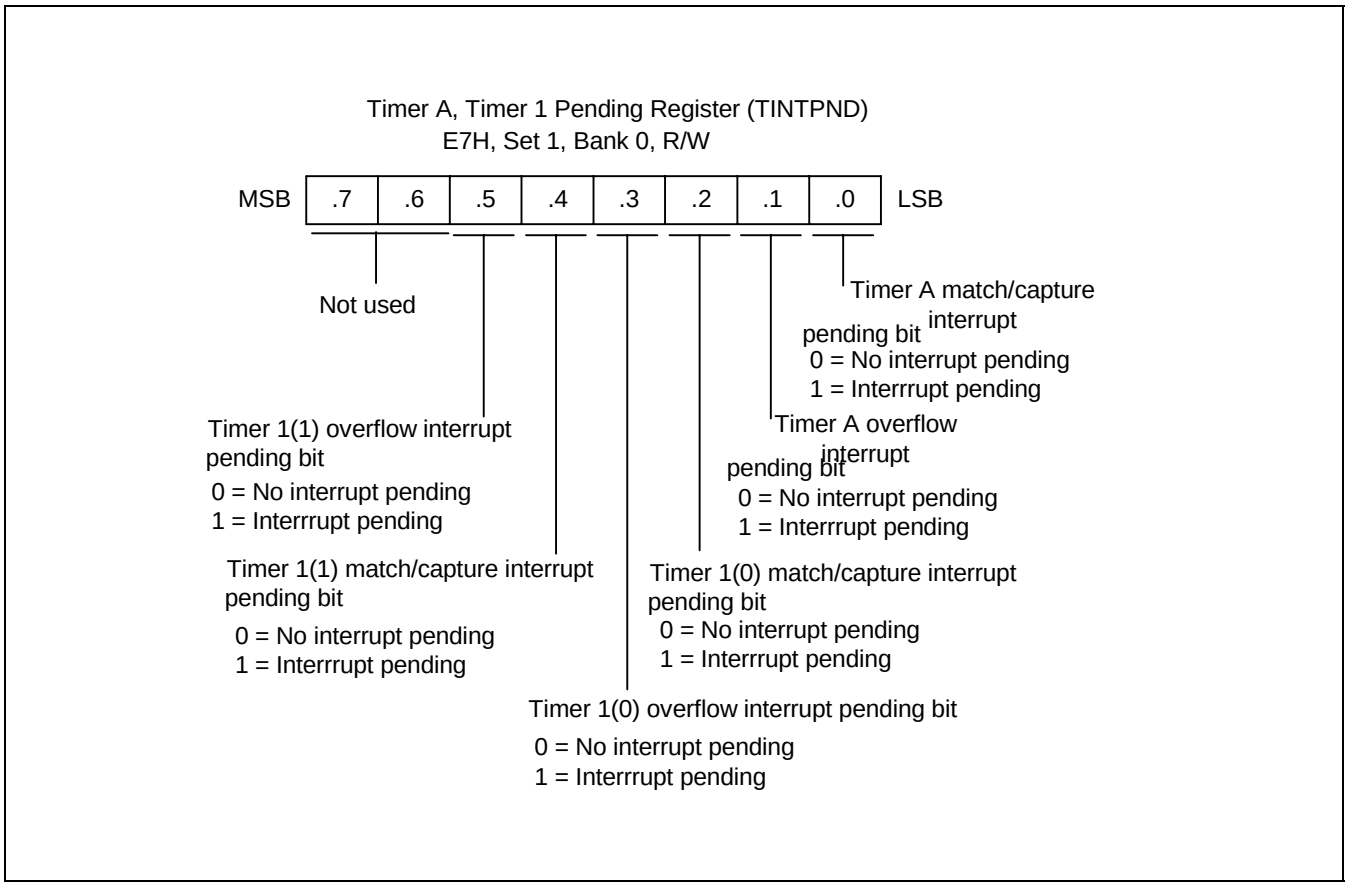
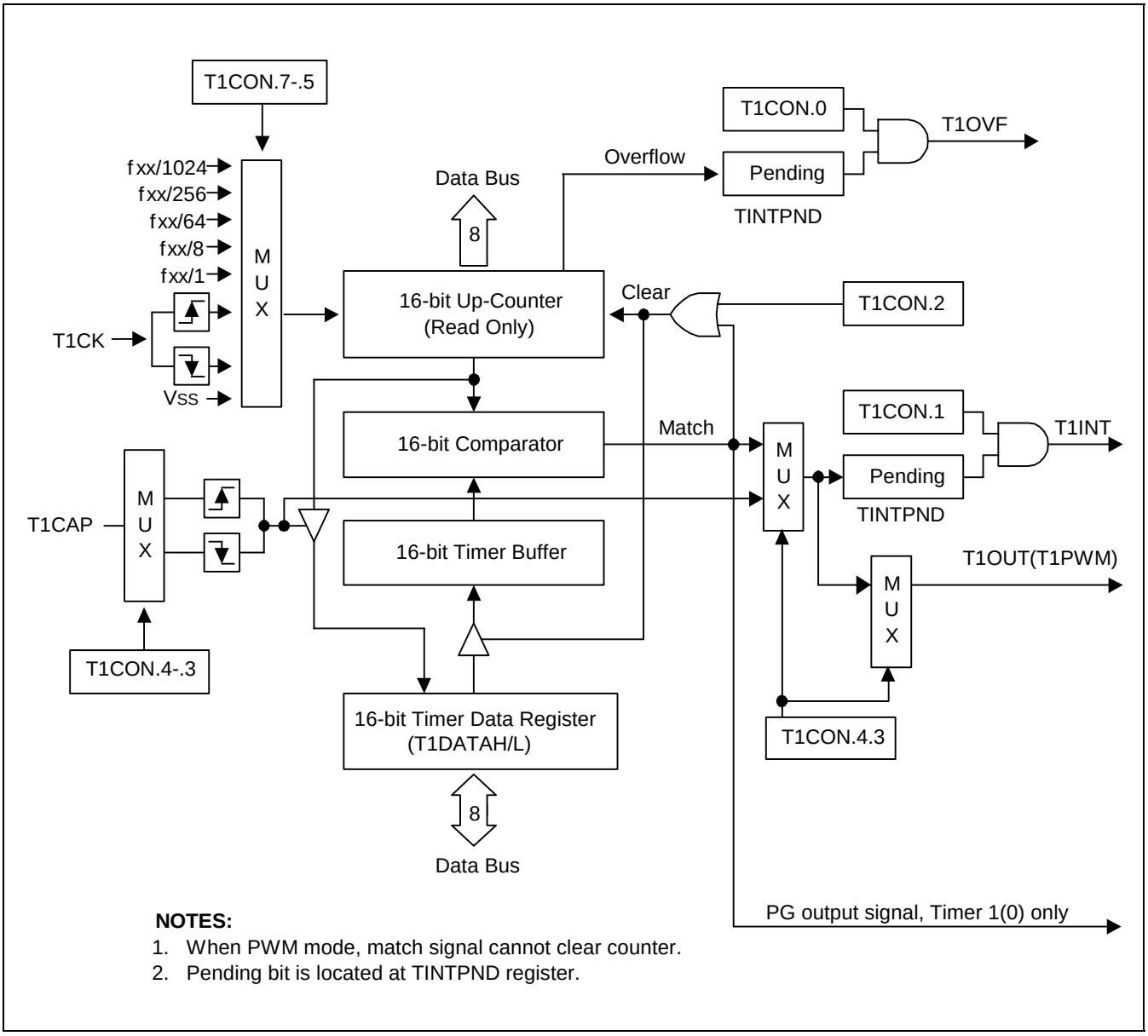


Figure 12-2. Timer A, Timer 1(0,1) Pending Register (TINTPND)

BLOCK DIAGRAM



NOTES:

1. When PWM mode, match signal cannot clear counter.
2. Pending bit is located at TINTPND register.

Figure 12-3. Timer 1(0,1) Functional Block Diagram

☞ PROGRAMMING TIP – Using the Timer 1(0)

```
                ORG         0000h

                VECTOR      0C8h,TIM1_INT

                ORG         0100h

INITIAL:
                LD          SYM,#00h            ;  Disable Global/Fast interrupt
                LD          IMR,#00001000b      ;  Enable IRQ3 interrupt
                LD          SPH,#00000000b      ;  Set stack area
                LD          SPL,#00000000b
                LD          BTCON,#10100011b    ;  Disable Watch-dog

                SB1
                LD          T1CON0,#01000110b   ;  Enable interrupt ,fxx/64, Interval,
                                                ;  Interval= 1.536 ms (10 MHz x'tal)
                LDW         T1DATAH0,#00F0h     ;  T1DATAH0=00h, T1DATAL0=F0h
                SB0

                EI

MAIN:
                •
                •
                •
                MAIN ROUTINE
                •
                •
                •

                JR          T,MAIN

TIM1_INT:
                •
                •
                •
                Interrupt service routine
                •
                •
                •
                IRET

                END
```

13 SERIAL I/O PORT

OVERVIEW

Serial I/O module, SIO can interface with various types of external devices that require serial data transfer. SIO has the following functional components:

- SIO data receive/transmit interrupt (IRQ4, vector D0H) generation
- 8-bit control register, SIOCON (set 1, bank 1, E1H, read/write)
- Clock selection logic
- 8-bit data buffer, SIODATA (set 1, bank 1, E0H, read/write)
- 8-bit prescaler (SIOPS), (set 1, bank 1, F4H, read/write)
- 3-bit serial clock counter
- Serial data I/O pins (P2.0–P2.1, SO, SI)
- External clock input/output pin (P2.2, SCK)

The SIO module can transmit or receive 8-bit serial data at a frequency determined by its corresponding control register settings. To ensure flexible data transmission rates, you can select an internal or external clock source.

PROGRAMMING PROCEDURE

To program the SIO modules, follow these basic steps:

1. Configure P2.1, P2.0 and P2.2 to alternative function (SI, SO, SCK) for interfacing SIO module by setting the P2CONL register to appropriately value.
2. Load an 8-bit value to the SIOCON control register to properly configure the serial I/O module. In this operation, SIOCON.2 must be set to "1" to enable the data shifter.
3. For interrupt generation, set the serial I/O interrupt enable bit, SIOCON.1 to "1".
4. To transmit data to the serial buffer, write data to SIODATA and set SIOCON.3 to 1, then the shift operation starts.
5. When the shift operation (transmit/receive) is completed, the SIO pending bit (SIOCON.0) is set to "1" and an SIO interrupt request is generated.

SIO CONTROL REGISTER (SIOCON)

The control register for the serial I/O interface module, SIOCON, is located in set 1, bank 1 at address E1H. It has the control settings for SIO module.

- Clock source selection (internal or external) for shift clock
- Interrupt enable
- Edge selection for shift operation
- Clear 3-bit counter and start shift operation
- Shift operation (transmit) enable
- Mode selection (transmit/receive or receive-only)
- Data direction selection (MSB first or LSB first)

A reset clears the SIOCON value to '00H'. This configures the corresponding module with an internal clock source, P.S clock, at the SCK, selects receive-only operating mode, the data shift operation and the interrupt are disabled, and the data direction is selected to MSB-first.
So, if you want to use SIO module, you must write appropriate value to SIOCON.

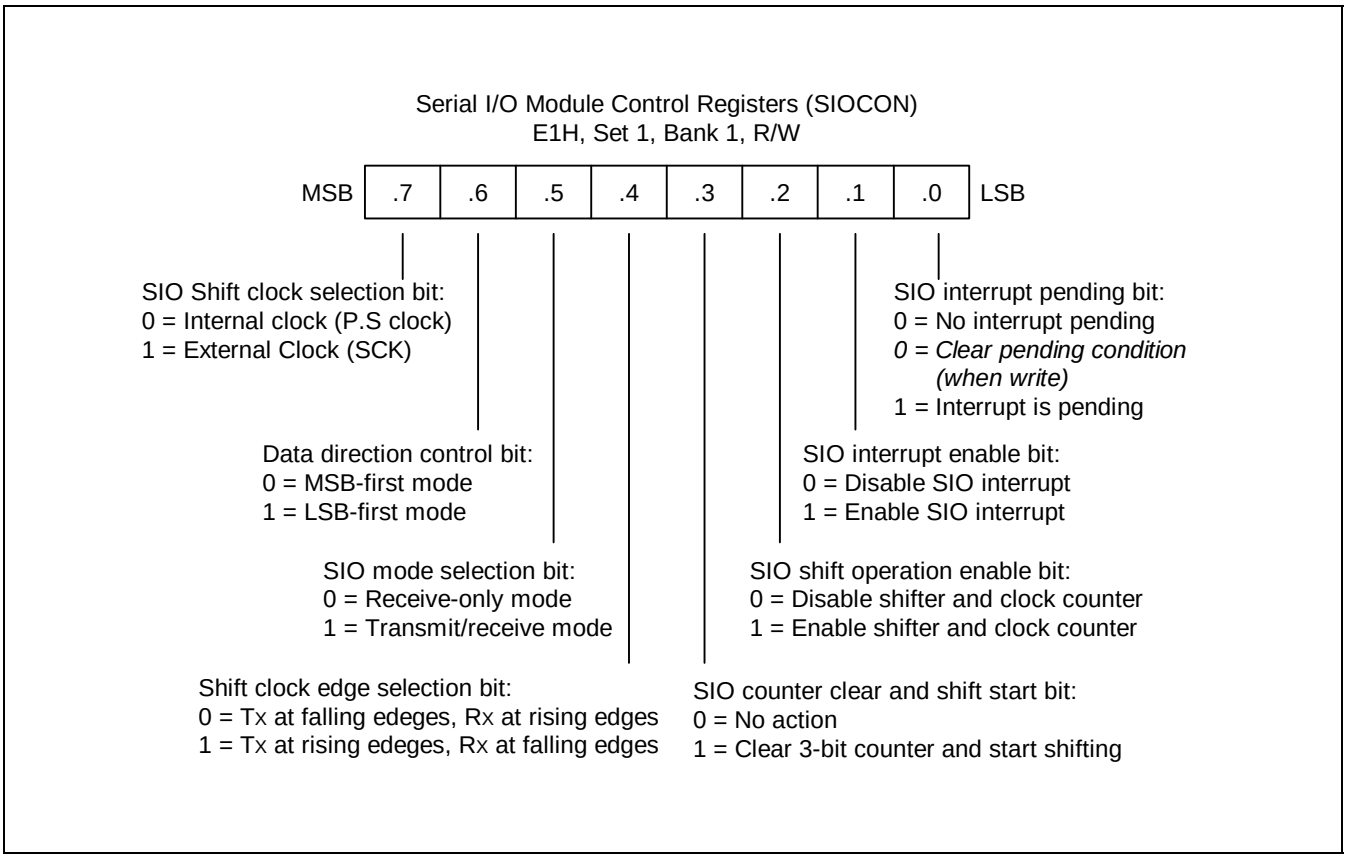


Figure 13-1. Serial I/O Module Control Registers (SIOCON)

SIO PRESCALER REGISTER (SIOPS)

The control register for the serial I/O interface module, SIOPS, is located in set 1, bank 1, at address F4H. The value stored in the SIO prescaler registers, SIOPS, lets you determine the SIO clock rate (baud rate) as follows:

Baud rate = Input clock (fxx)/[(SIOPS value + 1) × 4] or SCK input clock.

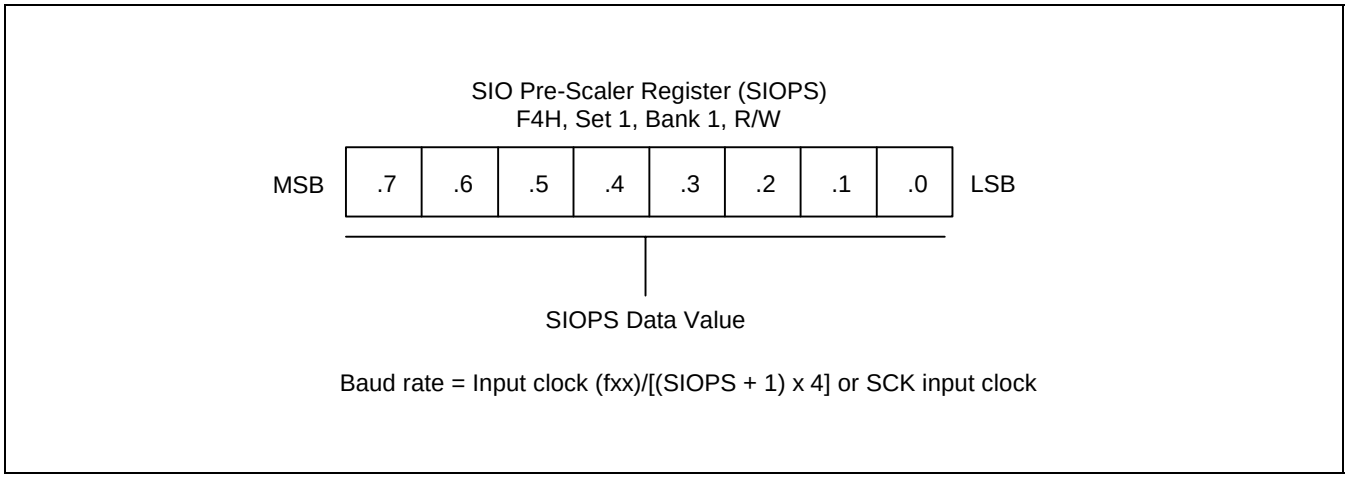


Figure 13-2. SIO Prescaler Register (SIOPS)

BLOCK DIAGRAM

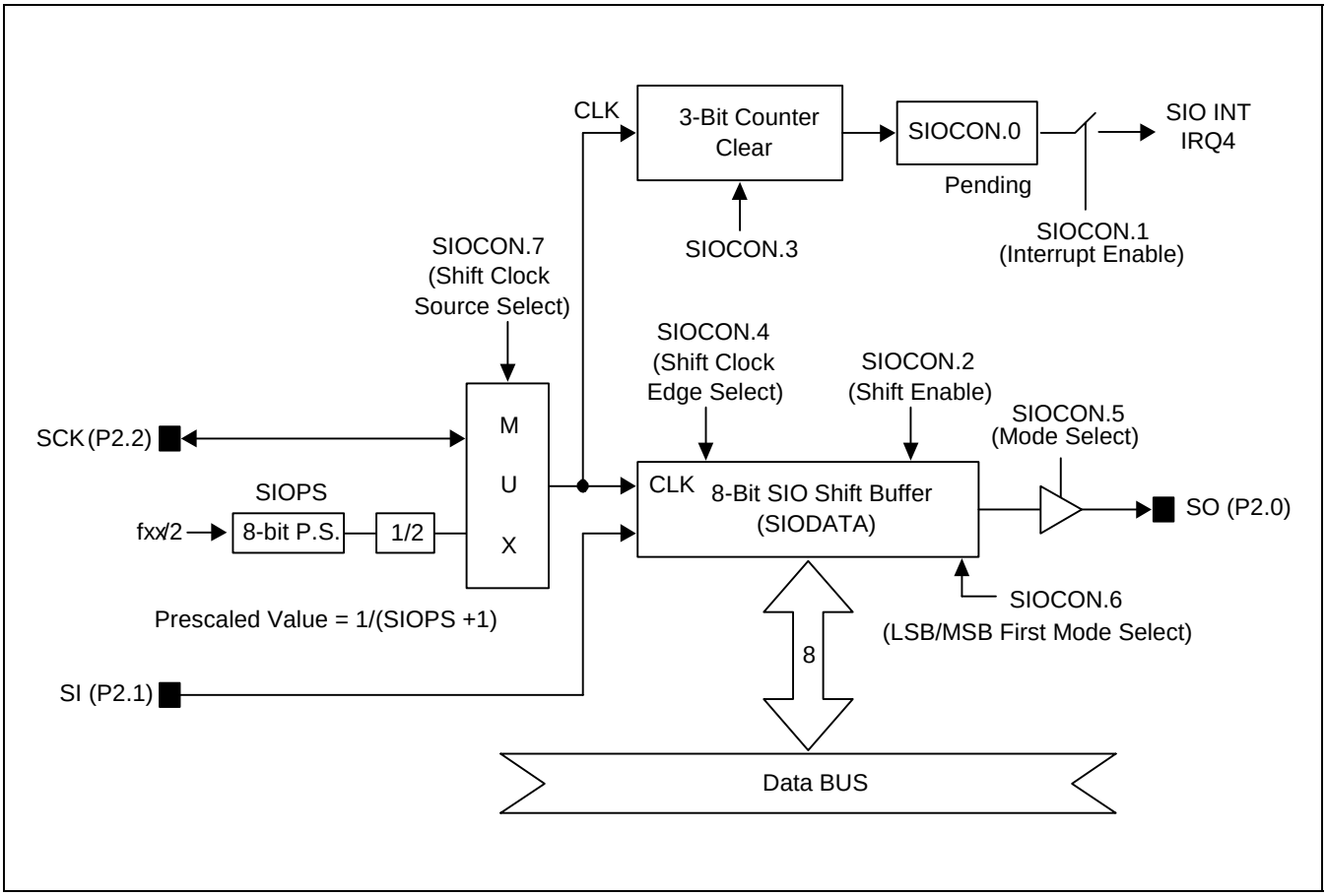


Figure 13-3. SIO Functional Block Diagram

SERIAL I/O TIMING DIAGRAMS

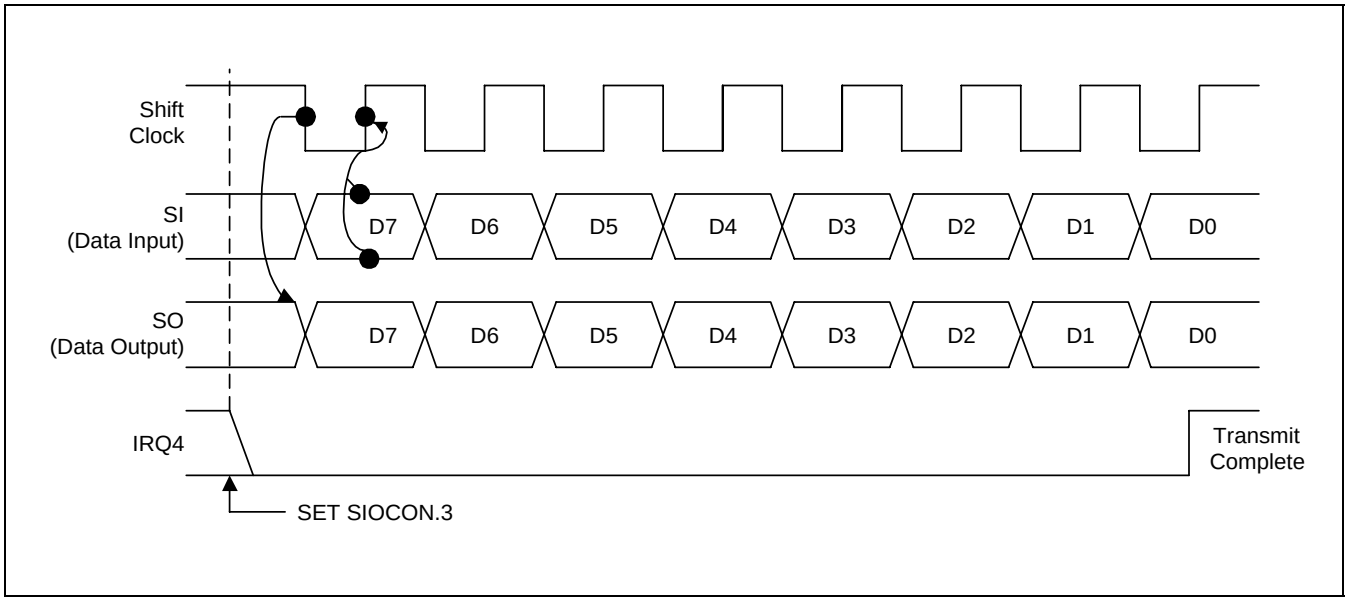


Figure 13-4. SIO Timing in Transmit/Receive Mode (Tx at falling edge, SIOCON.4=0)

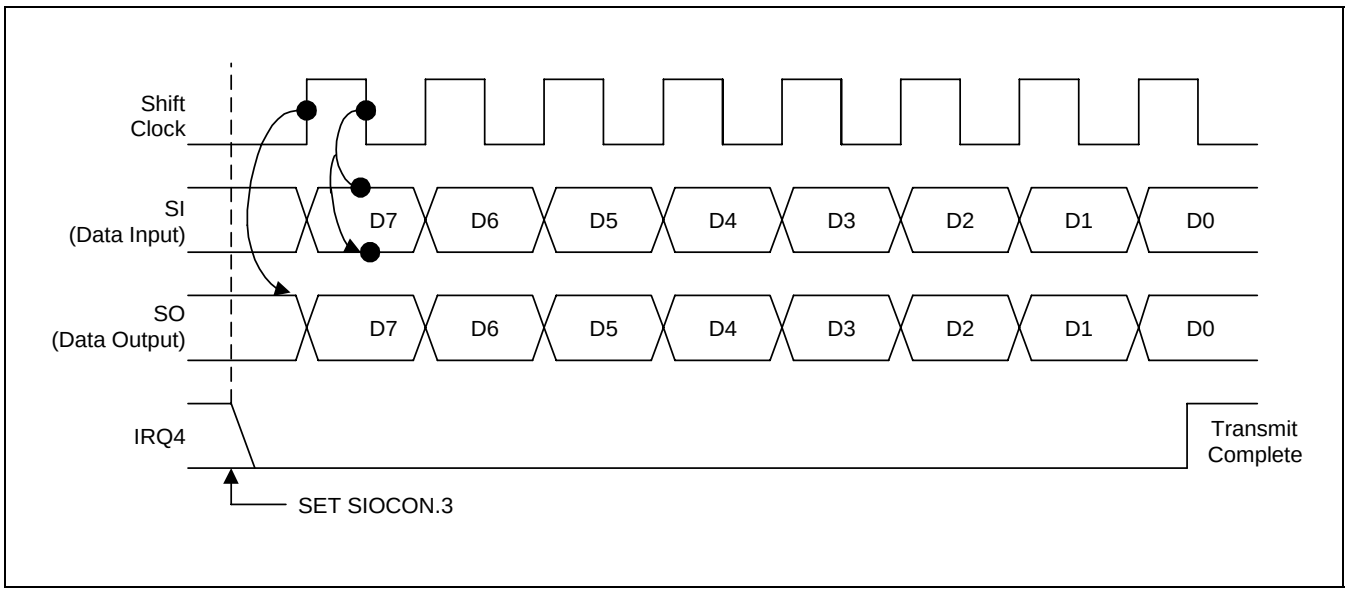


Figure 13-5. SIO Timing in Transmit/Receive Mode (Tx at rising edge, SIOCON.4=1)

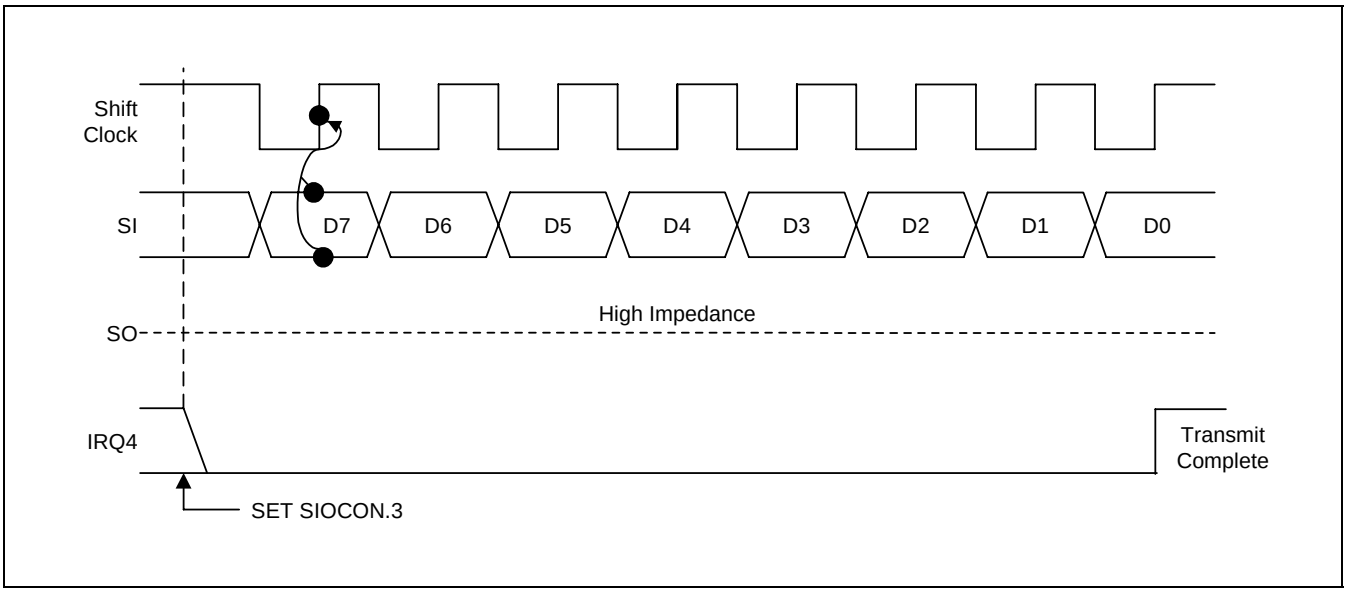


Figure 13-6. SIO Timing in Receive-Only Mode (Rising edge start)

☞ **PROGRAMMING TIP – Use Internal Clock to Transfer and Receive Serial Data**

1. The method that uses interrupt is used.

```
          •
          DI                              ;  Disable All interrupts
          LD        P2CONL #03H           ;  P2.2–P2.0 are selected to alternative function for
                                          ;  SI, SO, SCK, respectively

          SB1
          LD        SIODATA, TDATA        ;  Load Tx data to SIO buffer
          LD        SIOPS, #90H           ;  Baud rate = input clock (fxx)/[(144 + 1) x 4]
          LD        SIOCON, #2EH          ;  Internal clock, MSB first, transmit/receive mode
          SB0                             ;  Select falling edges to start shift operation
                                          ;  Clear 3-bit counter and start shifting
                                          ;  Enable shifter and clock counter
                                          ;  Enable SIO interrupt and clear pending
          EI
          •
SIOINT    PUSH      RP0                   ;
          SRP0      #RDATA                ;
          SB1
          LD        R0, SIODATA           ;  Load received data to general register
          OR        SIOCON, #08H          ;  SIO restart
          AND       SIOCON,#11111110b     ;  Clear interrupt pending bit
          SB0
          POP       RP0
          IRET
```

☞ **PROGRAMMING TIP – Use Internal Clock to Transfer and Receive Serial Data (Continued)**

2. The method that uses software pending check is used.

```
                •
                •
                •
                DI                              ;  Disable All interrupts

                SB1
                LD      SUSR, #00H              ;  Select SIO interface module
                LD      SIODATA, TDATA          ;  Load Tx data to SIO buffer
                LD      SIOPS, #90H             ;  Baud rate = input clock(fxx)/[(144 + 1) × 4]
                LD      SIOCON, #2CH            ;  Internal clock, MSB first, transmit/receive mode
                                                ;  Select falling edges to start shift operation
                                                ;  clear 3-bit counter and start shifting
                                                ;  Disable SIO interrupt
                EI

SIOtest:        LD      R6, SIOCON              ;  To check whether transmit and receive is finished
                BTJRF   SIOtest,R6.0            ;  Check pending bit
                NOP
                AND     SIOCON,#0FEH            ;  Pending clear by software
                LD      RDATA,SIODATA           ;  Load received data to RDATA
                •
                •
                •
                SB0
                •
                •
                •
```

14 UART(0,1)

OVERVIEW

The UART block has a full-duplex serial port with programmable operating modes: There is one synchronous mode and three UART (Universal Asynchronous Receiver/Transmitter) modes:

- Serial I/O with baud rate of fxx/(16 × (16bit BRDATA+1))
- 8-bit UART mode; variable baud rate, fxx/(16 × (16bit BRDATA+1))
- 9-bit UART mode; variable baud rate, fxx/(16 × (16bit BRDATA+1))
- 9-bit UART mode, variable baud rate, fxx/(16 × (16bit BRDATA+1))

UART receive and transmit buffers are both accessed via the data register, UDATA0, is set 1, bank 1 at address E2H, UDATA1, is set 1, bank 1 at address FAH. Writing to the UART data register loads the transmit buffer; reading the UART data register accesses a physically separate receive buffer.

When accessing a receive data buffer (shift register), reception of the next byte can begin before the previously received byte has been read from the receive register. However, if the first byte has not been read by the time the next byte has been completely received, the first data byte will be lost (Overrun error).

In all operating modes, transmission is started when any instruction (usually a write operation) uses the UDATA0, UDATA1 register as its destination address. In mode 0, serial data reception starts when the receive interrupt pending bit (UARTPND.1, UARTPND.3) is "0" and the receive enable bit (UARTCON0.4, UARTCON1.4) is "1". In mode 1, 2, and 3, reception starts whenever an incoming start bit ("0") is received and the receive enable bit (UARTCON0.4, UARTCON1.4) is set to "1".

PROGRAMMING PROCEDURE

To program the UART0 modules, follow these basic steps:

1. Configure P5.3 and P5.2 to alternative function (RxD0 (P5.3), TxD0 (P5.2)) for UART0 module by setting the P5CONL register to appropriatly value.
2. Load an 8-bit value to the UARTCON0 control register to properly configure the UART0 I/O module.
3. For parity generation and check in UART0 mode 2 or 3, set parity enable bit (UARTPND.5) to “1”.
4. For interrupt generation, set the UART0 interrupt enable bit (UARTCON0.1 or UARTCON0.0) to "1".
5. When you transmit data to the UART0 buffer, write transmit data to UDATA0, the shift operation starts.
6. When the shift operation (transmit/receive) is completed, UART0 pending bit (UARTPND.1 or UARTPND.0) is set to "1" and an UART0 interrupt request is generated.

UART CONTROL REGISTER (UARTCON0, UARTCON1)

The control register for the UART0 and UART1 is called UARTCON0 in set 1, bank 1 at address E3H, UARTCON1 in set 1, bank 1 at address FBH. It has the following control functions:

- Operating mode and baud rate selection
- Multiprocessor communication and interrupt control
- Serial receive enable/disable control
- 9th data bit location for transmit and receive operations (modes 2 and 3 only)
- Parity generation and check for transmit and receive operations (modes 2 and 3 only)
- UART transmit and receive interrupt control

A reset clears the UARTCON0, UARTCON1 value to "00H". So, if you want to use UART0, or UART1 module, you must write appropriate value to UARTCON0, UARTCON1.

UART Control Register
(UARTCON0) E3H, Set 1, Bank 1, R/W
(UARTCON1) FBH, Set 1, Bank 1, R/W

MSB	MS1	MS0	MCE	RE	TB8	RB8	RIE	TIE	LSB

Operating mode and
baud rate selection bits
(see table below)

Multiprocessor communication (1)
enable bit (for modes 2 and 3 only):
0 = Disable
1 = Enable

Serial data receive enable bit:
0 = Disable
1 = Enable

If parity disable mode (PEN0,1 = 0),
location of the 9th data bit to be transmitted in
UART mode 2 or 3 ("0" or "1").

If parity enable mode (PEN0,1 = 1),
Even/odd parity selection bit for transmit data in
UART mode 2 or 3;
0 : Even parity bit generation for transmit data
1 : Odd parity bit generation for transmit data

Transmit interrupt enable bit:
0 = Disable
1 = Enable

Received interrupt enable bit:
0 = Disable
1 = Enable

If parity disable mode (PEN0,1 = 0),
location of the 9th data bit that was received in
UART mode 2 or 3 ("0" or "1").

If parity enable mode (PEN0,1 = 1),
Even/odd parity selection bit for receive data in
UART mode 2 or 3.
0 : Even parity check for the received data
1 : Odd parity check for the received data

MS1	MS0	Mode	Description (2)	Baud Rate
0	0	0	Shift register	fxx / (16 x (16bit BRDATA + 1))
0	1	1	8-bit UART	fxx / (16 x (16bit BRDATA + 1))
1	0	2	9-bit UART	fxx / (16 x (16bit BRDATA + 1))
1	1	3	9-bit UART	fxx / (16 x (16bit BRDATA + 1))

NOTES:

1. In mode 2 or 3, if the UARTCON.5 bit is set to "1" then the receive interrupt will not be activated if the received 9th data bit is "0". In mode 1, if UARTCON.5 = "1" then the receive interrut will not be activated if a valid stop bit was not received.
2. The descriptions for 8-bit and 9-bit UART mode do not include start and stop bits for serial data receive and transmit.
3. Parity enable bits, PEN0 and PEN1, are located in the UARTPND register at address FCH, Bank 1.
4. Parity enable and parity error check can be available in 9-bit UART mode (Mode 2, 3) only.

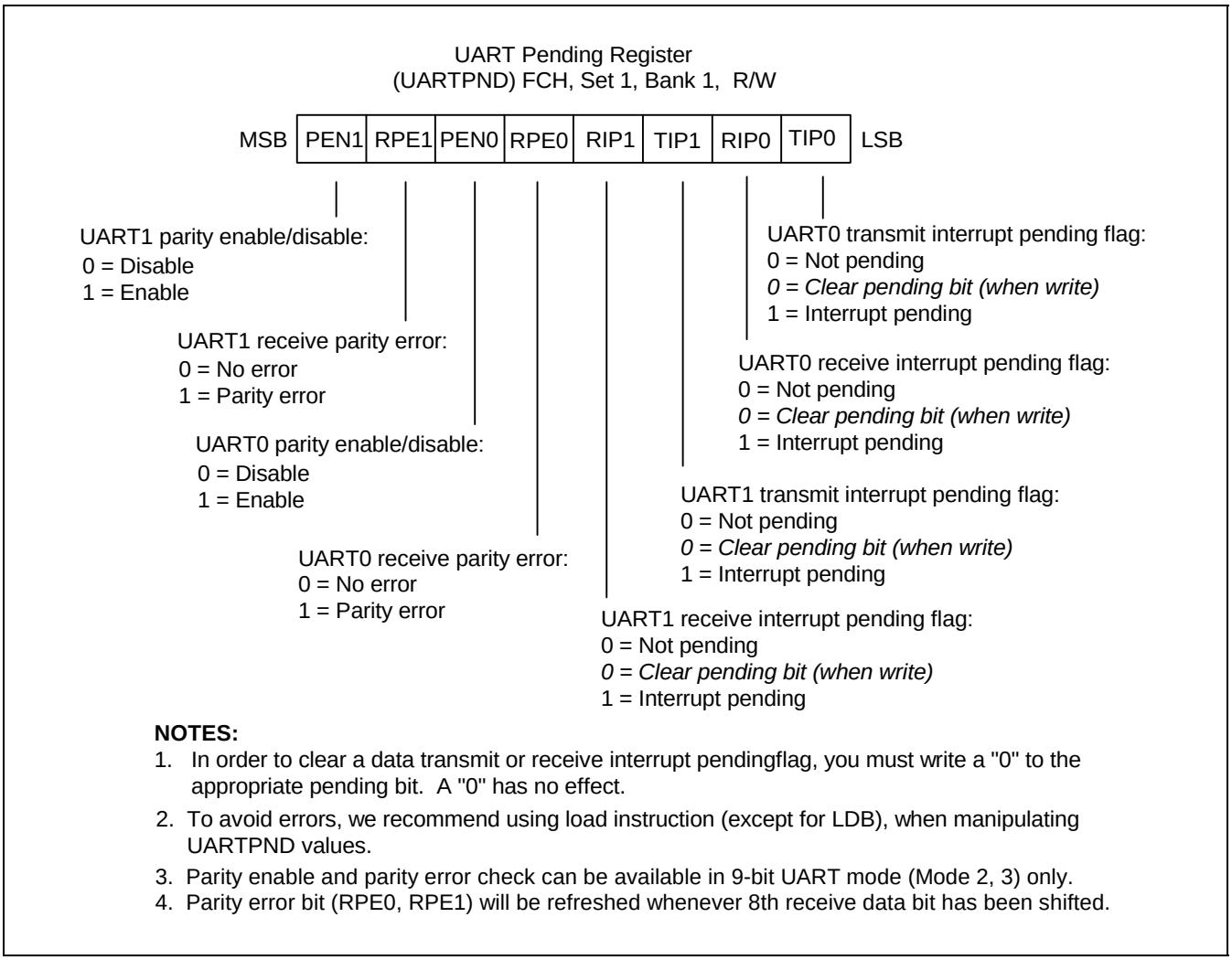
Figure 14-1. UART Control Register (UARTCON0, UARTCON1)

UART INTERRUPT PENDING REGISTER (UARTPND)

The UART0 and UART1 interrupt pending register, UARTPND is located in set 1, bank 1 at address FCH. It contains the UART0 data transmit interrupt pending bit (UARTPND.0) and the receive interrupt pending bit (UARTPND.1), the UART1 data transmit interrupt pending bit (UARTPND.2) and the receive interrupt pending bit (UARTPND.3).

In mode 0 of the UART module, the receive interrupt pending flag UARTPND.1, UARTPND.3 is set to "1" when the 8th receive data bit has been shifted. In mode 1, 2, and 3, the UARTPND.1, UARTPND.3 bit is set to "1" at the halfway point of the stop bit's shift time. When the CPU has acknowledged the receive interrupt pending condition, the UARTPND.1, UARTPND.3 flag must then be cleared by software in the interrupt service routine.

In mode 0 of the UART module, the transmit interrupt pending flag UARTPND.0, UARTPND.2 is set to "1" when the 8th transmit data bit has been shifted. In mode 1, 2, or 3, the UARTPND.0, UARTPND.2 bit is set at the start of the stop bit. When the CPU has acknowledged the transmit interrupt pending condition, the UARTPND.0, UARTPND.2 flag must then be cleared by software in the interrupt service routine.



NOTES:

1. In order to clear a data transmit or receive interrupt pendingflag, you must write a "0" to the appropriate pending bit. A "0" has no effect.
2. To avoid errors, we recommend using load instruction (except for LDB), when manipulating UARTPND values.
3. Parity enable and parity error check can be available in 9-bit UART mode (Mode 2, 3) only.
4. Parity error bit (RPE0, RPE1) will be refreshed whenever 8th receive data bit has been shifted.

Figure 14-2. UART Interrupt Pending Register (UARTPND)

In mode 2 and 3 (9-bit UART data), by setting the parity enable bit (PEN0, PEN1) of UARTPND register to '1', the 9th data bit of transmit data will be an automatically generated parity bit. Also, the 9th data bit of the received data will be treated as a parity bit for checking the received data.

In parity enable mode (PEN0 = 1), UARTCON0.3 (TB8) and UARTCON0.2 (RB8) will be a parity selection bit for transmit and receive data respectively. The UARTCON0.3 (TB8) is for settings of the even parity generation (TB8 = 0) or the odd parity generation (TB8 = 0) in the transmit mode. The UARTCON0.2 (RB8) is also for settings of the even parity checking (RB8= 0) or the odd parity checking (RB8 =1) in the receive mode. The parity enable (generation/checking) functions are not available in UART mode 0 and 1.

If you don't want to use a parity mode, UARTCON0.2 (RB8) and UARTCON0.3 (TB8) are a normal control bit as the 9th data bit, in this case, PEN0 (UART0) and PEN1 (UART1) must be disable ("0") in mode 2 and 3. Also it is needed to select the 9th data bit to be transmitted by writing TB8 to "0" or "1".

The receive parity error flag (RPE0, RPE1) will be set to '0' or '1' depending on parity error whenever the 8th data bit of the receive data has been shifted.

UART DATA REGISTER (UDATA0, UDATA1)

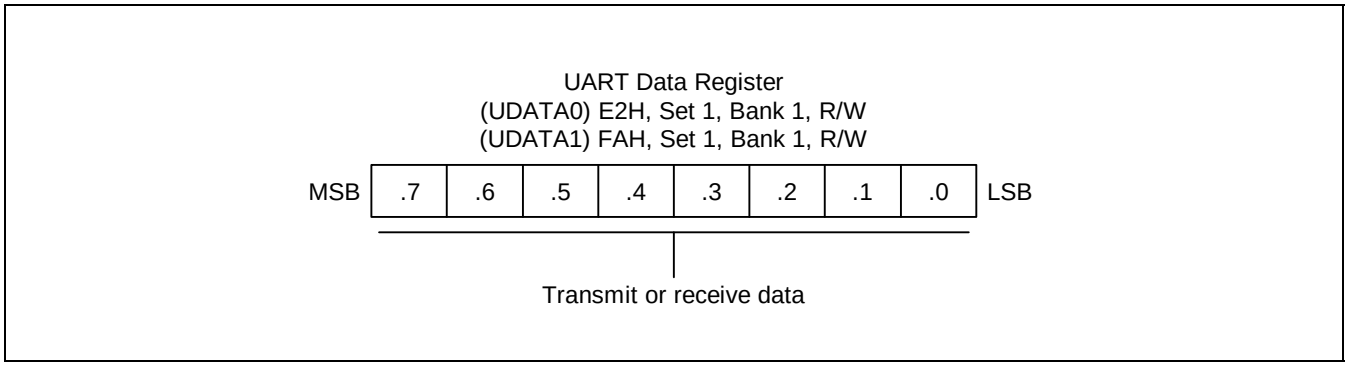


Figure 14-3. UART Data Register (UDATA0, UDATA1)

UART BAUD RATE DATA REGISTER (BRDATAH0, BRDATAL0, BRDATAH1, BRDATAL1)

The value stored in the UART0 baud rate register, (BRDATAH0, BRDATAL0), lets you determine the UART0 clock rate (baud rate). The value stored in the UART1 baud rate register, (BRDATAH1, BRDATAL1), lets you determine the UART1 clock rate (baud rate).

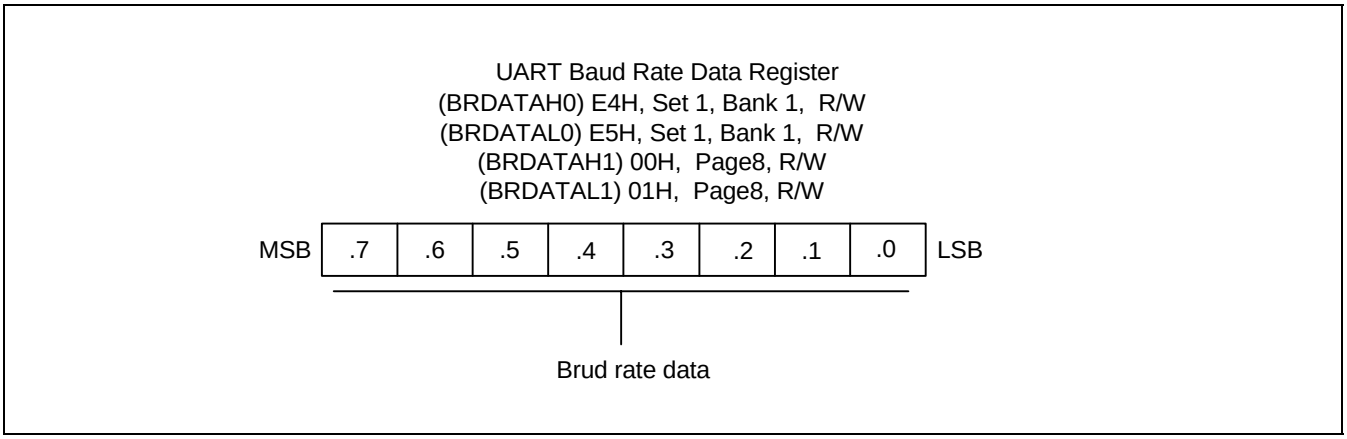


Figure 14-4. UART Baud Rate Data Register (BRDATAH0, BRDATAL0, BRDATAH1, BRDATAL1)

BAUD RATE CALCULATIONS

Mode 0 Baud Rate Calculation

In mode 0, the baud rate is determined by the baud rate data register, 16bit BRDATA

Mode 0 baud rate = fxx/(16 × (16Bit BRDATA + 1))

Mode 2 Baud Rate Calculation

In mode 2, the baud rate is determined by the baud rate data register, 16bit BRDATA

Mode 2 baud rate = fxx/(16 × (16Bit BRDATA + 1))

Modes 1 and 3 Baud Rate Calculation

In modes 1 and 3, the baud rate is determined by the baud rate data register, 16bit BRDATA

Mode 1 and 3 baud rate = fxx/(16 × (16Bit BRDATA + 1))

Table 14-1. Commonly Used Baud Rates Generated by BRDATA0, BRDATA1

Baud Rate	Oscillation Clock	BRDATAH0(1)		BRDATAL0(1)	
		Decimal	Hex	Decimal	Hex
76,800 Hz	10 MHz	0	0H	7	7H
38,400 Hz	10 MHz	0	0H	15	FH
19,200 Hz	10 MHz	0	0H	31	1FH
9,600 Hz	10 MHz	0	0H	64	40H
4,800 Hz	10 MHz	0	0H	129	81H
2,400 Hz	10 MHz	1	1H	3	3H
600 Hz	10 MHz	4	4H	16	10H
38,461 Hz	8 MHz	0	0H	12	0CH
12,500 Hz	8 MHz	0	0H	39	27H
19,230 Hz	4 MHz	0	0H	12	0CH
9,615 Hz	4 MHz	0	0H	25	19H

BLOCK DIAGRAM

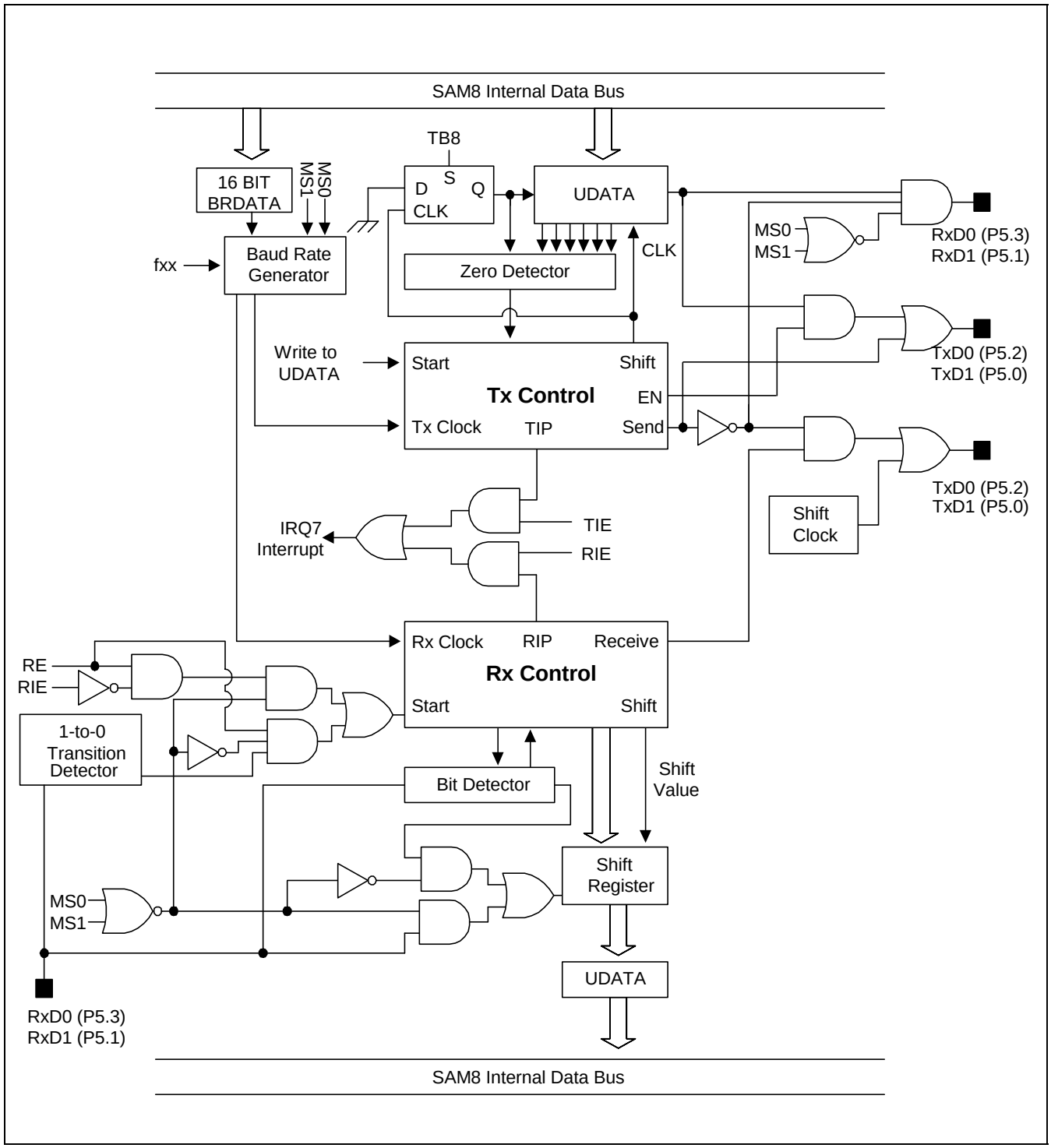


Figure 14-5. UART Functional Block Diagram

UART MODE 0 FUNCTION DESCRIPTION

In mode 0, UART0 is input and output through the RxD0 (P5.3) pin and TxD0 (P5.2) pin outputs the shift clock. Data is transmitted or received in 8-bit units only. The LSB of the 8-bit value is transmitted (or received) first.

Mode 0 Transmit Procedure

1. Select mode 0 by setting UARTCON0.6 and .7 to "00B".
2. Write transmission data to the shift register UDATA0 (E2H, set 1, bank 1) to start the transmission operation.

Mode 0 Receive Procedure

1. Select mode 0 by setting UATCON0.6 and .7 to "00B".
2. Clear the receive interrupt pending bit (UARTPND.1) by writing a "0" to UARTPND.1.
3. Set the UART0 receive enable bit (UARTCON0.4) to "1".
4. The shift clock will now be output to the TxD0 (P5.2) pin and will read the data at the RxD0 (P5.3) pin. A UART0 receive interrupt (IRQ7, vector F0H) occurs when UARTCON0.1 is set to "1".

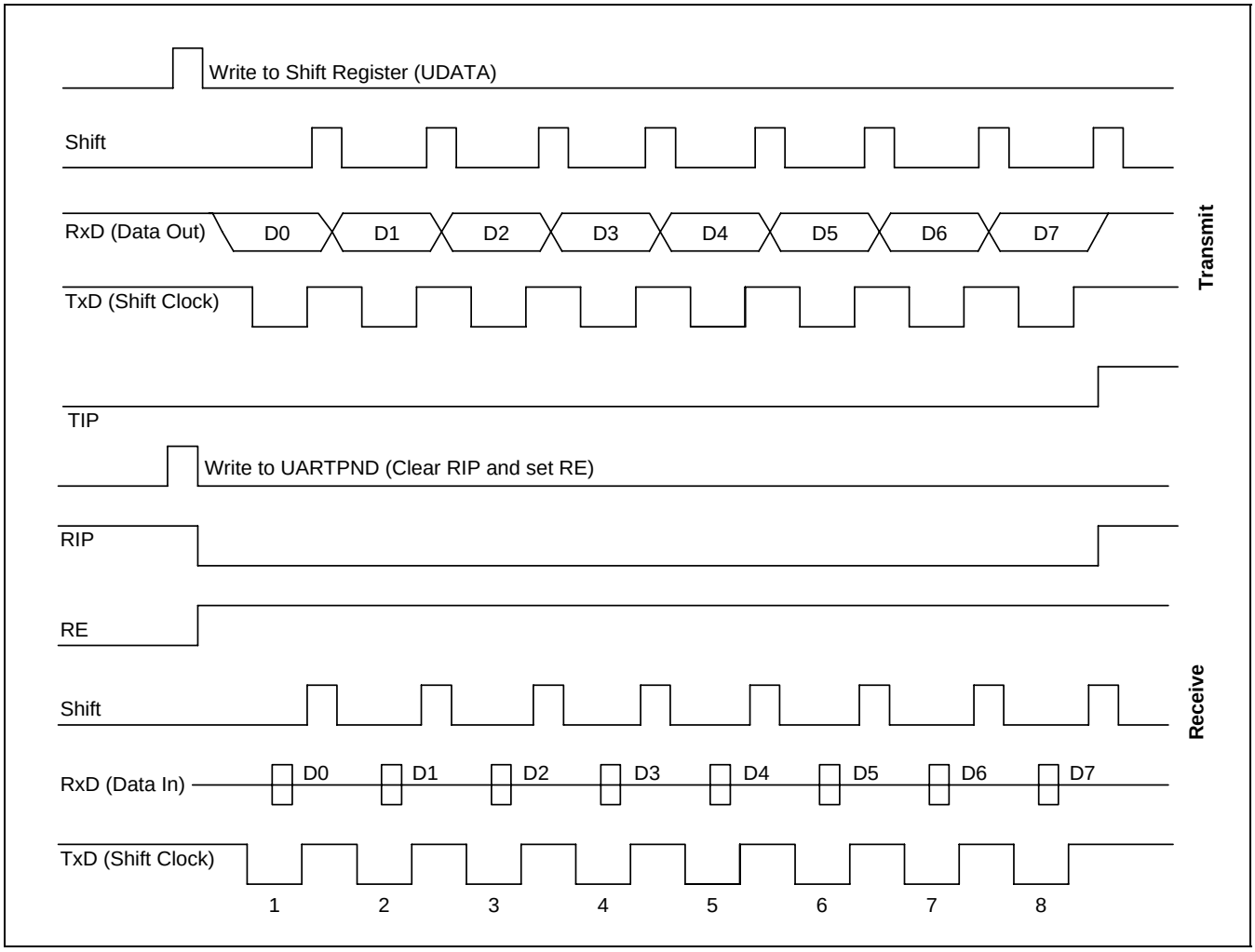


Figure 14-6. Timing Diagram for UART Mode 0 Operation

UART MODE 1 FUNCTION DESCRIPTION

In mode 1, 10-bits are transmitted (through the TxD0 (P5.2) pin) or received (through the RxD0 (P5.3) pin). Each data frame has three components:

- Start bit ("0")
- 8 data bits (LSB first)
- Stop bit ("1")

When receiving, the stop bit is written to the RB8 bit in the UARTCON0 register. The baud rate for mode 1 is variable.

Mode 1 Transmit Procedure

1. Select the baud rate generated by 16bit BRDATA.
2. Select mode 1 (8-bit UART0) by setting UARTCON0 bits 7 and 6 to '01B'.
3. Write transmission data to the shift register UDATA0 (E2H, set 1, bank 1). The start and stop bits are generated automatically by hardware.

Mode 1 Receive Procedure

1. Select the baud rate to be generated by 16bit BRDATA.
2. Select mode 1 and set the RE (Receive Enable) bit in the UARTCON0 register to "1".
3. The start bit low ("0") condition at the RxD0 (P5.3) pin will cause the UART0 module to start the serial data receive operation.

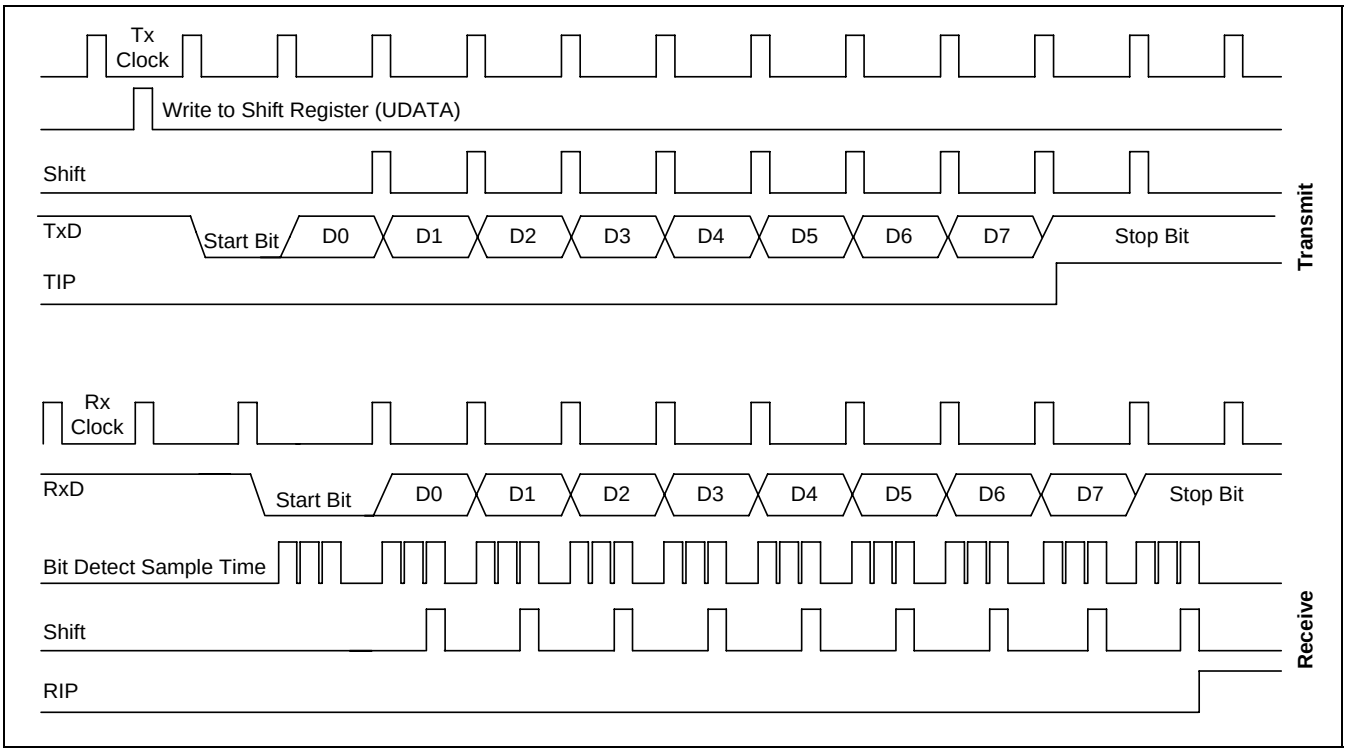


Figure 14-7. Timing Diagram for UART Mode 1 Operation

UART MODE 2 FUNCTION DESCRIPTION

In mode 2, 11-bits are transmitted (through the TxD0 pin) or received (through the RxD0 pin). Each data frame has four components:

- Start bit ("0")
- 8 data bits (LSB first)
- Programmable 9th data bit or parity bit
- Stop bit ("1")

< In parity disable mode (PEN0 = 0 or PEN1 = 0) >

The 9th data bit to be transmitted can be assigned a value of "0" or "1" by writing the TB8 bit (UARTCON0.3). When receiving, the 9th data bit that is received is written to the RB8 bit (UARTCON0.2), while the stop bit is ignored. The baud rate for mode 2 & 3 is fosc/(16 x (16bit BRDATA + 1)) clock frequency.

< In parity enable mode (PEN0 = 1 or PEN1 = 1) >

The 9th data bit to be transmitted can be an automatically generated parity of "0" or "1" depending on a parity generation by means of TB8 bit (UARTCON0.3). When receiving, the received 9th data bit is treated as a parity for checking receive data by means of the RB8 bit (UARTCON0.2), while the stop bit is ignored. The baud rate for mode 2 & 3 is fosc/(16 x (16bit BRDATA + 1)) clock frequency.

Mode 2 & 3 Transmit Procedure

1. Select the baud rate generated by 16bit BRDATA.
2. Select mode 2 & 3 (9-bit UART0) by setting UARTCON0 bits 6 and 7 to '10B'. Also, select the 9th data bit to be transmitted by writing TB8 to "0" or "1" and set PEN0, PEN1 bit of UARTPND register to “0” if you don’t use a parity mode.
   If you want to use the parity enable mode, select the parity bit to be transmitted by writing TB8 to "0" or "1" and set PEN0, PEN1 bit of UARTPND register to “1”.
3. Write transmission data to the shift register, UDATA0 (E2H, set 1, bank 1), to start the transmit operation.

Mode 2 & 3 Receive Procedure

1. Select the baud rate to be generated by 16bit BRDATA.
2. Select mode 2 & 3 and set the receive enable bit (RE) in the UARTCON0 register to "1".
3. If you don’t use a parity mode, set PEN0, PEN1 bit of UARTPND register to “0” to disable parity mode.
   If you want to use the parity enable mode, select the parity type to be check by writing TB8 to "0" or "1" and set PEN0, PEN1 bit of UARTPND register to “1”. Only 8 bits (Bit0 to Bit7) of received data are available for data value.
4. The receive operation starts when the signal at the RxD pin goes to low level.

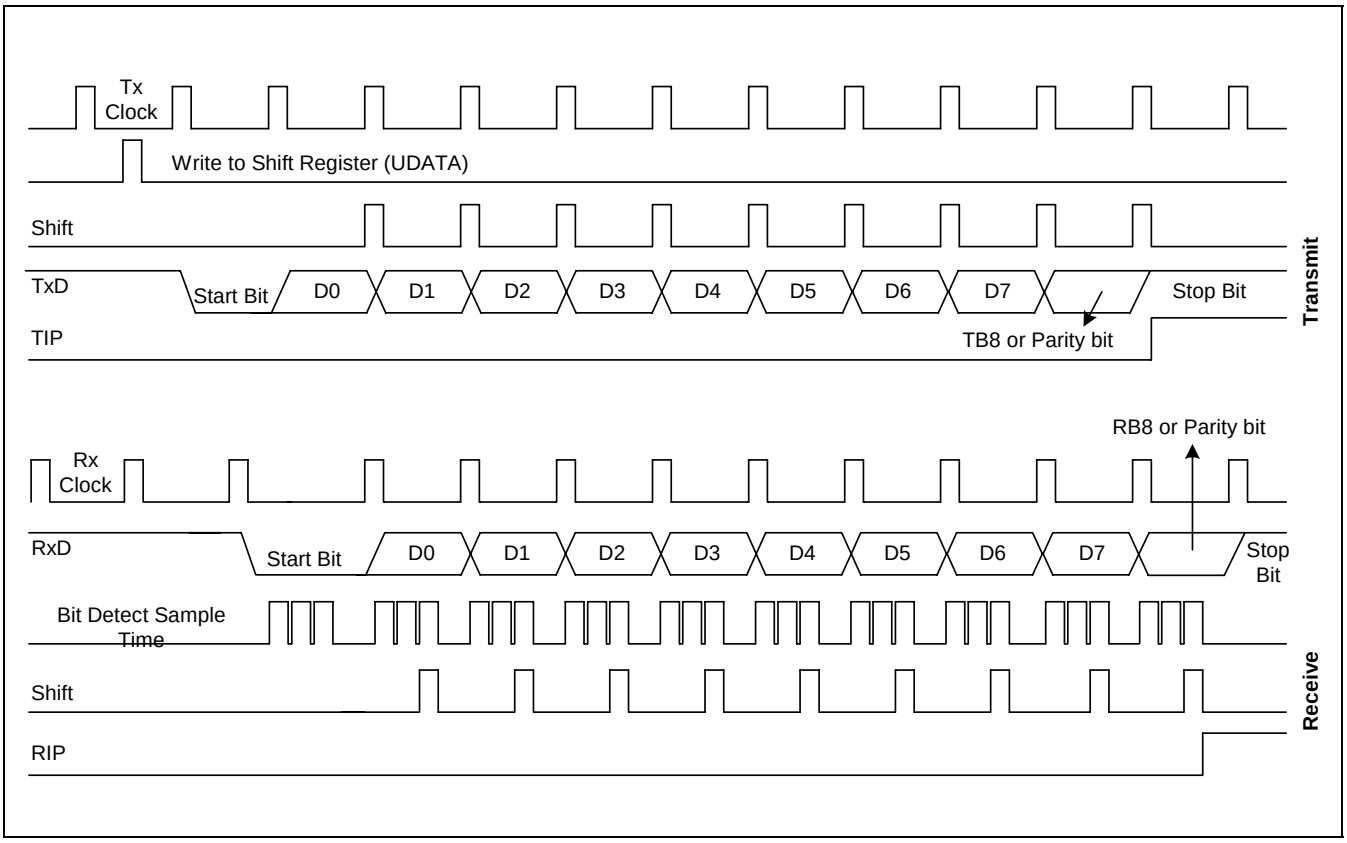


Figure 14-8. Timing Diagram for UART Mode 2 & 3 Operation

SERIAL COMMUNICATION FOR MULTIPROCESSOR CONFIGURATIONS

The S3C8-series multiprocessor communication features let a "master" S3F84NB send a multiple-frame serial message to a "slave" device in a multi- S3F84NB configuration. It does this without interrupting other slave devices that may be on the same serial line.

This feature can be used only in UART modes 2 or 3 with the parity disable mode. In these modes 2 and 3, 9 data bits are received. The 9th bit value is written to RB8 (UARTCON0.2 or UARTCON1.2). The data receive operation is concluded with a stop bit. You can program this function so that when the stop bit is received, the serial interrupt will be generated only if RB8 = "1".

To enable this feature, you set the MCE bit in the UARTCON registers. When the MCE bit is "1", serial data frames that are received with the 9th bit = "0" do not generate an interrupt. In this case, the 9th bit simply separates the address from the serial data.

Sample Protocol for Master/Slave Interaction

When the master device wants to transmit a block of data to one of several slaves on a serial line, it first sends out an address byte to identify the target slave. Note that in this case, an address byte differs from a data byte: In an address byte, the 9th bit is "1" and in a data byte, it is "0".

The address byte interrupts all slaves so that each slave can examine the received byte and see if it is being addressed. The addressed slave then clears its MCE bit and prepares to receive incoming data bytes.

The MCE bits of slaves that were not addressed remain set, and they continue operating normally while ignoring the incoming data bytes.

While the MCE bit setting has no effect in mode 0, it can be used in mode 1 to check the validity of the stop bit. For mode 1 reception, if MCE is "1", the receive interrupt will be issue unless a valid stop bit is received.

Setup Procedure for Multiprocessor Communications

Follow these steps to configure multiprocessor communications:

1. Set all S3F84NB devices (masters and slaves) to UART mode 2 or 3 with parity disable.
2. Write the MCE bit of all the slave devices to "1".
3. The master device's transmission protocol is:
   - First byte: the address identifying the target slave device (9th bit = "1")
   - Next bytes: data (9th bit = "0")
4. When the target slave receives the first byte, all of the slaves are interrupted because the 9th data bit is "1". The targeted slave compares the address byte to its own address and then clears its MCE bit in order to receive incoming data. The other slaves continue operating normally.

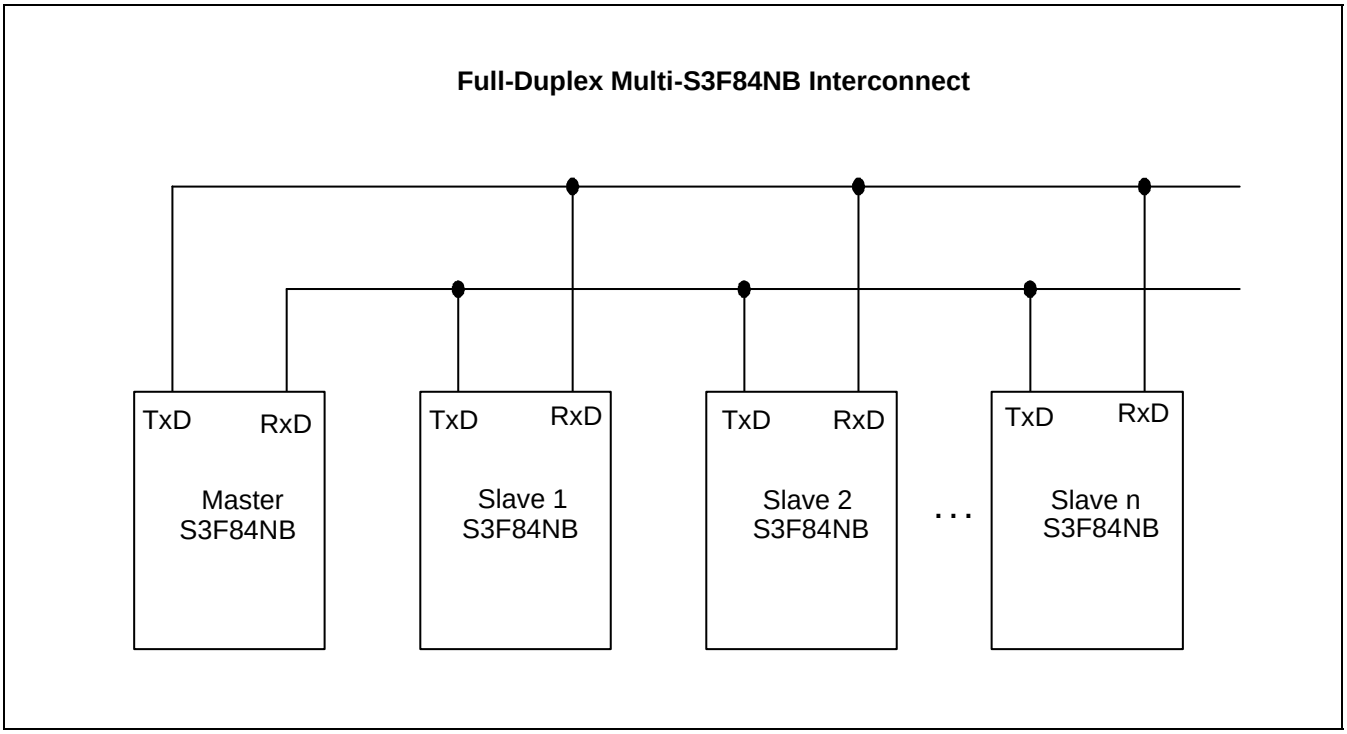


Figure 14-9. Connection Example for Multiprocessor Serial Data Communications

15 A/D CONVERTER

OVERVIEW

The 10-bit A/D converter (ADC) module uses successive approximation logic to convert analog levels entering at one of the eight input channels to equivalent 10-bit digital values. The analog input level must lie between the AV_{REF} and AV_{SS} values. The A/D converter has the following components:

- Analog comparator with successive approximation logic
- D/A converter logic (resistor string type)
- ADC control register, ADCON (set 1, bank 1, F7H, read/write, but ADCON.3 is read only)
- Eight multiplexed analog data input pins (ADC0–ADC7)
- 10-bit A/D conversion data output register (ADDATAH, ADDATAL)
- Internal AV_{REF} and AV_{SS}

FUNCTION DESCRIPTION

To initiate an analog-to-digital conversion procedure, at first, you must configure P1.0–P1.7 to analog input before A/D conversions because the P1.0–P1.7 pins can be used alternatively as normal data I/O or analog input pins. To do this, you load the appropriate value to the P1CONH, and P1CONL (for ADC0–ADC7) register.
And you write the channel selection data in the A/D converter control register ADCON to select one of the eight analog input pins (ADCn, n = 0–7) and set the conversion start or enable bit, ADCON.0. A 10-bit conversion operation can be performed for only one analog input channel at a time. The read-write ADCON register is located in set 1, bank 1 at address F7H.

During a normal conversion, ADC logic initially sets the successive approximation register to 200H (the approximate half-way point of an 10-bit register). This register is then updated automatically during each conversion step. The successive approximation block performs 10-bit conversions for one input channel at a time. You can dynamically select different channels by manipulating the channel selection bit value (ADCON.6-.4) in the ADCON register.

To start the A/D conversion, you should set the enable bit, ADCON.0. When a conversion is completed, ADCON.3, the end-of-conversion (EOC) bit is automatically set to 1 and the result is dumped into the ADDATAH, ADDATAL registers where it can be read. The ADC module enters an idle state. Remember to read the contents of ADDATAH and ADDATAL before another conversion starts. Otherwise, the previous result will be overwritten by the next conversion result.

NOTE

Because the ADC does not use sample-and-hold circuitry, it is important that any fluctuations in the analog level at the ADC0–ADC7 input pins during a conversion procedure be kept to an absolute minimum. Any change in the input level, perhaps due to circuit noise, will invalidate the result.

A/D CONVERTER CONTROL REGISTER (ADCON)

The A/D converter control register, ADCON, is located in set1, bank 1 at address F7H. ADCON is read-write addressable using 8-bit instructions only. But, the EOC bit, ADCON.3 is read only. ADCON has four functions:

- Bits 6–4 select an analog input pin (ADC0–ADC7).
- Bit 3 indicates the end of conversion status of the A/D conversion.
- Bits 2–1 select a conversion speed.
- Bit 0 starts the A/D conversion.

Only one analog input channel can be selected at a time. You can dynamically select any one of the eight analog input pins, ADC0–ADC7 by manipulating the 3-bit value for ADCON.6–ADCON.4

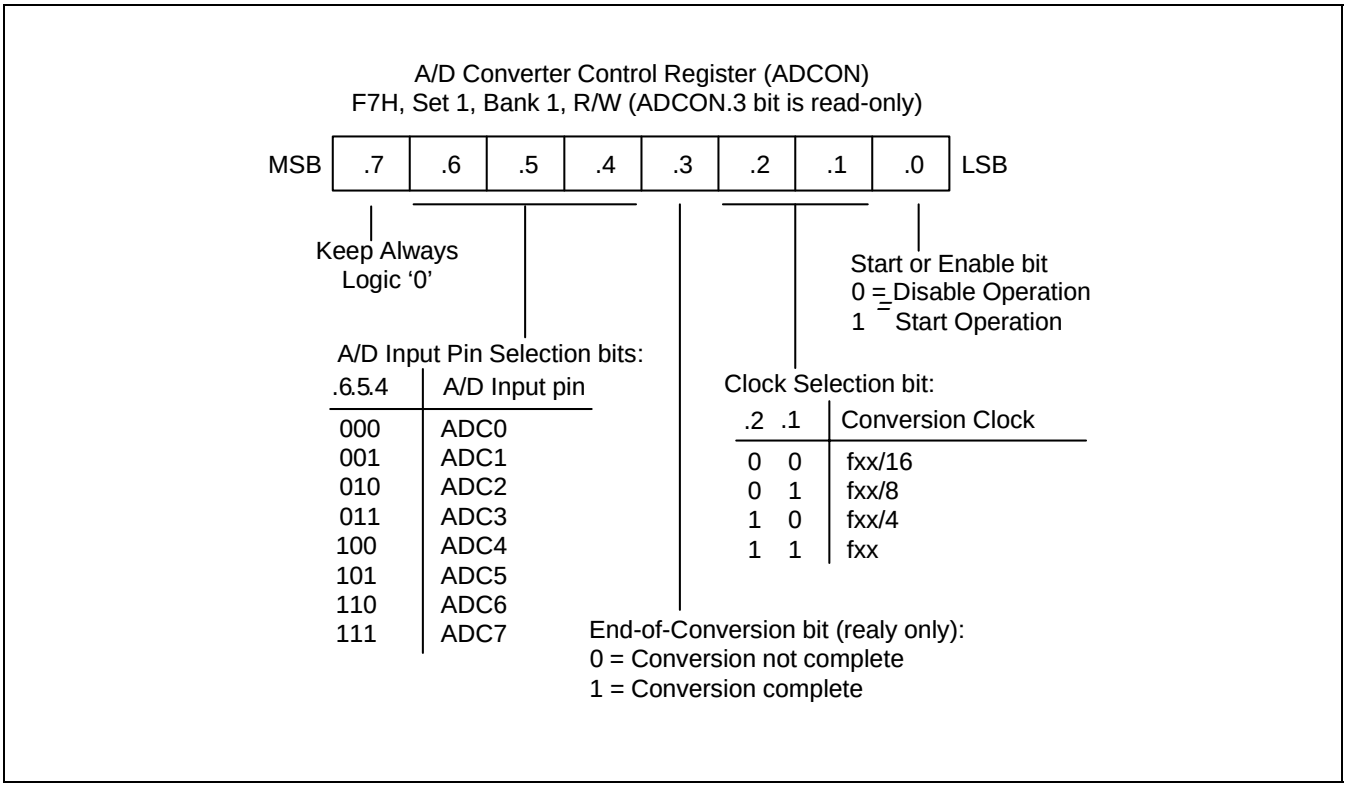


Figure 15-1. A/D Converter Control Register (ADCON)

Conversion Data Register High Byte (ADDATAH)
F8H, Set 1, Bank 1, Read only

MSB	.7	.6	.5	.4	.3	.2	.1	.0	LSB

Conversion Data Register Low Byte (ADDATAL)
F9H, Set 1, Bank 1, Read only

MSB	x	x	x	x	x	x	.1	.0	LSB

Figure 15-2. A/D Converter Data Register (ADDATAH, ADDATAL)

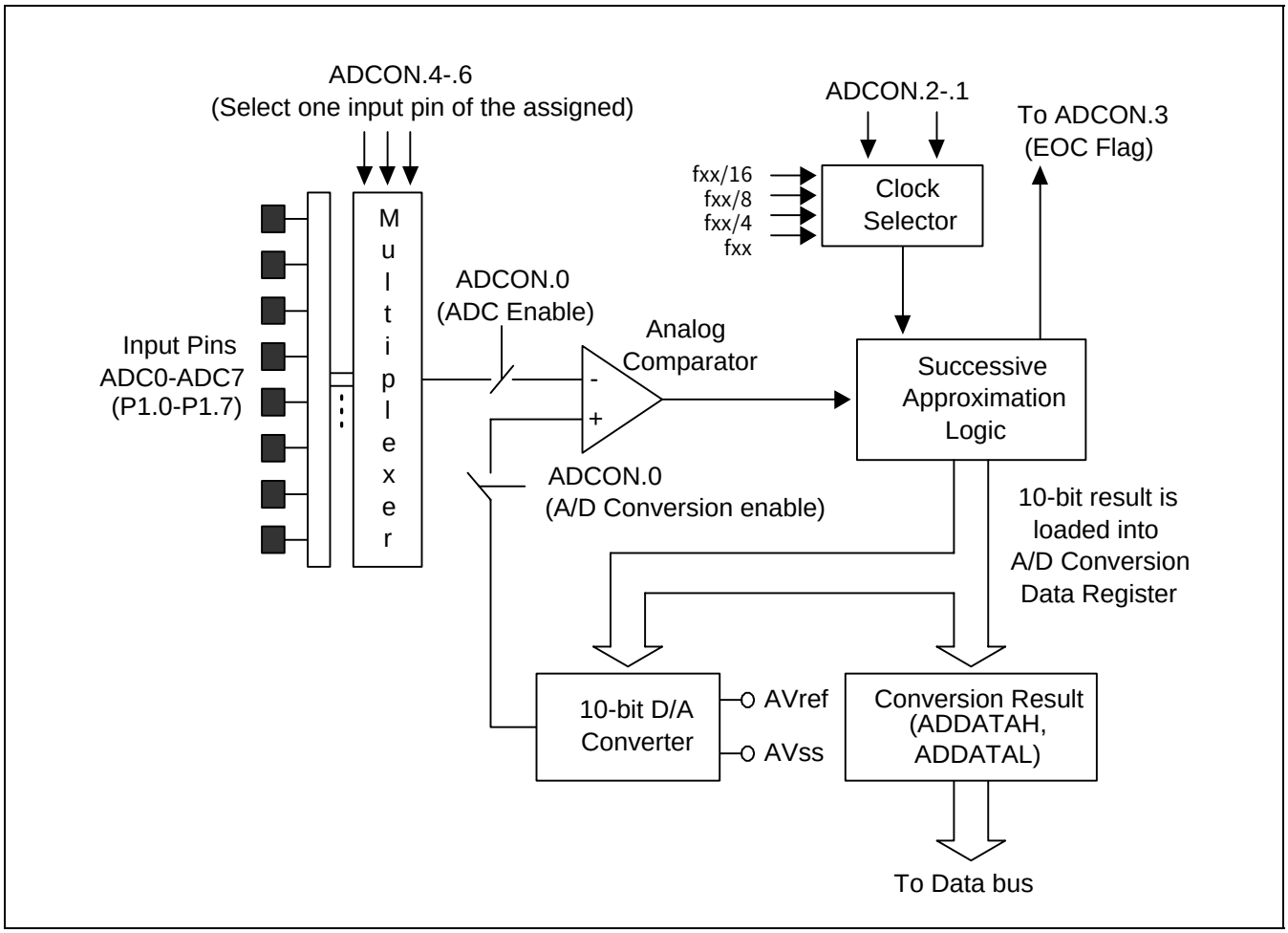


Figure 15-3. A/D Converter Circuit Diagram

INTERNAL REFERENCE VOLTAGE LEVELS

In the ADC function block, the analog input voltage level is compared to the reference voltage. The analog input level must remain within the range AV_{SS} to AV_{REF} (AV_{REF} = V_{DD}).

Different reference voltage levels are generated internally along the resistor tree during the analog conversion process for each conversion step. The reference voltage level for the first bit conversion is always 1/2 AV_{REF}.

CONVERSION TIMING

The A/D conversion process requires 4 steps (4 clock edges) to convert each bit and 10 clocks to step-up A/D conversion. Therefore, total of 50 clocks is required to complete a 10-bit conversion: With a 10 MHz CPU clock frequency, one clock cycle is 400 ns (4/fxx). If each bit conversion requires 4 clocks, the conversion rate is calculated as follows:

4 clocks/bit × 10-bits + step-up time (10 clock) = 50 clocks
50 clock × 400 ns = 20 μs at 10 MHz, 1 clock time = 4/fxx

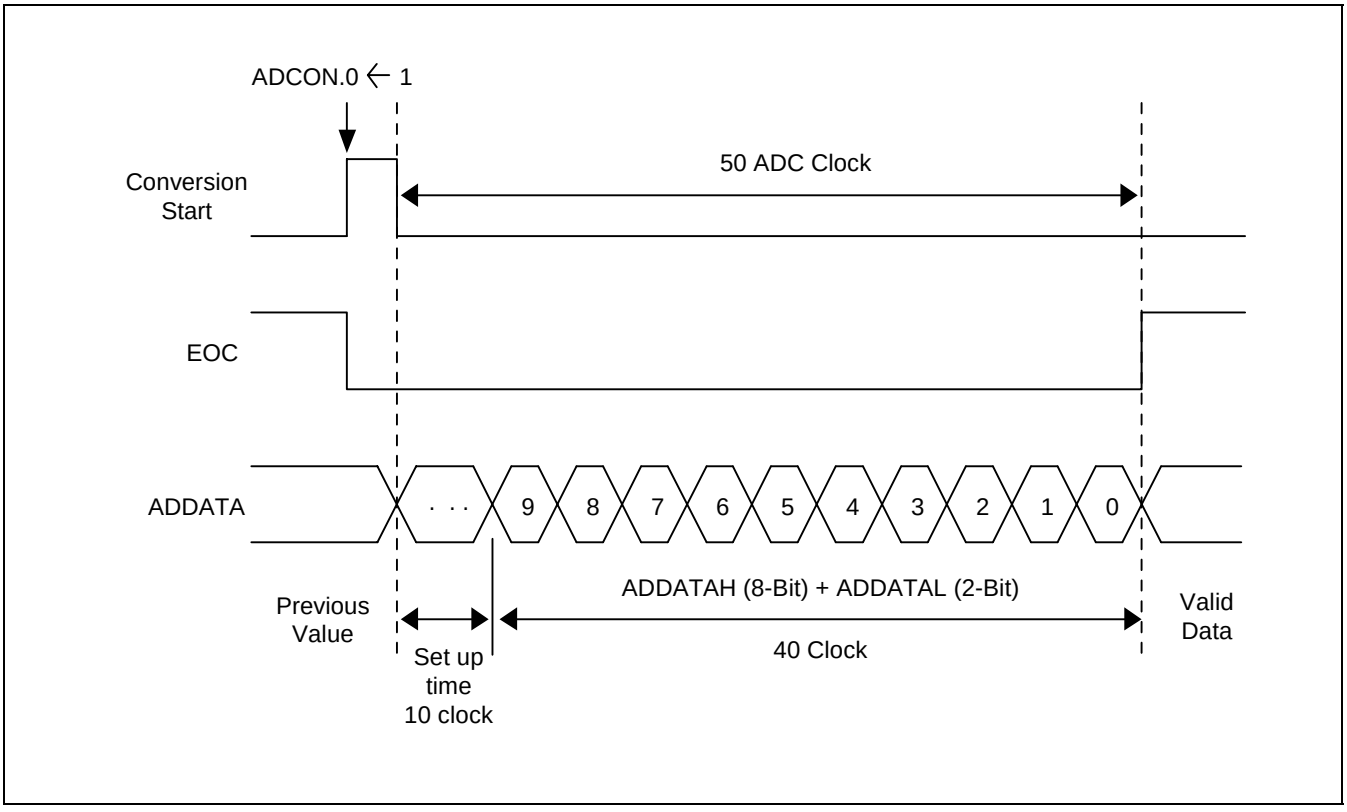
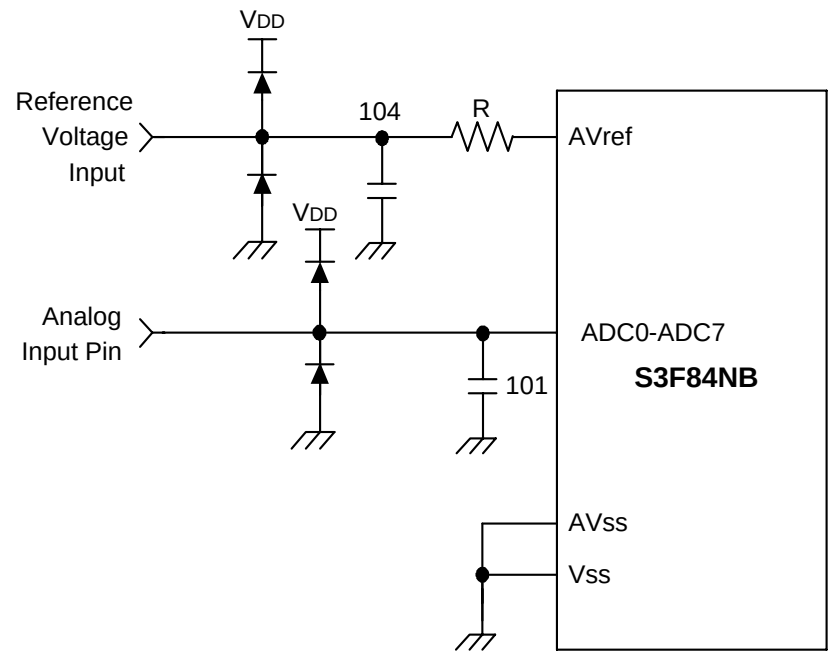


Figure 15-4. A/D Converter Timing Diagram

INTERNAL A/D CONVERSION PROCEDURE

1. Analog input must remain between the voltage range of AV_{SS} and AV_{REF}.
2. Configure P1.0–P1.7 for analog input before A/D conversions. To do this, you load the appropriate value to the P1CONH and P1CONL (for ADC0–ADC7) registers.
3. Before the conversion operation starts, you must first select one of the eight input pins (ADC0–ADC7) by writing the appropriate value to the ADCON register.
4. When conversion has been completed, (50 clocks have elapsed), the EOC, ADCON.3 flag is set to "1", so that a check can be made to verify that the conversion was successful.
5. The converted digital value is loaded to the output register, ADDATAH (8-bit) and ADDATAL (2-bit), then the ADC module enters an idle state.
6. The digital conversion result can now be read from the ADDATAH and ADDATAL register.



NOTE: The symbol "R" signifies an offset resistor with a value of from 50 to 100Ω
.

Figure 15-5. Recommended A/D Converter Circuit for Highest Absolute Accuracy

☞ PROGRAMMING TIP – Configuring A/D Converter

```
                •
                •
                SB0
                LD      P1CONH, #11111111B  ;  P1.7–P1.4 A/D Input MODE
                LD      P1CONL, #11111111B  ;  P1.3–P1.0 A/D Input MODE
                •
                •

                SB1
                LD      ADCON, #00000001B   ;  Channel ADC0, fxx, Conversion start
AD0_CHK:        TM      ADCON, #00001000B   ;  A/D conversion end ? → EOC check
                JR      Z, AD0_CHK          ;  No

                LD      AD0BUFH, ADDATAH    ;  8-bit Conversion data
                LD      AD0BUFL, ADDATAL    ;  2-bit Conversion data
                SB0
                •
                •

                SB1
                LD      ADCON, #00110001B   ;  Channel ADC3, fxx, Conversion start
AD3_CHK:        TM      ADCON, #00001000B   ;  A/D conversion end ? → EOC check
                JR      Z, AD3_CHK          ;  No

                LD      AD3BUFH, ADDATAH    ;  8-bit Conversion data
                LD      AD3BUFL, ADDATAL    ;  2-bit Conversion data
                SB0
                •
                •
```

16 WATCH TIMER

OVERVIEW

Watch timer functions include real-time and watch-time measurement and interval timing for the system clock. To start watch timer operation, set bit1 and bit 6 of the watch timer mode register, WTCON.1and 6, to “1”. After the watch timer starts and elapses a time, the watch timer interrupt is automatically set to “1”, and interrupt requests commence in 1.955 ms or 0.125, 0.25 and 0.5-second intervals.

The watch timer can generate a steady 0.5 kHz, 1 kHz, 2 kHz, or 4 kHz signal to the BUZZER output (BZOUT pin). By setting WTCON.3 and WTCON.2 to “11b”, the watch timer will function in high-speed mode, generating an interrupt every 1.955 ms. High-speed mode is useful for timing events for program debugging sequences.

Watch timer has the following functional components:

- Real-time and Watch-time measurement
- Using a main system or subsystem clock source
- Buzzer output frequency generator
- Timing tests in high-speed mode

WATCH TIMER CONTROL REGISTER (WTCON: R/W)

F5H	WTCON.7	WTCON.6	WTCON.5	WTCON.4	WTCON.3	WTCON.2	WTCON.1	WTCON.0
RESET	"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"

Table 16-1. Watch Timer Control Register (WTCON): Set 1, Bank 1, F5H, R/W

Bit Name	Values		Function	Address
WTCON.7	0		Select (fx/256) as the watch timer clock (fx: Main clock)	F5H
	1		Select subsystem clock as watch timer clock	
WTCON.6	0		Disable watch timer interrupt	
	1		Enable watch timer interrupt	
WTCON.5-.4	0	0	0.5 kHz buzzer (BZOUT) signal output	
	0	1	1 kHz buzzer (BZOUT) signal output	
	1	0	2 kHz buzzer (BZOUT) signal output	
	1	1	4 kHz buzzer (BZOUT) signal output	
WTCON.3-.2	0	0	Set watch timer interrupt to 0.5 s.	
	0	1	Set watch timer interrupt to 0.25 s.	
	1	0	Set watch timer interrupt to 0.125 s.	
	1	1	Set watch timer interrupt to 1.955 ms.	
WTCON.1	0		Disable watch timer, clear frequency dividing circuits	
	1		Enable watch timer	
WTCON.0	0		Interrupt is not pending, clear pending bit when write	
	1		Interrupt is pending	

NOTE: Main system clock frequency (fx) is assumed to be 8MHz

WATCH TIMER CIRCUIT DIAGRAM

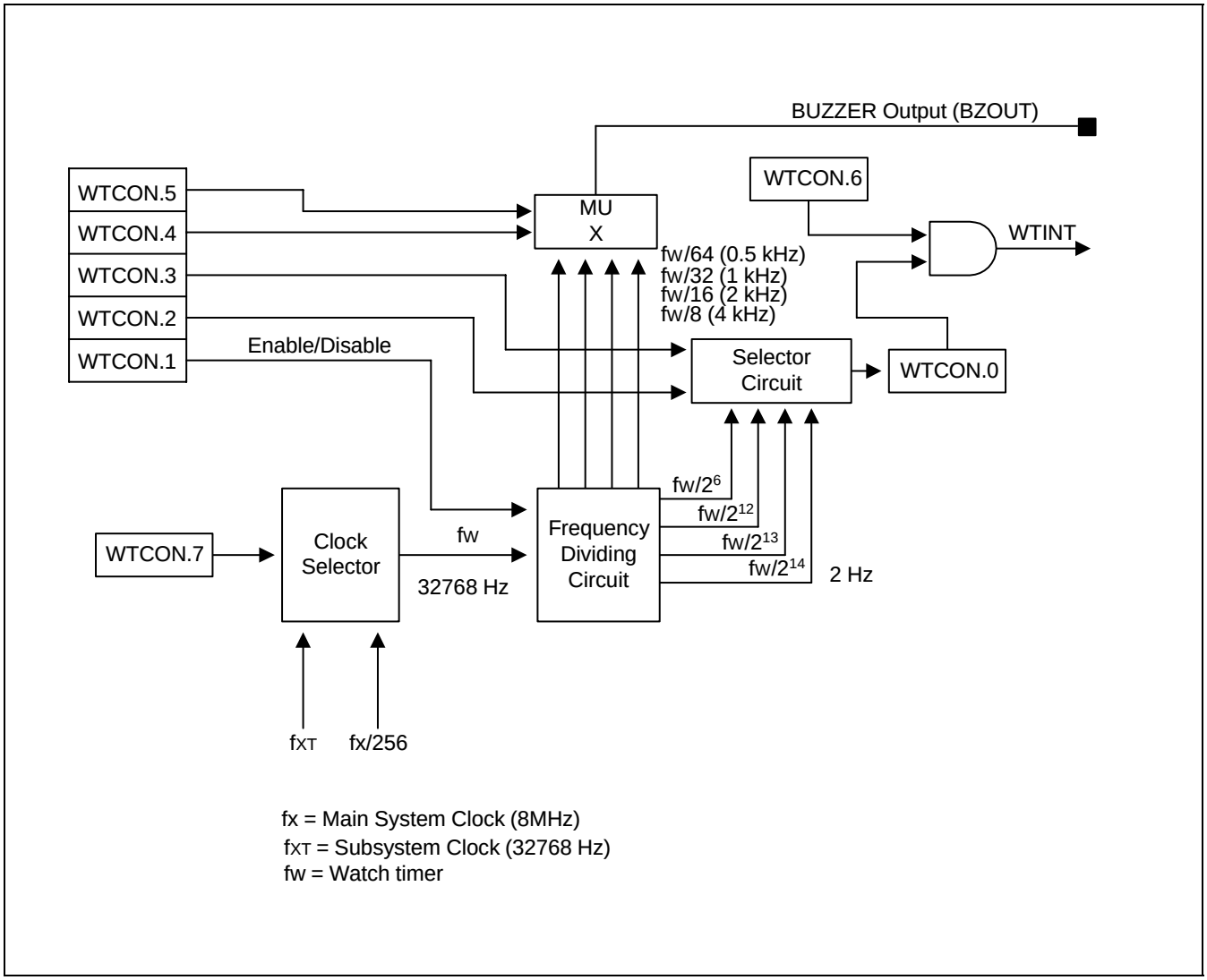


Figure 16-1. Watch Timer Circuit Diagram

☞ PROGRAMMING TIP – Using the Watch Timer

```
                ORG         0000h

                VECTOR      0D2h,WT_INT

                ORG         0100h

INITIAL:
                LD          SYM,#00h            ;  Disable Global/Fast interrupt
                LD          IMR,#00010000b      ;  Enable IRQ4 interrupt
                LD          SPH,#00000000b      ;  Set stack area
                LD          SPL,#0FFh
                LD          BTCON,#10100011b    ;  Disable Watch-dog
                SB1
                LD          WTCON,#11001110b    ;  0.5 kHz buzzer, 1.955ms duration interrupt
                                                ;  Interrupt enable, (fxt:32,768Hz)
                SB0
                EI

MAIN:
                •
                •
                •
                MAIN ROUTINE
                •
                •
                •

                JR          T, MAIN

WT_INT:
                •
                •
                •
                SB1
                AND         WTCON,#11111110b    ;  pending clear

                SB0
                IRET

                .END
```

17 PATTERN GENERATION MODULE

OVERVIEW

PATTERN GNERATION FLOW

You can output up to 8-bit through P0.0–P0.7 by tracing the following sequence. First of all, you have to change the PGDATA into what you want to output. And then you have to set the PGCON to enable the pattern generation module and select the triggering signal. From now, bits of PGDATA are on the P0.0–P0.7 whenever the selected triggering signal occurs.

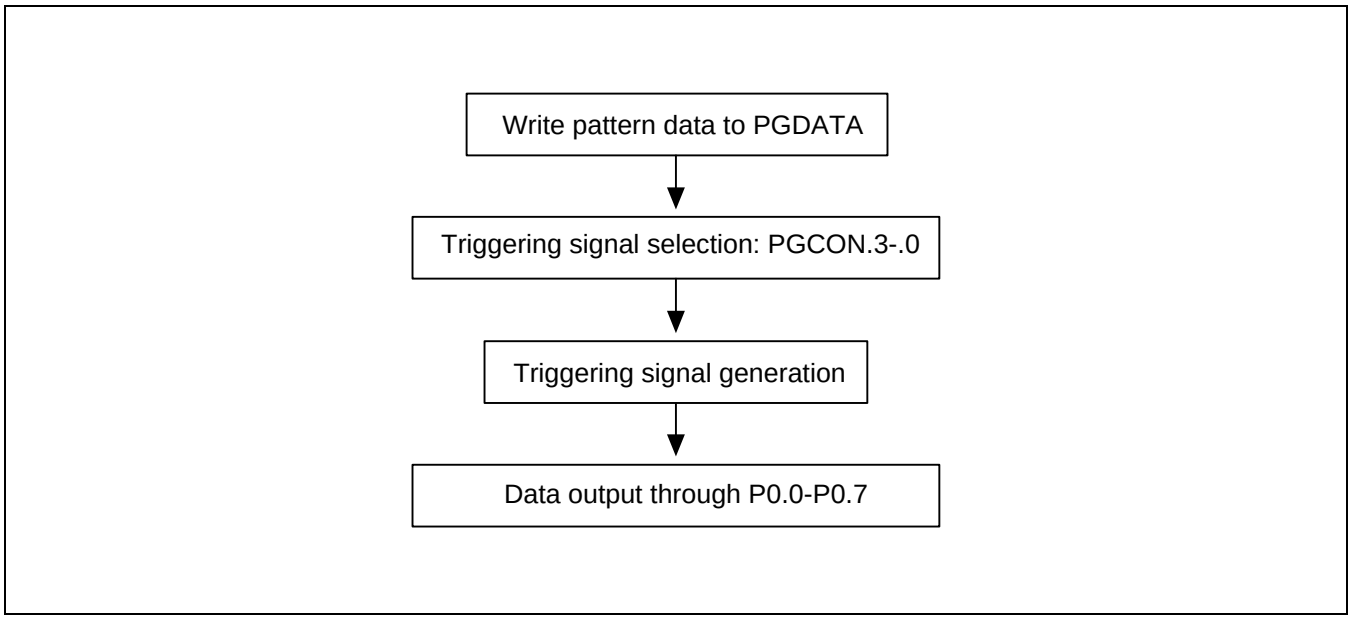


Figure 17-1. Pattern Generation Flow

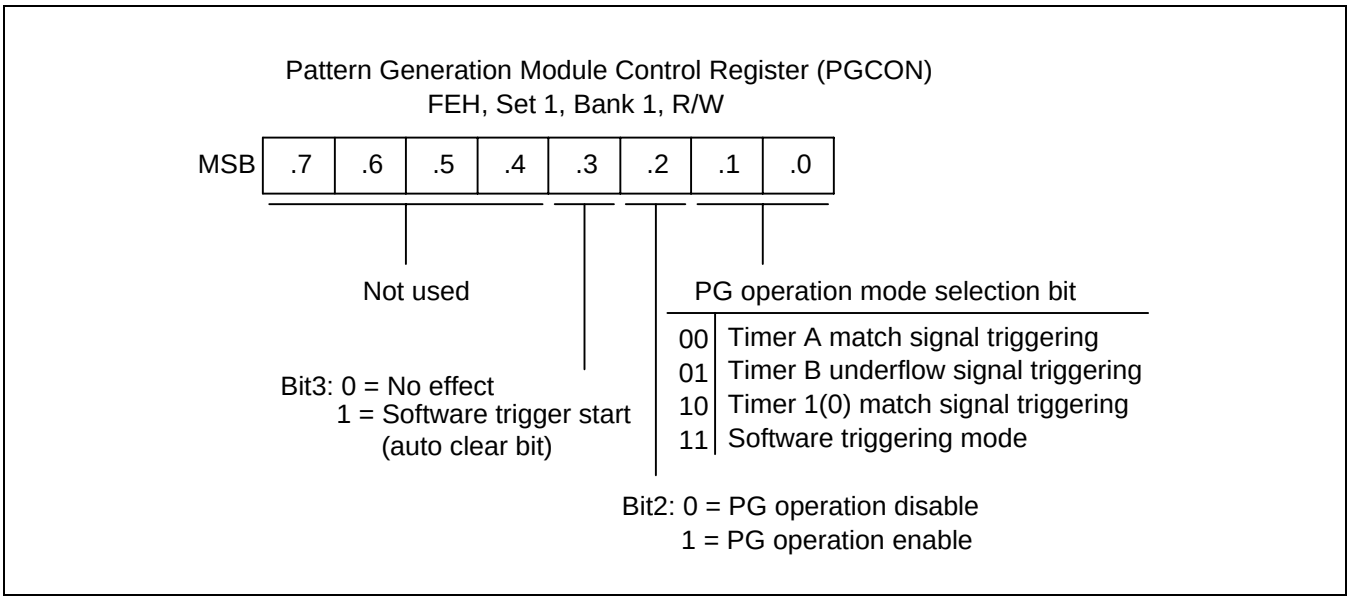


Figure 17-2. PG Control Register (PGCON)

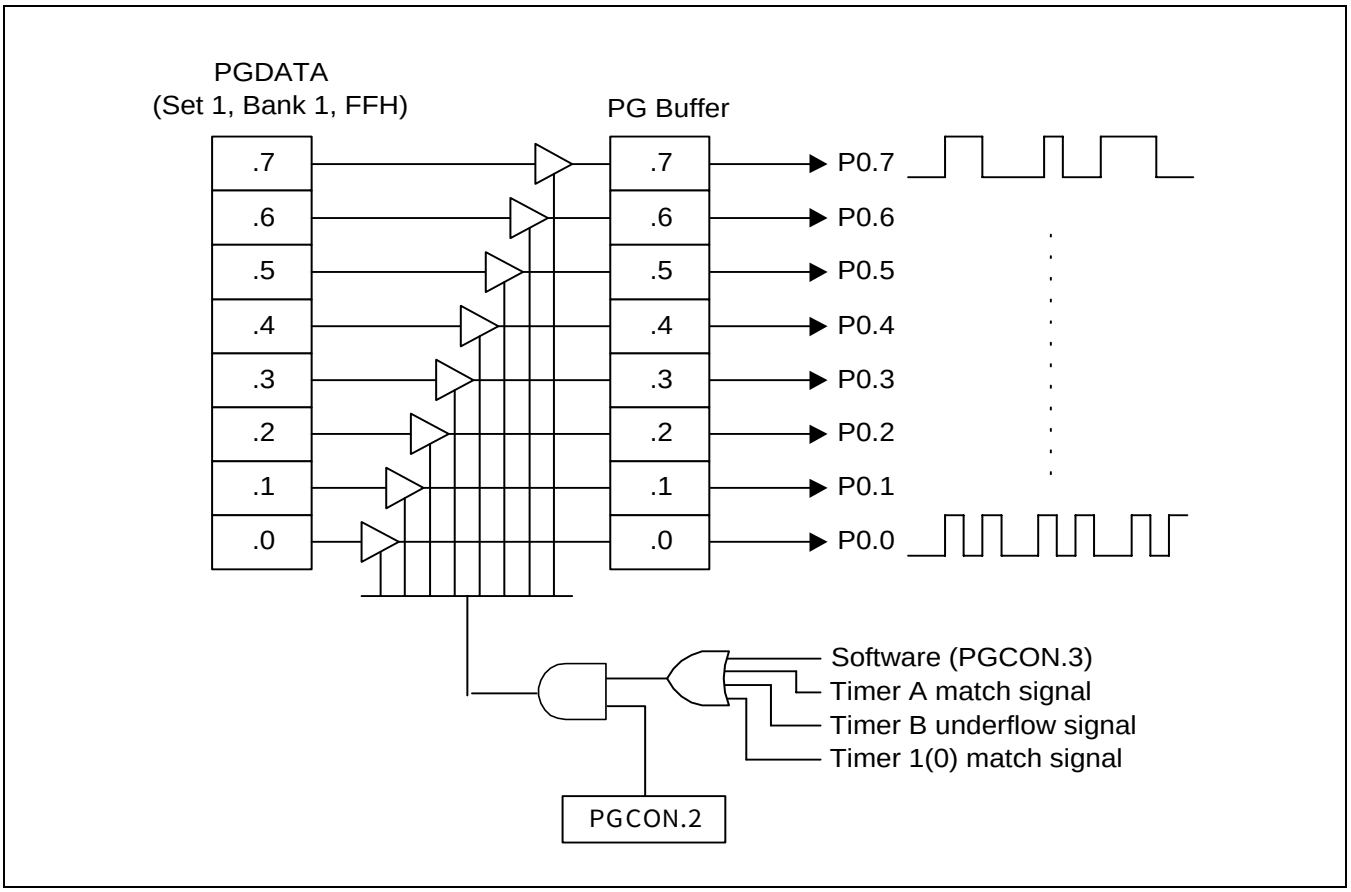


Figure 17-3. Pattern Generation Circuit Diagram

☞ Programming Tip – Using the Pattern Generation

```
        ORG     0000h

        ORG     0100h
INITIAL:
        SB0
        LD      SYM, #00h           ;  Disable Global/Fast interrupt → SYM
        LD      IMR, #01h           ;  Enable IRQ0 interrupt
        LD      SPH, #0h            ;  High byte of stack pointer → SPH
        LD      SPL, #0FFh          ;  Low byte of stack pointer → SPL
        LD      BTCON, #10100011b   ;  Disable Watch-dog
        LD      CLKCON, #00011000b  ;  Non-divided (fxx)

        LD      P0CON, #11111111b   ;  Enable PG output mode

        EI

MAIN:
        NOP
        NOP

        SB1
        LD      PGDATA, #10101010b  ;  PG data setting
        OR      PGCON, #00000100b   ;  Triggering by Timer A match then pattern data are output
        SB0

        NOP
        NOP

        JR      T, MAIN

        .END
```

18 LOW VOLTAGE RESET

OVERVIEW

By smart option (3FH.7 in ROM), user can select internal RESET (LVR) or external RESET.

The S3F84NB can be reset in four ways:

- by external power-on-reset
- by the external reset input pin pulled low
- by the digital watchdog timing out
- by the Low Voltage reset circuit (LVR)

During an external power-on reset, the voltage V_{DD} is High level and the RESETB pin is forced Low level. The RESETB signal is input through a Schmitt trigger circuit where it is then synchronized with the CPU clock. This brings the S3F84NB into a known operating status. To ensure correct start-up, the user should take that reset signal is not released before the V_{DD} level is sufficient to allow MCU operation at the chosen frequency.

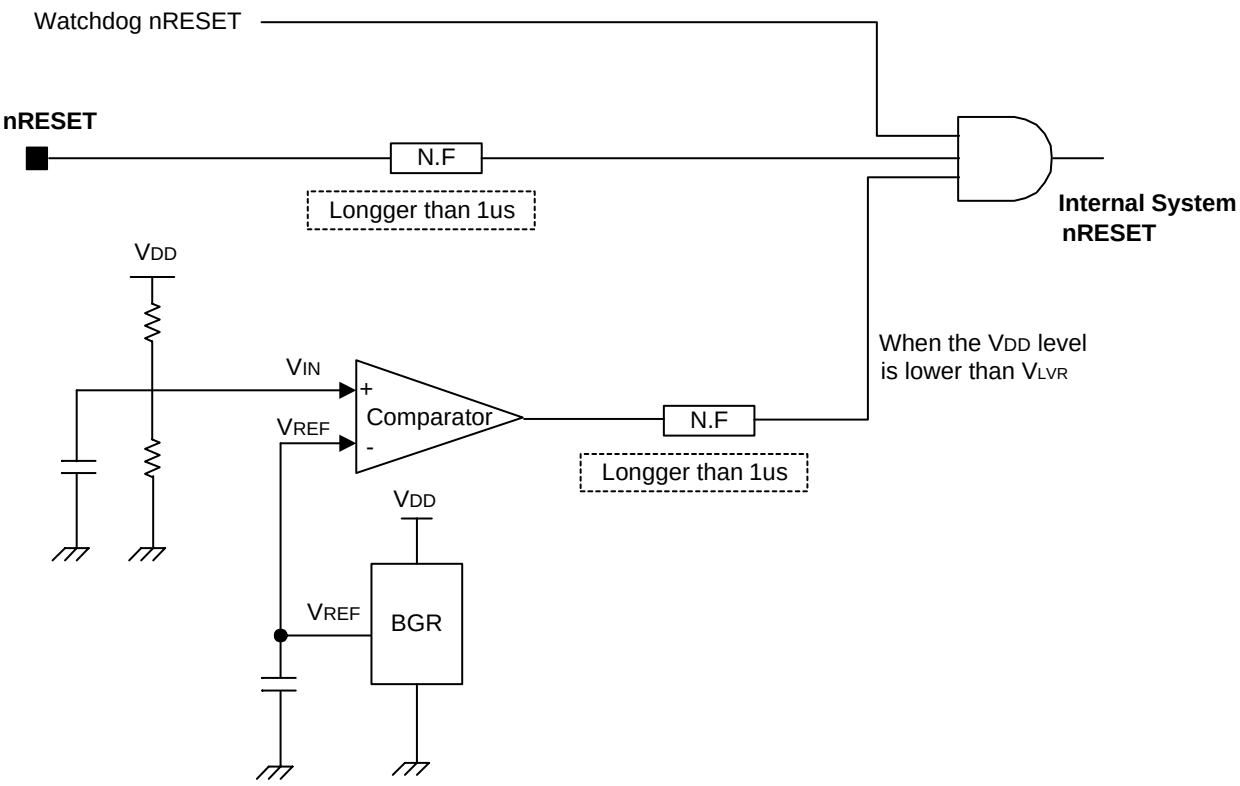
The RESETB pin must be held to Low level for a minimum time interval after the power supply comes within tolerance in order to allow time for internal CPU clock oscillation to stabilize. The minimum required oscillation stabilization time for a reset is approximately 6.55 ms ($\cong 2^{16}$/fosc, fosc= 10 MHz).

When a reset occurs during normal operation (with both V_{DD} and RESETB at High level), the signal at the RESETB pin is forced Low and the reset operation starts. All system and peripheral control registers are then set to their default hardware reset values (see Table 8-1).

The MCU provides a watchdog timer function in order to ensure graceful recovery from software malfunction. If watchdog timer is not refreshed before an end-of-counter condition (overflow) is reached, the internal reset will be activated.

The S3F84NB has a built-in low voltage reset circuit that allows detection of power voltage drop of external V_{DD} input level to prevent a MCU from malfunctioning in an unstable MCU power level. This voltage detector works for the reset operation of MCU. This Low Voltage reset includes an analog comparator and Vref circuit. The value of a detection voltage is set internally by hardware. The on-chip Low Voltage Reset, features static reset when supply voltage is below a reference voltage value (Typical 3.0 V). Thanks to this feature, external reset circuit can be removed while keeping the application safety. As long as the supply voltage is below the reference value, there is an internal and static RESET. The MCU can start only when the supply voltage rises over the reference voltage.

When you calculate power consumption, please remember that a static current of LVR circuit should be added a CPU operating current in any operating modes such as Stop, Idle, and normal RUN mode.



NOTES: BGR is Band Gap voltage Reference

Figure 18-1. Low Voltage Reset Circuit

NOTE

To program the duration of the oscillation stabilization interval, you make the appropriate settings to the basic timer control register, BTCON, *before* entering Stop mode. Also, if you do not want to use the basic timer watchdog function (which causes a system reset if a basic timer counter overflow occurs), you can disable it by writing '1010B' to the upper nibble of BTCON.

19 EMBEDDED FLASH MEMROY INTERFACE

OVERVIEW

The S3F84NB has an on-chip flash memory internally instead of masked ROM. The flash memory is accessed by instruction 'LDC'. This is a sector erasable and a byte programmable flash. User can program the data in a flash memory area any time you want. The S3F84NB's embedded 64K-byte memory has two operating features as below:

- User Program Mode
- Tool Program Mode

Flash ROM Configuration

The S3F84NB flash memory consists of 512sectors. Each sector consists of 128bytes. So, the total size of flash memory is 512x128 bytes (64KB). User can erase the flash memory by a sector unit at a time and write the data into the flash memory by a byte unit at a time.

- 64Kbyte Internal flash memory
- Sector size: 128-Bytes
- 10years data retention
- Fast programming Time:
  Sector Erase: 10ms (min)
  Byte Program: 32us (min)
- Byte programmable
- User programmable by 'LDC' instruction
- Sector (128-Bytes) erase available
- External serial programming support
- Endurance: 10,000 Erase/Program cycles (min)
- Expandable OBPTM (On Board Program)

User Program Mode

This mode supports sector erase, byte programming, byte read and one protection mode (Hard Lock Protection). The S3F84NB has the internal pumping circuit to generate high voltage. Therefore, 12.5V into Vpp (TEST) pin is not needed. To program a flash memory in this mode several control registers will be used.
There are four kind functions in user program mode – programming, reading, sector erase, and one protection mode (Hard lock protection).

Tool Program Mode

This mode is for erasing and programming full area of flash memory by external programming tools. The 6 pins of S3F84NB are connected to a programming tool and then internal flash memory of S3F84NB can be programmed by Serial OTP/MTP Tools, SPW2 plus single programmer or GW-PRO2 gang programmer and so on. The other modules except flash memory module are at a reset state. This mode doesn't support the sector erase but chip erase (all flash memory erased at a time) and two protection modes (Hard lock protection/ Read protection). The read protection mode is available only in tool program mode. So in order to make a chip into read protection, you need to select a read protection option when you write a program code to a chip in tool program mode by using a programming tool. After read protect, all data of flash memory read "00". This protection is released by chip erase execution in the tool program mode.

Table 19-1. Descriptions of Pins Used to Read/Write the Flash in Tool Program Mode

Normal Chip Pin Name	During Programming			
	Pin Name	Pin No.	I/O	Function
P5.6	SDAT	14[7]	I/O	Serial data pin. Output port when reading and input port when writing. SDAT (P5.6) can be assigned as an input or push-pull output port.
P5.5	SCLK	15[8]	I	Serial clock pin. Input only pin.
TEST	TEST	20[13]	I	Tool mode selection when TEST pin sets Logic value '1'. If user uses the flash writer tool mode (ex.spw2+ etc.), user should connect TEST pin to V_{DD}. (S3F84NB supplies high voltage 12.5V by internal high voltage generation circuit.)
nRESET	nRESET	23[16]	I	Chip Initialization
V_{DD}, V_{SS}	V_{DD}, V_{SS}	16[9], 17[10]	–	Power supply pin for logic circuit. V_{DD} should be tied to +3.3 V during programming.

NOTE: [ ] means 64QFP package.

ISP™ (ON-BOARD PROGRAMMING) SECTOR

ISP™ sectors located in program memory area can store On Board Program Software (Boot program code for upgrading application code by interfacing with I/O port pin). The ISP™ sectors can't be erased or programmed by 'LDC' instruction for the safety of On Board Program Software.

The ISP sectors are available only when the ISP enable/disable bit is set 0, that is, enable ISP at the Smart Option. If you don't like to use ISP sector, this area can be used as a normal program memory (can be erased or programmed by 'LDC' instruction) by setting ISP disable bit ("1") at the Smart Option. Even if ISP sector is selected, ISP sector can be erased or programmed in the tool program mode by serial programming tools.

The size of ISP sector can be varied by settings of smart option (Refer to Figure 2-2 and Table 19-2). You can choose appropriate ISP sector size according to the size of On Board Program Software.

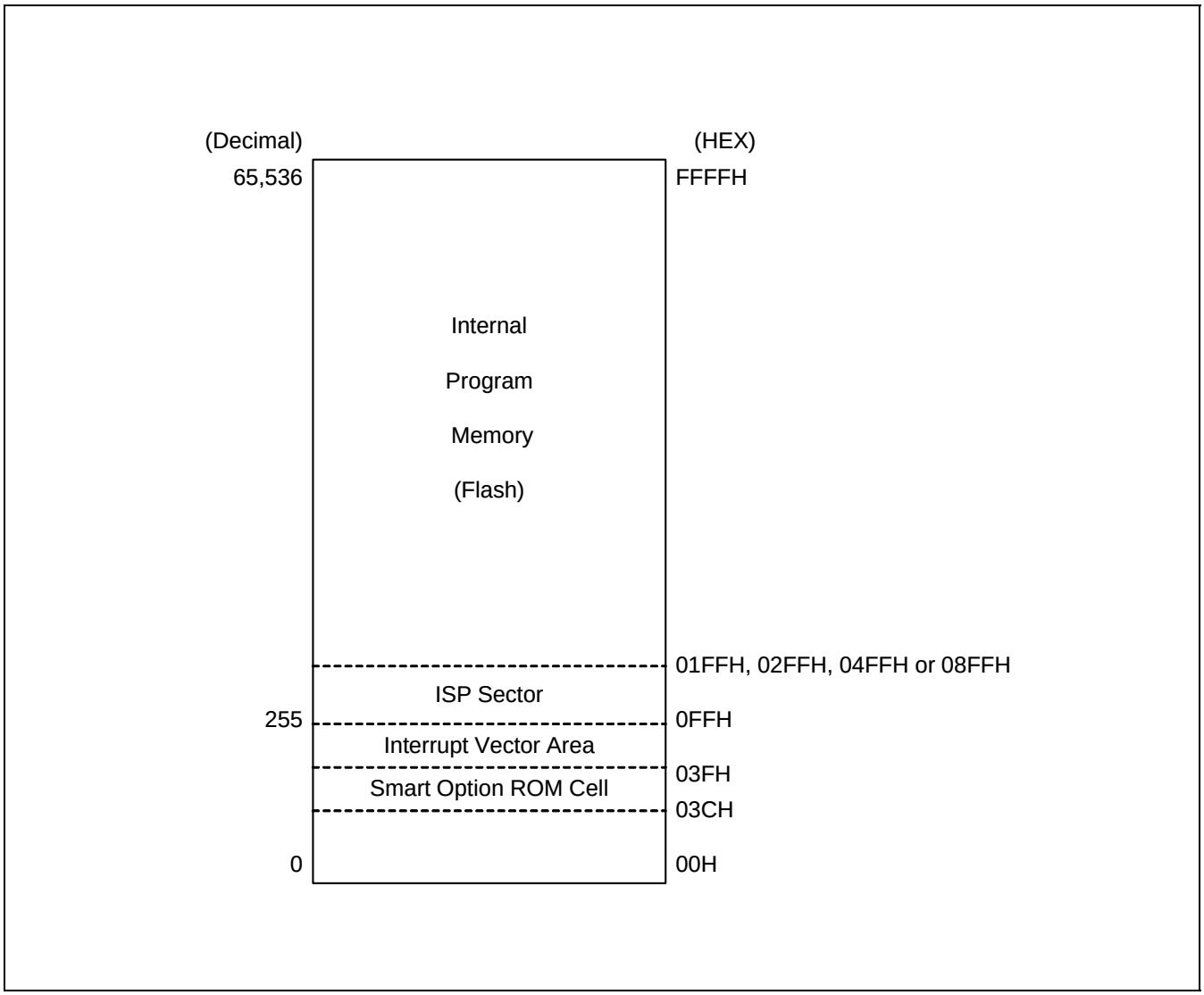


Figure 19-1. Program Memory Address Space

SMART OPTION

Smart option is the program memory option for starting condition of the chip. The program memory addresses used by smart option are from 003CH to 003FH. The S3F84NB only use 003EH and 003FH. User can write any value in the not used addresses (003CH and 003DH). The default value of smart option bits in program memory is 0FFH (IPOR disable, LVD enable in the stop mode, Normal reset vector address 100H, ISP protection disable). Before execution the program memory code, user can set the smart option bits according to the hardware option for user to want to select.

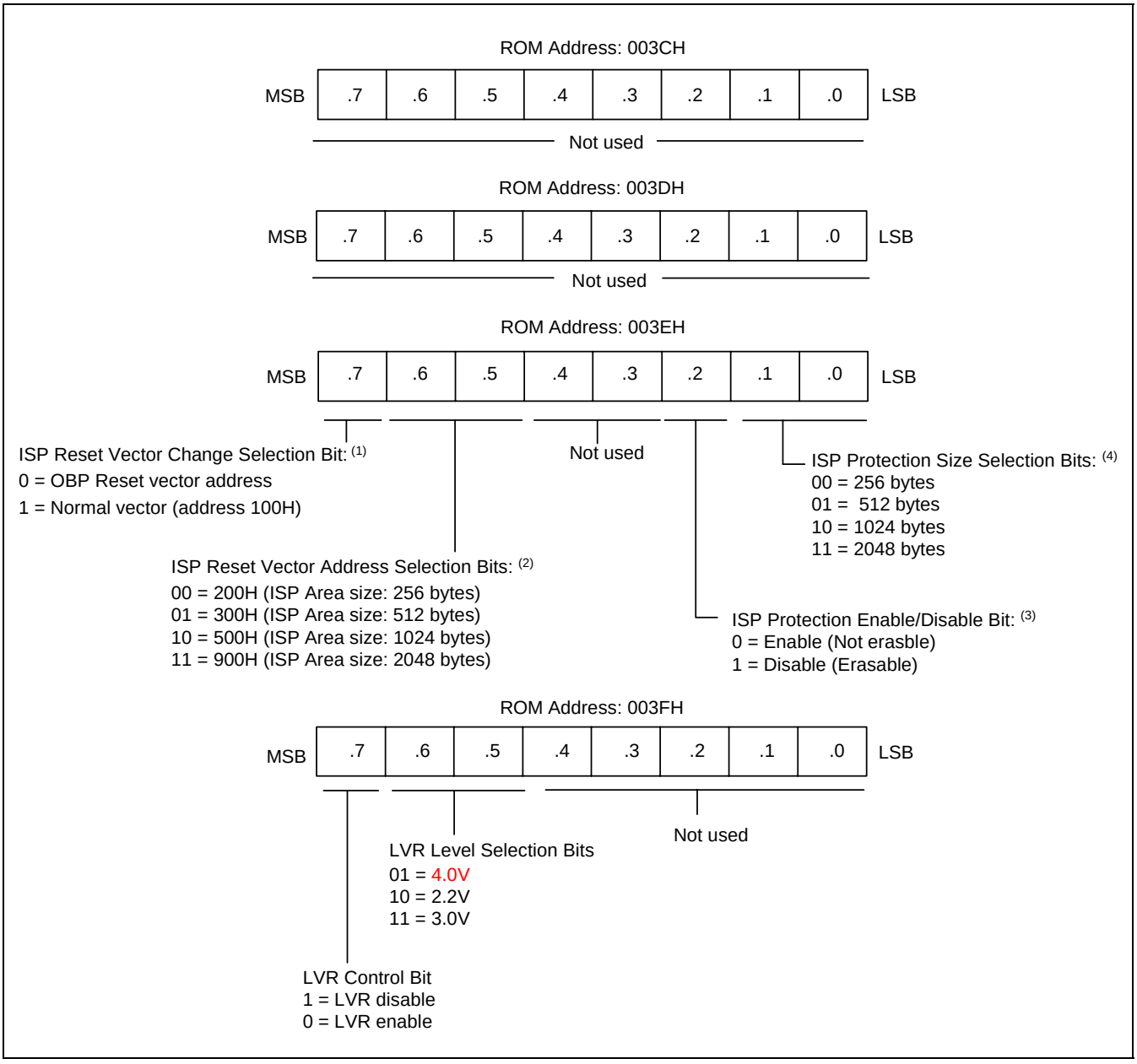


Figure 19-2. Smart Option

NOTES

1. By setting ISP Reset Vector Change Selection Bit (3EH.7) to '0', user can have the available ISP area.
   If ISP Reset Vector Change Selection Bit (3EH.7) is '1', 3EH.6 and 3EH.5 are meaningless.
2. If ISP Reset Vector Change Selection Bit (3EH.7) is '0', user must change ISP reset vector address from 0100H to some address which user want to set reset address (0200H, 0300H, 0500H or 0900H).
   If the reset vector address is 0200H, the ISP area can be assigned from 0100H to 01FFH (256bytes). If 0300H, the ISP area can be assigned from 0100H to 02FFH (512bytes). If 0500H, the ISP area can be from 0100H to 04FFH (1024bytes). If 0900H, the ISP area can be from 0100H to 08FFH (2048bytes).
3. If ISP Protection Enable/Disable Bit is '0', user can't erase or program the ISP area selected by 3EH.1 and 3EH.0 in flash memory.
4. User can select suitable ISP protection size by 3EH.1 and 3EH.0. If ISP Protection Enable/Disable Bit (3EH.2) is '1', 3EH.1 and 3EH.0 are meaningless.

Table 19-2. ISP Sector Size

Smart Option (003EH) ISP Size Selection Bit			Area of ISP Sector	ISP Sector Size
Bit 2	Bit 1	Bit 0		
1	x	x	0	0
0	0	0	100H – 1FFH (256 Bytes)	256 Bytes
0	0	1	100H – 2FFH (512 Bytes)	512 Bytes
0	1	0	100H – 4FFH (1024 Bytes)	1024 Bytes
0	1	1	100H – 8FFH (2048 Bytes)	2048 Bytes

NOTE: The area of the ISP sector selected by smart option bit (3EH.2 – 3EH.0) can't be erased and programmed by 'LDC' instruction in user program mode.

ISP RESET VECTOR AND ISP SECTOR SIZE

If you use ISP sectors by setting the ISP enable/disable bit to "0" and the reset vector selection bit to "0" at the smart option, you can choose the reset vector address of CPU as shown in Table 19-3 by setting the ISP reset vector address selection bits. (Refer to Figure 2-2 Smart Option).

Table 19-3. Reset Vector Address

Smart Option (003EH) ISP Reset Vector Address Selection Bit			Reset Vector Address after POR	Usable Area for ISP Sector	ISP Sector Size
Bit 7	Bit 6	Bit 5			
1	x	x	0100H	0	0
0	0	0	0200H	100H – 1FFH	256 Bytes
0	0	1	0300H	100H – 2FFH	512 Bytes
0	1	0	0500H	100H – 4FFH	1024 Bytes
0	1	1	0900H	100H – 8FFH	2048 Bytes

NOTE: The selection of the ISP reset vector address by Smart Option (003EH.7 – 003EH.5) is not dependent of the selection of ISP sector size by Smart Option (003EH.2 – 003EH.0).

FLASH MEMORY CONTROL REGISTERS (USER PROGRAM MODE)

FLASH MEMORY CONTROL REGISTER (FMCON)

FMCON register is available only in user program mode to select the flash memory operation mode; sector erase, byte programming, and to make the flash memory into a hard lock protection.

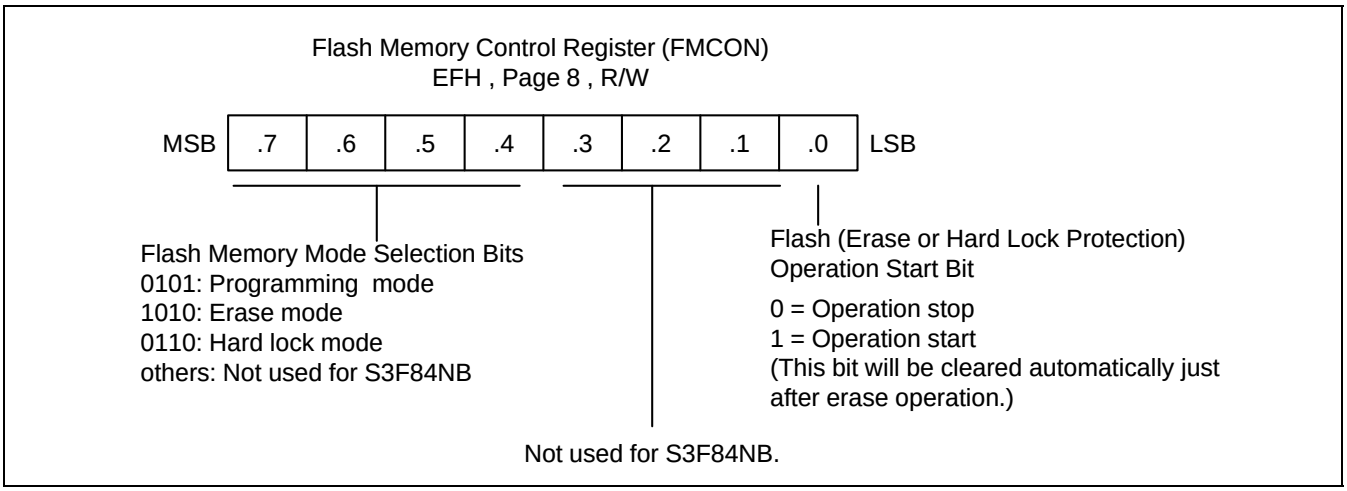


Figure 19-3. Flash Memory Control Register (FMCON)

The bit 0 of FMCON register (FMCON.0) is a bit for the operation start of Erase and Hard Lock Protection. Therefore, operation of Erase and Hard Lock Protection is activated when you set FMCON.0 to “1”. If you write FMCON.0 to 1 for erasing, CPU is stopped automatically for erasing time (min.10ms). After erasing time, CPU is restarted automatically. When you read or program a byte data from or into flash memory, this bit is not needed to manipulate.

FLASH MEMORY USER PROGRAMMING ENABLE REGISTER (FMUSR)

The FMUSR register is used for a safe operation of the flash memory. This register will protect undesired erase or program operation from malfunctioning of CPU caused by an electrical noise. After reset, the user-programming mode is disabled, because the value of FMUSR is “00000000B” by reset operation. If necessary to operate the flash memory, you can use the user programming mode by setting the value of FMUSR to “10100101B”. The other value of “10100101B”, user program mode is disabled.

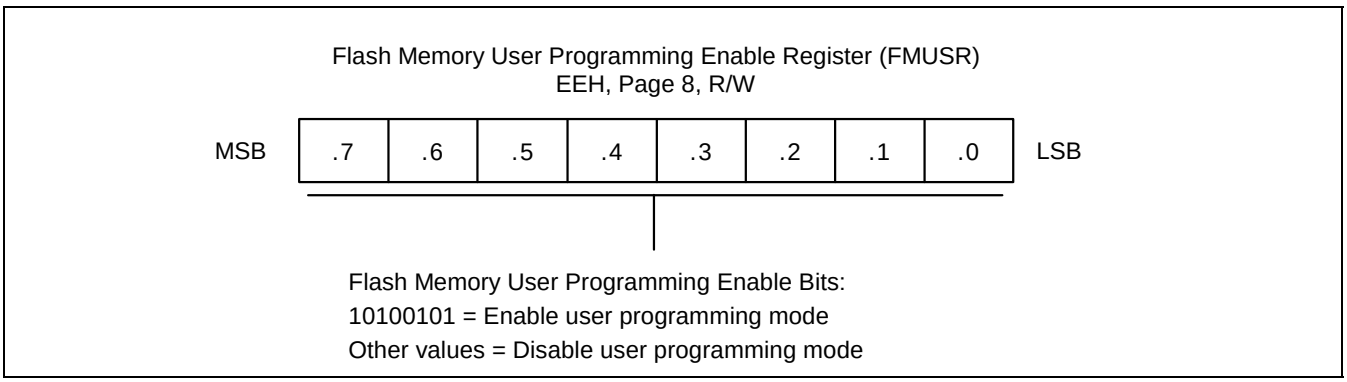


Figure 19-4. Flash Memory User Programming Enable Register (FMUSR)

FLASH MEMORY SECTOR ADDRESS REGISTERS

There are two sector address registers for the erase or programming flash memory. The FMSECL (Flash Memory Sector Address Register Low Byte) indicates the low byte of sector address and FMSECH (Flash Memory Address Sector Register High Byte) indicates the high byte of sector address. The FMSECH is needed for S3F84NB because it has 512 sectors.

One sector consists of 128-bytes. Each sector's address starts XX00H or XX80H, that is, a base address of sector is XX00H or XX80H. So bit .6-.0 of FMSECL don't mean whether the value is '1' or '0'. We recommend that it is the simplest way to load the sector base address into FMSECH and FMSECL register. When programming the flash memory, user should program after loading a sector base address, which is located in the destination address to write data into FMSECH and FMSECL register. If the next operation is also to write one byte data, user should check whether next destination address is located in the same sector or not. In case of other sectors, user should load sector address to FMSECH and FMSECL Register according to the sector. (Refer to page 15-16 PROGRAMMING TIP – Programming)

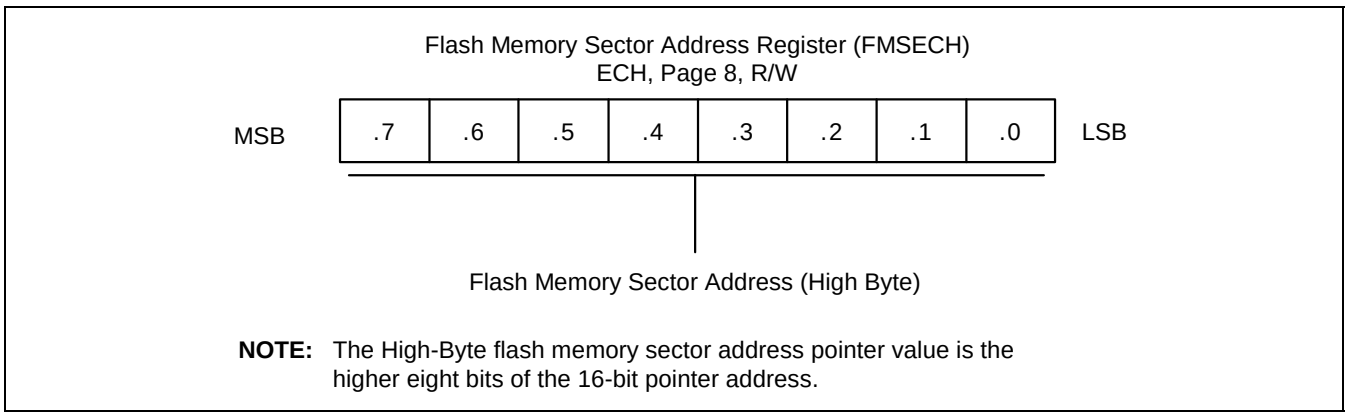


Figure 19-5. Flash Memory Sector Address Register (FMSECH)

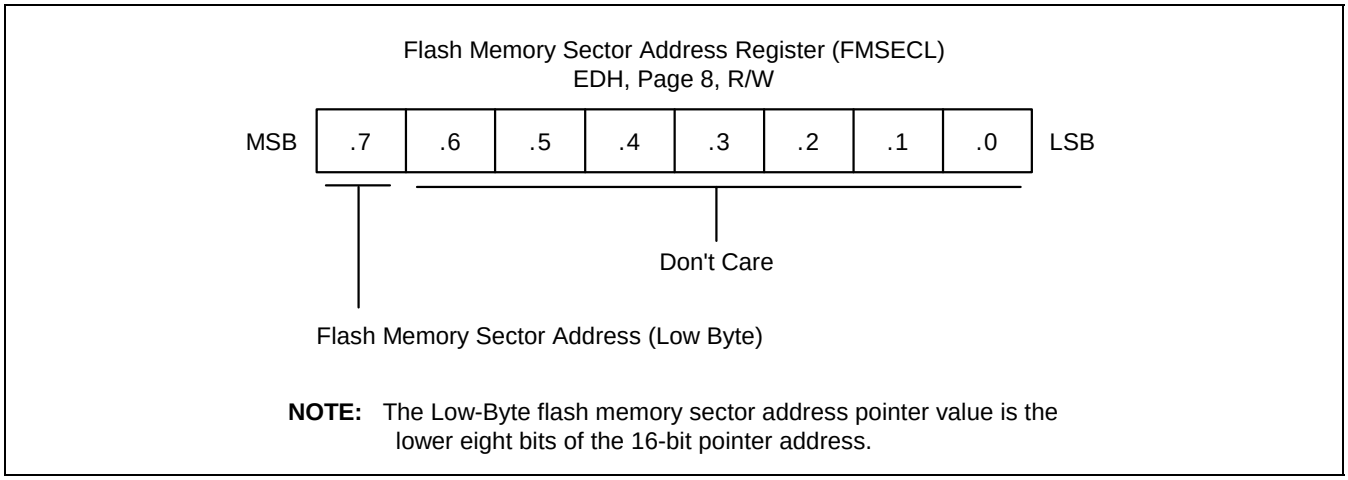


Figure 19-6. Flash Memory Sector Address Register (FMSECL)

SECTOR ERASE

User can erase a flash memory partially by using sector erase function only in user program mode. The only unit of flash memory to be erased in the user program mode is a sector.
The program memory of S3F84NB, 64Kbytes flash memory, is divided into 512 sectors. Every sector has all 128-byte sizes. So the sector to be located destination address should be erased first to program a new data (one byte) into flash memory. Minimum 10ms' delay time for the erase is required after setting sector address and triggering erase start bit (FMCON.0). Sector erase is not supported in tool program modes (MDS mode tool or programming tool).

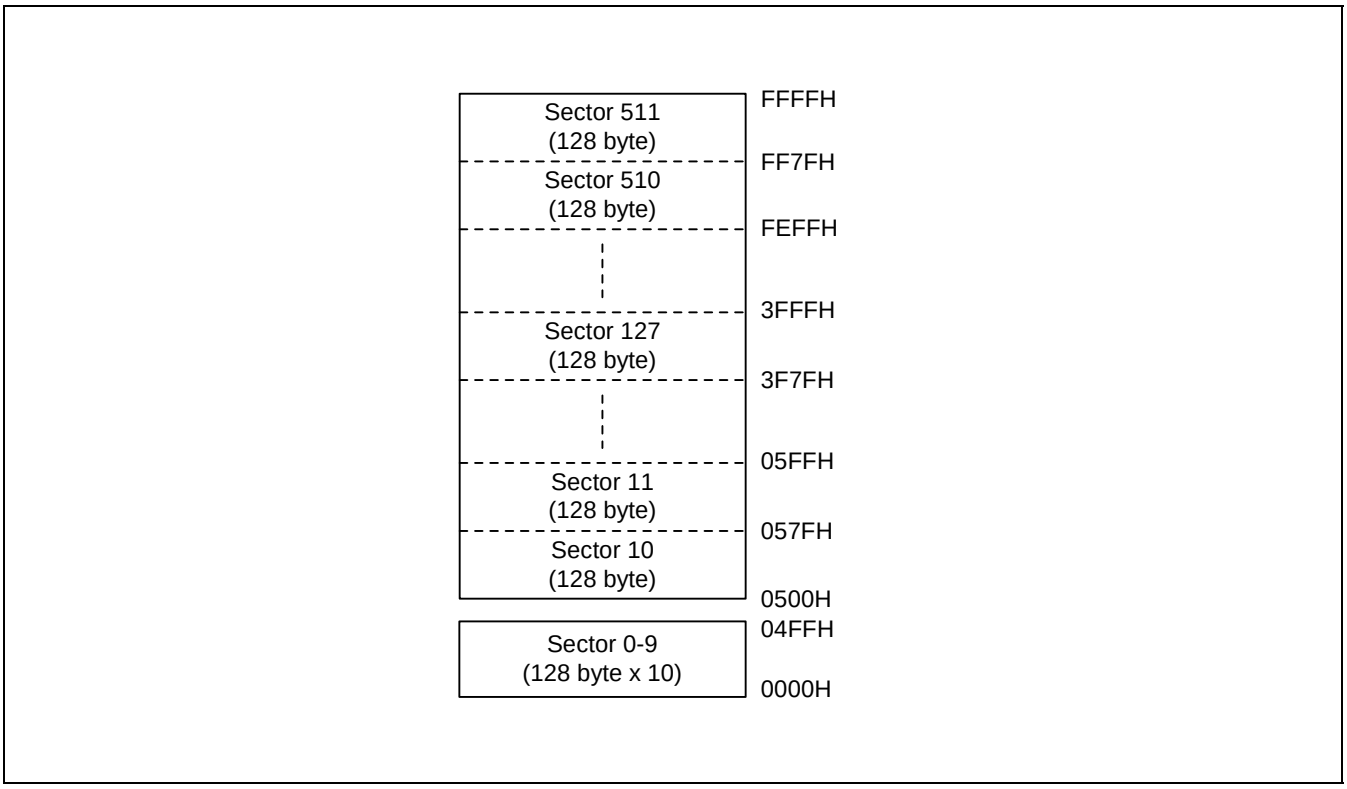


Figure 19-7. Sector Configurations in User Program Mode

The Sector Erase Procedure in User Program Mode

1. Set Flash Memory User Programming Enable Register (FMUSR) to “10100101B”.
2. Set Flash Memory Sector Address Register (FMSECH and FMSECL).
3. Set Flash Memory Control Register (FMCON) to “10100001B”.
4. Set Flash Memory User Programming Enable Register (FMUSR) to “00000000B”.

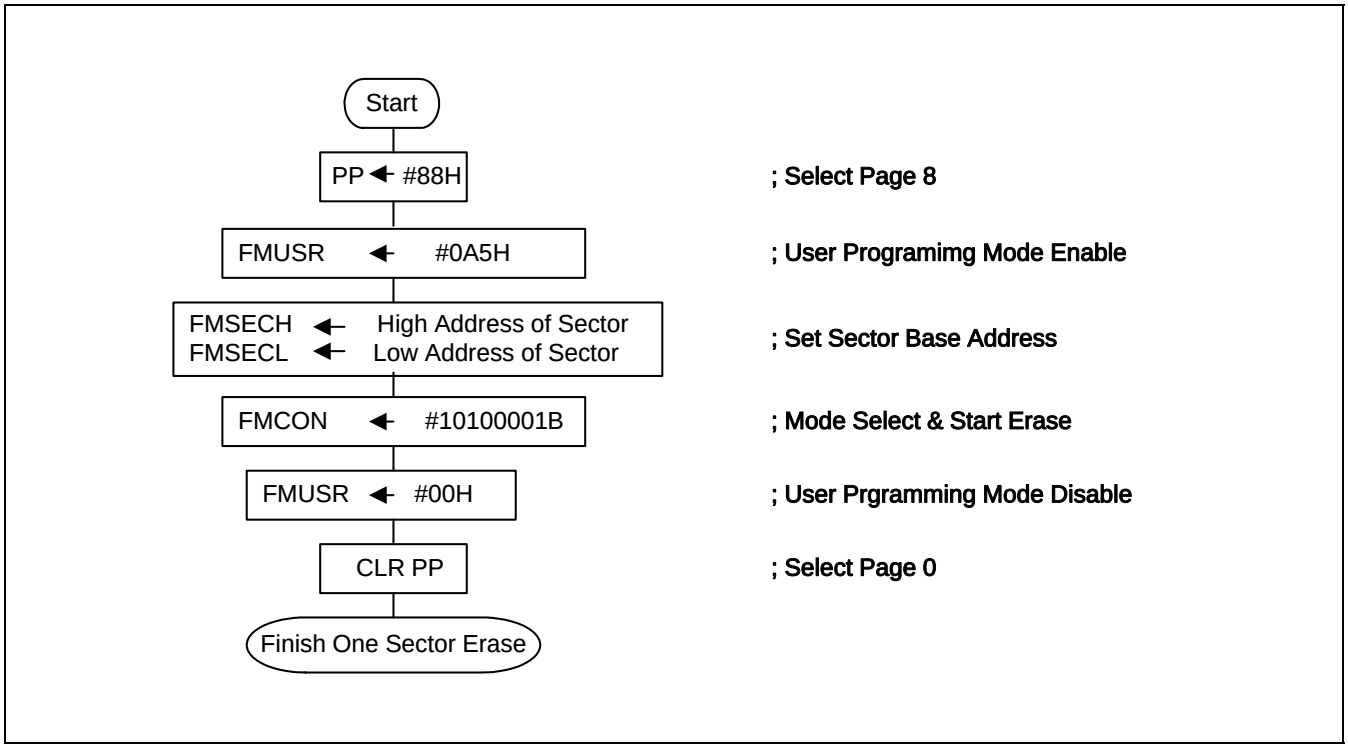


Figure 19-8. Sector Erase Flowchart in User Program Mode

NOTES

1. If user erases a sector selected by Flash Memory Sector Address Register FMSECH and FMSECL, FMUSR should be enabled just before starting sector erase operation. And to erase a sector, Flash Operation Start Bit of FMCON register is written from operation stop ‘0’ to operation start ‘1’. That bit will be cleared automatically just after the corresponding operation completed. In other words, when S3F84NB is in the condition that flash memory user programming enable bits is enabled and executes start operation of sector erase, it will get the result of erasing selected sector as user’s a purpose and Flash Operation Start Bit of FMCON register is also clear automatically.
2. If user executes sector erase operation with FMUSR disabled, FMCON.0 bit, Flash Operation Start Bit, remains 'high', which means start operation, and is not cleared even though next instruction is executed. So user should be careful to set FMUSR when executing sector erase, for no effect on other flash sectors.

☞ PROGRAMMING TIP – Sector Erase

Case1. Erase one sector

```
                    •
                    •
ERASE_ONESECTOR:
                    LD      PP,#88H
                    LD      FMUSR,#0A5H         ; User program mode enable
                    LD      FMSECH,#40H         ; Set sector address 4000H,sector 128,
                    LD      FMSECL,#00H         ; among sector 0~511
                    LD      FMCON,#10100001B    ; Select erase mode enable & Start sector erase

ERASE_STOP:         LD      FMUSR,#00H          ; User program mode disable
                    LD      PP,#00H
```

Case2.Erase flash memory space from Sector (n) to Sector (n + m)

```
                    •
                    •
;;Pre-define the number of sector to erase

                    LD      SecNumH,#00H        ; Set sector number
                    LD      SecNumL,#128        ; Selection the sector128 ( base address 4000H )
                    LD      R6,#01H             ; Set the sector range (m) to erase
                    LD      R7,#7DH             ; into High-byte(R6) and Low-byte(R7)
                    LD      R2,SecNumH
                    LD      R3,SecNumL

ERASE_LOOP:         CALL    SECTOR_ERASE
                    XOR     P4,#11111111B       ; Display ERASE_LOOP cycle
                    INCW    RR2
                    LD      SecNumH,R2
                    LD      SecNumL,R3
                    DECW    RR6
                    LD      R8,R6
                    OR      R8,R7
                    CP      R8,#00H
                    JP      NZ,ERASE_LOOP
                    •
                    •
```

```
SECTOR_ERASE:
                LD      R12,SecNumH
                LD      R14,SecNumL
                MULT    RR12,#80H           ; Calculation the base address of a target sector
                MULT    RR14,#80H           ; The size of one sector is 128-bytes
                ADD     R13,R14
                                            ; BTJRF  FLAGS.7,NOCARRY
                                            ; INC    R12
NOCARRY:
                LD      R10,R13
                LD      R11,R15

ERASE_START:
                LD      PP,#88H
                LD      FMUSR,#0A5H         ; User program mode enable
                LD      FMSECH,R10          ; Set sector address
                LD      FMSECL,R11
                LD      FMCON,#10100001B    ; Select erase mode enable & Start sector erase
ERASE_STOP:
                LD      FMUSR,#00H          ; User program mode disable
                LD      PP,#00H
                RET
```

PROGRAMMING

A flash memory is programmed in one-byte unit after sector erase. The write operation of programming starts by ‘LDC’ instruction.

The program procedure in user program mode

1. Must erase target sectors before programming.
2. Set Flash Memory User Programming Enable Register (FMUSR) to “10100101B”.
3. Set Flash Memory Control Register (FMCON) to “0101000XB”.
4. Set Flash Memory Sector Address Register (FMSECH and FMSECL) to the sector base address of destination address to write data.
5. Load a transmission data into a working register.
6. Load a flash memory upper address into upper register of pair working register.
7. Load a flash memory lower address into lower register of pair working register.
8. Load transmission data to flash memory location area on ‘LDC’ instruction by indirectly addressing mode
9. Set Flash Memory User Programming Enable Register (FMUSR) to “00000000B”.

NOTE

In programming mode, it doesn’t care whether FMCON.0’s value is “0” or “1”.

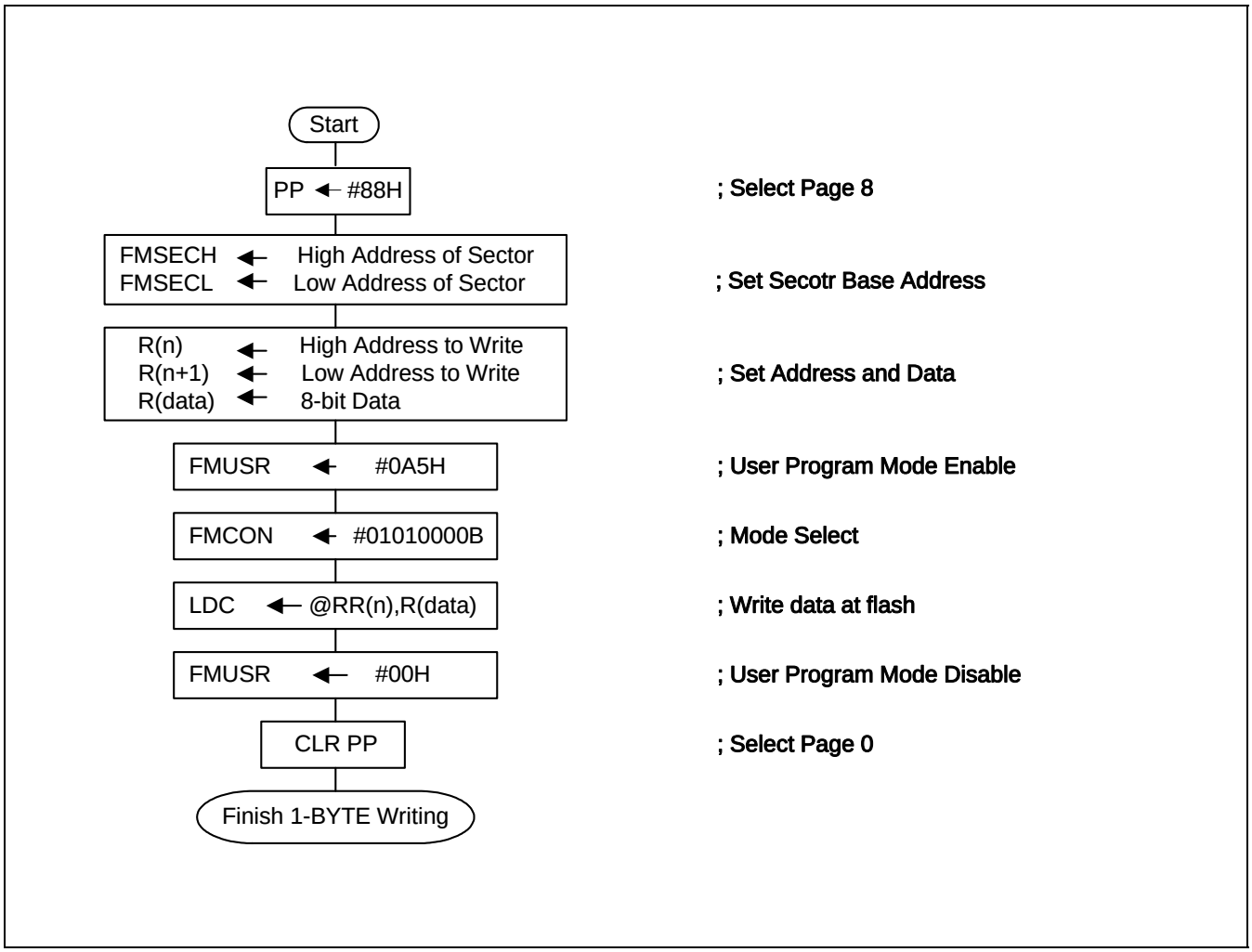


Figure 19-9. Byte Program Flowchart in a User Program Mode

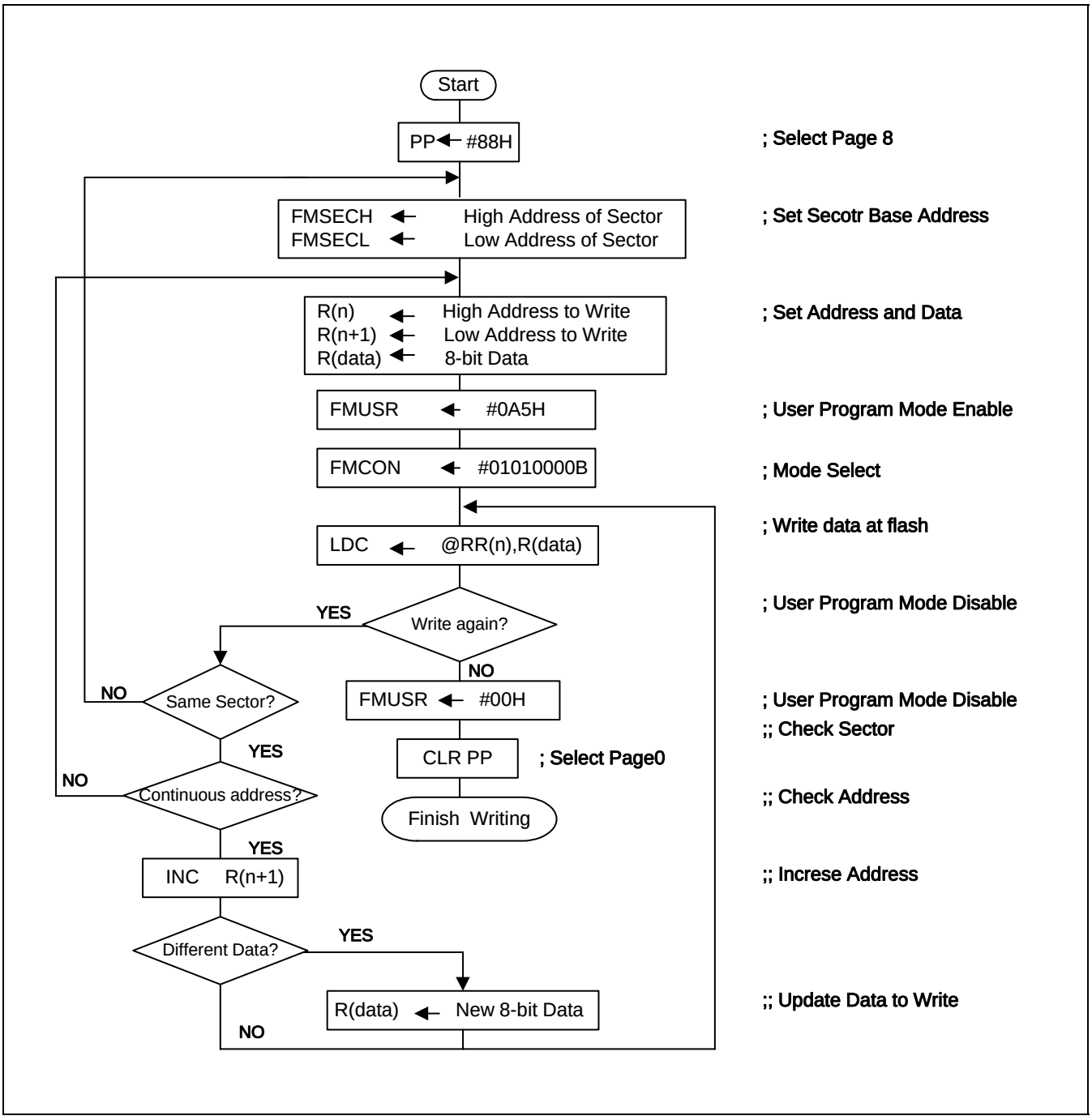


Figure 19-10. Program Flowchart in a User Program Mode

☞ PROGRAMMING TIP – Programming

Case1. 1-Byte Programming

```
    •
    •
WR_BYTE:                        ; Write data “AAH”  to destination address 4010H
    LD      PP,#88H
    LD      FMUSR,#0A5H         ; User program mode enable
    LD      FMCON,#01010000B    ; Selection programming mode
    LD      FMSECH, #40H        ; Set the base address of sector (4000H)
    LD      FMSECL, #00H
    LD      R9,#0AAH            ; Load data “AA” to write
    LD      R10,#40H            ; Load flash memory upper address into upper register of pair working
                                ; register
    LD      R11,#10H            ; Load flash memory lower address into lower register of pair working
                                ; register
    LDC     @RR10,R9            ; Write data 'AAH' at flash memory location (4010H)

    LD      FMUSR,#00H          ; User program mode disable
    LD      PP,#00H
```

Case2. Programming in the same sector

```
    •
    •
WR_INSECTOR:                    ; RR10-->Address copy  (R10 –high address,R11-low address)

    LD      R0,#40H

  LD        PP,#88H
    LD      FMUSR,#0A5H         ; User program mode enable
    LD      FMCON,#01010000B    ; Selection programming mode and Start programming
    LD      FMSECH,#40H         ; Set the base address of sector located in target address to write data
    LD      FMSECL,#00H         ; The sector 128’s base address is 4000H.
    LD      R9,#33H             ; Load data “33H” to write
    LD      R10,#40H            ; Load flash memory upper address into upper register of pair working
                                ; register
    LD      R11,#40H            ; Load flash memory lower address into lower register of pair working
                                ; register
WR_BYTE:
    LDC     @RR10,R9            ; Write data '33H' at flash memory location
    INC     R11                 ; Reset address in the same sector by INC instruction
    DJNZ    R0,WR_BYTE          ; Check whether the end address for programming reach 407FH or not.

    LD      FMUSR,#00H          ; User Program mode disable
    LD      PP,#00H
```

Case3. Programming to the flash memory space located in other sectors

```
    •
    •
WR_INSECTOR2:
    LD      R0,#40H
    LD      R1,#40H

    LD      PP,#88H
    LD      FMUSR,#0A5H         ; User program mode enable
    LD      FMCON,#01010000B    ; Selection programming mode and Start programming
    LD      FMSECH,#01H         ; Set the base address of sector located in target address to write data
    LD      FMSECL,#00H         ; The sector 2's base address is 100H
    LD      R9,#0CCH            ; Load data "CCH" to write
    LD      R10,#01H            ; Load flash memory upper address into upper register of pair working
                                ; register
    LD      R11,#40H            ; Load flash memory lower address into lower register of pair working
                                ; register
    CALL    WR_BYTE

    LD      R0,#40H
WR_INSECTOR50:
    LD      FMSECH,#19H         ; Set the base address of sector located in target address to write data
    LD      FMSECL,#00H         ; The sector 50's base address is 1900H
    LD      R9,# 55H            ; Load data "55H" to write
    LD      R10,#19H            ; Load  flash memory upper address into upper register of pair working
                                ; register
    LD      R11,#40H            ; Load flash memory lower address into lower register of pair working
                                ; register
    CALL    WR_BYTE

WR_INSECTOR128:
    LD      FMSECH,#40H         ; Set the base address of sector located in target address to write data
    LD      FMSECL,#00H         ; The sector 128's base address is 4000H
    LD      R9,#0A3H            ; Load data "A3H" to write
    LD      R10,#40H            ; Load  flash memory upper address into upper register of pair working
                                ; register
    LD      R11,#40H            ; Load flash memory lower address into lower register of pair working
                                ; register
WR_BYTE1:
    LDC     @RR10,R9            ; Write data 'A3H' at flash memory location
    INC     R11
    DJNZ    R1,WR_BYTE1

    LD      FMUSR,#00H          ; User Program mode disable
    LD      PP,#00H
    •
    •
WR_BYTE:
    LDC     @RR10,R9            ; Write data written by R9  at flash  memory location
    INC     R11
    DJNZ    R0,WR_BYTE
    RET
```

READING

The read operation starts by ‘LDC’ instruction.

The program procedure in user program mode

1. Load a flash memory upper address into upper register of pair working register.
2. Load a flash memory lower address into lower register of pair working register.
3. Load receive data from flash memory location area on ‘LDC’ instruction by indirectly addressing mode

☞ **PROGRAMMING TIP – Reading**

```
                •
                •
                LD      R2,#03H     ; Load flash memory's upper address
                                    ; to upper register of pair working register
                LD      R3,#00H     ; Load flash memory's lower address
                                    ; to lower register of pair working register

LOOP:           LDC     R0,@RR2     ; Read data from flash memory location
                                    ; (Between 300H and 3FFH)
                INC     R3
                CP      R3,#0FFH
                JP      NZ,LOOP
                •
                •
                •
                •
```

HARD LOCK PROTECTION

User can set Hard Lock Protection by writing '0110B' in FMCON7-4. This function prevents the changes of data in a flash memory area. If this function is enabled, the user cannot write or erase the data in a flash memory area. This protection can be released by the chip erase execution in the tool program mode. In terms of user program mode, the procedure of setting Hard Lock Protection is following that. In tool mode, the manufacturer of serial tool writer could support Hardware Protection. Please refer to the manual of serial program writer tool provided by the manufacturer.

The program procedure in user program mode

1. Set Flash Memory User Programming Enable Register (FMUSR) to "10100101B".
2. Set Flash Memory Control Register (FMCON) to "01100001B".
3. Set Flash Memory User Programming Enable Register (FMUSR) to "00000000B".

☞ **PROGRAMMING TIP – Hard Lock Protection**

```
•
•
LD      PP,#88H
LD      FMUSR,#0A5H          ; User program mode enable
LD      FMCON,#01100001B     ; Select Hard Lock Mode and Start protection
LD      FMUSR,#00H           ; User program mode disable
LD      PP,#00H
•
•
```

20 ELECTRICAL DATA

OVERVIEW

In this chapter, S3F84NB electrical characteristics are presented in tables and graphs. The information is arranged in the following order:

- Absolute maximum ratings
- Input/output capacitance
- D.C. electrical characteristics
- A.C. electrical characteristics
- Oscillation characteristics
- Oscillation stabilization time
- Data retention supply voltage in stop mode
- Serial I/O timing characteristics
- UART timing characteristics in mode 0
- A/D converter electrical characteristics
- LVR Circuit Characteristics
- A.C. Electrical Characteristics for Internal Flash ROM

Table 20-1. Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{DD}	–	– 0.3 to + 6.5	V
Input Voltage	V_I	All input ports	– 0.3 to V_{DD} + 0.3	
Output Voltage	V_O	All output ports	– 0.3 to V_{DD} + 0.3	
Output Current High	I_{OH}	One I/O pin active	– 18	mA
		All I/O pins active	– 60	
Output Current Low	I_{OL}	One I/O pin active	+ 30	
		Total pin current for ports 2-4, and 5	+ 100	
		Total pin current for ports 0,1, and 6	+ 200	
Operating Temperature	T_A	–	– 40 to + 85	°C
Storage Temperature	T_{STG}	–	– 65 to + 150	

Table 20-2. Input/Output Capacitance

(T_A = – 40°C to 85°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Input Capacitance	C_{IN}	f = 1 MHz; unmeasured pins are tied to V_{SS}	–	–	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

Table 20-3. D.C. Electrical Characteristics

(T_A = – 40°C to + 85°C, V_{DD} = 2.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Operation Voltage	V_{DD}	Fx = 1 – 4MHz fxt = 32.8 kHz, LVR off	2.0	–	5.5	V
		Fx = 1 – 4MHz fxt = 32.8 kHz, LVR on	LVR	–	5.5	
		Fx = 1 – 10 MHz	3.0	–	5.5	
Input High Voltage	V_{IH1}	V_{DD} = 2.0 V to 5.5 V All Port and nRESET	0.8 V_{DD}	–	V_{DD}	V
	V_{IH2}	V_{DD} = 2.0 V to 5.5 V X_{IN} and XT_{IN}	V_{DD} – 0.5			
Input Low Voltage	V_{IL1}	V_{DD} = 2.0 V to 5.5 V All Ports and nRESET	–	–	0.2 V_{DD}	V
	V_{IL2}	V_{DD} = 2.0 V to 5.5 V X_{IN} and XT_{IN}			0.4	
Output High Voltage	V_{OH}	V_{DD} = 5.5 V I_{OH} = –1 mA All Ports	V_{DD} – 1.0	–	–	V
Output Low Voltage	V_{OL1}	V_{DD} = 5.5 V, I_{OL} = 15 mA Ports 0,1, and 6	–	0.4	2.0	V
	V_{OL2}	V_{DD} = 5.5 V, I_{OL} = 4 mA Ports 2, 3, 4 and 5				
Input High Leakage Current	I_{LIH1}	V_{IN} = V_{DD} All input pins except I_{LIH2}	–	–	1	µA
	I_{LIH2}	V_{IN} = V_{DD} X_{IN}, X_{OUT} and XT_{IN}, XT_{OUT}			20	
Input Low Leakage Current	I_{LIL1}	V_{IN} = 0 V All input pins except and I_{LIL2}	–	–	– 1	
	I_{LIL2}	V_{IN} = 0 V X_{IN}, X_{OUT} and XT_{IN}, XT_{OUT}			– 20	
Output High Leakage Current	I_{LOH}	V_{OUT} = V_{DD} All output pins	–	–	2	
Output Low Leakage Current	I_{LOL}	V_{OUT} = 0 V All output pins	–	–	– 2	

Table 20-3. D.C. Electrical Characteristics (Continued)

(T_A = – 40°C to + 85°C, V_{DD} = 2.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Pull-up Resistor	R_P	V_{DD} = 5.5 V; V_{IN} = 0 V Port 0-6	25	50	100	kΩ
Supply Current (1)	$I_{DD1(2)}$	V_{DD} = 2.0 V to 5.5 V RUN mode 10 MHz CPU clock	–	6	12	mA
	I_{DD2}	V_{DD} = 2.0 V to 5.5 V Idle mode 10 MHz CPU clock	–	1.5	3	
	I_{DD3}	Sub operating: main-osc stop V_{DD} = 2.0 V to 5.5 V 32.768 kHz crystal oscillator	–	480	960	uA
	I_{DD4}	Sub idle mode: main-osc stop V_{DD} = 2.0 V to 5.5 V 32.768 KHz crystal oscillator	–	420	840	
	I_{DD5}	V_{DD} = 2.0 V to 5.5 V Stop mode	–	200	400	

NOTES:

1. Supply current does not include current drawn through internal pull-up resistors or external output current loads.
2. I_{DD1} and I_{DD2} include a power consumption of subsystem oscillator.
3. I_{DD3} and I_{DD4} are the current when the main system clock oscillation stop and the subsystem clock is used.
4. I_{DD5} is the current when the main and subsystem clock oscillation stop.
5. All currents (I_{DD1}– I_{DD5}) include the current consumption of LVR circuit.

Table 20-4. A.C. Electrical Characteristics

(T_A = – 40°C to + 85°C, V_{DD} = 2.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Interrupt Input High, Low Width (Ports 4 and 6)	t_{INTH}, t_{INTL}	V_{DD} = 5 V	500	–	–	ns
nRESET Input Low Width	t_{RSL}	Input	10	–	–	µs

NOTE: User must keep more large value then min value.

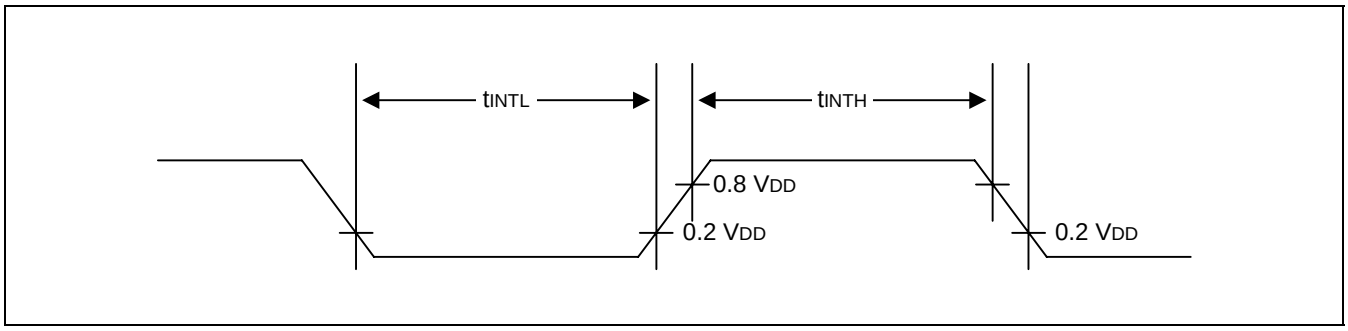


Figure 20-1. Input Timing for External Interrupts (Ports 4 and 6)

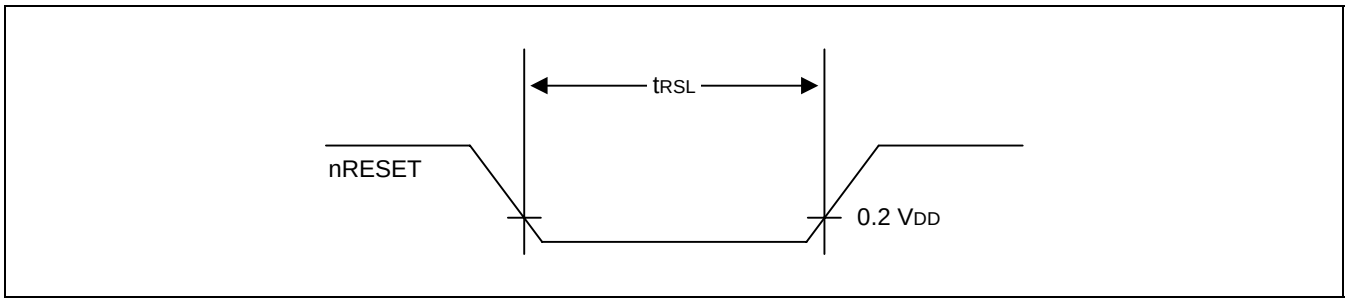


Figure 20-2. Input Timing for nRESET

Table 20-5. Main Oscillator Frequency (f_{OSC1})

(T_A = – 40°C + 85°C)

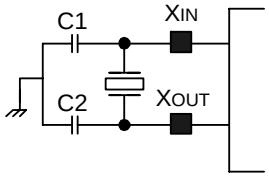
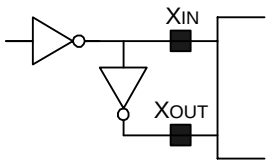
Oscillator	Clock Circuit	Test Condition	Min	Typ	Max	Unit
Main crystal or ceramic		V_{DD} = 2.0 to 5.5 V	1	–	10	MHz
External clock (Main System)		V_{DD} = 2.0 to 5.5 V	1	–	10	MHz

Table 20-6. Main Oscillator Clock Stabilization Time (t_{ST1})

(T_A = – 40°C + 85°C, V_{DD} = 2.0 V to 5.5 V)

Oscillator	Test Condition	Min	Typ.	Max	Unit
Main Crystal	f_{OSC} > 1.0 MHz;	–	–	20	ms
Main Ceramic	Oscillation stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	–	–	10	
External Clock (Main System)	X_{IN} input High and Low width (t_{XH}, t_{XL})	25	–	500	ns
Oscillator Stabilization Wait Time	t_{WAIT} when released by a reset (1)	–	$2^{16}/f_{OSC}$	–	sec
	t_{WAIT} when released by an interrupt (2)	–	–	–	sec

NOTES:
1. f_{OSC} is the oscillator frequency.
2. The duration of the oscillator stabilization wait time, t_{WAIT}, when it is released by an interrupt is determined by the settings in the basic timer control register, BTCON.

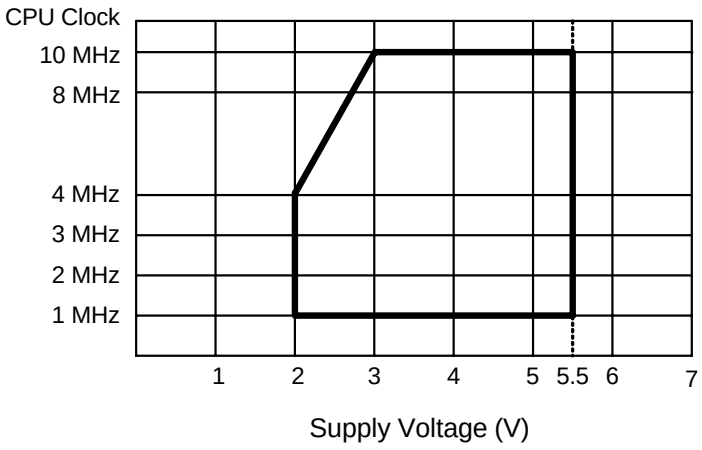


Figure 20-3. Operating Voltage Range

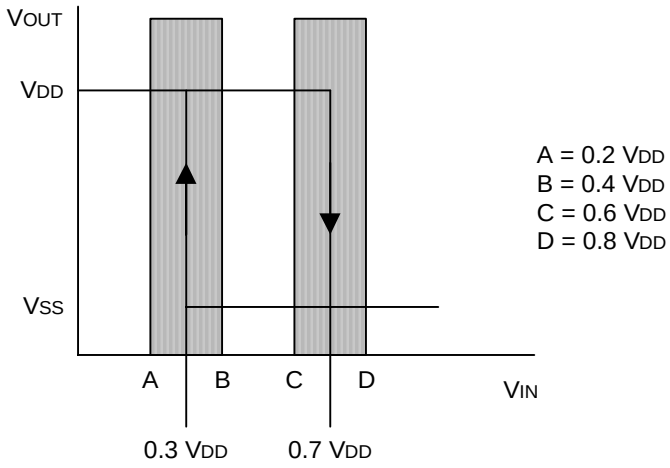


Figure 20-4. Schmitt Trigger Input Characteristics Diagram

Table 20-7. Sub Oscillator Frequency (f_{OSC2})

(T_A = –40 °C + 85 °C, V_{DD} = 2.0 V to 5.5 V)

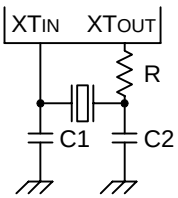
Oscillator	Clock Circuit	Test Condition	Min	Typ.	Max	Unit
Crystal		Crystal oscillation frequency XT_{IN} and XT_{OUT} are connected with R and C by soldering.	32	32.768	34	kHz

Table 20-8. Subsystem Oscillator (crystal) Stabilization Time (t_{ST2})

(T_A = 25 °C)

Oscillator	Test Condition	Min	Typ.	Max	Unit
Crystal	V_{DD} = 4.5 V to 5.5 V	–	800	1600	ms
	V_{DD} = 2.0 V to 3.3 V	–	2000	4000	

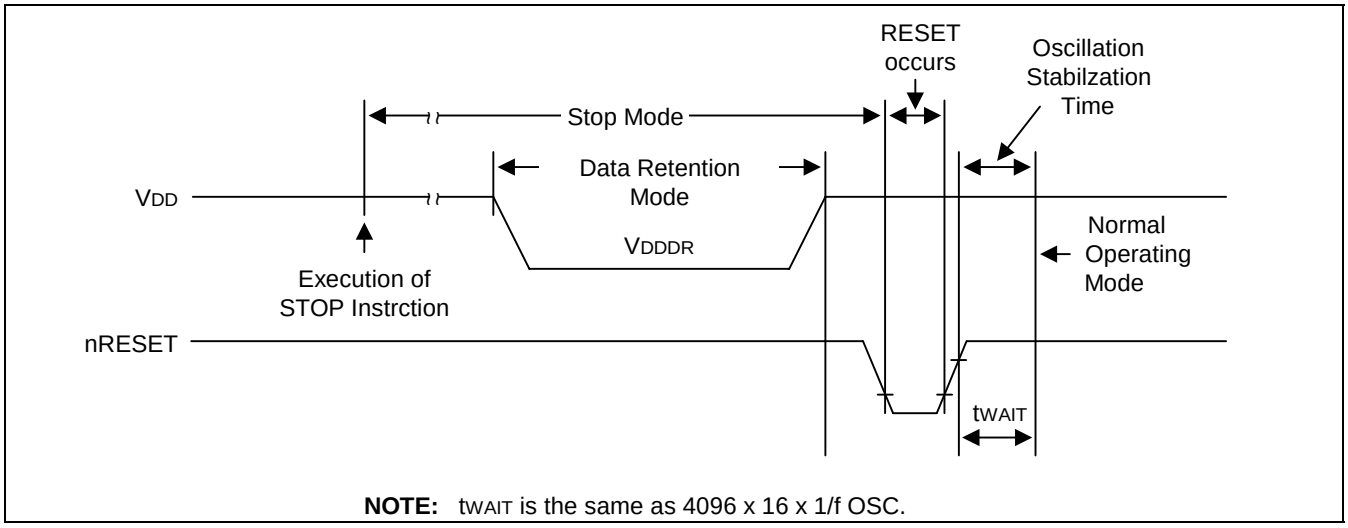
NOTE: Oscillation stabilization time (t_{ST2}) is the time required for the oscillator to it's normal oscillation when stop mode is released by interrupts. The value Typ. and Max are measured by buzzer output signal after stop release.
For example in voltage range of 4.5 V to 5.5 V of normal mode, we can see the buzzer output signal within 400 ms at our test condition.

Table 20-9. Data Retention Supply Voltage in Stop Mode

(T_A = –40°C to + 85°C, V_{DD} = 2.0 V to 5.5 V)

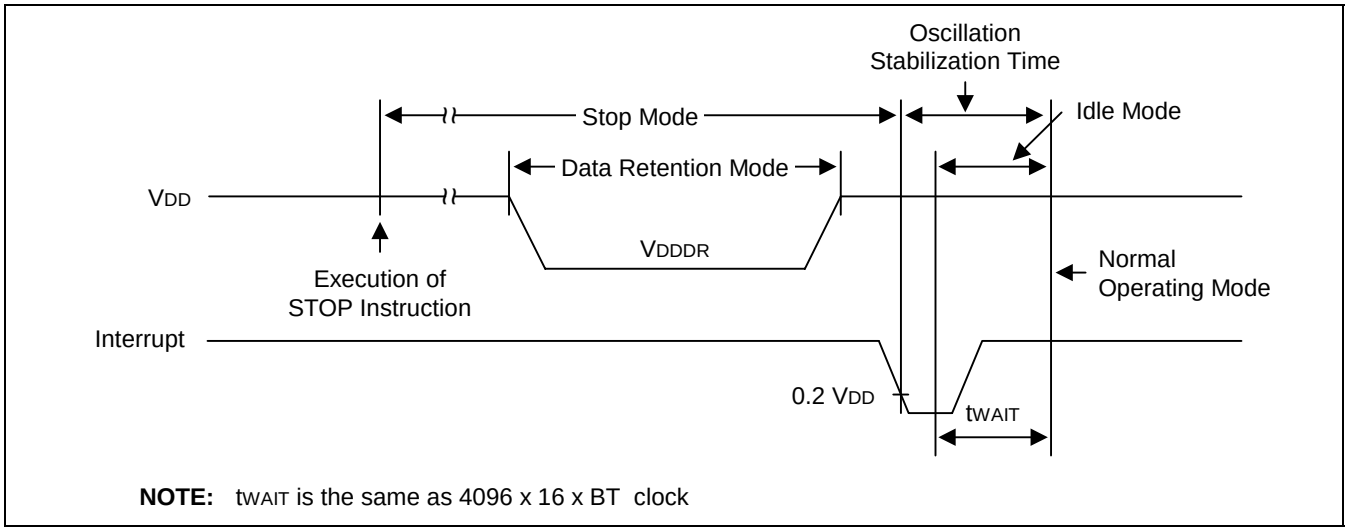
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention Supply Voltage	V_{DDDR}	Stop mode	2	–	5.5	V
Data Retention Supply Current	I_{DDDR}	Stop mode, V_{DDDR} = 2.0 V	–	–	8	µA

NOTE: Supply current does not include current drawn through internal pull-up resistors or external output current loads.



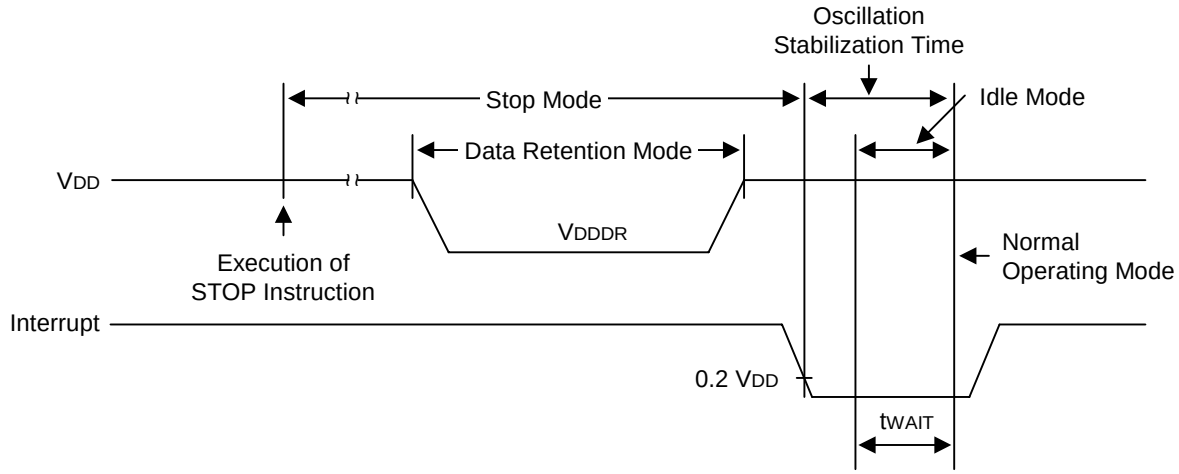
NOTE: tWAIT is the same as 4096 x 16 x 1/f OSC.

Figure 20-5. Stop Mode Release Timing initiated by nRESET



NOTE: tWAIT is the same as 4096 x 16 x BT clock

Figure 20-6. Stop Mode (Main) Release Timing Initiated by Interrupts



NOTE: When the case of select the fxx/128 for basic timer input clock before enter the stop mode.
t_{WAIT} = 128 x 16 x (1/32768) = 62.5 ms

Figure 20-7. Stop Mode (Sub) Release Timing Initiated by Interrupts

Table 20-10. Serial I/O Timing Characteristics

(T_A = – 40°C to + 85°C, V_{DD} = 2.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SCK Cycle Time	t_{CKY}	External SCK source	1000	–	–	ns
		Internal SCK source	1000			
SCK High, Low Width	t_{KH}, t_{KL}	External SCK source	500	–	–	
		Internal SCK source	$t_{KCY}/2 - 50$			
SI Setup Time to SCK Low	t_{SIK}	External SCK source	250	–	–	
		Internal SCK source	250			
SI Hold Time to SCK High	t_{KSI}	External SCK source	400	–	–	
		Internal SCK source	400			
Output Delay for SCK to SO	t_{KSO}	External SCK source	–	–	300	
		Internal SCK source			250	

NOTE: "SCK" means serial I/O clock frequency, "SI" means serial data input, and "SO" means serial data output.

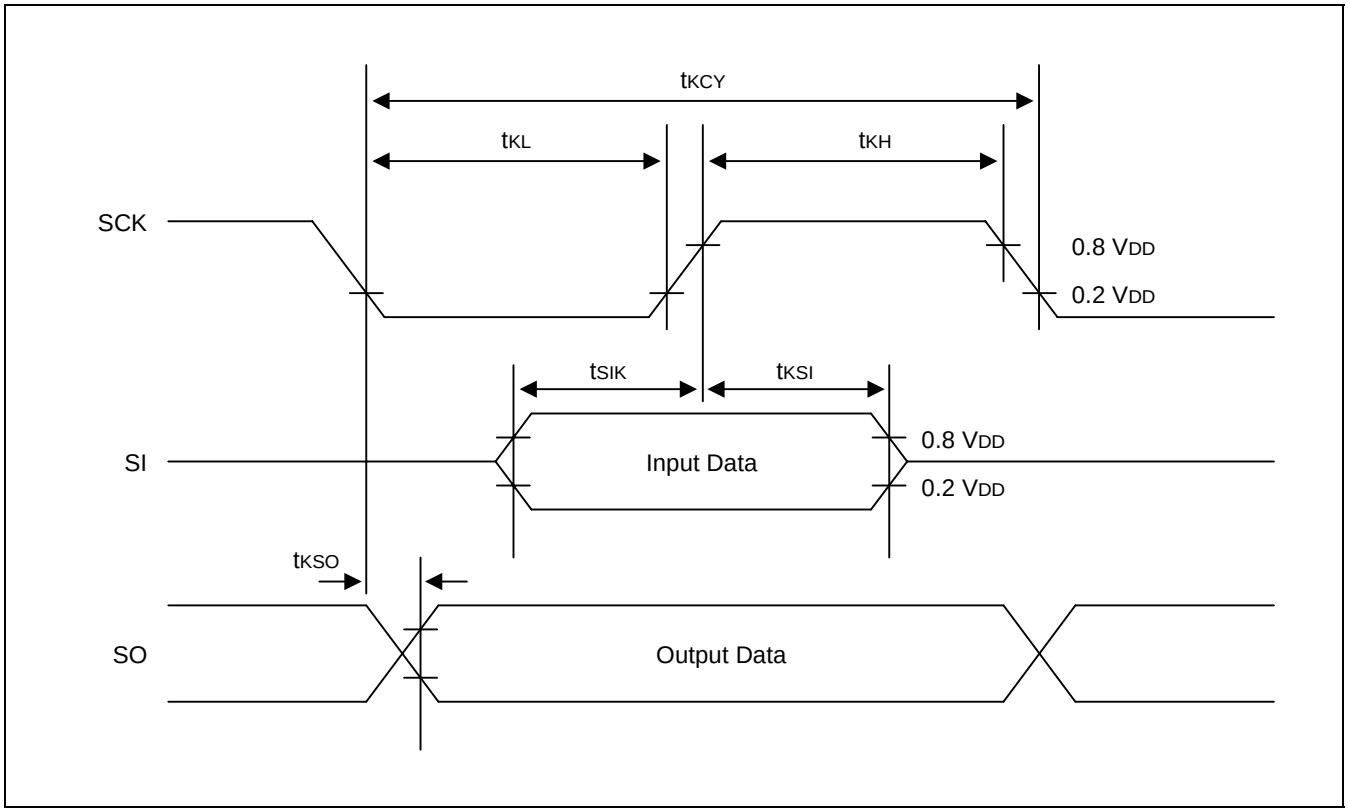


Figure 20-8. Serial Data Transfer Timing

Table 20-11. UART Timing Characteristics in Mode 0

(T_A = – 40°C to + 85°C, V_{DD} = 2.0 V to 5.5 V, Load capacitance = 80 pF)

Parameter	Symbol	Min	Typ.	Max	Unit
Serial port clock cycle time	t_{SCK}	500	$t_{CPU} \times 6$	700	ns
Output data setup to clock rising edge	t_{S1}	300	$t_{CPU} \times 5$	–	
Clock rising edge to input data valid	t_{S2}	–	–	300	
Output data hold after clock rising edge	t_{H1}	$t_{CPU} – 50$	t_{CPU}	–	
Input data hold after clock rising edge	t_{H2}	0	–	–	
Serial port clock High, Low level width	t_{HIGH}, t_{LOW}	200	$t_{CPU} \times 3$	400	

NOTES:
1. All timings are in nanoseconds (ns) and assume a 10-MHz CPU clock frequency.
2. The unit t_{CPU} means one CPU clock period.

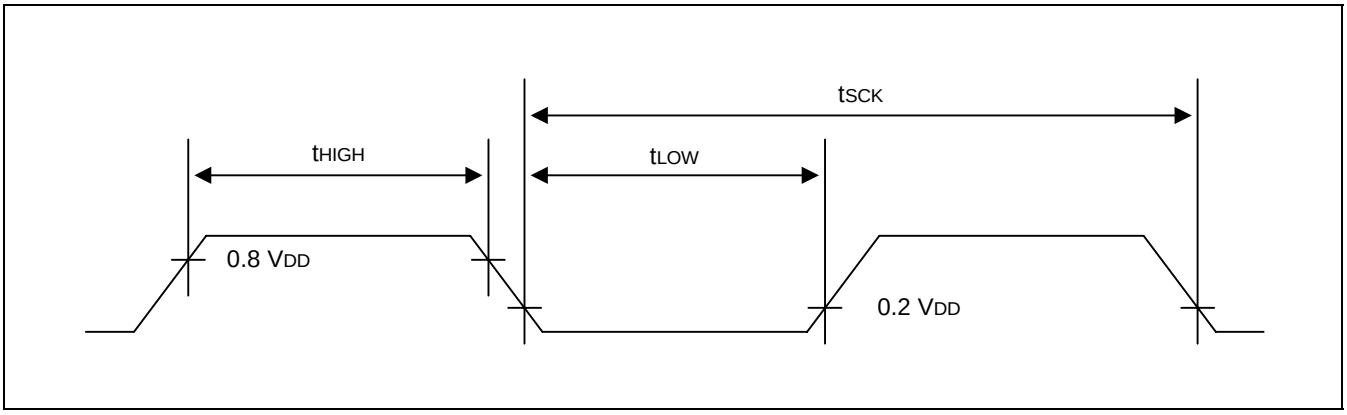


Figure 20-9. Waveform for UART Timing Characteristics

Table 20-12. A/D Converter Electrical Characteristics

(T_A = – 40°C to + 85°C, V_{DD} = 2.0 V to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Test Conditions	Min	Typ.	Max	Unit
Resolution			–	10	–	bit
Total accuracy		V_{DD} = 5.12 V	–	–	± 3	LSB
Integral linearity error	ILE	CPU clock = 10 MHz AV_{REF} = 5.12 V		–	± 2	
Differential linearity error	DLE	AV_{SS} = 0 V		–	± 1	
Offset error of top	EOT			± 1	± 3	
Offset error of bottom	EOB			± 0.5	± 2	
Conversion time (1)	t_{CON}	10-bit conversion 50 x 4/f_{OSC} (3), f_{OSC} = 10 MHz	–	25	–	μs
Analog input voltage	V_{IAN}	–	AV_{SS}	–	AV_{REF}	V
Analog input impedance	R_{AN}	–	2	1000	–	MΩ
Analog reference voltage	AV_{REF}	–	2.5	–	V_{DD}	V
Analog ground	AV_{SS}	–	V_{SS}	–	V_{SS} + 0.3	
Analog input current	I_{ADIN}	AV_{REF} = V_{DD} = 5 V	–	–	10	μA
Analog block current (2)	I_{ADC}	AV_{REF} = V_{DD} = 5 V	–	1	3	mA

NOTES:

1. "Conversion time" is the time required from the moment a conversion operation starts until it ends.
2. I_{ADC} is operating current during A/D conversion.
3. f_{OSC} is the main oscillator clock.

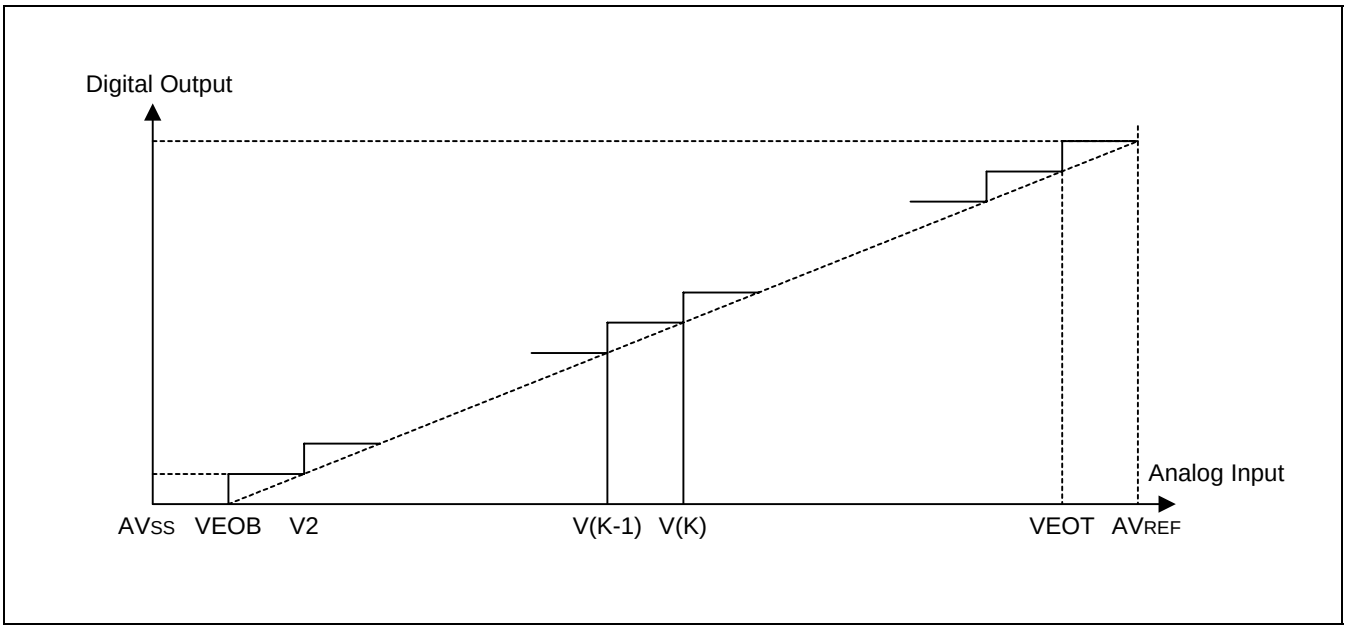


Figure 20-10. Definition of DLE and ILE

Table 20-13. LVR Circuit Characteristics

(T_A = 25 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Low voltage reset	V_{LVR}	–	1.9 2.6 3.5	2.2 3.0 4.0	2.5 3.4 4.5	V

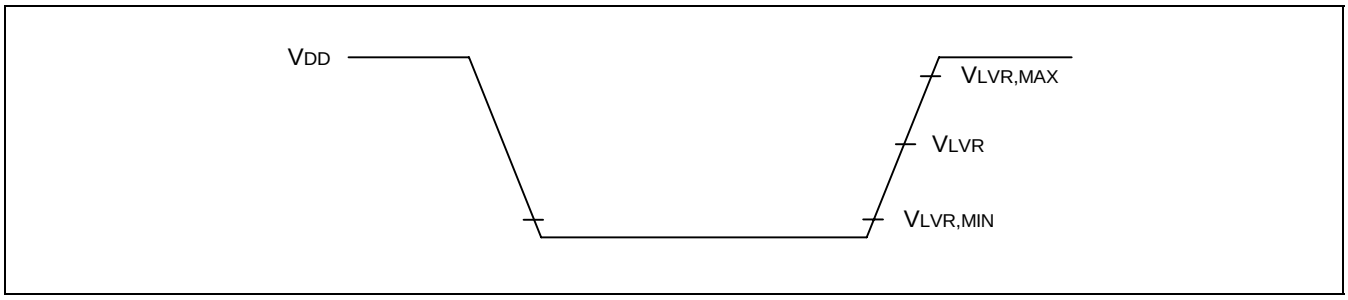


Figure 20-11. LVR Reset Timing

Table 20-14. AC Electrical Characteristics for Internal Flash ROM

(T_A = –25 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Flash Erase/Write/Read Voltage	Fewrv	V_{DD}	2.0	5.0	5.5	V
Programming Time (1)	Ftp		32	–	60	μS
Sector Erasing Time (2)	Ftp1		10	–	20	mS
Chip Erasing Time (3)	Ftp2		50	–	100	mS
Data Access Time	Ft_{RS}	V_{DD} = 2.0 V	–	250	–	nS
Number of Writing/Erasing	FNwe	–	10,000	–	–	Times
Data Retention	Ftdr	–	10	–	–	Years

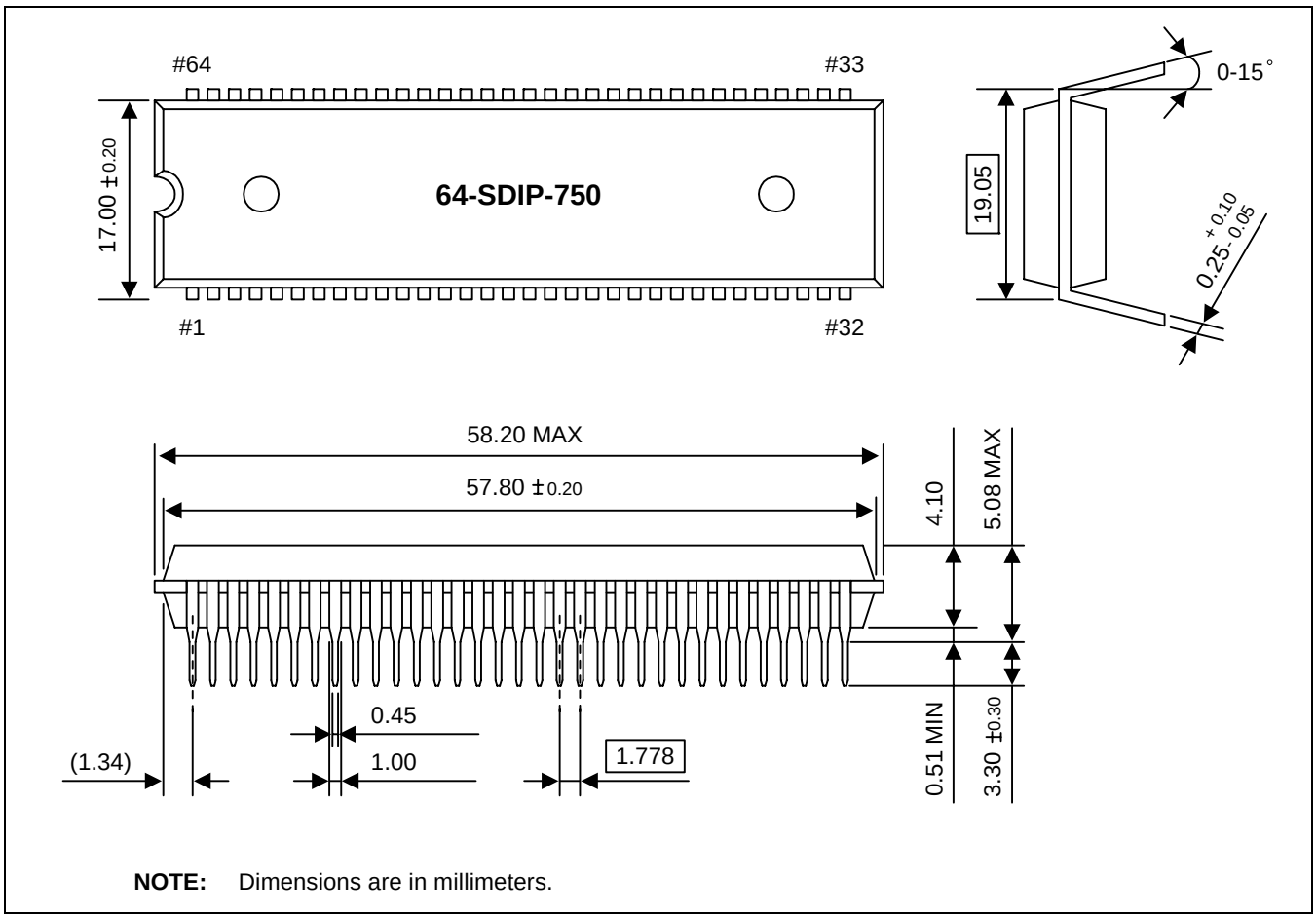
NOTES:

1. The programming time is the time during which one byte (8-bit) is programmed.
2. The Sector erasing time is the time during which all 128-bytes of one sector block is erased.
3. In the case of S3F84NB, the chip erasing is available in Tool Program Mode only.

21 MECHANICAL DATA

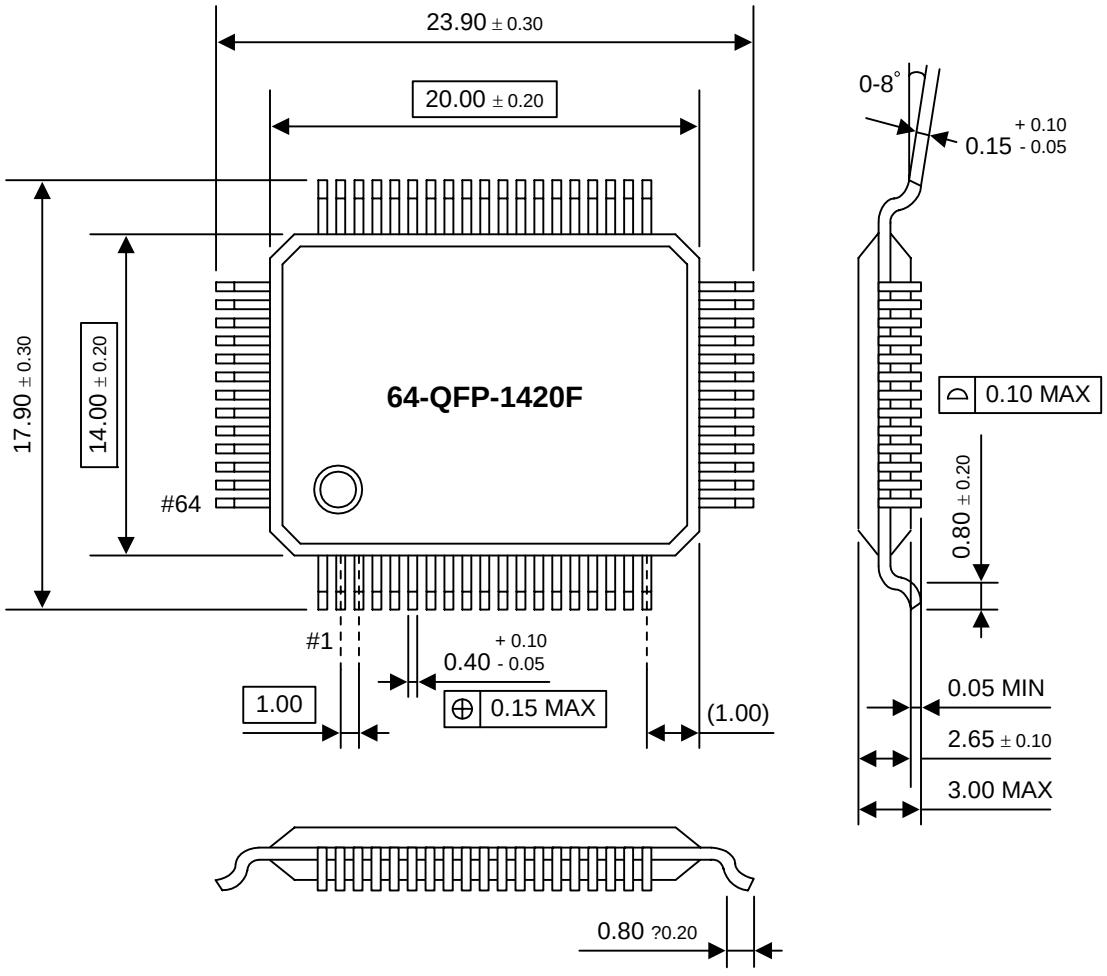
OVERVIEW

The S3F84NB microcontrollers are available in a 64-SDIP-750, 64-QFP-1420F package.



NOTE: Dimensions are in millimeters.

Figure 21-1. 64-SDIP-750 Package Dimensions



NOTE: Dimensions are in millimeters.

Figure 21-2. 64-QFP-1420F Package Dimensions

22 DEVELOPMENT TOOLS

OVERVIEW

Samsung provides a powerful and easy-to-use development support system on a turnkey basis. The development support system is composed of a host system, debugging tools, and supporting software. For a host system, any standard computer that employs Win95/98/2000 as its operating system can be used. A sophisticated debugging tool is provided both in hardware and software: the powerful in-circuit emulator, SMDS2+ or SK-1000, for the S3C7-, S3C9-, and S3C8- microcontroller families. SMDS2+ is a newly improved version of SMDS2, and SK-1000 is supported by a third party tool vendor. Samsung also offers supporting software that includes, debugger, an assembler, and a program for setting options.

SHINE

Samsung Host Interface for In-Circuit Emulator, SHINE, is a multi-window based debugger for SMDS2+. SHINE provides pull-down and pop-up menus, mouse support, function/hot keys, and context-sensitive hyper-linked help. It has an advanced, multiple-windowed user interface that emphasizes ease of use. Each window can be easily sized, moved, scrolled, highlighted, added, or removed.

SASM

The SASM is a re-locatable assembler for Samsung's S3C8-series microcontrollers. The SASM takes a source file containing assembly language statements and translates them into a corresponding source code, an object code and comments. The SASM supports macros and conditional assembly. It runs on the MS-DOS operating system. As it produces the re-locatable object codes only, the user should link object files. Object files can be linked with other object files and loaded into memory. SASM requires a source file and an auxiliary register file (device_name.reg) with device specific information.

SAMA ASSEMBLER

The Samsung Arrangeable Microcontroller (SAM) Assembler, SAMA, is a universal assembler, and generating an object code in the standard hexadecimal format. Assembled program codes include the object code used for ROM data and required In-circuit emulators program control data. To assemble programs, SAMA requires a source file and an auxiliary definition (device_name.def) file with device specific information.

HEX2ROM

HEX2ROM file generates a ROM code from a HEX file which is produced by the assembler. A ROM code is needed to fabricate a microcontroller which has a mask ROM. When generating a ROM code (.OBJ file) by HEX2ROM, the value "FF" is automatically filled into the unused ROM area, up to the maximum ROM size of the target device.

TARGET BOARDS

Target boards are available for all the S3C8-series microcontrollers. All the required target system cables and adapters are included on the device-specific target board. TB84NB is a specific target board for the S3F84NB development.

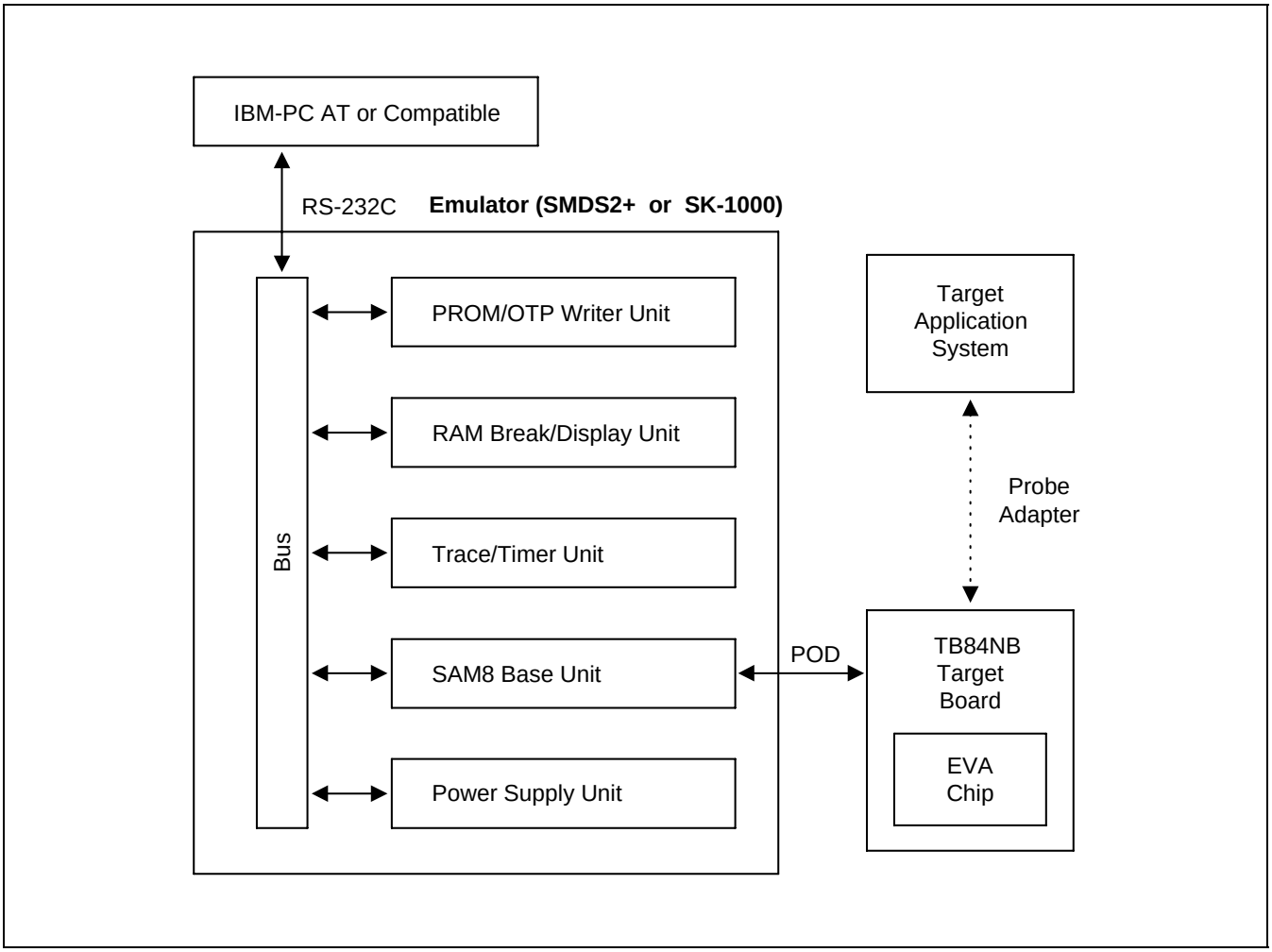


Figure 22-1. SMDS+ or SK-1000 Product Configuration

TB84NB TARGET BOARD

The TB84NB target board is used for the S3F84NB microcontroller.
It is supported by the SMDS2+ or SK-1000 development system (In-Circuit Emulator). Figure 22-2. TB84NB Target Board Configuration

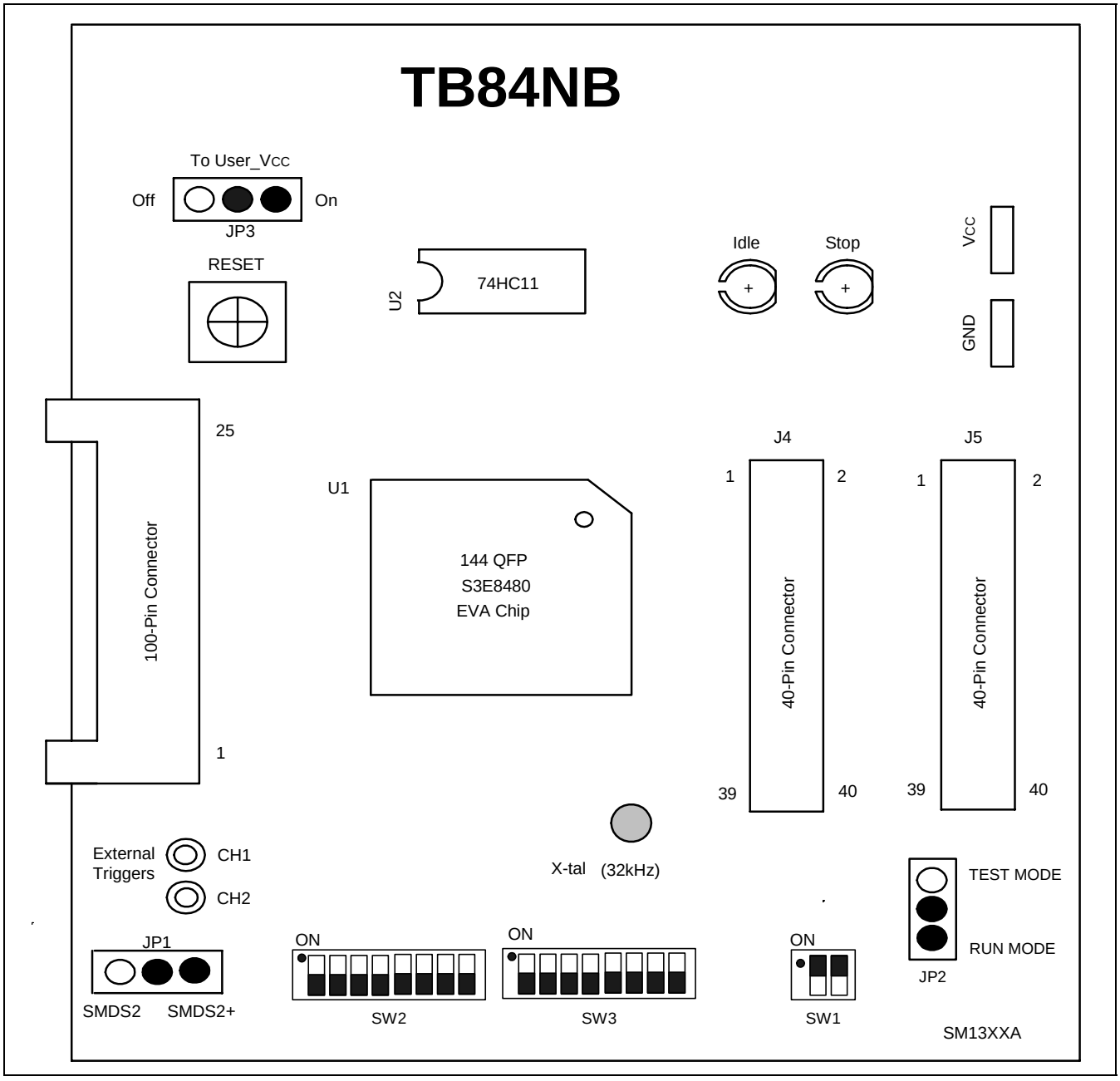
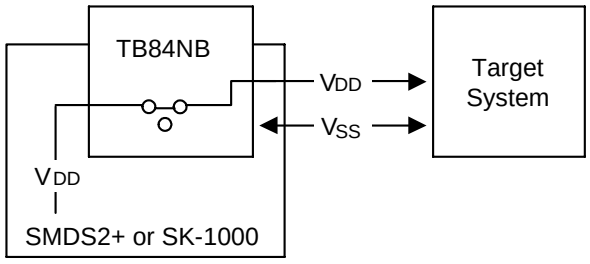
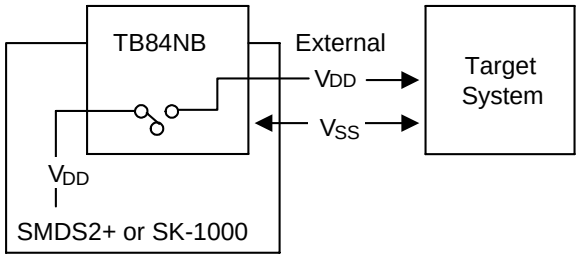


Figure 22-2. S3F84NB Target Board Configuration

NOTE: The circle or rectangle filled in black means the default position of jumpers or switches.

Table 22-1. Power Selection Settings for TB84NB

To User_Vcc' Settings	Operating Mode	Comments
To User_VDD Off ○ ● ● On		SMDS2+ or SK-1000 supplies V_{DD} to the target board (evaluation chip) and the target system.
To User_VDD Off ● ● ○ On		SMDS2+ or SK-1000 supplies V_{DD} only to the target board (evaluation chip). The target system must have a power supply of its own.

NOTE: The following symbol in the "To User_Vcc" Setting column indicates the electrical short (off) configuration:

SMDS2+ Selection (SAM8)

In order to write data into program memory that is available in SMDS2+, the target board should be selected to be for SMDS2+ through a switch as follows. Otherwise, the program memory writing function is not available.

Table 22-2. The SMDS2+ Tool Selection Setting

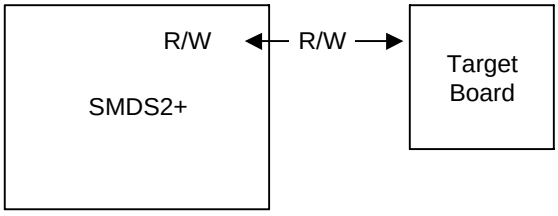
"JP1" Setting	Operating Mode
SMDS2 ○ ● ● SMDS2+	

Table 22-3. Using Single Header Pins to Select Operation Mode

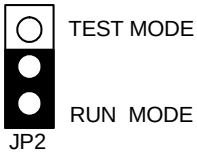
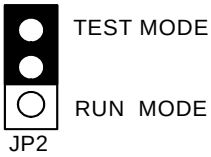
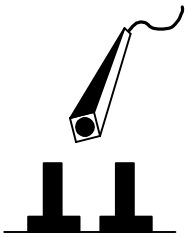
	**Run Mode.**
	**Test Mode.**

Table 22-4. Using Single Header Pins as the Input Path for External Trigger Sources

Target Board Part	Comments
External Triggers 	 You can connect an external trigger source to one of the two external trigger channels (CH1 or CH2) for the SMDS2+ breakpoint and trace functions.

IDLE LED

This LED is ON when the evaluation chip (S3E84N0) is in idle mode.

STOP LED

This LED is ON when the evaluation chip (S3E84N0) is in stop mode.

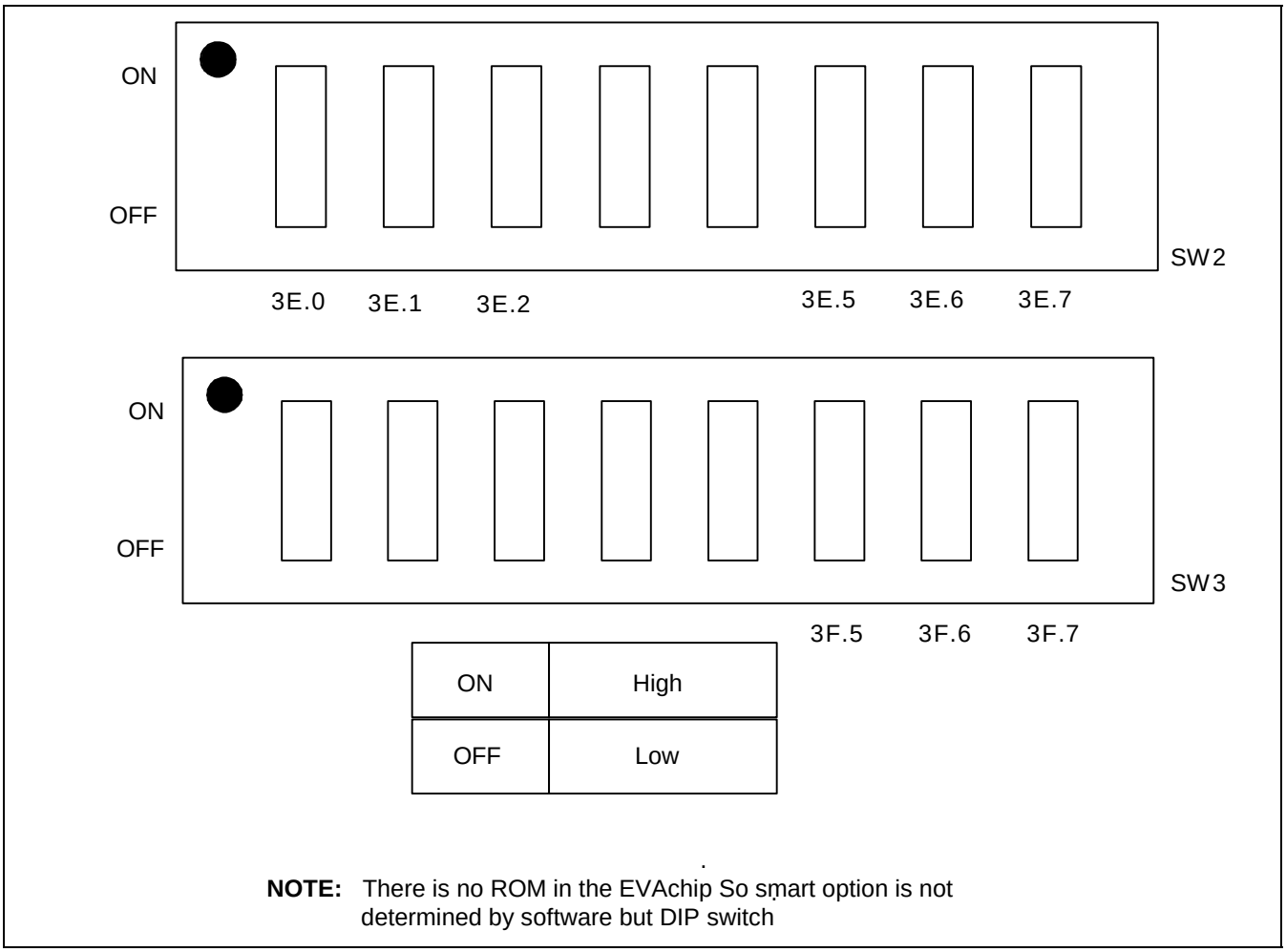


Figure 22-3. DIP Switch for Smart Option

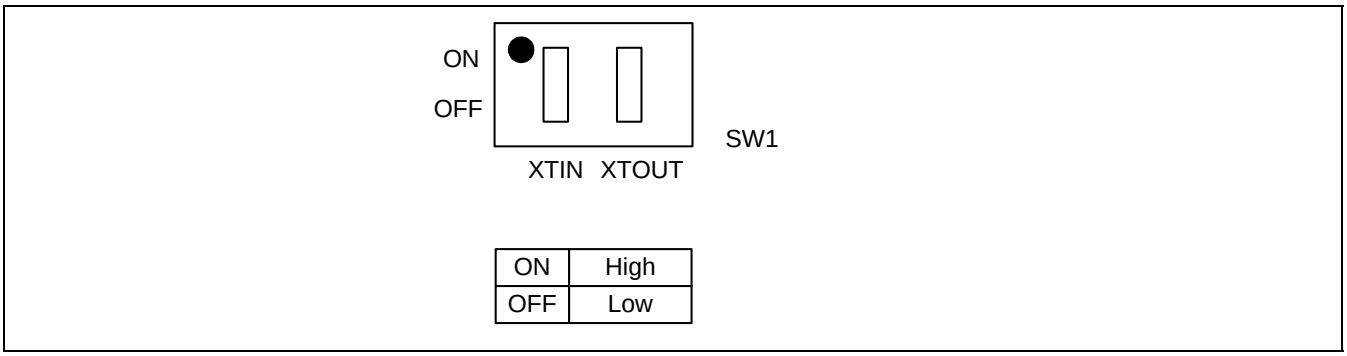


Figure 22-4. DIP Switch for Port 6 (Sub Oscillator or normal I/O)

SWITCH	ON	OFF
SW1.1	Connection to XTin enable	Connection to XTin disable
SW1.2	Connection to XTout enable	Connection to XTout disable

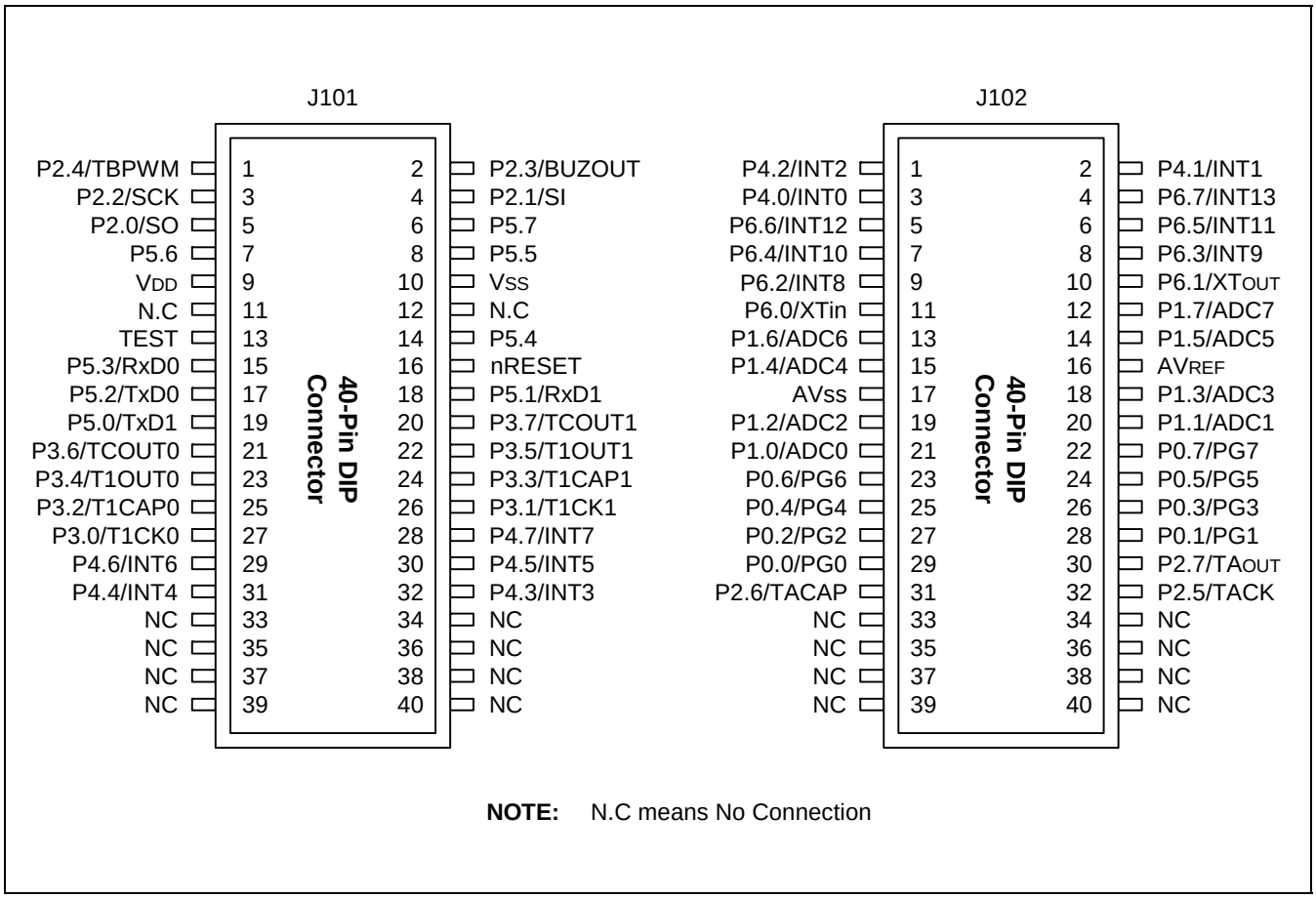


Figure 22-5. 40-Pin Connector Pin Assignment for TB84NB

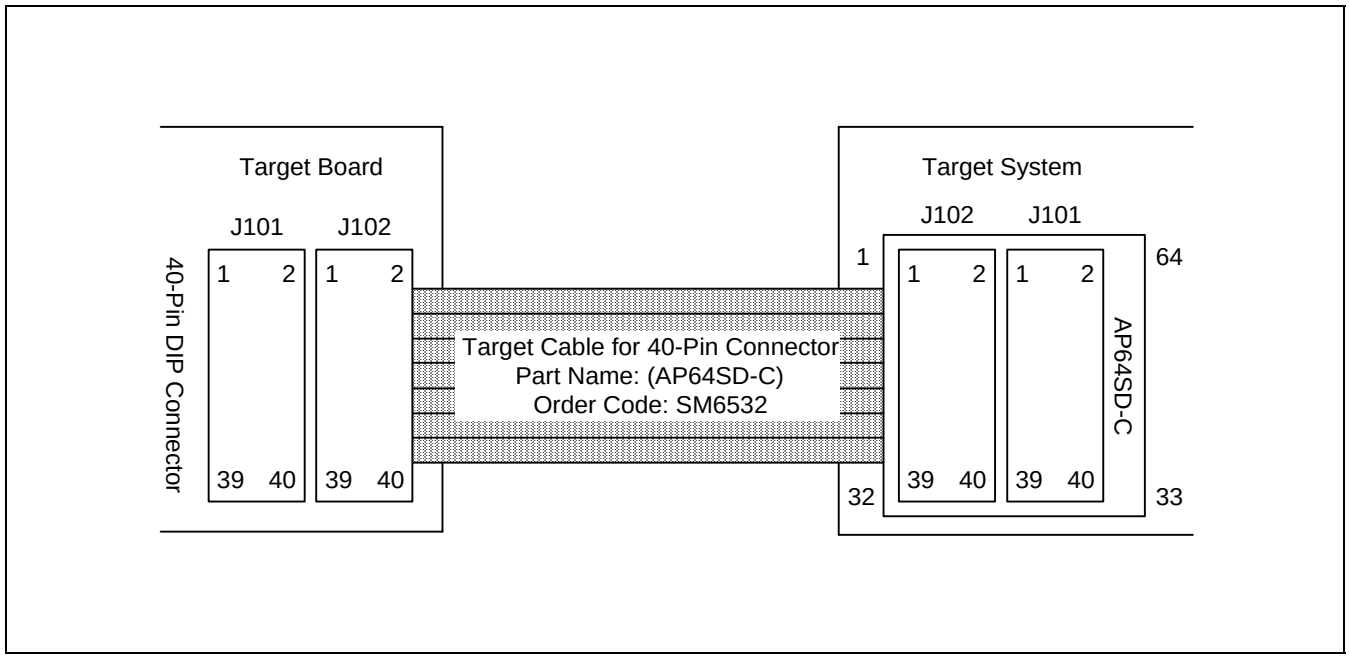


Figure 22-6. TB84NB Adapter Cable for 64-SDIP Package

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