The MELSEC Q Series Automation Platform

Q Series PACs are multi-disciplinary automation platforms addressing the needs of both OEMs and end users. The Q Series is the original multi-CPU system, with up to 4 CPUs to divide-and-conquer larger applications. It provides scalable automation solutions to both small and very large systems, offering a broad spectrum of automation capabilities. Additional CPUs and intelligent function module expansions allow the Q series to handle sophisticated motion, process control, PC and C language based control, MES IT interfacing, and numerous types of communication and networking.

Key Features:

- CPU types ranging from small/medium systems, to complex networked systems with tens of thousands of I/O
- Reduced lifecycle costs via remote system management & maintenance
- Redundant CPU capability available for hot-backup of critical systems
- Multiple CPU capability (up to 4 CPUs) adding open ended system performance and flexibility
- Multiple programs allowing concurrent development, code reuse, better program organization and faster troubleshooting for less downtime
- Multiple simultaneous access to the system allowing for faster system debugging and maintenance
- Networking & communication options distribute Q Series systems over wide areas while reducing wiring costs
- Sequence CPUs can also address process applications by means of built-in PID capabilities
- Extremely compact package saves panel costs
- Certified by UL, cUL, CE (as indicated), as well as DNV, ABS, RINA, BV, LR and NK shipping approvals for all Q Series products

Required Manuals

Model Number	Description	Contents	Included with CPU?	Stk Item
IB(NA)0800061	QCPU(Q mode) CPU Module User's Manual (Hardware)	General specs, CE compliance information, Installation, safety requirements, Power supply wiring, overview of system parts	No (included with base units)	–
SH(NA)080483ENG	Q CPU (Q Mode) User's Manual (Hardware Design, Maintenance & Inspection)	CPU H/W specs, PSU spec, Base Unit specs, CE compliance information, Maintenance & inspection, Installation, Troubleshooting	No (purchase separately)	–
SH(NA)080484ENG	QCPU(Q Mode) User's Manual (Function Explanation, Program Fundamentals)	CPU specifications, system configuration, programming basics, I/O assignments, memory organization, CPU functions, communication with intelligent function modules, parameters & devices, program up/downloads, overview of multiple program architecture, programming basics, overview of multiple CPU system	No (purchase separately)	–
SH(NA)080485ENG	QCPU User's Manual (Multiple CPU System)	Outline, system configuration, concept for multiple CPU system, communication between CPU modules, processing time of QCPU in multiple CPU system, parameter added for multiple CPU system, precautions for use of AnS Series module, starting up the multiple CPU system	No (purchase separately)	–
SH(NA)080039	QCPU(Q Mode)/QnACPU Programming Manual (Common Instructions)	General Description, Instruction Tables, Configuration of Instructions, How To Read Instructions, Sequence Instructions, Basic Instructions, Application Instructions, Instructions For Data Link, QCPU Instructions, Redundant System Instructions, Error Codes	No (purchase separately)	–
SH(NA)080041	QCPU(Q Mode)/QnACPU Programming Manual (SFC)	General Description, System Configuration, Specifications, SFC Program Configuration, SFC Program Processing Sequence, SFC Program Execution	No (purchase separately)	–
SH(NA)080076	Q CPU (Q Mode) Programming Manual (MELSAP-L)	General Description, System Configuration, Specifications, SFC Program Configuration, SFC Program Processing Sequence, SFC Program Execution	No (purchase separately)	–
SH(NA)080040	QCPU(Q Mode)/QnACPU Programming Manual (PID Control Instructions)	General Description, System Configuration for PID Control, PID Control Specifications, Functions of PID Control, PID Control Procedure, PID Control Instructions, How To Read Explanations For Instructions, Incomplete Derivative PID Control Instructions and Program Examples, Complete Derivative PID Control Instructions and Program Examples	No (purchase separately)	–
SH(NA)080366	Programming Guide Book for Structured Text (ST)	Covers Structured Text programming method	No (purchase separately)	–

Note: Many of these manuals are available by free download from our website, www.meau.com

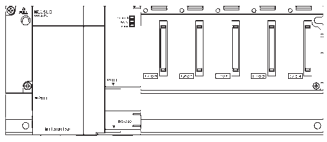
Ⓐ MELSEC Q Series CPUs

Basic Model Sequence CPUs

These CPUs offer an economical entry-level version of the Q Series for small scale systems.

Key Features:

- Multiple CPU support; use up to three CPUs to combine sequence, process, motion & PC control on a single system (Version B or later)
- Compatible with Q Series Intelligent Function Utility configuration tools
- Offers full range of Q Series network & communication features, including CC-Link IE 100Mbit Ethernet, MELSECNET/H
- Integrated PSU, CPU and base unit available to simplify system construction with Q00JCPUs



- Built in serial communications via CPU port (using MELSEC Communication (MC) protocol)
- Security functions
- Flash memory for programs & parameters
- Supports floating point, function block, PID and SFC programming (Version B or later)

MELSEC Q Series Basic Sequence CPU

Model Number		Q00JCPU-E	Q00JCPU-S8 (*5)	Q00CPU	Q01CPU
Stocked Item		S	S	S	S
Certification		UL • cUL • CE	UL • cUL • CE	UL • cUL • CE	UL • cUL • CE
Hardware Format		Combined CPU, PSU and 5-Slot Base Unit	Combined CPU, PSU and 8 slot Base Unit	CPU only	CPU only
Control Method		Repeated operation using stored program			
I/O Control Method		Refresh mode			
Programming Language (Sequence Control Dedicated Language)		Relay symbol type (ladder) logic symbolic language (list)			
Processing Speed (Sequence Instruct)	LD X0	200ns		160ns	100ns
	MOV (MOV D0 D1)	700ns		560ns	350ns
Total Number of Instructions		249 (excluding intelligent function module dedicated instructions)			
Constant Scan (ms) (Program Start at Given Time Intervals)		1 to 2000ms (can be specified in 1ms increments)			
Program Capacity (*1)		8k steps (32 kbyte)		8k steps (32 kbyte)	14k steps (56 kbyte)
Memory Capacity	Program Memory (Drive 0)	58 kbyte		94 kbyte	
	Standard RAM (Drive 3)	0		128 kbyte	
	Standard ROM (Drive 4)	58 kbyte		94 kbyte	
Number of Stored Programs	Program Memory	1	1	1	1
	Standard ROM	1	1	1	1
Number of Stored File Registers	Standard RAM	—	—	1	1
Number of I/O Device Points		2048 points (X/Y0 to 7FF) (*2)			
Number of I/O Points		256 points (X/Y0 to FF)		1024 points (X/Y0 to 3FF) (*3)	
Internal Relay [M]		Default 8192 points (M0 to 8191)			
Latch Relay [L]		2048 points (L0 to 2047)			
Link Relay [B]		2048 points (B0 to 7FF)			
Timer [T]		Default 512 points (T0 to 511) (used as low-speed or high-speed timer) Switching between low-speed and high-speed timers is set by instruction Low-speed/high-speed timer timing increments are parameter-set (Low-speed timer: 1 to 1000ms, 1ms increments, default 100ms) (High-speed timer: 0.1 to 100ms, 0.1ms increments, default 10ms)			
Retentive Timer [ST]		Default 0 point (ST0 to 511) (used as low-speed or high-speed timer) Switching between low-speed and high-speed timers is set by instruction Low-speed/high-speed timer timing increments are parameter-set. (Low-speed timer: 1 to 1000ms, 1ms increments, default 100ms) (High-speed timer: 0.1 to 100ms, 0.1ms increments, default 10ms)			
Counter [C]		Normal counters Default 512 points (C0 to 511) Interrupt counters Max. 128 (Default 0 points, parameter setting)			
Data Register [D]		Default 11136 points (D0 to 11135)			
Link Register [W]		Default 2048 points (W0 to 7FF)			
Annunciator [F]		Default 1024 points (F0 to 1023)			
Edge Relay [V]		Default 1024 points (V0 to 1023)			
File Register	[R]	None		32768 points (R0 to 32767)	
	[ZR]	None		65536 points (ZR0 to 65535)	
Special Link Relay [SB]		1024 points (SB0 to 3FF)			
Special Link Register [SW]		1024 points (SW0 to 3FF)			
Step Relay (*4)		2048 points (SW0 to 3FF)			
Index Register [Z]		10 points (Z0 to 9)			
Pointer [P]		300 points (P0 to 299)			
Interrupt Pointer [I]		128 points (I0 to 127) In parameters, set the cyclic intervals of the system interrupt pointers I28 to I31 (2 to 1000ms, 1ms increments)			
Special Relay [SM]		1024 points (SM0 to 1023)			
Special Register [SD]		1024 points (SD0 to 1023)			
Function Input [FX]		16 points (FX0 to F)			
Function Output [FY]		16 points (FY0 to F)			
Function Register [FD]		5 points (FD0 to 4)			
Link Direct Device		Device for direct access to link device. Dedicated. Specified format: J□□\□□			
Intelligent Function Module Direct Device		Device for direct access to buffer memory of intelligent function module. Specified format: U□□\G□□			
Latch (Power Failure Comp.) Range		L0 to 2047 (default) (Latch range setting can be made for B, F, V, T, ST, C, W and D)			
Remote RUN/PAUSE Contact		1 point can be set for each RUN and PAUSE contacts from X0-7FF.			
Clock Function		Year, month, day, hour, minute, second, day of week (Automatic leap year judgment) Accuracy –3.2 to +5.27 (TYP +1.98) s/day at 0°C Accuracy –2.57 to +5.27 (TYP +2.22) s/ day at 25°C Accuracy –11.68 to +3.65 (TYP –2.64) s/ day at 55°C			
Permissible Instantaneous Power Failure Time		20ms		Depends on power supply module	
5VDC Internal Current Consumption (A)		0.26		0.25	0.27
Weight (kg)		0.66		0.13	
Dimensions W x H x D mm (in)		245 (9.65) x 98 (3.86) x 98 (3.86)	328 (12.92) x 98 (3.86) x 98 (3.86)	27.4 (1.08) x 98 (3.86) x 89.3 (3.52)	

Notes:

1. Maximum actual program size is (program capacity—34 steps).
2. Sum of the number of I/O points on the main/extension base directly controlled by the CPU module and the number of I/O points controlled as remote I/O by the remote I/O network.
3. Number of I/O points on the main/extension base directly controlled by the CPU module.
4. The "Step relay" is a device for the SFC function, only applicable to version B CPUs or higher.
5. Q00JCPU-S8 has the same functionalities as Q00JCPU-E.