AN-835
APPLICATION NOTE

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Understanding High Speed ADC Testing and Evaluation

by Brad Brannon and Rob Reeder

SCOPE

This document describes both the characterization and production test methods used by Analog Devices' High Speed Converter Group to evaluate high speed ADCs. While this application note should be considered a reference, it is not a substitute for a product data sheet.

DYNAMIC TEST HARDWARE SETUP

SNR, SINAD, worst spur, and IMD are tested using a hardware setup similar to that shown in Figure 1. In production tests, the test hardware is highly integrated, but the hardware principles are the same. The basic setup for dynamic testing includes a signal generator, band-pass filter, test fixture, low noise power supply, encode source (often integrated on the evaluation board), data acquisition module, and data analysis software. Analog Devices provides application hardware and software to aid in bench evaluation. See the ADC FIFO Kit section.

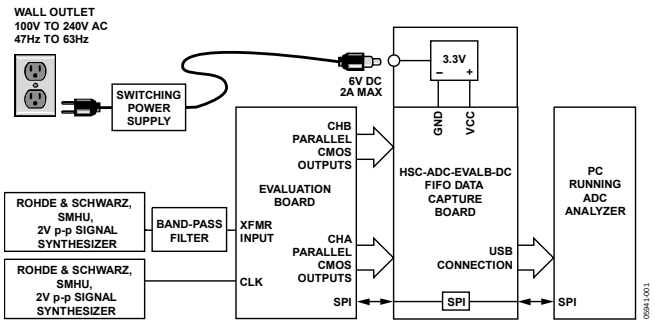


Figure 1. Typical Characterization Test Setup

ADC FIFO KIT

The high speed ADC FIFO evaluation kit (HSC-ADC-EVALA-SC/HSC-ADC-EVALA-DC and HSC-ADC-EVALB-SC/HSC-ADC-EVALB-DC includes a memory board to capture blocks of digital data from Analog Devices' high speed analog-to-digital converter (ADC) evaluation boards and ADC Analyzer™ software. For more information on the ADC FIFO evaluation kit, visit www.analog.com/FIFO.

The FIFO board can be connected to a PC through a standard USB cable and used with the ADC Analyzer software to quickly evaluate the performance of high speed ADCs. Users can view an FFT for a specific analog input and clock rate and analyze SNR, SINAD, SFDR, and harmonic information. There are single-channel and dual-channel versions of the FIFO board available. The FIFO data sheet should be consulted to determine which version is required for a specific ADC. LVDS and serial output devices may need an additional adapter board called HSC-ADC-FPGA. This will be specified in the product data sheet. For more detailed information on HSC-ADC-FPGA serial LVDS adapter board, FIFO, and how the ADC Analyzer software works see the Analog Devices website www.analog.com/FIFO.

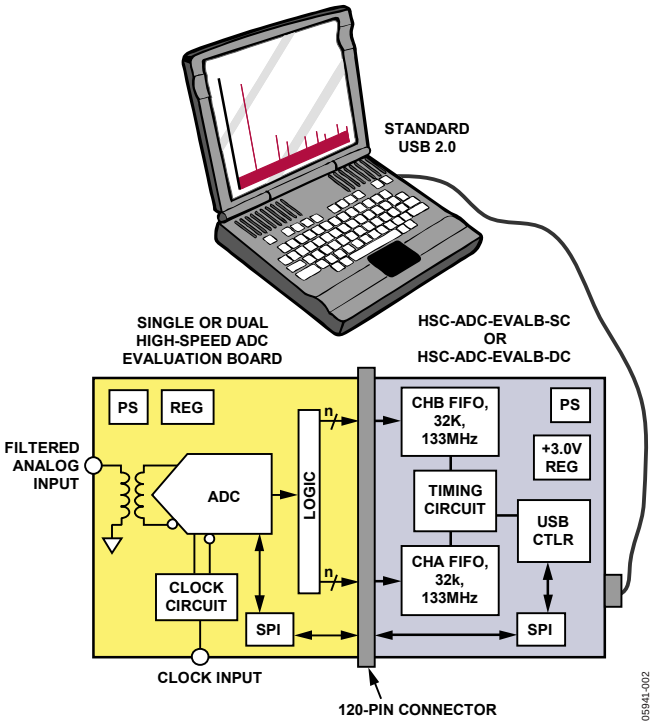


Figure 2. Typical ADI ADC FIFO Kit Setup

TABLE OF CONTENTS

REVISION HISTORY

4/06—Revision 0: Initial Version

BACKGROUND

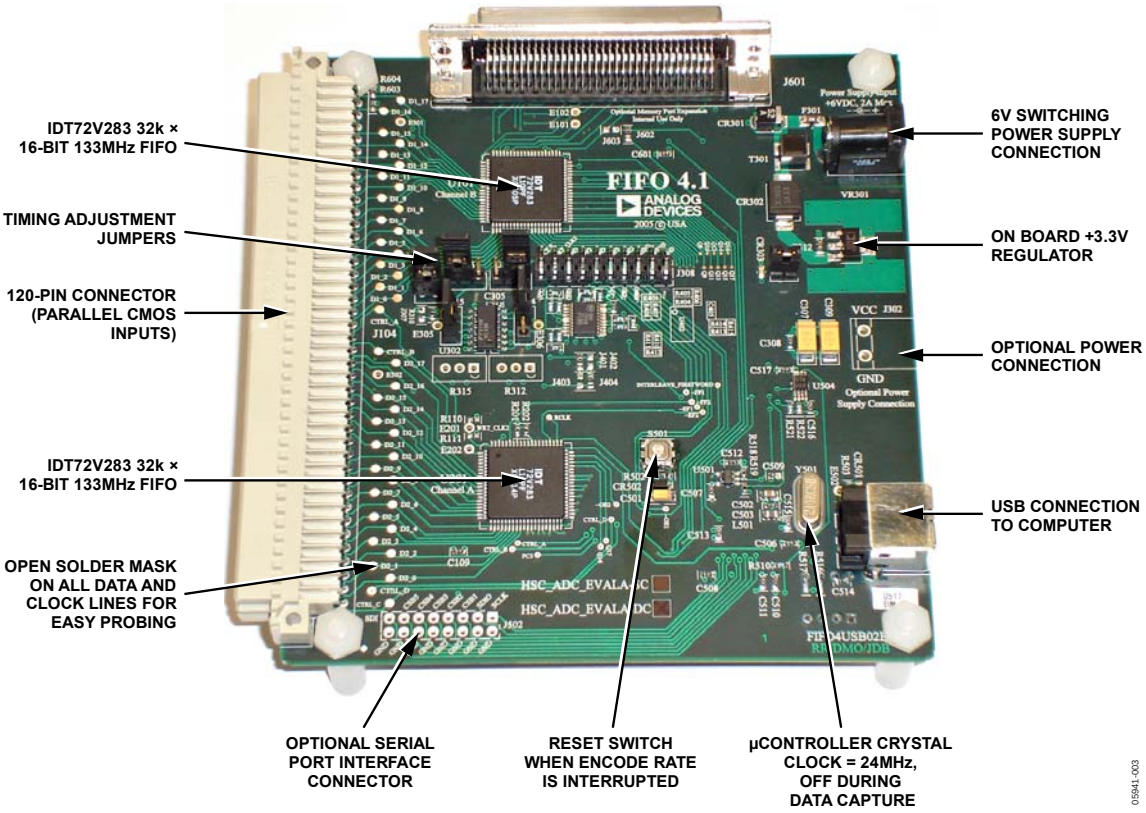


Figure 3. Dual-Channel ADC FIFO Board

ADIsimADC

ADIsimADC™ is Analog Devices ADC behavioral modeling tool. ADIsimADC accurately models many of the time and frequency domain errors common to ADCs. This tool can be invaluable in terms of both simple converter selection and complete system simulation. The tool is fully integrated into the ADC Analyzer software to aid in simple converter selection; it is also supported by several third-party CAD vendors. Currently, ADIsimADC is supported by MATLAB®, C++, National Instruments' LabVIEW™ and Signal Express, Agilent's ADS, and Applied Wave Research's Visual System Stimulator™. Others will be available in the future. The tool can be downloaded from the website along with a complete collection of current models. Links are provided to third-party tools that support ADIsimADC. (For more information on ADIsimADC behavioral modeling, visit www.analog.com/ADIsimADC.)

As mentioned, the tool is provided with ADC Analyzer software, which provides direct access to ADIsimADC, allowing users to simulate a given ADC based on a behavioral model of the ADC (no hardware required). Information about ADIsimADC can be found at www.analog.com/ADIsimADC. For more detailed information on ADIsimADC, see the AN-737 Application Note.

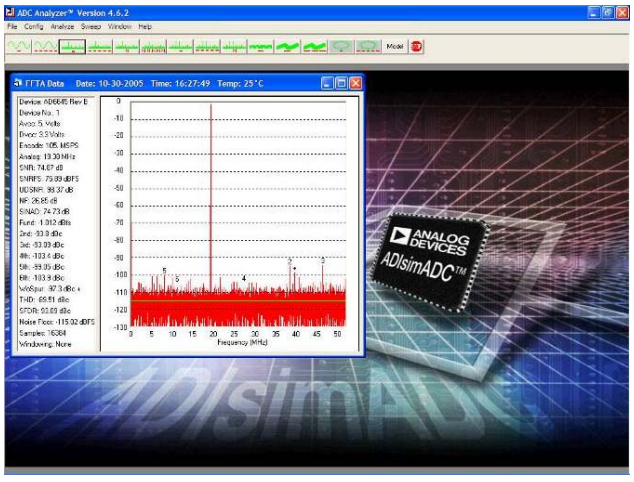


Figure 4. ADC Analyzer

ANALOG SIGNAL SOURCE

Usually, dynamic testing employs a Rohde & Schwarz (www.rohde-schwarz.com) SMA/SMHU/SMG/SMGU, an Agilent (www.agilent.com) 8644 signal generator, or a Wenzel (www.wenzel.com) crystal oscillator. These sources have proven to provide exceptional performance (low phase noise, flat frequency response, and reasonable harmonic performance) for frequencies of a few kilohertz to those of a few gigahertz. Harmonic performance of these generators is typically not as good as the intrinsic linearity of a given ADC, mandating the need for additional filtering between the signal generator and the analog input to the ADC.

ANALOG SIGNAL FILTER

Both fixed frequency and tunable frequency band-pass filters are utilized for device testing. The fixed frequency filters are typically smaller than tunable filters and often provide slightly better performance. Tunable filters allow testing across a wide range of frequencies using one filter. Several filter manufacturers, including K&L Microwave (www.klmicrowave.com), TTE (www.tte.com), and Allen Avionics, Inc., (www.allenavionics.com), provide excellent filters for ADC testing.

There are two types of filters that are often used for ADC testing: low-pass filters and band-pass filters. These can be used individually or combined to yield the level of performance required for an application.

Low-pass filters are a good choice when a wide range of analog frequencies must be applied to the ADC. However, they allow noise to pass from the signal generator to the ADC. This noise may reduce the level of performance measured for the ADC. A typical low-pass filter is the J97 available from TTE. Usually, low-pass filters have a transition band that defines where the pass band ends and the stop band begins. Along with this specification, a guaranteed stop-band rejection is specified. In the case of the J97, the transition band is defined to be between 1.0 and 1.2 times the 3 dB frequency, and the guaranteed stop-band rejection is 80 dB. Energy beyond 1.2 times the 3 dB frequency is reduced by a minimum of 80 dB.

Band-pass filters are used when analog frequencies are fixed and will not be changed. Band-pass filters also eliminate much of the wideband noise generated by signal sources and typically provide the best performance for ADC testing. Filters such as TTE's Q56 series have a bandwidth defined as a percentage of the center frequency. The more narrow the bandwidth, the less noise that passes through the filter; however, the analog frequency is more restricted, and there is a greater insertion loss. Once a center frequency is chosen, the bandwidth can be determined. Ideally, a bandwidth of 5% to 6% should be selected, keeping in mind that good noise performance is being traded for analog frequency flexibility. As with low-pass filters, the band-pass filter has a transition band that defines the shape between the 3 dB frequency (above and below the center frequency) and the frequency of the guaranteed stop-band performance. In the case of TTE's Q56, the stop-band rejection is 60 dB.

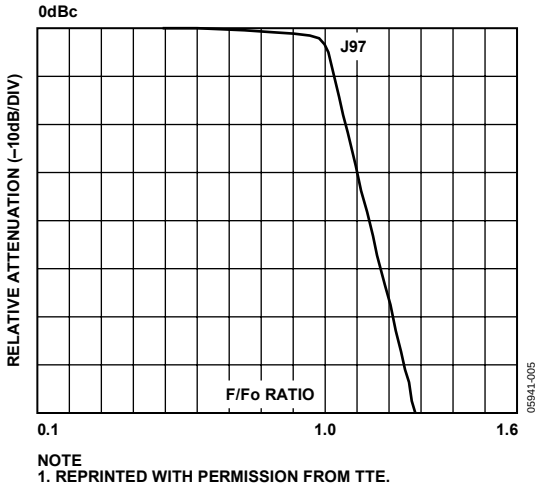


Figure 5. Typical Performance of TTE's J97

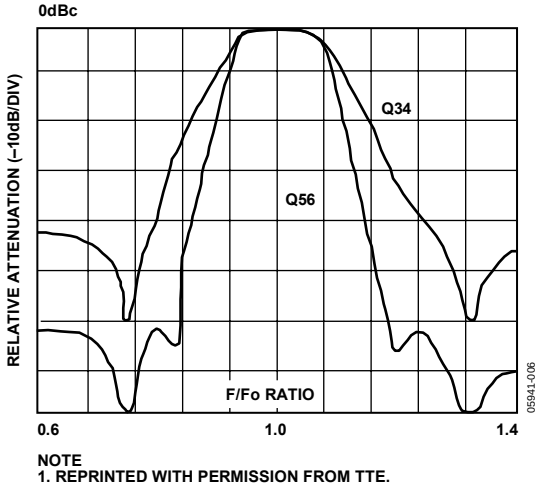


Figure 6. Typical Band-Pass Performance of TTE's Q34 and Q56

As noted previously, band-pass filters may only have a stop-band rejection of 60 dB, meaning that signals that fall into the stop band will be rejected by 60 dB. If, for example, a signal source has a harmonic that is 25 dB below the fundamental, the effective level of the harmonic is −85 dBc after a Q56 filter. For many high performance ADCs, this is not sufficient. When performance of −100 dBc or better is required, it is common to cascade a band-pass filter with a low-pass filter. When selecting a low-pass filter to follow a band-pass filter, the low-pass frequency should be selected such that stop-band performance of the low-pass filter optimally filters any harmonics that pass through the band-pass filter. With a J97 low-pass filter, stop-band rejection is reached at 1.2 times the 3 dB frequency. If the second harmonic of the band-pass filter is set equal to 1.4 times the low-pass 3 dB frequency, it ensures that all harmonics passing through the band-pass filter are filtered and that the additional insertion loss of the low-pass filter does not significantly reduce the level of the desired pass band. In this case, the low-pass frequency should equal 1.4 times the band-pass frequency and theoretically the

cascaded rejection should be about 140 dB. Although this is difficult to achieve in practice due to coupling and radiation effects, this technique is a useful one and can achieve well beyond −100 dBc harmonic rejection. It is also worth noting that a 0.5 dB to 3 dB pad can be placed between the band-pass and low-pass series combination. This helps to provide a better match between the two filters, which are nominally specified at 50 Ω.

When specifying filters, request those made with large cores to prevent saturation. Filters are typically designed for an input power of about 5 dBm. In many cases, however, ADC drive requirements are much larger than this, causing core saturation and distortion. Specifying larger cores reduces the spurious distortion caused by core saturation. Finally, it is worth mentioning that filter connectors can also be specified. Although adapters are easily found to convert between connector types, using them introduces mismatches that can subtly affect converter performance. While this might not be a problem with 8-bit and 10-bit converters, it is quite noticeable with 12-, 14-, and 16-bit converters.

ENCODE SIGNAL SOURCES

For high performance converters, stock signal generators usually are insufficient as encode sources because of both close-in and wideband phase noise. Fixed-frequency oscillators are typically used for encode sources. High performance crystal oscillators manufactured by Wenzel (www.wenzel.com) and Techtrol Cyclonetics, Inc., (TCI) (www.tci-ant.com) can be used. Wenzel's Sprinter and Ultra Low Noise series can offer optimum phase noise performance. Another source of high quality encode sources is Valpey Fisher (www.valpeyfisher.com), which offers several options, including differential PECLs and VCXOs. For less demanding applications, standard CMOS clock modules can be used and are available from various manufacturers. For end applications that require the clock to be synchronized with an external reference, a voltage-controlled crystal oscillator (VCXO) in a PLL loop can be employed.

Figure 7. Typical Low Cost CMOS Clock Oscillator

It is very important that an appropriate clock oscillator be used in each ADC design. Selection of the proper clock is aided by Analog Devices AN-501 Application Note and AN-756 Application Note. These application notes explain how to measure aperture jitter and how to specify a clock that meets the required phase noise or jitter specification. Failure to properly specify a clock source will degrade SNR performance, as shown in Figure 8 and Figure 9. As a reference, a typical Wenzel clock oscillator has about 0.07 ps of aperture jitter, whereas the CMOS clock oscillators have about 0.3 ps or more of aperture jitter.

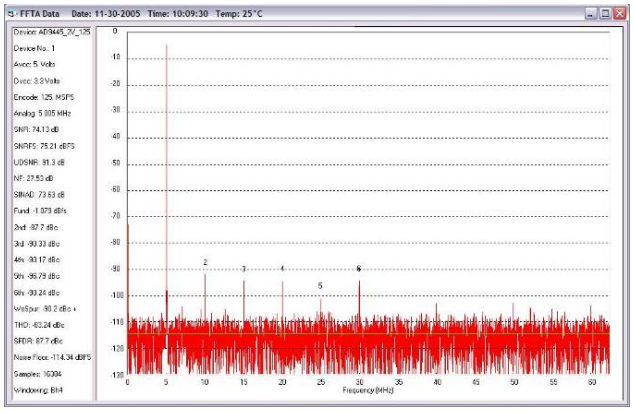


Figure 8. AD9445 with Analog IF of 130 MHz @ −1.0 dBFS using a Wenzel Clock, SNR = 75.2 dBFS

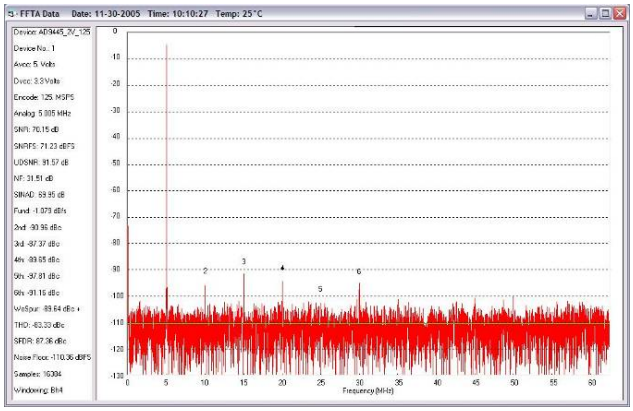


Figure 9. AD9445 with Analog IF of 130 MHz @ −1.0 dBFS using a CMOS Clock, SNR = 71.2 dBFS

When clock sources are not available with the desired jitter performance, it is possible to divide a higher frequency clock into lower rates. This has the effect of reducing the jitter at the rate of 10 log(x), where x is the division ratio. The limitation of this, however, is the jitter of the gates themselves. The AN-501 Application Note provides an indication of the clock jitter associated with various logic families.

When custom clocking is desired, a PLL is often required. A PLL allows the ADC to be synchronized to an external clock reference using a VCO or VCXO. However, it is difficult to clock more than one device using a simple PLL, but adding delays between the devices can facilitate such clocking. Devices such as the AD9510 are ideal for clock cleanup and distribution.

The additive jitter of the AD9510 is about 0.22 ps, and the device is optimized for driving ADCs, DACs, and various logic devices.

POWER SUPPLIES

Power supplies for ADCs are very important. Therefore, it is important to provide clean, quiet power supplies because most ADCs have poor power supply rejection ratios. While switching regulators are fine for many applications, linear regulators often provide a quieter, higher performance solution. Devices such as the ADP3338 and ADP3339 provide very low noise and well-regulated sources, and they are very suitable for most ADC applications. Additionally, they are available in a variety of voltages and can source up to 1 A to 1.5 A, respectively.

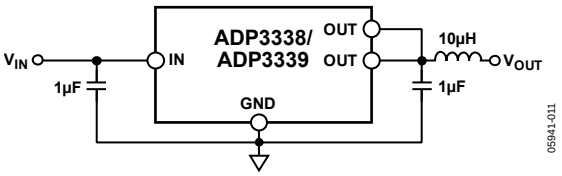


Figure 10. ADP3338/ADP3339 Typical Application

DATA ACQUISITION

Data acquisition and processing is accomplished with high speed caching memory. Data is collected at full ADC speed or can be decimated depending on the testing method used. Bench testing uses the ADI FIFO kit data capture board (no decimation required) in conjunction with the ADC Analyzer software (See the ADC FIFO Kit section for more details). Typically 16k, 32k, and 64k FFTs are performed, but bench FFTs can be as large as 4M samples. When the analog input source is not synchronized with the clock (noncoherent sampling), a Hanning or Blackman-Harris windowing function is typically used. (For more information, see "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform," Fredric J. Harris, Proceedings on the IEEE. Vol. 66, No. 1, January 1978.)

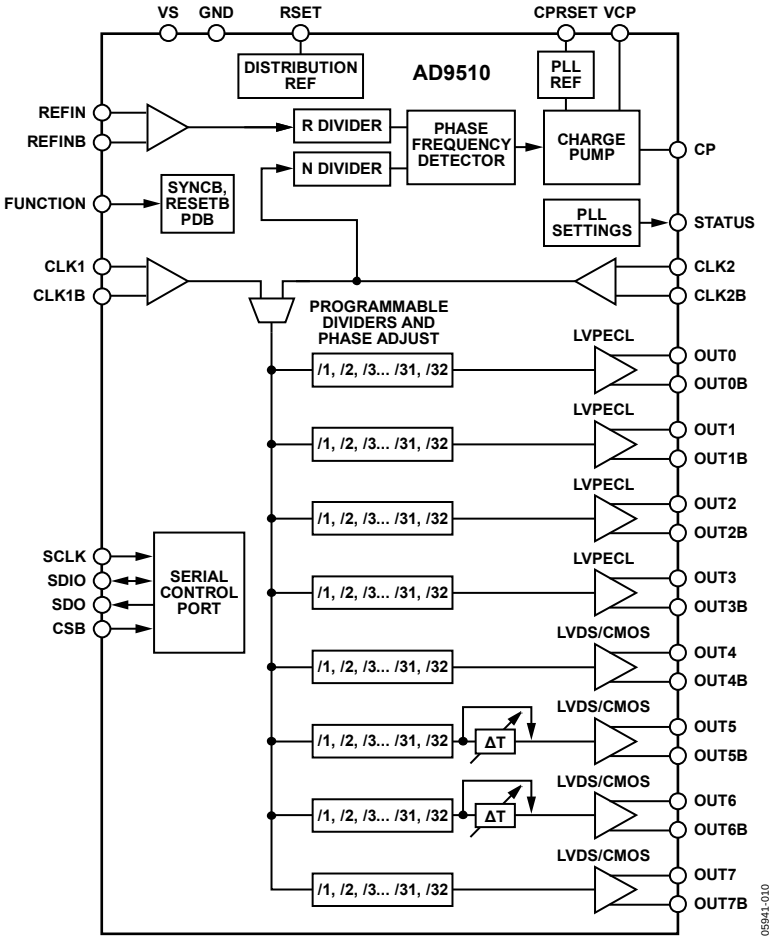


Figure 11. AD9510 Low Jitter Clock Source

AC TEST DEFINITIONS

AC or dynamic tests are typically made with the analog signal at the rated frequency with a signal power of 0.1 dB, 0.5 dB, or 1 dB below full scale (dBFS). If different amplitudes are used, they will be defined in the data sheet test conditions. For these tests, the encode rate is usually set at or near the maximum rated value. The data sheet should be consulted to determine the remainder of the test conditions, including power supply and temperature conditions.

FFT TESTING

Both coherent and noncoherent FFT testing can be used, depending on the actual test conditions. When coherent testing is used, the analog frequency is chosen such that the captured data samples exercise as many converter codes as possible in the record length. This is accomplished by using a prime relationship between the analog frequency and the encode rate.

For example, if coherent sampling is used and a 10 MHz analog input is desired with a specified sample rate of 65 MSPS, the calculated coherent analog input frequency is 10.0015258789063 MHz, or exactly 2521 cycles. This can be calculated using the following equation:

$$Cycles = \frac{f_{DESIRED\_FREQUENCY}}{\frac{Sample\_Rate}{FFT\_Samples}}$$

The number of cycles should be rounded to the nearest integer. When possible, the nearest prime number should be selected to ensure that the maximum number of quantization levels of the converter are exercised. Once the number of cycles has been selected, the previous equation can be solved using the desired analog input frequency.

FFT testing typically results in measurements expressed in decibels. Units can be expressed in dBc, which is the desired signal referenced to the carrier, or in dBFS, which is the desired signal referenced to the full scale of the converter. Either unit can be converted to the other by adding or subtracting the level of the carrier from full scale. (For more information about FFT testing, see "The FFT: Fundamentals and Concepts," Tektronix, Inc., 070-1754-00, Production Group 45, first printing December 1975.)

SINGLE-TONE FFT

Signal-to-Noise Ratio (SNR, dB)

The signal-to-noise ratio (SNR) is the ratio of the rms signal amplitude to the rms value of the sum of all spectral components except the first six harmonics and dc. As the input level is decreased, SNR typically decreases decibel-for-decibel in a linear fashion.

Signal-to-Noise Ratio Referenced to Full Scale (SNRFS, dBFS)

The signal-to-noise ratio referenced to full scale (SNRFS) is the ratio of the rms full scale to the rms value of the sum of all spectral components except the first six harmonics and dc. SNRFS is expressed in decibels referenced to full scale (dBFS). The difference between SNR and SNRFS is the difference between the fundamental amplitude and full scale.

Signal-to-Noise-and-Distortion (SINAD, dB)

The signal-to-noise and distortion (SINAD) is the ratio of the rms signal amplitude to the rms value of the sum of all spectral components, including harmonics but excluding dc. The difference between SNR and SINAD is the energy contained in the first six harmonics.

User-Defined Signal-to-Noise Ratio (UDSNR, dB)

User-defined signal-to-noise ratio (UDSNR) is a term used in ADC Analyzer software (see the *ADC Analyzer User Manual*). It is the ratio of the rms signal amplitude to the rms sum of all spectral components except the first six harmonics and dc within the specified band set by the user. The ADC Analyzer software allows the noise bandwidth to the left and right of the desired signal to be set independently. UDSNR is reported in decibels.

Noise Figure (NF, dB)

The noise figure (NF) is the ratio of the noise power at the output of a device to the noise power at the input to the device, where the input noise temperature is equal to the reference temperature (298 K). The noise figure is expressed in decibels.

The noise figure of an ADC can be computed for a single configuration. Assuming that the input range, termination, and sample rate are fixed, the NF for an ADC can be calculated using the following equation:

$$Noise\ Figure = 10\times\log\left(\frac{V^2_{rms}/Z_{IN}}{0.001}\right) - SNRFS - 10\times\log\left(\frac{Encode\ Frequency}{2}\right) - 10\times\log\left(\frac{k\times T\times B}{0.001}\right)$$

where:
K = Boltzman's constant = 1.38×10^{-23}
T = temperature in Kelvin = 273 K
B = bandwidth = 1 Hz
Encode Frequency = ADC clock rate
V rms = rms full-scale input voltage
Z_{IN} = input impedance
SNRFS = full-scale ADC SNR

Noise Floor (dBFS)

Noise floor is a term used in ADC Analyzer software (see the *ADC Analyzer User Manual*). Noise floor is equivalent to

$$Noise\ Floor = SNRFS - 10\log\left(\frac{FFT\ Bins}{2}\right)$$

This is an indication of the average noise in each FFT bin. If the size of the FFT is doubled, this number decreases by 3 dB. Noise floor does not provide an absolute measurement, but instead gives a relative indication of where the noise is for a given setup.

Effective Number of Bits (ENOB, Bits)

The effective number of bits (ENOB) provide a measure of an ADC's performance that is expressed in bits. ENOB is most accurately measured using a sine wave, curve-fit method (see *Calculate an ADC's Effective Bits*). The most common method for computing ENOB is to use the following equation based on the SINAD at the full scale of the converter:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Spurious-Free Dynamic Range (SFDR, dBc)

The spurious-free dynamic range (SFDR) is the ratio of the rms value of the signal to the rms value of the peak spurious spectral component for the analog input that produces the worst result. In most cases, SFDR is a harmonic of the input signal applied to the ADC.

Harmonic Distortion (dBc or dBFS)

A harmonic is a spectral component that is an integer multiple of the driven analog input frequency. For example, the frequency of the second harmonic is twice the analog input.

Most ADCs have specifications for one or more harmonics. Typically, the second and third harmonics are singled out because they have the worst performance of all the harmonics.

Harmonic distortion, no matter the order, is the ratio of the rms signal amplitude to the rms value of the specified harmonic component, reported in dBc or dBFS.

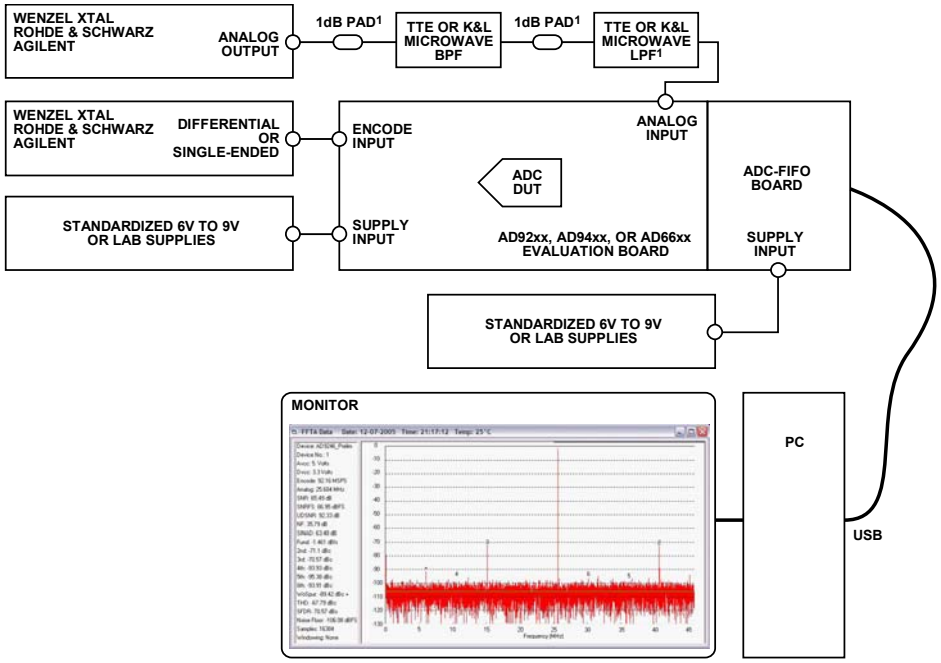
Because ADCs are nonlinear devices, the output is rich in spectral components. The worst spurious energy may not be directly related to the first two harmonics (2HD and 3HD) and is measured by the worst other spurious (WoSpur). WoSpur is the ratio of the rms signal amplitude to the rms value of the worst spurious component excluding the first six harmonically related components; it is reported in dBc.

Total Harmonic Distortion (THD, dBc)

Total harmonic distortion (THD) is the ratio of the rms signal energy to the rms value of the sum of the first six harmonics.

Harmonic Image (dBc)

The harmonic image measurement result is valid only when analyzing interleaved ADCs. This specification does not apply to most ADCs. Harmonic image is the ratio of the rms signal amplitude to the rms value of the nonharmonic component generated from the clocking phase difference of two ADCs, reported in dBc.



[1] OPTIONAL TO IMPROVE PERFORMANCE.

NOTES
1. AIN LEVELS SHOULD BE ADJUSTED FOR THE FREQUENCY AND LEVEL SPECIFIED.
2. ENCODE SETTING SHOULD BE ADJUSTED TO THE SPECIFIED RATE.
3. UNLESS ONBOARD REGULATORS ARE USED, SUPPLIES SHOULD BE AT NOMINAL.
4. TEMPERATURE SHOULD BE AT AMBIENT, UNLESS OTHERWISE NOTED.
5. USE THE APPROPRIATE CONFIGURATION FILE FOR ADC ANALYZER.

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Figure 12. Single-Tone Test Setup

TWO-TONE FFT

When multiple tones are passed through a converter with nonlinearities, intermodulation distortion products (IMD) result. Two-tone testing in an ADC is a means of specifying these nonlinearities. Because many of the distortion products may be relatively high in the analog spectrum, it is possible that the frequencies have aliased. This should be kept in mind when identifying distortion products.

F1 + F2 (dBc)

This term represents the second-order distortion product that appears at the frequency and is the sum of the two input frequencies. The measure of this term is the ratio of its rms value to the rms value of one of the two input tones expressed in dBc.

F2 – F1 (dBc)

This term represents the second-order distortion product that appears at the frequency and is the difference of the two input frequencies. The measure of this term is the ratio of its rms value to the rms value of one of the two input tones expressed in dBc.

Second-Order Input Intercept Point (IIP2, dBm)

The second-order input intercept point (IIP2) is the measure of the full-scale input signal power of the converter minus the IMD second-order products. It is reported in dBm.

2F1 ± F2 and 2F2 ± F1 (dBc)

These terms represent the third-order distortion products of the converter. The measure of each term is the ratio of its rms value to the rms value of one of the two input tones expressed in dBc. The peak spurious component is considered an IMD product.

Third-Order Input Intercept Point (IIP3, dBm)

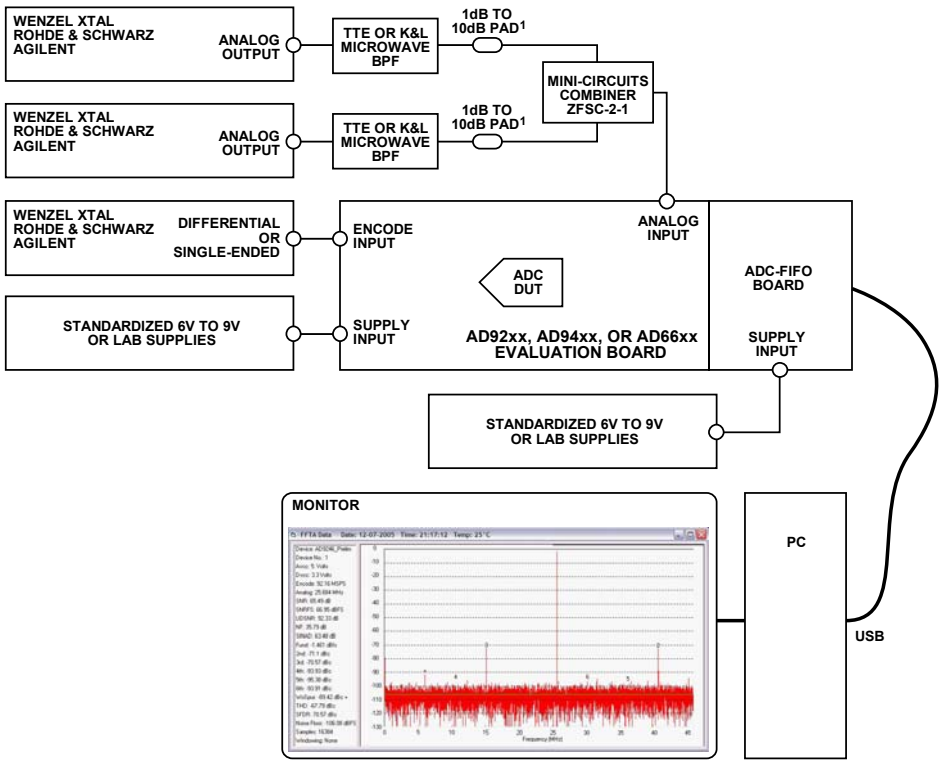
The third-order input intercept point (IIP3) is the measure of the full-scale input signal power of the converter minus half the IMD third-order products. It is reported in dBm.

Worst Other Spur (WoSpur, dBc)

The worst other spur (WoSpur) is the worst resulting spurious not related to the second- or third-order distortion products resulting from mixing two analog input signals. The measure of this term is the ratio of its rms value to the rms value of one of the two input tones expressed in dBc.

Two-Tone SFDR (dBc)

The spurious-free dynamic range (SFDR) is the ratio of the rms value of the signal to the rms value of the peak spurious spectral component for the analog input that produces the worst result. In most cases, SFDR is a harmonic of the input signal applied to the ADC.



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5. USE THE APPROPRIATE CONFIGURATION FILE FOR ADC ANALYZER.

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Figure 13. Two-Tone Test Setup

NOISE POWER RATIO (NPR, dB)

The noise power ratio (NPR) is a dynamic test that is used to assess the converters performance with a fully loaded Gaussian noise source. The noise level is adjusted such that the converter is loaded just below the point of clipping with a Nyquist-limited noise source. Then a narrow band of noise is removed with a deep notch filter. The noise within the notch is measured using FFT techniques to determine the ratio of noise density in the notch to the noise density without the notch. The results are expressed in decibels. NPR is optimized just prior to clipping, as shown in Figure 14. Once clipping begins, NPR falls off rapidly as the input signal is increased. If the input signal is reduced, NPR falls off approximately 1 dB for each decibel reduction in noise power.

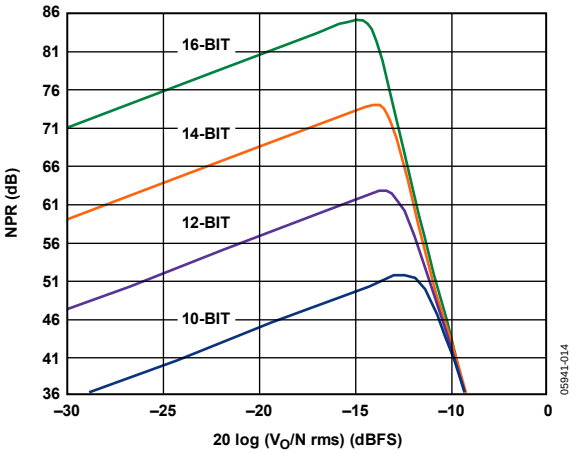


Figure 14. Typical NPR Curves

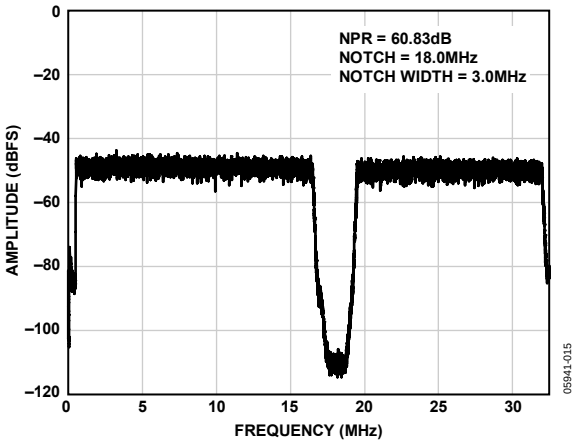


Figure 15. Typical NPR Response for a 12-Bit Converter

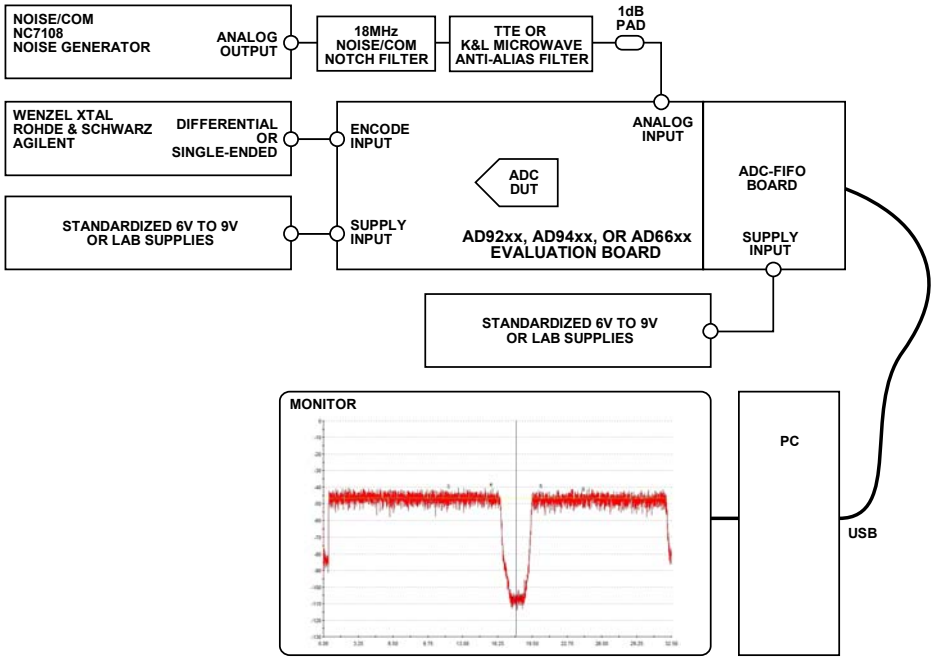


Figure 16. NPR Test Setup

FULL POWER BANDWIDTH (MHz)

Analog input bandwidth is the analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB. A particular value of SFDR or SNR performance is not implied by this test.

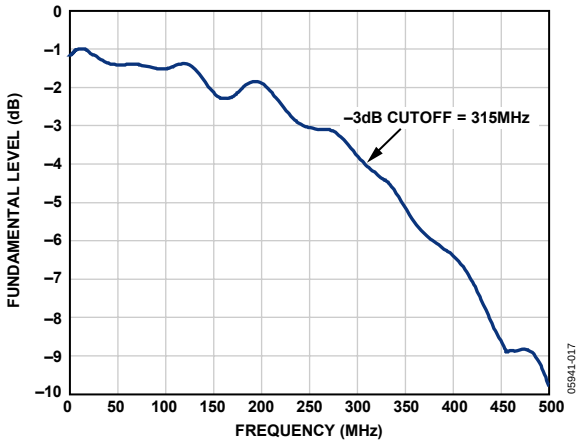
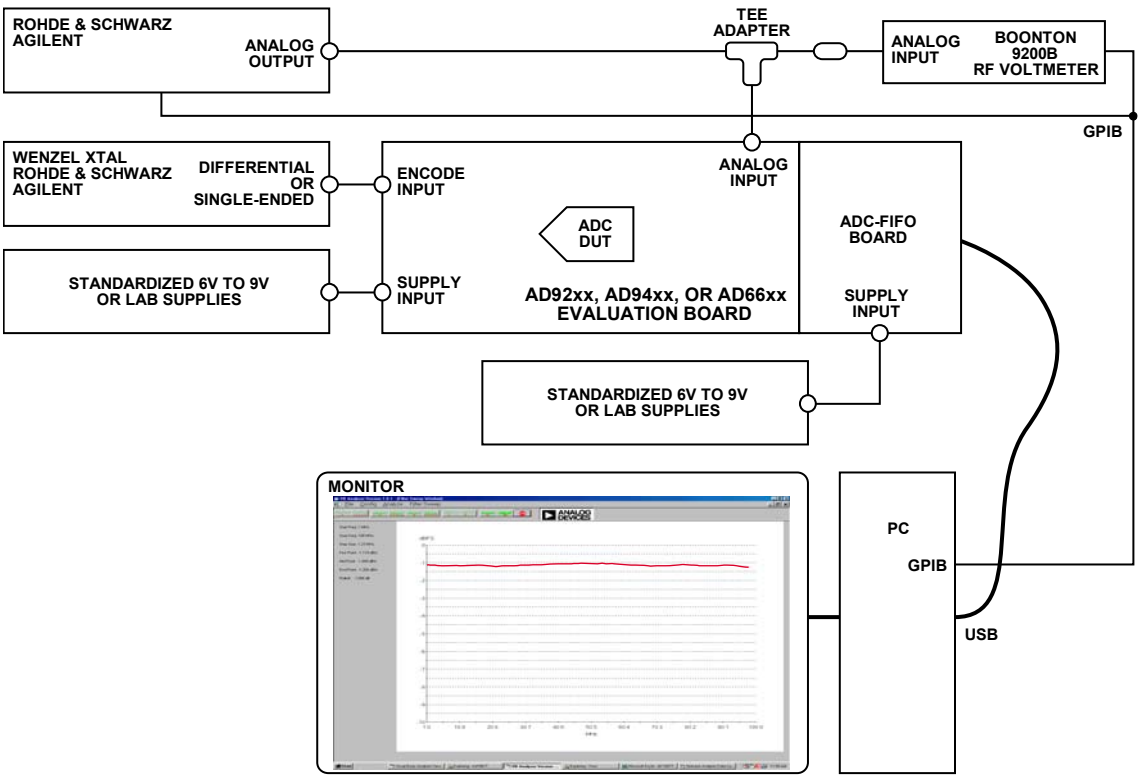


Figure 17. Typical Full Power Bandwidth Response



NOTES
1. AIN LEVELS SHOULD BE ADJUSTED FOR –1dB AT A 10MHz REFERENCE FREQUENCY.
2. ENCODE SETTING SHOULD BE ADJUSTED TO THE SPECIFIED RATE.
3. UNLESS ONBOARD REGULATORS ARE USED, SUPPLIES SHOULD BE AT NOMINAL.
4. TEMPERATURE SHOULD BE AT AMBIENT, UNLESS OTHERWISE NOTED.
5. USE THE APPROPRIATE CONFIGURATION FILE FOR ADC ANALYZER.
6. BOONTON PROBES SHOULD USE UNTERMINATED ADAPTERS.

05941-018

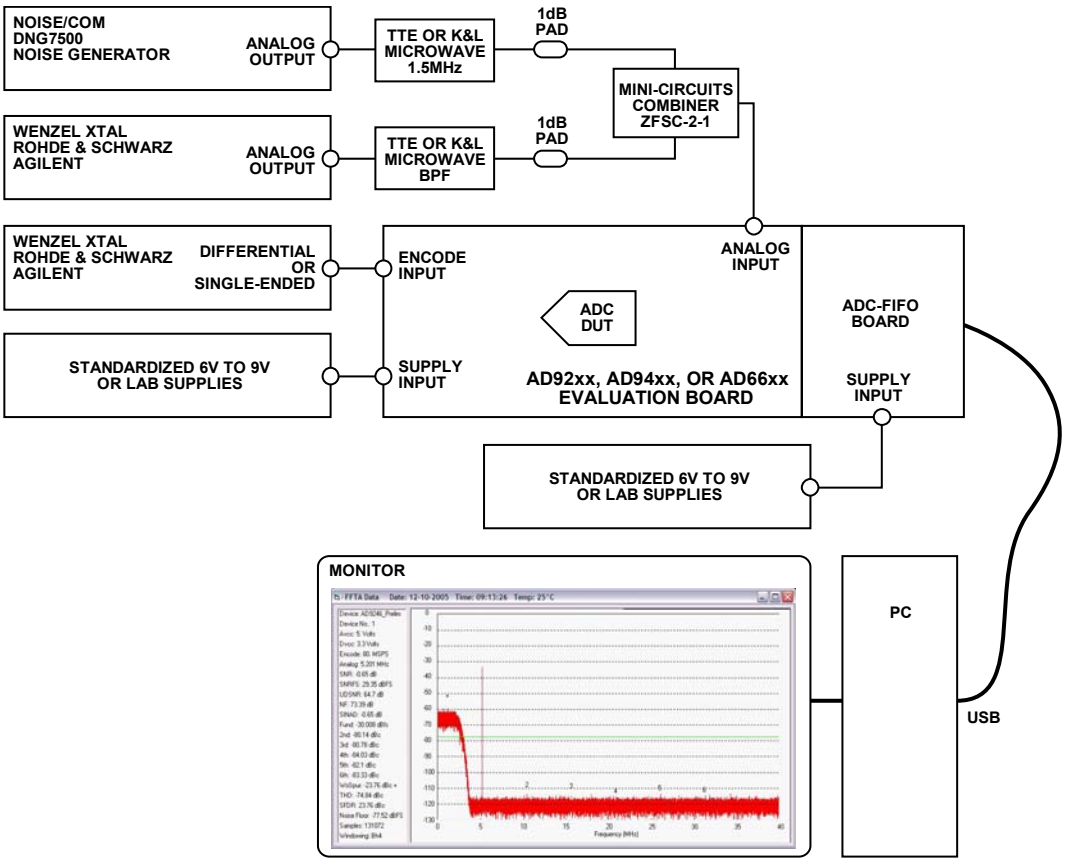
Figure 18. Full Power Bandwidth Test Setup

DITHER TESTING

Applying extra noise to an ADC's analog input causes dithering of the transfer function, reducing the spurious caused by static nonlinearities. While dither does little to reduce distortion caused by slew rate limitations, it is very efficient at reducing localized errors that hinder ADC performance.

There are two types of dither: out-of-band and wideband. As shown in the setup in Figure 19, out-of-band dither is band-limited noise placed out of band, where it will not spectrally disrupt converter performance. This technique is commonly used in communication systems, where digital filters are used to select desired signals and filter out all others. Wideband dither is often used in high performance test equipment. In this configuration, wideband analog noise is added to the input and the digital equivalent is subtracted from the output. The net effect of either technique is that spurious performance of the converter is greatly enhanced. For more details, see the AN-410 Application Note.

It is common for spurious performance to improve by 15 dB or more when dither is used, depending on the application. Many data sheets include dithered performance plots for comparison. In addition, using the ADC Analyzer software with ADIsimADC allows dither to be added to the simulation, further demonstrating how dither will improve performance.



NOTES
1. AIN LEVELS SHOULD BE ADJUSTED FOR THE FREQUENCY AND LEVEL SPECIFIED.
2. ENCODE SETTING SHOULD BE ADJUSTED TO THE SPECIFIED RATE.
3. UNLESS ONBOARD REGULATORS ARE USED, SUPPLIES SHOULD BE AT NOMINAL.
4. TEMPERATURE SHOULD BE AT AMBIENT, UNLESS OTHERWISE NOTED.
5. USE THE APPROPRIATE CONFIGURATION FILE FOR ADC ANALYZER. ADJUST DC BINS TO EXCLUDE DITHER.
6. USE AN ADC-FIFO BOARD WITH AT LEAST 64k.
7. ADJUST NOISE/COM DITHER LEVEL FOR MAXIMUM SFDR PERFORMANCE.

05941-019

Figure 19. Dither Test Setup

ANALOG INPUT

Analog Input Impedance

Analog input impedance is the ratio of the complex input voltage divided by the complex input current for the analog input. Analog input impedance is typically measured with a network analyzer and displayed on a Smith chart.

In some instances, the complex input can be broken down into resistive, capacitive, or inductive terms and reported as such.

Voltage Standing Wave Ratio (VSWR)

VSWR is a measure of the amount of power that is reflected back from the input of the ADC. This is a measure of the efficiency of the transfer of energy to the input port of the ADC.

The amount of power reflected back from the device can be computed from the input impedance based on the following equation:

$$\rho = \frac{Z_{IN} - Z_0}{Z_{IN} + Z_0}$$

where:
ρ is the amount of power reflected back from the device.
Z_{IN} is the complex input impedance of the ADC.
Z_0 is the desired impedance of the network.

From the reflection coefficient, the VSWR can be calculated by using the following equation:

$$VSWR = \frac{1 + \rho}{1 - \rho}$$

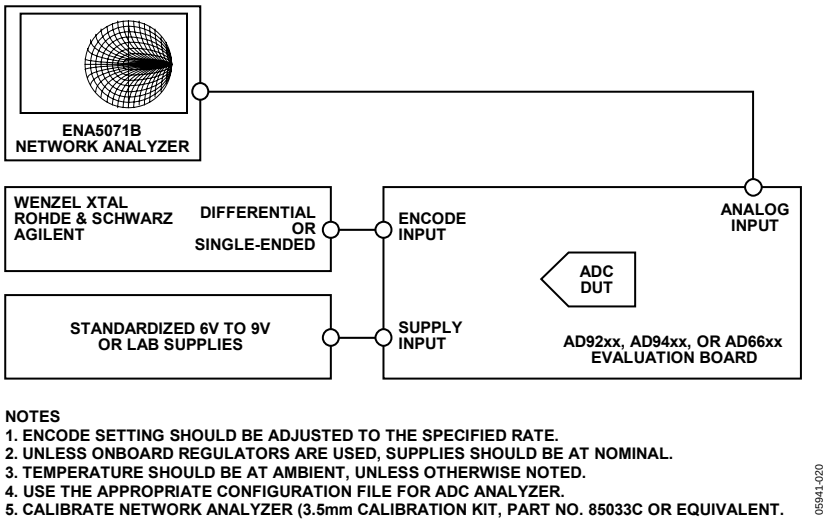
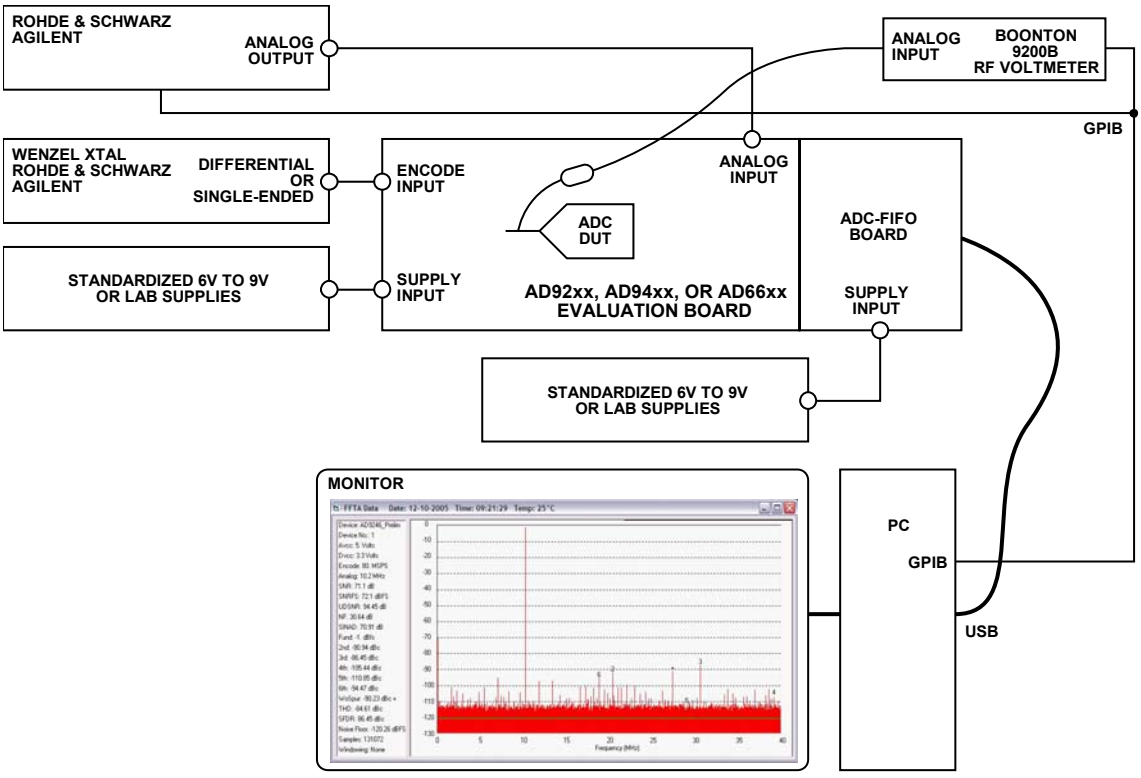


Figure 20. Analog Input Impedance and VSWR Test Setup

ANALOG INPUT FULL-SCALE RANGE (V p-p)

Analog input full-scale range is the range of peak-to-peak voltage (either single-ended or differential) that can be applied to the analog input(s) of the converter to generate a valid full-scale response.



NOTES
1. AIN LEVELS SHOULD BE ADJUSTED FOR –1dB AT 10MHz.
2. ENCODE SETTING SHOULD BE ADJUSTED TO THE SPECIFIED RATE.
3. UNLESS ONBOARD REGULATORS ARE USED, SUPPLIES SHOULD BE AT NOMINAL.
4. TEMPERATURE SHOULD BE AT AMBIENT, UNLESS OTHERWISE NOTED.
5. USE THE APPROPRIATE CONFIGURATION FILE FOR ADC ANALYZER.
6. BOONTON PROBES SHOULD USE UNTERMINATED ADAPTERS.

05941-021

Figure 21. Analog Input Full-Scale Range Test Setup

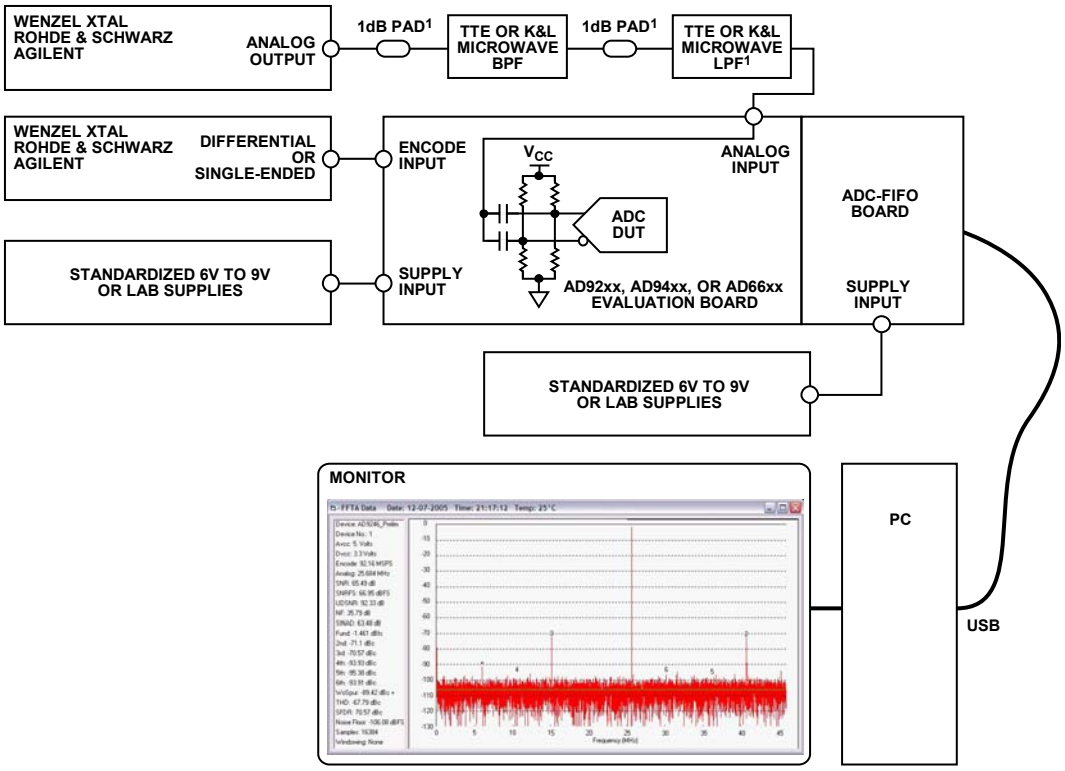
COMMON-MODE INPUT RANGE (V)

Common-mode input range is the range of dc offsets applied to both inputs of a differential input ADC for which the converter will operate normally. For many converters, the range is very limited, but some operate over a wide common-mode range. The converter's data sheet should be consulted to determine the specific common-mode range.

COMMON-MODE REJECTION RATIO (CMRR, dB)

The common-mode rejection ratio (CMRR) is defined as the amount of rejection on the differential analog inputs when a common signal is applied. Typically, CMRR is expressed in decibels and can be calculated as shown in the following equation:

$$CMRR = 20 \log \left(\frac{A_{DIFFERENTIAL}}{A_{COMMON\ MODE}} \right)$$



[1] OPTIONAL TO IMPROVE PERFORMANCE.

NOTES
1. AIN LEVELS SHOULD BE ADJUSTED FOR THE FREQUENCY AND LEVEL SPECIFIED.
2. ENCODE SETTING SHOULD BE ADJUSTED TO THE SPECIFIED RATE.
3. UNLESS ONBOARD REGULATORS ARE USED, SUPPLIES SHOULD BE AT NOMINAL.
4. TEMPERATURE SHOULD BE AT AMBIENT, UNLESS OTHERWISE NOTED.
5. USE THE APPROPRIATE CONFIGURATION FILE FOR ADC ANALYZER.
6. RESISTIVE DIVIDER MAY NOT BE NECESSARY FOR SOME ADCs.

05941-022

Figure 22. CMRR Test Setup

APERTURE DELAY (ps)

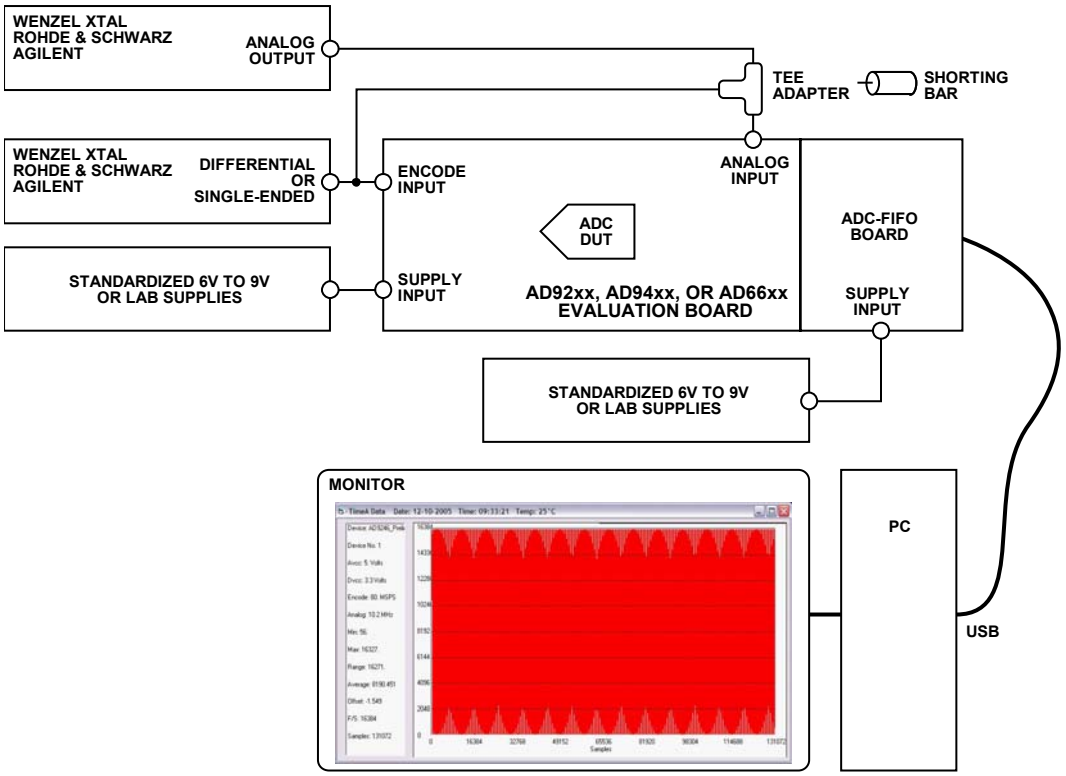
Aperture delay (AD) is a measure of the difference in the delay between the analog path and the encode path. It is measured by observing the time from the 50% point of the rising edge of the sample clock to the time at which the input signal is actually sampled.

AD can be measured by using the following test configuration:

1. Connect the analog input to an analog filtered source.
2. Using a program like ADC Analyzer, adjust the input until the single-tone FFT results in a full-scale signal (0 dBFS).
3. Disconnect the analog input, and use a shorting bar to short the analog input to ground.
4. Use a continuous average time domain plot to measure the offset of the part.
5. Remove the shorting bar from the analog input and reconnect the analog input as shown in Figure 23.
6. Record the new offset value and use it to solve the following equation:

$$t_{AD} = \sin^{-1}\left(\frac{\left(Code_{AVERAGE} - Offset\right)/(2^N/2)}{2\pi \times Frequency}\right)$$

where:
$2^N/2$ is the midscale of a 16-bit ADC.
Offset is the offset of the part measured using a continuous average time domain plot (see Step 4).
$Code_{AVERAGE}$ is the new offset value obtained after removing the shorting bar from the analog input and reconnecting the analog input (see Step 5).



NOTES
1. AIN LEVELS SHOULD BE ADJUSTED FOR 0dBFS OUTPUT FOR THE INPUT FREQUENCY OF MIDBAND.
2. ENCODE SETTING SHOULD BE ADJUSTED TO THE SPECIFIED RATE.
3. UNLESS ONBOARD REGULATORS ARE USED, SUPPLIES SHOULD BE AT NOMINAL.
4. TEMPERATURE SHOULD BE AT AMBIENT, UNLESS OTHERWISE NOTED.
5. USE THE APPROPRIATE CONFIGURATION FILE FOR ADC ANALYZER.

05941-023

Figure 23. Aperture Delay Test Setup

APERTURE JITTER OR APERTURE UNCERTAINTY (ps RMS)

Aperture jitter is the sample-to-sample variation in aperture delay that can be manifested as frequency-dependent noise on the ADC input. Details on measuring aperture jitter can be found in the AN-501 Application Note, and details on converting aperture jitter to phase noise can be found in the AN-756 Application Note.

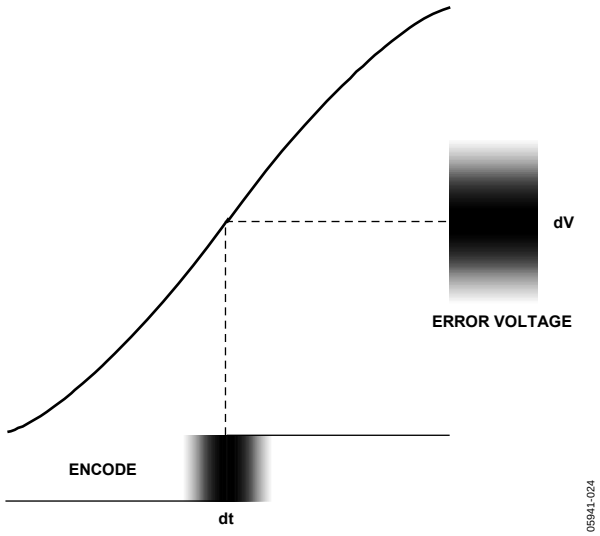


Figure 24. Aperture Uncertainty

CROSSTALK (dB)

Crosstalk is defined as the measure of any feedthrough coupling onto the quiet channel of a multichannel ADC. Crosstalk is measured in three ways under two conditions.

Condition One

If a signal is driven near full scale, crosstalk can be measured by one of the following methods:

- Drive any two channels using a different midbaseband frequency for each that are at least 2 MHz apart at −0.5 dBFS. Record the same fundamental frequency on any open channel (nondriven). Repeat for all channel combinations.
- Drive any N − 1 channel using a single midbaseband frequency at −0.5 dBFS. Record the same fundamental frequency on any open channel (nondriven). Repeat for all channel combinations.

Condition Two

If a signal is driven 3 dB over full scale, known as the overdriven condition, crosstalk can be measured as follows:

- Use either method described in the Condition One section, but with a midbaseband frequency amplitude set to 3 dB above full scale.

All results are expressed in decibels as a ratio of the energy of the undesired signal on the quite channel to the energy on the driven channel.

INPUT-REFERRED NOISE (LSB RMS)

Input-referred noise is a measure of the wideband noise generated by the ADC. A histogram of the output codes is created while the input is grounded. Input-referred noise is calculated using the standard deviation of the histograms, and it is presented in terms of LSB rms.

This measurement can also be correlated using SNRFS measurements and converting decibels to volts using the following equation:

$$Noise_{INPUT} = \frac{V\ p\text{-}p}{2 \times \sqrt{2} \times 10^{SNR/20}}$$

where *V p-p* is the ADC full-scale input range, and *SNR* is the full-scale SNR performance when driven by a small input signal.

OUT-OF-RANGE RECOVERY TIME (CLK CYCLES)

Out-of-range recovery time is the time required for the ADC to recover to the rated accuracy after an input transient moves from 10% above positive full scale to 10% above negative full scale or from 10% below negative full scale to 10% below positive full scale.

DIGITAL TIME DOMAIN

Minimum Conversion Rate (MSPS)

The minimum conversion rate is the clock rate at which the SNR of the lowest specified analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate (MSPS)

The maximum conversion rate is the clock rate at which parametric testing is performed. Higher operating rates are possible, but they are not guaranteed.

Pipeline Delay (CLK Cycles)

Pipeline delay is the delay through the converter as a function of the encode cycles. To maximize throughput, many high speed converters leverage pipeline processing. As a result, the corresponding data is not output until several clock cycles after the signal is sampled. This delay is the pipeline delay and can be expressed as whole or fractional clock cycles, depending on the data converter.

Propagation Delay (ns)

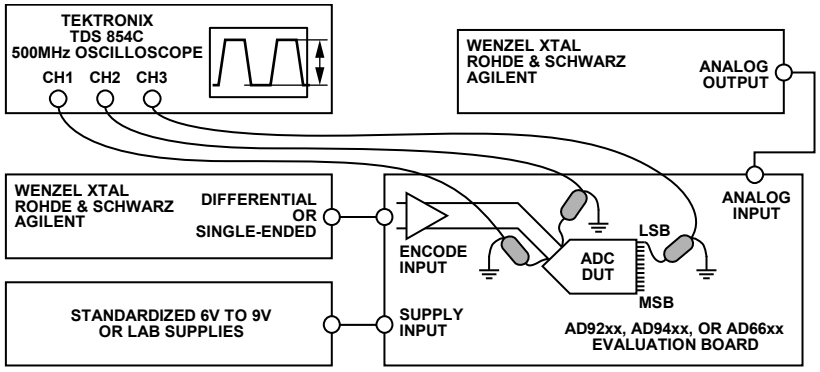
Propagation delay is the delay between the clock logic threshold (or 50% point for a differential clock input) and the time when all bits are within valid logic levels.

Encode Pulse Width or Encode Duty Cycle

Encode pulse width high is the minimum amount of time that the encode signal can be in a logic high state and achieve the specified performance. Encode pulse width low is the minimum amount of time that the encode signal can be in a logic low state and achieve the specified performance. In a traditional ADC, when the encode signal is in a logic high state, the circuit is in a sample mode. If held in a high state for an insufficient amount of time, the sample process will fail to complete. If held in a low state for an insufficient amount of time, the circuit will fail to accurately acquire the signal to be sampled. Optimal operation is achieved when the acquire and sample times are suitably balanced.

In many converters, the encode duty cycle is provided instead of pulse-width measurements. This is usually stated for the maximum rated encode and expressed as a range of the percentage of time that the encode line may be in the high state.

For this test, rated performance is defined as the range over which SNRFS performance is within −3 dB of nominal performance.



NOTES
1. AIN SHOULD BE SET TO A LOW FREQUENCY FULL-SCALE SIGNAL.
2. ENCODE SETTING SHOULD BE ADJUSTED TO THE SPECIFIED RATE.
3. UNLESS ONBOARD REGULATORS ARE USED, SUPPLIES SHOULD BE AT NOMINAL.
4. TEMPERATURE SHOULD BE AT AMBIENT, UNLESS OTHERWISE NOTED.
5. USE THE APPROPRIATE REVS ON EVALUATION BOARD AND PARTS AS NOTED.
6. ALL OSCILLOSCOPE PROBES SHOULD BE SOLDERED DOWN AND GROUNDED.
7. TEKTRONIX PROBES M/N: P6243 OR BETTER SHOULD BE USED. <1pF WITH 1GHz BW.

05941-025

Figure 25. Propagation Delay Test Setup

CONVERSION ERROR RATE (CER)

The conversion error rate (CER) is a measurement of the frequency of errors generated by the ADC. An error is defined as output codes that fall outside the bounds of converter noise in excess of that allowed by normally distributed noise. Converter noise is defined as the noise normally generated by quantization, thermal effects, and clock jitter and is generally considered Gaussian. A sample is considered to be an error if the frequency of occurrence exceeds that predicted by a normal distribution.

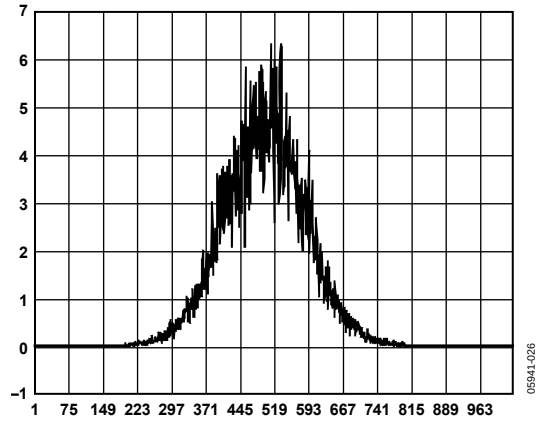


Figure 26. Gaussian-Distributed ADC Output

Noise magnitude is normalized to Sigma (σ) and can be determined by measuring the full-scale SNR and then solving the following equation using this value:

$$\sigma = \frac{2^N}{2 \times \sqrt{2} \times 10^{SNR/20}}$$

Once sigma has been determined based on the expected SNR (or from the data sheet), a method can be employed to capture data such that the expected ADC code is subtracted from the actual code, resulting in a distribution histogram. With a statistically large data set, it can be expected that for normal ADC noise, the resultant distribution will be similar to that shown in Figure 26. For a large distribution, excess samples in any of these ranges is an indication of bit errors, as shown in Table 1.

Table 1. Sigma vs. Normal Probability of Occurrence

σ	Normal Probability of Occurrence	Natural Occurrences Outside in 1 Million Samples
3.09	2×10^{-3}	2000
3.72	2×10^{-4}	200
4.26	2×10^{-5}	20
4.75	2×10^{-6}	2
5.20	2×10^{-7}	0.2
5.61	2×10^{-8}	0.02
6.0	2×10^{-9}	0.002
6.36	2×10^{-10}	0.0002

It should be noted that with a sample rate of 100 MSPS, one error outside the 6.36 sigma is normal in a 50-second window and does not constitute a conversation error. Only when the rate exceeds 2×10^{-10} is a conversation error indicated. In practice, external devices including latching and memory elements make it difficult to measure anything beyond about 2×10^{-6} or 2×10^{-7}.

DC TEST DEFINITIONS

GAIN ERROR (%FS)

Gain error is the difference between the measured full scale and ideal full scale. This is usually expressed as a percentage of full scale.

GAIN MATCHING (%FS)

Gain matching is the ratio of the maximum full scale to the minimum full scale of a multichannel ADC. It is expressed as a percentage of full scale using the following equation:

$$Gain\ Matching = \left(\frac{FSR_{MAX} - FSR_{MIN}}{\frac{FSR_{MAX} + FSR_{MIN}}{2}} \right) \times 100\%$$

where FSR_{MAX} is the most positive gain error of the ADC, and FSR_{MIN} is the most negative gain error.

OFFSET ERROR (%FS)

Offset error is the difference between the measured and ideal voltage at the analog input that produces the midscale code at the output. This is usually expressed as a percentage of full scale.

OFFSET MATCHING (mV)

Offset matching is the difference in offsets, expressed in millivolts between the channels of a multichannel converter. It is computed with the following equation:

$$Offset\ Matching = VOFFSET_{MAX} - VOFFSET_{MIN}$$

where $VOFFSET_{MAX}$ is the most positive offset error, and $VOFFSET_{MIN}$ is the most negative offset error.

Offset matching is usually expressed in millivolts with the full-scale input range stated in the product data sheet.

TEMPERATURE DRIFT (ppm)

The temperature drifts for offset error and gain error specify the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}. This is usually expressed in ppm.

VOLTAGE OUTPUT HIGH/VOLTAGE OUTPUT LOW (VOH/VOL, V)

Voltage output high (VOH) is the voltage representing the high logic level. Voltage output low (VOL) is the voltage representing the low logic level.

DC or static tests are typically made with dc or very low frequency test signals. The purpose of these tests is to determine the baseline values of many of the core converter specifications. Test conditions vary by product; therefore, the product's data sheet should be consulted to determine actual test conditions.

LINEARITY

There are two types of converter linearity: differential nonlinearity (DNL) and integral nonlinearity (INL). The basic measure of an ADC is the range of voltages for which each code is active. The integration of these voltages determines the overall transfer function of the converter. Together these two basic measurements determine the characteristic static performance of the ADC.

These tests are frequently performed using histogram techniques. A histogram is collected by driving the analog input of the ADC with a signal of known statistical qualities. For example, a dc ramp has the quality of a uniform probability density function. This means that when driving an ADC input, each ADC code has an equal probability of occurring over a large observation window. Other waveforms, such as sine waves, have known functions as well. Although such waveforms are not uniform, they can be accurately described mathematically (see *The Data Conversion Handbook*, Walt Kester, Newness, 2005, Page 315.).

Typical histogram tests are performed by taking as large a number of samples as is reasonable. For high resolution converters, this may be 4 million samples or more.

Differential Nonlinearity Error (DNL, LSB)

Differential nonlinearity (DNL) is the variation of any code from an ideal 1 LSB step. This is measured by examining each of the histogram bins and comparing the actual probability of occurrence to the ideal probability. This results in a direct measure of DNL for each code.

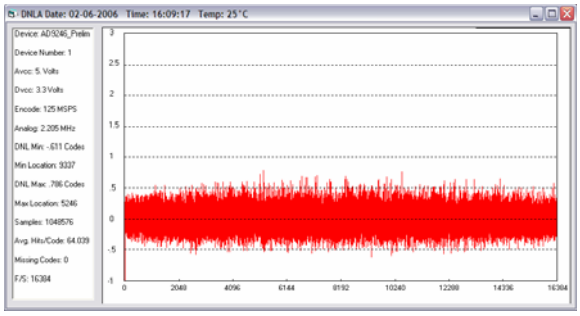


Figure 27. Typical 10-Bit DNL

Missing Code

A code is said to be missing if the DNL for that code is −1 LSB. A missing code is defined as a missing quantization level and can result from a variety of causes. Most products are designed or screened for no missing codes.

Integral Nonlinearity Error (INL, LSB)

Integral nonlinearity (INL) is the deviation of the transfer function from a reference line measured in fractions of 1 LSB using a best straight line determined by a least-mean-squared curve fit. This is measured by integrating the histogram to form a transfer function and then performing the linear regression on this function. The difference between the actual transfer function and this best fit line is the INL.

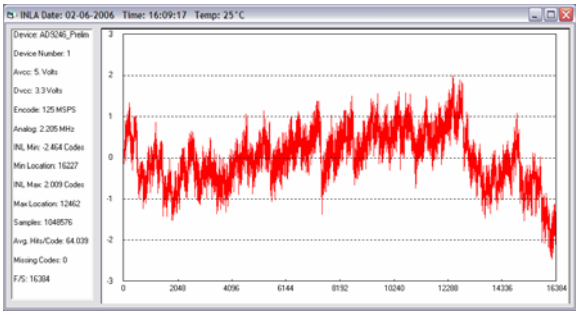
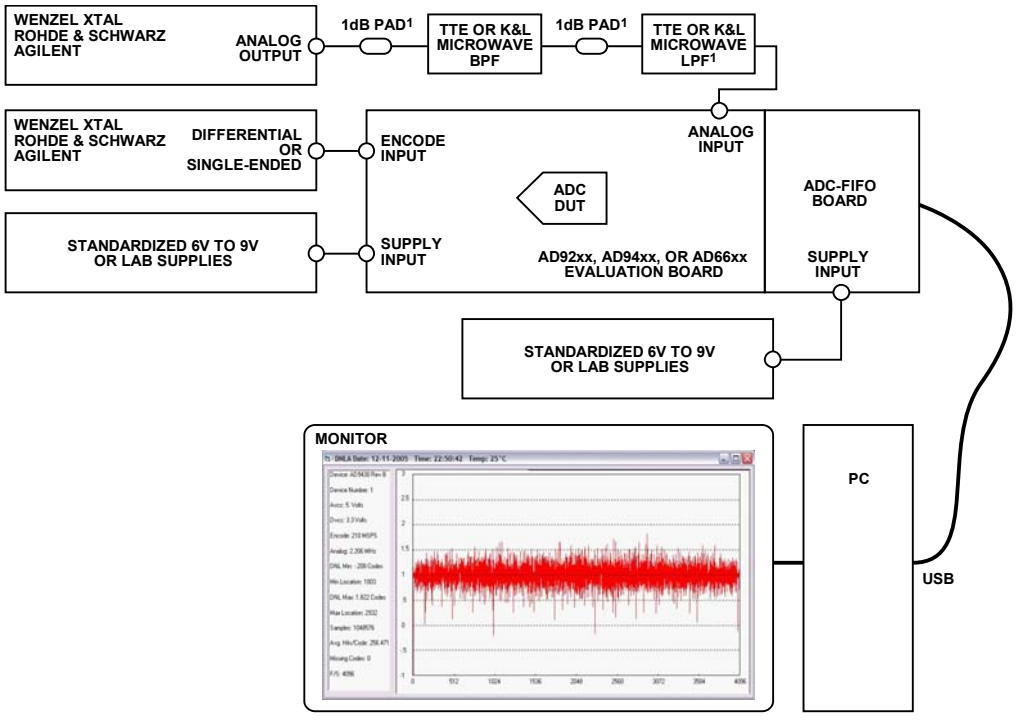


Figure 28. Typical 10-Bit INL



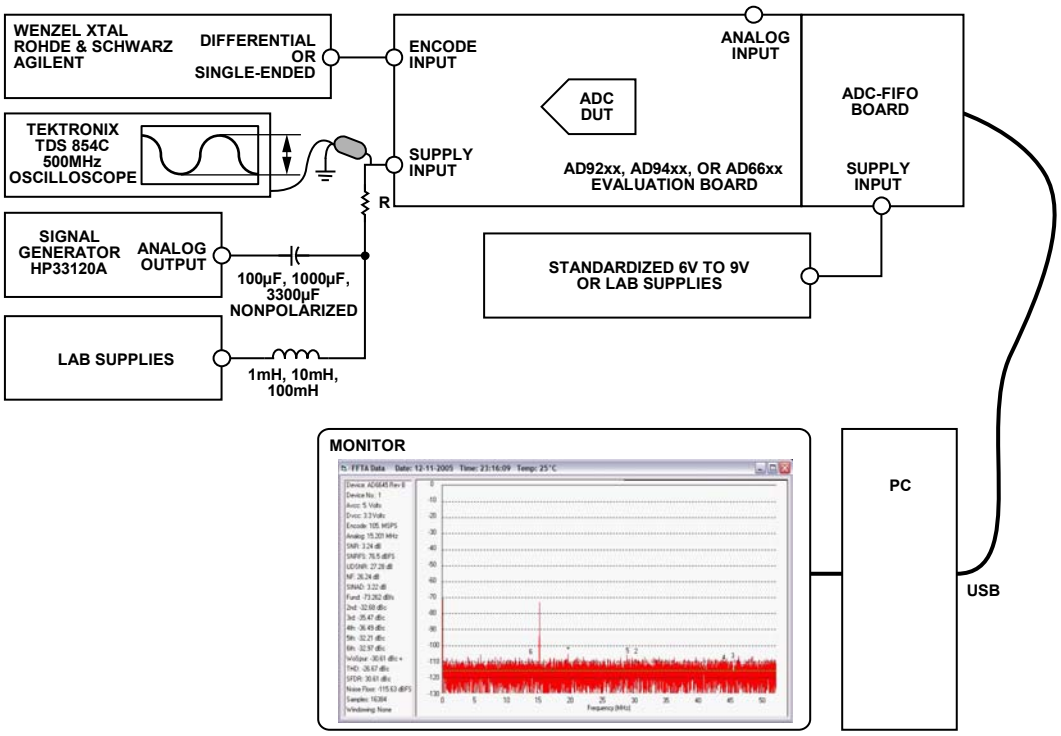
[1] OPTIONAL TO IMPROVE PERFORMANCE.

NOTES
1. AIN LEVELS SHOULD BE ADJUSTED FOR –0.01dBFS AND ABOUT 2.2MHz.
2. ENCODE SETTING SHOULD BE ADJUSTED TO THE SPECIFIED RATE.
3. UNLESS ONBOARD REGULATORS ARE USED, SUPPLIES SHOULD BE AT NOMINAL.
4. TEMPERATURE SHOULD BE AT AMBIENT, UNLESS OTHERWISE NOTED.
5. CUSTOMER SOFTWARE DOES NOT SUPPORT INL AND DNL TESTING.
6. USE APPROPRIATE REVS ON EVALUATION BOARD AND PARTS AS NOTED.

Figure 29. DNL and INL Test Setup

POWER SUPPLY REJECTION RATIO (PSRR, dB)

Power supply rejection ratio (PSRR) is a measurement of the amount of a signal on the power supply that is coupled to the digital output of the ADC. PSRR can be measured by changing the power supply and then measuring the change in offset of the converter, expressed as a percentage of full scale. More typically, PSRR is measured by injecting an ac signal of known amplitude on the power supply pins and then measuring the observed spectrum of an FFT. PSRR is the difference between the values measured by ADC in volts minus the input value measured by the oscilloscope, expressed in decibels.



NOTES
1. ALL BYPASS CAPACITORS AND FERRITE BEADS SHOULD BE REMOVED FROM THE EVALUATION BOARD.
2. ENCODE SETTING SHOULD BE ADJUSTED TO THE SPECIFIED RATE.
3. THE VALUE OF R IS RELATED TO THE SOURCE IMPEDANCE OF THE END POWER SUPPLIES.
4. THE SIGNAL MEASURED BY THE OSCILLOSCOPE IS COMPARED TO THE FFT OUTPUT TO DETERMINE THE PSRR.
5. TEKTRONIX PROBES M/N: P6243 OR BETTER SHOULD BE USED. <1pF WITH 1GHz BW.

Figure 30. PSRR Test Setup

REFERENCES

Additional information on data converter characterization can be found in *The Data Conversion Handbook* by Walt Kester, Newness, ISBN 0-7506-7841-0. Additional reference books, including the *High Speed Design Techniques*, the *Practical Analog Design Techniques*, the *Linear Design Seminar*, and the *System Applications Guide*, can be found on ADI's website. In addition to the many reference books, various applications notes, articles, and reprints are available from your Analog Devices sales representative, or you can visit our website at www.analog.com for additional information.

NOTES

AN05941-0-4/06(0)