# VR Hall Module Kit User's Manual
## D000015 Rev B
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## Contents

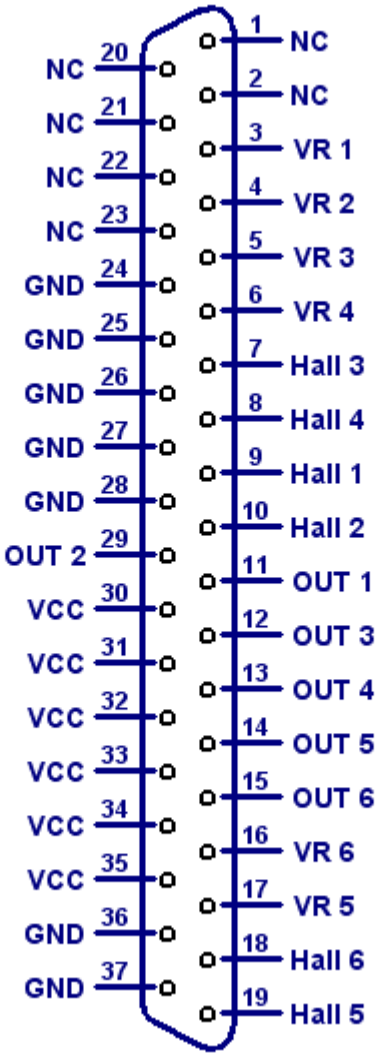
# Introduction

The Drivven VR/Hall Module Kit offers a set of automotive style inputs to interface with standard automotive position sensors. It provides six channels which may be software selected as a VR sensor or hall-effect sensor input.

**Features:**

- 6 Ch. total, individually software-configured as VR or hall-effect sensor inputs
  - VR sensor inputs
    - +/-150 V input range
    - Adaptive threshold
  - Hall-effect sensor or general purpose digital inputs
    - Digital input with hysteresis
    - Over/under voltage protection
    - Optional Pullup, Pulldown, and Divide resistors
    - RC filter for noise rejection
- External output for each channel according to software configuration
- Sensor power output
  - 5V @ 100mA
  - Protected with resettable fuse

## Pinout


1 NC
2 NC
3 VR 1
4 VR 2
5 VR 3
6 VR 4
7 Hall 3
8 Hall 4
9 Hall 1
10 Hall 2
11 OUT 1
12 OUT 3
13 OUT 4
14 OUT 5
15 OUT 6
16 VR 6
17 VR 5
18 Hall 6
19 Hall 5
20 NC
21 NC
22 NC
23 NC
24 GND
25 GND
26 GND
27 GND
28 GND
29 OUT 2
30 VCC
31 VCC
32 VCC
33 VCC
34 VCC
35 VCC
36 GND
37 GND

# Hardware

This module provides six input channels which may be individually software selected as VR sensor input or hall-effect sensor input. It also provides sensor power and ground. Sensor power is provided directly from the cRIO chassis backplane. All sensors should not draw more than a total of 100mA. VCC pins are protected with a 0.1A resettable fuse.

Each of the six channels provide an external digital output. The signal output is configured according to the software selection of VR or Hall.

A properly strain relieved DB-37 connector (not included) is used to interface to the module. National Instruments provides the "cRIO-9933 37-pin Conn. Kit, screw term conn. and DSUB shell" which is compatible with this module. However, any DB-37 connector system may be used. Drivven recommends the following DB-37 connector parts and tools available from several electronics parts distributors (Allied, Mouser, Digikey, etc.).

Table 1. Connector parts list

| Description | Mfr.'s Part # |
|---|---|
| AMP HDP-20 Series 109 37P Receptacle Housing | 1757820-4 |
| AMP HDP-20 Series 109 Crimp Socket Contact | 205090-1 |
| Norcomp D-Sub Connector Hood, 37P 45 Degree | 971-037-020R121 |
| AMP D-Sub Insert/Extract Tool | 91067-2 |
| Paladin D-Sub 4-Indent Crimp Tool 26-20 AWG | 1440 |

# Powering the Module

The VR/Hall module requires power from one source, from the CompactRIO backplane male high density D-Sub 15-pin (HD15) connector which mates with the module's female HD15 connector. This power source provides a regulated 5 volts and ground to various digital logic functions within the module. The CompactRIO 5V source is active whenever the CompactRIO or R-Series Expansion Chassis is properly powered. The module should only be powered at the HD15 connector by plugging it into a CompactRIO or R-Series Expansion Chassis. The module's HD15 connector should not be connected to any other device. **Do not** connect 5VDC power to the "VCC" outputs of the DB37 connector. Those pins are 5V outputs.

# Platform Compatibility

CompactRIO modules from Drivven are compatible within two different platforms from National Instruments. One platform is CompactRIO, consisting of a CompactRIO controller and CompactRIO chassis as shown in Figure 1a below.

Figure 1a. CompactRIO platform compatible with Drivven CompactRIO modules.

The other platform is National Instruments PXI which consists of any National Instruments PXI chassis along with a PXI RT controller and PXI-78xxR R-Series FPGA card. An R-Series expansion chassis must be connected to the PXI FPGA card via a SHC68-68-RDIO cable. The CompactRIO modules insert into the R-Series expansion chassis. This platform is shown in Figure 1b below.

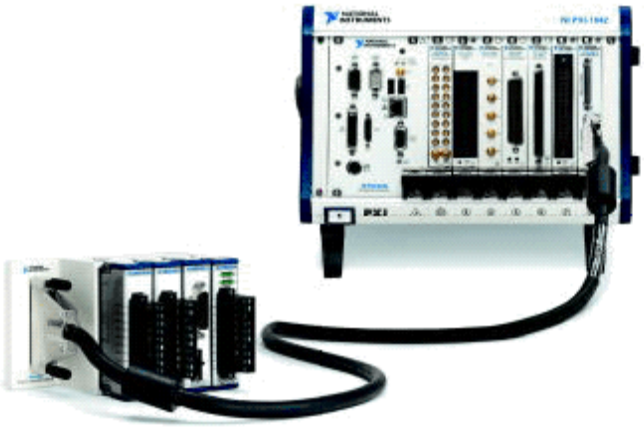


Figure 1b. PXI platform compatible with Drivven CompactRIO modules.

Drivven CompactRIO modules are not compatible with the National Instruments CompactDAQ chassis.

Drivven CompactRIO modules REQUIRE one of the hardware support systems described above in order to function. The modules may not be used by themselves and/or interfaced to third party devices at the backplane HD15 connector. These efforts will not be supported by Drivven or National Instruments.

## VR Sensor Inputs

The VR Hall module provides up to six identical VR sensor inputs. A Variable Reluctance (VR) sensor is a standard production automotive speed sensor. It is an electro-magnetic sensing device containing a winding of wire around a permanent magnetic core. It relies on the movement of ferrous material (steel teeth) past the tip of the sensor to change the magnetic flux of the sensor. This creates a voltage pulse across the leads of the sensor's wire coil. Figures 4 and 5 below show a typical VR signal with respect to toothed wheels, as shown in figures 2 and 3. The VR signal will go positive as a tooth approaches the sensor tip. The signal will then rapidly swing back through zero precisely at the center of the tooth. As the tooth moves away from the sensor tip the voltage will continue in the negative direction and then return to zero.

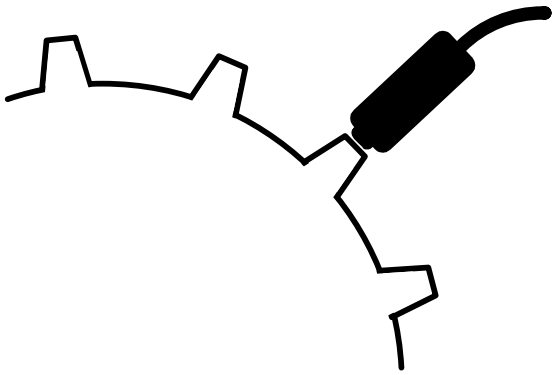


Figure 2. Positive tooth trigger wheel

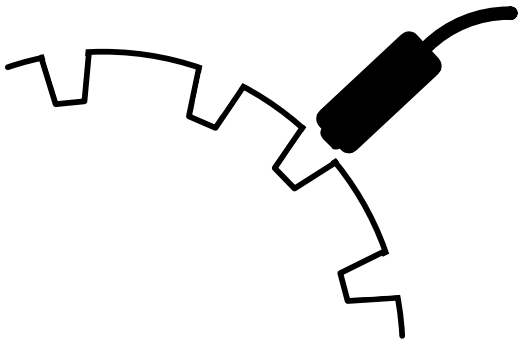


Figure 3. Negative tooth trigger wheel

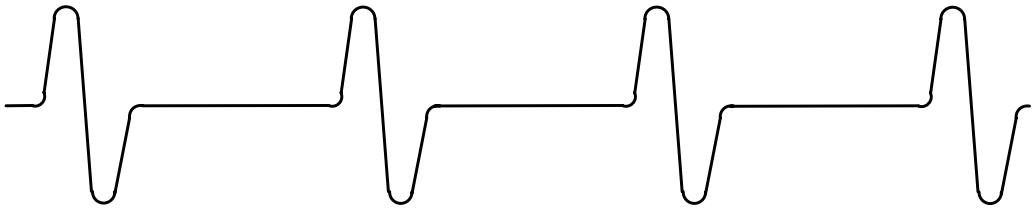


Figure 4. Correct signal polarity for VR input circuit

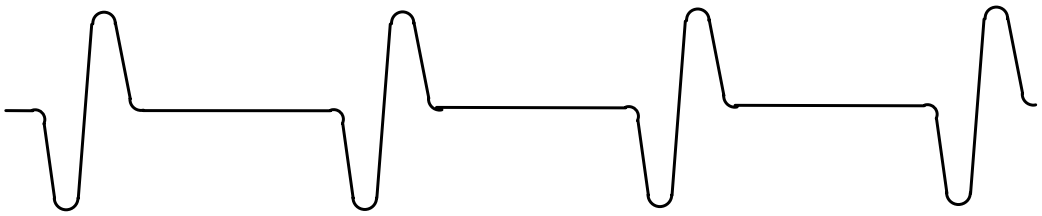


Figure 5. Incorrect signal polarity for VR input circuit

Each VR sensor input requires two connections. The VR Hall module pins labeled VR1 thru VR6 are the positive sensor inputs. The negative sensor inputs must be connected to GND pins on the module. The polarity of the sensor connection to the module is critical. The leads of the sensor should be connected such that the positive input of the VR circuit sees the waveform shown in Figure 4. The waveform shown Figure 5 is incorrect, and the VR circuit will not properly respond to this waveform. The rapid zero crossing of the VR signal must be in the negative direction.

The polarity of the physical tooth or gap on the trigger wheel will contribute to the polarity of the voltage pulse from the sensor. Figure 2 demonstrates a positive physical tooth polarity and Figure 3 demonstrates a negative physical tooth polarity. Assuming the lead polarity of a sensor remained the same, one of the configurations would generate the waveform shown in Figure 4, while the other configuration would generate the waveform shown in Figure 5.

Triggers wheels are designed so that the physical center of each tooth or gap corresponds to a known angular position of the wheel. This physical center of the tooth or gap always corresponds to the rapid zero-crossing of the generated voltage pulse.

The VR circuit is designed so that the rapid negative zero-crossing of the raw sensor signal corresponds to the rising edge of a digital pulse sent to the RIO FPGA. The VR output signal to the FPGA will go TRUE at the rapid negative zero crossing of the external VR pulse and remain TRUE until the external VR pulse returns to 0V. An example of this is shown in Figure 6. Within LabVIEW FPGA the system designer can route this digital signal to the EPT CrankSig or CamSig input. The signal can also be routed to any other speed measurement sub-VI.

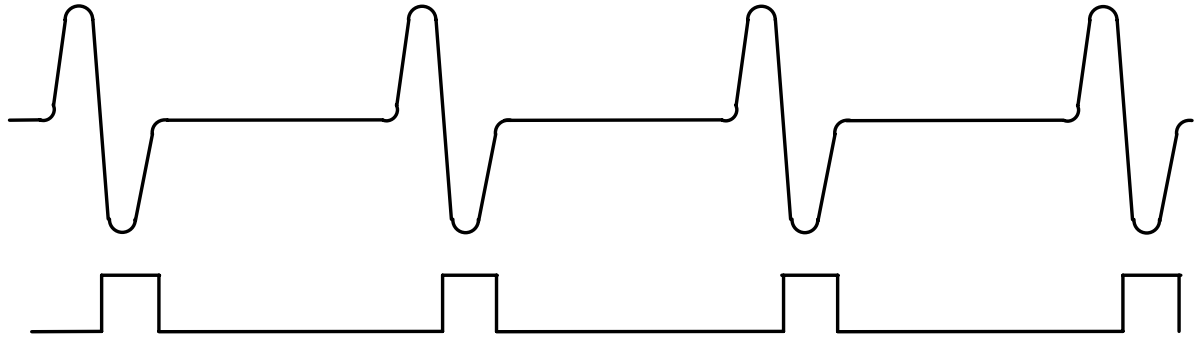


Figure 6. VR input pulse and resulting digital output from VR circuit

The absolute maximum VR pulse amplitude allowed by the circuit is +/-150 volts. If the input signal exceeds this voltage, damage may occur to the circuit. The amplitude should not exceed +/-150 volts at maximum engine speed. The minimum VR pulse amplitude that will generate a digital output by the VR circuit is +/-200 millivolts.

The VR circuit implements adaptive noise rejection features during continuous incoming VR pulses. In general, an adaptive arming threshold voltage is generated with each VR pulse and bleeds down thereafter. The next pulse must have an amplitude that exceeds the arming threshold in order for a digital output to be generated at the rapid zero-crossing. The initial arming threshold is set to approximately 70% of each pulse's amplitude.

Given a constant gap between the sensor and the trigger teeth, the amplitude of a VR pulse is directly proportional to the speed of the trigger wheel. For example, if the VR amplitude at 1000 RPM is +/-10 volts, then the amplitude at 2000 RPM will be +/-20 volts. By using an oscilloscope to measure the VR amplitude at a low speed, this relationship can be used to determine what the maximum amplitude will be at the maximum speed. If the maximum amplitude of +/-150 volts will be exceeded at maximum speed, then the sensor gap must be increased, or the designer must obtain a custom VR circuit configuration from Drivven.

## Hall-Effect Sensor Inputs

The VR Hall module provides up to six identical hall-effect sensor input circuits. The hall-effect inputs are designed to take a digital input from a hall-effect or proximity sensor. Typical sensors of this type will have an open-collector output, requiring a pullup resistor at the collector. The hall-effect inputs will also read active TTL compatible signals. The standard configuration includes a 4.7K pullup to 5V for use with open collector type inputs. The input is protected against typical automotive battery voltages and can be connected to actively-driven, battery voltage signals. Channels with this configuration are protected from voltage swings of +/-30V.

The circuit's output to the RIO FPGA reverses the polarity of the input by going low when the input voltage is greater than 2.0V. The output goes high when the input is less than 1.0V.

Figure 7 shows the standard configuration of the hall-effect sensor input circuits.

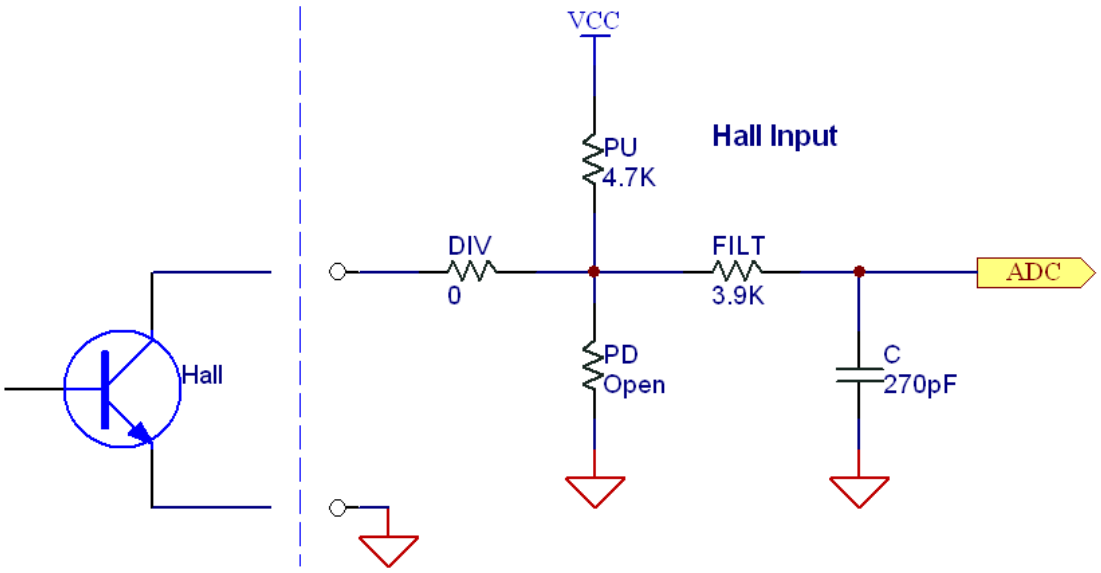



Figure 7. Hall-effect circuit input configuration

# Software Installer

The VR/Hall Module Kit is provided with an installer package which may be downloaded from Drivven's Sharepoint website after obtaining login access from Drivven. User's may go to http://portal.drivven.com/SoftwareDownload and enter the provided username and password to gain access to the specific product installer packages which have been purchased. The installer packages are executables which should be run on the intended development computer, having LabVIEW development tools installed. After installing the package, a "Start->Programs->Drivven->ProductRelease" menu item will be added to the desktop. The specific product will have an example LabVIEW project appear under the "Examples" menu and the user manual will appear under the "Manuals" menu. User's may copy and open the example project to experiment with the module or use as a starting point for a new application. All software files, example projects and documentation are installed to:

C:\Program Files\National Instruments\LabVIEW X.X\vi.lib\addons\DrivvenProductRelease\.

When working with block diagrams, user's will notice a "Drivven" function palette added to the standard LabVIEW palette, specific for the RT or FPGA target. VIs for a specific Drivven product will be categorized according to product name. Also, some Drivven products will install RT and FPGA VIs under a "General" function palette which is intended to be used across multiple products.

**Requirements**
The Drivven VIs require:

- LabVIEW 8.5 Full Development or later
- LabVIEW RT Module 8.5 or later
- LabVIEW FPGA Module 8.5 or later
- NI-RIO 2.4 or later

The VR/Hall Module Kit is provided with a LabVIEW FPGA VI for interfacing to the module and reporting VR and hall signal results.

Figure 8 shows the icon which represents vr_hall.vi.

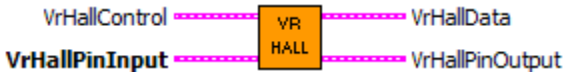


Figure 8. vr_hall_revx.vi icon with leads.

The FPGA VI must be placed within a Single Cycle Loop (SCL) of a LabVIEW FPGA block diagram. The SCL must execute at the default clock rate of 40 MHz.

The FPGA VI requires a pre-synthesized netlist file having a matching name and an extension of .ngc. The netlist file must be located in the same directory as the matching VI. The installer will place this file in the LabVIEW addons directory along with the FPGA VI.

# Creating a LabVIEW Project

Drivven recommends working from the provided example application as a starting point for learning the use of the Drivven software blocks. However, the following section describes starting a LabVIEW project from scratch and adding a Drivven module.

1.) Install the Drivven software by running the installer executable and accepting the software license agreement.
2.) Restart LabVIEW, if previously running, and create a new LabVIEW project.
3.) Give the new project a name by clicking the "Save Project" button on the project toolbar.
4.) Right click on the highest item in the project hierarchy ("Project:…") and navigate to "New->Targets and Devices…"
5.) Within the "Add Targets and Devices…" dialog, select the appropriate radio button, depending on whether you already have an existing powered and configured RT target on the network or if you are adding a new RT target which is not present yet on the network.
    a. Existing Target or Device
        i. Expand the appropriate category in the "Targets and Devices" list to see the discovered targets in that category.
        ii. Double-click the desired target to add it to your project.
    b. New Target or Device
        i. Expand the appropriate category in the "Targets and Devices" list to see all possible targets within that category.
        ii. Double-click the desired target to add it to your project.
6.) If the new RT target is not currently on the network, right-click on the RT target within the project and open the properties dialog to set the IP address or DNS name if necessary.
7.) Right-click on the RT target within the project and navigate to "New->Targets and Devices…"
8.) Within the "Add Targets and Devices…" dialog, select the appropriate radio button, depending on whether you already have an existing FPGA target connected to an existing RT target or if you are adding a new FPGA target which is not present yet.
    a. Existing Target or Device
        i. Expand the appropriate category in the "Targets and Devices" list to see the discovered FPGA targets in that category.
        ii. Double-click the desired target to add it to your project.
    b. New Target or Device
        i. Expand the appropriate category in the "Targets and Devices" list to see all possible targets within that category
        ii. Double-click the desired target to add it to your project.
9.) If the new FPGA target was not currently in the system, right-click on the FPGA target within the project and open the properties dialog to set the resource name if necessary. The resource name can be found from MAX when connected to the actual remote system.
10.) If the FPGA target is a PXI or PCI card, then a R Series expansion chassis must be added under the FPGA target. This is done by right-clicking on the FPGA target and navigating to "New->R Series Expansion Chassis". Within the following dialog, select the appropriate FPGA connector to which the chassis will be connected. A unique name for the chassis may also be specified.
11.) Right click on the R-Series expansion chassis or cRIO FPGA target chassis and navigate to "New->C Series Modules…"
12.) Select the "New Target or Device" radio button and double-click on the "C Series Module" in the "Targets and Devices" list. In the following dialog, select the desired Drivven module at the bottom of the "Module Type" list. The Drivven modules will be appended there if any Drivven module software has been installed. Select the appropriate module

location. Finally, specify an appropriate name for the module, which will later appear in the FPGA I/O nodes in the FPGA block diagram. Having meaningful module names is important for preventing coding mistakes.

13.) After adding a module to the project, a folder will automatically be added to the project having the same module name given in the module configuration dialog. The folder will contain the FPGA I/O pins for the module slot. These I/O pins can be selected in the block diagram when connecting the module VI PinInput and PinOutput clusters to FPGA I/O nodes. The example application, discussed below, should be consulted for further details about connecting the PinInput and PinOutput clusters to FPGA I/O nodes. Within the example projects, notice the FPGA I/O node elements having module name prefixes.

14.) Some Drivven modules can be automatically recognized by LabVIEW when adding cRIO modules to the project. However, Drivven does not recommend using this feature because the module names, which are automatically assigned, are not meaningful (Mod1, Mod2, etc) and can lead to coding mistakes when wiring the Drivven FPGA VIs to the I/O nodes. Adding the modules to the project manually, as described above, is still the recommended method.

# Sub VI Documentation

## vr_hall_revb.vi

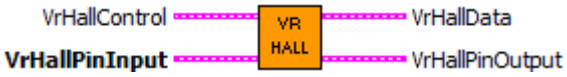
This VI is for interfacing directly with the Drivven VR/Hall sensor module and for providing an interface to the LabVIEW RT level.

The FPGA VI must be placed within a Single Cycle Loop (SCL) of a LabVIEW FPGA block diagram. The SCL must execute at the default clock rate of 40 MHz.

The FPGA VI requires a pre-synthesized netlist file having a matching name and an extension of .ngc. The netlist file must be located in the same directory as the matching VI. The installer will place this file in the LabVIEW addons directory along with the FPGA VI.

The PinInput and PinOutput clusters are wired to LabVIEW FPGA I/O nodes which are configured for a cRIO controller chassis or a cRIO R-Series expansion chassis. Refer to the LabVIEW FPGA documentation for details about creating and configuring FPGA I/O nodes.

**Connector Pane**




**Controls and Indicators**

**VrHallControl** Cluster of controls to select the sensor type for eac channel. When FALSE, the channel is configured for a VR sensor and is connected internally to the associated VR input pin of the module external connector. When TRUE, the channel is configured for a Hall sensor (or general purpose digital input) and is connected internally to the associated Hall input pin of the module external connector.

**VrHallPinInput** These boolean controls must be connected to their corresponding FPGA I/O Node input item.

**VrHallData** When selected as a VR sensor input, the VR/Hall output signal will go TRUE at the rapid negative zero crossing of the external VR pulse and remain TRUE until the external VR pulse returns to 0V. It is important to only use the rising edge of this digital signal because it is always lined up with the rapid negative zero crossing of the external VR pulse. When selected as a hall-effect sensor or general purpose digital input, the VR/Hall output is an inverted version of the external signal presented to the hall-effect input channel. The external output pins also reflect the same signal as presented to the RIO FPGA.

**VrHallPinOutput** The boolean indicator named IDSelectEn must be connected to a Set Output Enable method of an FPGA I/O Method Node. The boolean indicator named IDSelectOut must be connected to a Set Output Data method of an FPGA I/O Method Node. The remaining boolean indicators must be connected to their corresponding FPGA I/O Node output item.

## Warning About FPGA I/O Node Wiring

Great care should be taken to ensure that I/O nodes are wired to the correct PinInput and PinOutput clusters of the correct module VI. If wired incorrectly, then undefined behavior or module damage could result. LabVIEW FPGA does not yet provide a method for 3rd party module vendors to hide the DIO pins behind module VIs and still be portable to various system configurations. Therefore, a double-check of the I/O node wiring is recommended.

Two LabVIEW FPGA code snippets are shown below from an ADCombo implementation which illustrate this issue. Figure 9 shows the correct implementation of the FPGA I/O node block for the PinOutput cluster of the ADCombo. On the other hand, figure 10 shows a coding mistake that should be avoided. Notice the ADCombo output items where a Spark module output item is selected instead of the correct ADCombo module output item. This means that the Spark (DIO5) output is being driven by the ADCombo logic and will cause strange behavior of the spark module, or possible damage.

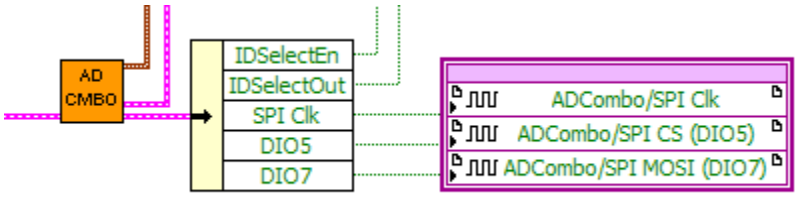



Figure 9. Representative FPGA output node for ADCombo with correct output item selection.

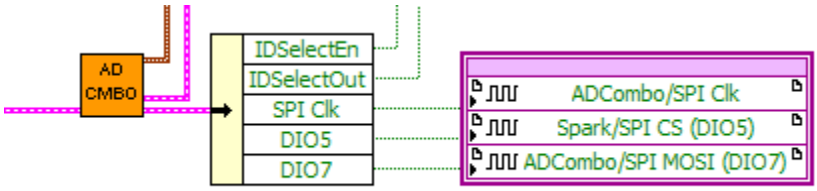



Figure 10. Representative FPGA output node for ADCombo with incorrect output item selection for DIO5. This will cause strange behavior or damage to the spark module. Applying meaningful names to the modules within the project can help identify these coding mistakes.

# Standard Circuit Configuration

The VR/Hall module is hardware-configurable. It may be ordered with the default options outlined below or may be custom ordered. It may not be configured by the user.

**Standard VR Configuration**

| Channel | VR Amplitude Voltage |
|---|---|
| 1 | +/- 150V |
| 2 | +/- 150V |
| 3 | +/- 150V |
| 4 | +/- 150V |
| 5 | +/- 150V |
| 6 | +/- 150V |

**Standard Hall Configuration**

| Channel | Pullup Resistor (ohms) | Pulldown Resistor (ohms) | Divide Resistor (ohms) | Break Frequency (Hz) | Intended Use |
|---|---|---|---|---|---|
| 1 | 4.7k | open | 0 | 150K | Hall, Prox, Switch or TTL |
| 2 | 4.7k | open | 0 | 150K | Hall, Prox, Switch or TTL |
| 3 | 4.7k | open | 0 | 150K | Hall, Prox, Switch or TTL |
| 4 | 4.7k | open | 0 | 150K | Hall, Prox, Switch or TTL |
| 5 | 4.7k | open | 0 | 150K | Hall, Prox, Switch or TTL |
| 6 | 4.7k | open | 0 | 150K | Hall, Prox, Switch or TTL |

# Custom Configuration

For an additional service charge, Drivven will custom configure each VR and/or Hall chanel. Customization can take place during or after module purchase.

When requesting a custom configuration please provide all of the following information.

| | |
|---|---|
| **Customer Business Name** | |
| **Contact Name** | |
| **Contact Phone** | |
| **Contact Email** | |
| **Shipping Address** | |
| **Unit Serial Number** | |
| **Has this unit been modified by the user?** | |

| Channel | Pullup Resistor (ohms) | Pulldown Resistor (ohms) | Divide Resistor (ohms) | Break Frequency (Hz) | Intended Use |
|---|---|---|---|---|---|
| **Hall 1** | | | | | |
| **Hall 2** | | | | | |
| **Hall 3** | | | | | |
| **Hall 4** | | | | | |
| **Hall 5** | | | | | |
| **Hall 6** | | | | | |

| Channel | VR Amplitude Voltage |
|---|---|
| **VR 1** | |
| **VR 2** | |
| **VR 3** | |
| **VR 4** | |
| **VR 5** | |
| **VR 6** | |

# Examples

The following screen capture in Figure 11 shows a LabVIEW FPGA block diagram with the VR/Hall FPGA VI used for general purpose speed measurement. The VR/Hall signals may also be routed to the CrankSig and CamSig inputs of Drivven's EPT VIs for engine position tracking. This FPGA application is entirely contained within a single cycle loop, clocked at the required 40 MHz. This example project and VI is included in the VR/Hall Module Kit VI software bundle.

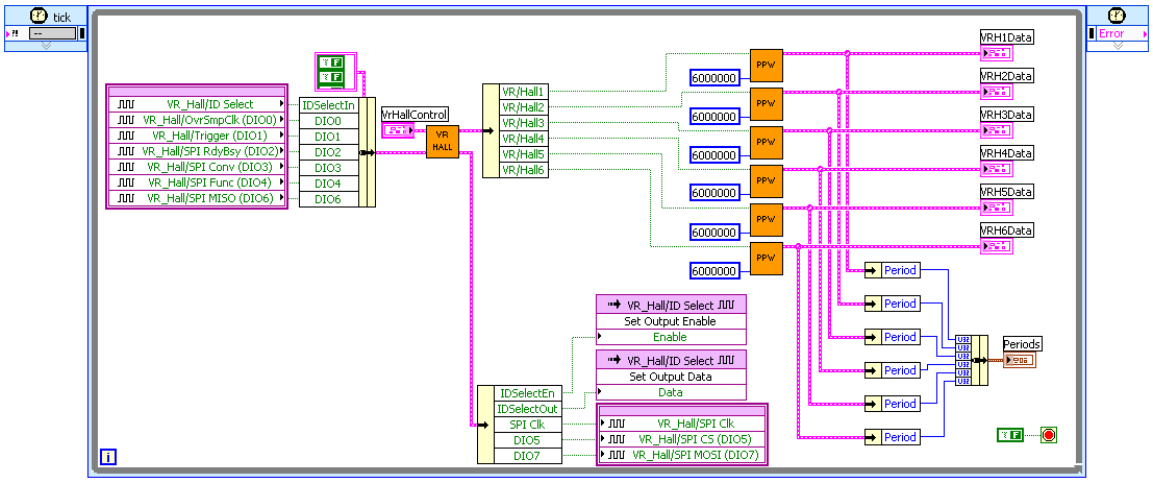



Figure 11. LabVIEW FPGA Block diagram example.