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Final Project Report
Stereo Audio Amplifier

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145-82-8718
ECE 20-32

ECE 20-32
Engineering Electronics

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May 8, 2000

Abstract of Design Project

Stereo Amplifier
By

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This report covers the design and implementation of a multi-stage stereo audio amplifier with its own voltage regulator, LED display, and digital volume control for each channel. The input can come directly from a CD audio player or similar device, and typical 8 Ohm speakers are driven. Digital volume control is implemented using a dipswitch, but this control device could easily be replaced by electronic components. The signal output is clean with no distortion up to certain audio levels, but some distortion occurs at higher levels.

The unit is designed with five distinct components. The power supply provides positive and negative 12 Volts. The digital volume control is implemented using a summing amplifier, and there is one for each channel. Amplification is done in two stages, each of which is centered on Bipolar Junction Transistors. The first stage is a Common Emitter Circuit that functions to amplify the voltage of the signal. This stage has a large output resistance and can not effectively drive 8 speakers. The second stage is a Class A-B Power Amplifier that provides the Common Emitter stage with a larger load, and is itself able to drive the low-resistance speaker with an acceptable current gain.

LED output was achieved using multiple comparators, which compare the output to predetermined levels and light the LED's when different levels are reached.

Finally, the chosen design performs almost perfectly to specifications (with distortion) when simulated in the Microsim PSPICE™ circuit simulator, but under actual construction there is higher amplification.

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1. Specifications

The product is to be suitable for in-home use. The input can be stereo or mono from any low impedance audio source such as a compact disc or MP3 player. The input must not exceed the maximum voltage level of 250mV peak, since audio quality can not be guaranteed at such levels. The system must drive two 8-Ohm speakers with a minimum gain of –3dB and 20dB. This is 0.7V/V and 10V/V in terms of amplitude. Additionally, there can be no more than a +/- 1 dB gain difference over the audible range of 300Hz to 10kHz without distortion.

The volume must be digitally controllable with 3 bits on each channel and there must be 4-stage LED indicators corresponding to 0.25V, .5V, 1V, and 2V output levels for each channel as well.

The system is run from the normal household wall socket supply of 120 Vrms at 60Hz. The design can be adapted to accept input from any type of audio plug. Output is adaptable to normal speaker wire.

2. Theory of Operation

The circuit is constructed of five distinct components: the power supply, the volume control, a Common Emitter Stage (or CEC), which functions to amplify the voltage signal, a Class AB Power Amplifier Stage (or Power Amp), which increases the current output, and an LED output stage. Each channel has its own volume control, CEC, Power Amp, and display circuitry. See figure 1 for a block diagram.

Figure 1 - Circuit Diagram
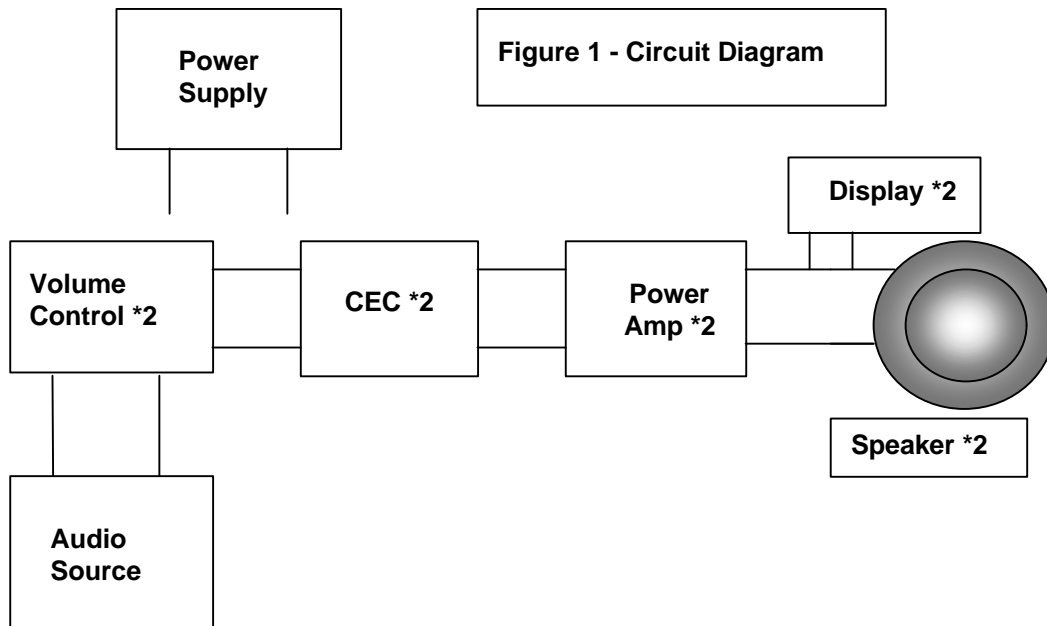
It was decided to control the volume by altering signal at the input stage. This was done with the summing operational amplifier configuration which allows for precise gain control with predetermined resistors. The signal then passes to the CEC stage, which has a high input impedance. The CEC circuit amplifies the voltage signal, and it has a large, adjustable output impedance so

it does not deliver current to the 8 load of the speaker. The class AB power

amplifier has a medium input impedance and a very low output impedance,

which allows it to drive the 8 speaker with little loss of gain. The output signal

is relayed to a series of comparators which compare the signal amplitude to the

predetermined voltages indicated in the specifications. When the output

reaches the predetermined value, the comparator is activated and outputs a

voltage which lights the appropriate LED. All of this is powered by the power

supply that reduces and rectifies the 120 Vrms wall socket signal into +/-12

VDC.

Each of these stages will now be explained in detail.

The Power Supply

The power supply takes the large AC signal from a household wall socket

and reduces and rectifies it to the +/- 12 Volt DC signals required to operate the

circuit. The first step is to pass the signal through a transformer with a ratio of

approximately 6:1. The secondary of the transformer outputs an AC signal with

30V peak waves. The signal is then fully rectified[1] into positive and negative

only signal sweeps using a standard bridge rectifier configuration (See figure 2).

The prototype used a pre-built bridge rectifier for space considerations and cost-

effectiveness, but assembly out of individual components is an alternative.

By taking the center tap of the transformer as ground, the rectified output

sweeps of the bridge rectifier nodes are defined as +15 and –15 Volt peak half-

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[1] Fully rectified meaning that there is a signal output for both the positive and negative input
sweeps

waves. The waves are then smoothed out by placing large (2200 uF) capacitors

between the positive/negative outputs and ground. The capacitors charge

during the output peaks and discharge when the waves are low. This smoothes

the signal into almost DC with some ripple. Voltage regulators are then used to

further smooth the signal and to provide a more reliable output.

It is important to note that interference and feedback in the power supply

was a significant problem once the entire circuit was connected. This problem

was alleviated by connecting large capacitors from the positive and negative

nodes to ground at multiple sites of the circuitry. The large capacitors act as

shorts to AC signals only, and so any distortions propagating in the supply lines

are grounded through them.

Figure 2 - Power Supply
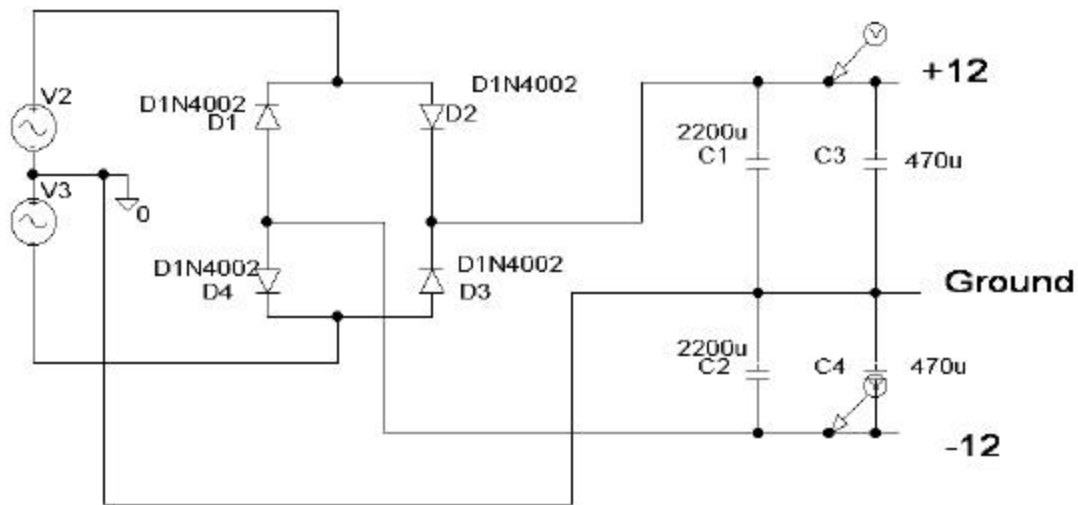
The Volume Control

There were several alternatives for digitally controlling the volume of the signal. One way was to alter the state of the amplifying CEC circuit by using the dipswitch to change resistance values. This method introduces no noise, but there are several obstacles that make it impractical. Most importantly, specifications require exact decibel volume control, corresponding to 0.707 and 10 V/V gains.

The gain of the CEC is most easily controlled by changing the value of Rc in the circuit. However, such changes have far reaching implications. By changing Rc, the bias of the entire circuit is altered. Furthermore, the output impedance of the circuit depends directly on Rc, so these changes also affect the transfer of the signal to the Power Amp. All of these interconnected reliances make precise calculation of overall gain levels impractical.

The circuit was designed with gain control happening at the input of the circuit. Since whatever goes into the circuit was multiplied by 10, the maximum input gain was 1 and the minimum was 0.07. These gains were achieved precisely by using an operational amplifier in the weighted summer configuration (see figure 3).

With the weighted summer, the gain, which is the ratio of the output voltage to the input voltage, is controlled by changing and adding resistances between the source and the inverting input node. There is also a feedback

resistance Rf, which is static. The equation for the gain is:

$$Av = -\left(\frac{Rf}{R1} + \frac{Rf}{R2} + \text{K} \ \frac{Rf}{Rn} \right)$$

In this design, there was one Rn activated for each bit of the dipswitch. The specifications were exceeded by implementing a fourth bit, which enabled elimination of the input signal for each channel completely. While the maximum and minimum gains were defined, the intermediate steppings were left open. The constraints were that with only the base resistor connected the gain of the control would be 0.07 and with all of the bits activated, the gain would be 1.

Since the human ear hears on a logarithmic scale (6db is twice as loud), it was determined to calculate the gains of each bit accordingly. With 3 bits there are 8 possible states. Dividing the difference between 20db and –3db into 8 pieces, the required gain for each bit was determined. See Table 1 for the resistance values.

Table 1 - Control Resistance Values	
R000	14.3 k
R001	28.8 k
R010	3 k
R100	1.8 k

The volume control was tested and the results are shown in table 2.

Table 2 - Volume Control Results (500mV peak in)			
Binary	Base 10	Output (peak)	Gain
000	0	35	0.07
001	1	50	0.1
010	2	200	0.4
011	3	216	0.432
100	4	290	0.58
101	5	300	0.6

110	6	440	0.88
111	7	500	1

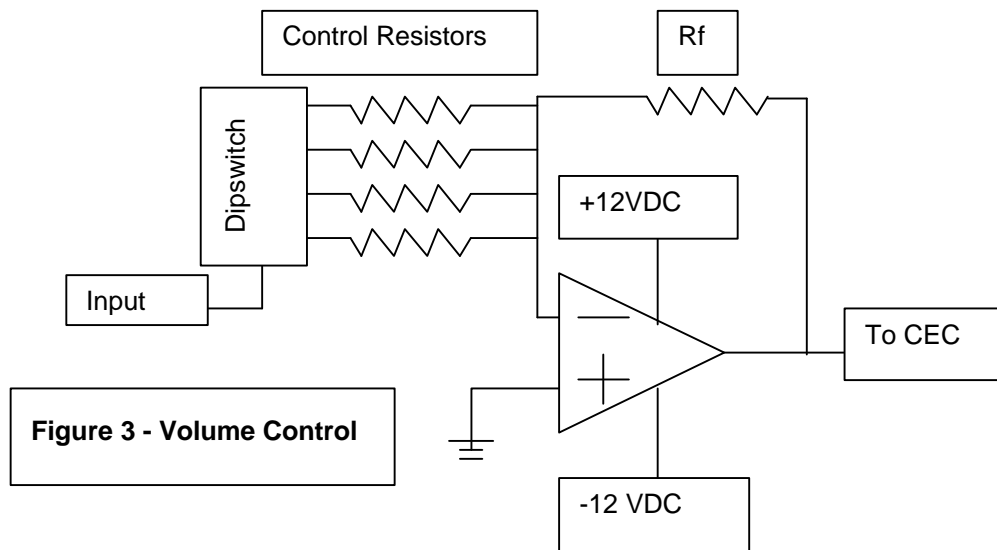The results show that the output behaved and added according to the formula.


Figure 3 - Volume Control

One problem that occurred was the introduction of a hum upon the addition of the volume control. It was later determined that this may have come from the operation amplifier's existence before the amplification process. The amplifier uses the positive and negative power supply lines to do its amplification, and any small variances are transferred through the op amp into the signal that it outputs. In this way, the small supply ripple is then magnified along with the reset of the signal in the amplification stages.

It is possible to control the gain at the output stage of the circuit by placing the operational amplifier at the output stage of the circuit. This way the small supply distortion is not magnified by the rest of the circuit, and there is the added bonus of the op-amp's high input impedance and low output impedance.

However, this is not very power efficient because tpower is wasted by the circuit in amplifying the signal which is then cut down in the end by the volume control.

The CEC

The CEC Circuit has a large voltage gain and works using the inherent amplification properties of the NPN BJT. See Figure 3. The concept is to use the BJT to amplify small variations of the current input into the base node. IB is

Figure 4 - CEC

Volume Control
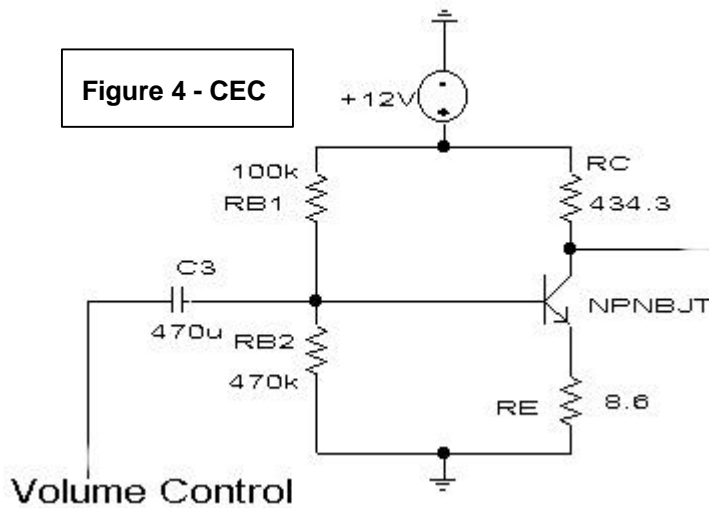
increased by an input voltage variation and this current is amplified by a factor Beta (a large number that can vary from BJT to BJT) in IC, the current flowing into the Collector node. The connection to the collector node has a resistance in series, so when current flow increases into C, there is a voltage drop at C, and vice versa. This is the essential logic behind the CEC, and note that since an increase in the input voltage causes a decrease in the output voltage, the output signal is reversed and the gain is a negative number. This, however, does not matter with audio output. The exact current amplification in IB, which comes from input variation, is a function of the resistor RB along with the other parameters of the circuit and the circuit bias.

Biasing of the CEC is the design work for this stage. It is required that the BJT always stay in forward active mode, meaning that the voltage in the collector is always higher than that of the base which in turn must be higher than that at the emitter node. For undistorted amplification, this relationship must

remain true up to the highest and lowest peaks of the output. Since there is a

single voltage source of 12V, maximum amplification can occur with 12V peak

to peak, providing 6V peaks from a bias point of 6V. This is a rough maximum,

as the base voltage must be at least 07 Volts above the emitter voltage, which is

at 0V minimum but is often at a higher voltage. Additionally, when the base

voltage increases slightly (from input), the collector voltage will be at its

minimum, meaning that peaks will create the absolute worst case for

maintaining forward active mode.

There is a single voltage source (in this case +12V DC) with which to

create the bias, and the balance is adjusted with values of the resistors RB1,

RB2, RC, and RE. The source and load resistances connected to the CEC do

not affect its operation because they are coupled to it with capacitors, which act

as open circuits to DC values and short circuits to signals with high enough

frequency. This phenomenon comes about from the equation for impedance of

a capacitor, $Z = 1 / jwC$. As can be seen, impedance is reduced by a high

frequency w and by a high capacitance C. In order to create a minimal

resistance for the inputs and outputs of the circuit for the entire frequency range,

it is necessary to use as high a capacitance value as possible. Polar capacitors

may fail if the incorrect voltage polarity is maintained across them, but for the

AC values with high enough frequencies and low enough voltages, this never

happens. Capacitors are also used for coupling the output of the CEC to the

input of the Power Amplifier. This is done because the bias voltage of the CEC

collector is approximately 6V and it is desired for the signal and not this steady voltage level to be sent to the power amplifier.

Note that the load resistance does greatly affect the gain of the CEC by acting as a resistance to ground in parallel with RC in the small signal realm. This reduces the current running though RC (by half if Rload = RC), which in turn reduces the gain. This is one reason why the CEC must be designed for a gain much higher than the required gain. Roughly, the highest gain possible out of the CEC is 24 V/V. Additionally, in order to maintain maximum power transfer to the Power Amplifier, it is desired that RC of the CEC equal the input load of the Power Amp. This is a design constraint that illustrates the complex interoperation of the circuit as a whole.

The bias point is controlled differently and in complex ways by each of the resistors in the circuit. The values RB1 and RB2 are used to control the bias voltage and current of the base. A larger value of RC will increase possible gain but alter the bias point of the collector. It was observed that varying the value of RE could control the output gain, but that it was also easy to create distortion this way. Since the specifications require precise output levels, using a dipswitch to change any of these resistance values was deemed unacceptable.

It is important to note that the standard BJT is capable of immense amplification, but that this is actually harmful given the voltage swing limits imposed by the power supply. In order to reduce the gain and take account for the variability of Beta from BJT to BJT, the resistor Re must not be shorted to ground for the small signal. The presence of Re in the small signal domain

causes the gain formula to contain a Beta value in the numerator and the denominator, and so these large numbers balance each other. There are techniques to control the Re seen for DC bias and the AC signal independently, and these involve the use of capacitors to bypass parts of Re and introduce different Re's to the small signal. Further research may be able to utilize this for more optimal bias and gain control.
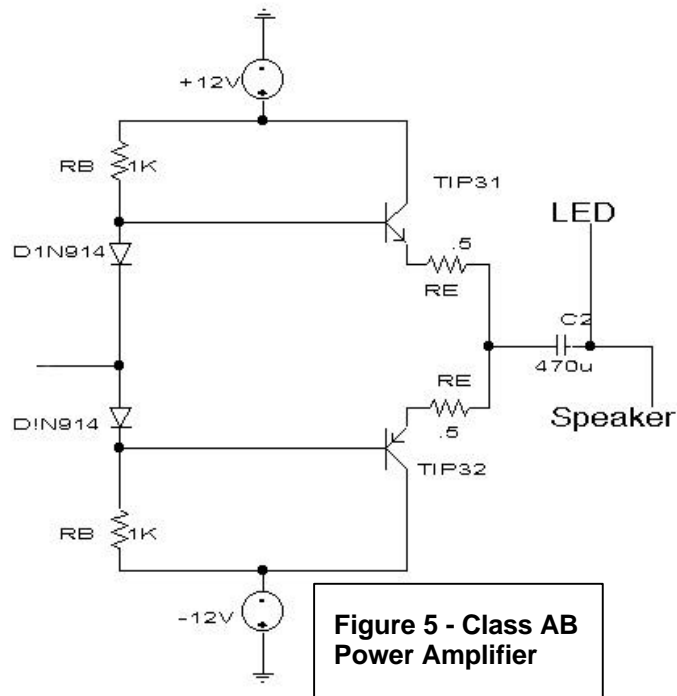
The spice circuits and results are shown in the Spice section, but the following tables report the values used and the results.

Table 3 - Design Values for CEC				
Part	Value		Part	Value
RB1	100kOhm		RE	8.6 Ohm
RB2	470kOhm		C1 (input)	470 uF
RC = Rout	434.3Ohm		C2 (output)	2* 0.82 uF

Table 4 - Bias Point of CEC (simulated)				
Measurement	Value		Measurement	Value
IB	0.109 mA		VB	0.9 V
IC	17.9 mA		VC	4.24 V
IE	18 mA		VE	0.15 V

The Power Amplifier

The power amplifier in itself produces a gain of approximately 1 without a load. The theory of the system utilizes the 0.7V voltage drop which always exists between the base and emitter provided the BJT is in forward active mode. Signal input is at the base, and when the signal rises by a certain voltage, the emitter voltage rises accordingly. Proper biasing of the collector and emitter is accomplished by simply grounding the emitter and connecting the collector directly to the voltage source. If the voltage input were directly connected to the base, there would be two problems: input values lower than 0.7V would not cause a rise in the emitter because the BJT is not in forward active mode, and negative sweeps of the input signal would not be seen for the same reason. An option to allow positive and negative sweeps is to use a resistor and the voltage source so as to bias the base as done for the CEC, but this creates a constant flow of current through the circuit, which wastes power. The answer is to add a pnp BJT connected to a negative voltage source (see figure 5).

Figure 5 - Class AB Power Amplifier

With a negative input swing the NPN BJT is off but the PNP BJT is sent into forward bias, allowing current flow. Because of symmetry, note that the output node (the emitter of each) is essentially at 0V with no input. Also note that without input there is no current flow through the BJT's, which saves power.

To solve the 0.7V voltage clipping, it is desired to bias both of the bases at + or – 0.7V. This is accomplished by connecting diodes between the source and the base and ensuring that enough current runs through them by connecting the branch to the voltage sources. Note that once again the input bias voltage is essentially zero because of symmetry. Biasing the bases in this manner eliminates clipping because both bases are already on the verge of forward active mode. Unfortunately, this bias allows for small amounts of current to flow through both branches, which reduces the efficiency of the circuit.

The input resistance is approximately r_{pi}, which is Beta/gm. In turn, gm is directly proportional to IC, the current flowing through the BJT's. The input impedance is not as important as the output impedance, which has been found to be proportional to the 1/(ip+in), ip and in being the current running through the BJT's. Since the two are complementary, this values remains fairly constant at the bias point. It can be seen that in order to obtain a small Rout, a large biasing current is required.

It was found that the bias current through the BJT's could be increased by lowering the RB values seen in Figure 5. However, when a signal is amplified by the circuit, the values of ip and in get much larger, and this reduces

the value of Rout, causing runaway current flow. It is quite easy to destroy standard BJT's in this manner. To avoid this, Power BJTs (TIP31 and TIP32) were used. These transistors are capable of handling very large currents without being destroyed. The large currents still caused heat issues, and this was somewhat alleviated by attaching heat sinks to the BJT's. Furthermore, the the values of the RB values were balanced to 1 k to reduce overheating and power consumption without creating too large an output resistance.

Another purpose of the RB's is to allow enough current flow to ensure a voltage drop across the diodes while not wasting power by allowing too much. The diodes used were D1N914's. These diodes are rated with higher conductance and faster response than the usual D1N4002 diodes.

Note the presence of small RE's. These resistors prevent runaway current flow which can occur as the BJT's heat up and allow increased current to flow. Increased current causes an increased voltage drop across the resistors, reducing the emitter voltage and reducing the current flow in the first place. See Tables 3 and 4 for the design values and bias point of the Power Amp.

Table 5 - Design Values for the Power Amp				
Part	Value		Part	Value
RB1	100kOhm		RE	62.8 Ohm
RB2	50kOhm		C1 (not pictured)	470 uF
RC = Rout	760Ohm		C2 (not pictured)	470 uF

Table 6 - Bias Point Values of Power Amp (simulated)				
Measurement	Value		Measurement	Value
IB (npn)	2.17 mA		VB1	0.73 V
IB (pnp)	1.7 mA		VB2	-1.18 V
IC1=IC2	19.1 mA		VE	-0.21 V

The LED Display

The concept behind the LED display is a simple array of comparators, one comparator for each light. An integrated bar display having 10 lights was used to provide a cleaner looking circuit, and it was decided to make the middle two lights power indicators, and for the level indications to extend to the left for the left channel and to the right for the right channel. The overall effect was very professional.

Since an operational amplifier is required for each comparator, it was decided to use comparator chips, each containing 4 op-amps. This made the stage more compact and required a smaller number of connecting wires. However, this compactness also made the wiring very crowded and difficult to navigate.

Figure 6 - Single LED Stage
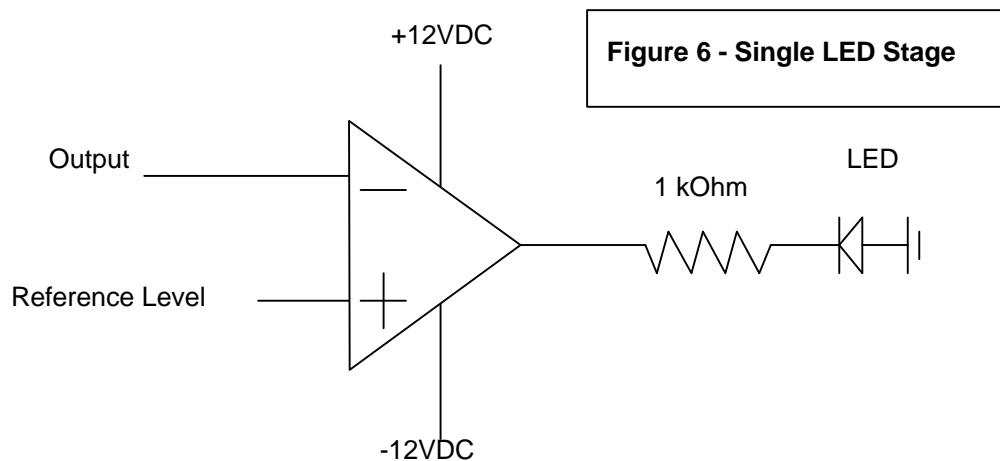
The comparator is the most basic use of the operational amplifier. If the non-inverting input (plus sign) is more than a little larger than the inverting input

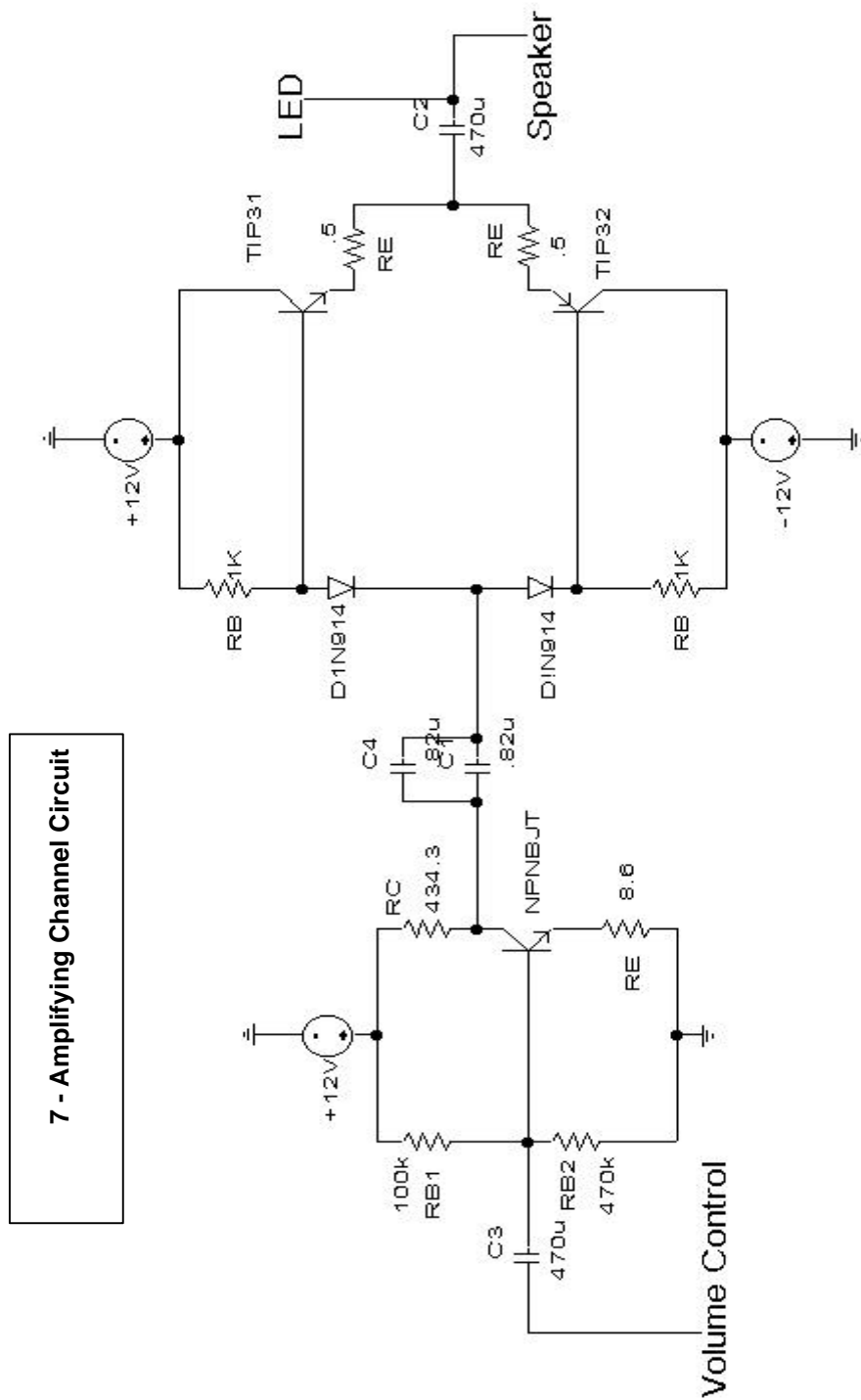(minus sign), the voltage +VDC (in this case +12V) is output. −VDC is output for the reversed case.

In this design, a voltage splitting ladder was first designed to set up the reference voltages required by the specifications. The ladder runs from +12 supply line to ground. The resistance values and corresponding voltages are found in the following table.
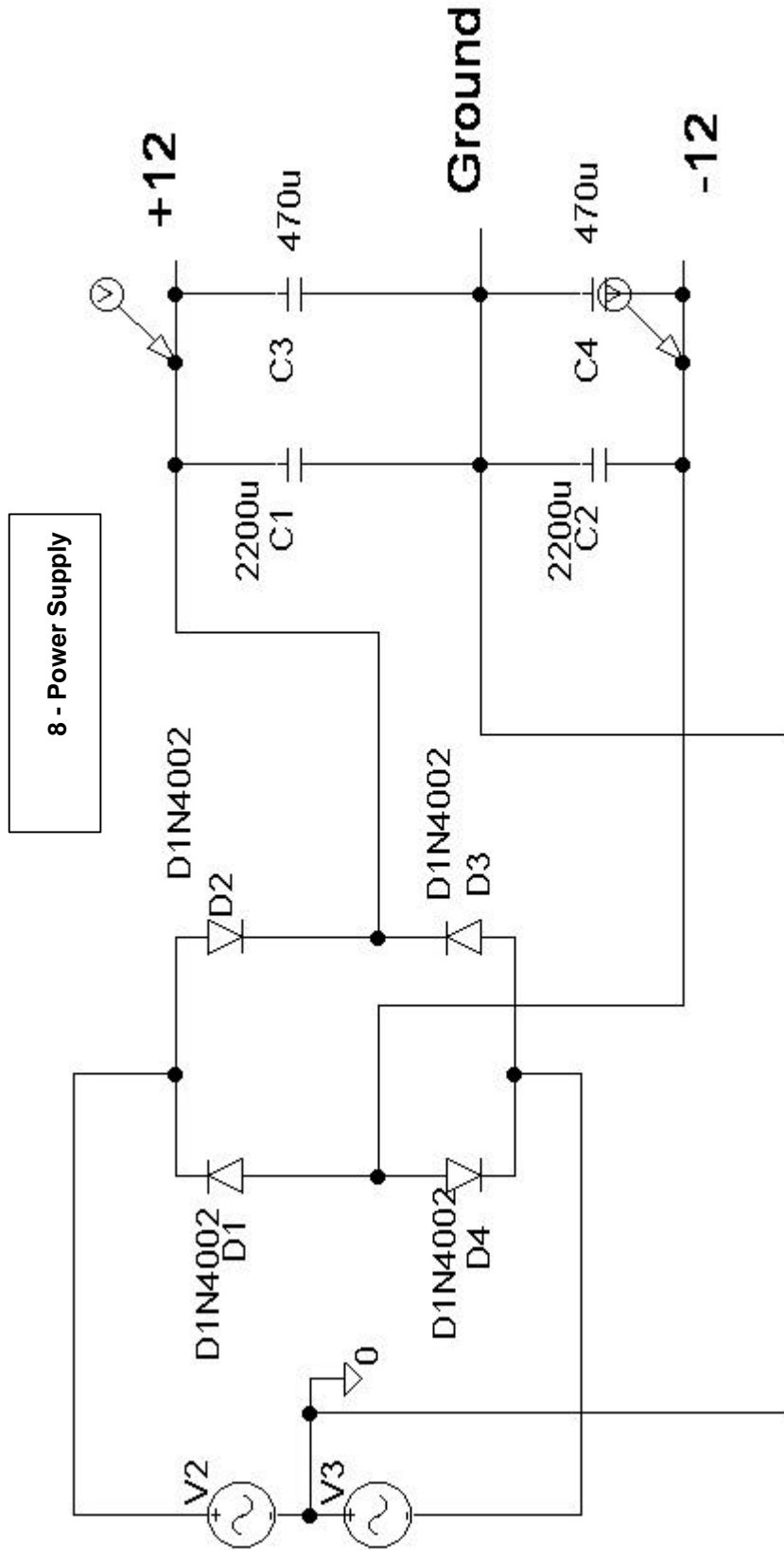
Table 7 - Voltage Ladder Values	
Resistor	Voltage at Low End
40kOhm	2 V
4kOhm	1 V
2kOhm	0.5 V
1kOhm	0.25V
1kOhm	0 V

The operational amplifiers in each of the chips were set up with these voltages as the reference vales. The output from the power amplifier was fed into the input nodes of the op-amps. Capacitors were used to remove DC bias values. Whenever the level increased above the reference value, the comparator would output a -12 Volt value. This caused the LED to become forward biased and to light up. A 1 kOhm resistor is placed in series with the LED to prevent over current in the LED. While this configuration does not give LED output on negative output swings, this in inconsequential since the frequencies are so high.

3. Circuit Diagrams, Layouts, and Wiring
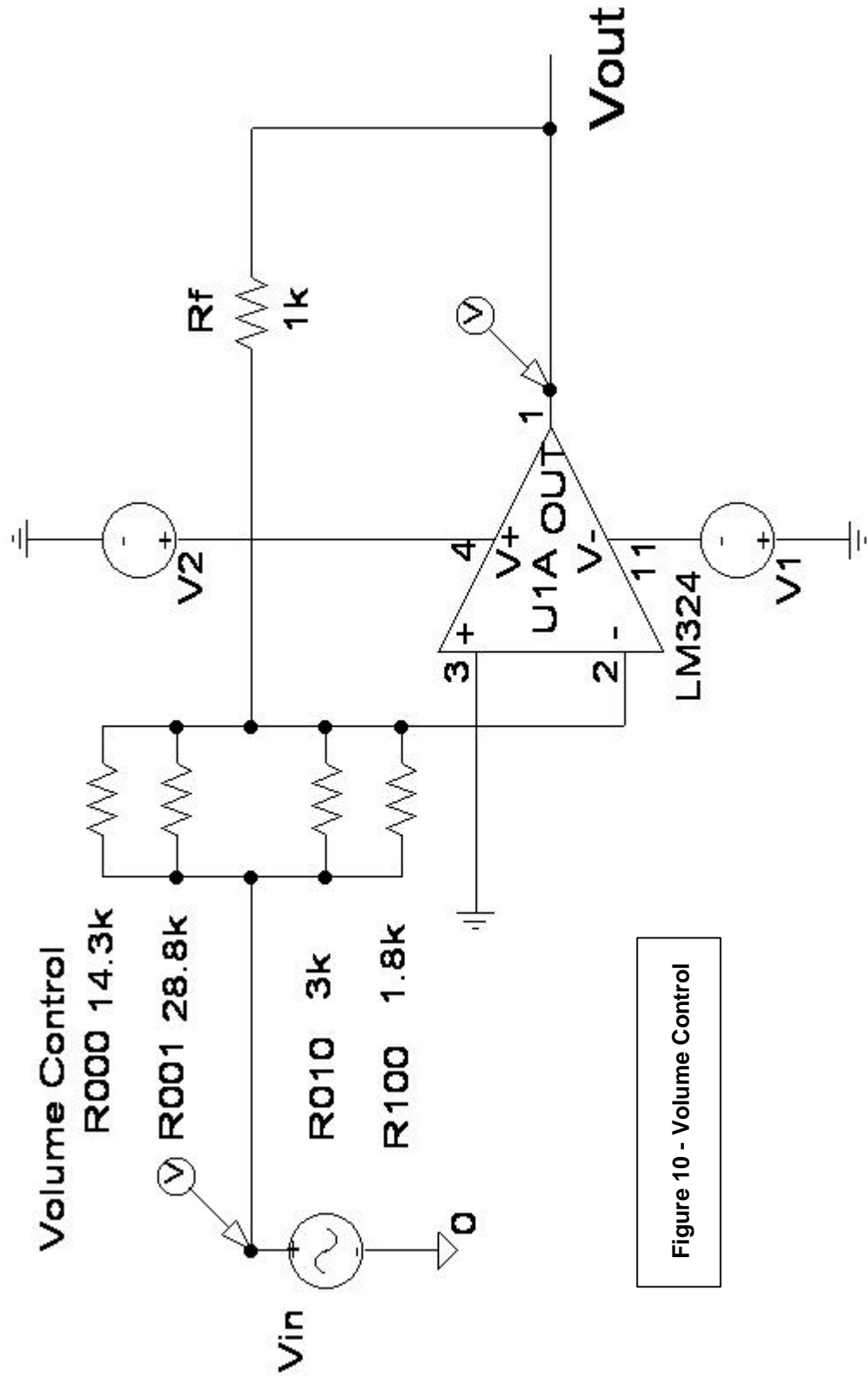
See figures 7-10 for the entire circuit.

7 - Amplifying Channel Circuit

8 - Power Supply

Figure 10 - Volume Control

Physical Layout
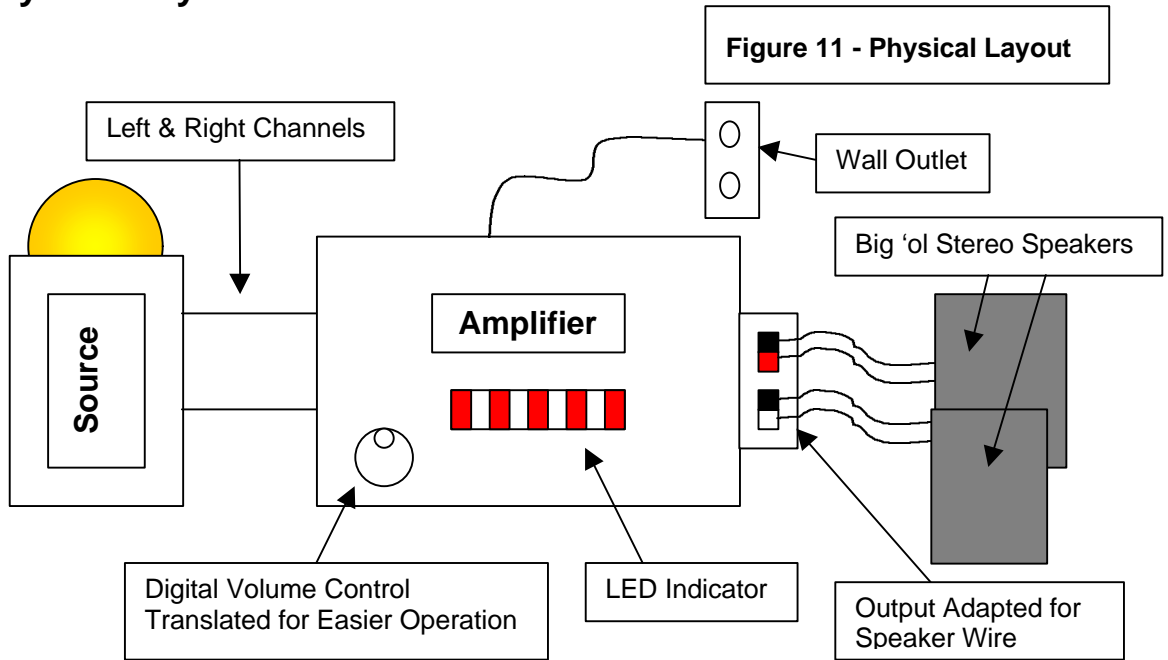
Figure 11 - Physical Layout

Left & Right Channels

Wall Outlet

Big 'ol Stereo Speakers

Amplifier

Source

Digital Volume Control
Translated for Easier Operation

LED Indicator

Output Adapted for
Speaker Wire

4. Spice Simulation

Spice simulation resulted in inexact, yet satisfactory behavior. Generally, capacitors in spice created much more impedance to the AC signal than they did in real tests. Because of this, all capacitors in spice were set to 100mF for simulation purposes. The layouts in the previous section were used for simulation. Lack of available parts made it necessary to substitute LM324 op-amps in place of the LM741C models that were actually used. Furthermore, center-tapped transformers and dipswitches were not available in pspice. Voltage regulators are also not found in pspice, and so the output signals are seen without their effects.
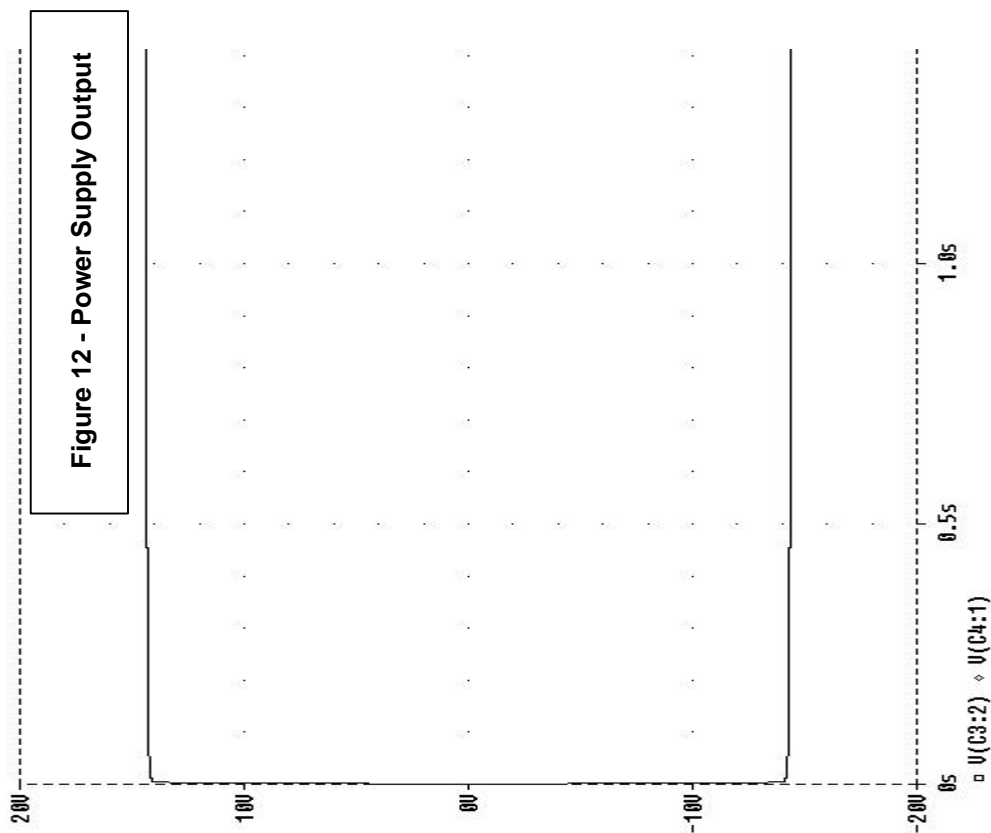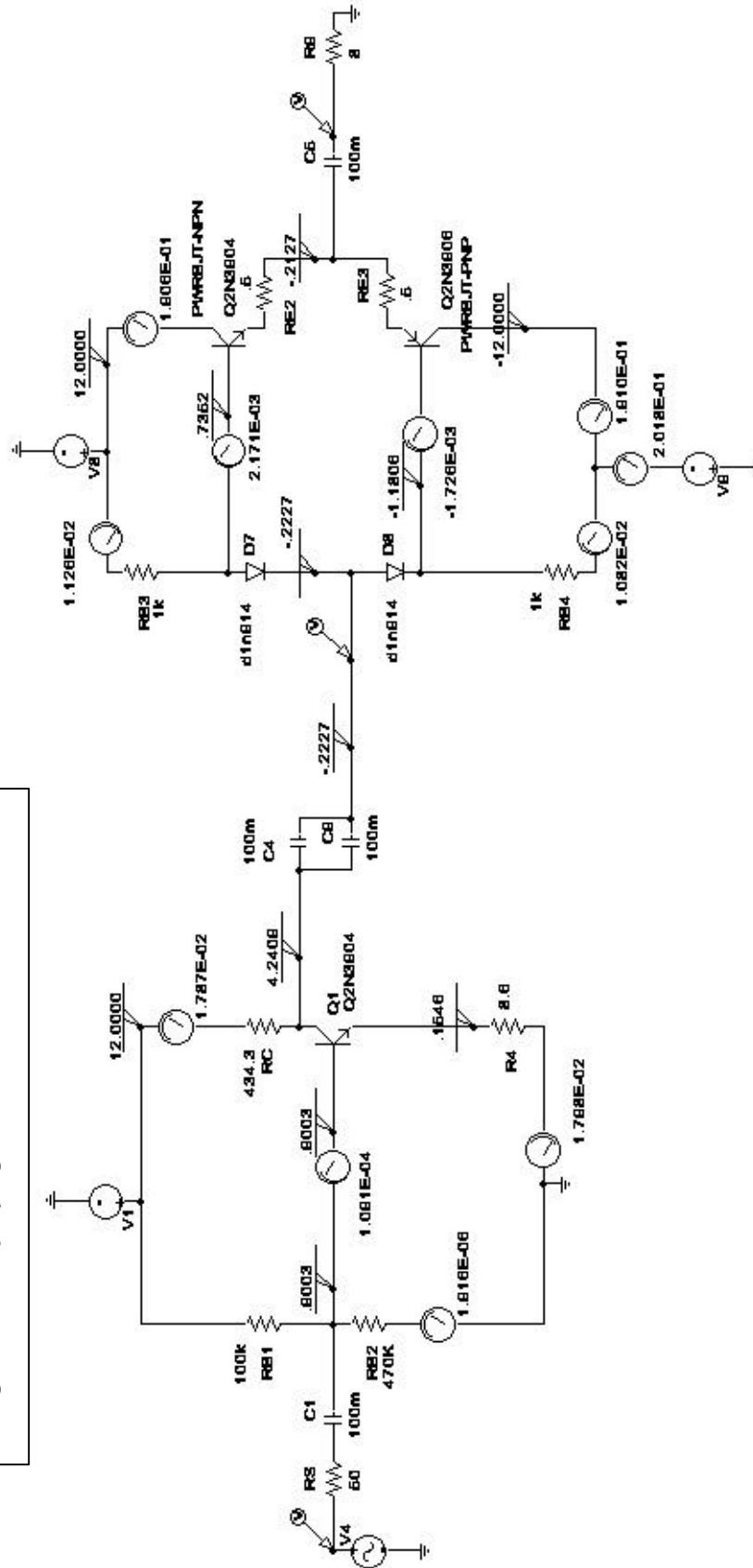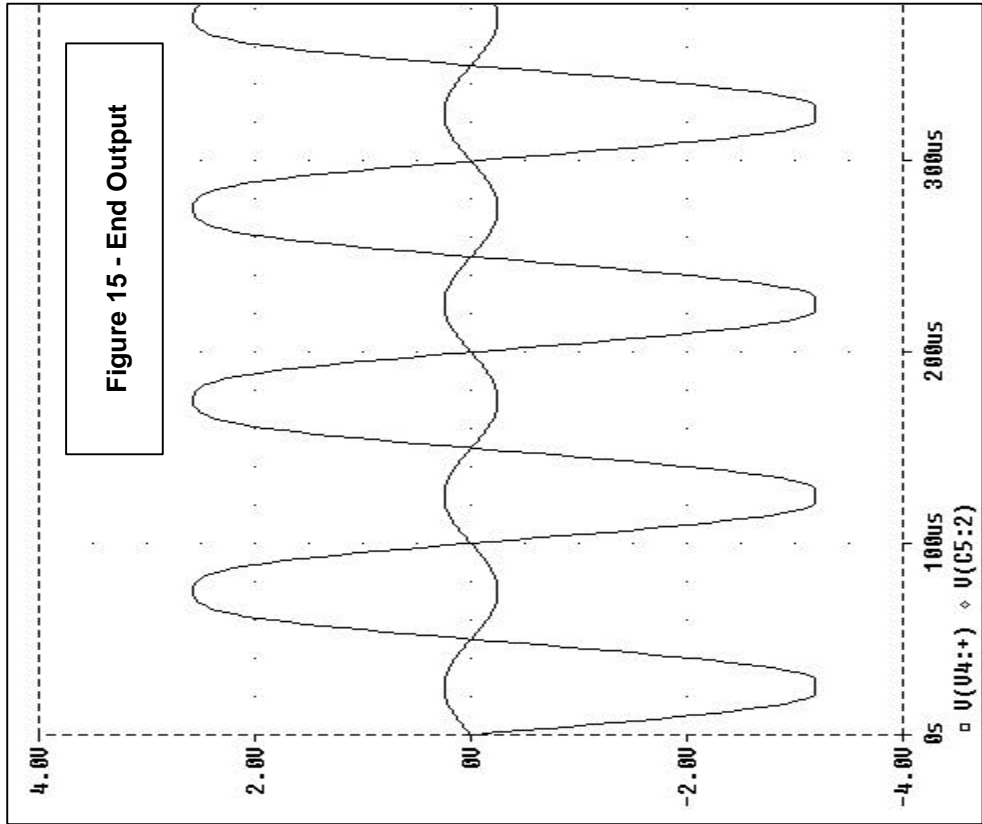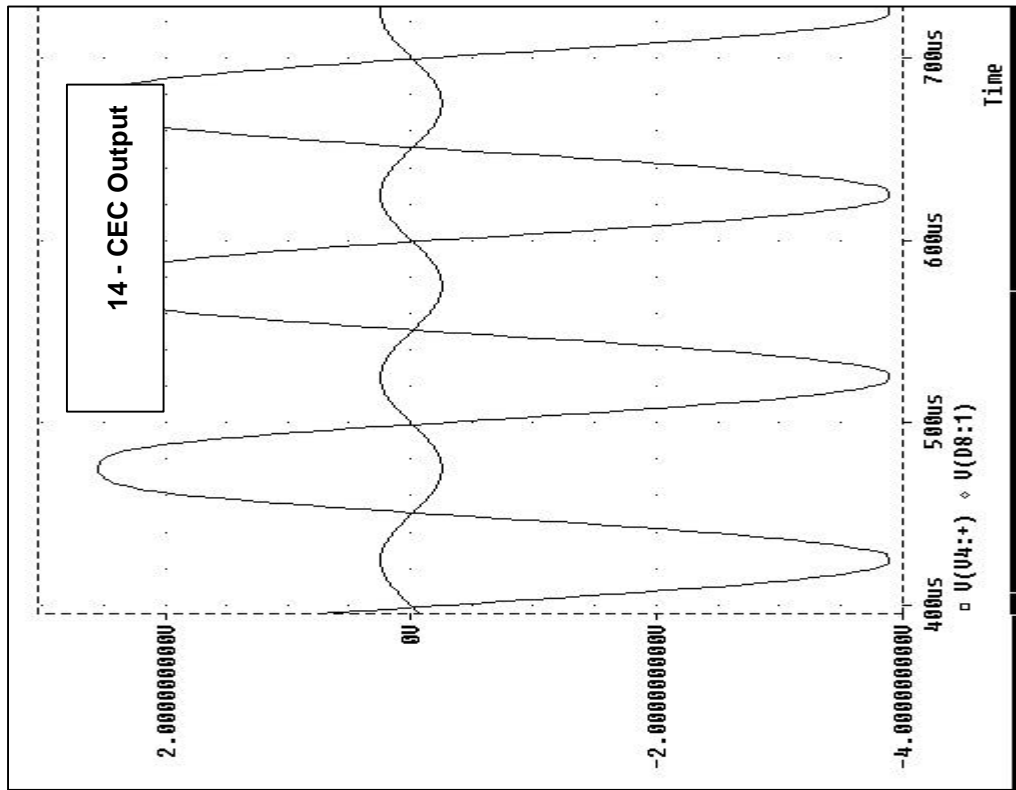

Figure 12 - Power Supply Output

Figure 13 - Amplifying Test Circuit with Bias Point

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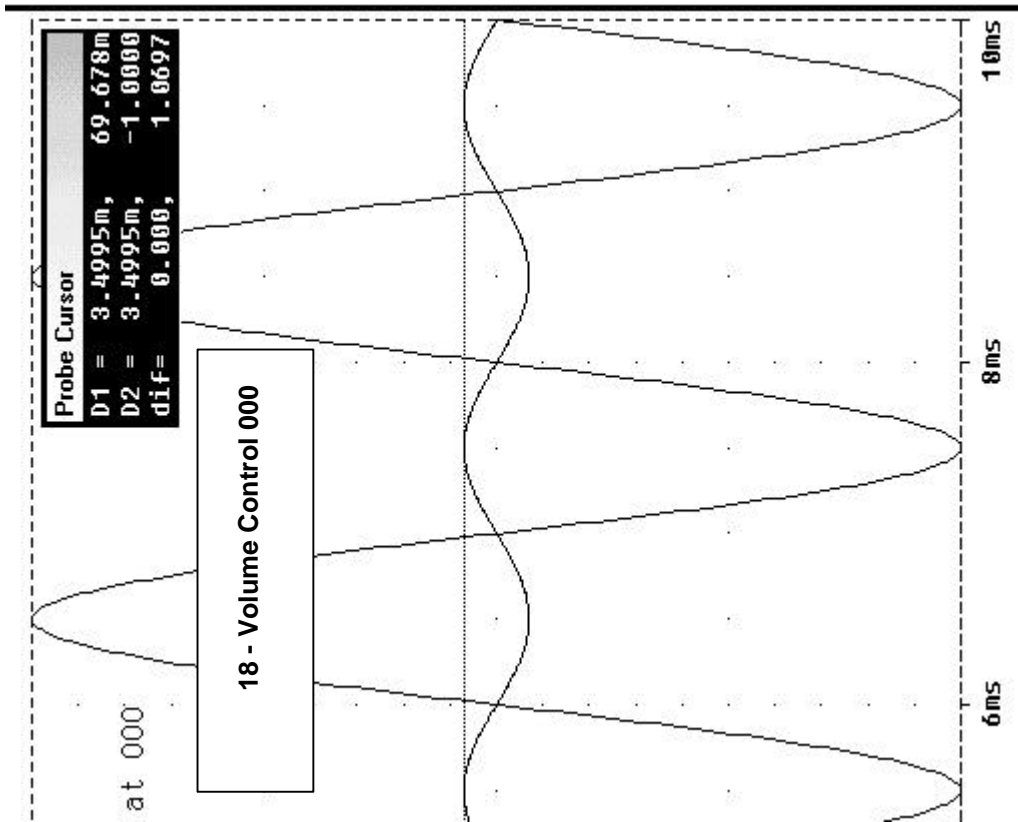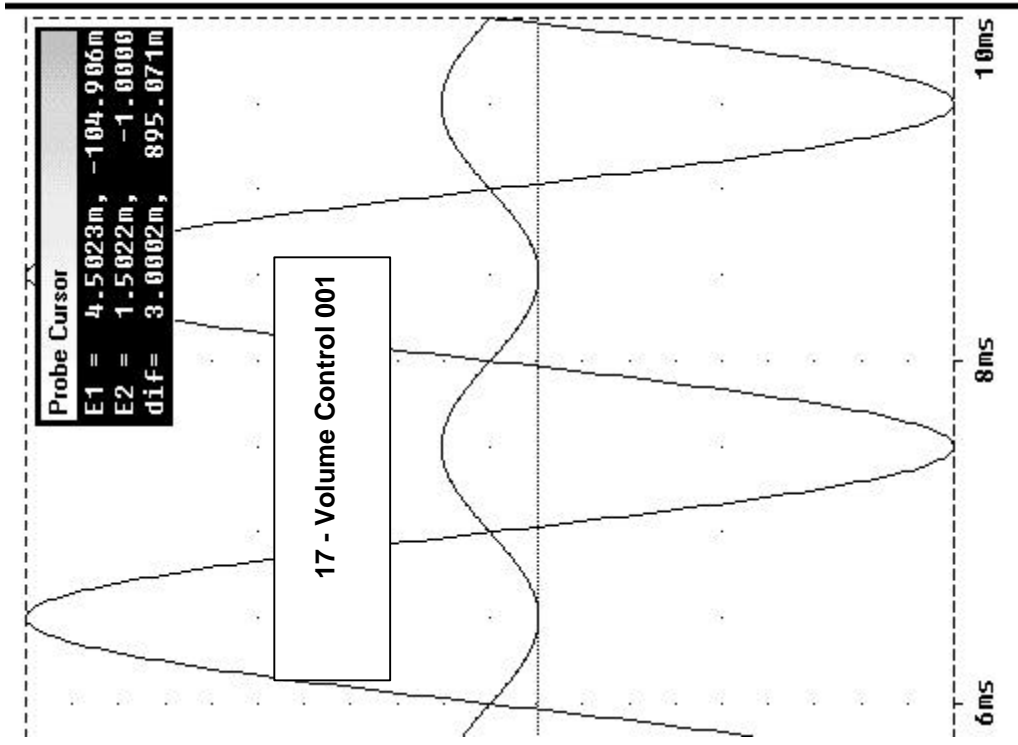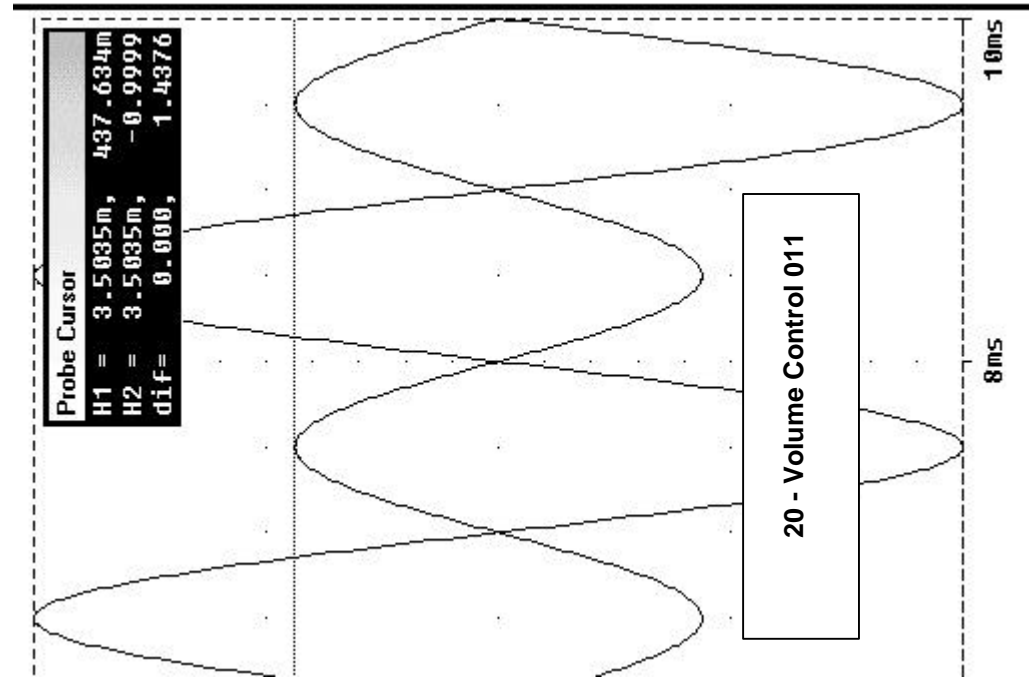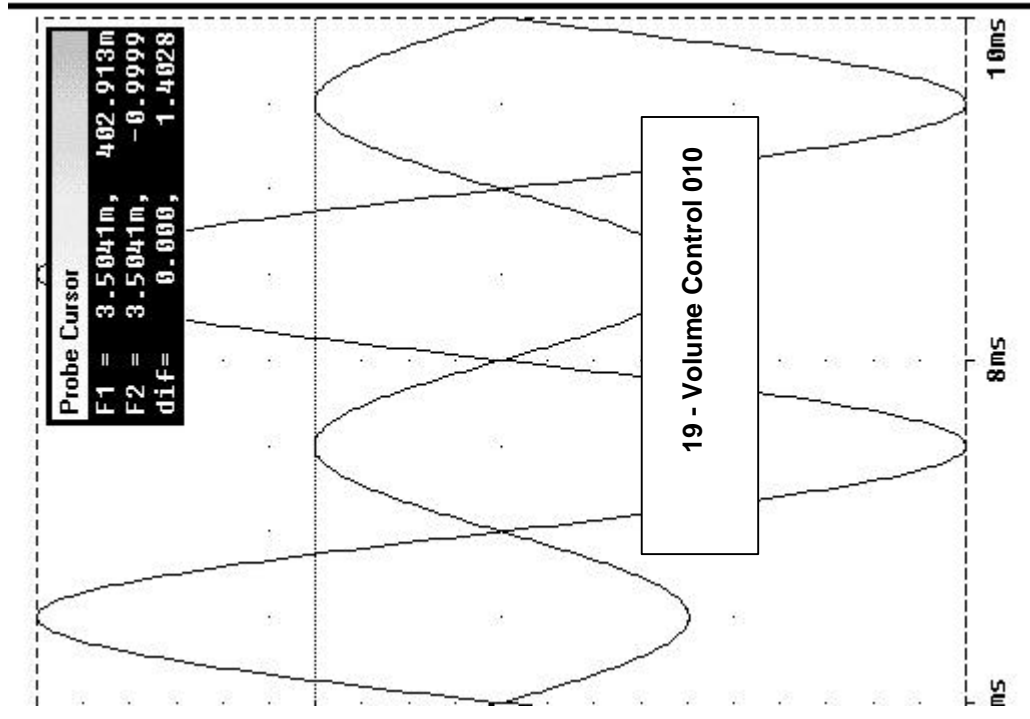Figure 15 - End Output

14 - CEC Output

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Figures 14 and 15 show the simulated outputs of the amplifying stages. The smaller waves are the input and the larger ones are the output. Note that the circuit shows clipping on the negative swings, but this clipping does not appear in the real circuit. In the real circuit, there is distortion in the positive swing when amplitudes are high. This distortion could be removed with tuning of the CEC for lower gain levels. This circuit was designed for maximum gain possible but unforeseen distortion was realized too late in the game.

Figure 16 shows the response of the LED driving circuit. When the input is hither than the reference voltage, the comparator outputs negative 12 Volts which turns the led on.

Figures 17, 18, 19, and 20 show the output levels of the volume control at different binary digits. The smaller wave in each case is the output, and these simulations correspond to the measurements taken and reported in Table 2.

16 - LED Driving Op Amp Response

B1 = 24.900m, 775.413m
B2 = 26.114m, 877.821m
dif= -1.2146m, -102.408m

10.00000000U

0U

-10.00000000U

24ms   28ms   32ms   36ms   40ms

□ U(Uin:+)   ◇ U(U1A:OUT)

Probe Cursor

E1 = 4.5023m, -104.906m
E2 = 1.5022m,   -1.0000
dif= 3.0002m, 895.071m

17 - Volume Control 001

6ms ___ 8ms ___ 10ms

Probe Cursor

D1 = 3.4995m, 69.678m
D2 = 3.4995m,   -1.0000
dif= 0.000,   1.0697

at 000

18 - Volume Control 000

6ms ___ 8ms ___ 10ms

20 - Volume Control 011

19 - Volume Control 010

22 - Volume Control 111

Probe Cursor
G1 = 5.5019m,   625.109m
G2 = 5.5019m,   -1.0000
dif=   0.000,   1.6251

21 - Volume Control 100

5. Testing Procedure

To test performance, an audio source, cable connection, wall outlet (120 Vrms @ 60 Hz), and two speakers with wire are required. The audio source is connected to the input, the speakers to the output, and the power supply is plugged into the wall.

Connecting a signal generator to the input and an oscilloscope to the output allows for comparison to determine the gain. In place of a speaker, an 8 resistor may be attached to the output. Distortion can also be seen on the oscilloscope.

6. User's Manual

Operation:

- Attach input and speaker output.

- Plug in amplifier

- Begin playing audio and adjust volume control as desired.

Maintenance:

- If circuit malfunctions, use voltmeter to check forward bias of BJTs.

  Replacement of BJT's may be required.

- If distortion begins or a burning smell develops, disconnect power supply.

  Allow circuit to cool. Service may be required.

Safety Precautions:

- Do not touch open circuitry when power is enabled.

- Do not run the circuit at full volume for prolonged periods of time without

  adequate ventilation or cooling.

- Do not swallow or lick the circuit.

- The circuit is not for children under 12 years of age as it contains small

  parts which may be harmful if swallowed.

7. Electrical Parts List

Table 8 – Electrical Parts List			
Number	Name	Part Number	Description
2	NPN BJT	2N3904	Silicon Bipolar Junction Transistor
2	NPN Pwr BJT	TIP 31	
2	PNP Pwr BJT	TIP 32	
4	Diode	1N914	High Conductance Diode
4	Breadboard		Standard Electrical Breadboard
2	2200uF Cap.		Electrolytic Capacitors
2	Comparator	Radio Shack 339	Quad-Comparator Chips
2	Heat Sink		
1	LED Display	Radio Shack	10-Element LED Bar graph Display
1	Bridge Rectifier	Radio Shack	Full-Wave Bridge Rectifier
2	LM741C		Operational Amplifier
1	Transformer		18V CT

8. Conclusions

The circuit was an overall success, but things did not turn out as originally planned. The initial intention was to build the preamplifier stage using a CSC Mosfet design, but satisfactory performance could not be achieved. Additionally, the experimentation with power amplifier design resulted in the destruction of many NPN and PNP BJT's. Design progress was delayed while additional parts were on order.

There is distortion in the circuit output at high levels and this could have been avoided if it had not been for a miscalculation in the gain requirements. The circuit was mistakenly built for the highest possible gain, while a lower gain would have been sufficient with less distortion.

The gain at frequencies higher than 500 Hz is 21.3 dB. At 300 Hz the gain is 20.6 dB. This makes the maximum difference over the range 0.7 dB, which is within specifications. The circuit produces full amplification at frequencies up to 250 kHz. The loss of gain at the lower amplitudes is most likely due to impedance from the capacitors used as DC blockers. The loss at higher frequencies may be due to interferences or the internal capacitances of the BJT's. See Appendix 1 for printouts of the resulting frequencies.

The spice analysis was not as encouraging as the constructed circuit. This shows that while spice may be a valuable tool in some respects, it is no replacement for direct experimentation. The final design was achieved mostly through a series of trial, error, and tweaking potentiometers. Circuit knowledge

was used to adjust appropriate values until acceptable results were produced.

Further improvements on the design are planned.

9. References

Sedra, Adel S, and Kenneth C. Smith. <u>Microelectronic Circuits.</u> New York: Oxford University

    Press, 1998.

Appendices

Appendix A: Circuit Measurements

Following are results of the circuit at varying frequencies.