AXM-A75

Multifunction I/O Mezzanine Module

USER'S MANUAL

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IMPORTANT SAFETY CONSIDERATIONS

It is very important for the user to consider the possible adverse effects of power, wiring, component, sensor, or software failures in designing any type of control or monitoring system. This is especially important where economic property loss or human life is involved. It is important that the user employ satisfactory overall system design. It is agreed between the Buyer and Acromag, that this is the Buyer's responsibility.

1.0 GENERAL INFORMATION

The AXM-A75 is a high speed analog input/output mezzanine board compatible with Acromag's line of re-configurable PMC and XMC FPGA modules. The AXM-A75 has 16 differential analog inputs, 8 analog outputs and 16 digital inputs/outputs.

KEY FEATURES

High Speed Analog Input - sixteen independent 16-bit Analog to Digital Converter (ADC) channels provide simultaneous sampling at a maximum rate of 500 KHz. The digitized output of each ADC is simultaneously input to the Field Programmable Gate Array (FPGA) for data collection and processing.

Programmable Input Voltage Range - four gain selections are available that allow a bipolar input voltage range from ± 1.28 Volts to ± 10.24 Volts.

Analog Output – eight 16-bit Digital to Analog Converter (DAC) channels provide simultaneous update with a maximum rate of 100 KHz.

Programmable Output Voltage Range – three gain selections are available that allow a bipolar output voltage range from ± 10 Volts to ± 10.5263 Volts.

Calibration Constants – factory calibration constants used to correct gain and offset errors are stored in on-board FLASH memory. Correction constants are stored for each channel and gain selection combination. Gain and offset correction are supported for both analog input and analog output.

General Purpose Digital Input or Output – sixteen general purpose I/O signals are provided. The outputs are pulled high via pull-up resistors.

Example Design – the example VHDL design provided in the base board EDK provides the following features:

- Control of ADC sample rate and gain selection.
- Gain and offset error correction is applied in FPGA hardware for analog inputs and on-chip for analog outputs.
- Each ADC channel includes a FIFO capable of storing 2050 samples.
- All enabled ADC channels are sampled simultaneously. ADC sample rate can range from 1/34 Hz to 500 KHz.
- Control of DAC gain selection.

Analog Input FIFO Status Interrupts – Interrupts can be generated when an input channel's FIFO half full condition is reached or when a FIFO overflow occurs.

ENGINEERING DESIGN KIT

Acromag does not provide an engineering design kit specifically for the AXM-A75 module. However, an example design is included in the Engineering Design Kit of the PMC/XMC base board. Refer to the PMC/XMC base board's manual for further information on the available Engineering Design Kit.

BOARD CONTROL SOFTWARE

Acromag does not provide board control software specifically for the AXM-A75 series board. However, the AXM-A75 module can be accessed via the control software for the base PMC or XMC module. These products (sold separately) facilitate the product interface in the following operating systems: Windows™DLL, VxWorks, and Linux. Refer to the PMC/XMC base board's manual for further information.

2.0 PREPARATION FOR USE

UNPACKING AND INSPECTION

Upon receipt of this product, inspect the shipping carton for evidence of mishandling during transit. If the shipping carton is badly damaged or water stained, request that the carrier's agent be present when the carton is opened. If the carrier's agent is absent when the carton is opened and the contents of the carton are damaged, keep the carton and packing material for the agent's inspection.

For repairs to a product damaged in shipment, refer to the Acromag Service Policy to obtain return instructions. It is suggested that salvageable shipping cartons and packing material be saved for future use in the event the product must be shipped.

This board is physically protected with packing material and electrically protected with an anti static bag during shipment. It is recommended that the board be visually inspected for evidence of mishandling prior to applying power.

The board utilizes static sensitive components and should only be handled at a static-safe workstation.

CARD CAGE CONSIDERATIONS

Refer to the specifications for loading and power requirements. Be sure that the system power supplies are able to accommodate the power requirements of the carrier board, plus the installed PMC or

XMC modules, plus the AXM-A75 within the voltage tolerances specified.

IMPORTANT: Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature.

The lack of air circulation within the computer chassis is a cause for some concern. Most, if not all, computer chassis do not provide a fan for cooling of add-in boards. The dense packing of the mezzanine modules to the carrier board alone results in elevated module and carrier board temperatures, and the restricted air flow within the chassis aggravates this problem. Adequate air circulation must be provided to prevent a temperature rise above the maximum operating temperature and to prolong the life of the electronics. If the installation is in an industrial environment and the board is exposed to environmental air, careful consideration should be given to air-filtering.

Front Panel Field I/O Connector J1

The AXM-A75 front panel field I/O connector (J1) is a 68 pin VHDCI receptacle. A cable assembly and termination panel (or user defined terminations) can be quickly mated to the field I/O connector. The pin assignment for this connector is shown in Table 2-1.

Table 2-1 J1 Pin Assignment

Pin Description	Number	Pin Description	Number
GND	1	DIO0	35
DIO1	2	DIO2	36
DIO3	3	DIO4	37
DIO5	4	DIO6	38
DIO7	5	GND	39
DIO8	6	DIO9	40
DIO10	7	DIO11	41
DIO12	8	DIO13	42
DIO14	9	DIO15	43
GND	10	VOUT1	44
GND	11	VOUT2	45
GND	12	VOUT3	46
GND	13	VOUT4	47
GND	14	VOUT5	48
GND	15	VOUT6	49
GND	16	VOUT7	50
GND	17	VOUT8	51
GND	18	GND	52
VIN16-	19	VIN16+	53
VIN15-	20	VIN15+	54
VIN14-	21	VIN14+	55
VIN13-	22	VIN13+	56
VIN12-	23	VIN12+	57
VIN11-	24	VIN11+	58
VIN10-	25	VIN10+	59
VIN9-	26	VIN9+	60
VIN8-	27	VIN8+	61
VIN7-	28	VIN7+	62
VIN6-	29	VIN6+	63
VIN5-	30	VIN5+	64
VIN4-	31	VIN4+	65
VIN3-	32	VIN3+	66
VIN2-	33	VIN2+	67
VIN1-	34	VIN1+	68

The sixteen differential analog input channels are labeled VINx- and VINx+ where x is the channel number 1 to 16. Analog outputs are labeled VOUTx where x is the channel number 1 to 8. Digital input / output signals are labeled DIOx where x is bit 0 to 15. Signal returns are labeled GND.

Analog Inputs: Noise and Grounding Considerations

Differential inputs require two leads (+ and -) per channel, and provide rejection of common mode voltages. This allows the desired signal to be accurately measured. However, the signal being measured cannot be floating. It must be referenced to analog common on the AXM module and be within the normal input voltage range. Shielded cable of the shortest length possible is strongly recommended.

Non-Isolation Considerations

The board is non-isolated, since there is electrical continuity between the logic and field I/O grounds. As such, the field I/O connections are not isolated from the system. Care should be taken in designing installations without isolation to avoid noise pickup and ground loops caused by multiple ground connections.

3.0 PROGRAMMING INFORMATION

This Section provides the specific information necessary to program and operate the mezzanine board.

This mezzanine board is intended only for use on specific Acromag PMC/XMC FPGA modules. As such only a small portion of I/O memory space is currently reserved for operation of the mezzanine board. The remaining memory space is defined in the base board's User's Manual.

AXM-A75 Memory Map

The AXM-A75 specific memory space address map for the board is shown in Table 3-1. Note that the base address from the base PMC/XMC module in memory space must be added to the addresses shown to properly access the board registers. Register accesses as 32, 16, and 8-bits in memory space are permitted unless otherwise indicated. A detailed description of each of the registers follows after Table 3-1.

Table 3-1 Memory Map

PCIBar2 + (Hex)	D31 D16	D15 D00	PCIBar2 + (Hex)
0003 ↓ 7FFF	Reserved for base PMC/XMC Module		0000 ↓ 7FFC
8003	Board Status Register and Software Reset		8000
8007 ↓ 80FF	Reserved for base PMC/XMC Module		8004 ↓ 80FC
8103	Control Register		8100

PCIBar2 + (Hex)	D31 D16	D15 D00	PCIBar2 + (Hex)
8107	Status Register 0		8104
810B		Status Register 1	8108
810F		Digital I/O	810C
8113	Conversion Timer		8110
8117		FLASH data	8114
811B		Digital I/O Direction	8118
811F ↓ 81FF	unused		811C ↓ 81FC
8203		ADC 1 data	8200
8207	ADC1 gain correction		8204
820B		ADC 1 offset	8208
820F	unused		820C
8213		ADC 2 data	8210
8217	ADC 2 gain correction		8214
821B		ADC 2 offset	8218
821F	unused		821C
8223		ADC 3 data	8220
8227	ADC 3 gain correction		8224
822B		ADC 3 offset	8228
822F	unused		822C
8233		ADC 4 data	8230
8237	ADC 4 gain correction		8234
823B		ADC 4 offset	8238
823F	unused		823C
8243		ADC 5 data	8240
8247	ADC 5 gain correction		8244
824B		ADC 5 offset	8248
824F	unused		824C
8253		ADC 6 data	8250
8257	ADC 6 gain correction		8254
825B		ADC 6 offset	8258
825F	unused		825C
8263		ADC 7 data	8260
8267	ADC 7 gain correction		8264
826B		ADC 7 offset	8268
826F	unused		826C
8273		ADC 8 data	8270
8277	ADC 8 gain correction		8274
827B		ADC 8 offset	8278
827F	unused		827C
8283		ADC 9 data	8280
8287	ADC 9 gain correction		8284
828B		ADC 9 offset	8288
828F	unused		828C
8293		ADC 10 data	8290

PCIBar2 + (Hex)	D31 D16	D15 D00	PCIBar2 + (Hex)
8297	ADC 10 gain correction		**8294**
829B		ADC 10 offset	**8298**
829F	unused		**829C**
82A3		ADC 11 data	**82A0**
82A7	ADC 11 gain correction		**82A4**
82AB		ADC 11 offset	**82A8**
82AF	unused		**82AC**
82B3		ADC 12 data	**82B0**
82B7	ADC 12gain correction		**82B4**
82BB		ADC 12 offset	**82B8**
82BF	unused		**82BC**
82C3		ADC 13 data	**82C0**
82C7	ADC 13 gain correction		**82C4**
82CB		ADC 13 offset	**82C8**
82CF	unused		**82CC**
82D3		ADC 14 data	**82D0**
82D7	ADC 14 gain correction		**82D4**
82DB		ADC 14 offset	**82D8**
82DF	unused		**82DC**
82E3		ADC 15 data	**82E0**
82E7	ADC 15 gain correction		**82E4**
82EB		ADC 15 offset	**82E8**
82EF	unused		**82EC**
82F3		ADC 16 data	**82F0**
82F7	ADC 16 gain correction		**82F4**
82FB		ADC 16 offset	**82F8**
82FF	unused		**82FC**
8303		DAC 1 data	**8300**
8307		DAC 1 coarse gain	**8304**
830B		DAC 1 fine gain	**8308**
830F		DAC 1 offset	**830C**
8313		DAC 2 data	**8310**
8317		DAC 2 coarse gain	**8314**
831B		DAC 2 fine gain	**8318**
831F		DAC 2 offset	**831C**
8323		DAC 3 data	**8320**
8327		DAC 3 coarse gain	**8324**

PCIBar2 + (Hex)	D31 D16	D15 D00	PCIBar2 + (Hex)
832B		DAC 3 fine gain	8328
832F		DAC 3 offset	832C
8333		DAC 4 data	8330
8337		DAC 4 coarse gain	8334
833B		DAC 4 fine gain	8338
833F		DAC 4 offset	833C
8343		DAC 5 data	8340
8347		DAC 5 coarse gain	8344
834B		DAC 5 fine gain	8348
834F		DAC 5 offset	834C
8353		DAC 6 data	8350
8357		DAC 6coarse gain	8354
835B		DAC 6 fine gain	8358
835F		DAC 6 offset	835C
8363		DAC 7 data	8360
8367		DAC 7 coarse gain	8364
836B		DAC 7 fine gain	8368
836F		DAC 7 offset	836C
8373		DAC 8 data register	8370
8377		DAC 8 coarse gain	8374
837B		DAC 8 fine gain	8378
837F		DAC 8 offset	837C
8383 ↓ 1FFFFF	Reserved for base PMC Module		8380 ↓ 1FFFFC

FLASH Data Format

Factory calibration constants are stored in FLASH memory. The FLASH memory device is a Numonyx M25P10. **Error! Reference source not ound.** shows the memory map of the FLASH contents. All numeric constants are 32 bit values stored in little endian byte order.

Table 3-2 FLASH Memory Map

Addr	D31 D16	D15 D00	Addr
0007	FLASH ID = "AXM-A75" (null terminated character string)		**0000**
000B	10.24 Volt Range Channel 1 Offset		**0008**
000F	10.24 Volt Range Channel 2 Offset		**000C**
0013	10.24 Volt Range Channel 3 Offset		**0010**
	. . .		
0047	10.24 Volt Range Channel 16 Offset		**0044**
004B	10.24 Volt Range Channel 1 Gain		**0048**
004F	10.24 Volt Range Channel 2 Gain		**004C**
0053	10.24 Volt Range Channel 3 Gain		**0050**
	. . .		
0087	10.24 Volt Range Channel 16 Gain		**0084**
008B	5.12 Volt Range Channel 1 Offset		**0088**
008F	5.12 Volt Range Channel 2 Offset		**008C**
0093	5.12 Volt Range Channel 3 Offset		**0090**
	. . .		
00C7	5.12 Volt Range Channel 16 Offset		**00C4**
00CB	5.12 Volt Range Channel 1 Gain		**00C8**
00CF	5.12 Volt Range Channel 2 Gain		**00CC**
00D3	5.12 Volt Range Channel 3 Gain		**00D0**
	. . .		
0107	5.12 Volt Range Channel 16 Gain		**0104**
010B	2.56 Volt Range Channel 1 Offset		**0108**
010F	2.56 Volt Range Channel 2 Offset		**010C**
0113	2.56 Volt Range Channel 3 Offset		**0110**
	. . .		
0147	2.56 Volt Range Channel 16 Offset		**0144**
014B	2.56 Volt Range Channel 1 Gain		**0148**
014F	2.56 Volt Range Channel 2 Gain		**014C**
0153	2.56 Volt Range Channel 3 Gain		**0150**
	. .		

Addr	D31 D16	D15 D00	Addr
	.		
0187	2.56 Volt Range Channel 16 Gain		**0184**
018B	1.28 Volt Range Channel 1 Offset		**0188**
018F	1.28 Volt Range Channel 2 Offset		**018C**
0193	1.28 Volt Range Channel 3 Offset		**0190**
	. . .		
01C7	1.28 Volt Range Channel 16 Offset		**01C4**
01CB	1.28 Volt Range Channel 1 Gain		**01C8**
01CF	1.28 Volt Range Channel 2 Gain		**01CC**
01D3	1.28 Volt Range Channel 3 Gain		**01D0**
	. . .		
0207	1.28 Volt Range Channel 16 Gain		**0204**
020B	DAC Offset Channel 1		**0208**
020F	DAC Offset Channel 2		**020C**
0213	DAC Offset Channel 3		**0210**
	. . .		
0227	DAC Offset Channel 8		**0224**
0247	Unused		**0228**
024B	DAC Gain Channel 1		**0248**
024F	DAC Gain Channel 2		**024C**
0253	DAC Gain Channel 3		**0250**
	. . .		
0267	DAC Gain Channel 8		**0264**

Board Status and Reset Register (Read/Write, PCIBar2 + 8000H)

This read/write register is used to issue a software reset, view and clear pending interrupts, and to identify the attached AXM module. It may also provide other functions that are defined by the base board. Writing a "1" to bit 31 of this register will cause a software reset affecting both the PMC base board and the majority of AXM-A75 registers. Bits 15 to 13 are used for AXM identification code.

Read of this register reflects the interrupt pending status. Read of a "1" in bits 1 or 0 indicates that an interrupt is pending for the corresponding interrupt.

Table 3-3 Board Status and Reset Register 8000H

BIT	FUNCTION
31	Software Reset (Write Only)

BIT	FUNCTION	
30- 16	Reserved for base board	
15 - 13	AXM Identification bits (Read Only)	
	AXM-EDK	"001"
	AXM-A75	"011"
12 - 2	Reserved for base board	
1	FIFO overflow interrupt pending	
0	FIFO half full interrupt pending	

Control Register - (Read/Write, PCIBar2 + 8100H)

The control register is used to enable interrupts, control amplifier gain, control the FLASH chip select signal, and start/stop the A/D converter for each channel. See Table 3-4 for a description of each of the register bits.

Table 3-4 Control Register 8100H

BIT	FUNCTION
31	FIFO overflow interrupt enable
30	FIFO half full interrupt enable
29 – 28	Amplifier Gain "00" Gain 1, full scale input range ± 10.24 Volts "01" Gain 2, full scale input range ± 5.12 Volts "10" Gain 4, full scale input range ± 2.56 Volts "11" Gain 8, full scale input range ± 1.28 Volts
27	FLASH Select – This bit is connected directly to the "select" input of the serial FLASH device.
26	LDAC – transfer DAC data from data registers to output registers, all channels (write only, read zero)
25	CLR – clear DAC data registers to 0x00 all channels, (write only, read zero)
24 – 16	unused
15 – 0	Convert channel [16 .. 1]– each channel can be individually controlled 0 – channel stopped 1 – enable continuous conversion

Status Register 0 - (Read/Write, PCIBar2 + 8104H)

Status Register 0 provides access to the FIFO overflow and half full status bits for each channel.

Table 3-5 Status Register 0 8104H

BIT	FUNCTION

BIT	FUNCTION
31- 16	FIFO overflow interrupt pending / clear channel [16 .. 1] A '1' indicates that at least one A/D sample was lost due to an attempted write to a full FIFO. Write a '1' to clear the bit.
15 - 0	FIFO half full interrupt pending channel [16 .. 1] A '1' indicates that there are at least 1024 samples in the FIFO.

Status Register 1 - (Read/Write, PCIBar2 + 8108H)

Status Register 1 provides access to the FIFO empty status bits for each channel.

Table 3-6 Status Register 1 8108H

BIT	FUNCTION
31 – 16	Unused
15 – 0	FIFO empty channel [16 .. 1] A '1' indicates that the FIFO is empty.

Digital I/O (Read/Write, PCIBar2 + 810CH)

The Digital I/O register provides access to the 16 digital I/O lines. Digital I/O lines are pulled high via a 4.75K Ohm resistor to +5 Volts. The levels of the digital I/O lines are returned upon a read to this address. The appropriate output enable bit must be '1' in the Digital I/O Direction register to enable writing to a digital output.

Table 3-7 Digital I/O 810CH

BIT	FUNCTION
31 - 16	unused
15 - 0	Digital I/O signals [15 .. 0]

Conversion Timer Register - (Read/Write, PCIBar2 + 8110H)

This read/write register controls the sample period of all A/D converters. Sample period = count * ADC Clock Period. Set count to zero to allow A/D converters to sample at their maximum rate of 500 KHz. For sample rates less than 500 KHz, enter a count > 2 µS/ADC Clock Period. This register must be written using a 32 bit write command. The minimum sample period is 2 µS. The maximum sample period is $(2^{32} - 1)$ * ADC Clock Period. The ADC Clock Period is 10.101 nS for host boards based on Xilinx Virtex 4 FPGA's. The ADC Clock Period is 8 nS for host boards based on Virtex 5 or Spartan 6.

Table 3-8 Conversion Timer 8110H

BIT	FUNCTION
31 – 0	Sample Period = register value * ADC Clock Period

FLASH Data Register - (Read/Write, PCIBar2 + 8114H)

A byte write to this address triggers a write/read serial transfer to/from the serial FLASH device. A byte read from this address returns the data read from a previous write/read serial transfer.

WARNING: Factory calibration data is stored in FLASH. Writing to FLASH could result in loss of factory calibration data. See **Error! eference source not found.**.

Table 3-9 FLASH Data Register 8114H

BIT	FUNCTION
31 - 8	unused
7 - 0	FLASH data

Digital I/O Direction Register - (Read/Write, PCIBar2 + 8118H)

The Digital I/O Direction provides an output enable for each of the 16 digital I/O lines. Write a '1' to a bit to enable the output.

Table 3-10 Digital I/O 8118CH

BIT	FUNCTION
31 - 16	unused
15 - 0	Digital I/O Direction [15 .. 0] 0 – input 1 – output

ADC Channels

There are three registers associated with each of the sixteen ADC channels: data, gain correction, and offset correction. The data register is a 16-bit read only register. Reading this register will retrieve the oldest value from the FIFO associated with that channel. Each of the ADC channels will apply a gain and offset correction to each sample prior to writing the result to a FIFO. The addition and multiplication operations are done in FPGA hardware using one of the FPGA's DSP blocks for each channel. The gain and offset registers are set to one and zero respectively upon reset to pass uncorrected ADC values to the FIFOs. Typical start-up operation would include reading factory calibration constants from AXM-A75 on-board FLASH memory and writing the appropriate correction values for the currently selected full scale range to the gain and offset registers for each channel.

ADC Data Format

The output from the ADC is offset binary format as shown in Table 3-11. The full scale range (±10.24, ±5.12, ±2.56, ±1.28) is controlled by the gain selection in the control register. See Table 3-4.

Table 3-11 ADC Data Format

DESCRIPTION	DIGITAL OUTPUT
+ Full Scale	FFFF
Midscale (zero)	8000
1 LSB Below Midscale	7FFF
- Full Scale	0000

ADC Offset Register

The offset register contains a 16 bit two's complement value that is added to the value output from the ADC to correct offset errors. There is a separate offset register for each channel.

ADC Gain Register

The gain register is a 17 bit fixed point positive fractional number ranging from 0 to 1.999984 weighted as shown in Table 3-12. The 17 bit fixed point number is least significant bit justified in a 32 bit register. This number is multiplied by the offset corrected ADC value to correct for gain errors. There is a separate gain register for each channel.

Table 3-12 Gain Register Number Format

BIT	Binary Fixed Point
31 - 17	(unused, read as 0)
16	1
15	1/2
14	1/4
13	1/8
12	1/16
11	1/32
10	1/64
9	1/128
8	1/256
7	1/1024
6	1/2048
5	1/4096
4	1/8192
3	1/16536
2	1/32768
1	1/65536
0	1/131072

Uncalibrated ADC Performance

The uncalibrated analog input channel performance is affected by four error sources. These are the instrumentation amplifier, difference amplifier, ADC reference and the ADC. Each of these

devices can contribute to the offset and gain error of the system. These errors can be corrected by calibration.

Analog Input Channel Calibration Procedure

Accurate calibration of the analog input channel digitized values can be accomplished by applying external precision calibration voltages.

The calibration voltages are used to find two points that determine the straight line characteristic of the analog channel.

Factory calibration constants are calculated using the following equations.

$$Gain = 1, 2, 4 \; or \; 8$$

$$FullScaleRange = \frac{20.48}{Gain}$$

$$IdealZero = \frac{-10.24}{Gain}$$

$$IdealSlope = \frac{2^{16}}{FullScaleRange}$$

$$ActualSlope = \frac{CountCALHI - CountCALLO}{VoltsCALHI - VoltsCALLO}$$

$$ActualIntercept = CountCALHI - ActualSlope * VoltsCALHI$$

$$Offset = IdealZero * AcualSlope + ActualIntercept$$

$$CorrectionFactor = \frac{IdealSlope}{ActualSlope}$$

$$OffsetCorrection = \; \|Offset\|$$

$$GainCorrection = \|CorrectionFactor * 2^{16}\|$$

The values calculated for OffsetCorrection and GainCorrection are stored in FLASH memory for each gain selection for each ADC channel. The values are then used in the following equation to correct each input sample for offset and gain errors.

$$CorrectedData = \frac{(CountIN + OffsetCorrection) * GainCorrection}{2^{16}}$$

Note: The average of many ADC values (e.g. 2048) should be used when calculating new correction coefficients to reduce the measurement uncertainty.

DAC Channels

There are four registers associated with each of the eight ADC channels: data, coarse gain correction, fine gain correction and offset correction. The data register is a 16-bit write/read register. Reading this register will retrieve the last value that was loaded into the DAC

register for that channel. Each of the D/A channels will apply a gain and offset correction to each output word. The addition and multiplication operations are done in each DAC device. The gain and offset registers are set to one and zero respectively upon reset to pass uncorrected DAC values to the outputs. Typical start-up operation would include reading factory calibration constants from AXM-A75 on-board FLASH memory and writing the appropriate correction values for the currently selected full scale range to the coarse gain, fine gain and offset registers for each channel.

DAC Data Register

The DAC data format is 16 bit offset binary. The ideal output from the DAC for some select output codes is shown in Table 3-13. The full scale range (FSR) is controlled by the coarse gain selection register for each channel (See Table 3-4). The FSR choices are ±10, ±10.2564 and ±10.5263 Volts.

Table 3-13 DAC Data Format

Volts	DIGITAL OUTPUT
+FSR * 32767/32768	FFFF
+FSR * 1/32767	8001
Midscale (zero)	8000
-FSR * 1/32767	7FFF
-FSR * 32767/32768	0000

DAC Coarse Gain Register

The coarse gain register is a two bit register that allows the selection of one of three Full Scale Ranges: ±10, ±10.2564 and ±10.5263 Volts as shown in Table 3-14. There is a separate coarse gain register for each channel.

Table 3-14 DAC Coarse Gain Selections

FSR Volts	Register Value
±10	0
±10.2564	1
±10.5263	2

DAC Fine Gain Register

The fine gain register is a six bit register that allows the user to adjust the gain of each DAC by −32 LSBs to +31 LSBs in 1 LSB steps, as shown in Table 3-15.

Table 3-15 DAC Fine Gain Selections

Gain Adjustment	FG5	FG4	FG3	FG2	FG1	FG0
+31 LSBs	0	1	1	1	1	1
+30 LSBs	0	1	1	1	1	0
No adjustment	0	0	0	0	0	0
-30 LSBs	1	0	0	0	0	1
-31 LSBs	1	0	0	0	0	0

DAC Offset Register

The offset register is an eight bit register that allows the user to adjust the offset of each DAC by −16 LSBs to +15.875 LSBs in steps of one-eighth LSB, as shown in Table 3-16.

Table 3-16 DAC Offset Correction

Gain Adjustment	OF7	OF6	OF5	OF4	OF3	OF2	OF1	OF0
+15.875 LSBs	0	1	1	1	1	1	1	1
+15.75 LSBs	0	1	1	1	1	1	1	0
No adjustment	0	0	0	0	0	0	0	0
-15.875 LSBs	1	0	0	0	0	0	0	1
-16 LSBs	1	0	0	0	0	0	0	0

Note: the LDAC bit in the control register must be written to trigger a transfer from the DAC data registers to the DAC offset register.

Updating DAC outputs

The values written to the DAC data registers are not immediately applied to the DAC outputs. The LDAC bit in the control register must be written to trigger a transfer from the DAC data registers to the DAC outputs (see Table 3-4). The transfer from the data register to DAC outputs occurs simultaneously for all DAC channels.

4.0 THEORY OF OPERATION

Field I/O Connections

The field I/O interface to the AXM-A75 is provided through connector P1 (refer to Table 2-1). **Field I/O signals are NON-ISOLATED.** This means that the field return and logic common have a direct electrical connection to each other. As such, care must be taken to avoid ground loops (see Section 2.0 for connection recommendations). Ignoring this effect may cause operation errors, and with extreme abuse, possible circuit damage.

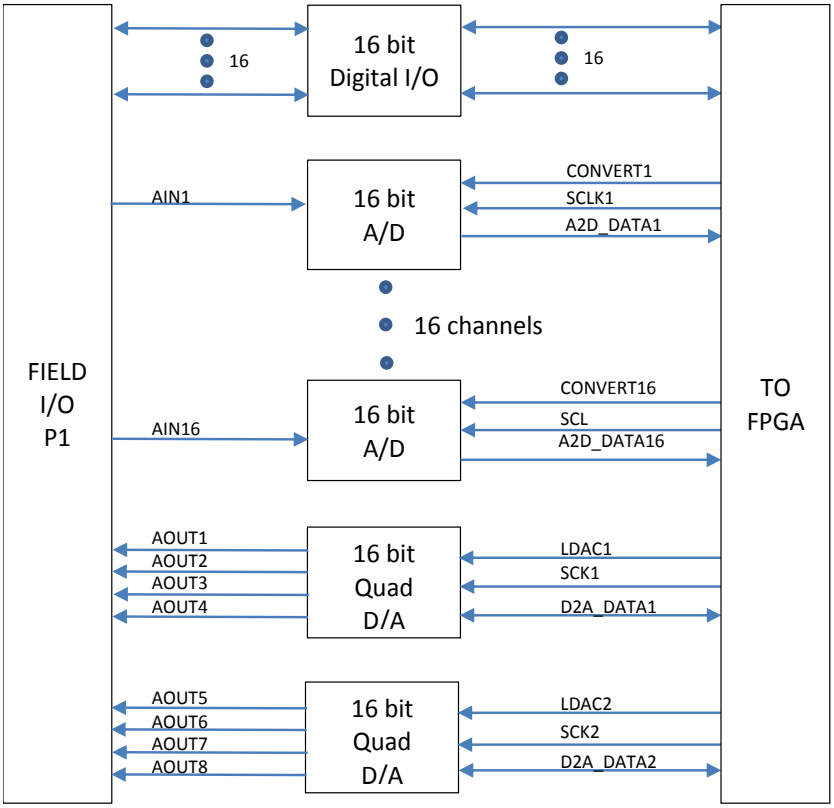


Figure 1 AXM-A75 Block Diagram

Digital I/O

A block diagram of a single digital I/O channel is shown in Figure 2 Digital I/O. This structure is replicated 16 times on the AXM-A75. The signal DIG_OUT_STROBE is activated upon a write to the Digital I/O register. The level of DIG_IO_n is returned upon a read of the Digital I/O register. The signal DIG_OUT_DIR_STROBE is activated upon a write to the Digital I/O Direction Register. When the DIG_OUT_DIR_n signal is logic high the contents of the DIG_OUT_n flip-flop will be driven onto the DIG_IO_n signal. The level translator is a NXP GTL2010.

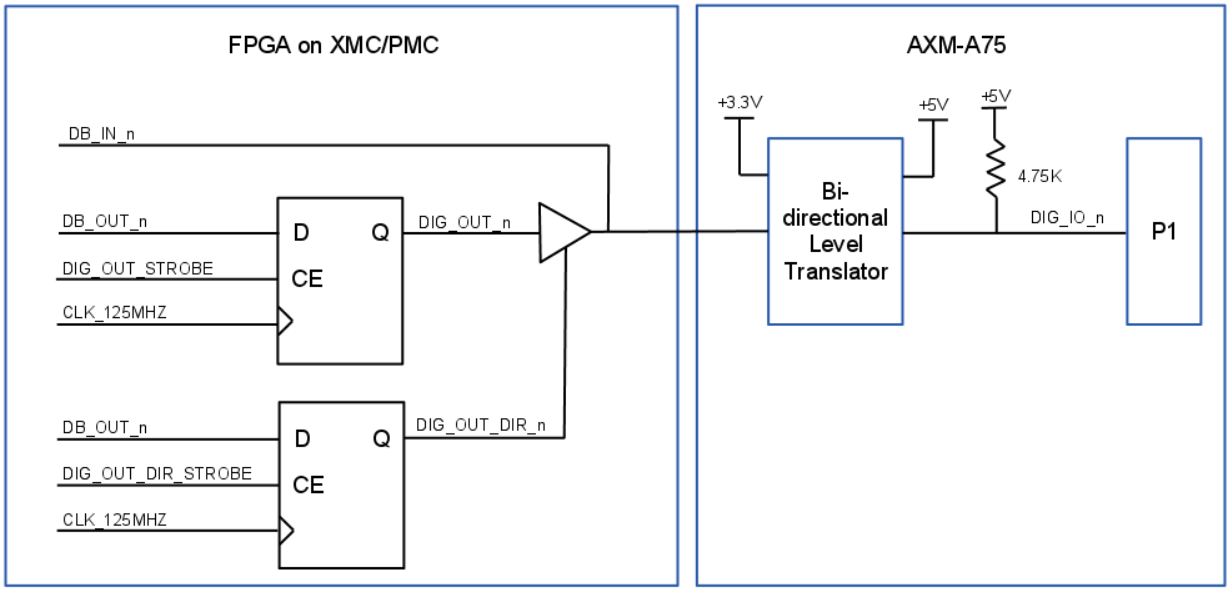


Figure 2 Digital I/O

Analog Outputs

Two Analog Devices AD5764R quad bipolar voltage output DACs are used to provide the eight analog output channels. Each DAC uses its own on-chip reference as its reference source. Although each DAC has separate clock, sync, load and serial I/O signals connected to the FPGA, the firmware as delivered with the EDK provides access to only a single quad DAC at a time. The CLR, BIN2SCOMP and RESET signals are common to both DACs.

Analog Inputs

Each of the analog input channels consists of a differential low pass filter followed by an instrumentation amplifier, a difference amplifier and an ADC.

The differential low pass RC filter is intended to reduce RF interference. The 3db cutoff frequency of the filter is 421 kHz differential, 8.84 MHz common mode.

An Analog Devices AD8251 Programmable Gain (Instrumentation) Amplifier (PGA) takes as input the channel's + and - inputs and outputs a single ended voltage proportional to it. The gain can be 1, 2, 4, or 8 and is selected through the gain selection bits in the control register. The gain selection affects all channels.

The output from the PGA is input to a Texas Instruments INA159 level translation difference amplifier that divides its input voltage by 5 and level shifts the output by one half of the 4.096 reference voltage. The output from the difference amplifier drives an Analog Devices AD7686 16 bit, 500 kSPS ADC. Each of the ADCs has separate clock, convert and serial data connections to the FPGA allowing synchronous acquisition and simultaneous data transfer.

5.0 SERVICE AND REPAIR

SERVICE AND REPAIR ASSISTANCE

Surface-Mounted Technology (SMT) boards are generally difficult to repair. It is highly recommended that a non-functioning board be returned to Acromag for repair. The board can be damaged unless special SMT repair and service tools are used. Further, Acromag has automated test equipment that thoroughly checks the performance of each board.

Please refer to Acromag's Service Policy Bulletin or contact Acromag for complete details on how to obtain parts and repair.

PRELIMINARY SERVICE PROCEDURE

Before beginning repair, be sure that all of the procedures in section 2.0 PREPARATION FOR USE have been followed. Replacement of a suspected faulty unit with one that is known to work correctly is a good technique to isolate a faulty board.

CAUTION: POWER MUST BE TURNED OFF BEFORE REMOVING OR INSERTING BOARDS

WHERE TO GET HELP

If you continue to have problems, your next step should be to visit the Acromag worldwide web site at http://www.acromag.com. Our web site contains the most up-to-date product and software information.

Go to the "Support" tab to access:

- Application Notes
- Frequently Asked Questions (FAQ's)

- Product Knowledge Base
- Tutorials
- Software Updates/Drivers

An email question can also be submitted from within the Knowledge Base or directly from the "Contact Us" tab.

Acromag's application engineers can also be contacted directly for technical assistance via telephone or FAX through the numbers listed below. When needed, complete repair services are also available.

Phone: 248-295-0310
Fax: 248-624-9234
Email: solutions@acromag.com

6.0 SPECIFICATIONS

Physical

Physical Configuration ..... Single AXM Module
Stacking Height ..... 5 mm
Length ..... 38.5 mm (1.516 inches)
Width ..... 73.75 mm (2.904 inches)
Board Thickness ..... 1.59 mm (0.062 inches)

Connectors

P1 (FPGA Interface)..... 162-pin receptacle, 5 mm stack height, high speed terminal strip (Samtec QTS-075-01-L-D-A-K)
J1 (Field I/O)..... 68-pin VHDCI receptacle (Amphenol HE11-RDA-101-3-C)

Environmental

Operating Temperature..... 0 to +70°C
Relative Humidity..... 5-95% non-condensing
Storage Temperature..... -55°C to +150°C
Non-Isolated..... Logic and field commons have a direct electrical connection
Radiated Field Immunity..... Designed to comply with IEC61000-4-3 class A
Surge Immunity..... Not required for signal I/O per European Norm EN61000-6-1
Electric Fast Transient Immunity
Designed to comply with IEC61000-4-4 class A
Radiated Emissions ..... Designed to comply with CISPR 16-2-3 class A
Electrostatic Discharge ..... Designed to comply with IEC6100-4-2 Level 2
Conducted Radio Frequency Interference
Designed to comply with IEC6100-4-6 class A

Power Requirements

+3.3 Volts (±5%) ..... 39 mA typical
50 mA maximum
+5 Volts (±5%) ..... 54 mA typical
65 mA maximum
+12V (±5%) ..... 103 mA typical
115 mA maximum
-12V (±5%) ..... 92 mA typical
115 mA maximum

ANALOG INPUTS

Device ..... ADI AD7686
Input Channels ..... 16 differential
Input Signal Type ..... Voltage (Non-isolated)
Input Ranges: ..... ±10.24, ±5.12, ±2.56 and ±1.28 V
Input Overvoltage Protection ..... ±31 V with power on
±19 V with power off
Input Resistance ..... 5.300 GΩ, typical differential
Input Bias Current ..... 5 nA typical
40 nA maximum
Common Mode Rejection Ratio ... 98 dB typical (60 Hz)
Input Channel to Input Channel Rejection Ratio[1]
41 dB typical (100 kHz)
Output Channel to Input Channel Rejection Ratio[2]
85 dB typical (1 kHz)
Accuracy .....

Gain	% Full Scale @ 25°C	% Full Scale 0 – 70°C
1	0.011	0.026
2	0.013	0.029
4	0.015	0.033
8	0.018	0.040

Programmable Gain Instrumentation Amplifier

Device ..... ADI AD8251
PGA Linearity Error ..... ±0.005% maximum (3.27 LSB)
Offset Error RTI[3] ..... ±1.0 mV typical, ±2.5 mV maximum
Offset vs. Temperature ..... ±(0.6 + 1.5/G) µV/°C typical (G=1,2,4,8)
±(1.2 + 5/G) µV/°C maximum
Gain Error (all gains)[3] ..... 0.01% typical, 0.1% maximum

[1] Input channel to input channel rejection ratio was measured with a 100 KHz 1V pk-pk sine wave input on an adjacent channel.
[2] The output channel to input channel rejection ratio was measured with all output channels driving a 10k ohm load outputting a 1 kHz 20 V pk-pk sine wave. Load resistors were located on a termination panel connected to a 2 meter cable.

Gain vs. Temperature..... 3 ppm/°C typical
10 pm/°C maximum

Difference Amplifier

Device..... TI INA159
Gain Error..... ±0.005% typical
±0.024% maximum
Gain Error vs. Temperature ..... ±1 ppm/°C typical
Offset Error ..... ±100 µV typical
±500 µV maximum
Offset Voltage vs. Temperature.... ±1.5 µV/°C typical
Reference Divider Accuracy ..... ±0.002% typical
±0.024% maximum

Voltage Reference REF3240

Device..... TI REF3240
Accuracy..... 0.01% typical
±0.2% maximum
Output Voltage Temperature Drift 4 ppm/°C typical
7 ppm/°C maximum
Thermal Hysteresis[4] ..... 100 ppm first cycle
25 ppm additional cycles
Noise ..... 78 µV RMS typical

Analog to Digital Converter

ADC..... ADI AD7686
A/D Resolution..... 16-bits
Data Format ..... straight binary
No Missing Codes..... no missing codes 15-bits
A/D Integral Linearity Error..... ±0.6 LSB typical
±2 LSB maximum
Offset Error ..... ±0.1 mV typical ±10 V range
±1.6 mV maximum
Gain Error Temperature Drift ..... ±0.3 ppm/°C typical
Offset Temperature Drift..... ±0.3 ppm/°C typical
Full Scale Error ..... ±0.5% maximum
A/D Conversion Time ..... 2 µS maximum
Conversion Rate..... 500 kHz maximum
Input Noise..... 2 LSB rms typical

[3] Software calibration eliminates these error components
[4] Acromag does not temperature cycle this product before shipping to customers. If the product is operated at the extremes of its temperature range, the voltage reference could drift by the amount specified for first cycle.

ANALOG OUTPUTS

Digital to Analog Converter

Device..... ADI AD5764RB
Resolution ..... 16 bits
Output Ranges ..... ±10, ±10.2564, and ±10.5263 V
Settling Time ..... 8 µS typical full-scale step to ±1 LSB
10 µS maximum
Slew Rate..... 5 V/µS typical
Integral Nonlinearity ..... ±2 LSB maximum
Differential Nonlinearity ..... ±1 LSB maximum
Bipolar Zero Error..... ±2 mV maximum
Internal Reference ..... 4.995 V minimum
5.005 V maximum
Short Circuit Current ..... 10 mA typical
Load Current ..... ±1 mA maximum for specified performance
Capacitive Load Stability ..... 200 pF maximum with $R_{LOAD}=\infty$
1000 pF maximum with R_{LOAD}=10K Ω
DC Output Impedance ..... 0.3 Ω maximum
Gain Drift..... ±2 ppm full scale range/°C
Bipolar Zero Drift ..... ±2 ppm full scale range/°C
Accuracy..... 0.015 % full scale @ 25°C
0.029 % full scale @ 0 – 70°C

7.0 APPENDIX

CABLE: MODEL 5028-420 (Ultra SCSI/VHDCI male to SCSI-3 male, Round, Shielded)

Type: Round shielded cable, 34-wire pairs (Ultra SCSI/VHDCI male and SCSI-3 male connectors). The cable length is 2 meters (6.56 feet). This shielded cable is recommended for all I/O applications (both digital I/O and precision analog I/O).

Application: Used to connect Model 5025-288 termination panel to the board.

Length: 2 meters (6.56 feet)

Cable: 34 wire pairs, 28 AWG, foil/braided shield inside a PVC jacket.

Connectors: Ultra SCSI/VHDCI and SCSI-3, 68-pin male connectors with backshell. Keying: The connectors have a "D Shell".

Schematic and Physical Attributes: See Drawing 4502-153.

Electrical Specifications: 30 VAC per UL and CSA (SCSI-3 connector spec.'s). 1 Amp maximum at 50% energized (SCSI-3 connector spec.'s).

Operating Temperature: -30°C to +80°C.

Storage Temperature: -40°C to +85°C.

Shipping Weight: 1.0 pound (0.5Kg), packed.

TERMINATION PANEL: MODEL 5025-288

Type: Termination Panel for 68 Pin SCSI-3 Cable Connection

Application: To connect field I/O signals to the board.

Termination Panel: Acromag Part 4001-066. The 5025-288 termination panel facilitates the connection of up to 68 field I/O signals and connects to the board (connectors only) via a round shielded cable (Model 5028-432). Field signals are accessed via screw terminal strips. The terminal strip markings on the termination panel (1-68) correspond to field I/O (pins 1-68) on the board. Each board has its own unique pin assignments. Refer to the board manual for correct wiring connections to the termination panel.
Schematic and Physical Attributes: See Drawing 4501-920.

Field Wiring: 68-position terminal blocks with screw clamps. Wire range 12 to 26 AWG.

Mounting: Termination panel is snapped on the DIN mounting rail.

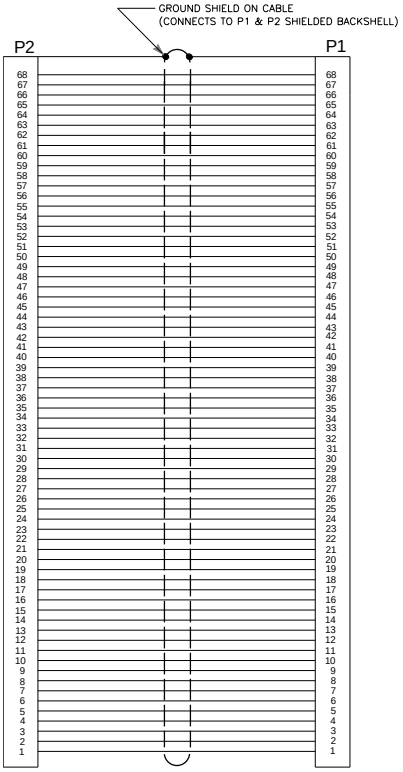
Printed Circuit Board: Military grade FR-4 epoxy glass circuit board, 0.063 inches thick.

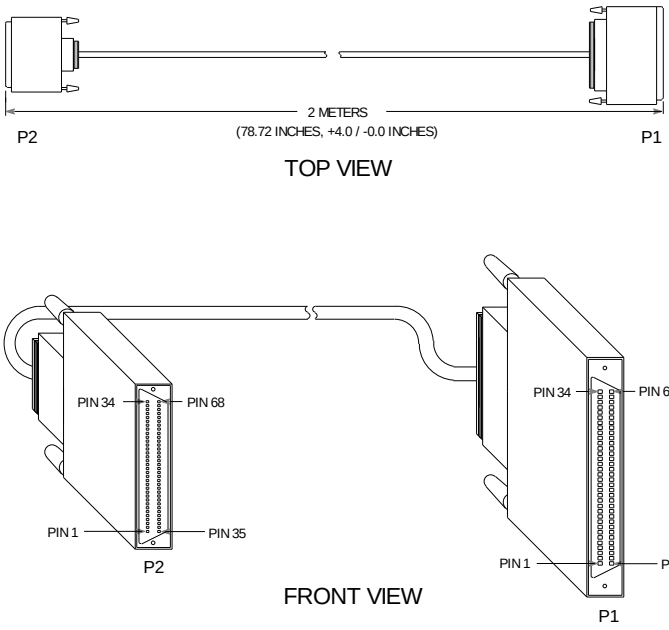
Operating Temperature: -40°C to +100°C

Storage Temperature: -40°C to +100°C.

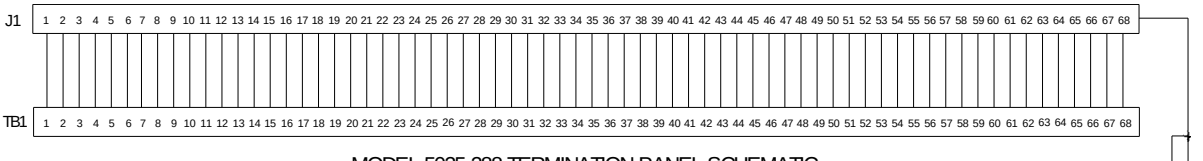
Shipping Weight: 1.0 pounds (0.5kg) packaged.

8.0 DRAWINGS

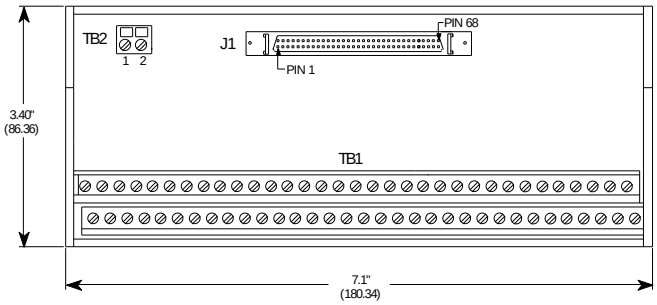


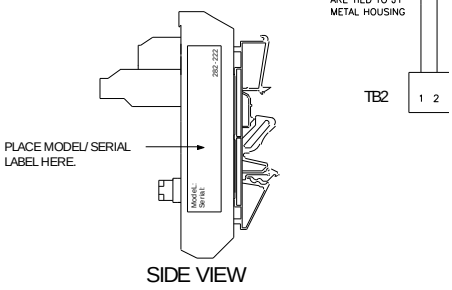


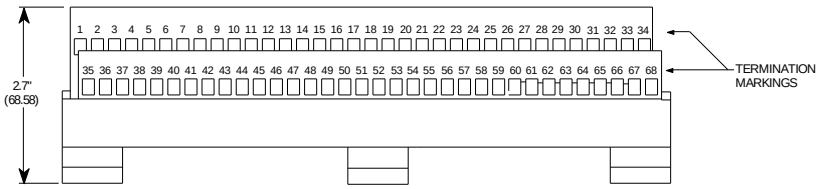
MODEL 5028-420 ULTRA SCSI/VHDCI TO
SCSI-3 68 PIN CABLE ASSEMBLY, SHIELDED 4502-153A



MODEL 5025-288 TERMINATION PANEL SCHEMATIC







NOTE:
DIMENSIONS ARE IN INCHES.
(MILLIMETERS)

4501-920