TB-FMCH-12GSDI
Hardware User Manual

Rev.1.00

Revision History

Version	Date	Description	Publisher
Rev.1.00	2015/03/17	Initial release	Curnow

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Introduction

Thank you for purchasing the **TB-FMCH-12GSDI** board. Before using the product, be sure to carefully read this user manual and fully understand how to correctly use the product. First read through this manual, and then always keep it handy.

SAFETY PRECAUTIONS

Be sure to observe these precautions!

Observe the precautions listed below to prevent injuries to you or other personnel or damage to property.

- **Before using the product, read these safety precautions carefully to assure correct use.**
- **These precautions contain serious safety instructions that must be observed.**
- **After reading through this manual, be sure to always keep it handy.**

The following conventions are used to indicate the possibility of injury/damage and classify precautions if the product is handled incorrectly.

Danger	Indicates the high possibility of serious injury or death if the product is handled incorrectly.
Warning	Indicates the possibility of serious injury or death if the product is handled incorrectly.
Caution	Indicates the possibility of injury or physical damage in connection with houses or household goods if the product is handled incorrectly.

The following graphical symbols are used to indicate and classify precautions in this manual.
(Examples)

	Turn off the power switch.
	Do not disassemble the product.
	Do not attempt this.

Warning	
	**In the event of a failure, disconnect the power supply.** If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately and contact our sales personnel for repair.
	**If an unpleasant smell or smoking occurs, disconnect the power supply.** If the product is used as is, a fire or electric shock may occur. Disconnect the power supply immediately. After verifying that there is no smoking, contact our sales personnel for repair.
	**Do not disassemble, repair or modify the product.** Otherwise, a fire or electric shock may occur due to a short circuit or heat generation. For inspection, modification or repair, contact our sales personnel.
	**Do not touch a cooling fan.** As a cooling fan rotates at high speed, do not put your hand close to it. Otherwise, it may cause injury to persons. Never touch a rotating cooling fan.
	**Do not place the product on unstable locations.** Otherwise, it may drop or fall, resulting in injury to persons or failure.
	**If the product is dropped or damaged, do not use it as is.** Otherwise, a fire or electric shock may occur.
	**Do not touch the product with a metallic object.** Otherwise, a fire or electric shock may occur.
	**Do not place the product in dusty or humid locations or where water may splash.** Otherwise, a fire or electric shock may occur.
	**Do not get the product wet or touch it with a wet hand.** Otherwise, the product may break down or it may cause a fire, smoking or electric shock.
	**Do not touch a connector on the product (gold-plated portion).** Otherwise, the surface of a connector may be contaminated with sweat or skin oil, resulting in contact failure of a connector or it may cause a malfunction, fire or electric shock due to static electricity.

Caution	
	Do not use or place the product in the following locations. • Humid and dusty locations • Airless locations such as closet or bookshelf • Locations which receive oily smoke or steam • Locations exposed to direct sunlight • Locations close to heating equipment • Closed inside of a car where the temperature becomes high • Static-prone locations • Locations close to water or chemicals Otherwise, a fire, electric shock, accident or deformation may occur due to a short circuit or heat generation.
	Do not place heavy things on the product. Otherwise, the product may be damaged.

■ Disclaimer

This product is an SDI interface for Xilinx FPGA evaluation boards. Tokyo Electron Device Limited assumes no responsibility for any damages resulting from the use of this product for purposes other than those stated.

Even if the product is used properly, Tokyo Electron Device Limited assumes no responsibility for any damages caused by:

(1) Earthquake, thunder, natural disaster or fire resulting from the use beyond our responsibility, acts by a third party or other accidents, the customer's willful or accidental misuse, or use under other abnormal conditions.
(2) Secondary impact arising from use of this product or its unusable state (business interruption or others)
(3) Use of this product against the instructions given in this manual.
(4) Malfunctions due to connection to other devices.

Tokyo Electron Device Limited assumes no responsibility or liability for:

(1) Erasure or corruption of data arising from use of this product.
(2) Any consequences or other abnormalities arising from use of this product, or
(3) Damage of this product not due to our responsibility or failure due to modification.

This product has been developed by assuming its use for research, testing or evaluation. It is not authorized for use in any system or application that requires high reliability.
Repair of this product is carried out by replacing it on a chargeable basis, not repairing the faulty devices. However, non-chargeable replacement is offered for initial failure if such notification is received within two weeks after delivery of the product.
The specification of this product is subject to change without prior notice.
The product is subject to discontinuation without prior notice.

1. Related Documents and Accessories

All documents relating to this board can be downloaded from the TED Support Web at address
http://ppg.teldevice.co.jp/eng/index.htm

Board accessories:

- HDBNC-BNC Cable Belden 1694A 12cm x2
- FMC spacer set
  - AS-2610 x2
  - AS-2625 x2
  - B-2606-S1N x6
  - BS-2610E x4

2. Overview

The TB-FMCH-12GSDI FMC has a dedicated SDI input, a dedicated SDI output, and three SDI channels that are either input or output. Each SDI channel supports a data rate up to 11.88 Gbps. It also has a video sync input for a video sync separator chip. All video signal connections are via 75 ohm HDBNC jacks. A video clock generator can also produce common video timing signals from oscillators or from HVF sync signals from the host FPGA.

The TB-FMCH-12GSDI uses Samtec's FMC HPC connector for connection with a platform board having High-Pin Count connectors. It is a single width air-cooled FMC that is compatible with the ANSI/VITA 57.1 FPGA Mezzanine Card (FMC) Standard. A second FMC HPC connector allows a second TB-FMCH-12GSDI to be stacked to double the number of SDI inputs and outputs.

Note: Even if your target carrier card supports a single TB-FMCH-12GSDI, there is no guarantee that stacking will be supported (typically due to limited gigabit transceiver connectivity). If stacking is a critical feature for you, please contact your sales representative to confirm operation prior to ordering/stacking.

The TB-FMCH-12GSDI supports SD/HD/3G/6G/12G SDI rates to enable next generation UHDTV 4k/60fps video over a single coaxial cable.

3. Features

SDI Video Reclocker	MACOM M23145G
SDI Cable Driver	MACOM M23428G
SDI Cable Equalizer/Reclocker	MACOM M23554G
FMC Main Connector	Samtec ASP-134488-01
FMC Extender Connector	Samtec ASP-134486-01
SDI Connectors	Samtec HDBNC-J-P-GN-RA-BH2
FPGA GPIO Signal Level	1.2V through 3.3V using voltage level translators or AC coupling
Video Sync Separator	Texas Instruments LMH1981
Video Clock Generator	Texas Instruments LMH1983

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND
2	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_BIDIR_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_BIDIR_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Figure 3-1 FMC HPC Connector Pin Layout from VITA 57.1

4. Block Diagram

Figure 4-1 shows the TB-FMCH-12GSDI block diagram.
The FMC-HPC main connector is mounted on the component side of the board.
The FMC-HPC extender connector is mounted coincident with the main connector on the opposite side of the board. Voltage level translators are not shown in the block diagram.

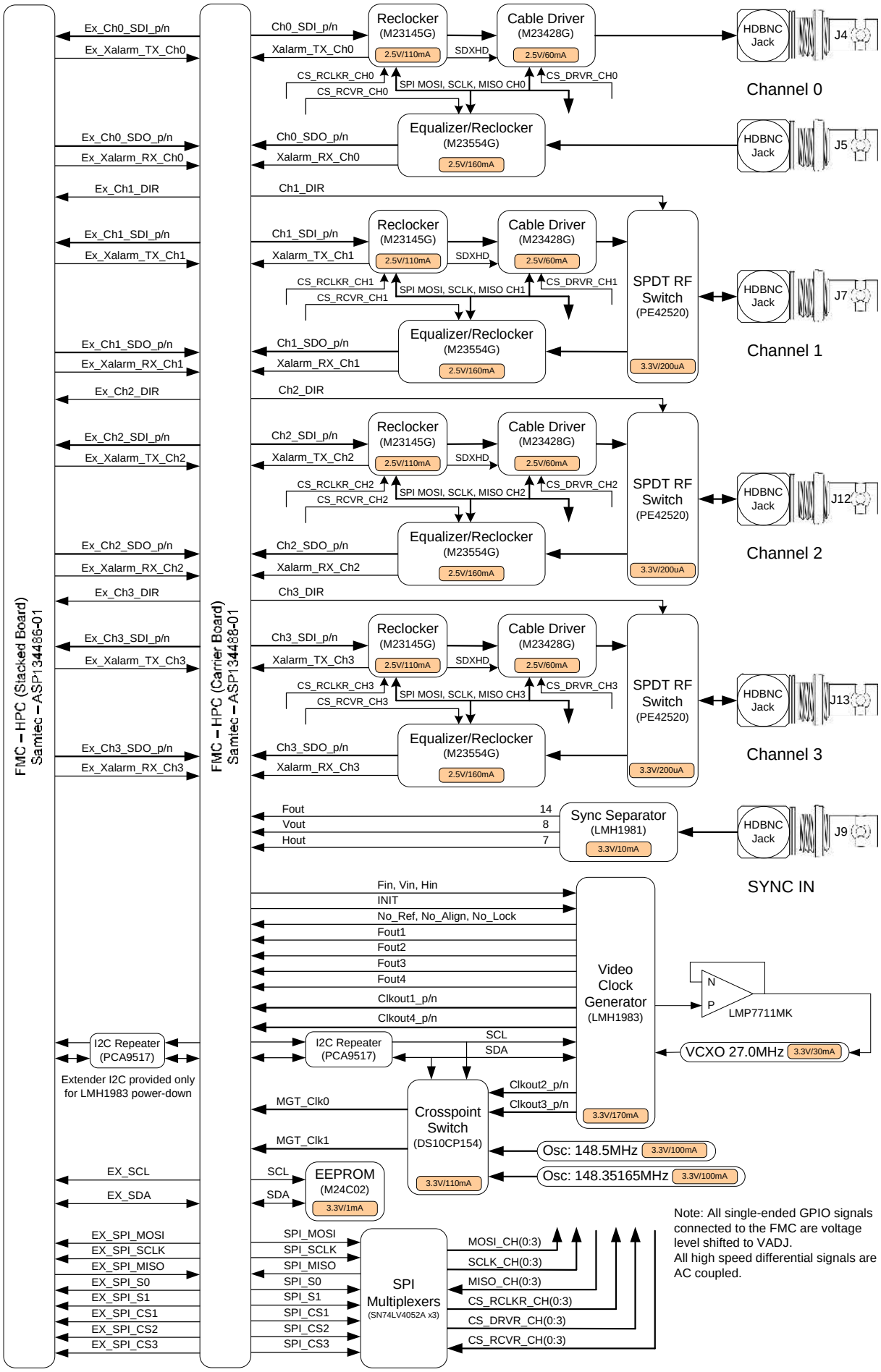

Figure 4-1 TB-FMCH-12GSDI Block Diagram

5. External View of the Board

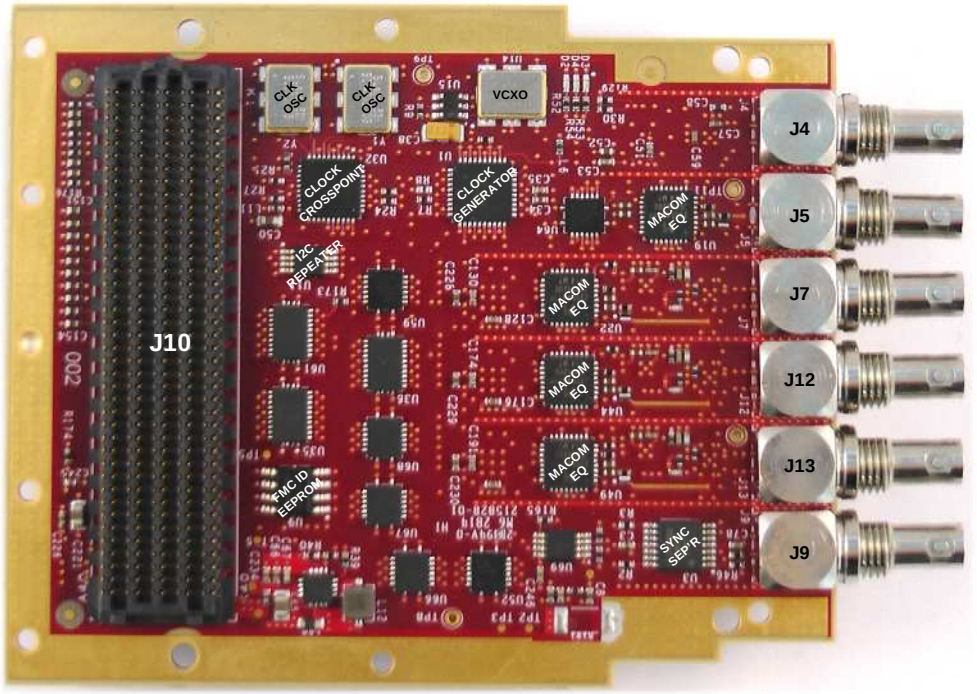

Figure 5-1 External View of TB-FMCH-12GSDI (Component Side)

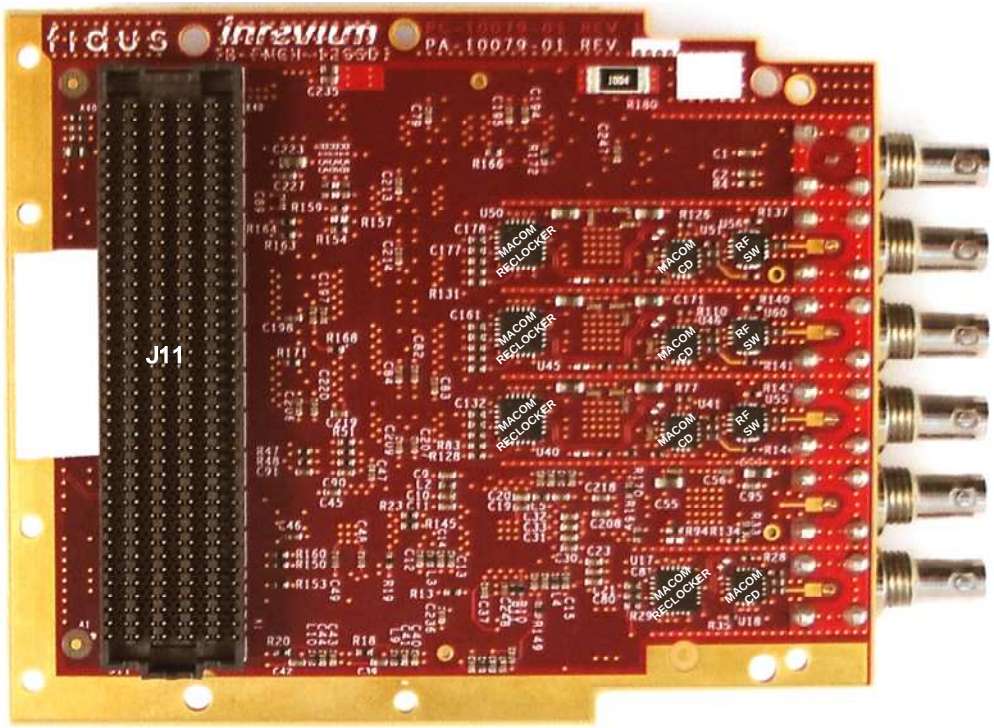

Figure 5-2 External View of TB-FMCH-12GSDI (Solder Side)

6. Board Specification

The following shows the TB-FMCH-12GSDI board physical specifications.

External Dimensions	84.00 mm long x 69.00 mm wide
Number of Layers	16 layers
Board Thickness	1.6 mm
Material	Megtron 6
SDI Connectors	Samtec HDBNC-J-P-GN-RA-BH2
FMC Main Connector	Samtec ASP-134488-01
FMC Extender Connector	Samtec ASP-134486-01

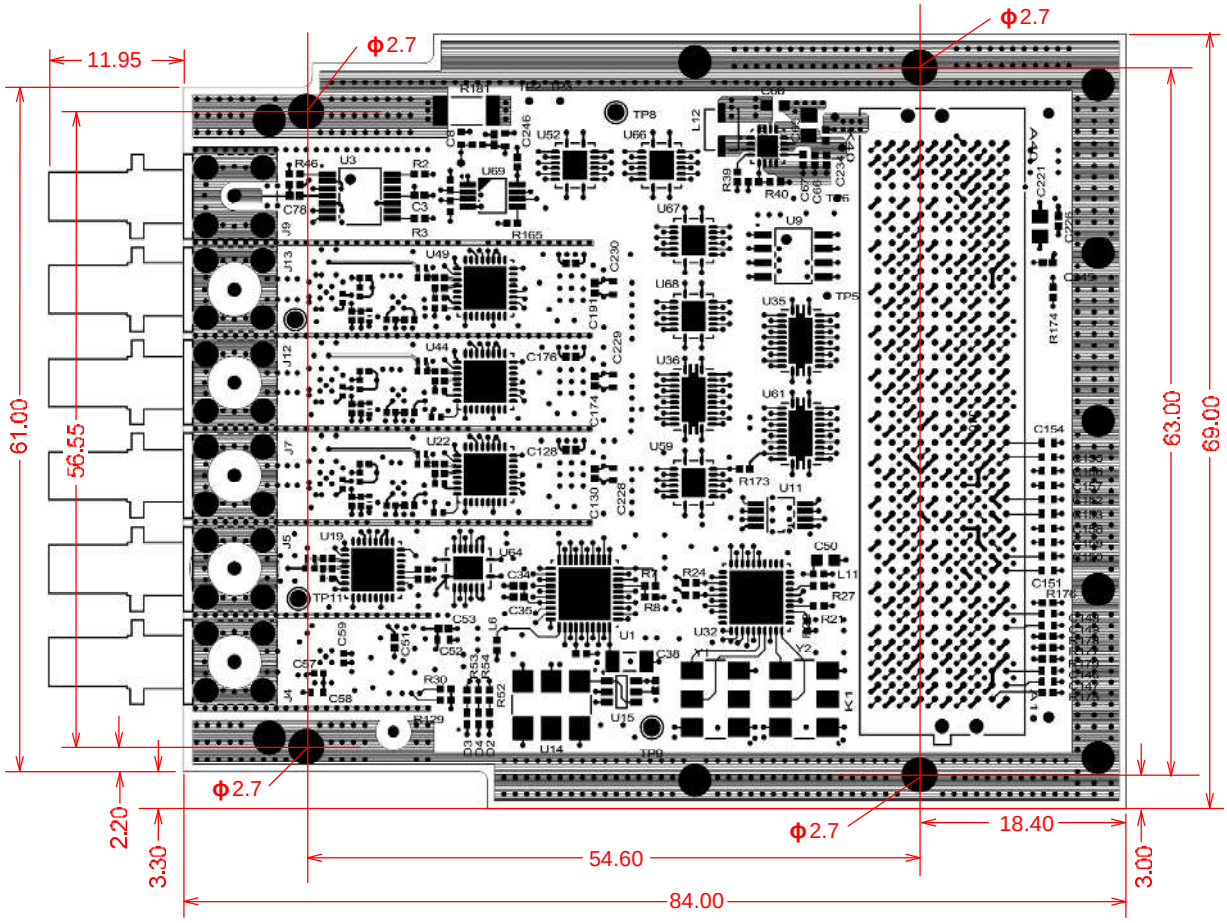

Figure 6-1 TB-FMCH-12GSDI Board Dimensions (mm)

7. Supplying Power to the Board

The power structure of the TB-FMCH-12GSDI is relatively simple. The total power dissipation is under 5 watts. There is one switching power regulator (TPS62130) to produce 2.5 volts from the 12 volt FMC rail (12P0V). The MACOM ICs and the SPI multiplexers use only the 2.5 volt rail. All the other ICs, except for the voltage translators and the I2C repeaters, use the FMC 3.3 volt rail (3P3V). The voltage translators and I2C repeaters use the FMC VADJ voltage, which can be range between 1.2 volts to 3.3 volts. The FMC 3P3VAUX voltage is used only by the FMC EEPROM and a single I2C repeater.

The current draw from the 12P0V voltage is less than 300 mA. The current draw from the 3P3V rail is about 500 mA, worst case. There is no over-current or over-voltage protection on the 3P3V or 12P0V rails, although both are LC filtered.

8. Connectors

There are a total of eight connectors on the FMC. One HPC FMC connector is for the main board (J10) and another HPC FMC connector (J11) is for a second TB-FMCH-12GSDI, to provide double the SDI channels, if required. The six HDBNC SDI channel connector are located in a row on the front edge of the card.

Note: Only stack FMCs that are identical (i.e. same part number and same revision). Do not attempt to stack different FMCs. Stacking FMCs of different types or revisions could cause damage.

8.1. HPC FMC Connector to Main Board

The FMC connector (High-Pin Count) connecting to the main board uses Samtec ASP-134488-01.
Table 8-1 shows the FMC connector pin assignment. In this table the C2M direction means carrier-to-mezzanine, which is an input to the FMC. The M2C direction means mezzanine-to-carrier, which is an output from the FMC. ‘BI-DIR’ means bi-directional, so the signal direction could be either an input or an output. Pins not included in the table are unconnected, including all HA[0:23] and HB[0:21] signals.

Table 8-1 HPC FMC Main Board Connector Pin Assignment

J10 Pin	Schematic Signal Name	VITA 57.1 Name	FMC Direction	Type	Description
SDI Differential Pairs					
C2	CH0_SDI_P	DP0_C2M_P	In	LVDS	Channel 0 Output
C3	CH0_SDI_N	DP0_C2M_N			
A22	CH1_SDI_P	DP1_C2M_P	In	LVDS	Channel 1 Output
A23	CH1_SDI_N	DP1_C2M_N			
A26	CH2_SDI_P	DP2_C2M_P	In	LVDS	Channel 2 Output
A27	CH2_SDI_N	DP2_C2M_N			
A30	CH3_SDI_P	DP3_C2M_P	In	LVDS	Channel 3 Output
A31	CH3_SDI_N	DP3_C2M_N			
C6	CH0_SDO_P	DP0_M2C_P	Out	LVDS	Channel 0 Input
C7	CH0_SDO_N	DP0_M2C_N			
A2	CH1_SDO_P	DP1_M2C_P	Out	LVDS	Channel 1 Input
A3	CH1_SDO_N	DP1_M2C_N			
A6	CH2_SDO_P	DP2_M2C_P	Out	LVDS	Channel 2 Input
A7	CH2_SDO_N	DP2_M2C_N			
A10	CH3_SDO_P	DP3_M2C_P	Out	LVDS	Channel 3 Input
A11	CH3_SDO_N	DP3_M2C_N			
SPI and I2C Signals					
D17	F_SPI_MOSI	LA13_P	In	LVCMOS (VADJ)	SPI MOSI
D18	F_SPI_MISO	LA13_N	Out	LVCMOS (VADJ)	SPI MISO
D20	F_SPI_SCLK	LA17_CC_P	In	LVCMOS (VADJ)	SPI SCLK
D11	F_SPI_S0	LA05_P	In	LVCMOS (VADJ)	SPI Mux Select 0
D9	F_SPI_S1	LA01_CC_N	In	LVCMOS (VADJ)	SPI Mux Select 1
D15	F_SPI_CS1	LA09_N	In	LVCMOS (VADJ)	SPI Chip Select for M23145G
D14	F_SPI_CS2	LA09_P	In	LVCMOS (VADJ)	SPI Chip Select for M23428G
D12	F_SPI_CS3	LA05_N	In	LVCMOS (VADJ)	SPI Chip Select for M23554G
H13	F_CTL_I2C_SCL	LA07_P	In	LVCMOS OD (VADJ)	Control I2C Clock
H14	F_CTL_I2C_SDA	LA07_N	BI-DIR	LVCMOS OD (VADJ)	Control I2C Data
C30	none	SCL	In	LVCMOS	FMC ID EEPROM I2C Clock
C31	none	SDA	BI-DIR	LVCMOS	FMC ID EEPROM I2C Data

J10 Pin	Schematic Signal Name	VITA 57.1 Name	FMC Direction	Type	Description
Video Clocks					
H4	F_CLKOUT1_P	CLK0_M2C_P	Out	LVDS	LMH1983 CLKOUT1
H5	F_CLKOUT1_N	CLK0_M2C_N			
G2	F_CLKOUT4_P	CLK1_M2C_P	Out	LVDS	LMH1983 CLKOUT4
G3	F_CLKOUT4_N	CLK1_M2C_N			
D4	F_CLKOUT2_P	GBTCLK0_M2C_P	Out	LVDS	DS10CP154A OUT0
D5	F_CLKOUT2_N	GBTCLK0_M2C_N			
B20	F_CLKOUT3_P	GBTCLK1_M2C_P	Out	LVDS	DS10CP154A OUT1
B21	F_CLKOUT3_N	GBTCLK1_M2C_N			
G15	F_FOUT	LA12_P	Out	LVCMOS (VADJ)	LMH1981 OEOUT
G12	F_VOUT	LA08_P	Out	LVCMOS (VADJ)	LMH1981 VSOUT
G13	F_HOUT	LA08_N	Out	LVCMOS (VADJ)	LMH1981 HSOUT
G21	F_FIN	LA20_P	In	LVCMOS (VADJ)	LMH1983 FIN
G18	F_VIN	LA16_P	In	LVCMOS (VADJ)	LMH1983 VIN
G19	F_HIN	LA16_N	In	LVCMOS (VADJ)	LMH1983 HIN
G9	F_FOUT1	LA03_P	Out	LVCMOS (VADJ)	LMH1983 FOUT1
G6	F_FOUT2	LA00_CC_P	Out	LVCMOS (VADJ)	LMH1983 FOUT2
G7	F_FOUT3	LA00_CC_N	Out	LVCMOS (VADJ)	LMH1983 FOUT3
G10	F_FOUT4	LA03_N	Out	LVCMOS (VADJ)	LMH1983 FOUT4
Control and Miscellaneous Signals					
C10	F_XALARM_TX_CH0	LA06_P	Out	LVCMOS (VADJ)	CH 0, M23145G xALARM
C11	F_XALARM_TX_CH1	LA06_N	Out	LVCMOS (VADJ)	CH 1, M23145G xALARM
C14	F_XALARM_TX_CH2	LA10_P	Out	LVCMOS (VADJ)	CH 2 M23145G xALARM
C15	F_XALARM_TX_CH3	LA10_N	Out	LVCMOS (VADJ)	CH, 3 M23145G xALARM
H16	F_XALARM_RX_CH0	LA11_P	Out	LVCMOS (VADJ)	CH 0, M23554G xALARM
H17	F_XALARM_RX_CH1	LA11_N	Out	LVCMOS (VADJ)	CH 1, M23554G xALARM
H19	F_XALARM_RX_CH2	LA15_P	Out	LVCMOS (VADJ)	CH 2, M23554G xALARM
H20	F_XALARM_RX_CH3	LA15_N	Out	LVCMOS (VADJ)	CH 3, M23554G xALARM
G30	F_CH1_DIR	LA29_P	In	LVCMOS (VADJ)	CH 1, PE42520 CTRL
G33	F_CH2_DIR	LA31_P	In	LVCMOS (VADJ)	CH 2, PE42520 CTRL
C18	F_CH3_DIR	LA14_P	In	LVCMOS (VADJ)	CH 3, PE42520 CTRL

J10 Pin	Schematic Signal Name	VITA 57.1 Name	FMC Direction	Type	Description
G16	F_INIT	LA12_N	In	LVCMOS (VADJ)	LMH1983 INIT
H7	F_NO_REF	LA02_P	Out	LVCMOS (VADJ)	LMH1983 NO_REF
H8	F_NO_ALIGN	LA02_N	Out	LVCMOS (VADJ)	LMH1983 NO_ALIGN
H10	F_NO_LOCK	LA04_P	Out	LVCMOS (VADJ)	LMH1983 NO_LOCK
H1	Not connected	VREF_A_M2C	Out		
K1	Not connected	VREF_B_M2C	Out		
D1	Not connected	PG_C2M	In		Not used
F1	10k to VCC_3V3	PG_M2C	Out		Not used
H2	0 ohm to GND	PRSNT_M2C_N	Out	GND	
D29	Not connected	TCK	In		
D30	0 ohm to TDO	TDI	In		JTAG Bypassed
D31	0 ohm to TDI	TDO	Out		JTAG Bypassed
D33	Not connected	TMS	In		
D34	Not connected	TRST_N	In		
C34	GA0	GA0	In	LVCMOS	ID EEPROM E1
D35	GA1	GA1	In	LVCMOS	ID EEPROM E0
J39	Not connected	VIO_B_M2C	Out		
K40	Not connected	VIO_B_M2C	Out		

J10 Pin	Schematic Signal Name	VITA 57.1 Name	FMC Direction	Type	Description
Extender SDI Differential Pairs					
A34	EX_CH0_SDI_P	DP4_C2M_P	In	LVDS	Channel 0 Output
A35	EX_CH0_SDI_N	DP4_C2M_N			
A38	EX_CH1_SDI_P	DP5_C2M_P	In	LVDS	Channel 1 Output
A39	EX_CH1_SDI_N	DP5_C2M_N			
B36	EX_CH2_SDI_P	DP6_C2M_P	In	LVDS	Channel 2 Output
B37	EX_CH2_SDI_N	DP6_C2M_N			
B32	EX_CH3_SDI_P	DP7_C2M_P	In	LVDS	Channel 3 Output
B33	EX_CH3_SDI_N	DP7_C2M_N			
A14	EX_CH0_SDO_P	DP4_M2C_P	Out	LVDS	Channel 0 Input
A15	EX_CH0_SDO_N	DP4_M2C_N			
A18	EX_CH1_SDO_P	DP5_M2C_P	Out	LVDS	Channel 1 Input
A19	EX_CH1_SDO_N	DP5_M2C_N			
B16	EX_CH2_SDO_P	DP6_M2C_P	Out	LVDS	Channel 2 Input
B17	EX_CH2_SDO_N	DP6_M2C_N			
B12	EX_CH3_SDO_P	DP7_M2C_P	Out	LVDS	Channel 3 Input
B13	EX_CH3_SDO_N	DP7_M2C_N			
Extender SPI and I2C Signals					
H31	EX_SPI_MOSI	LA28_P	In	LVCMOS (VADJ)	SPI MOSI
H32	EX_SPI_MISO	LA28_N	Out	LVCMOS (VADJ)	SPI MISO
H34	EX_SPI_SCLK	LA30_P	In	LVCMOS (VADJ)	SPI SCLK
H25	EX_SPI_S0	LA21_P	In	LVCMOS (VADJ)	SPI Mux Select 0
H23	EX_SPI_S1	LA19_N	In	LVCMOS (VADJ)	SPI Mux Select 1
H29	EX_SPI_CS1	LA24_N	In	LVCMOS (VADJ)	SPI Chip Select for M23145G
H28	EX_SPI_CS2	LA24_P	In	LVCMOS (VADJ)	SPI Chip Select for M23428G
H26	EX_SPI_CS3	LA21_N	In	LVCMOS (VADJ)	SPI Chip Select for M23554G
C26	EX_CTL_I2C_SCL	LA27_P	In	LVCMOS OD (VADJ)	Control I2C Clock
C27	EX_CTL_I2C_SDA	LA27_N	BI-DIR	LVCMOS OD (VADJ)	Control I2C Data
C22	EX_SCL	LA18_CC_P	In	LVCMOS OD (VADJ)	FMC ID EEPROM I2C Clock
C23	EX_SDA	LA18_CC_N	BI-DIR	LVCMOS OD (VADJ)	FMC ID EEPROM I2C Data

J10 Pin	Schematic Signal Name	VITA 57.1 Name	FMC Direction	Type	Description
Extender Control and Miscellaneous Signals					
G24	EX_XALARM_TX_CH0	LA22_P	Out	LVCMOS (VADJ)	CH 0, M23145G ALARM
G25	EX_XALARM_TX_CH1	LA22_N	Out	LVCMOS (VADJ)	CH1, M23145G xALARM
G27	EX_XALARM_TX_CH2	LA25_P	Out	LVCMOS (VADJ)	CH 2, M23145G xALARM
G28	EX_XALARM_TX_CH3	LA25_N	Out	LVCMOS (VADJ)	CH 3, M23145G xALARM
D23	EX_XALARM_RX_CH0	LA23_P	Out	LVCMOS (VADJ)	CH 0, M23554G xALARM
D24	EX_XALARM_RX_CH1	LA23_N	Out	LVCMOS (VADJ)	CH 1, M23554G xALARM
D26	EX_XALARM_RX_CH2	LA26_P	Out	LVCMOS (VADJ)	CH 2, M23554G xALARM
D27	EX_XALARM_RX_CH3	LA26_N	Out	LVCMOS (VADJ)	CH 3, M23554G xALARM
G31	EX_CH1_DIR	LA29_N	In	LVCMOS (VADJ)	CH, 1 PE42520 CTRL
G34	EX_CH2_DIR	LA31_N	In	LVCMOS (VADJ)	CH, 2 PE42520 CTRL
C19	EX_CH3_DIR	LA14_N	In	LVCMOS (VADJ)	CH 3, PE42520 CTRL
H22	EX_PRSNT	LA19_P	Out	LVCMOS	Extender Present
H1	Not connected	VREF_A_M2C	Out		
K1	Not connected	VREF_B_M2C	Out		
D1	Not connected	PG_C2M	In		Not used
F1	Not connected	PG_M2C	Out		
H2	EX_PRSNT	PRSNT_M2C_N	Out	LVCMOS	
D29	Not connected	TCK	In		
D30	Not connected	TDI	In		
D31	Not connected	TDO	Out		
D33	Not connected	TMS	In		
D34	Not connected	TRST_N	In		
C34	GA0	GA0	In	LVCMOS	ID EEPROM E1
D35	GA1	GA1	In	LVCMOS	ID EEPROM E0
J39	Not connected	VIO_B_M2C	Out		
K40	Not connected	VIO_B_M2C	Out		

8.2. HPC FMC Connector for the Extender TB-FMCH-12GSDI Card

The FMC connector (High-Pin Count) connecting to the extender FMC uses Samtec ASP-134486-01. Table 8-2 shows the FMC extender connector pin assignment.

Table 8-2 HPC FMC Extender Board Connector Pin Assignment

J11 Pin	Schematic Signal Name	VITA 57.1 Name	FMC Direction	Type	Description
SDI Differential Pairs					
C2	EX_CH0_SDI_P	DP0_C2M_P	In	LVDS	Channel 0 Output
C3	EX_CH0_SDI_N	DP0_C2M_N			
A22	EX_CH1_SDI_P	DP1_C2M_P	In	LVDS	Channel 1 Output
A23	EX_CH1_SDI_N	DP1_C2M_N			
A26	EX_CH2_SDI_P	DP2_C2M_P	In	LVDS	Channel 2 Output
A27	EX_CH2_SDI_N	DP2_C2M_N			
A30	EX_CH3_SDI_P	DP3_C2M_P	In	LVDS	Channel 3 Output
A31	EX_CH3_SDI_N	DP3_C2M_N			
C6	EX_CH0_SDO_P	DP0_M2C_P	Out	LVDS	Channel 0 Input
C7	EX_CH0_SDO_N	DP0_M2C_N			
A2	EX_CH1_SDO_P	DP1_M2C_P	Out	LVDS	Channel 1 Input
A3	EX_CH1_SDO_N	DP1_M2C_N			
A6	EX_CH2_SDO_P	DP2_M2C_P	Out	LVDS	Channel 2 Input
A7	EX_CH2_SDO_N	DP2_M2C_N			
A10	EX_CH3_SDO_P	DP3_M2C_P	Out	LVDS	Channel 3 Input
A11	EX_CH3_SDO_N	DP3_M2C_N			
SPI and I2C Signals					
D17	EX_SPI_MOSI	LA13_P	In	LVCMOS (VADJ)	SPI MOSI
D18	EX_SPI_MISO	LA13_N	Out	LVCMOS (VADJ)	SPI MISO
D20	EX_SPI_SCLK	LA17_CC_P	In	LVCMOS (VADJ)	SPI SCLK
D11	EX_SPI_S0	LA05_P	In	LVCMOS (VADJ)	SPI Mux Select 0
D9	EX_SPI_S1	LA01_CC_N	In	LVCMOS (VADJ)	SPI Mux Select 1
D15	EX_SPI_CS1	LA09_N	In	LVCMOS (VADJ)	SPI Chip Select for M23145G
D14	EX_SPI_CS2	LA09_P	In	LVCMOS (VADJ)	SPI Chip Select for M23428G
D12	EX_SPI_CS3	LA05_N	In	LVCMOS (VADJ)	SPI Chip Select for M23554G
H13	EX_CTL_I2C_SCL	LA07_P	In	LVCMOS OD (VADJ)	Control I2C Clock
H14	EX_CTL_I2C_SDA	LA07_N	BI-DIR	LVCMOS OD (VADJ)	Control I2C Data
C30	EX_I2C_SCL	SCL	In	LVCMOS	FMC ID EEPROM I2C Clock
C31	EX_I2C_SDA	SDA	BI-DIR	LVCMOS	FMC ID EEPROM I2C Data

J11 Pin	Schematic Signal Name	VITA 57.1 Name	FMC Direction	Type	Description
Control and Miscellaneous Signals					
C10	EX_XALARM_TX_CH0	LA06_P	Out	LVCMOS (VADJ)	Channel 0 M23145G xALARM
C11	EX_XALARM_TX_CH1	LA06_N	Out	LVCMOS (VADJ)	Channel 1 M23145G xALARM
C14	EX_XALARM_TX_CH2	LA10_P	Out	LVCMOS (VADJ)	Channel 2 M23145G xALARM
C15	EX_XALARM_TX_CH3	LA10_N	Out	LVCMOS (VADJ)	Channel 3 M23145G xALARM
H16	EX_XALARM_RX_CH0	LA11_P	Out	LVCMOS (VADJ)	Channel 0 M23554G xALARM
H17	EX_XALARM_RX_CH1	LA11_N	Out	LVCMOS (VADJ)	Channel 1 M23554G xALARM
H19	EX_XALARM_RX_CH2	LA15_P	Out	LVCMOS (VADJ)	Channel 2 M23554G xALARM
H20	EX_XALARM_RX_CH3	LA15_N	Out	LVCMOS (VADJ)	Channel 3 M23554G xALARM
G30	EX_CH1_DIR	LA29_P	In	LVCMOS (VADJ)	Channel 1 PE42520 CTRL
G33	EX_CH2_DIR	LA31_P	In	LVCMOS (VADJ)	Channel 2 PE42520 CTRL
C18	EX_CH3_DIR	LA14_P	In	LVCMOS (VADJ)	Channel 3 PE42520 CTRL
H1	Not connected	VREF_A_M2C	Out		
K1	Not connected	VREF_B_M2C	Out		
D1	Not connected	PG_C2M	In		Not used
F1	10k to VCC_3V3	PG_M2C	Out		Not used
H2	EX_PRSNT	PRSNT_M2C_N	Out	LVCMOS	Extender Present
D29	Not connected	TCK	In		
D30	0 ohm to TDO	TDI	In		
D31	0 ohm to TDI	TDO	Out		
D33	Not connected	TMS	In		
D34	Not connected	TRST_N	In		
C34	GA0	GA0	In	LVCMOS	ID EEPROM E1
D35	GA1	GA1	In	LVCMOS	ID EEPROM E0
J39	Not connected	VIO_B_M2C	Out		
K40	Not connected	VIO_B_M2C	Out		

8.3. HDBNC Connectors

The SDI connectors use Samtec coaxial High Density BNC (HDBNC) HDBNC-J-P-GN-RA-BH2 connectors. Figure 8-1 shows the positions and assignments for each front edge connector.

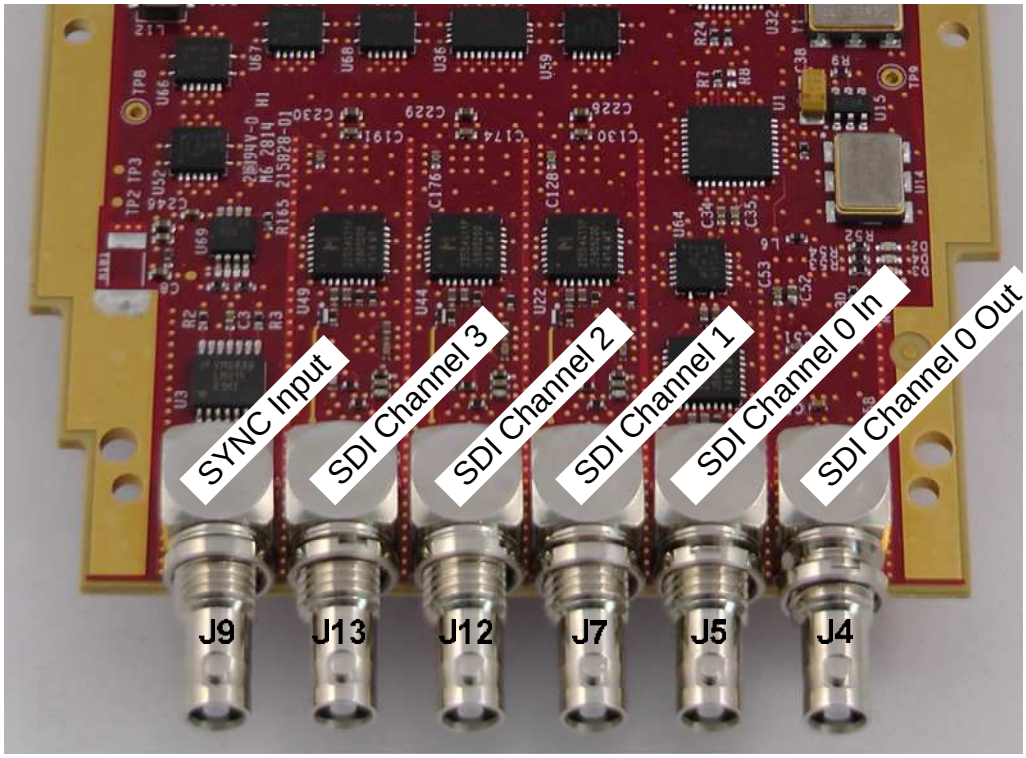

Figure 8-1 TB-FMCH-12GSDI Front Edge HDBNC Coaxial Connectors

9. SDI Channels

The main function of the TB-FMCH-12GSDI card is to enable SDI connectivity. To accomplish this, there are 5 HDBNC connectors. SDI channel 0 consists of two HDBNC connectors: 1 dedicated input, and 1 dedicated output. SDI channels 1, 2, and 3, are each provisioned with a single HDBNC connector. An SPDT RF switch located at each connector on channels 1, 2, and 3, determines the desired functionality (i.e. input or output). The system block diagram at the beginning of this document depicts the key components that are present on each channel.

Table 9-1 SDI Channel Major Components

Manufacturer	Part Number	Description
Transmit System		
MACOM	M23145G	Multi-Rate Digital Re-Clocker
MACOM	M23428G	Low Jitter Cable Driver
Receive System		
MACOM	M23554G	Adapter Equalizer w/ Re-Clocker
Transit/Receive		
Peregrine	PE42520	SPDT RF Switch (9KHz to 13GHz, 50 ohm)

Each device in the table above is programmable via SPI.

Each RF switch direction is controlled by the signal: CHx_DIR; 0=Rx (input to FMC), 1=Tx (output from FMC). Although the switch is absorptive and offers good isolation, it is recommended that any transmit circuitry be disabled when operating in receive mode.

Note: Exceeding the maximum input level or connecting multiple outputs together can cause irreparable damage to the TB-FMCH-12GSDI FMC. Always confirm your Tx/Rx switch configurations prior to enabling outputs or driving inputs.

Note: All SDI inputs/outputs are AC coupled.

Note: Maximum input levels

- Peregrine Semiconductor, PE42520 RF Switch: Frequency dependent, refer to PE42520 datasheet, and remember to consider that this is a 50 ohm specified part operating in a 75 ohm system.
- MACOM M23554G Adaptive Cable Equalizer: 880mVpp

Note: The PE42520 is a 50 ohm RF switch. Signal integrity assessments have confirmed that this part will work as required in this 75 ohm system.

10. Multiplexed SPI Busses

All MACOM devices (M23145G, M23428G, M23554G) are configured/controlled via four-wire SPI busses. As there are 12 MACOM devices per TB-FMCH-12GSDI, there would be many FPGA pins required, for just the SPI busses. To reduce the number of FMC signal connections to something more desirable, at the expense of complexity, the busses are multiplexed. Structurally, each of the four SDI channels has a separate SPI bus. Table 10-1 shows the connections and signals for the SPI busses. Three dual SP4T SN74LV4052 multiplexer chips are controlled with two signals (SPI_S0, SPI_S1) to select which of the four SPI busses is connected to the FPGA. The maximum SPI bus clock frequency is 20MHz.

The following table show which SPI bus is active based on the state of the multiplexer selection signals, and which chip select signal corresponds with which MACOM device.

Table 10-1 SPI Decoding

SPI_S1	SPI_S0	SDI Ch Selected
0	0	0
0	1	1
1	0	2
1	1	3

Chip Select Signal	Device Selected
SPI_CS1	Reclocker (M23145G)
SPI_CS2	Cable Driver (M23428G)
SPI_CS3	Equalizer (M23554G)

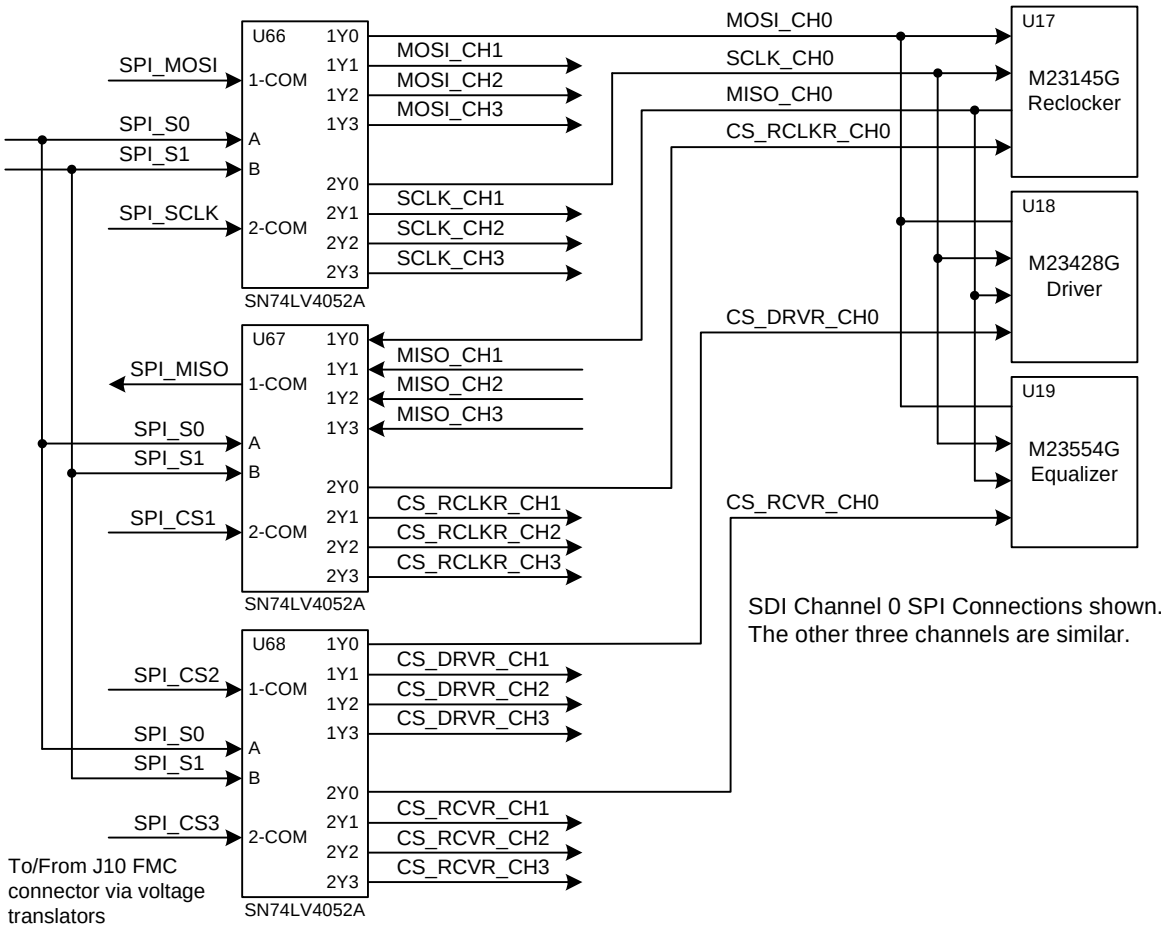

Figure 10-1 SPI Multiplexer Connections

11. FMC I2C EEPROM

A 2kbit I2C EEPROM (M24C02) is provided for FMC identification, as described in section 5.5 of ANSI/VITA 57.1. It is at I2C address 0b1010000x and is connected to the FMC dedicated I2C pins at J10-C30 (SCL) and J10-C31 (SDA). The pull-up resistors to 3V3_AUX are populated (R163 and R164). The EEPROM is permanently enabled for writing.

The FMC identification EEPROM for the extender card is connected to J10-C22 (LA18_CC_P) for SCL and J10-C23 (LA18_CC_N) for SDA. These signals are connected to J11-C30 (SCL) and J11-C31 (SDA) via a PCA9517 I2C bus repeater.

The FMC identification EEPROM is programmed at the factory to enable automated identification, verification, and configuration of Main Board parameters. The contents of the EEPROM are displayed in Appendix A.

Note: The user must be cognizant that the FMC I2C EEPROM is always write-enabled. As it contains critical information required for correct operation, one must never overwrite the factory settings.

12. Sync Input

The Sync input on the FB-FMCH-12GSDI FMC allows the user to synchronize the FPGA-FMC system to an external video system.

The Sync input on HDBNC J9 is first terminated with 75 ohms (to ground) and then AC coupled before entering the LMH1981 video sync separator. The LMH1981 will accept a wide variety of video signals up to 1080p. The odd/even field, horizontal, and vertical sync outputs are connected to the FMC carrier board connector. The LMH1981 automatically detects the video format and accepts video signals up to 1.2Vpp. Please see the LMH1981 data sheet for complete details on its operation.

Note: Exceeding the maximum input level on the Sync input can cause irreparable damage to the TB-FMCH-12GSDI FMC. Do not exceed 1.2Vpp and 0V DC.

13. Video Clock Generation

Figure 13-1 shows the video clock generation circuit. It basically consists of the LMH1983 video clock generator and the DS10CP154 crosspoint switch. The LMH1983 is very versatile and can generate almost any required SDI video clocks. The LMH1983 and the crosspoint switch are controlled via an I2C bus. Two oscillators feed the crosspoint switch to supply common video clock frequencies. The LMH1983 FIN, HIN, and VIN clocks can also be supplied from the LMH1981 sync separator through the FPGA so the SDI channels can be synchronized with an external video source.

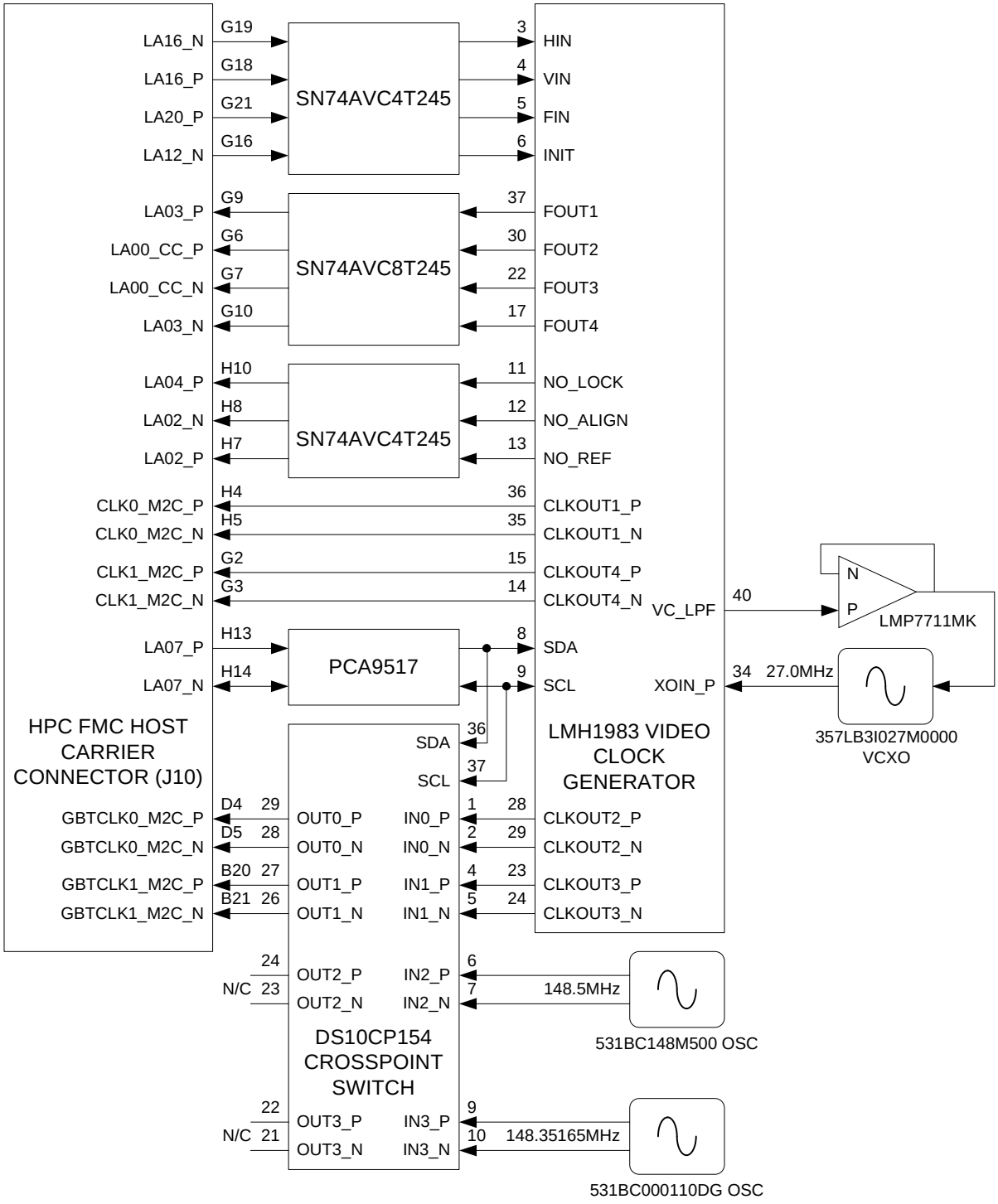

Figure 13-1 Video Clock Generation Circuit

14. Test Points and LEDs

There are 11 test points accessible on the side of the card on which the HDBNC connectors are mounted. This includes four through-hole ground test points and seven test point pads for voltage rails. Table 14-1 lists all the test points and Figure 14-1 shows the locations of the test points. Note that TP7 does not exist.

There are three LEDs on the side of the card on which the HDBNC connectors are mounted. The LEDs are on the LMH1983 video clock generator status outputs. D2 is on the NO_REF output, D3 is on the NO_ALIGN output and D4 is on the NO_LOCK output. There are no LEDs for any voltage rail.

Table 14-1 Test Points

Test Point	Schematic Signal Name	Nominal Voltage	Component Pin
TP1	None	12V	U34-11, 12
TP2	2V5	2.5V	none
TP3	3V3	3.3V	none
TP4	12V	12.0V	J10-C35, C37
TP5	3V3_AUX	3.3V	J10-D32
TP6	FMC_VADJ	1.2V to 3.3V	J10-E39, F40, G39, H40
TP8	GND	ground	---
TP9	GND	ground	---
TP10	GND	ground	---
TP11	GND	ground	---
TP12	3V3_VDSS	3.3V	U3-3, 6, 11

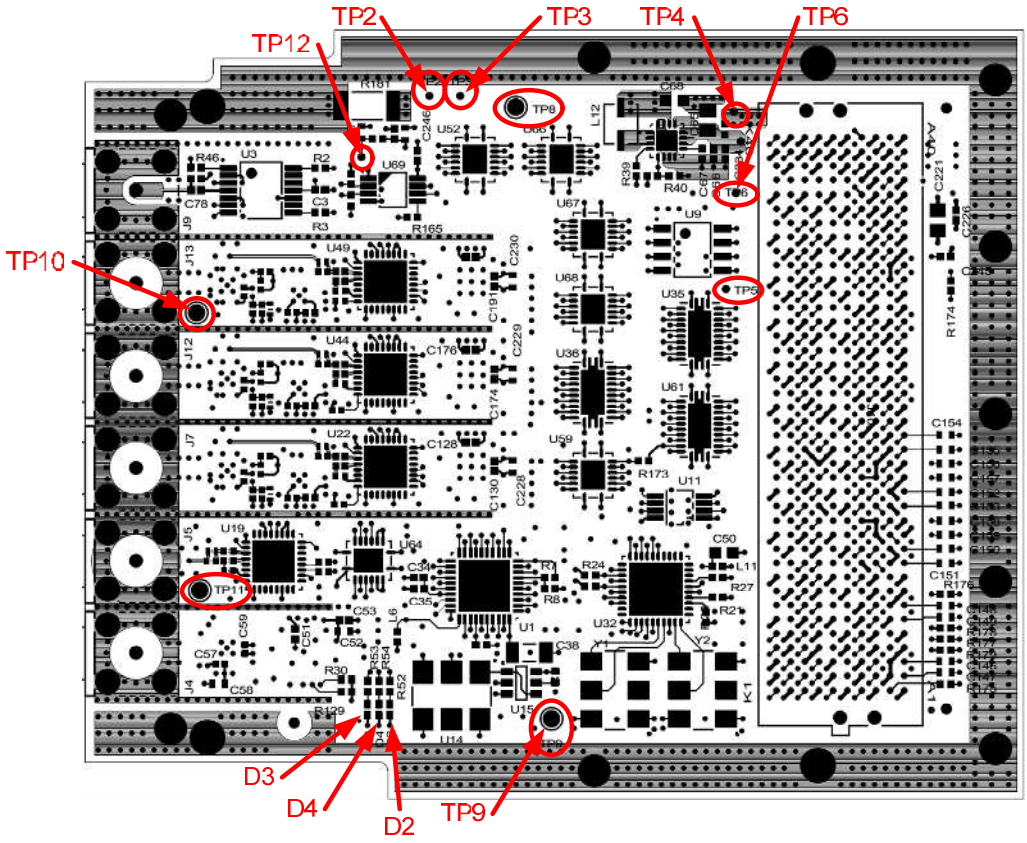

Figure 14-1 Test Point and LED Locations on HDBNC Connector Side

15. Usage Example

An FPGA demonstration load is available on the inrevium website.

16. Appendix A: FMC I2C EEPROM Contents

The following table describes the contents of the FMC I2C EEPROM as programmed at the factory.

Table 16-1 FMC I2C EEPROM Contents

NOT CURRENTLY AVAILABLE

TOKYO ELECTRON DEVICE

PLD Solution Dept. PLD Division
URL: **http://solutions.inrevium.com/**
E-mail: psd-support@teldevice.co.jp

HEAD Quarter: Yokohama East Square, 1-4 Kinko-cho, Kanagawa-ku, Yokohama City,
Kanagawa, Japan 221-0056
TEL: +81-45-443-4016 FAX: +81-45-443-4058