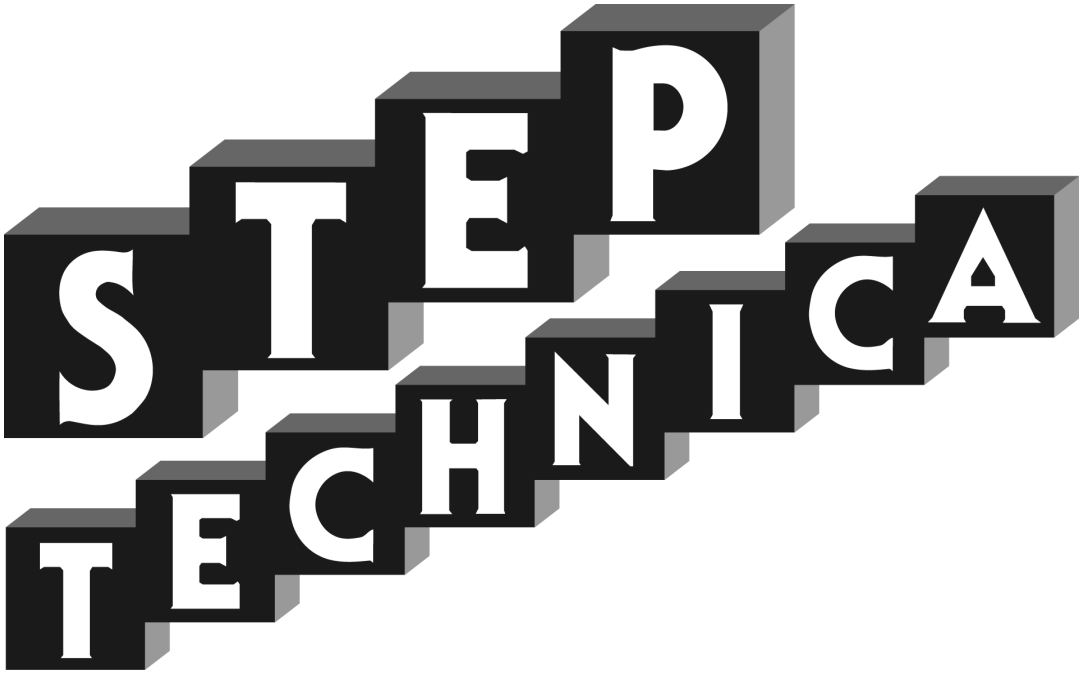
STD-HLS02-V1.5E

STEP TECHNICA CO.,LTD.



HUB-IC MKY02

User's Manual

(for Hi-speed Link System)

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Preface

This manual describes the MKY02, or a kind of HUB-IC in a Hi-speed Link System.
Be sure to read ***"Hi-speed Link System Introduction Guide"*** before understanding this manual and the MKY02.
In this manual, the Hi-speed Link System is abbreviated as "HLS".

● **Target Readers**

This manual is for:

- Those who first build an HLS
- Those who first use StepTechnica's various ICs to build an HLS

● **Prerequisites**

This manual assumes that you are familiar with:

- Network technology
- Semiconductor products (especially microcontrollers and memory)

● **Related Manuals**

- Hi-speed Link System Introduction Guide
- Hi-speed Link System Technical Guide
- Hi-speed Link System Center IC Manuals

[Caution]

- Some terms in this manual are different from those used on our website and in our product brochures. The brochure uses ordinary terms to help many people in various industries understand our products.
  Please understand technical information on HLS Family and CUnet Family based on technical documents (manuals).

■ This manual has been prepared based on Standard English™ meeting the requirements of the International Organization for Standardization (ISO) and the American National Standards Institute (ANSI). This English manual is consistent with the Japanese document **"STD-HLS02-V1.5J"**.

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CONTENTS

Chapter 1 Concepts for Using MKY02 (HUB)

1.1 Role of MKY02 1-3
1.2 Basic HLS Configuration 1-3
1.3 HLS Configuration using HUBs 1-4
1.3.1 Extending Total Length of Network Cable 1-4
1.3.2 Branching Multi-dropped Network Cables 1-6
1.3.3 Eliminating Connection or Disconnection of Termination Resistor to or from Each Device 1-7
1.3.4 Star Topology 1-8
1.3.5 Handling Fiber-optic Cables 1-9
1.4 Basic HUB Connection 1-10
1.5 Multi-drop Network of HUBs 1-11
1.6 Port Addition to HUB 1-12
1.7 MKY02 Operation 1-13
1.7.1 Receiving and Sending Packets 1-13
1.7.2 Signal Correction 1-14
1.7.3 Detection of Error Packet 1-14
1.8 Features of MKY02 1-15

Chapter 2 MKY02 Hardware 2-3

Chapter 3 Single Connection of MKY02

3.1 Voltage Levels of Pins Connecting to Signal Pins 3-4
3.2 Supplying Driving Clock and Hardware Reset Signal 3-5
3.2.1 Supplying Driving Clock 3-5
3.2.2 Setting Cascade Clock and Baud Rate 3-6
3.2.3 Hardware Reset 3-7
3.3 Connecting Network Interface 3-8
3.3.1 Selecting Communication Mode 3-8
3.3.2 Connection of Port 0 3-8
3.3.3 Connection of Ports 1 to 7 3-9
3.3.4 Recommended Network Connection 3-10
3.4 Connecting Monitor LEDs 3-11
3.4.1 Packet Receive Monitor 3-11
3.4.2 Packet Error Monitor 3-12
3.4.3 Port Receive Monitor 3-13
3.5 Handling Cascade Connection Pins 3-15
3.6 Cautions for Designing HUB 3-15
3.7 Example Circuit for Single Connection of MKY02 3-16

Chapter 4 Cascade Connection of MKY02

4.1 Concepts of Port Addition 4-3
4.1.1 Port Addition by Stacking Method 4-3
4.1.2 Port Addition by Cascade Connection 4-4
4.1.3 Maximum Available Cascade Connections 4-4
4.2 Practical Side of Cascade Connection 4-5
4.2.1 Cascade Pins 4-5
4.2.2 Operation of Cascade Connection Pins 4-6
4.2.3 Connection of Cascade Clocks and Determination of Baud Rate 4-7
4.2.4 Connection of Hardware Reset Signal 4-7
4.2.5 Selecting Communication Mode 4-8
4.2.6 Connection of Each Port 4-8
4.2.7 Placement of Monitor LEDs 4-9
4.3 Example Circuit for Port-added HUB by Cascade Connection 4-10

Chapter 5 Ratings

5.1 Electrical Ratings 5-3
5.2 AC Characteristics 5-3
5.2.1 Clock and Reset Timing 5-4
5.2.2 Port Pin Timing (TXE0 to 7, TXD0, TXD17, RXD0 to 7) 5-5
5.2.3 Cascade Connection Pin Timing 5-6
5.2.4 Output Timing of #LEDRCV and #LEDRZE Pins 5-6
5.2.5 Timing of Receive Monitor Pin of Individual Port (RLLD, RLDT, RLCK) 5-7
5.3 Package Dimensions 5-8
5.4 Recommended Soldering Conditions 5-9
5.5 Recommended Reflow Conditions 5-9

Figures

Fig. 1.1 Basic HLS Configuration 1-3
Fig. 1.2 Extension of Network Cable Length 1-4
Fig. 1.3 Multipoint Connection of Network Cables 1-6
Fig. 1.4 Eliminating Problems with Termination Resistors 1-7
Fig. 1.5 Star Topology 1-8
Fig. 1.6 Serial Connection of Fiber-optic Cables 1-9
Fig. 1.7 Basic Connection and Number of Inserted HUBs 1-10
Fig. 1.8 HUB in Intermediate Position of Multi-drop Network 1-11
Fig. 1.9 Adding Ports by Cascading MKY02s 1-12
Fig. 1.10 Inserted Count of HUBs with Added Ports 1-12
Fig. 1.11 MKY02 Operating Principles 1-13
Fig. 1.12 Example of Signal Transformation and Correction 1-14
Fig. 2.1 MKY02 Pin Assignment 2-3
Fig. 2.2 Pin Electrical Characteristics in I/O Circuit Types of MKY02 2-6
Fig. 3.1 Connection Causing Leakage Current 3-4
Fig. 3.2 Cascade Clock Generation 3-6
Fig. 3.3 Clock Connection 3-6
Fig. 3.4 Hardware Reset 3-7
Fig. 3.5 Selecting Communication Mode 3-8
Fig. 3.6 TRX Connection of Port 0 3-8
Fig. 3.7 TRX Connection of Ports 1 to 7 3-9
Fig. 3.8 TRX Connection of HUB with 4 Ports 3-9
Fig. 3.9 Recommended Network Connection 3-10
Fig. 3.10 Connection of Receive Monitor LED 3-11
Fig. 3.11 Connection of Packet Error Monitor LED 3-12
Fig. 3.12 RLLD, RLDT, and RLCK Outputs 3-13
Fig. 3.13 8-port Receive Monitor 3-14
Fig. 3.14 4-port Receive Monitor 3-14
Fig. 3.15 Handling of Cascade Connection Pins 3-15
Fig. 3.16 Example of Single Connection Circuit in Half-duplex Mode 3-16
Fig. 3.17 Example of Single Connection Circuit in Full-duplex Mode 3-17

Fig. 4.1 Addition of Three-stacked Ports 4-3
Fig. 4.2 Port Addition by Three Cascade Connections 4-4
Fig. 4.3 Cascade Pin Connection for Three MKY02s 4-5
Fig. 4.4 Cascade Pin Connection for Two MKY02s 4-5
Fig. 4.5 Center Ports and Operation during Receiving 4-6
Fig. 4.6 Satellite Ports and Operation during Receiving 4-6
Fig. 4.7 Connection of Cascade Clocks 4-7
Fig. 4.8 Selection of Communication Mode 4-8
Fig. 4.9 Monitor Placement Example for Port-added HUB 4-9
Fig. 4.10 Example Circuit for HUB with 22 Ports 4-10
Fig. 4.11 Example of Connection in Full-duplex Mode 4-13

Tables

Table 1-1 Baud Rates and Recommended Total Extension Number of Inserted HUBs 1-4
Table 2-1 Pin Functions of MKY02 2-4
Table 2-2 Electrical Ratings of MKY02 2-6
Table 3-1 Output Frequencies of Cascade Clocks 3-6
Table 5-1 Absolute Maximum Ratings 5-3
Table 5-2 Electrical Ratings 5-3
Table 5-3 AC Characteristics Measurement Conditions 5-3

Chapter 1 Concepts for Using MKY02 (HUB)

This chapter describes the concepts for using the MKY02 (HUB) in the Hi-speed Link System (HLS).

1.1 Role of MKY02.....1-3
1.2 Basic HLS Configuration 1-3
1.3 HLS Configuration using HUBs.....1-4
1.4 Basic HUB Connection.....1-10
1.5 Multi-drop Network of HUBs.....1-11
1.6 Port Addition to HUB.....1-12
1.7 MKY02 Operation.....1-13
1.8 Features of MKY02 1-15

Chapter 1 Concepts for Using MKY02 (HUB)

This chapter describes the concepts for use of the MKY02 (HUB) in the HLS.

1.1 Role of MKY02

MKY02 is a kind of HUB-IC that constitutes a HUB to be used in the HLS network.
Be sure to read ***"Hi-speed Link System Introduction Guide"*** and ***"Center IC User's Manuals"*** before using the MKY02 and understanding this manual.

1.2 Basic HLS Configuration

Figure 1.1 shows the basic HLS configuration with one center IC and multiple satellite ICs connected on a multi-drop network. Rt in the figure indicates a termination resistor.

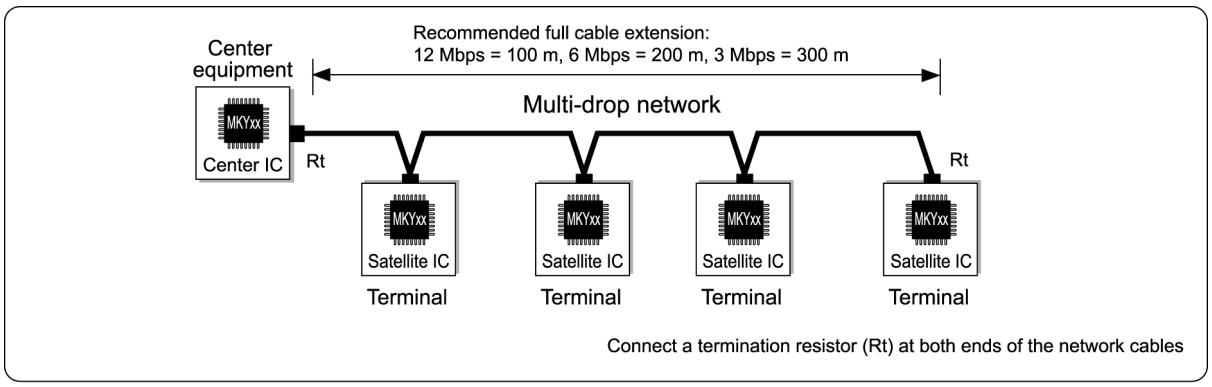


Fig. 1.1 Basic HLS Configuration

Some user systems may need the following for the basic HLS configuration:

(1) To extend the total length of a network cable.
(2) To branch pieces of multi-dropped network.
(3) To eliminate connection or disconnection of termination resistor to or from each device.
(4) To use transmission systems such as optical fiber cables.

There will be difficulty solving these needs using such basic HLS configuration shown in Figure 1.1.

1.3 HLS Configuration using HUBs

Adding HUBs to the HLS network, the user system can satisfy it's own needs (1) to (4) described above.

Caution When adding, a HUB to the network, the center IC constituting the HLS must be compatible with the HUB. If incompatible, the center IC does not link correctly with satellite ICs.

1.3.1 Extending Total Length of Network Cable

Adding HUB(s) to the HLS network, the user can extend the total length of the network cable. Figure 1.2 shows an example of extending the total length of the network cable. Rt in the figure indicates a termination resistor.

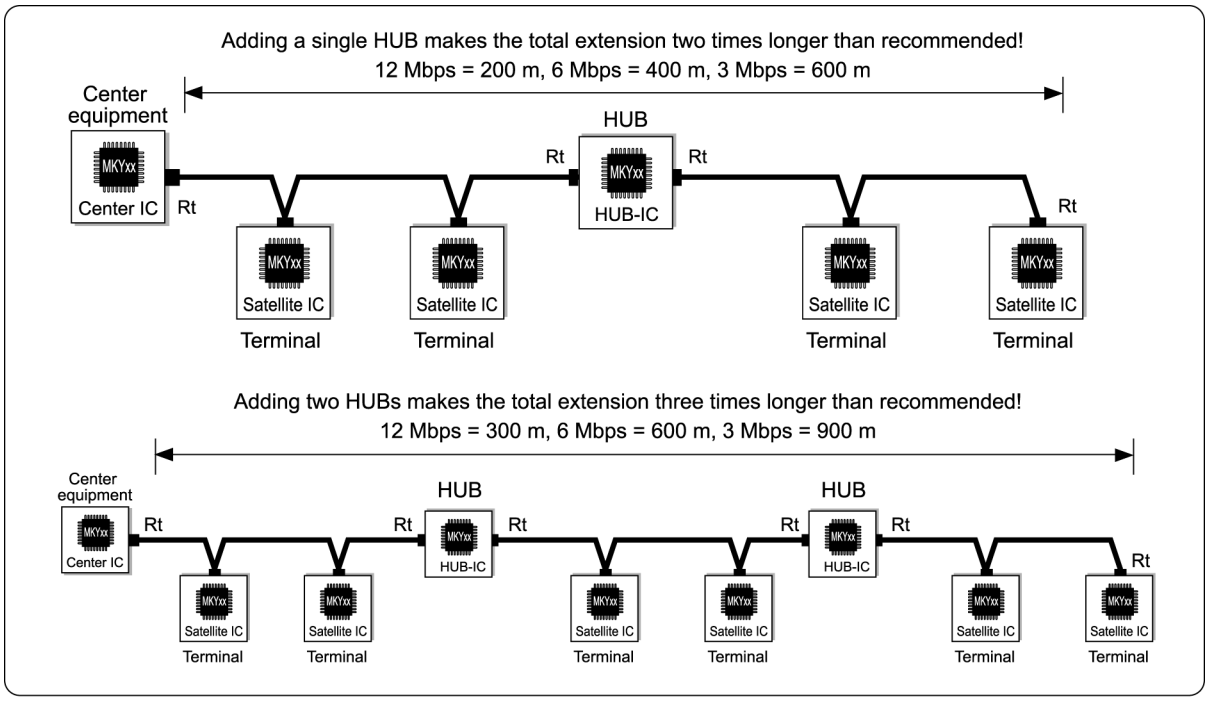


Fig. 1.2 Extension of Network Cable Length

The user system can extend the recommended network cable length by adding the inserted count of HUBs +1 to the basic HLS configuration. For example, adding a single HUB doubles cable length, adding two HUBs triples cable length, and adding seven HUBs increases the cable length eightfold. Table 1-1 shows the baud rates and the recommended total extension based on the number of the inserted HUBs when using the recommended network connection.

Table 1-1 Baud Rates and Recommended Total Extension Number of Inserted HUBs

	Number of inserted HUBs							
Baud rate	0 (Basic configuration)	1	2	3	4	5	6	7
12 Mbps	100 m	200 m	300 m	400 m	500 m	600 m	700 m	800 m
6 Mbps	200 m	400 m	600 m	800 m	1 km	1.2 km	1.4 km	1.6 km
3 Mbps	300 m	600 m	900 m	1.2 km	1.5 km	1.8 km	2.1 km	2.4 km

The practical limit of network cable length varies with the performance of drivers/receivers, cable types, cabling environments, and how many cables are multi-drop connected. StepTechnica's recommended network cable length is about 1/2 of the cable length limit obtained from our practical experiments. These values are provided as a guide for stable HLS operation in various user systems (,but performance is not guaranteed).

Therefore, in many user systems, the user can use the network cable longer than the total length shown in Table 1-1.

The maximum number of HUBs that can be added is determined by the function of the center IC. For example, if the user system uses the MKY36 as a center IC, the user can add up to seven HUBs. For details, refer to ***"Center IC User's Manual"***.

1.3.2 Branching Multi-dropped Network Cables

The network cables can be branched by adding HUBs to the HLS network. Figure 1.3 shows an example of an HLS configuration in which network cables are branched.

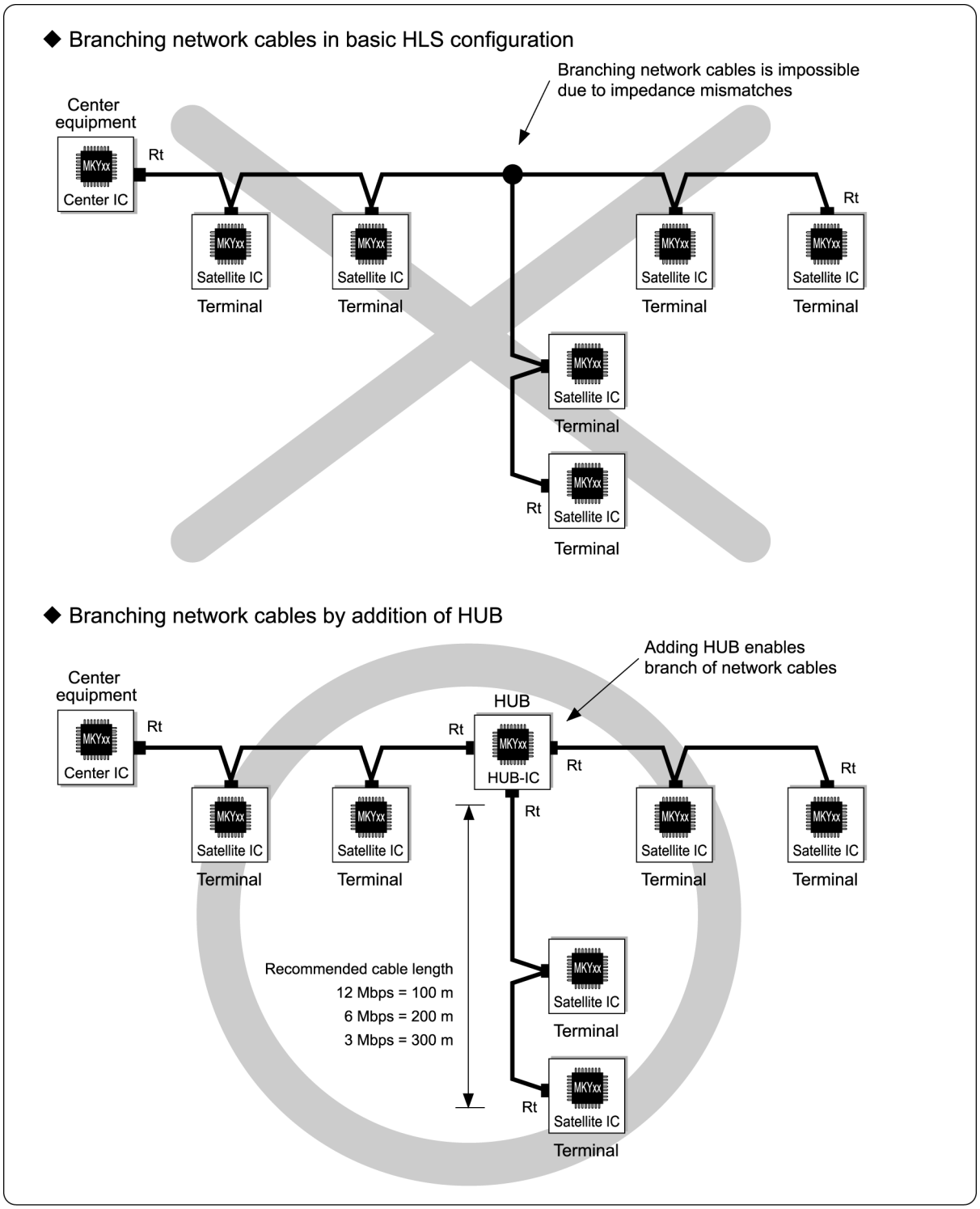


Fig. 1.3 Multipoint Connection of Network Cables

Figure 1.3 shows the network cables that are branched in T shape. Adding a HUB using the MKY02 also enables multiple branchings with many ports.

1.3.3 Eliminating Connection or Disconnection of Termination Resistor to or from Each Device

In a network using the HLS, termination resistors (Rt) cannot be connected to the terminal connected in the intermediate position (the halfway position in the network cable) of the multi-drop network. However, a "one-to-one" connection between all terminals can eliminate connection or disconnection of termination resistor to or from each device and simplifies the complexity of system installation as shown in Figure 1.4.

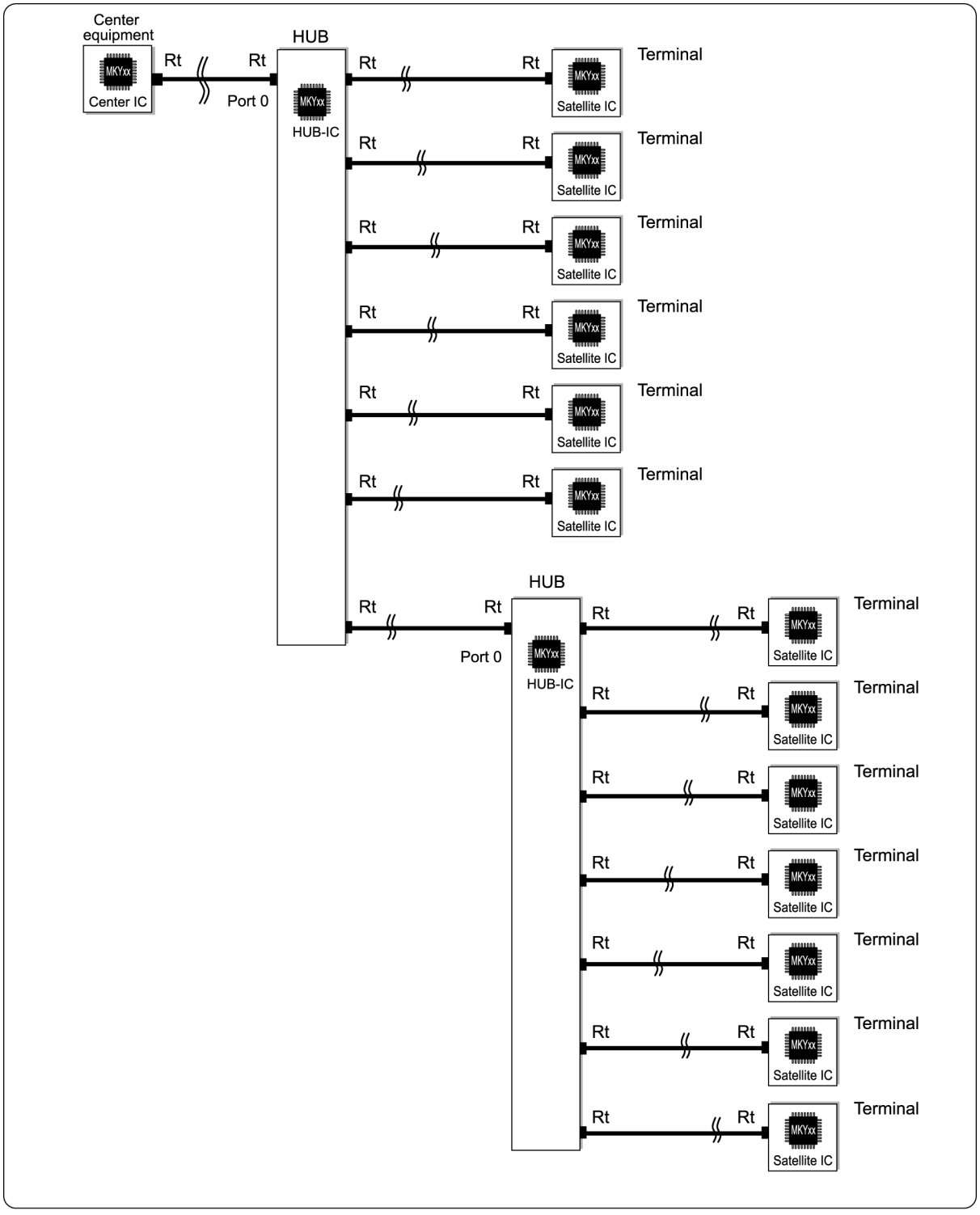


Fig. 1.4 Eliminating Problems with Termination Resistors

1.3.4 Star Topology

Mounting a HUB-IC to the terminal containing the center IC of the HLS can offer a star topology (Fig. 1.5). Furthermore, network cables in a star topology can also be multi-drop-connected.

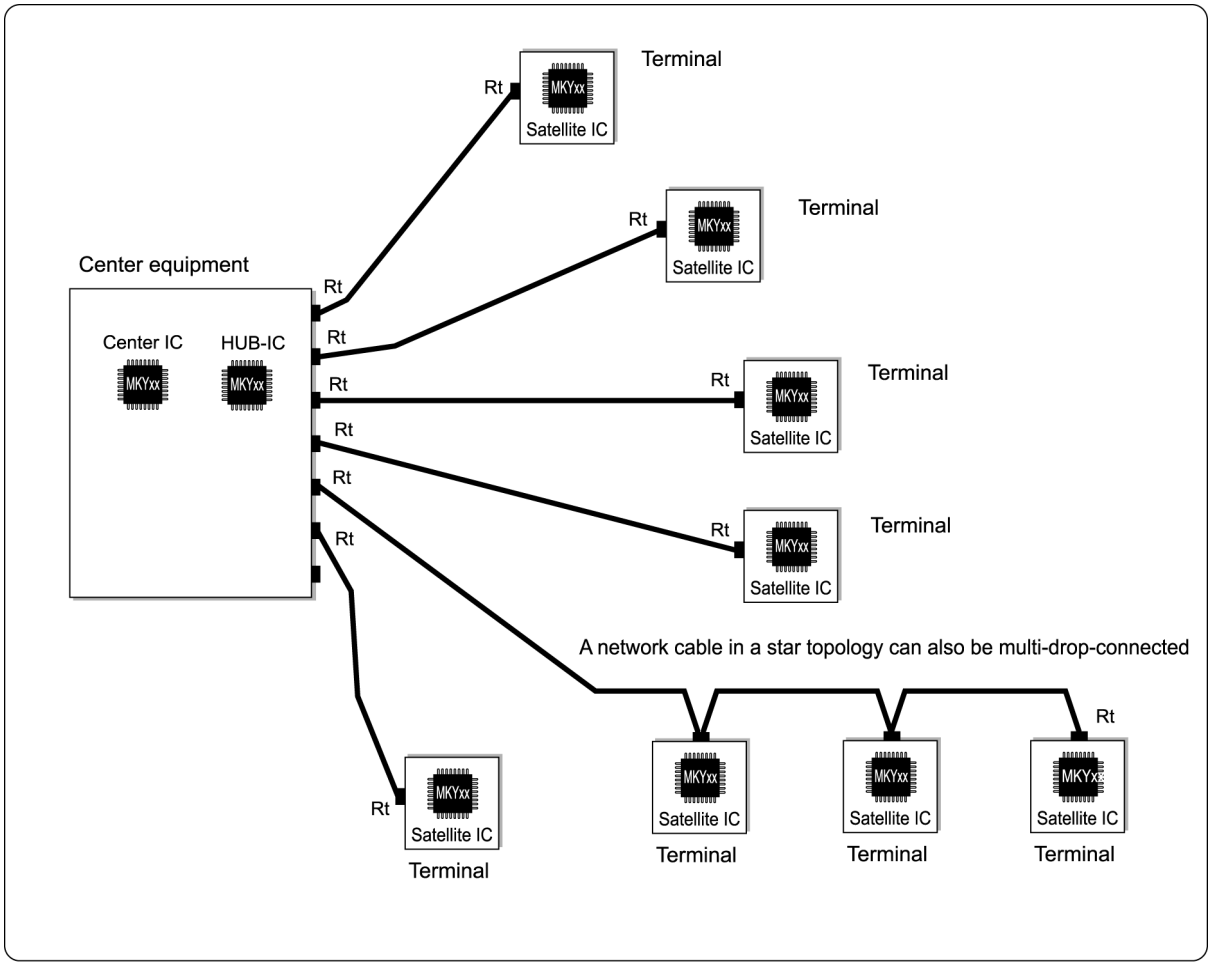


Fig. 1.5 Star Topology

1.3.5 Handling Fiber-optic Cables

There will be difficulties in multi-drop network of transmission signals using fiber-optic cables;

(1) Branching or connection of optical signals is extremely difficult.

(2) "Optical-to-electrical (O/E) conversion, and branching or connecting, and then electrical-to-optical (E/O) conversion" can cause cumulative signal distortion. Therefore, it is impractical to transmit in signals at high baud rates via fiber-optic cables (Fig. 1.6).

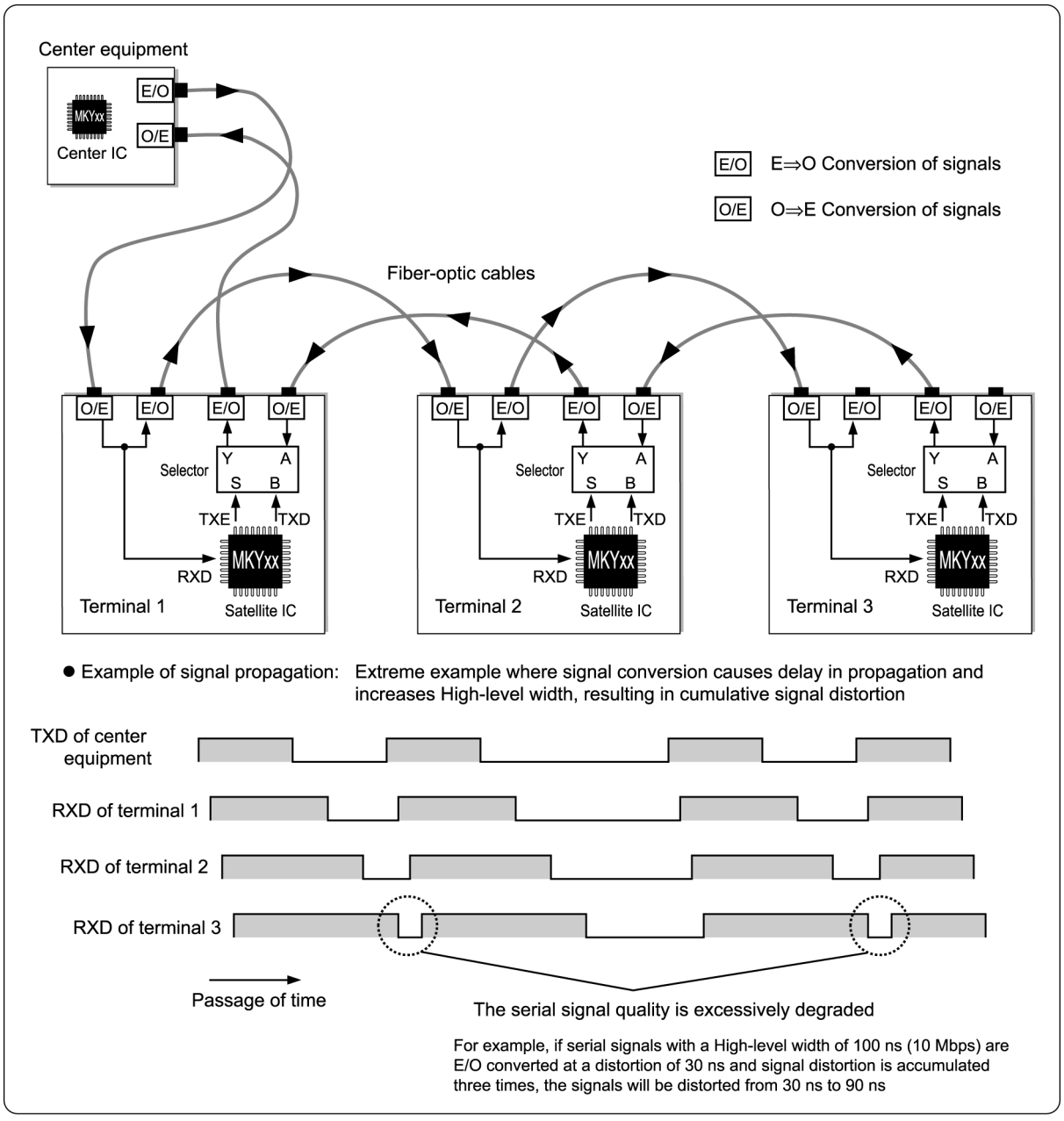


Fig. 1.6 Serial Connection of Fiber-optic Cables

Adding HUBs into the network using the HLS to connect ports and terminals "one-on-one" as shown in Figure 1.4 and 1.5 (excluding multi-drop-connected part) makes it easy to use fiber-optic cables. A "one-on-one" connection between ports and terminals does not cause cumulative signal distortion.

1.4 Basic HUB Connection

When adding HUBs to the HLS, connect them so that the HLS can be a tree structure as shown in Figure 1.7. In such a tree structure, the route node close to the center equipment is called the "center side". Be sure to connect port 0 to the center side.
The number of HUBs to be added in the routes derived from the center equipment is called the "number of inserted (HUBs)". The "number of inserted" HUBs is determined by the type of center IC and settings made at the center IC by the user system.

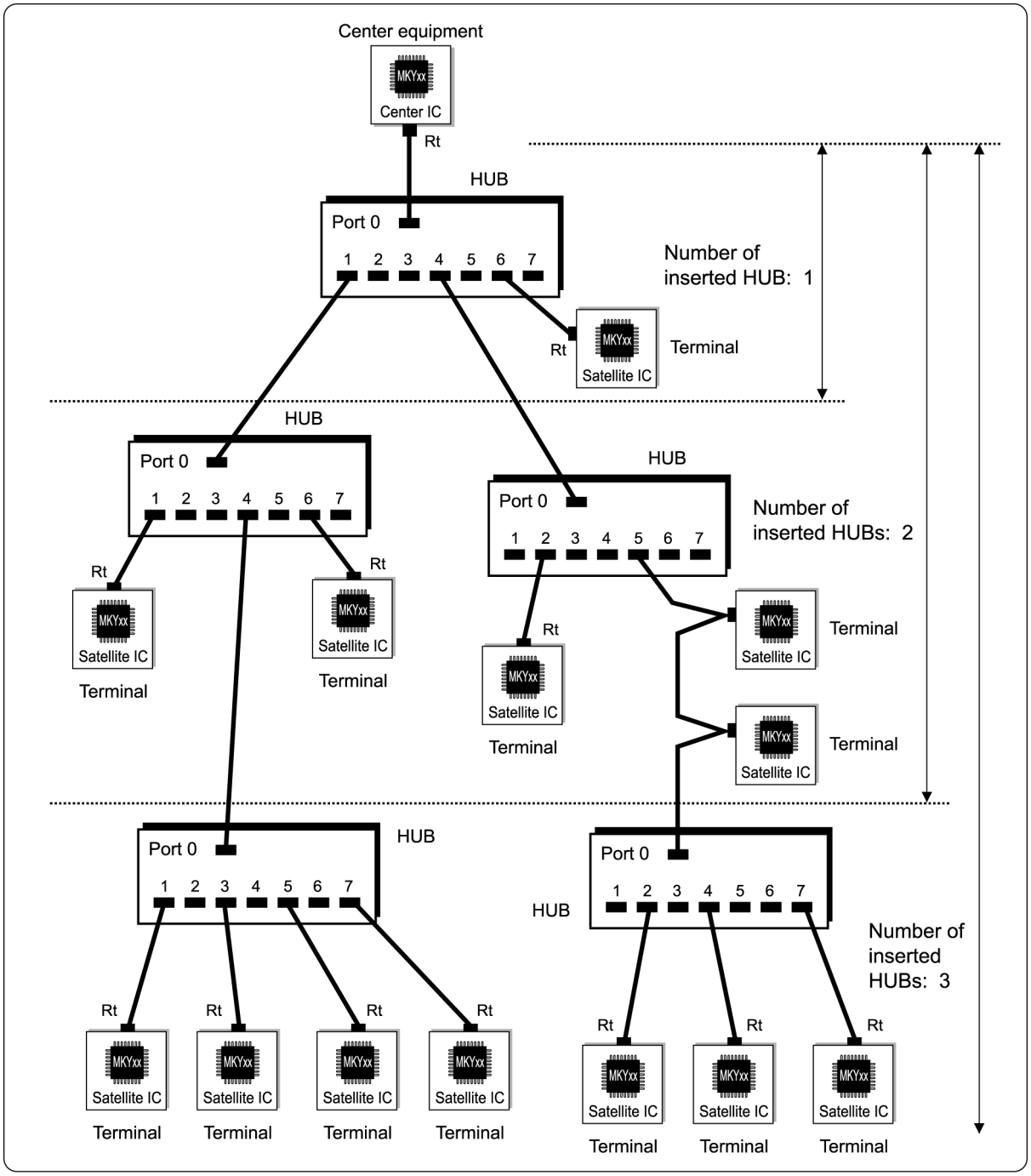


Fig. 1.7 Basic Connection and Number of Inserted HUBs

Caution In the system using the MKY36 as a center IC, the user can add up to seven HUBs. No HUBs can be into a system using the MKY33 as a center IC. For details on each of center ICs, refer to ***"User's Manual"*** for the center IC.

1.5 Multi-drop Network of HUBs

When adding HUBs to the HLS, the user can connect HUBs as multi-drop (Fig. 1.8).
The multi-drop network of HUBs is suitable for a user system in which the network cables should be divided.
The number of inserted HUBs shown in Figure 1.8 is "1".
As shown in Figure 1.8, in cases where port 0 of the HUB is placed in the intermediate position (the halfway position in the network cable) of a multi-drop network, do not connect a termination resistor to the port 0.
For details of the connection of a termination resistor, refer to ***"Hi-speed Link System Technical Guide"***.

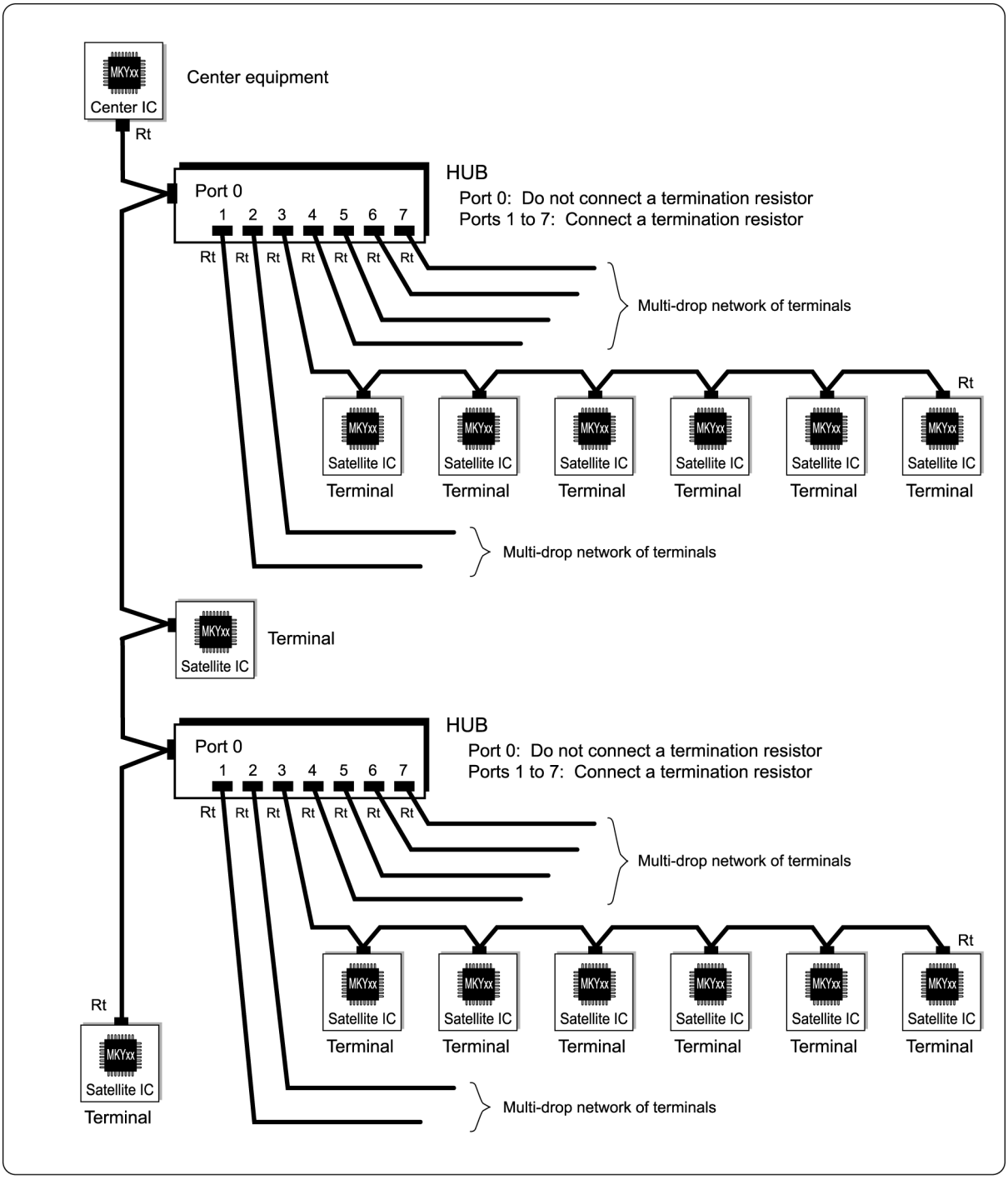


Fig. 1.8 HUB in Intermediate Position of Multi-drop Network

1.6 Port Addition to HUB

By cascading MKY02s, the user can add more ports to a HUB composed of the MKY02.
For example, a cascade connection of three MKY02s enables the HUB to have port 0 connecting the center side and 21 ports (7 ports × 3) connecting the satellite side (Fig. 1.9).

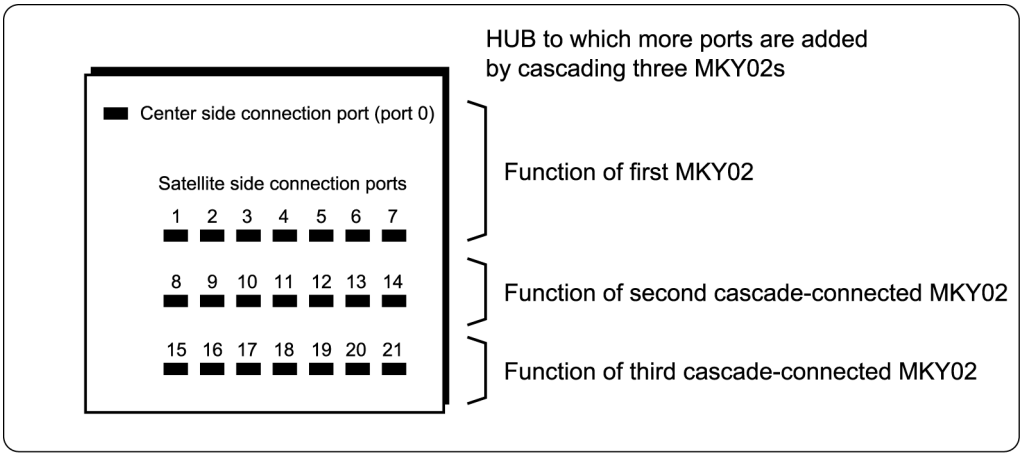


Fig. 1.9 Adding Ports by Cascading MKY02s

If a HUB with ports added by cascading MKY02s is added to a network, the number of inserted HUBs between terminals and the center IC connected to each port of the HUB is "1" (Fig. 1.10).

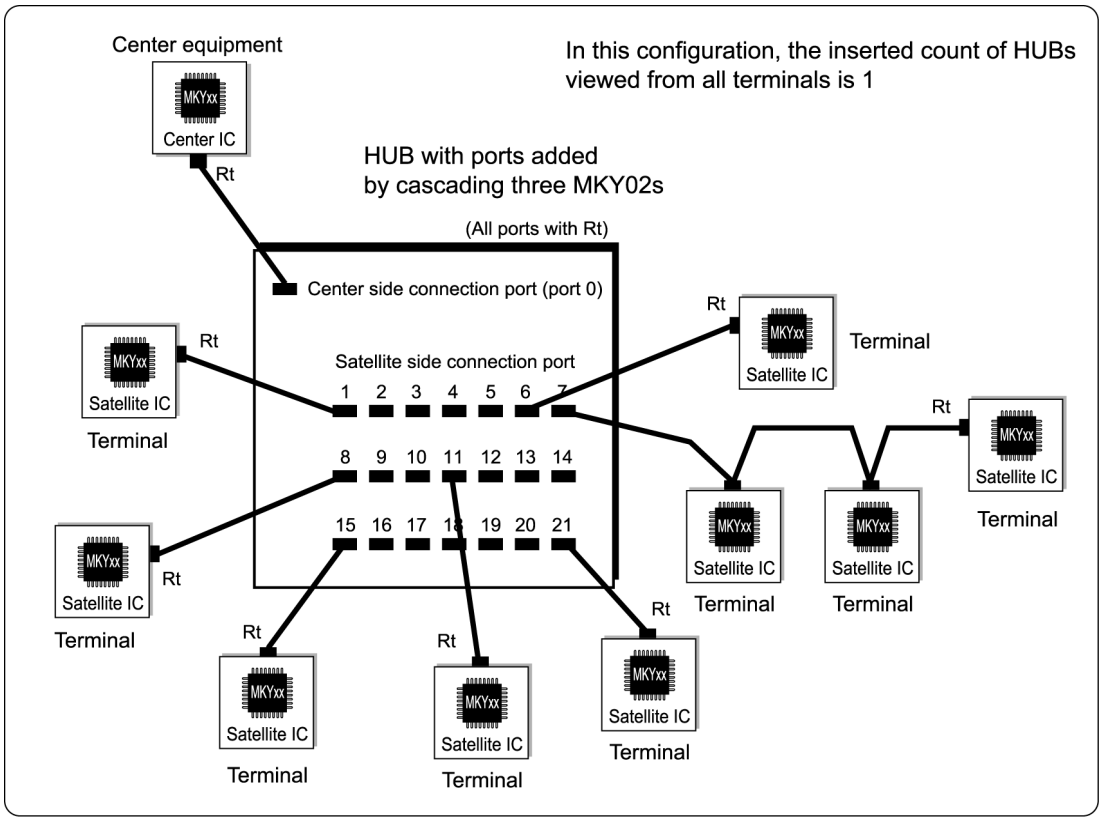


Fig. 1.10 Inserted Count of HUBs with Added Ports

Adding ports by cascading MKY02s is helpful to setup cables on multi-drop network or star topology. For details of cascading MKY02s, refer to ***"Chapter 4 Cascade Connection of MKY02"***.

1.7 MKY02 Operation

This section describes the operation of the MKY02. Be sure to read this section before adding HUBs to the HLS.

1.7.1 Receiving and Sending Packets

The MKY02 operates as follows:

(1) When the MKY02 receives a packet from port 0 (center side port), it corrects the signals constituting the packet into a complete format, and sends the corrected packet to ports 1 to 7.

(2) When the MKY02 receives a packet from any one of the ports 1 to 7 (satellite side ports), it corrects the signals constituting the packet into a complete format, and sends the corrected packet to port 0. During a series of operations, ports other than the active port do not receive a packet. (For example, while port 3 is active, ports 1, 2, and 4 to 7 do not receive a packet.)

(3) When the FH pin of the MKY02 is High level (full-duplex mode), the above operations (1) and (2) function independently.

(4) When the FH pin is Low level (half-duplex mode), either of the above operations (1) and (2) starting first functions. During this period, no ports receive a packet.

As described in (1) and (2) above, the MKY02 corrects the received packet into a complete format and sends it, resulting in a time lag of 52 × TBPS (max.) from receiving to sending packets (Fig. 1.11). Each port of the MKY02 has priorities to handle system exceptions generated when multiple ports receive a packet simultaneously. The MKY02 starts operation in ascending order of port numbers (Fig. 1.11). In full-duplex mode, ports 0 and 1 have no priorities.

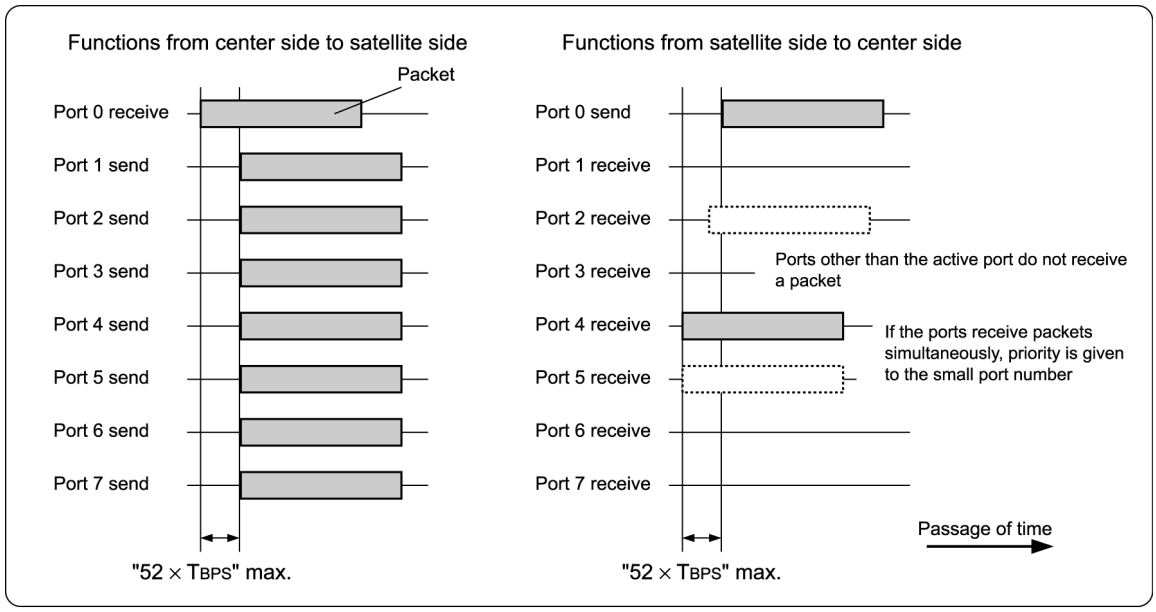


Fig. 1.11 MKY02 Operating Principles

Reference

Most of communication HUBs other than StepTechnica's are designed to start sending after receiving the full packet length. This mechanism decreases the signal response speed of the entire system significantly, in particular in a system with inserted a lot of HUBs. As shown in Figure 1.11, the MKY02 sends the corrected packet while receiving the packet, which causes only a slight decrease in the signal response time of the entire system.

1.7.2 Signal Correction

To lengthen the total extension of a network cable, in general, a buffer is inserted to amplify signals.
When the baud rate is relatively low, buffer insertion is practical. However, when the baud rate is high (fast), buffer insertion is impractical because signals transformed by signal propagation along network cables cannot be corrected even if they are amplified.
The HLS uses a RZ signal format for signals constituting a packet. Even if the signal format of the received packet is transformed up to ±49%, the MKY02, which is a kind of HUB-IC that can be inserted into the HLS network, corrects the packet into a RZ signal format to send it (Fig. 1.12). Therefore, in a system in which a signal propagates via multiple HUBs, the user can extend the network cable length by "the number of inserted HUB + 1" without cumulative signal transformation (refer to ***"1.3.1 Extending Total Length of Network Cable"***).

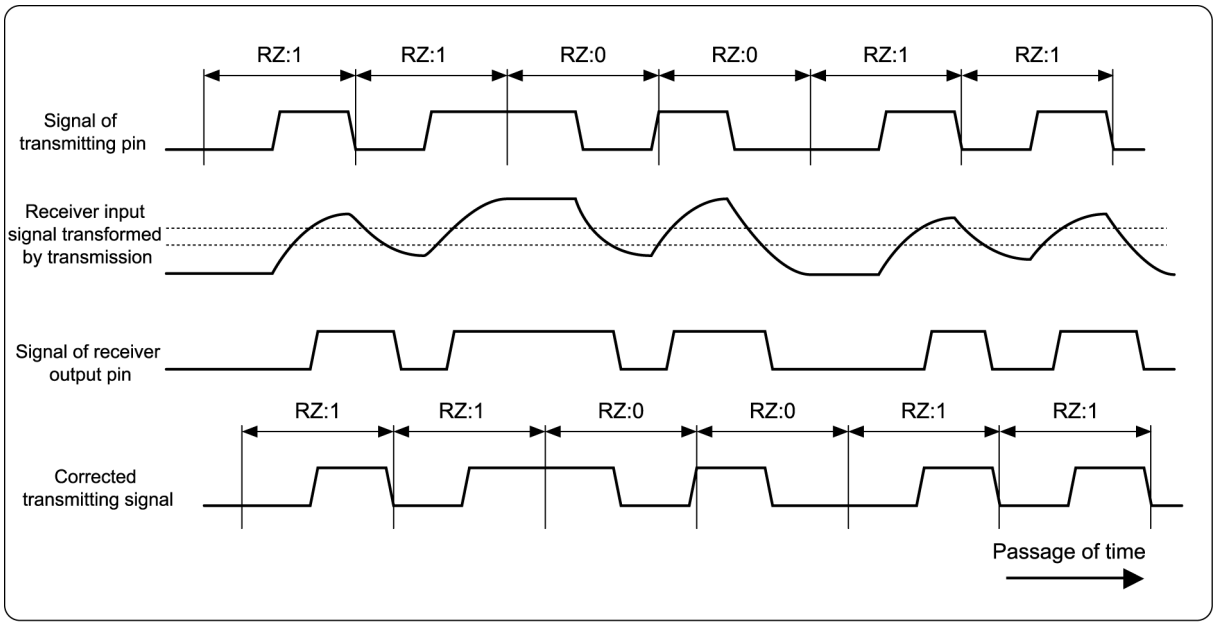


Fig. 1.12 Example of Signal Transformation and Correction

1.7.3 Detection of Error Packet

If the signal transformation of the received packet exceeds ±49%, the MKY02 recognizes the packet as an error packet. If the MKY02 detects an error in the received packet during sending, the MKY02 immediately stops sending to prevent improper correction and prevent the error packet from passing. When the MKY02 detects an error packet, it outputs pulses to the #LEDRZE pin for a given time and notifies the user.
Generally, the main causes for detection of an error packet are as follows:

(1) The center equipment and the terminal with satellite ICs were disconnected or system failure, or the network cables were disconnected.
(2) The packet format was damaged by external noise, and improper environments.
(3) The network performance reached the limit.
(4) Improper setup of the system or cables including the satellite address (SA) overlap.
(5) The system is operating in an extremely poor environment.

The detection frequency of error packets increases in the order of (1) to (5) above. For example, in (1), error packets are detected only when the terminal is disconnected, but in (5) above, error packets are detected frequently. If error packets are detected, the user needs to improve the system and environment.

1.8 Features of MKY02

This section describes the features of the MKY02 HUB-IC for the HLS.

(1) Supports full and half-duplex communication modes.
(2) Supports any baud rates up to 12.5 Mbps, including standard baud rates of 12, 6, and 3 Mbps.
(3) Has a dedicated port (port 0) connecting the center IC and seven ports (ports 1 to 7) connecting satellite ICs.
This can facilitate configuration of a HUB with two to eight ports using one MKY02.
(4) Has output pins that can turn on monitor LEDs when any one or more of the eight ports receive a packet.
(5) Has output pins for receiving monitor for each port to turn on monitor LEDs when eight ports receive a packet.
(6) Has output pins that can turn on monitor LEDs when any one or more of the eight ports receive an error packet.
(7) Has pins for cascade-connection that can add ports.
(8) Can be connected to both 5.0-V and 3.3-V TTL level signals using 5.0-V tolerant signal pins.
(9) Operates on 3.3-V single power supply and available in 0.5 mm pitch, 64 pins, TQFP.

The MKY02 can be used as the CUnet family of HUBs by setting the HC pin (pin 50). However, HLS and CUnet networks cannot be connected via the HUB. Note that the MKY02 is not a **"bridge"** for connecting networks using different family products.

For details of HUB of the CUnet family, refer to ***"MKY02 User's Manual (for CUnet)"***.

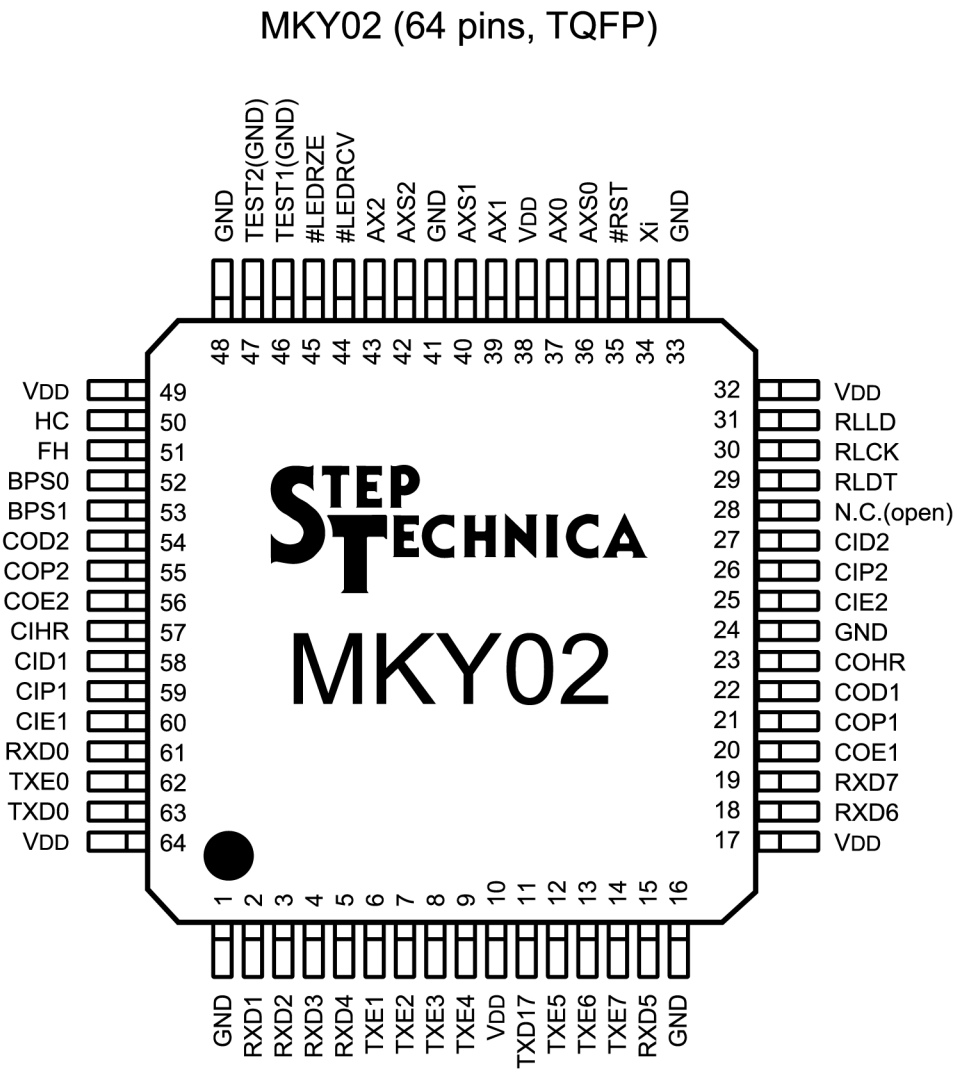
Chapter 2 MKY02 Hardware

This chapter describes the hardware such as pin assignment, pin functions, and input/output circuit type of the MKY02.

Chapter 2 MKY02 Hardware

This chapter describes the MKY02 hardware, such as pin assignment, pin functions, and I/O circuit type.

Figure 2.1 shows the MKY02 pin assignment.



Note: Pins prefixed with # are negative logic (active Low).
Leave the NC pin (pin 28) open.

Fig.2.1 MKY02 Pin Assignment

Table 2-1 lists the pin functions of the MKY02.

Table 2-1 Pin Functions of MKY02

Pin name	Pin No.	Logic	I/O	Function
RXD1 to RXD7	2 to 5 15, 18, 19	Positive	I	Input pins that input response packets (RP) from satellite ICs Connect to output pins target port receivers. When multiple ports input signals simultaneously, priority is given to pins with smaller port number. Fix these pins at High or Low when not in use.
TXE1 to TXE7	6 to 9 12 to 14	Positive	O	These pins go High when the ports of satellite ICs are enabled for sending Connect to gate pins of target port drivers. Leave these pins open when not in use.
TXD17	11	Positive	O	Output pin that output command packets (CP) to ports of satellite ICs Connect to input pins of port 1 to 7 drivers.
COE1	20	Positive	O	Output pin for cascade connection Connect to the CIE1 pin of the MKY02 for lower cascade connection. Leave this pin open when it is not cascade-connected.
COP1	21	Positive	O	Output pin for cascade connection Connect to the CIP1 pin of the MKY02 for lower cascade connection. Leave this pin open when is not cascade-connected.
COD1	22	Positive	O	Output pin for cascade connection Connect to the CID1 pin of the MKY02 for lower cascade connection. Leave this pin open when is not cascade-connected.
COHR	23	Positive	O	Output pin for cascade connection Connect to the CIHR pin of the MKY02 for lower cascade connection. Leave this pin open when is not cascade-connected.
CIE2	25	Positive	I	Input pin for cascade connection Connect to the COE2 pin of the MKY02 for lower cascade connection. Fix this pin at Low when is not cascade-connected.
CIP2	26	Positive	I	Input pin for cascade connection Connect to the COP2 pin of the MKY02 for lower cascade connection. Fix this pin at Low when it is not cascade-connected.
CID2	27	Positive	I	Input pin for cascade connection Connect to the COD2 pin of the MKY02 for lower cascade connection. Fix this pin at Low when is not cascade-connected.
N.C.	28	Positive	O	Be sure to leave this pin open.
RLDT	29	Positive	O	Data signal output pin for receive monitor LED drive circuit of individual port Leave this pin open when it is not used.
RLCK	30	Positive	O	Data clock output pin for receiving monitor LED drive circuit of individual port Leave this pin open when it is not used.
RLLD	31	Positive	O	Data load signal output pin for receiving monitor LED drive circuit of individual port Leave this pin open when it is not used.
Xi	34	Positive	I	External clock input pin (48 MHz recommended)
#RST	35	Negative	I	MKY02 hardware reset input pin Keep this pin Low for 10 or more clocks of the clock to be input to the AX0 pin immediately after power-on or when resetting hardware intentionally.
AXS0	36	Positive	O	Cascade clock output pin For details, refer to ***"3.2.2 Setting Cascade Clock and Baud Rate"***.
AX0	37	Positive	I	Cascade clock input pin For details, refer to ***"3.2.2 Setting Cascade Clock and Baud Rate"***.
AX1	39	Positive	I	Cascade clock input pin For details, refer to ***"3.2.2 Setting Cascade Clock and Baud Rate"***.
AXS1	40	Positive	O	Cascade clock output pin For details, refer to ***"3.2.2 Setting Cascade Clock and Baud Rate"***.
AXS2	42	Positive	O	Cascade clock output pin For details, refer to ***"3.2.2 Setting Cascade Clock and Baud Rate"***.

(Continue)

Table 2-1 Pin Functions of MKY02 (Continued)

Pin name	Pin No.	Logic	I/O	Function
AX2	43	Positive	I	Cascade clock input pin For details, refer to ***"3.2.2 Setting Cascade Clock and Baud Rate"***.
#LEDRCV	44	Negative	O	The LED driving output pin that keeps Low for a given time when an HLS packet is received from any port. This pin also keeps Low when a hardware reset is activated. Leave this pin open when it is not used.
#LEDRZE	45	Negative	O	The LED driving output pin that keeps Low for a given time when an error HLS packet is received from any port. This pin also keeps Low when a hardware reset is activated. Leave this pin open when it is not used.
TEST1	46	Positive	I	Be sure to connect this pin to GND pin (manufacturer test pin).
TEST2	47	Positive	I	Be sure to connect this pin to GND pin (manufacturer test pin).
HC	50	Positive	I	Be sure to fix this pin at High (This is input pin to set MKY02 as HLS HUB).
FH	51	Positive	I	Input pin that selects MKY02 communication mode Set this pin High when selecting Full-duplex mode, and Low when selecting half-duplex mode.
BPS0	52	Positive	I	Input pin that selects MKY02 baud rate For details, refer to ***"3.2.2 Setting Cascade Clock and Baud Rate"***.
BPS1	53	Positive	I	Input pin that selects MKY02 baud rate For details, refer to ***"3.2.2 Setting Cascade Clock and Baud Rate"***.
COD2	54	Positive	O	Output pin for cascade connection Connect to the CID2 pin of the MKY02 for higher cascade connection. Leave this pin open when it is not cascade-connected.
COP2	55	Positive	O	Output pin for cascade connection Connect to the CIP2 pin of the MKY02 for higher cascade connection. Leave this pin open when it is not cascade-connected.
COE2	56	Positive	O	Output pin for cascade connection Connect to the CIE2 pin of the MKY02 for higher cascade connection. Leave this pin open when it is not cascade-connected.
CIHR	57	Positive	I	Input pin for cascade connection Connect to the COHR pin of the MKY02 for higher cascade connection. Fix this pin at Low when it is not cascade-connected.
CID1	58	Positive	I	Input pin for cascade connection Connect to the COD1 pin of the MKY02 for higher cascade connection. Fix this pin at Low when it is not cascade-connected.
CIP1	59	Positive	I	Input pin for cascade connection Connect to the COP1 pin of the MKY02 for higher cascade connection. Fix this pin at Low when it is not cascade-connected.
CIE1	60	Positive	I	Input pin for cascade connection Connect to the COE1 pin of the MKY02 for higher cascade connection. Fix this pin at Low when it is not cascade-connected.
RXD0	61	Positive	I	Input pin that inputs command packet (CP) from center IC Connect this pin to output pin including receiver, etc.
TXE0	62	Positive	O	This pin goes High when sending to the center IC is enabled. Connect this pin to gate pin including driver, etc.
TXD0	63	Positive	O	Pin that sends response packet (RP) to center IC Connect this pin to drive input pin including driver, etc.
V_{DD}	10, 17, 32 38, 49, 64	---	---	Power pins for 3.3-V supply.
GND	1, 16, 24, 33, 41, 48	---	---	Power pins connected to 0V.

Note: Pins prefixed with # are negative logic (active Low).

Table 2-2 and Figure 2.2 shows the electrical ratings of the MKY02 pins.

Table 2-2 Electrical Ratings of MKY02

(#: Negative logic)

No	I/O	Name	Type
1	--	GND	--
2	I	RXD1	A
3	I	RXD2	A
4	I	RXD3	A
5	I	RXD4	A
6	O	TXE1	C
7	O	TXE2	C
8	O	TXE3	C
9	O	TXE4	C
10	--	V_{DD}	--
11	O	TXD17	C
12	O	TXE5	C
13	O	TXE6	C
14	O	TXE7	C
15	I	RXD5	A
16	--	GND	--
17	--	V_{DD}	--
18	I	RXD6	A
19	I	RXD7	A
20	O	COE1	C
21	O	COP1	C
22	O	COD1	C
23	O	COHR	C
24	--	GND	--
25	I	CIE2	A
26	I	CIP2	A
27	I	CID2	A
28	O	N.C.	C
29	O	RLDT	C
30	O	RLCK	C
31	O	RLLD	C
32	--	V_{DD}	--
33	--	GND	--
34	I	Xi	B
35	I	#RST	B
36	O	AXS0	C
37	I	AX0	B
38	--	V_{DD}	--
39	I	AX1	B
40	O	AXS1	C
41	--	GND	--
42	O	AXS2	C
43	I	AX2	B
44	O	#LEDRCV	D
45	O	#LEDRZE	D
46	I	TEST1	A
47	I	TEST2	A
48	--	GND	--
49	--	V_{DD}	--
50	I	HC	B
51	I	FH	B
52	I	BPS0	B
53	I	BPS1	B
54	O	COD2	C
55	O	COP2	C
56	O	COE2	C
57	I	CIHR	A
58	I	CID1	A
59	I	CIP1	A
60	I	CIE1	A
61	I	RXD0	A
62	O	TXE0	C
63	O	TXD0	C
64	--	V_{DD}	--

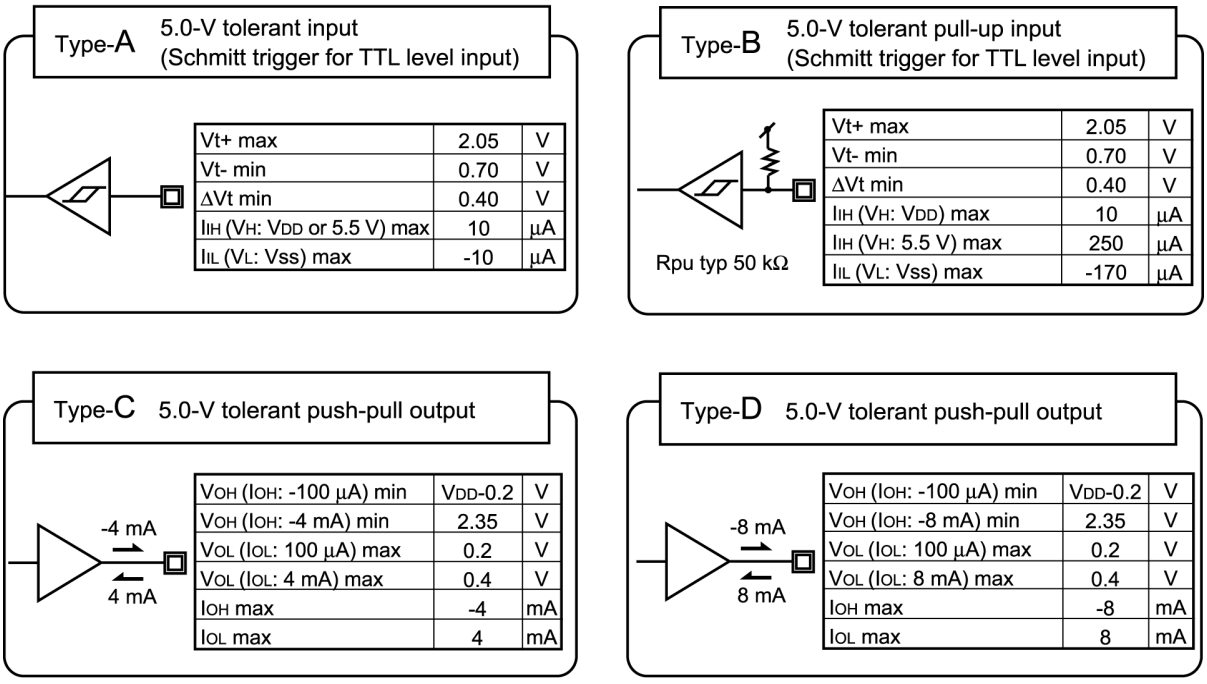


Fig. 2.2 Pin Electrical Characteristics in I/O Circuit Types of MKY02

Chapter 3 Single Connection of MKY02

This chapter describes the pin functions and how to connect pins required to design a "HUB with two to eight ports configured using one MKY02" inserted into the HLS.

3.1 Voltage Levels of Pins Connecting to Signal Pins 3-4
3.2 Supplying Driving Clock and Hardware Reset Signal..... 3-5
3.3 Connecting Network Interface.....3-8
3.4 Connecting Monitor LEDs.....3-11
3.5 Handling Cascade Connection Pins 3-15
3.6 Cautions for Designing HUB 3-15
3.7 Example Circuit for Single Connection of MKY02.....3-16

Chapter 3 Single Connection of MKY02

This chapter describes the pin functions and how to connect pins required to design a “HUB with two to eight ports configured using one MKY02” inserted into the HLS.

Before connecting the MKY02, be sure to connect the TEST1 pin (pin 46) and TEST2 pin (pin 47) to the GND pins.

In a “HUB configured using one MKY02” to be inserted into the HLS, be sure to fix the function select pin (HC: pin 50) at High.

Be sure to connect all GND pins (pins 1, 16, 24, 33, 41, 48) to the 0-V power supply and all V_{DD} pins (pin 10, 17, 32, 38, 49, 64) to the 3.3-V power supply. In addition, connect a 0.1 μF capacitor (10 V) (104) between adjacent V_{DD} pins and GND pins.

3.1 Voltage Levels of Pins Connecting to Signal Pins

All signal pins except those connected to VDD pins or GND pins of the MKY02 are tolerant types that can be connected to 5.0-V TTL signals.

(1) The pins can directly be connected to peripheral logic circuits driven by the 3.3-V power supply.

(2) The pins can be connected to TTL-level signals of peripheral logic circuits driven by the 5.0-V power supply.

A pull-up resistor can also be connected between the 5.0-V power supplies. However, if the input voltage of the MKY02 pins exceed 3.3 V, leakage current flows into the MKY02 pins (Fig. 3.1).

(3) Because the High-level voltages does not meet the 5.0-V CMOS input specifications, the MKY02 output pins cannot be connected to the CMOS input pins of peripheral logic circuits driven by the 5.0-V power supply. This pins cannot be connected even if a pull-up resistor is used between the 5.0-V power supplies (Fig. 3.1).

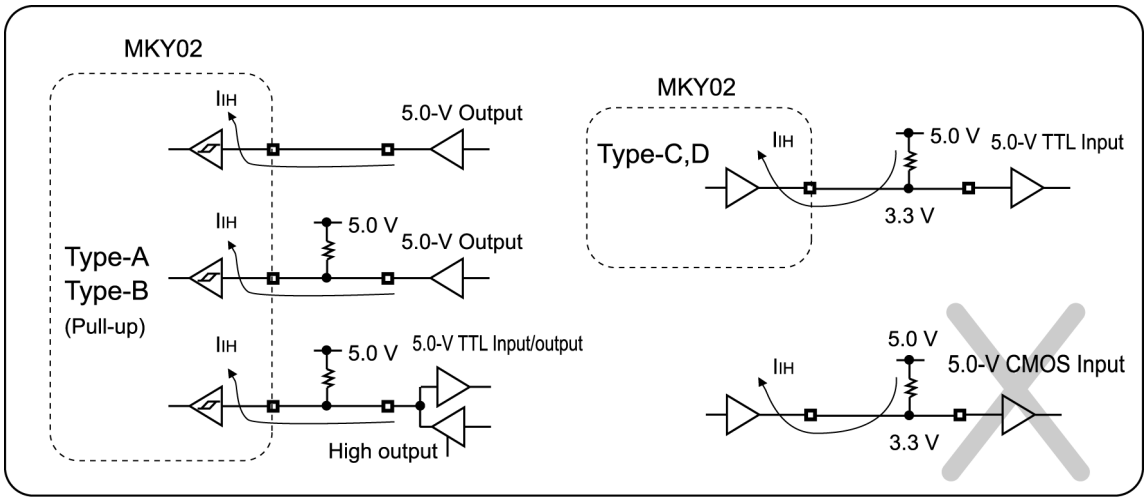


Fig. 3.1 Connection Causing Leakage Current

Caution

(1) When signal connecting to LSIs with different power-supply voltages, be sure to check the input/output electric specifications for the LSIs to connect.
Also, a voltage must not stay supplied to signal pins when the MKY02 is power-off.

(2) In the MKY02, if an external pull-up resistor is connected between non-pull-up input pin and the 5.0-V power supply, the voltage level rises up to 5.0 V.
Depending on the circuit conditions on the board with the MKY02, several tens of μs to several ms may be required for the voltage level to rise.
StepTechnica recommends pull-up resistors of 3 kΩ to 30 kΩ be connected.

(3) A pull-up resistor can be connected between the MKY02 output pins and the 5.0-V power supply. In this case, the High-level output is increased up to 3.3 V, but not to 5.0 V (Fig. 3.1).

3.2 Supplying Driving Clock and Hardware Reset Signal

This section describes how to supply a clock that drives the MKY02 and the hardware reset signal.

3.2.1 Supplying Driving Clock

Connect an oscillator-generated 48-MHz clock to the Xi pin (pin 34) of the MKY02 for driving clock. The specifications for supplying an external clock to the Xi pin are as follows:

(1) The upper frequency limit is 50 MHz and there is no lower frequency limit.
(2) For the electrical specifications of the Xi pin, refer to ***"Chapter 2 MKY02 Hardware"***.
(3) Connect a clock with a signal rise and fall time of 20 ns or less.
(4) Connect a clock with a minimum High-level or Low-level time of 5 ns or more.
(5) Connect a clock with a jitter component of:
- 250 ps or less at input frequency of 25 MHz or more
- 500 ps or less at input frequency of less than 25 MHz

(6) Connect a clock with a frequency accuracy of ±200 ppm or better.

A clock output by a commonly-used crystal oscillator meets the conditions (2) to (6) above.

3.2.2 Setting Cascade Clock and Baud Rate

The MKY02 uses three cascade clocks: AX0, AX1, and AX2. It has three cascade clock output pins: AXS0, AXS1, and AXS2 (Fig. 3.2).
A cascade clock is generated from the external clock supplied to the Xi pin based on a division ratio determined by the settings of the BPS0 and BPS1 pins.

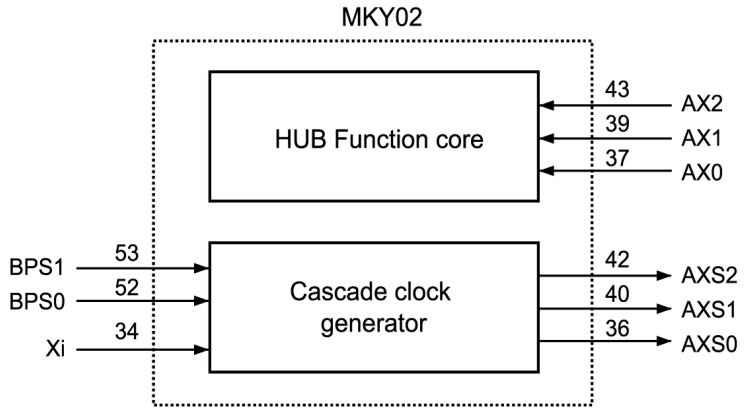


Fig. 3.2 Cascade Clock Generation

Conform the settings of the BPS0 (pin 52) and BPS1 (pin 53) pins to the baud rates of the HLS system into which the HUB is inserted.

To use a cascade clock, connect the output signal of the AXS0 pin to the AX0 pin, of the AXS1 pin to the AX1 pin, and of the AXS2 pin to the AX2 pin, as shown in Figure 3.3.

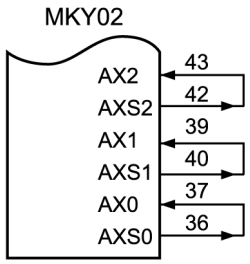


Fig. 3.3 Clock Connection

Table 3-1 shows the output frequencies of cascade clocks from the AXS0, AXS1, and AXS2 pins corresponding to the settings of the BPS0 and BPS1 pins when connecting a 48-MHz external clock to the Xi pin.

Table 3-1 Output Frequencies of Cascade Clocks

BPS1 pin	BPS0 pin	Baud rate	AXS0 pin	AXS1 pin	AXS2 pin
Hi	Hi	12 Mbps	48 MHz	12 MHz	6 MHz
Hi	Lo	6 Mbps	24 MHz	6 MHz	3 MHz
Lo	Hi	3 Mbps	12 MHz	3 MHz	1.5 MHz
Lo	Lo	1.5 Mbps	6 MHz	1.5 MHz	750 kHz

Reference The configuration to input cascade clocks output from the pins of the MKY02 to the pins of the MKY02 again enables cascade connection of the MKY02 described in ***"Chapter 4 Cascade Connection of MKY02"***. To design the "HUB with two to eight ports configured using one MKY02", connect the output signals as shown in Figure 3.3.

3.2.3 Hardware Reset

When a Low-level signal is input to the #RST (ReSeT) pin (pin 35), the MKY02 is hardware-reset. If a period in which the Low-level signal has been input is less than "one clock of the AX0-pin cascade clock", the signal is ignored to prevent a malfunction. To reset the MKY02 completely, the #RST pin must be kept Low for "10 clocks of the AX0-pin cascade clock" or more (Fig. 3.4) while supplying a cascade clock to the AX0 pin.

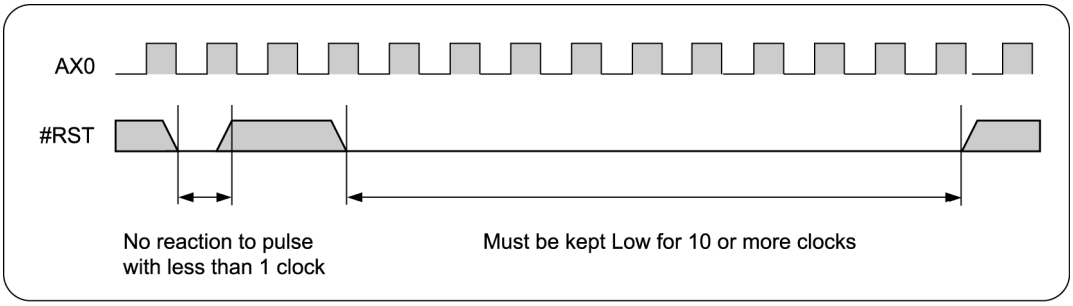


Fig. 3.4 Hardware Reset

Caution Design the circuit so that a hardware reset is surely activated immediately after MKY02 power-on.

3.3 Connecting Network Interface

This section describes connection of a network interface ("network I/F").
The MKY02 is a HUB IC with eight ports.
The MKY02 has one communication mode select pin common to all ports and eight sets of network I/F pins.
Port 0 has three network I/F pins: RXD0, TXE0, and TXD0.
Ports 1 to 7 correspond to the RXD1 pin to RXD7 pin and the TXEl pin to TXE7 pin, respectively, but there is no individual TXDn pin. There is one common TXD17 pin.

3.3.1 Selecting Communication Mode

When the specification of the HLS containing a HUB configured using the MKY02 is full-duplex mode, fix the FH pin (pin 51) at High. When the specification is half-duplex mode, fix the FH pin at Low (Fig. 3.5). In addition, conform the specification of the TRX (driver/receiver components) of the network cable connected to each port to the setting of the FH pin.

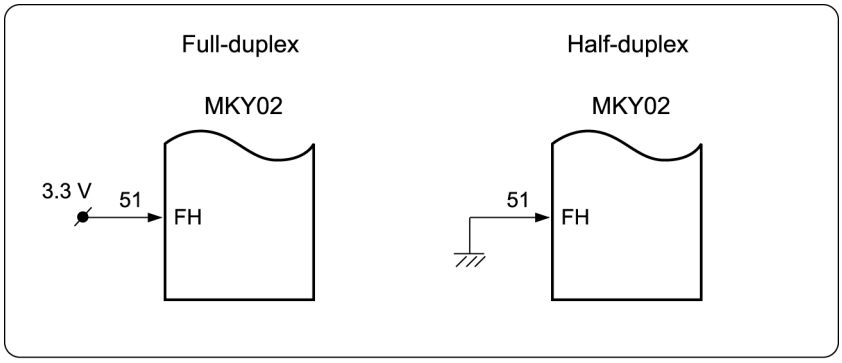


Fig. 3.5 Selecting Communication Mode

Reference In half-duplex mode, signals output from the TXD pins of the MKY02 may be input directly to the RXD pins of the MKY02 while the MKY02 is sending command packets (CP). The MKY02 is designed not to input data when the TXE pin is High when operated in half-duplex mode, so there is no problem.

3.3.2 Connection of Port 0

Connect the TRX of port 0 to three network I/F pins: RXD0, TXE0, and TXD0 (Fig. 3.6).

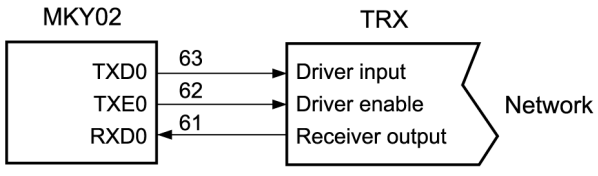


Fig. 3.6 TRX Connection of Port 0

3.3.3 Connection of Ports 1 to 7

Connect the output signals of the TXD17 pin to the driver input pins of the TRX (driver/receiver components) connected to ports 1 to 7. Connect the output signals of the transmit-enable pins (TXE1 to TXE7) of the MKY02 to the driver-enable input pins of the TRX connected to ports 1 to 7. Connect the receiver output signals of the TRX to the input pins (RXD1 to RXD7) of the MKY02 (Fig. 3.7).
When using selected ports of the satellite side in the HUB, use the ports in the order of lowest to highest port number. In this case, fix the input pins (RXDn) of unused ports at High or Low and leave the transmit-enable pins open (Fig. 3.8).

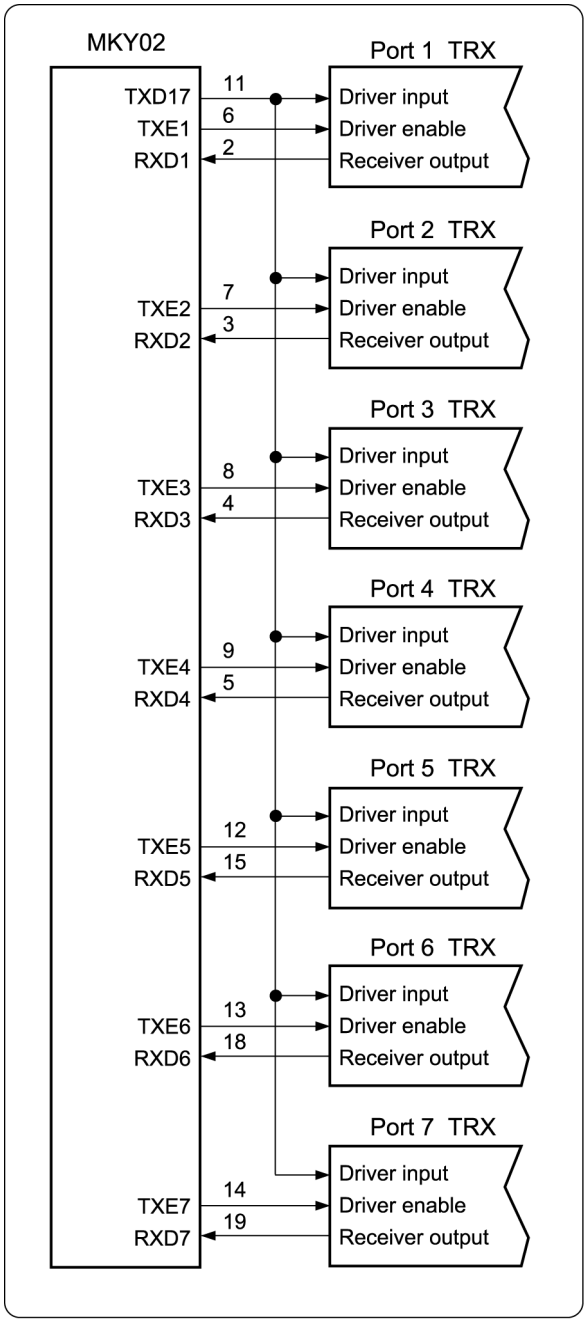


Fig. 3.7 TRX Connection of Ports 1 to 7

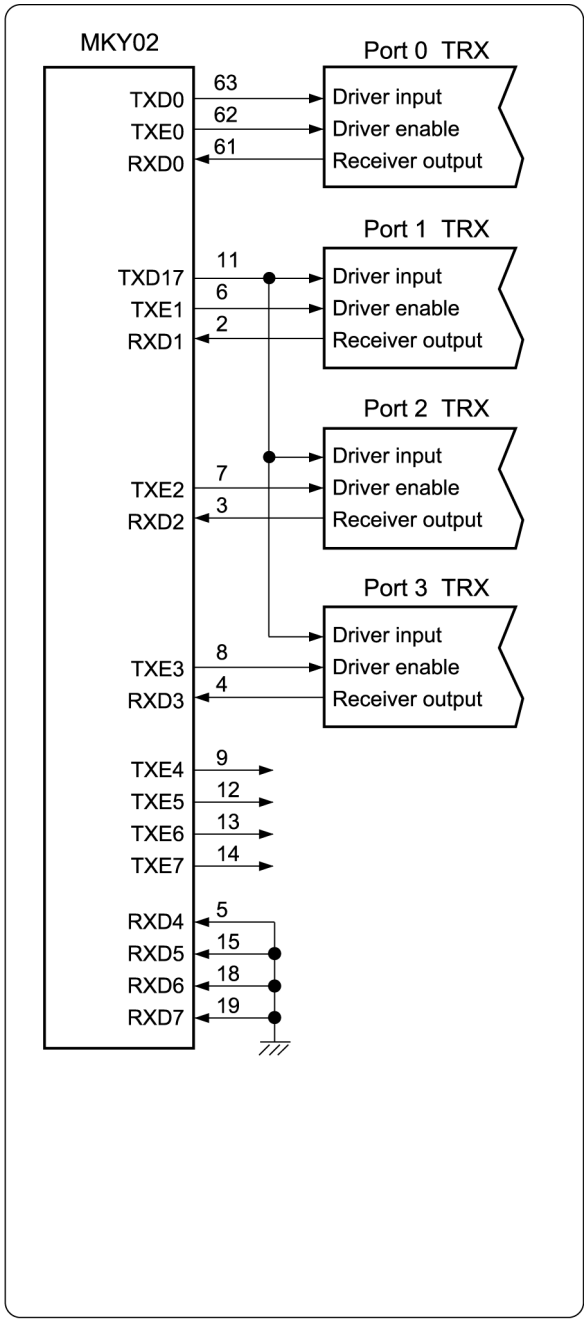


Fig. 3.8 TRX Connection of HUB with 4 Ports

3.3.4 Recommended Network Connection

Figure 3.9 shows a recommended network connection. The TRX (driver/receiver components) consists of an RS-485 driver/receiver (LSI driven at 5.0 V) and a pulse transformer. Recommended network cables include Ethernet LAN network cables (10BASE-T, Category 3 or higher) and shielded network cables. When operating the HLS, full-duplex mode requires two twisted-pair cables, and half-duplex requires one twisted-pair cable.

When HUB ports are connected at the end of the network cable, connect a termination resistor.

When HUB ports are connected in the intermediate position of the network cable, do not connect a termination resistor .

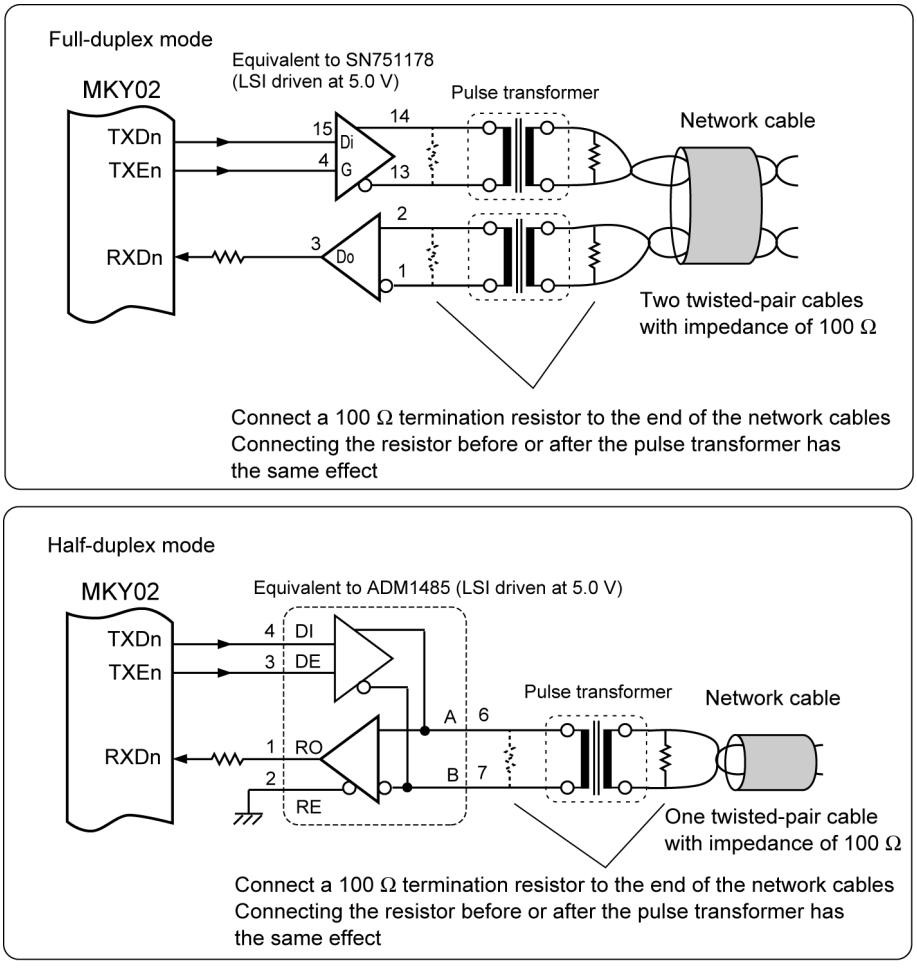


Fig. 3.9 Recommended Network Connection

Reference

Background information to help build a netwok and details of termination resistor are described in ***"Hi-speed Link System Technical Guide"***. For more information about how to select components or to get recommended components, visit our Web site at:

http://www.steptechnica.com/

3.4 Connecting Monitor LEDs

This section describes connection of monitor LEDs.

3.4.1 Packet Receive Monitor

The MKY02 has a #LEDRCV pin (pin 44) that outputs a Low level for a given time when any of the eight ports receives a packet. When an LED that goes on at Low level is connected to this #LEDRCV pin, it indicates that the HUB of the MKY02 is operating correctly.

This #LEDRCV pin has a drive capability of ±8 mA. If the LED can go on even at 8 mA or less, the connection shown in Figure 3.10 is possible. In this case, the hardware designer of a HUB needs to determine values of the current-limiting resistors according to the LED rating.

To test the LED, the #LEDRCV pin outputs a Low level for "500000 × TAX1" while a hardware reset is activated and after the hardware reset is canceled.

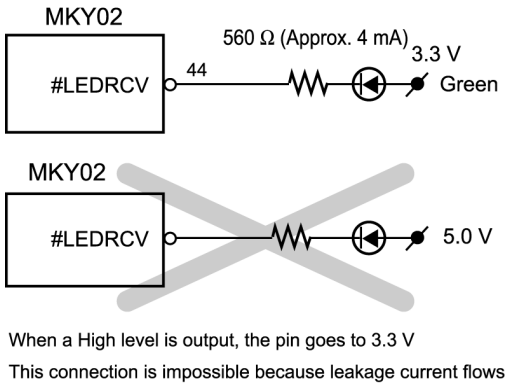


Fig. 3.10 Connection of Receive Monitor LED

The Low pulse output from the #LEDRCV pin is generated by a retriggerable one-shot multivibrator with a minimum time of "500000 × TAX1 (Xi = 48 MHz: 12 Mbps ≈ 43.69 ms, 6 Mbps ≈ 87.38 ms, 3 Mbps ≈ 174.76 ms)". Therefore, if any of the eight ports receives a packet again within a given time, the Low pulse width becomes wide. Even if 12 Mbps is selected as the baud rate of the MKY02, the narrowest time of the Low pulse is about 43.69 ms and the user can find that the LED is lit.

The green LED indicating stability should be connected to the #LEDRCV pin. When not used, leave this pin open.

Reference If the MKY02 is inserted into an HLS that operates correctly and continuously, the #LEDRCV pin outputs a Low level concecutively.

3.4.2 Packet Error Monitor

The MKY02 has a #LEDRZE pin (pin 45) that outputs a Low level for a given time when any port receives an error packet. When an LED that goes on at Low level is connected to this #LEDRZE pin, it indicates that any port of the MKY02 has received an error packet.

This #LEDRZE pin has a drive capability of ±8 mA. If the LED can go on even at 8 mA or less, the connection in Figure 3.11 is possible. In this case, the hardware designer of a HUB needs to determine the values of current-limiting resistors according to the LED rating.

To test the LED, the #LEDRZE pin outputs a Low level for "500000 × TAX1" while a hardware reset is activated and after the hardware reset is canceled.

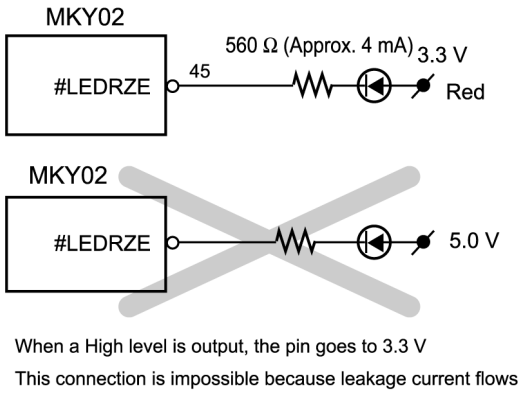


Fig. 3.11 Connection of Packet Error Monitor LED

The Low pulse output from the #LEDRZE pin is generated by a retriggerable one-shot multivibrator with a minimum time of "500000 × TAX1 (Xi = 48 MHz: 12 Mbps ≈ 43.69 ms, 6 Mbps ≈ 87.38 ms, 3 Mbps ≈ 174.76 ms)". Therefore, if any of the eight ports receives an error packet again within a given time, the Low pulse width becomes wide. Even if 12 Mbps is selected as the baud rate of the MKY02, the narrowest time of the Low pulse is about 43.69 ms and the user can find that the LED is lit.

The red LED to indicating an error should be connected to the #LEDRZE pin. When not used, leave this pin open.

Reference

The #LEDRZE pin may cause the LED to go on the following cases: If the cable connected to the HUB is near its length limit; if impedance mismatch occurs in network cables; if there is interference including external noise to external the system; Or if an error occurs in terminals or the center equipment. StepTechnica recommends the user put the LED where the user can check the LED indicator on the HUB easily.

3.4.3 Port Receive Monitor

The MKY02 has three output pins (RLDT, RLCK, RLLD) that can be used to add more port receive monitors corresponding to individual ports.

The RLDT pin (pin 29), RLCK pin (pin 30), and RLLD pin (pin 31) operate as follows:

(1) If a hardware reset is activated, all of the pins output a Low level.

(2) If a hardware reset is not activated, all of the pins output the signals shown in Figure 3.12 using a time of "$2^{17} \times$ TAX1" as one unit.

The MKY02 stores the status of the port that has received a packet for a time of "$2^{17} \times$ TAX1".

The MKY02 outputs the stored status to the RLDT pin as the signal format shown in Figure 3.12 for a next time of "$2^{17} \times$ TAX1".

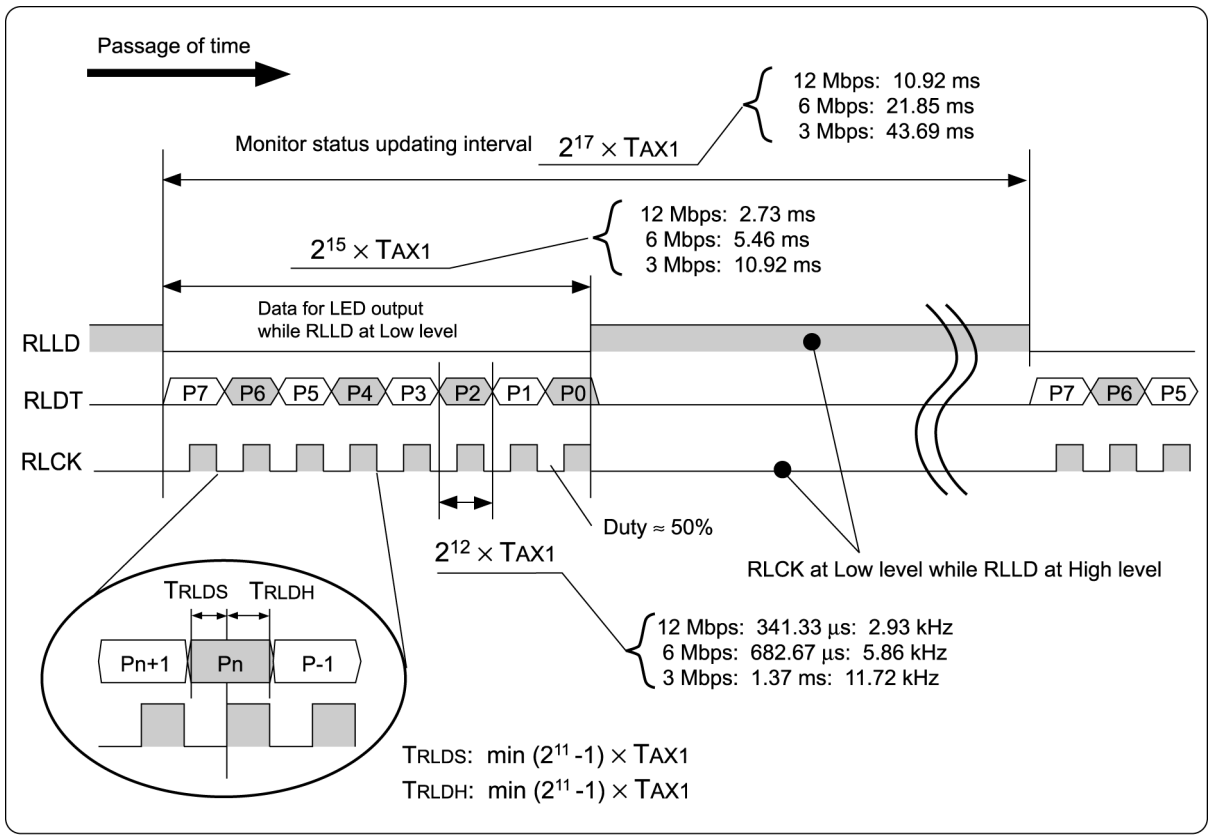


Fig. 3.12 RLLD, RLDT, and RLCK Outputs

As shown in Figure 3.13, adding an 8-bit shift register and 8-bit latch enables to add port receive monitors corresponding to individual ports. Figure 3.14 gives an example of the additional circuit for a HUB with four ports (when eight ports are not used).

When the MKY02 is inserted into an HLS that operates correctly and continuously, several cycles of packets are transmitted and received for a time of "$2^{17} \times$ TAX1". Therefore, the receive monitors corresponding to the ports connected to the center IC or satellite ICs may always be on.

The hardware designer of a HUB needs to determine the port receive monitor LEDs for individual ports and the values of current-limiting resistors shown in Figures. 3.13 and 3.14 to meet the output specifications for added latches. The green LED indicating stability should be connected as a port receive monitor LED.

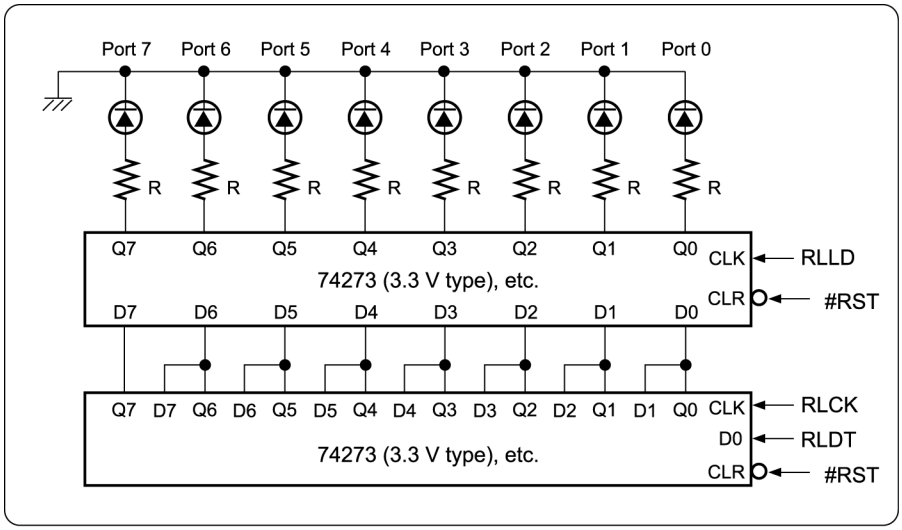


Fig. 3.13 8-port Receive Monitor

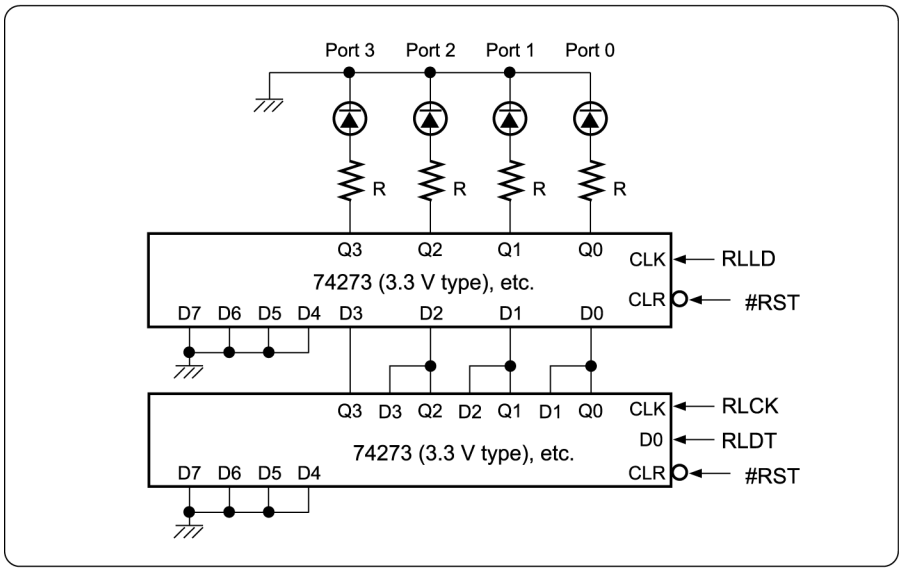


Fig. 3.14 4-port Receive Monitor

Leave the RLDT pin, RLCK pin, and RLLD pin open when an additional circuit is not connected to them.

Reference

If any of the receive monitor LEDs for individual ports go on, the LEDs described in ***"3.4.1 Packet Receive Monitor"*** also go on. Mounting both LEDs may cause confusion among the HUB users. The HUB designer or user system designer needs to determine the mounting of receive monitors.

3.5 Handling Cascade Connection Pins

When designing a HUB with two to eight ports configured using one MKY02, be sure to perform the following processing so that the cascade pins of the MKY02 do not function (Fig. 3.15).

(1) Fix the CIE1 pin (pin 60), CIP1 pin (pin 59), CID1 pin (pin 58), CIHR pin (pin 57), CIE2 pin (pin 25), CIP2 pin (pin 26), and CID2 pin (pin 27) at Low.

(2) Leave the COE1 pin (pin 20), COP1 pin (pin 21), COD1 pin (pin 22), COHR pin (pin 23), COE2 pin (pin 56), COP2 pin (pin 55), and COD2 pin (pin 54) open.

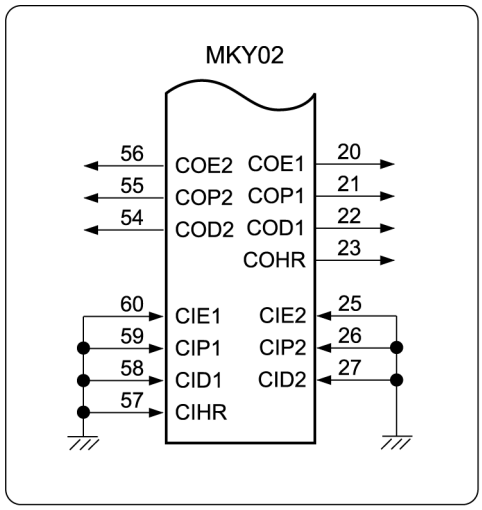


Fig. 3.15 Handling of Cascade Connection Pins

3.6 Cautions for Designing HUB

When designing a HUB configured using one MKY02, note the following points:

(1) When connecting the analog signal lines to the driver/receiver, pulse transformer, and network cable connector, do not cross each other or do not extend the anaog signla lines unnecessarily (except digital signal lines between the MKY02 and TRX components do not use overlong cables in order to avoid crosstalk (interference)).

(2) Connect a termination resistor when HUB ports are connected to the end of the network cable. Do not connect a termination resistor when HUB ports are connected in the intermediate position of the network cable.

(3) If ports 1 to 7 of the satellite side receive a packet simultaneously, priority is given to the port with smaller port number.

(4) The recommended pulse transformer (SPT-401 series) supports 3 to 12.5 Mbps. When designing a HUB using a baud rate other than these values, the designer needs to select an appropriate pulse transformer other than the SPT-401 series.

3.7 Example Circuit for Single Connection of MKY02

Figure 3.16 shows an example circuit for a HUB with eight ports (port 0 of the center side and ports 1 to 7 of the satellite side) in half-duplex mode. In the example circuit, 3, 6, and 12 Mbps can be set by DIP Switch (DIP-SW) and a receive monitor circuit has been added.

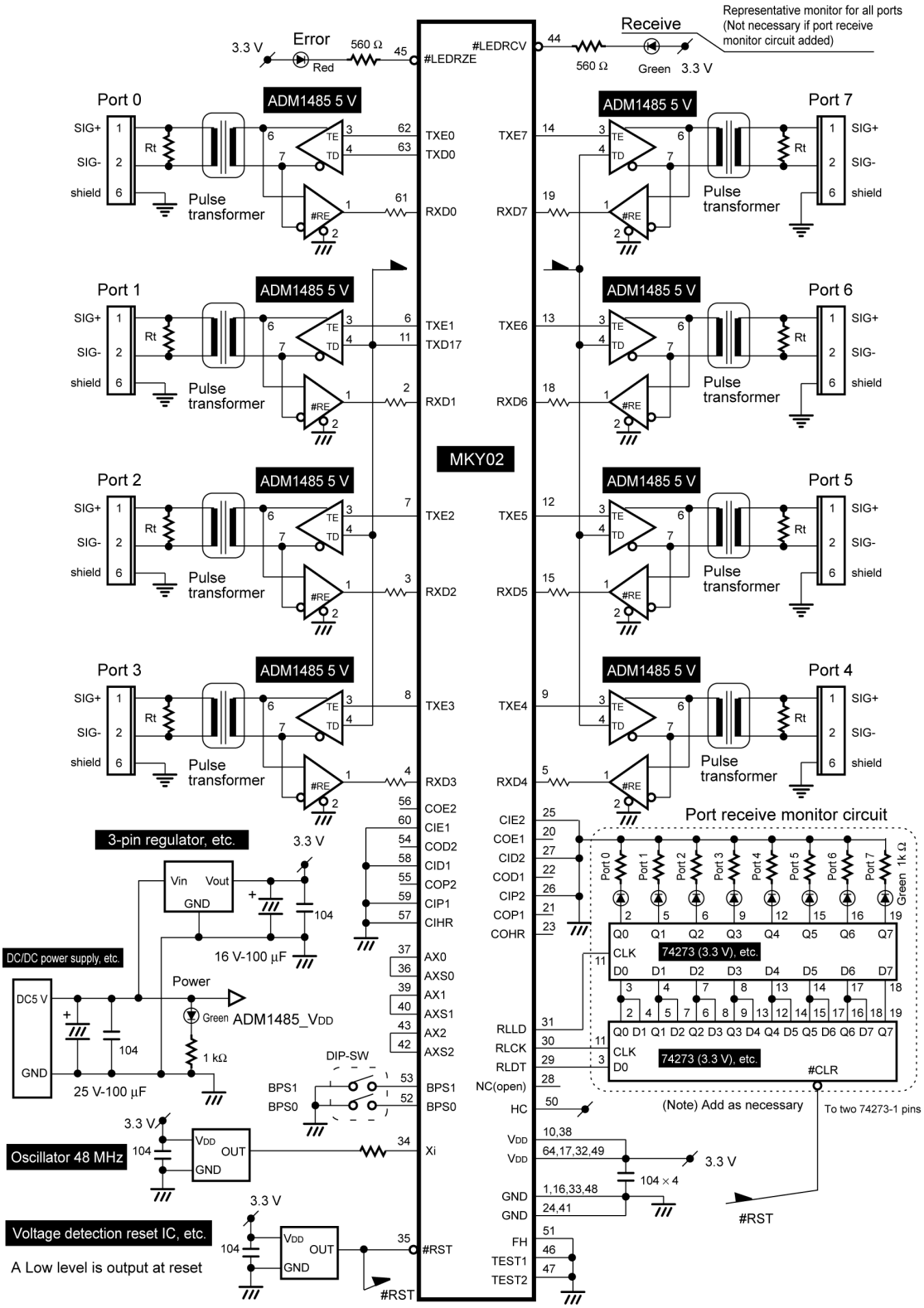


Fig. 3.16 Example of Single Connection Circuit in Half-duplex Mode

Figure 3.17 shows an example circuit for a HUB with eight ports in full-duplex mode.

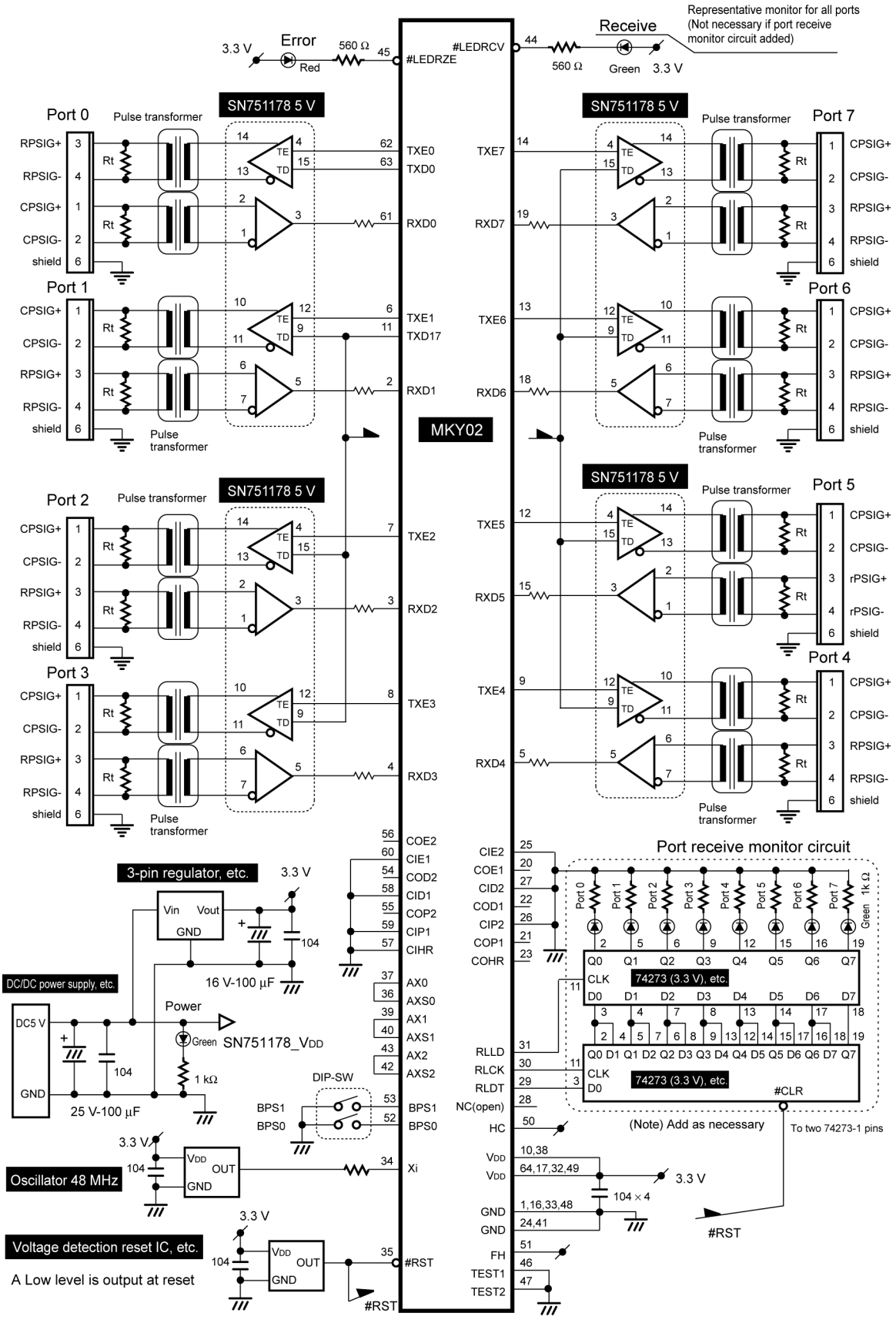


Fig. 3.17 Example of Single Connection Circuit in Full-duplex Mode

Chapter 4 Cascade Connection of MKY02

This chapter describes the pin functions and how to connect pins required to design a "multiport HUB (with nine or more ports) (refer to ***"1.6 Port Addition to HUB"***) configured using multiple MKY02s" to be inserted into the HLS.

4.1 Concepts of Port Addition 4-3

4.2 Practical Side of Cascade Connection 4-5

4.3 Example Circuit for Port-added HUB by Cascade Connection 4-10

Chapter 4 Cascade Connection of MKY02

This chapter describes the pin functions and how to connect pins required to design a "multiport HUB (with nine or more ports) (refer to ***"1.6 Port Addition to HUB"***) configured using multiple MKY02s" to be inserted into the HLS.

4.1 Concepts of Port Addition

This section describes the concepts of port addition to a HUB using multiple HUB-ICs.

4.1.1 Port Addition by Stacking Method

To add HUB ports using multiple MKY02s (HUB-ICs), "stacking" is suitable as shown in the Figure 4.1. "Stacking" is to connect one port of the sattelite side to the port 0 of the next MKY02.

The connection by "stacking" has the following demerits:

(1) Time lag (refer to ***"1.7.1 Receiving and Sending of Packets"***) increas in subsequent stacked ports.
(2) One satellite side port of the MKY02 cannot be used.

The increased time lag in the above (1) may be unuseful especially for the HLS used by a user system requiring high real-timeness.
In addition, some types of center ICs used in the HLS into which a HUB is inserted have restrictions on the "stacked" count, the number of available ports or the number of actually insertable HUBs may not meet the user system needs.

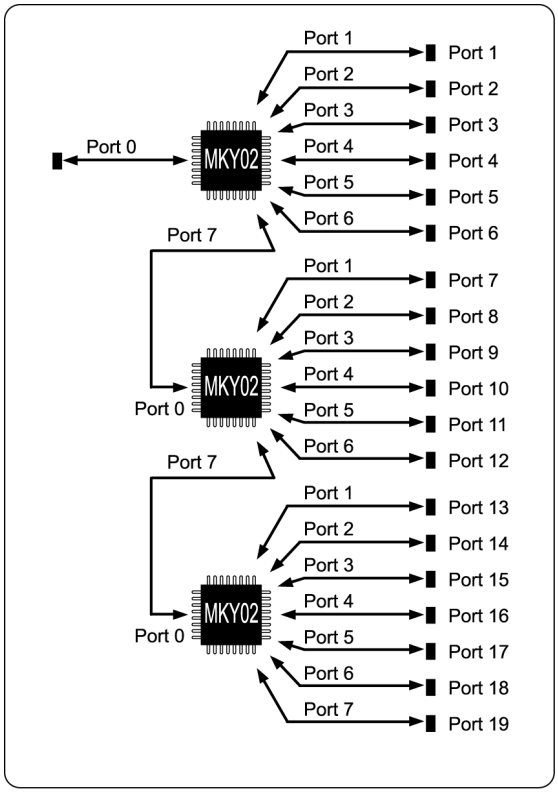


Fig. 4.1 Addition of Three-stacked Ports

4.1.2 Port Addition by Cascade Connection

The MKY02 has cascade connection pins to solve the problems caused by stacking.
If more than one MKY02 is used, the MKY02s can be handled as if they were one HUB-IC by connecting the cascade connection pins (Fig. 4.2).

If multiple MKY02s are cascade-connected, the time lag from receiving to sending packets described in ***"1.7.1 Receiving and Sending Packets"*** is consistent across any port and the HUB is identical to the HUB designed using one MKY02.

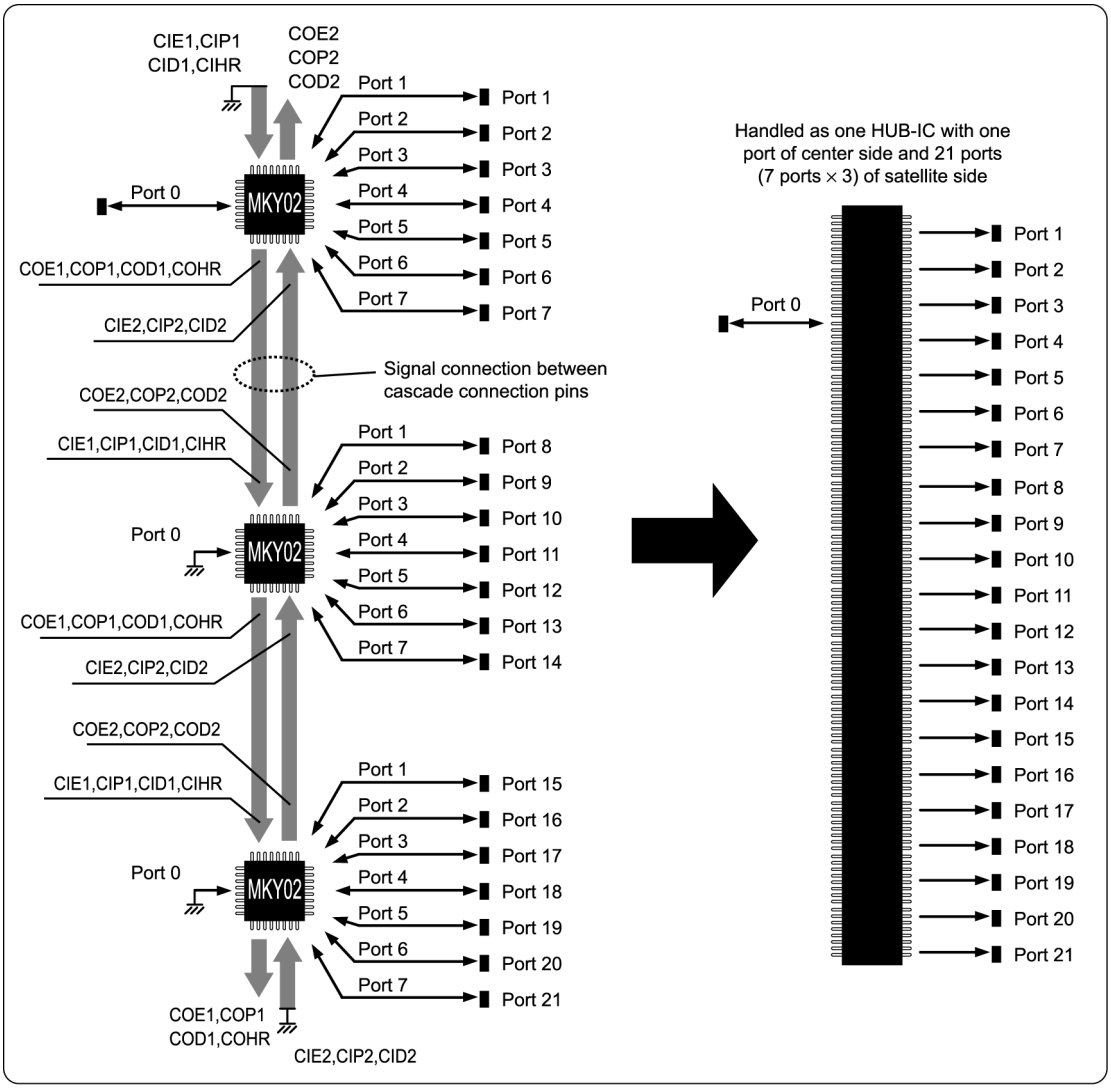


Fig. 4.2 Port Addition by Three Cascade Connections

4.1.3 Maximum Available Cascade Connections

When configuring a HUB for HLS, up to "9" MKY02s can be cascade-connected. Therefore, the HUB to which ports were added by cascade connection has a maximum number of one port of the center side and 63 ports (7 ports × 9) of the satellite side.

4.2 Practical Side of Cascade Connection

This section describes the practical side of cascade connection.

4.2.1 Cascade Pins

The MKY02 has the "priority" cascade pins: CIE1 (pin 60), CIP1 (pin 59), CID1 (pin 58), CIHR (pin 57), COE1 (pin 20), COP1 (pin 21), COD1 (pin 22) and COHR (pin 23), and the "reverse priority" cascade pins: CIE2 (pin 25), CIP2 (pin 26), CID2 (pin 27), COE2 (pin 56), COP2 (pin 55) and COD2 (pin 54).
To cascade-connect the MKY02, proceed as follows (refer to Fig. 4.3 and Fig. 4.4):

(1) Fix the cascade pins CIx1 (CIE1, CID1, CIP1) and CIHR of the highest-priority MKY02 at Low.
(2) Connect the cascade pins COx1 (COE1, COD1, COP1) and COHR of the MKY02 to the cascade pins CIx1 (CIE1, CID1, CIP1) and CIHR of the MKY02 with next "priority".
(3) Leave the cascade pins COx1 (COE1, COD1, COP1) and COHR of the MKY02 with the lowest priority open.
(4) Fix the cascade pins CIx2 (CIE2, CID2, CIP2) of the MKY02 with the lowest priority at Low.
(5) Connect the cascade pins COx2 (COE2, COD2, COP2) of the MKY02 to the cascade pins CIx2 (CIE2, CID2, CIP2) of the MKY02 with next "reverse-priority".
(6) Leave the cascade pins COx2 (COE2, COD2, COP2) of the MKY02 with highest-priority open.

Figure 4.2 shows that, of the three MKY02s, the MKY02 on the upper side is given the highest priority. If multiple MKY02s are cascade-connected, ports are assigned priorities in descending order. Therefore, number the satellite side ports according to priority (Fig. 4.2). For a center side port, use port 0 of the MKY02 with highest-priority and do not use port 0 of other MKY02 (Fig. 4.2).

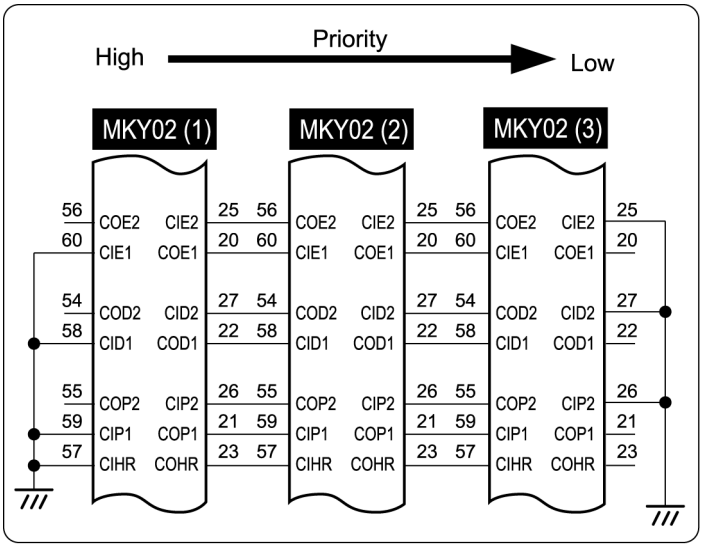


Fig. 4.3 Cascade Pin Connection for Three MKY02s

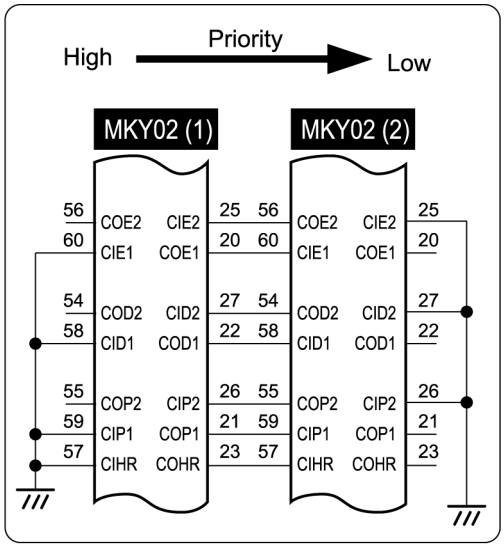


Fig. 4.4 Cascade Pin Connection for Two MKY02s

4.2.2 Operation of Cascade Connection Pins

The cascade connection pins of the cascade-connected MKY02 operate as follows:

(1) The packets which port 0 of the highest-priority MKY02 received are transmitted from ports 1 to 7 and are also transmitted from ports 1 to 7 of another MKY02 via the "priority" cascade connection pins (COE1, COP1, COD1, COHR, CIE1, CIP1, CID1, CIHR) (Fig. 4.5). At this time, the transmit packet data that is of an NRZ signal format is output from the COD1 pin and its minimum pulse width is a time of "2 × TBPS". The High-level status signals for packet transmission control are output from the COE1, COP1, and COHR pins.

(2) The packets which ports 1 to 7 of the non-highest-priority MKY02 received are transmitted from port 0 of the highest-priority MKY02 via the "reverse priority" cascade connection pins (COE2, COP2, COD2, CIE2, CIP2, CID2) (Fig. 4.6). At this time, the transmit packet data that is of an NRZ signal format is output from the COD2 pin and its minimum pulse width is a time of "2 × TBPS". The High-level status signals for packet transmission control are output from the COE2 and COP2 pins.

(3) The COE1, COP1, COD1, and COHR pins output a Low level in cases other than the above (1).

(4) The COE2, COP2, and COD2 pins output a Low level in cases other than the above (2).

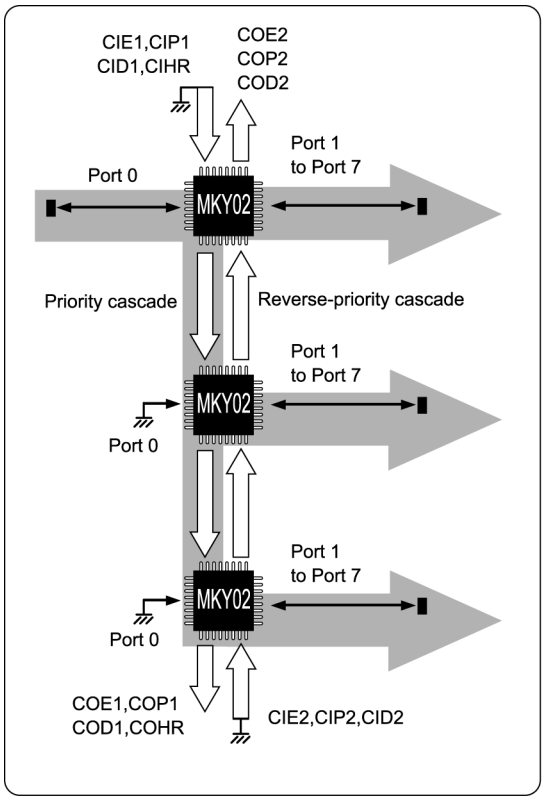


Fig. 4.5 Center Ports and Operation during Receiving

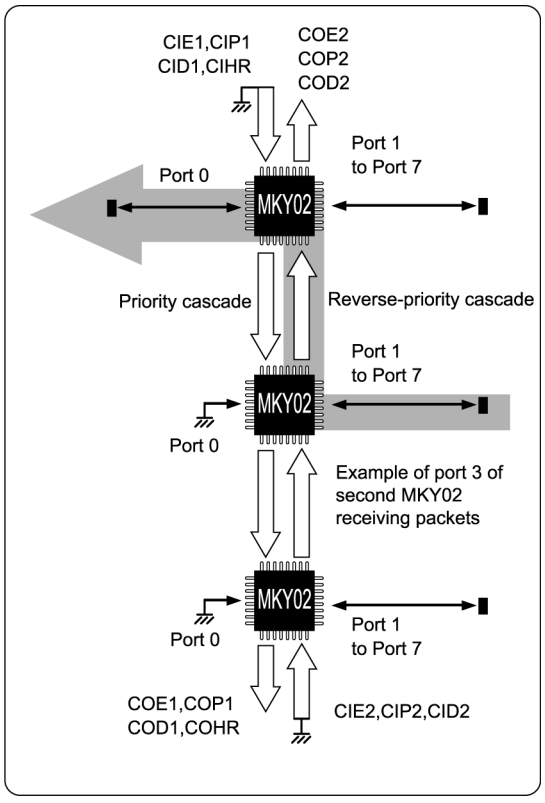


Fig. 4.6 Satellite Ports and Operation during Receiving

4.2.3 Connection of Cascade Clocks and Determination of Baud Rate

The MKY02 has a circuit which generates a cascade clock. A cascade clock for a baud rate suitable for the settings of the BPS1 and BPS0 pins from the clock to be input to the Xi pin (refer to ***"3.2.2 Setting Cascade Clock and Baud Rate"***).

When multiple MKY02s are is cascade-connected for use, the cascade clock generated by the highest-priority MKY02 is supplied to another MKY02 (Fig. 4.7). The baud rate set for the highest-priority MKY02 also applies to another MKY02.

Handle any MKY02 other than the highest-priority one as follows (refer to Fig. 4.7):

(1) Fix the Xi pin (pin 34) at a Low level or a High level (when left open, this pin can be fixed at a High level due to an internal pull-up resistor).

(2) Fix the BPS0 pin (pin 52) and BPS1 (pin 53) pin at a Low level or a High level (when left open, these pins can be fixed at a High level due to an internal pull-up resistor).

(3) Leave the AXS0 pin (pin 36), AXS1 pin (pin 40), and AXS2 pin (pin 42) pin open.

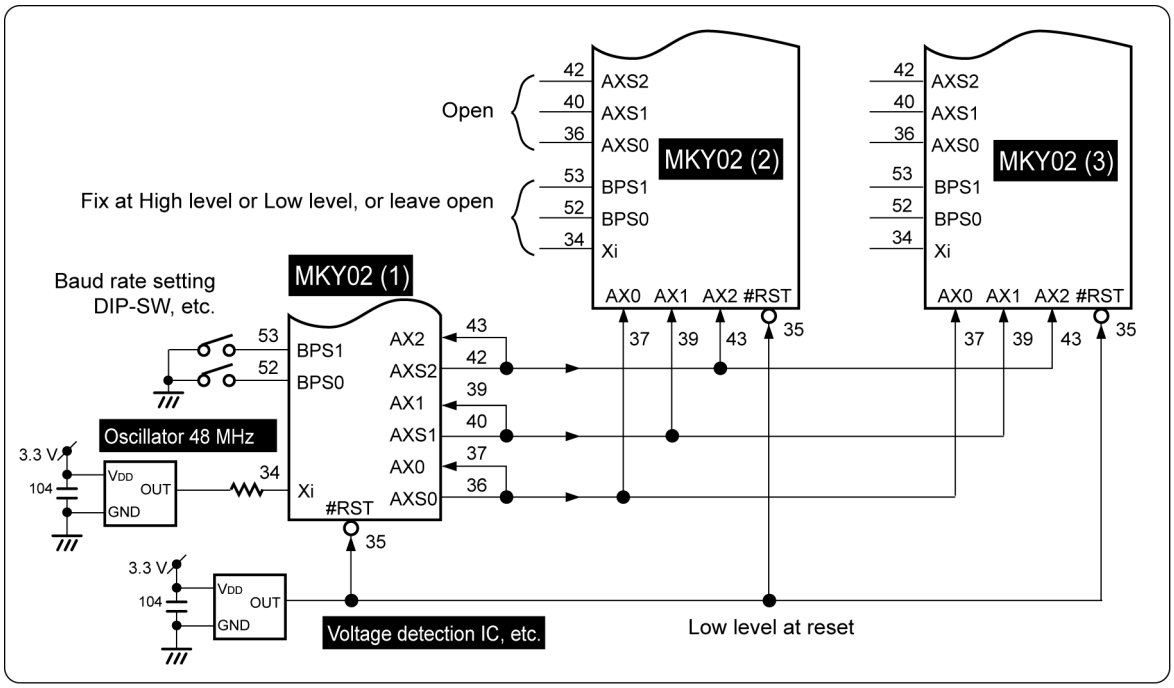


Fig. 4.7 Connection of Cascade Clocks

Caution In-phase clocks must be supplied to the AX0, AX1, and AX2 pins of all MKY02s to be cascade-connected. Therefore, when connecting cascade clocks, equalize the circuit pattern length of three clock lines. The circuit pattern length must be within 40 cm.

4.2.4 Connection of Hardware Reset Signal

Connect the hardware reset signal common to all MKY02s to be cascade-connected to the #RST pin (pin 35) (Fig. 4.7). For the specification of the hardware reset signal, follow the description in ***"3.2.3 Hardware Reset"***.

4.2.5 Selecting Communication Mode

When the specification for the HLS inserted the "port-added HUB" configured by cascade-connecting multiple MKY02s is full-duplex mode, fix the FH pin (pin 51) of all MKY02 at High. When the specification indicates half-duplex mode, fix the FH pin at Low (Fig. 4.8). In addition, conform the specification for the TRX (driver/receiver components) of the communication line connected to each port to the setting of the FH pin.

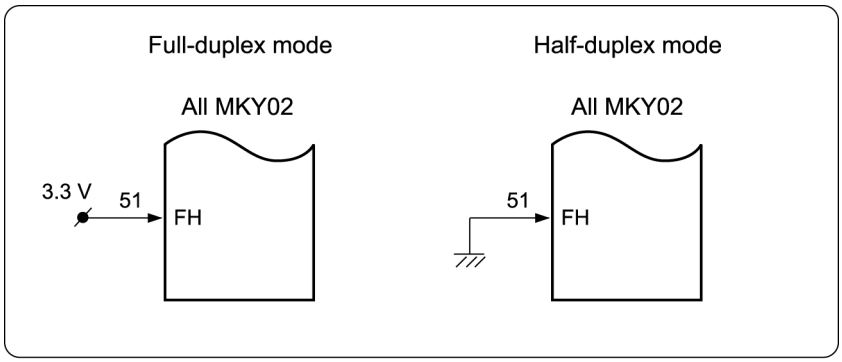


Fig. 4.8 Selection of Communication Mode

Caution The full-duplex mode and half-duplex mode cannot be mixed for cascade connection. Be sure to select the same mode for the MKY02s to be cascade-connected.

4.2.6 Connection of Each Port

In the "port-added HUB" configured by cascade-connecting multiple MKY02s, connect the TRX to port 0 of the highest-priority MKY02 (refer to ***"3.3.2 Connection of Port 0"***) and use it as a port to connect to the center IC.

Leave the TXE0 pin (pin 62) and TXD0 pin (pin 63) of any MKY02 other than the highest-priority one open.

Fix the RXD0 pin (pin 61) of any MKY02 other than the highest-priority one at a High or Low level.

Connect the TRX to each satellite port of multiple MKY02s (refer to ***"3.3.3 Connection of Ports 1 to 7"***) and use it as a port to connect to the satellite IC. For the handling of unused ports, refer to ***"3.3.3 Connection of Ports 1 to 7"***.

If multiple MKY02s are cascade-connected, ports are assigned priorities in descending order. Therefore, number the satellite ports according to priority (Fig. 4.2).

Reference Even if the TRX is connected to port 0 of any MKY02 other than the highest-priority one like port 0 of the highest-priority MKY02, there is no problem because no packet is received unless the communication lines are connected. This is effective when designing circuit boards for the single connection and cascade connection to be shared.

4.2.7 Placement of Monitor LEDs

The MKY02 has the function to connect various monitor LEDs (refert to ***"3.4 Connecting Monitor LEDs"***). In the port-added HUB by cascade-connecting multiple MKY02s, depending on the placement of monitor LEDs, the level of convenience increases in user system installation, network cable setup, and various maintenance works (refer to Fig. 4.9).

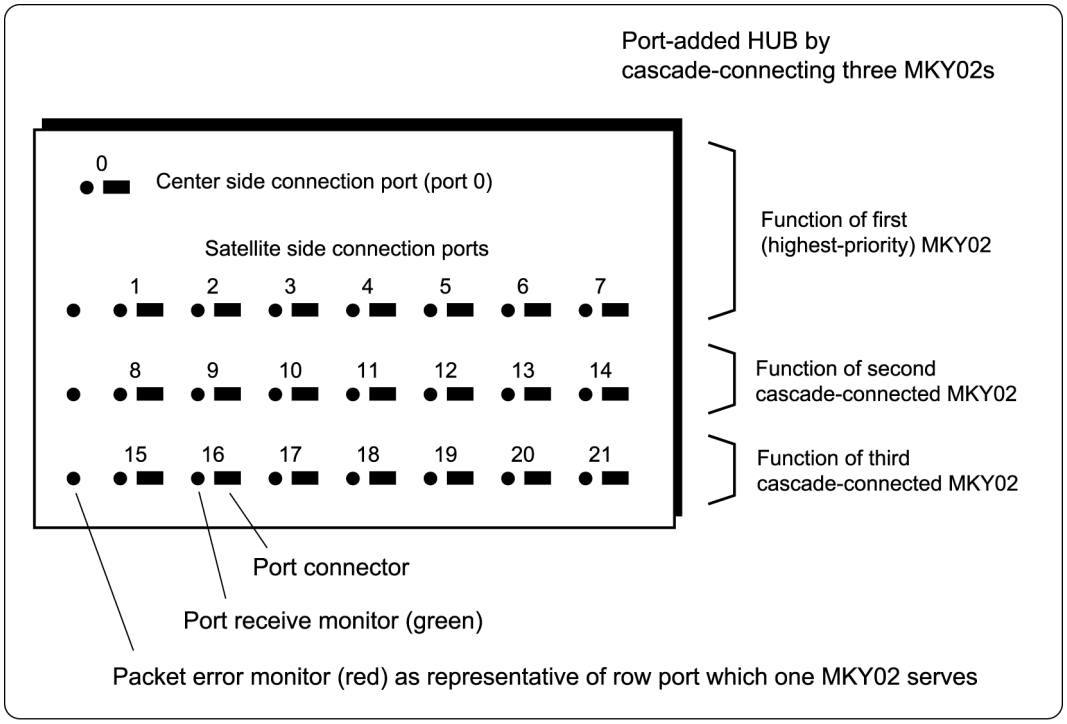


Fig. 4.9 Monitor Placement Example for Port-added HUB

StepTechnica recommends monitor LEDs be placed as follows.

(1) Place the port receive monitor LED beside each port connector (Fig. 4.9). For details of the port receive monitor, refer to ***"3.4.3 Port Receive Monitor"***.

(2) Place the packet error monitor LED as a representative of the port which one MKY02 serves by the number of MKY02 to be used (Fig. 4.9). For details of the packet error monitor, refer to ***"3.4.2 Packet Error Monitor"***.

The user who designs a HUB needs to determine the placement of monitor LEDs.

Reference

The packet receive monitor described in ***"3.4.1 Packet Receive Monitor"*** and the packet error monitor described in ***"3.4.2 Packet Error Monitor"*** function only when they receive packets from the input pins (RXD0 to RXD7) of each port. These monitors do not function for packets passing through the priority cascade connection signals and reverse-priority cascade connection signals described in ***"4.2.2 Operation of Cascade Connection Pins"***. Therefore, in the port-added HUB by cascade-connecting the MKY02, place the packet receive monitor and packet error monitor by the number of MKY02 to be used.

4.3 Example Circuit for Port-added HUB by Cascade Connection

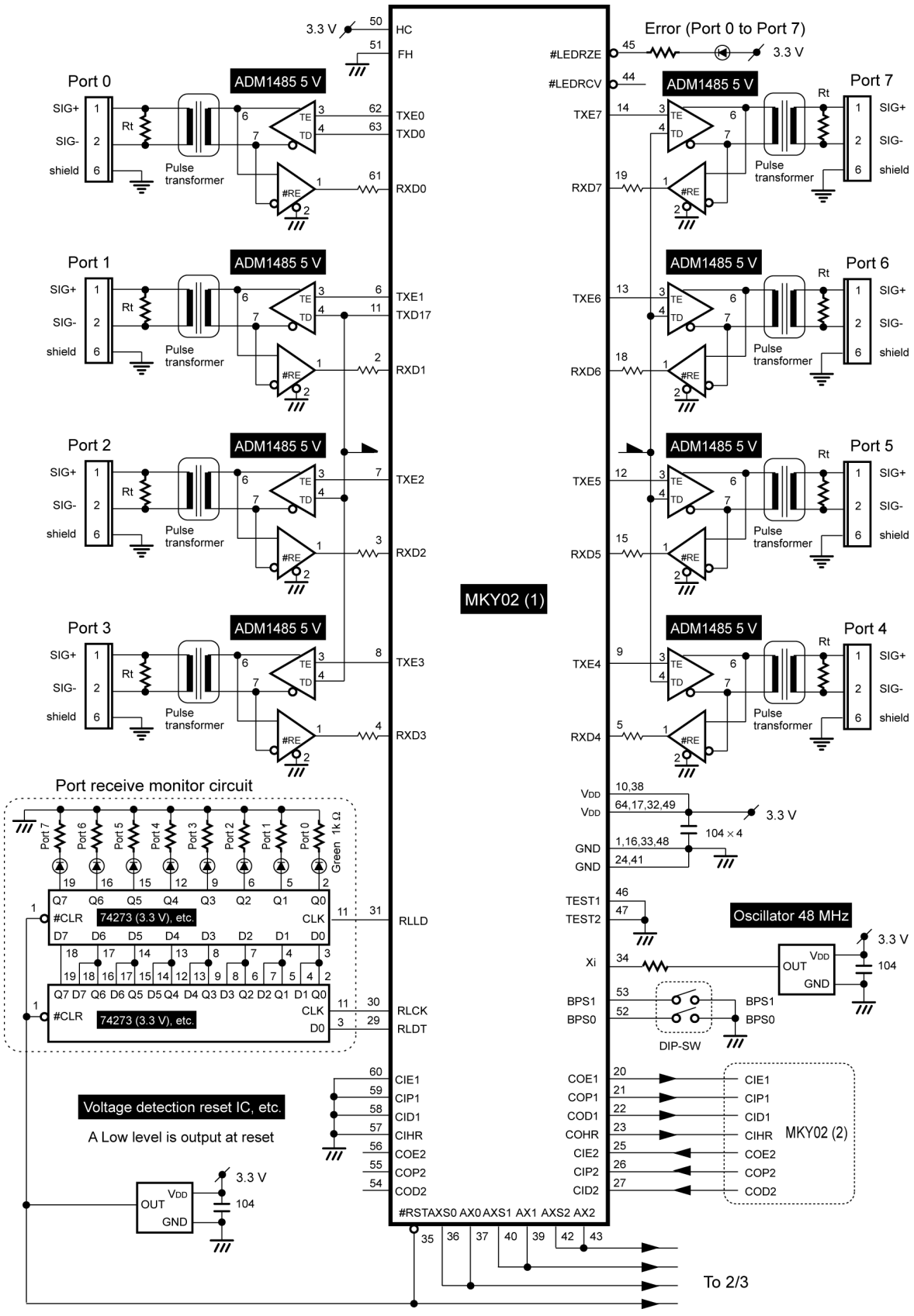


Fig. 4.10 Example Circuit for HUB with 22 Ports (1/3)

Figure 4.10 shows an example circuit for a HUB with 22 ports (port 0 of the center side and ports 1 to 21 of the satellite side) in half-duplex mode. In the example, the baud rates of 12 Mbps, 6 Mbps, and 3 Mbps can be set by DIP-SW and a port receive monitor circuit is added.

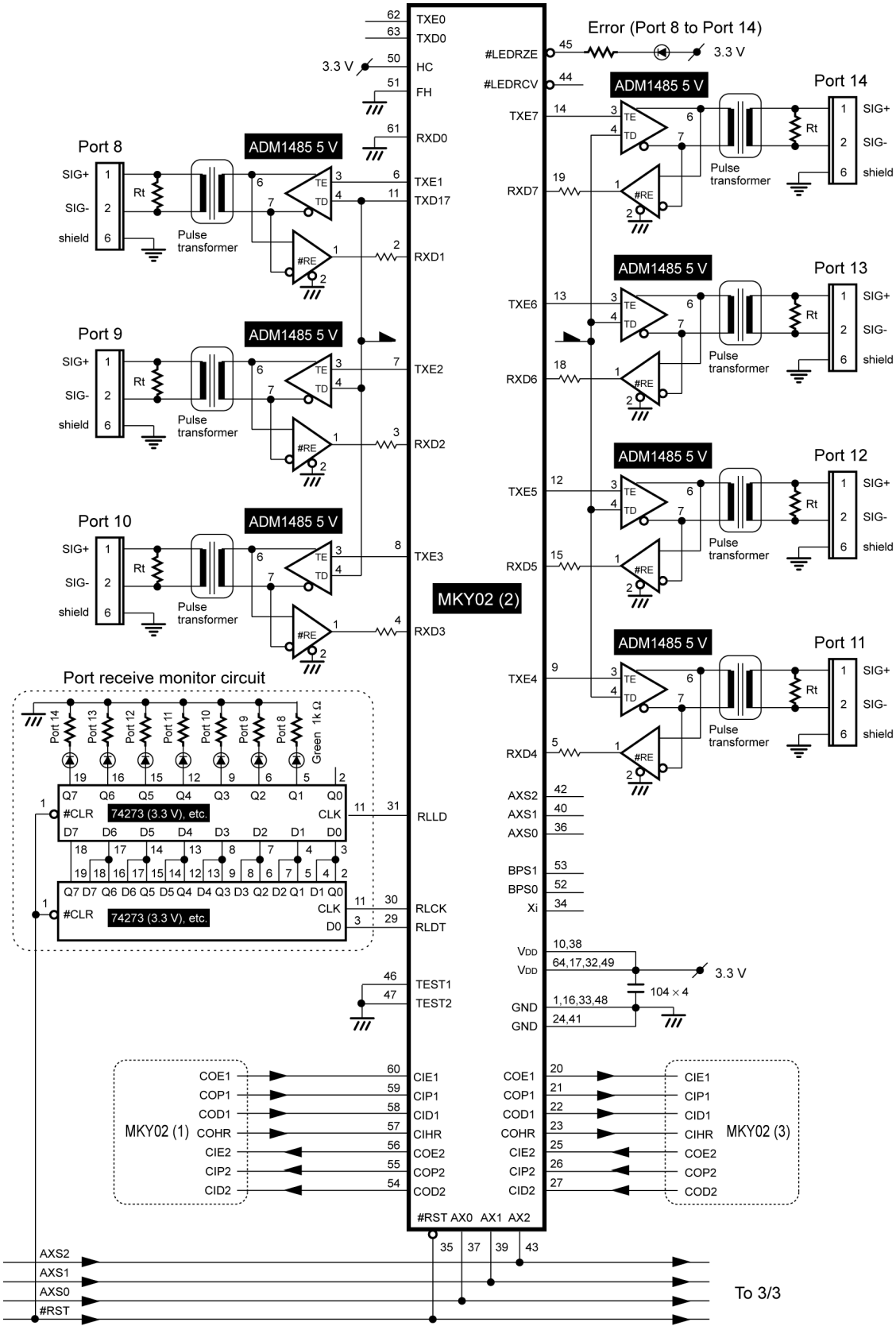


Fig. 4.10 Example Circuit for HUB with 22 Ports (2/3)

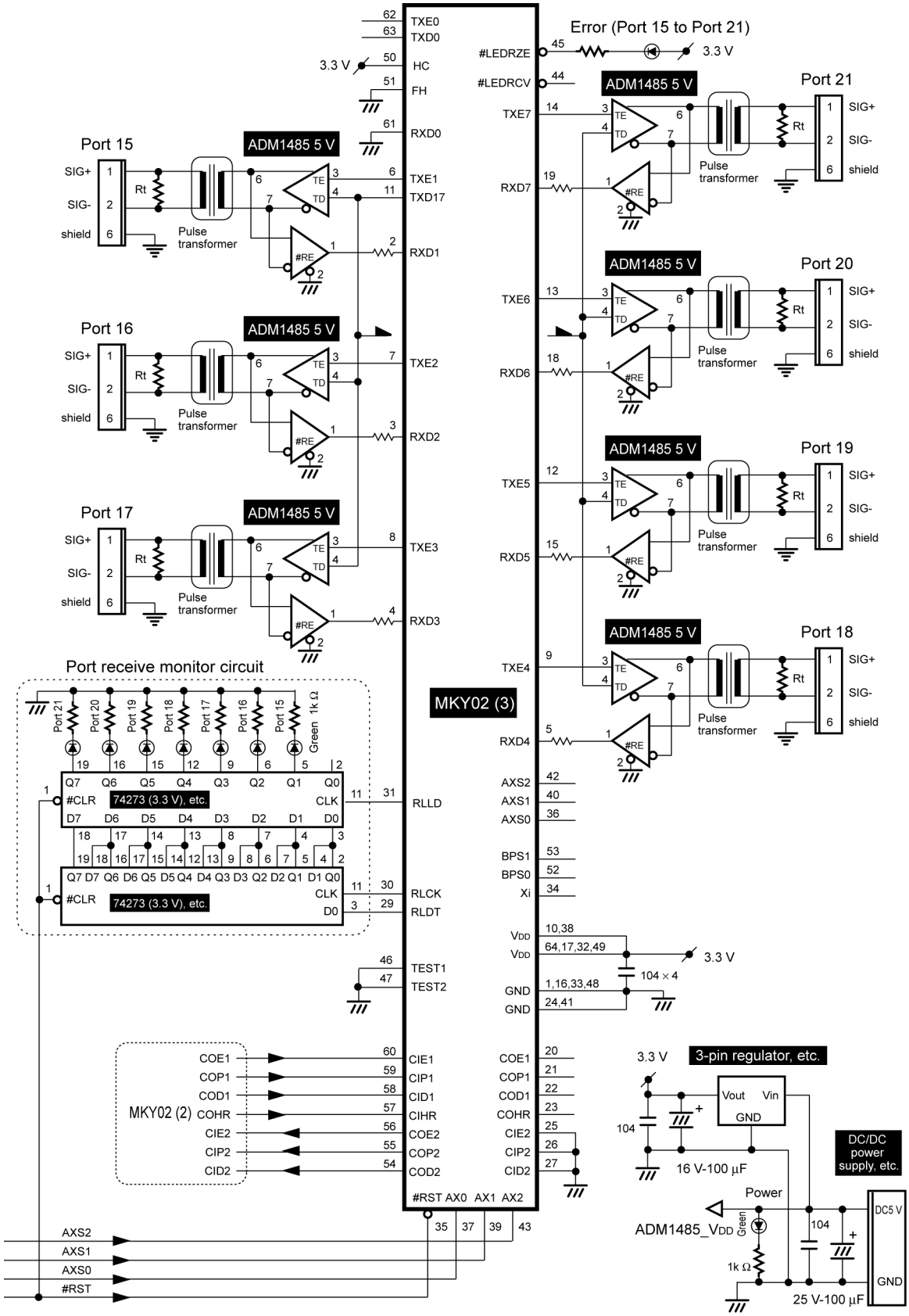


Fig. 4.10 Example Circuit for HUB with 22 Ports (3/3)

To design a HUB with 22 ports (port 0 of the center side and ports 1 to 21 of the satellite side) in full-duplex mode, change the connection of the TRX and FH pin (pin 51) in Figure 4.10 to those in Figure 4.11.

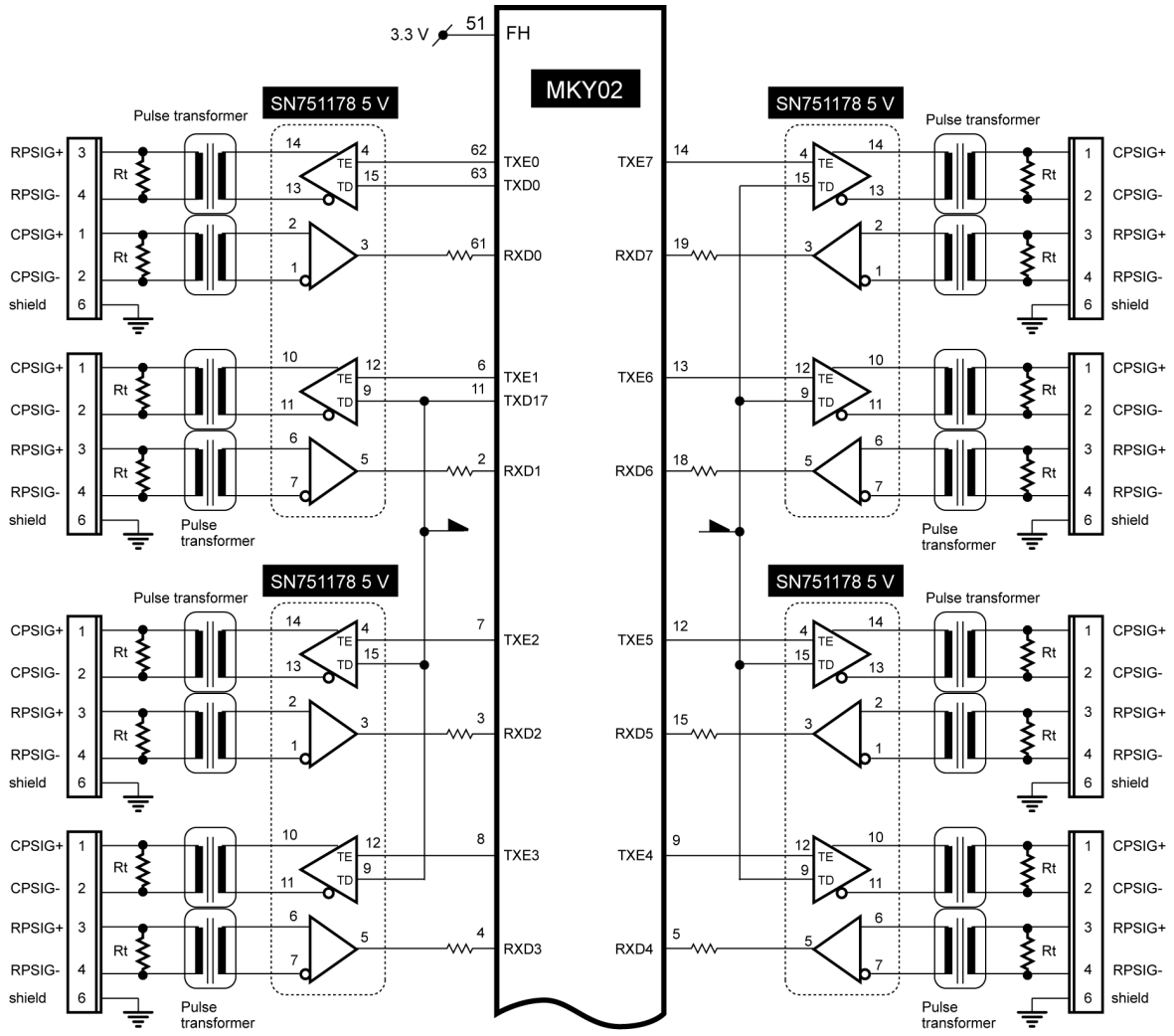


Fig. 4.11 Example of Connection in Full-duplex Mode

Chapter 5 Ratings

This chapter describes the ratings of the MKY02.

5.1 Electrical Ratings 5-3
5.2 AC Characteristics 5-3
5.3 Package Dimensions.....5-8
5.4 Recommended Soldering Conditions 5-9
5.5 Recommended Reflow Conditions 5-9

Chapter 5 Ratings

This chapter describes the ratings of the MKY02.

5.1 Electrical Ratings

Table 5-1 lists the absolute maximum ratings of the MKY02.

Table 5-1 Absolute Maximum Ratings

(Vss = 0 V)

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	-0.3 to +4.6	V
Input voltage	Vi	Vss-0.3 to +6.0	V
Output voltage	Vo	Vss-0.3 to +6.0	V
Signal pin input current	Ii	-6 to +6	mA
Peak output current	Iop	Peak ±20	mA
Allowable power dissipation	PT	345	mW
Operating temperature	Topr	-40 to +85	°C
Storage temperature	Tstg	-65 to +150	°C

Table 5-2 lists the electrical ratings of the MKY02.

Table 5-2 Electrical Ratings

(T_A = 25 °C Vss = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating power supply voltage	V_{DD}	---	3.0	3.3	3.6	V
Mean operating current	$V_{DD}A$	Vi = V_{DD} or Vss Xi = 50 MHz, AX0 = 50 MHz output open	---	55	65	mA
Mean operating current (operating at 6 Mbps)	$V_{DD}A$	Vi = V_{DD} or Vss Xi = 48 MHz, AX0 = 24 MHz output open	---	30	40	mA
Mean operating current (operating at 3 Mbps)	$V_{DD}A$	Vi = V_{DD} or Vss Xi = 48 MHz, AX0 = 12 MHz output open	---	18	25	mA
External input frequency	Fclk	Input to Xi pin	---	48	50	MHz
Input pin capacitance	Ci	V_{DD} = Vi = 0 V f = 1 MHz T_A = 25°C	---	6	---	pF
Output pin capacitance	Co		---	9	---	pF
I/O pin capacitance	Ci/o		---	10	---	pF
Rise/fall time of input signal	T_{IRF}	---	---	---	20	ns
Rise/fall time of input signal	T_{IRF}	Schmitt trigger input	---	---	30	μs

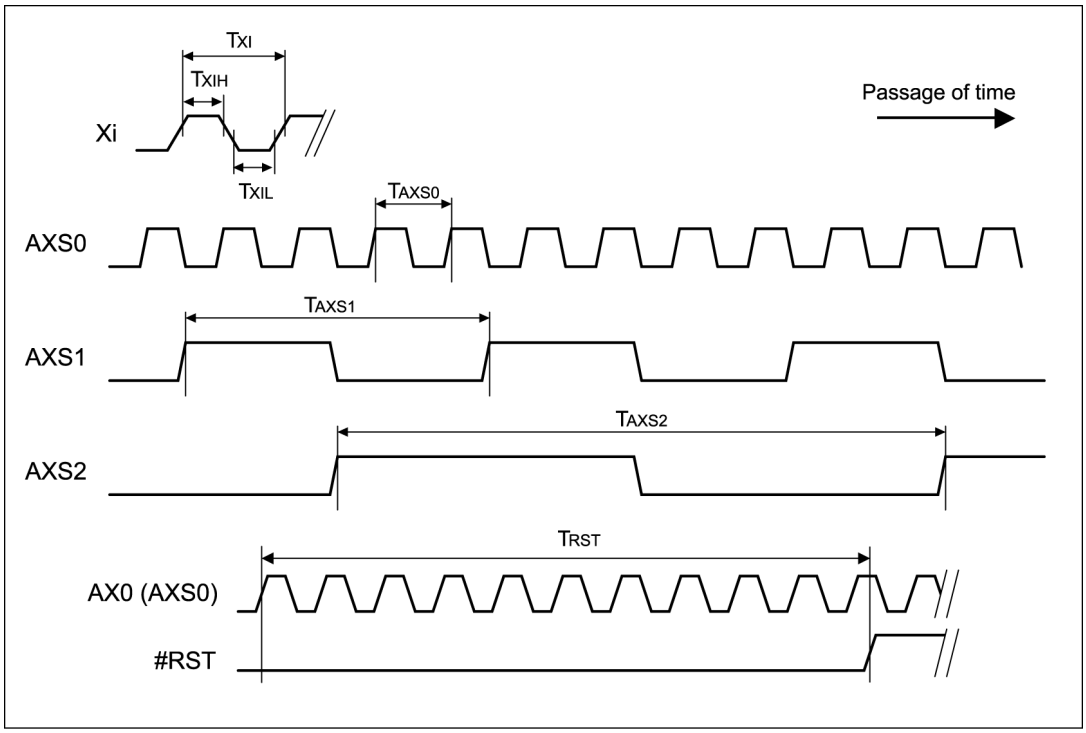
5.2 AC Characteristics

Table 5-3 lists the measurement conditions for AC characteristics of the MKY02.

Table 5-3 AC Characteristics Measurement Conditions

Symbol	Name	Value	Unit
C_{OL}	Output load capacitance	80	pF
V_{DD}	Power supply voltage	3.3	V
T_A	Temperature	25	°C

5.2.1 Clock and Reset Timing



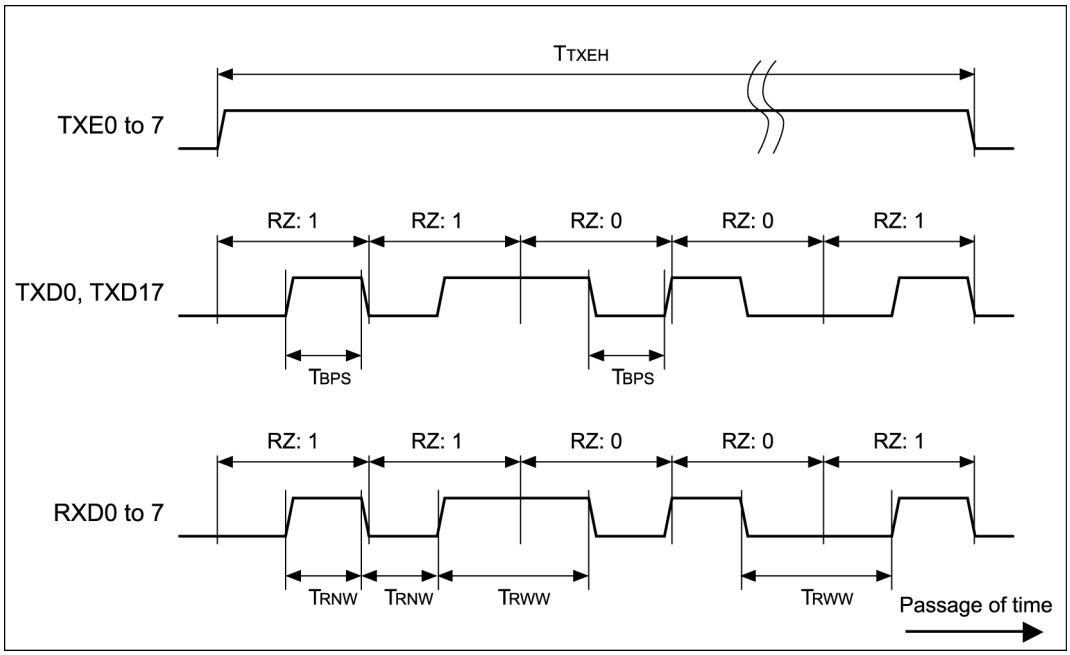
Symbol	Name	Min.	Max.	Unit
TXI	Clock period width	20	---	ns
TXIH	Clock High level width	5	---	ns
TXIL	Clock Low level width	5	---	ns
TRST	Reset enable Low level width	10 × TAX0	---	ns

BPS1 pin	BPS0 pin	TAXS0: TAX0	TAXS1: TAX1	TAXS2: TAX2	Unit	Remarks (Xi = 48 MHz)
Hi	Hi	TXI	4 × TXI	8 × TXI	ns	12 Mbps
Hi	Lo	2 × TXI	8 × TXI	16 × TXI	ns	6 Mbps
Lo	Hi	4 × TXI	16 × TXI	32 × TXI	ns	3 Mbps
Lo	Lo	8 × TXI	32 × TXI	64 × TXI	ns	1.5 Mbps

Reference

Input the clock output from AXS0 pin, to AX0 pin.
Input the clock output from AXS1 pin, to AX1 pin.
Input the clock output from AXS2 pin, to AX2 pin.

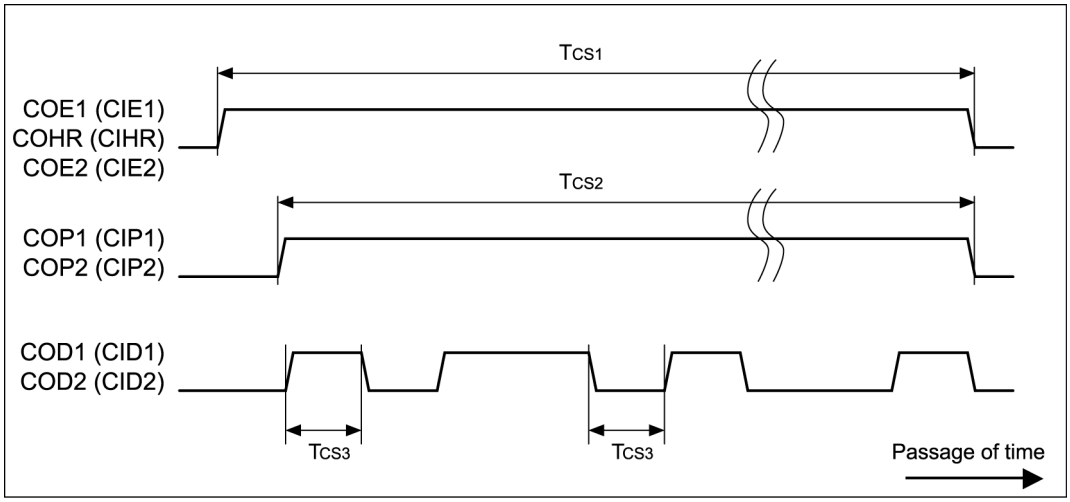
5.2.2 Port Pin Timing (TXE0 to 7, TXD0, TXD17, RXD0 to 7)



Symbol	Short pulse width of sendng signal	Unit
TBPS	TAX1 ±5	ns

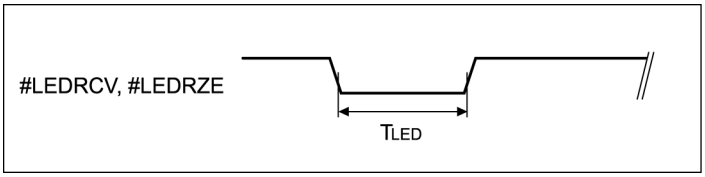
Symbol	Name	Min.	Typ.	Max.	Remarks
TTXEH	Period in which TXE pin goes High	--------	146 × TAX1	(146 × TAX1) + 5 ns	--------
TRNW	Short pulse width of input signal	0.51 × TAX1	1.0 × TAX1	1.49 × TAX1	Allowable pulse width as RZ signal
TRWW	Long pulse width of input signal	1.51 × TAX1	2.0 × TAX1	2.49 × TAX1	Allowable pulse width as RZ signal

5.2.3 Cascade Connection Pin Timing



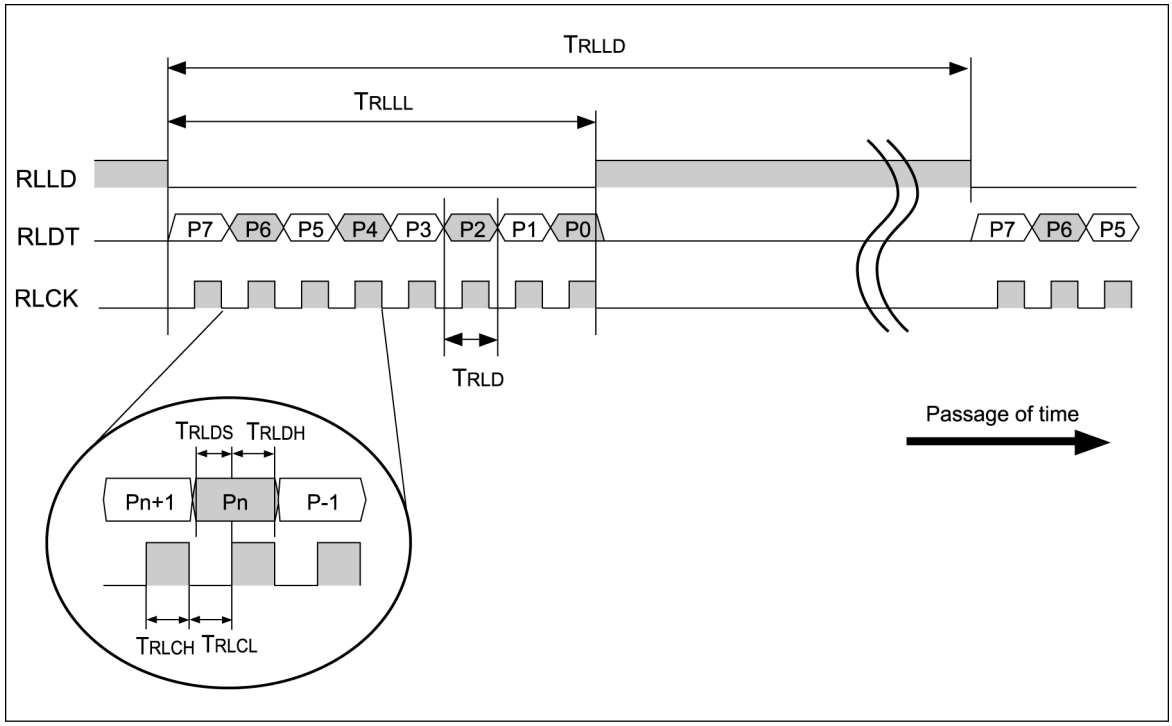
Symbol	Name	Min.	Typ.	Max.
TCS1	Cascade connection signal 1	--------	146 × TAX1	(146 × TAX1) + 5 ns
TCS2	Cascade connection signal 2	--------	142 × TAX1	(142 × TAX1) + 5 ns
TCS3	Cascade connection signal 3 (High or Low level short pulse width)	(2 × TAX1) - 5 ns	2 × TAX1	(2 × TAX1) + 5 ns

5.2.4 Output Timing of #LEDRCV and #LEDRZE Pins



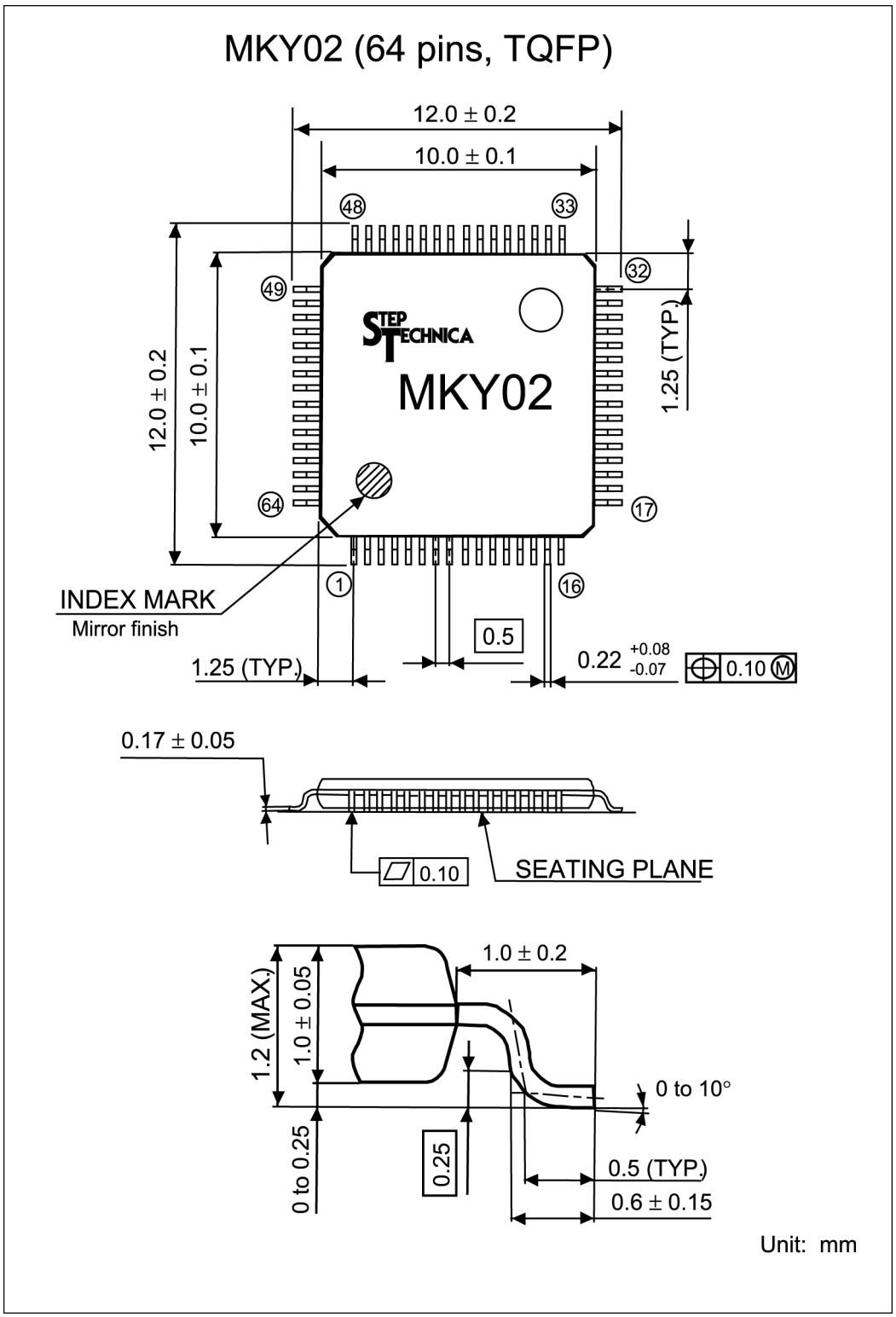
Symbol	Name	Min.	Max.	Unit
TLED	Pin Low level width	500,000 × TAX1	---	ns

5.2.5 Timing of Receive Monitor Pin of Individual Port (RLLD, RLDT, RLCK)



Symbol	Name	Min.	Typ.	Max.	Unit
TRLLD	Monitor status update interval	$(2^{17}-1) \times$ TAX1	$(2^{17}) \times$ TAX1	$(2^{17}+1) \times$ TAX1	ns
TRLLL	RLDT output time	$(2^{15}-1) \times$ TAX1	$(2^{15}) \times$ TAX1	$(2^{15}+1) \times$ TAX1	ns
TRLD	RLDT bit time	$(2^{12}-1) \times$ TAX1	$(2^{12}) \times$ TAX1	$(2^{12}+1) \times$ TAX1	ns
TRLDS	RLDT Setup	$(2^{11}-1) \times$ TAX1	$(2^{11}) \times$ TAX1	$(2^{11}+1) \times$ TAX1	ns
TRLDH	RLDT Hold	$(2^{11}-1) \times$ TAX1	$(2^{11}) \times$ TAX1	$(2^{11}+1) \times$ TAX1	ns
TRLCH	RLCK High level width	$(2^{11}-1) \times$ TAX1	$(2^{11}) \times$ TAX1	$(2^{11}+1) \times$ TAX1	ns
TRLCL	RLCK Low level width	$(2^{11}-1) \times$ TAX1	$(2^{11}) \times$ TAX1	$(2^{11}+1) \times$ TAX1	ns

5.3 Package Dimensions



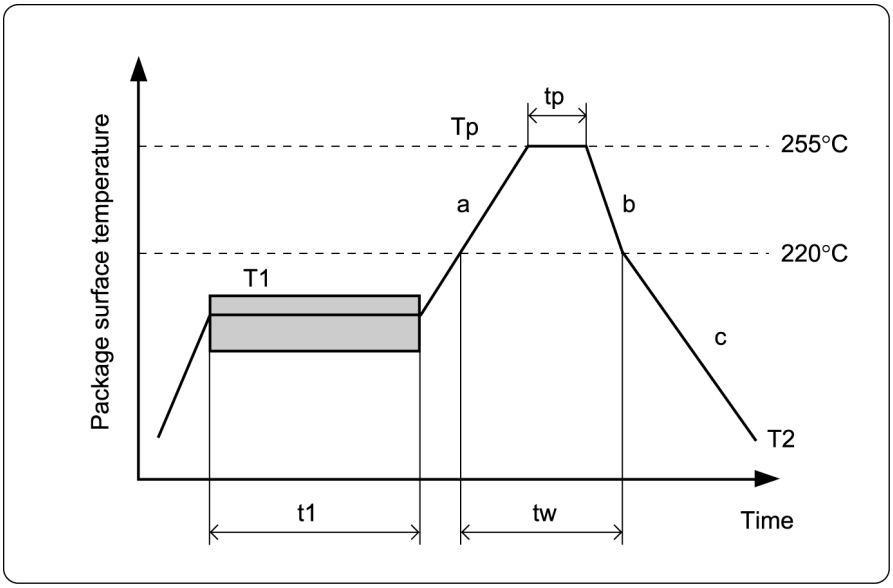
5.4 Recommended Soldering Conditions

Parameter	Symbol	Reflow	Manual soldering iron
Peak temperature (resin surface)	Tp	255°C max.	380°C max.
Peak temperature holding time	tp	10 s max.	5 s max.

Caution

(1) Product storage conditions: TA = 40°C max., RH = 85% for prevention of moisture absorption
(2) Manual soldering: Temperature of the tip of soldering iron 380°C, 5 s max.
(Device lead temperature 260°C, 10 s max., package surface temperature 150°C)
(3) Reflow: Twice max.
(4) Flux: Non-chlorine flux (should be cleaned sufficiently)
(5) Ultrasonic cleaning: Depending on frequencies and circuit board shapes, ultrasonic cleaning may cause resonance, affecting lead strength

5.5 Recommended Reflow Conditions



Parameter	Symbol	Value
Pre-heat (time)	t1	60 to 80/s
Pre-heat (temperature)	T1	150 to 190°C
Temperature rise rate	a	1 to 4°C/s
Peak condition (time)	tp	10 s max.
Peak condition (temperature)	Tp	255°C
Cooling rate	b	to 1.5°C/s
Cooling rate	c	to 0.5°C/s
High temperature area	tw	220°C, 60 s max.
Removal temperature	T2	≦ 100°C

Caution

The recommended conditions apply to hot-air reflow or infrared reflow. Temperature indicates resin surface temperature of the package.

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