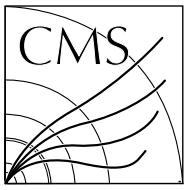
Available on CMS information server

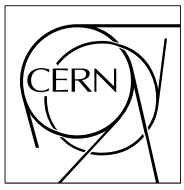
CMS NOTE 1999/058



The Compact Muon Solenoid Experiment

CMS Note

Mailing address: CMS CERN, CH-1211 GENEVA 23, Switzerland



April 29, 1999

Performance of the APV6, bonded to a full size Forward Milestone silicon detector

Simone Busoni, Carlo Civinini, Raffaello D'Alessandro, Michela Lenzi,
Marco Meschini, Andrea Piergentili, Marco Pieri
Dipartimento di Fisica e INFN Sez. di Firenze, Florence, Italy

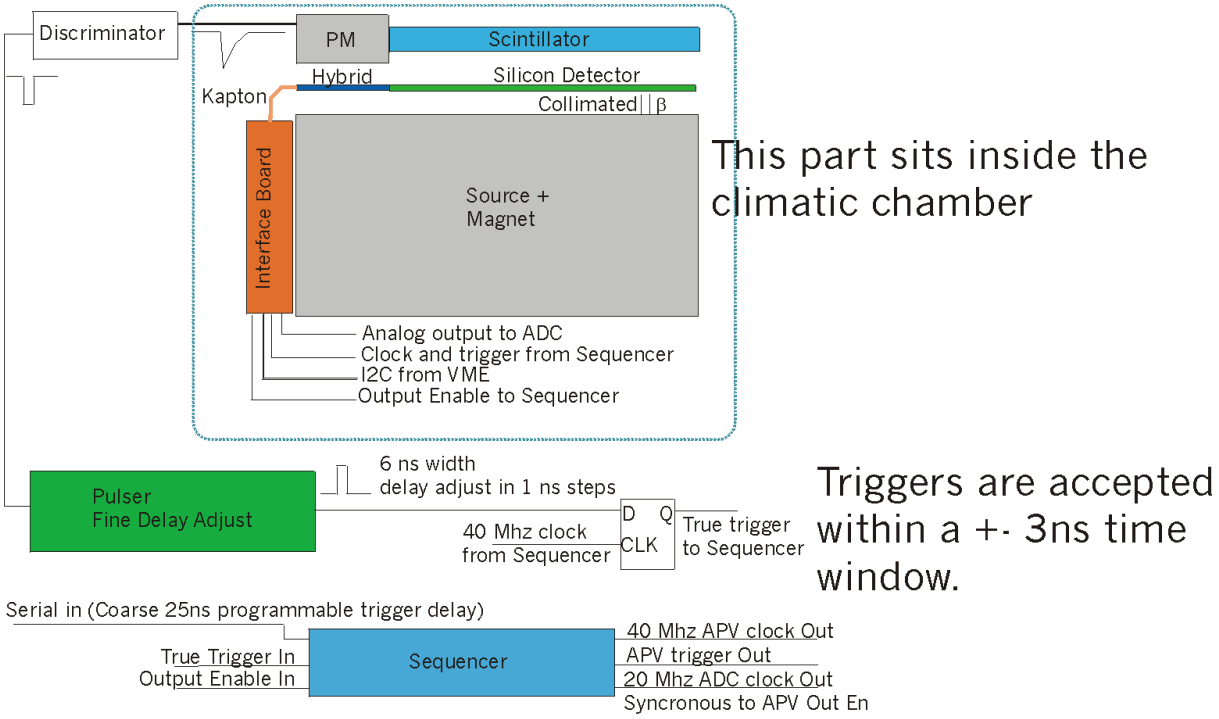
Abstract

We describe our test set-up used to read-out APV6 hybrids bonded to full size silicon detector modules [1] of the type built for the Forward Milestone. Choice of APV6 parameters is discussed and results with calibration pulses and MIPs are presented.

1 APV6 test set-up

1.1 Introduction

We have designed our set-up so that it can also be used with irradiated detectors; this has meant placing the source and part of the electronics inside a climatic chamber.



Interface Board does the following:
Differential Buffering of the APV analog signal (gain 6 mV/uA)
Level Addaptation of LVDS clock and trigger signals to the APV
Buffering of the Output Enable signal from the APV

Figure 1: Block diagram of the DAQ set-up

We have taken great care in assuring that all APV6 signals (trigger, reset, calibration) are correctly in phase with the 40 MHz clock, also great care has been placed on the receiving network so that the signals remain “clean”. The detector hybrids with the APV6s have been produced at CERN; these hybrids can hold up to four chips and have 100 Ohm resistors on them to terminate clock and signal lines. In our set-up these resistors have been unsoldered as correct termination and polarization levels are provided by the interface board (see appendix a). This last board also buffers the analog output and the output enable signals from the APV6s.
The β source used is Strontium 90; with the use of an electromagnet, only the end point electrons (~2MeV) are selected, collimated and sent to the detector. The scintillator placed on top of the tested detector provides the particle triggers.
Finally the pulser allows us to precisely set the correct delay value between arrival of the particle and the triggering of the APV6. Note that only particles arriving inside a +/- 3 ns time window of the clock rising edge are used for APV6 triggering. For more information on the use of the APV6 see ref. [2,3].

1.2 Settings

1.2.1 I2C registers

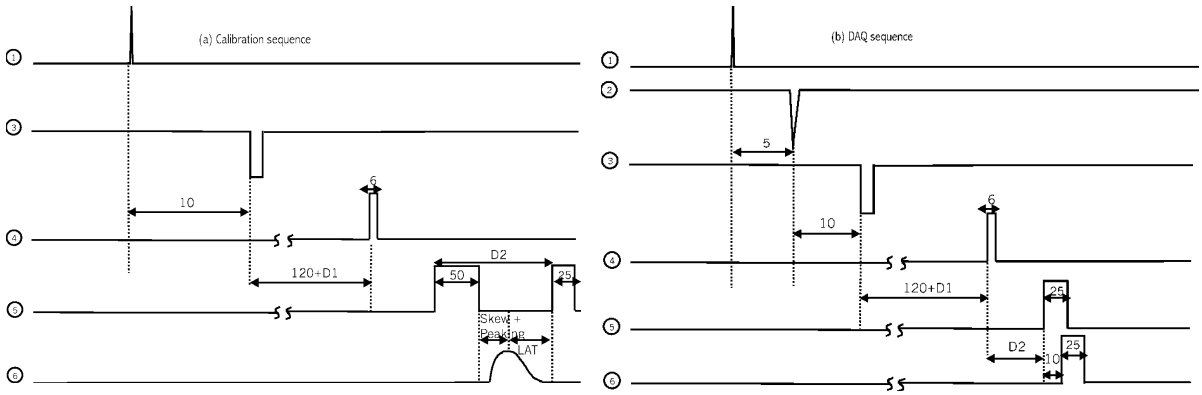
The APV6 allows great flexibility of use, with the possibility of setting various parameters which control the way the chip responds to input signals. We report in Table 1 the APV6 register nominal values[1] and the values used in October 1998 test beam and which we used in our set-up during calibration data taking. Most of the parameters have only minor variations with the exception of VADJ which sets the APV6 output baseline. The value of VSHA is set to zero; this sets the shaper timing constant at its shortest possible value (50 ns peaking time).

REGISTER	DEFAULT VALUE		REGISTER	B-TEST VALUE
IPRE	111 (0X 6F)		**IPRE**	120 (0X 78)
ISHA	88 (0X 58)		**ISHA**	81 (0X 51)
IPSP	84 (0X 54)		**IPSP**	66 (0X 42)
ISFB	43 (0X 2B)		**ISFB**	41 (0X 29)
VPRE	150 (0X 96)		**VPRE**	184 (0X B8)
VSHA	0		**VSHA**	0
VADJ	120 (0X 78)		**VADJ**	166 (0X A6)
VCAS	0		**VCAS**	0

Table 1: Nominal values for the APV6 registers (from ref. [2], and from the 1998 October test beam)

1.2.2 Timing

One of the most important parameters for the correct operation of the APV6 is the value of the latency register. Below (figure 2a, 2b) there are two timing diagrams for both modes of the APV6 settings: Calibration and DAQ. During the calibration procedure external delays due to the electronic chain that generates initial triggers are not important since the sequencer provides all the, correctly timed, pulses from only one initial external pulse sent to its own calibration input (see appendix b). As we can see from the diagram, the sequencer generates a pulse (Cal Request 50 ns long), followed, after a delay (D2 in steps of 25 ns set from the serial input), by a trigger pulse (25 ns long). After a settable delay (Skew register) from the falling edge of Cal Request, the APV6 receives a



delta-like pulse on its input, it then reaches its peak value. Latency is calculated from this moment onwards. By varying D2 (on the sequencer) one can choose which cell in the analog pipeline to sample.

Figure 2: Timing sequence for Calibration mode (a), DAQ mode (b). (1) is the time of particle passage, (2) photo-multiplier output, (3) discriminator output, (4) NIM logic + pulser delay D1 (1ns resolution), (5) trigger output to the APV6 on the sequencer board, (6a) signal after integration by the APV6 amplifier, (6b) trigger to the APV6 on the hybrid after cable and interface board. In Calibration mode (1) is replaced by an external pulser. All units are in ns, diagram not to scale.

---

[1] Nominal values are such as to ensure a reasonable working point for the APV6, close to the design values intended for the chip. On the other hand, process parameter variations mean that optimal values should be established by measurement.

In DAQ mode all delays are relevant, in addition we use a pulser to set an additional delay (D1) which is used to fine tune the exact value for the correct sampling of the particle signal (1 ns resolution). This has the same function basically of the Skew register used in calibration mode. As stated in the introduction, particles are accepted only if within +/- 3 ns from the APV6 40 MHz clock rising edge.

1.3 Detector characteristics and data processing

The detector used (see ref. [1]) is a wedge shaped single sided silicon microstrip detector with 1024 readout strips with pitch varying from 50 μ on the short side, reaching 70 μ at the end of the module. Strips are connected to the front-end electronics through decoupling capacitors which are integrated on the detector. These detectors have been fully characterized for what concerns impedance measurements between adjacent strips, between strips and the backplane, and of the decoupling capacitors. From these measurements we infer that at a bias voltage of 250 V, the input capacitance seen by the APV6 corresponds to 13.5 pF, while the decoupling capacitor transfers 91.8 % of the detector signal charge to the APV6. We bonded 256 strips to two APVs, the data shown is for 128 strips (1 APV only). Measured detector full depletion voltage is equal to 80 V.
Our data is reconstructed with the use of cluster finding algorithms standard to normal silicon detector operation. First common noise and pedestals are subtracted, then we look for strips (channels) which have a significant amount of charge on them (4 sigma noise cut). We then look at the nearest neighbours of these "seeds" to see whether they also have some charge (2 sigma noise cut). We sum the charge of the seed and its neighbours (cluster) and, if the total charge is greater than five times the noise sigma value, we record the event. Obviously in calibration mode the clustering algorithm is skipped. This procedure implies that our charge amplitude scale is always referred to zero. The noise values we quote are the charge weighted average of the cluster strip's noise.

2 Results

2.1 Calibration mode

We first took data using the internal calibration capacitors of the APV6.

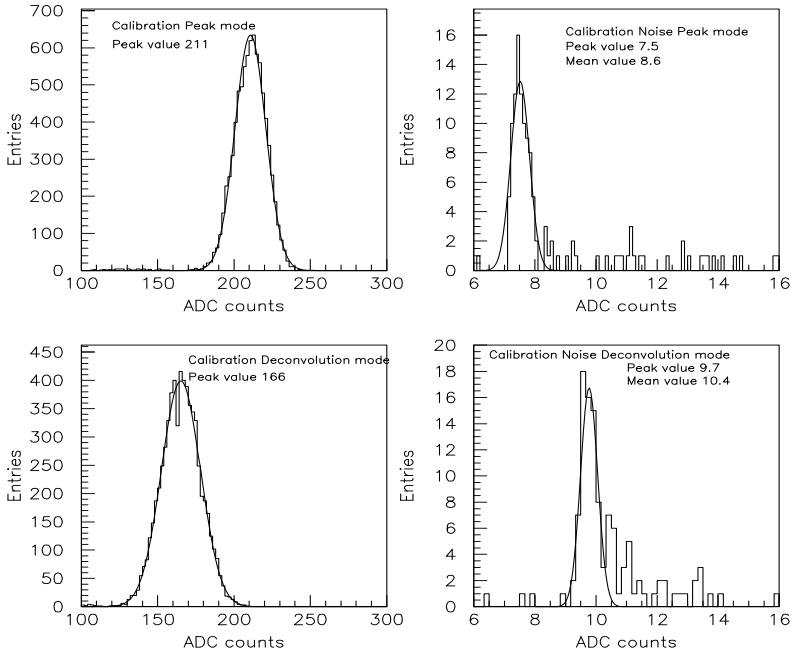


Figure 3: Data obtained using the internal calibration capacitors. Signal and strip noise[2], in peak (top) and deconvolution mode (bottom). Equivalent input capacitance 13.5 pF.

[2] The noise distribution plots show relevant tails which have nothing to do with the way the APV6 works but are due to some shorted strips on the detector that was used for these measurements.

I2C register settings are as above in table 1 (Test beam), in addition the three registers dedicated to calibration are set as follows:

- CLVL 0x3c
- CSKW 0xfd
- CDRV 0xf7

The first sets the amplitude of the calibration pulse, the second sets the skewing between calibration pulse and clock, the third which channels receive the pulse. In figure 3 we show the results obtained (signal and noise) both in peak mode and in deconvolution mode with pedestals and common noise subtracted. The spread of the signal distribution is due to gain variations between the 128 channels and injection capacitor value differences, convoluted with noise. The noise distribution plot shows the measured pedestal sigmas for the 128 channels. Common mode noise distribution (not shown), is gaussian with a sigma value of less than four ADC channels.

The value of the CLVL register was inferred from ref. [2] to be roughly equivalent to a 1 MIP signal (375 electrons per count). We verified with an external capacitor that this value is correct. Unfortunately this is a tricky measurement and we estimate an error of roughly 30% on this verification. Another work [3] gives an estimate of 625 electrons per count, implying that a MIP signal corresponds to a lower setting of CLVL = 39 and not 60 as we used. The difference between the two values is of the order of 45%, which could very well be given the above quoted error and the variations between different chips (due to injection capacitor values, reference current variations and so on). The data in the plots can be summarised as follows:

- S/N (peak) = 28.1
- S/N (deconvolution) = 17.1
- $S_{peak}/S_{decon} = 1.27$
- $N_{peak}/N_{decon} = 0.77$

Taking from ref. [3] the formula for the expected E.N.C. noise as a function of input capacitance,

- Peak mode: 510 + 36/pF
- Deconvolution mode: 1000 + 46/pF

we expect an E.N.C. value for our detector of 996 electrons in peak mode and 1621 electrons in deconvolution mode. If we use 375 electrons per count [2], then we injected 22500 electrons in the APV6. In this case we have a measured E.N.C. of 800 electrons in peak mode and 1315 electrons in deconvolution. On the other hand, choosing the 625 electron value from ref. [3] will result in an E.N.C. of 1334 electrons in peak mode and 2192 electrons in deconvolution mode. Again summarising:

Peak mode:	Deconvolution mode:
Expected noise: 996 electrons	Expected noise: 1621 electrons
Measured noise using ref.[2]: 800 electrons	Measured noise using ref.[2]: 1315 electrons
Measured noise using ref.[3]: 1334 electrons	Measured noise using ref.[3]: 2192 electrons

So while a value of 375 electrons per count seems to lead to an overly optimistic result, the 625 electrons per count leads to a ~30% worse result than what expected. Given the uncertainties on the absolute value of the injected source we then started taking data with the β source system.

2.2 DAQ mode with the β source

As mentioned before, the detector used with these measurements has a depletion voltage of ~80 V. We started by using the test-beam parameters for the I2C registers and with the detector biased at 100 V (figure 4 (top). The particles which hit the detector are ~2 MeV electrons. The peak value obtained by fitting a Landau distribution to the data is 101 ADC channels (Peak mode) and 80 ADC channels (Deconvolution mode).

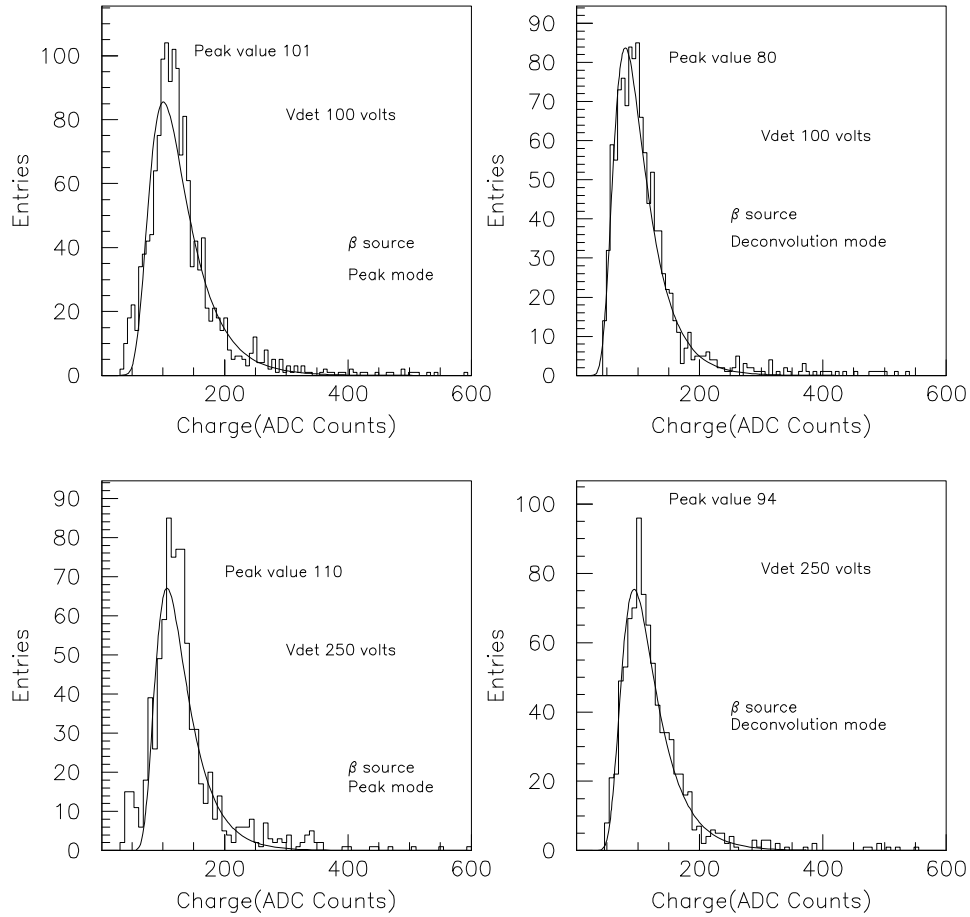


Figure 4: MIP signal in peak and deconvolution mode, Vdet = 100 V (top), Vdet = 250 V (bottom).

- S (peak,100 V) = 101, S/N = 13.5
- S (deconvolution, 100 V) = 80 , S/N = 8.2
- S_{peak}/S_{decon} = 1.27
- N_{peak}/N_{decon} = 0.77

The noise distributions (not shown) are in agreement with those obtained in the calibration runs, and the S_{peak}/S_{decon} , N_{peak}/N_{decon} values are also consistent. However the absolute value of the collected charge is less than half of what was obtained in the calibration runs. Even if we consider that due to the presence of de-coupling capacitors we lose (with these detectors) 8.2% of the ionisation charge and that the absolute value of the calibration has an estimated error of ~ 30% there still could be some other effect working against us. We thought that one possible explanation could be inefficient charge collection. To investigate this possibility we started raising the detector bias voltage up to 250 V, corresponding to roughly a factor three over-depletion. In figure 4 (bottom) we show the signal and noise in these conditions, again with test-beam I2C parameters.

- S (peak,250 V) = 110, S/N = 14.7
- S (deconvolution, 250 V) = 94, S/N = 9.7
- S_{peak}/S_{decon} = 1.17
- N_{peak}/N_{decon} = 0.77

This has a clearly beneficial effect, in as much that the detector signal is faster and thus the APV6 collects more charge but still we see less charge than what expected. At this point we also started changing the shaper time

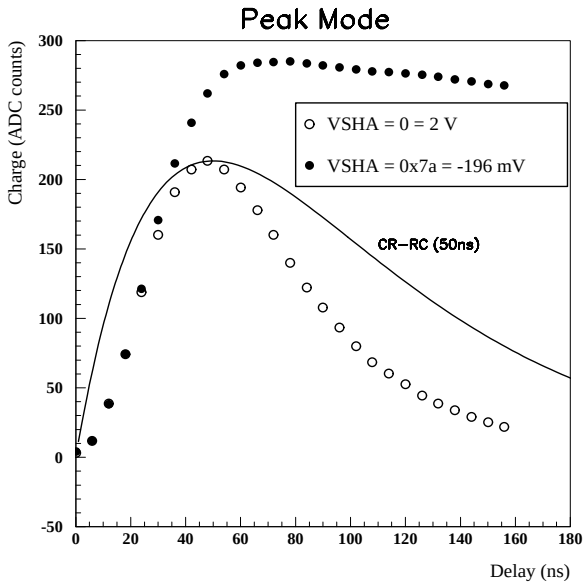


Figure 5: Pulse shape in peak mode, with VSHA = 0x0 and VSHA = 0x7E, also shown is the ideal response of a CR_RC shaper peaking at 50 ns.

constants through the register VSHA , assuming that a longer shaping time might be more suited to the actual pulse shape of a silicon detector signal (~ 10 ns long) which, given the APV6 fast shaping, is a far cry from an ideal delta like pulse. Changing this parameter can have serious implications concerning how the chip will perform in deconvolution mode. Namely we might lose its ability to resolve pulses with a 25 ns resolution. In figure 5 we show the actual pulse shapes we have measured (using the internal calibration) with this parameter set at 0 (nominal value from [2]) and at hexadecimal 7E both in peak and in deconvolution mode[3]. As one can see changing VSHA can change dramatically the pulse shape. In deconvolution mode, though, the algorithm manages anyway to filter out the long tail. We then took data with this setting. The results are shown in figure 7 where we show the Landau distributions for the MIP signals after common noise and pedestal subtraction, and the distribution of the pedestal widths for those strips that were exposed to the collimated β source.

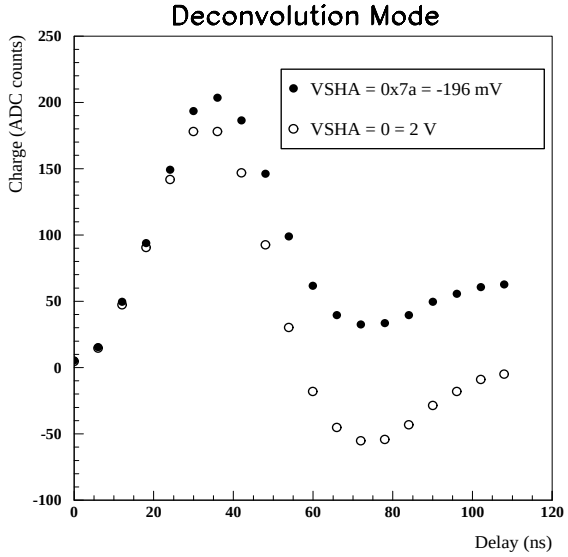


Figure 6: Pulse shape in deconvolution mode, with VSHA = 0x0 and VSHA = 0x7E.

[3] As one can easily observe from fig. 5, the choice made for the VSHA parameter is rather extreme. We would like to stress that this does not correspond to the optimal value we would choose for normal operation. We anyway wanted to test the chip functionality (especially in deconvolution mode) even with this extreme setting.

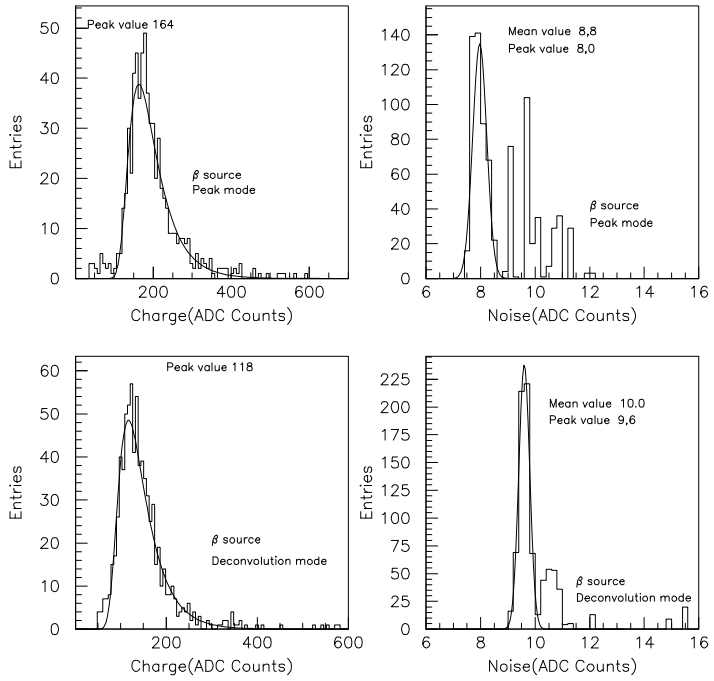


Figure 7: MIP signal and noise, in peak (top) and deconvolution mode (bottom), Vdet = 250 V, VSHA = 0x7E.

- S/N (peak) = 20.5
- S/N (deconvolution) = 12.3
- S_{peak}/S_{decon} = 1.39
- N_{peak}/N_{decon} = 0.83

These results are in some agreement with what we saw in calibration mode, especially when one considers, as stated previously, that the decoupling capacitors present on the detector further reduce the signal by ~10 %, and that the error on the absolute charge calibration value. In peak mode we have increased the delay by 15 ns (where the output reaches the maximum), this is in agreement with the expected amplifier response [2] and with what shown in figure 5. In deconvolution mode instead we retain the original delay setting, which gives the best results. In this mode it is very important to track precisely the starting point (0 to 10 %) of the pulse, which is not affected by the VSHA setting anyway. At this point we can use the Landau peak to extract the noise of our system in E.N.C. counts.
Assuming that a MIP releases 24000 electrons in our detector (a 2 MeV electron is a close approximation of a MIP), we have:

- 24000 * 0.92 = 22080 (Charge effectively transferred through the de-coupling capacitor)
- 22080/20.5 = 1077 electrons (noise in peak mode)
- 22080/12.3 = 1795 electrons (noise in deconvolution mode)

To be compared with the expected values of 996 and 1621 electrons for, respectively, peak and deconvolution mode.

One of our worries, with this high setting of VSHA, was that we might see charge (and clusters) for out of time (+/- 25 ns) events, since (as shown in figure 5b) the pulse shape does not return to zero after 25 ns. This would then lead to high values of occupancies in the tracker. In the event we checked this and the results of the delay scan can be seen in figure 8.

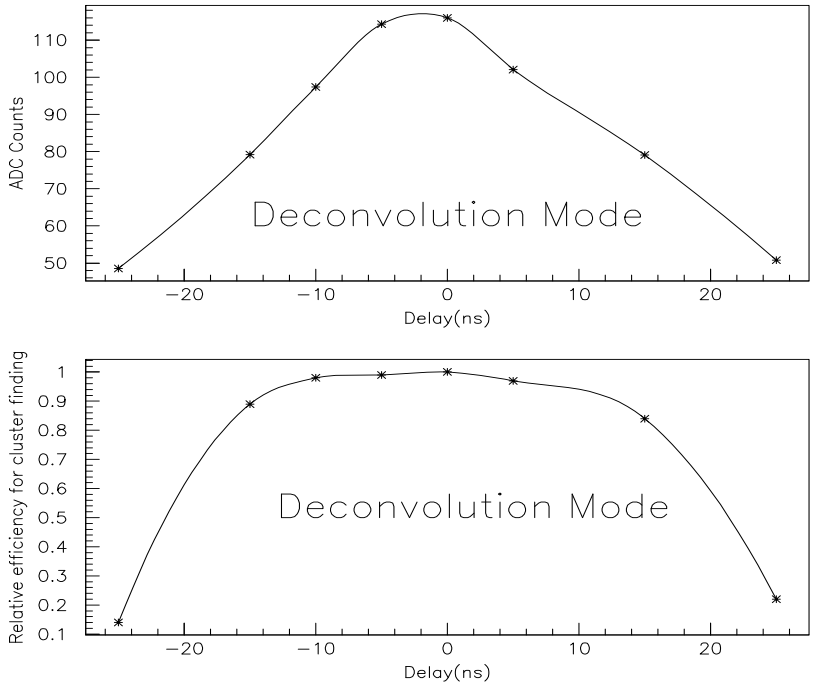


Figure 8: Charge values (top) and relative cluster finding efficiency (bottom) as a function of time (0 corresponds to the optimal setting) in deconvolution mode, Vdet = 250 V, VSHA = 0x7E.

The charge values, which correspond to the Landaus peak values, drop significantly, in agreement with the pulse shape of figure 5b but what is more important the cluster reconstruction efficiency drops to ~10 % at +/- 25 ns. Thus even this high setting of VSHA seems to have little influence on occupancy rates.
We think that a careful choice of this parameter is a must, for everybody interested in the use of the APV6 with silicon detectors. A good starting point is given by figure 9 taken from ref. [2].

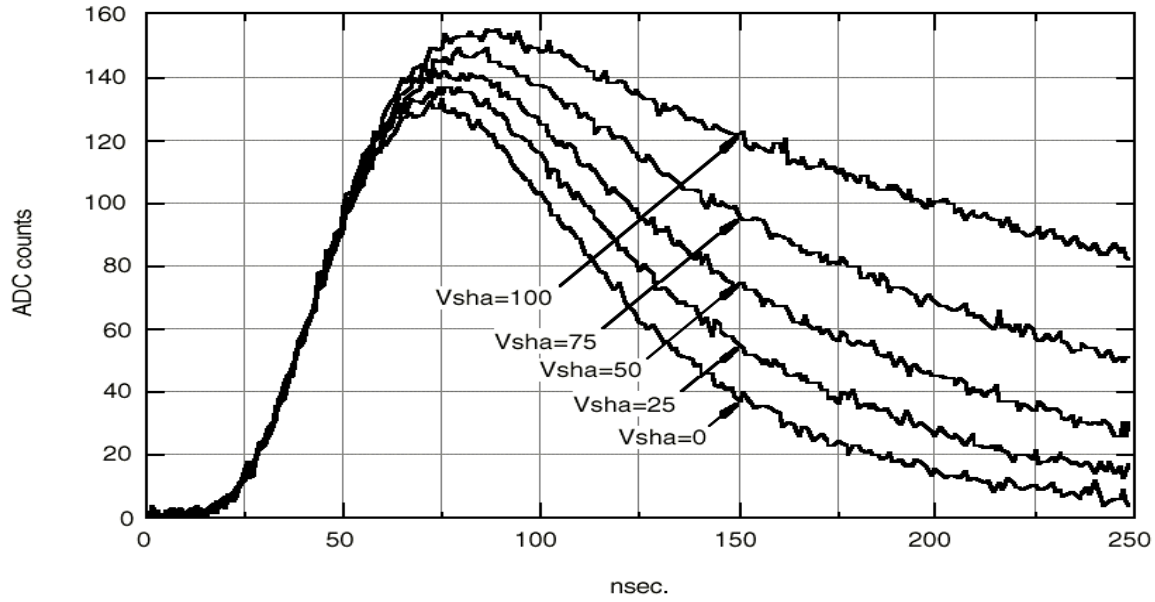


Figure 9: Measured pulse shapes at various settings of VSHA (decimal values) from the APV User Manual.

We have taken data with VSHA varying from 0 to 0x64. We have found that, in our case, increasing it beyond 0x4B, does not result in any increase in the seen charge, suggesting that the optimal value lies around 0x32 – 0x40.

4 Conclusions

The APV6 coupled to a full-sized detector seems to perform as expected from our previous experience with the PreMux chips. We have illuminated a Forward Milestone detector with 2 MeV electrons, obtaining signal to noise ratios of 20.5 to 1 in peak and 12.3 to 1 in deconvolution mode. We will now proceed to test irradiated detectors in the same way. The parameter settings and their influence on chip behaviour need further systematic testing on many more hybrids, so that we can have a better grasp of what the best possible operating conditions are for silicon detectors in the CMS tracker.

References

[1] **Characterization of neutron irradiated silicon microstrip detectors**, Lenzi et al. . *"To be published in Proceedings of Como 1998 INTERNATIONAL CONFERENCE ON ADVANCED TECHNOLOGY AND PARTICLE PHYSICS"*.

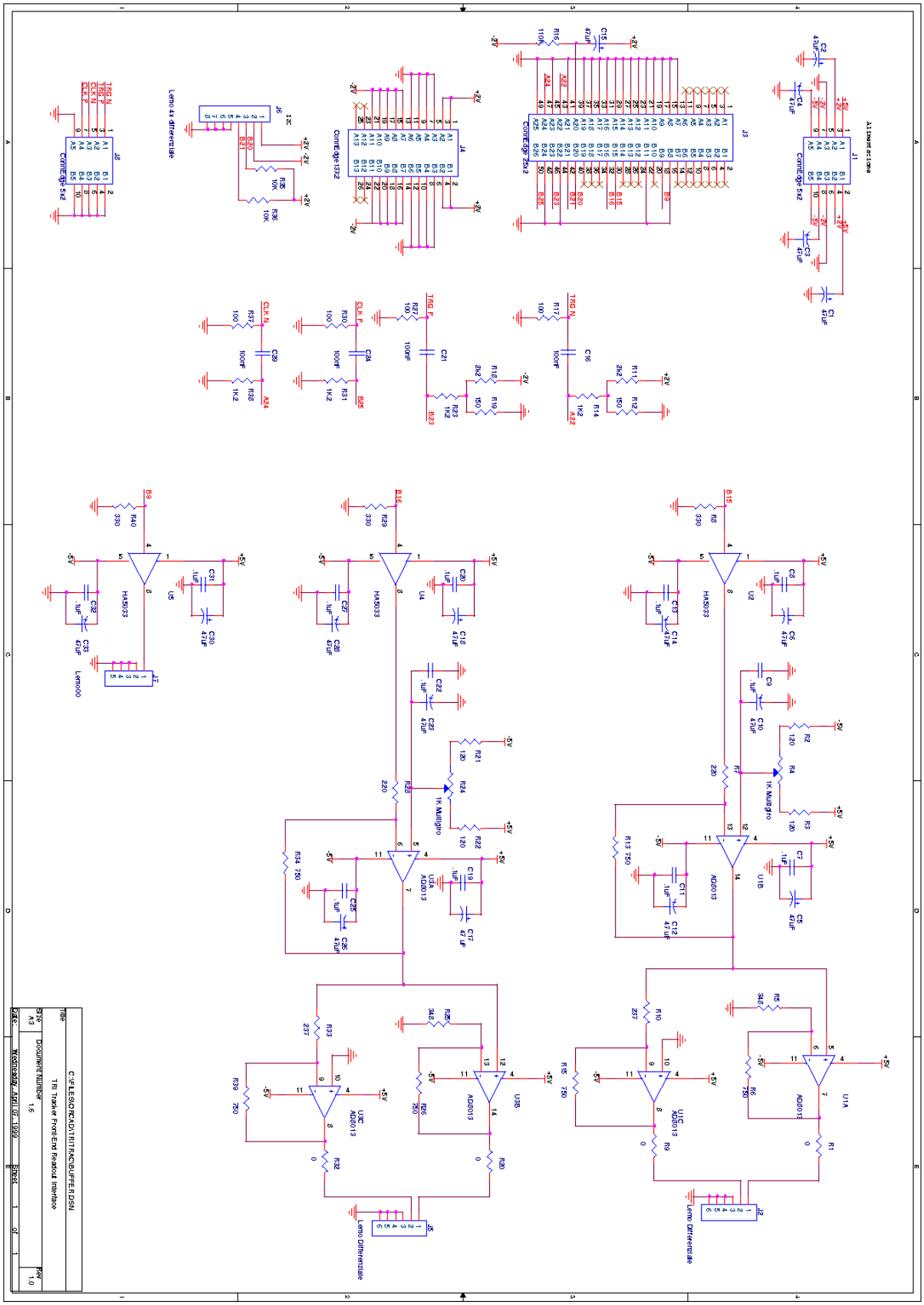
[2] **APV6 User Manual**, M. French .

[3] **The APV6 Readout chip for CMS Microstrip detectors**, M. Raymond et al., *"Third Workshop on electronics for LHC experiments, October 1997, CERN/LHCC/97-60"*.

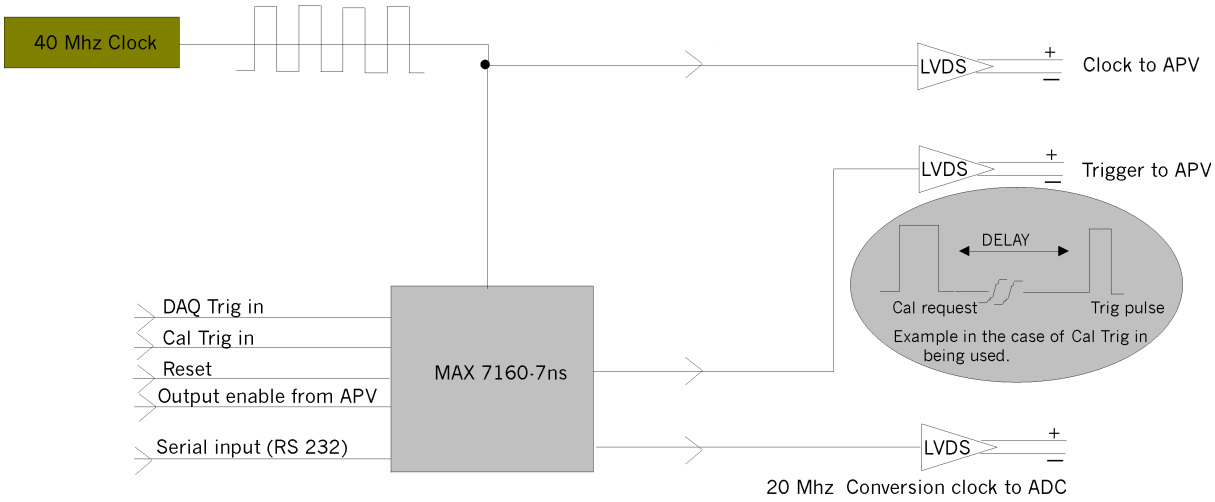
[4] **First Testbeam with APV6 – Silicon System**, M. Friedl, *"CMS Tracker Week, July 1998"*.

[5] **Addendum to the June 98 APV6-Testbeam**, W. Adam et al., *"CMS Week, December 1998"*.

Appendix (A): Layout of the interface board



Appendix (B): Sequencer block diagram



Serial Input: used to program the delay between DAQ Trig in and Trigger to APV (25 ns steps).
In calibration mode (use Cal Trig in), the sequencer will generate a prompt calibration pulse (50 ns width) followed (after the programmed delay) by a trigger pulse.
The ADC Conversion clock starts on falling edge of the Output enable from APV.

–