PCE385

PCI Express® Four Channel T1/E1/J1 Communications Processor

Hardware Installation Guide

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PERFORMANCE TECHNOLOGIES

Document Revision History

Part Number	Date	Explanation of Changes
126p0489.10	November 10, 2006	Draft
126p0489.11	February 22, 2007	Released
126p0489.12	March 29, 2007	Corrected “CE Certification” on page 81.
126p0489.13	November 1, 2007	Corrected “Safety Compliance” on page 82.
126p0489.14	January 31, 2008	Clarified up-plugging installation of the PCE335

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Errors and Omissions

Although diligent efforts are made to supply accurate technical information to the user, occasionally errors and omissions occur in manuals of this type. Refer to the Performance Technologies, Inc. Web site to obtain manual revisions or current customer information:

http://www.pt.com.

Performance Technologies, Inc., reserves its right to change product specifications without notice.

Symbols and Conventions in this Manual

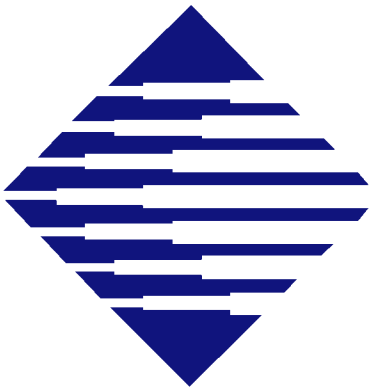
The following symbols appear in this document:

Caution:
There is risk of equipment damage. Follow the instructions.

Warning:
Hazardous voltages are present. To reduce the risk of electrical shock and danger to personal health, follow the instructions.

Caution:
Electronic components on printed circuit boards are extremely sensitive to static electricity. Ordinary amounts of static electricity generated by your clothing or work environment can damage the electronic equipment. It is recommended that anti-static ground straps and anti-static mats are used when installing the board in a system to help prevent damage due to electrostatic discharge.

Additional safety information is available throughout this guide and in Chapter 9, “Product Safety Information”.



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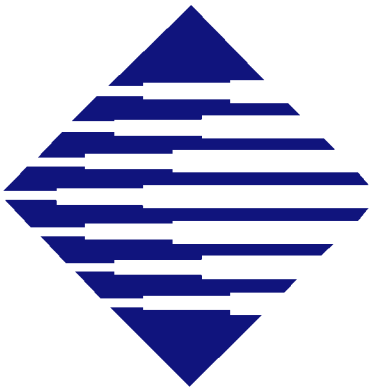

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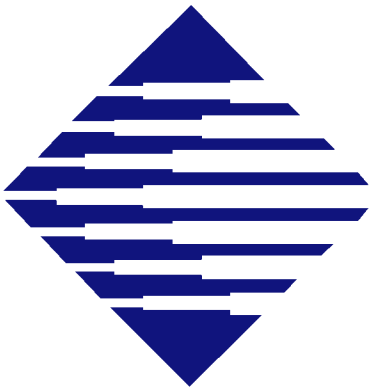

Chapter

1

About This Guide

Overview

This guide provides the PCE385, Version 1.0 installation and configuration procedures intended for the installer, and the product architecture description intended for the application developer of this board.

Here is a brief description of the information in this Guide:

Chapter 2, “Introduction” on page 17 provides an overview of the PCE385 and a summary of the interaction between the board components.

Chapter 3, “Installation” on page 25 provides the information required to install the PCE385.

Chapter 4, “Development Environment” on page 29 provides information about the board memory, interface, features, flash memory, operating modes, and Framer and Line Interface Unit (LIU) information required to develop applications. This chapter also provides information about the Joint Test Action Group/Bund Deutscher Mädel (JTAG/BDM) debug port and the console port.

Chapter 5, “ATM Channel Allocations” on page 55 provides information about Time Division Multiplexing (TDM) data flow, frame pulse, and the TDM clock. This chapter also provides information about how the signals are routed to the MPC8280 TDM inputs and outputs.

Chapter 6, “Pinouts” on page 69 provides information about the JTAG/BDM port, the nine-pin subminiature connector, and the P3 eight-pin header that is used to set the board configuration and operation mode.

Chapter 7, “Specifications” on page 77 provides information about the system requirements including the environmental requirements and the power requirements.

Chapter 8, “Data Sheets and Agency Approvals” on page 79 provides information about the data sheets, standards, and specifications for the technology designed into PCE385. This chapter also provides the agency approvals for the PCE385.

Chapter 9, “Product Safety” on page 85 provides information about safety precautions for the PCE385.

Related Documents

The PCE385 assembly should be used in conjunction with the Performance Technologies software package that you have chosen, for example:

- NexusWare Core
- NexusWare C7
- HDLC
- Frame Relay
- X.25

This product is compatible with the complete suite of Performance Technologies software.

Documentation to support the additional components that you purchased from Performance Technologies is available on the documentation CD. The most current documentation can be located at http://www.pt.com under the product you are inquiring about.

Text Conventions

Table 1-1: “Conventions in This Guide”describes the text conventions and the graphic conventions that are used in this guide.

Table 1-1: Conventions in This Guide

Convention	Used For
`Monospace font`	Monospace font represents sample code.
Bold font	Bold font represents: • paths • file names • UNIX commands • user input.
Italic font	Italic font represents: • notes that supply useful advice • supplemental information • referenced documents.
$ARCH	This symbol represents the processor architecture, currently this architecture is ppc, mips, arm, and i386.
< >	Angle brackets represent variables such as file names and passwords.
ALL CAPITALS	All capitals represent keys on the keyboard (for example, ENTER, TAB, and SPACEBAR keys).

Customer Support and Services

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1. **EMAIL** (Preferred Method) – Email us at the addresses listed below or our online email support form. Outline your problem in detail. Please include your return email address, and a telephone number.
2. **TELEPHONE** – Contact us via telephone at the number listed below, and request Technical Support. Our offices are open Monday to Friday, 8:00 a.m. and 8:00 p.m. (Eastern Standard Time).

Performance Technologies Support Contact Information

	Embedded Systems and Software (Includes Platforms, Blades, and Servers)	SS7 Systems (Includes SEGway™)
Email	support@pt.com	ss7support@pt.com
Email Form	http://www.pt.com/support/emailtechsupport.html	
Phone	+1 (585) 256-0248 (Monday to Friday, 8 a.m. to 8 p.m. Eastern Standard Time)	+1 (585) 256-0248 (Monday to Friday, 8 a.m. to 8 p.m. Eastern Standard Time)

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To submit a return merchandise authorization (RMA) request, complete the online RMA form at http://www.pt.com/support/RMA_Request_Form.doc and follow the instructions on the form. You will be notified with an RMA number if your return request has been approved. Shipping information for returning the unit to Performance Technologies will be provided once the RMA is issued.

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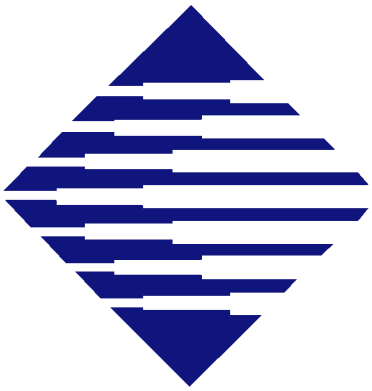


Chapter

2

Introduction

Overview

The PCE335 is a four-channel T1/E1/J1 communications processor for Peripheral Component Interconnect (PCI) Express based systems.This product uses the PCI Express bus for host processor communications and control. The product provides a high performance, fully channelized platform for use in both datacom and Telecom applications. The PCE385 can run protocols such as Frame Relay, Integrated Services Digital Network (ISDN), or any protocol using High-Level Data Link Control (HDLC) in Internet/Wide Area Network (WAN) environments. In Telecom applications, the PCE385 supports Message Transfer Part (MTP) level two on all four links. Time Division Multiplexing (TDM) line interface connections are made using four RJ-48C connectors on the front panel.

The core of the PCE335 is a Freescale MPC8280 PowerQUICC II communications microprocessor running at 450 MHz. This microprocessor includes an embedded Communications Processor Module (CPM) that uses a 32-bit Reduced Instruction Set Computer (RISC) controller residing on a separate local bus. The CPM instruction set is optimized for communications, moving the task of handling lower level communications and Direct Memory Access (DMA) activity off of the PowerPC core Central Processing Unit (CPU).

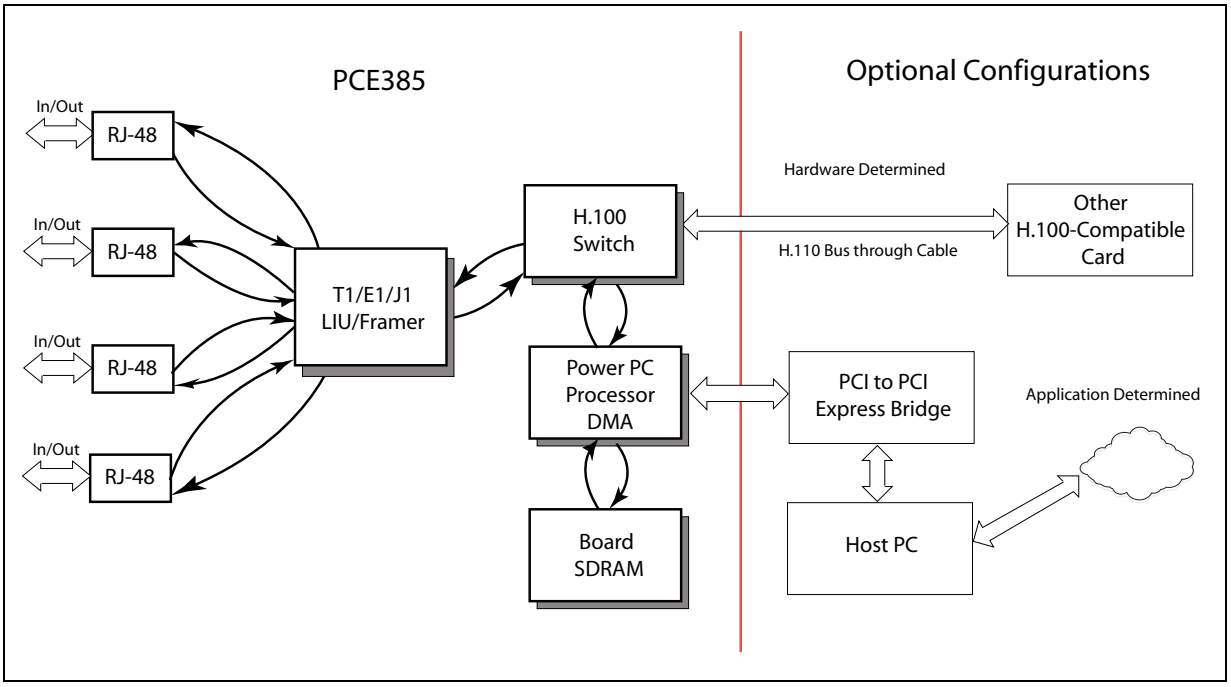
Topics in this chapter include:

Operational Overview

The PCE385 supports the following three modes of processing (see Figure 2-1: "Operational Overview Diagram"):

- Processing on the PCE385 Board
- Processing on the Host
- Processing on the H.100-Compatible Board

Figure 2-1: Operational Overview Diagram



Processing on the PCE385 Board

Processing on the PCE385, where the processing of packets takes place solely on the PCE385, is the normal configuration. Table 2-1: “Data Flow in Processing on the PCE385 Board” describes the flow of the data.

Table 2-1: Data Flow in Processing on the PCE385 Board

Number	Path / Operation	Output Data Type / Description
1	Line-in to LIU/Framer	Line data
2	LIU/Framer to H.100 Switch	TDM data (Framer converts line data to TDM data)
3	H.100 Switch to PowerPC Processor	TDM data [1]
4	PowerPC Processor to SDRAM	TDM data (processor sets up peripherals and sends data for storage)
5	SDRAM to PowerPC Processor	TDM data (data returns to processor when SDRAM buffer is full)

Table 2-1: Data Flow in Processing on the PCE385 Board (Continued)

Number	Path / Operation	Output Data Type / Description
6	PowerPC to H.100 Switch	TDM data
7	H.100 Switch to LIU/Framer	TDM data
8	LIU/Framer to Line-out	Line data (Framer converts TDM data to line data as T1/E1/J1)

1. The H.100 switch can either send it, using an H.100 cable, over the H.100 bus to another H.100-compatible board or forward it to the PowerPC Processor.

For a visual representation of this process, see Figure 2-1, “Operational Overview Diagram” on page 18.

Processing on the Host

The PCE385 processing on the host computer, where some processing of packets takes place on the Host computer, uses both the PCE385 board and the Host computer. Table 2-2: “Data Flow in Processing on the Host” describes the flow of the data.

Table 2-2: Data Flow in Processing on the Host

Number	Path / Operation	Output Data Type / Description
1	Line-in to LIU/Framer	Line data
2	LIU/Framer to H.100 Switch	TDM data (Framer converts line data to TDM data)
3	H.100 Switch to PowerPC Processor	TDM data
4	PowerPC Processor to SDRAM	TDM data (processor sets up peripherals and sends data for storage)
5	SDRAM to PowerPC Processor DMA	TDM data (data returns to processor when SDRAM buffer is full)
6	SDRAM to PowerPC Processor DMA	TDM data
7	PowerPC DMA to PCI Bridge	TDM data
8	PCI Bridge to Host PC	Line data (Framer converts TDM data to line data
9	Host PC to Ethernet or Other On-host action [1]	Line data

1. Other On-host action might include, transfer to other board, pass to alternative location with packets or return trip back to originating Line-in/Line-out.

For a visual representation of this process, see Figure 2-1, “Operational Overview Diagram” on page 18.

Processing on the H.100-Compatible Board

The PCE385 processing on the H.100-compatible board, where the processing of packets takes place on the H.100-compatible board, uses both the PCE385 board and the H.100-compatible board. Table 2-3: “Data Flow in Processing on the H.100-Compatible Board” describes the flow of the data.

Table 2-3: Data Flow in Processing on the H.100-Compatible Board

Number	Path / Operation	Output Data Type / Description
1	Line-in to LIU/Framer	Line data
2	LIU/Framer to H.100 Switch	TDM data (Framer converts line data to TDM data)
3	H.100 Switch to H.100-compatible board	TDM data over H.100 cable (H.100 bus)

For a visual representation of this process, see Figure 2-1, “Operational Overview Diagram” on page 18.

PCE385 Board Layout

Warning:
Use anti-static grounding straps and anti-static mats when you are handling the PCE335 to help prevent damage due to electrostatic discharge. Electronic components on printed circuit boards are extremely sensitive to static electricity. Ordinary amounts of static electricity generated by your clothing or work environment can damage the electronic equipment.

The PCE385 includes the following two boards:

- Main Board Component Layout
- Daughter Board Component Layout

Main Board Component Layout

This section describes the principal components of the PCE385 main board (see Table 2-4: “PCE385 Main Board Component Layout Call Out Definitions” and Figure 2-2, “PCE385 Main Board Component Layout” on page 21).

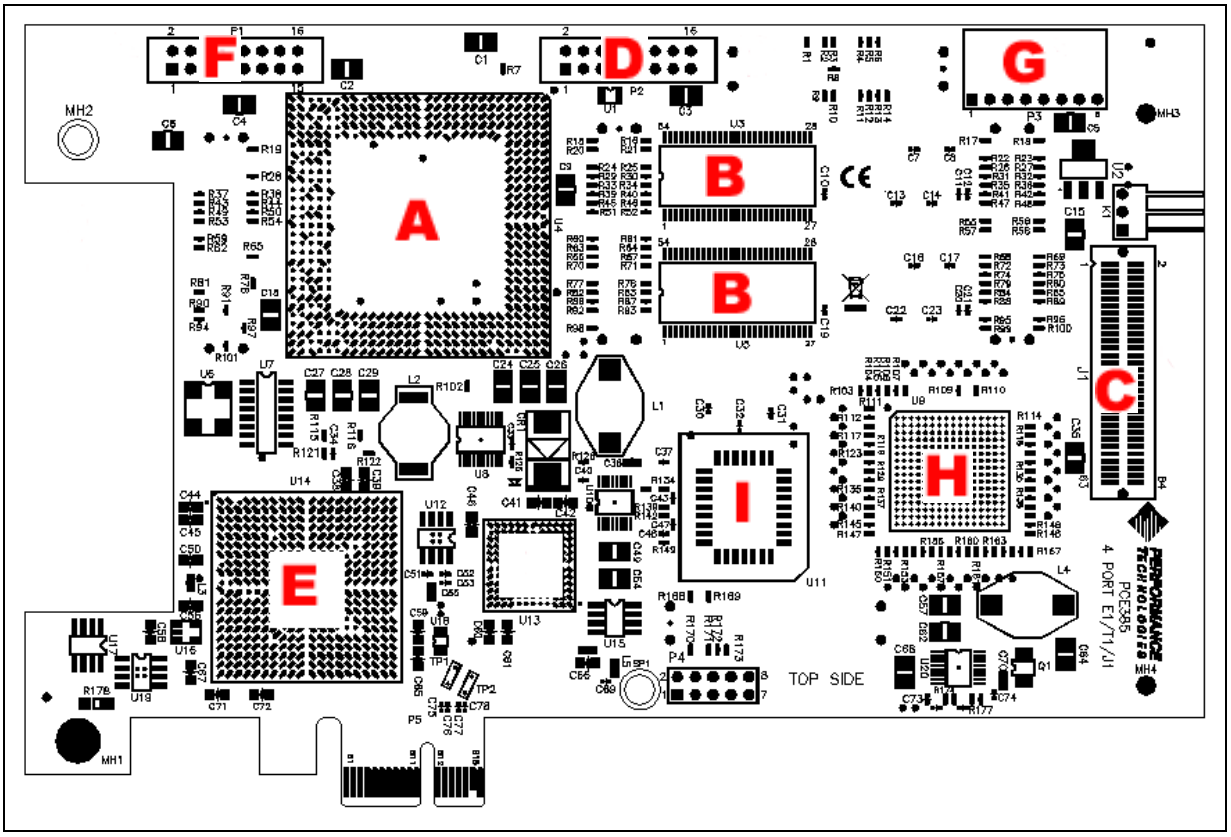
Table 2-4: PCE385 Main Board Component Layout Call Out Definitions

Call Out Letter	Item	Description
A	PowerQUICC II MPC	PowerPC 455 MHz CPU, 300 MHz CPM, 100 MHz Bus
B	SDRAM Chips	64-bit data width, 128 MB,7.5 ns
C	Daughter Board Interface Connector	Electronic connection point for the daughter and main board
D	JTAG Testing Port	JTAG port for the on board In-system Programmable CPLD.
E	PCI6466	PCI/PCI express nontransparent bridge

Table 2-4: PCE385 Main Board Component Layout Call Out Definitions (Continued)

Call Out Letter	Item	Description
F	MPC8280 COPS Header	COPS Header for JTAG debugging of the CPU
G	Option Jumper Block	Configuration header (see Table 6-4, “Option Jumper Block (P3) Pinout” on page 73)
H	Boot Prom	512 K x 8 Flash memory device that contains the CPU bootstrap code
I	PEX8111	PCI/PCI express transparent bridge

Figure 2-2: PCE385 Main Board Component Layout



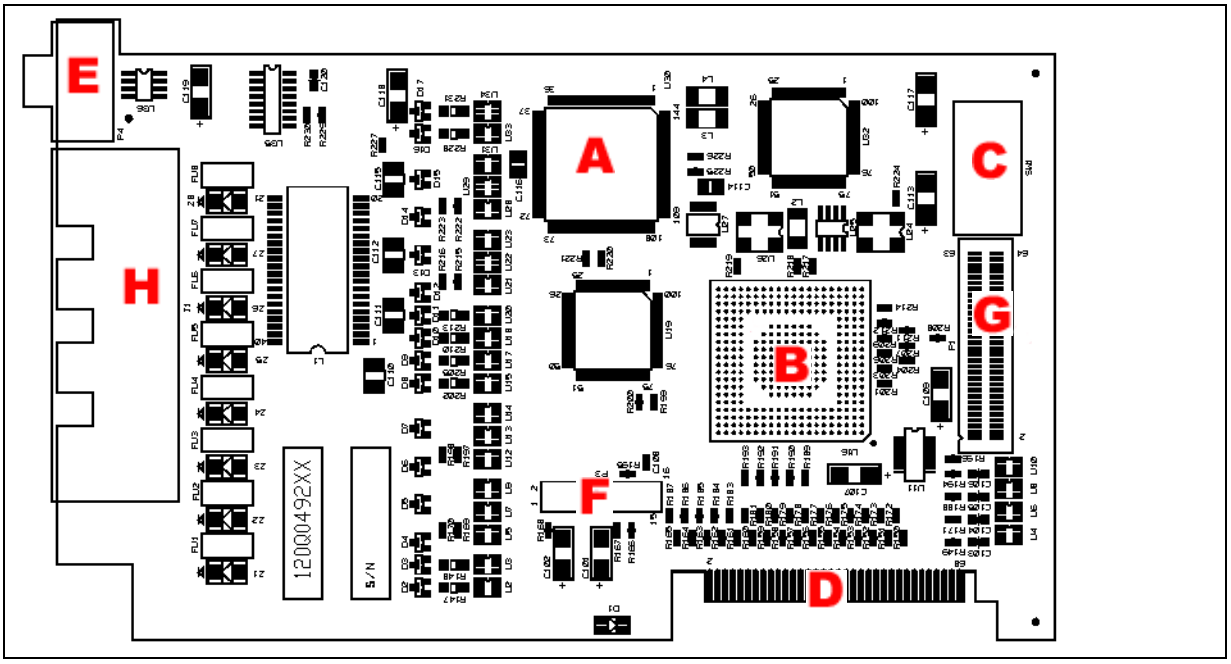
Daughter Board Component Layout

This section describes the principal components of the PCE385 daughter board (see Table 2-5: “PCE385 Daughter Board Component Layout Call Out Definitions” and Figure 2-3, “PCE385 Daughter Board Component Layout” on page 22.

Table 2-5: PCE385 Daughter Board Component Layout Call Out Definitions

Call Out Letter	Item	Description
A	Framer	T1/E1/J1 Framer
B	TDM Switch	H.100 TDM Compatible Switch
C	User Defined Switches	Application assigned values
D	H.100 Connection	Connection for H.100 cable
E	Micro 9-pin D Console Port Connection	Console port for hardware, software and application statuses
F	JTAG Connection	Programs PALs and Runs JTAG test for Hardware debug
G	Main Board Interface Connector	Electronic connection point for the daughter and main board
H	RJ-48C Connectors	T1 Interface Connections

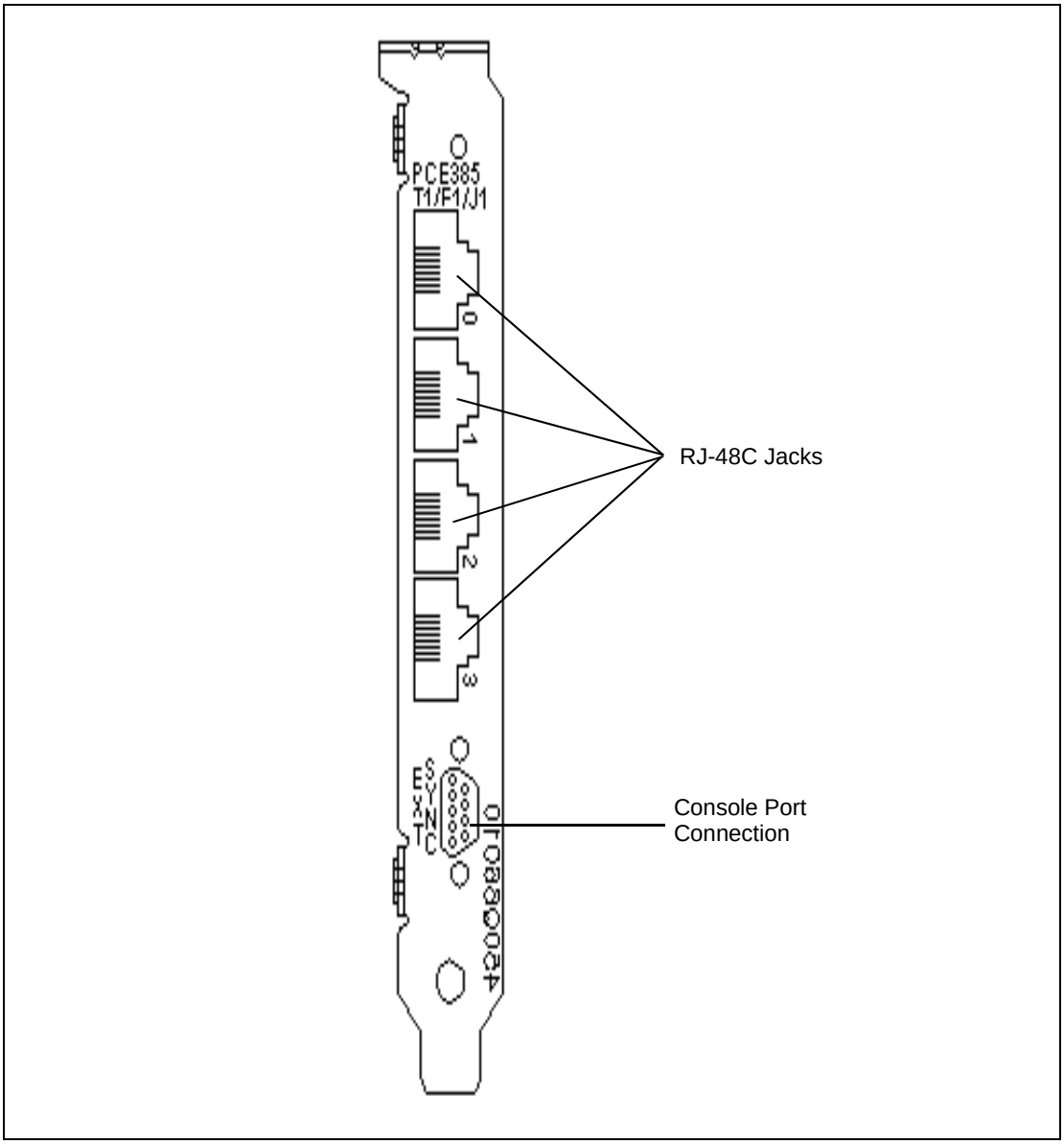
Figure 2-3: PCE385 Daughter Board Component Layout



Front Cover Plate

Installing and setting up the PCE385 requires working with the front cover plate (see Figure 2-4, “PCE385 Front Cover Plate Components” on page 23.)

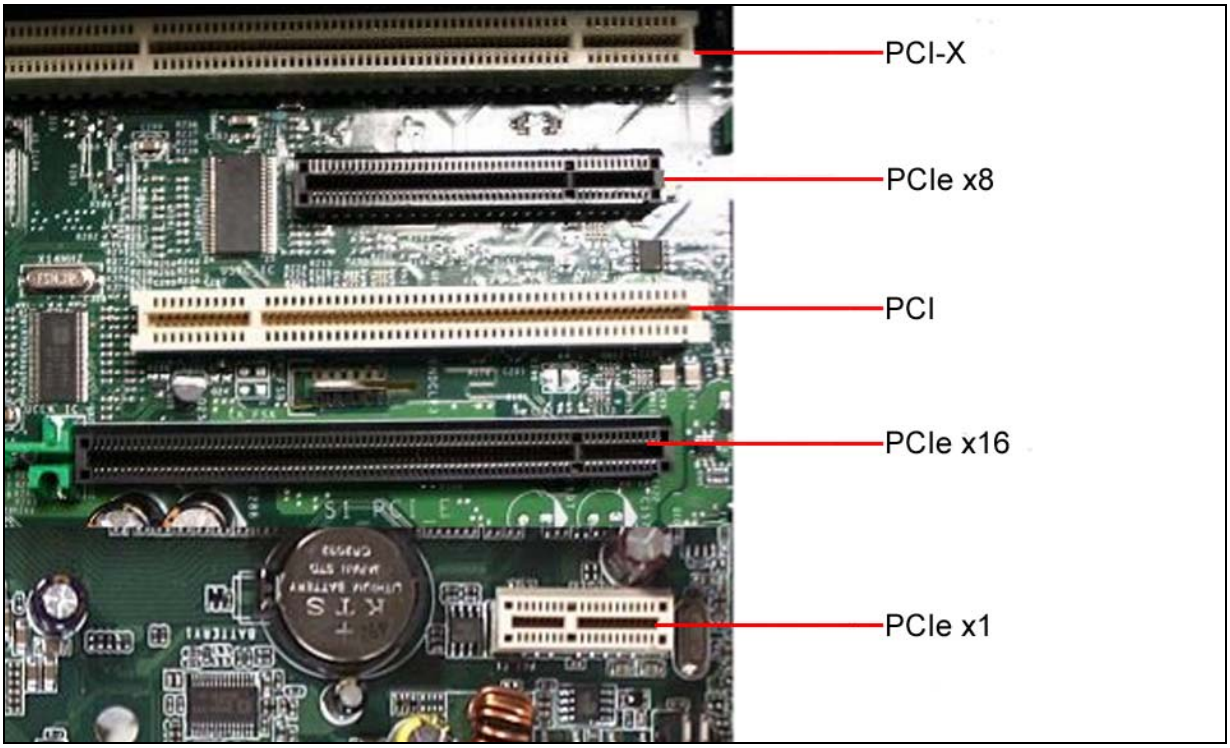
Figure 2-4: PCE385 Front Cover Plate Components



PCI Express Slots

The PCI Express vertical card-edge connectors are specified for Link widths of x1, x4, x8 and x16. These are not compatible with prior PCI interface standards such as PCI and PCI-X. Figure 2-5: "Types of PCI and PCI Express Slots on a PC Main Board" provides examples of the different types of PCI and PCI Express slots. The PCE385 edge connector utilizes an X1 lane interface. This is capable of up-plugging; that is, it may be inserted into an X2, X4, X8 or X16 slot. Installation is not restricted to an X1 slot. Further details are provided in “PCI Express Interface” on page 37

Figure 2-5: Types of PCI and PCI Express Slots on a PC Main Board



PCIe Slot Details

PCIe is a high-speed bidirectional peripheral interconnect that includes both a protocol and a layered architecture that has higher data transfer rates than the original PCI bus.

PCIe carries data in packets along two pairs of point-to-point data lanes, compared to the single parallel data bus of traditional PCI that routes data at a set rate. Bit rates for PCI Express reach 1.25 Gbps per lane direction, which equates to data transfer rates of approximately 400 MBps per lane.

The PCIe bus replaced the standard PCI bus when computer processor speeds started to exceed the capabilities of the PCI architecture. The PCI is a shared parallel bus architecture, the PCIe is a high speed serial switched architecture.

Note: *Sometimes abbreviated “PCX”, PCI Express is not the same as “PCI-X”. Because the abbreviations can be confusing, the accepted usage is “PCI-E” or “PCIe”.*

Chapter

3

Installation

Overview

This chapter provides information required to install the PCE385 in a PCIe slot on a PC.

Topics in this chapter include:

Unpacking the System

Caution:
If the packing container looks damaged, immediately contact the company responsible for the shipping and report the damage before opening and unpacking the container. It is recommended that you also notify Performance Technologies Customer Support (see “Customer Support and Services” on page 15).

Before you connect your system and install the software, verify using the packing slip that you received all the components. If you are missing any of the components shown on the packing slip, contact your Performance Technologies Sales Representative immediately.

Installing the PCE385

This section contains installation information for the PCE385 board.

Warning:

Make sure that the computer is turned off and the power cord is detached from the host chassis prior to installing the PCE385 board. Attempting to install the PCE385 in a computer chassis that has the power still active could result in electrical shock causing serious injury or death.

Warning:

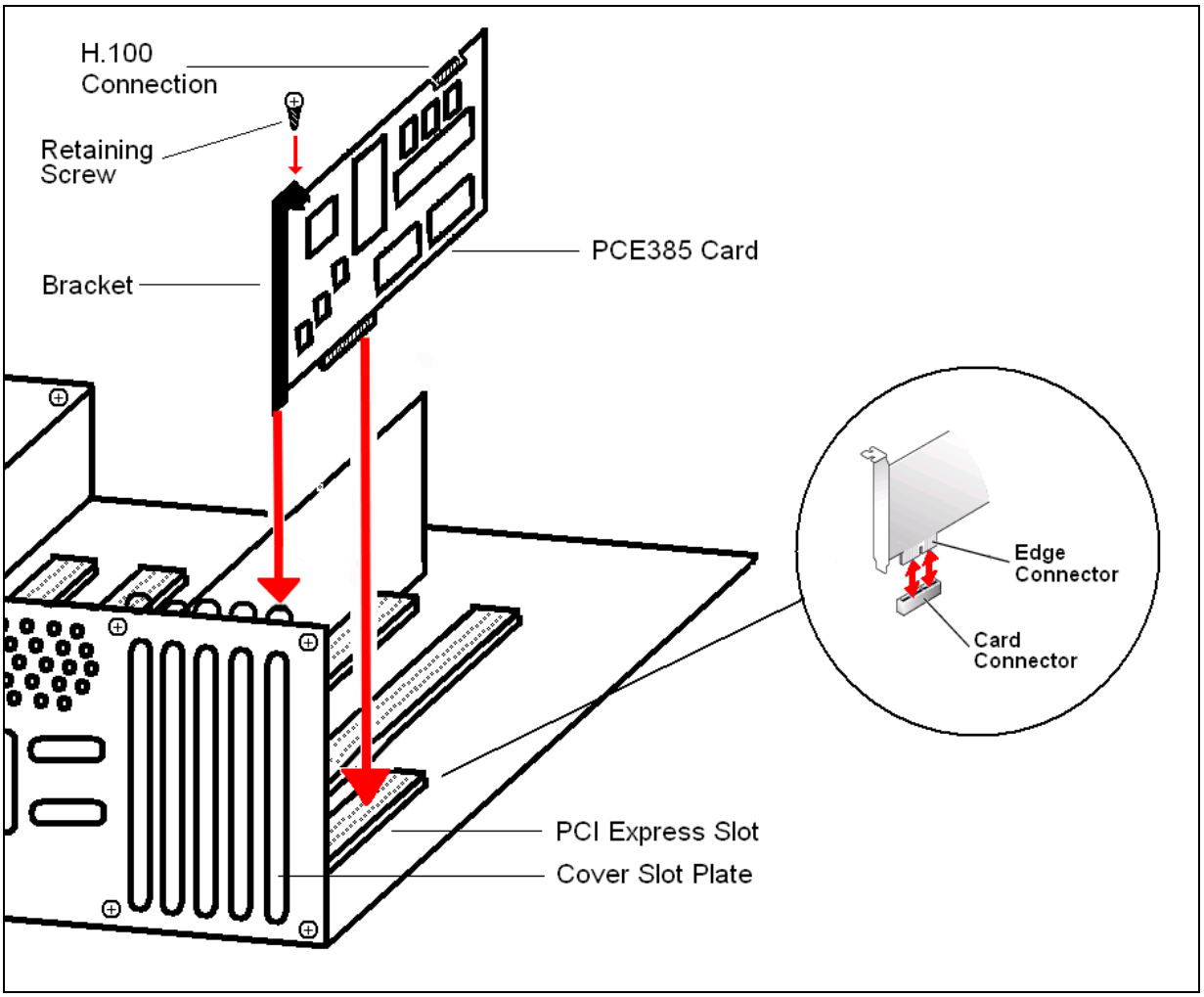
Use anti-static grounding straps and anti-static mats when you are handling the PCE335 to help prevent damage due to electrostatic discharge. Electronic components on printed circuit boards are extremely sensitive to static electricity. Ordinary amounts of static electricity generated by your clothing or work environment can damage the electronic equipment.

Use the following procedure to install the PCE385 in a computer chassis.

1. Turn off the power for the computer on which you are installing the PCE385.
2. Remove the rear cover or side panel that allows access to the inside of the computer by removing the retaining screws or other cover lock down devices.
3. Locate an empty PCI Express slot and remove the corresponding slot cover plate from the outside of the PC chassis. Note that the PCE385 is capable of up-plugging. See “PCI Express Slots” on page 24 for information about PCIe slots and up-plugging.
4. Line the PCE385 board up with the slot and press the PCE385 into the PCI Express slot with the cover plate end of the board over the edge of the main board. Use caution when pressing so you do not snap the board (see Figure 3-1, “PCE385 Insertion Diagram” on page 27).
5. Use the retaining screw that was with the cover plate and screw the board cover plate to the chassis.

   This step secures the board to the chassis and prevents the board from moving. When you are finished this step, the PCE385 is installed. You can now apply power to the PC and the PCE385 is ready for application development.

Figure 3-1: PCE385 Insertion Diagram



Chapter

4

Development Environment

Overview

This chapter provides information about the board memory, interface, features, flash memory, operating modes, and Framer and LIU information required to develop applications. This chapter also provides information about the JTAG/BDM Debug port and the Console port.

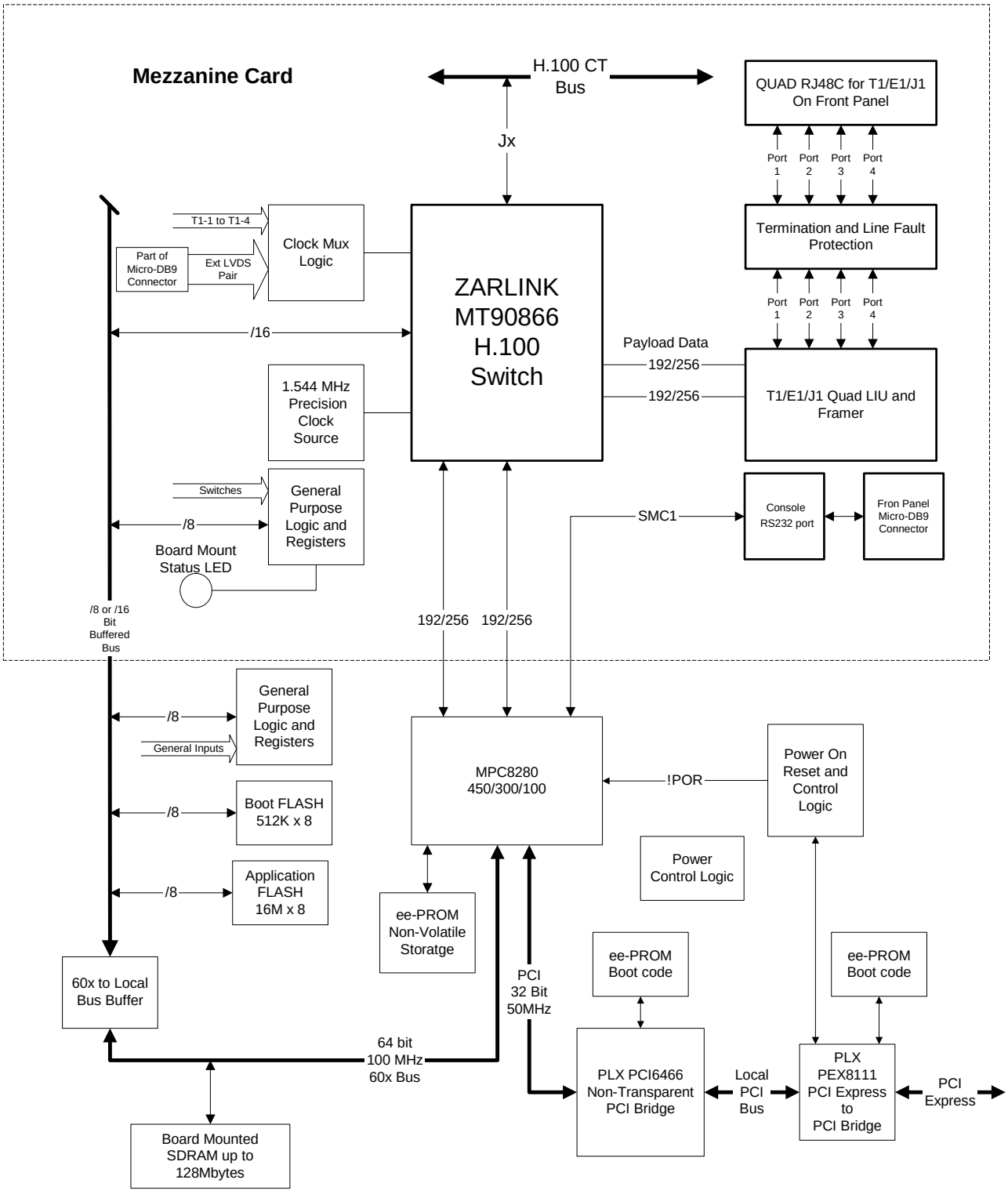
Note: *The information contained in this chapter should be used in conjunction with the software you purchased from Performance Technologies.*

Topics in this chapter include:

PCE385 Architectural Overview

The PCE385 is composed of a PCI Main Board and a Mezzanine Board. See “Main Board” on page 31 and “Mezzanine Board” on page 31. See Figure 4-1.

Figure 4-1: PCE385 Architectural Block Diagram



Main Board

The PCE385 main board contains all of the active components relating to PowerQUICC II communications microprocessor core operations, including the:

- Communication processor
- SDRAM memory
- Boot and Application Flash
- PCI bus interface
- General control and option register logic

For information about the logic on this board, refer to the *Freescale MPC8280 User's Manual.*

Mezzanine Board

The PCE385 mezzanine I/O board provides the:

- T1/E1 LIU and Framer
- H.100 Controller
- receiver and transmitter metallic connectors (RJ-48C)
- passive components including the telephony line protection

T1/E1 LIU and Framer

The on-board T1/E1 LIU and Framer receives and transmits framed serialized T1/E1/J1 bit streams, recover timing information, and demultiplex the T1/E1 data directly to the DS-0 level. The result is that 192/256/192 T1/E1/J1 DS-0 timeslots can be terminated in different manners. The data can be passed to the PCI bus as terminated data or to the H.100 bus as DS-0s in a TDM stream.

During receive, the LIU and Framers accept T1/E1 or J1 bipolar signals, perform equalization, convert the signals into binary digital data streams, receive frame synchronization, data recovery, frame overhead extraction, and provide data connection paths to the various on-board terminating interfaces using the H.100 controller.

During transmit, the LIU and Framers accept digital data from one of the terminating interfaces through the H.100 controller. The LIU and Framers perform frame generation overhead insertion, and convert the digital clock and data to the appropriate wave shapes for transmission as bipolar T1/E1 or J1 streams.

H.100 Controller

The H.100 controller interfaces the T1/E1 LIU and Framers to the TDM of the MPC8280 processor. Each local time slot can be assigned to any of the possible 4096 H.100 external time slots or reassigned to any other local time slot.

These possible time slots are based on the memory locations in the TDM switch to accommodate all of the time slots (DS0s) on the H.100 backplane (ribbon cable). The calculation is derived from 32 DS0s max per frame x 4 individual T1 or E1 connections muxed to the backplane per H.110/H.100 data bit x 32 data bits per H.100/H.110 backplane.

The PowerQuicc II CPM implements channel routing and time division multiplexing (TDM) to its internal communications controllers using its Internal Timeslot Assigner (TSA). Data can be routed to and from the various CPM communications controllers. The controllers used in the PCE385 application include:

- Two multi-channel communications controllers (MCC)
- One fast communications controller (FCC)
- Advanced CPM protocol specific functions, controlled by internal and downloadable firmware

Reset Logic

The reset logic for the PCE385 includes five major resets caused by the external PCI Express bus. They are:

- Power On Reset
- Hard Reset
- Soft Reset
- PCI Express Interface Resets
- Peripheral Resets

Table 4-1: “Reset Priorities” describes the priorities for the on-board resets.

Table 4-1: Reset Priorities

	PORESET	HRESET	SRESET	PCIRST	H100RST	QFALCRST
PORESET	---	X	X	---	X	X
HRESET	---	---	X	---	X	X
SRESET	---	---	---	---	X	X
PCIEXPRST	X	X	X	X	X	X
PCI6466RST	---	X	X	---	X	X

Power On Reset

The power on reset signal, PORESET#, is asserted by the baseboard Control Logic PAL in response to a PCI Express reset.

Hard Reset

The hard reset signal, PQ_HRESET#, is generated by the PowerQUICC II communications microprocessor. The communication processor generates PQ_HRESET# in response to any of the following (when enabled):

- Power on reset
- Software watchdog reset
- Bus monitor reset
- Checkstop reset

Soft Reset

The soft reset signal is accomplished by asserting the PQ_SRESET# signal. The signal is distributed to the MPC8280, Control logic PAL, the P9-A2 Analyzer Connector and the COP8 JTAG header for the debug port. The signal sources for PQ_SRESET# include the MPC8280 and the debugger port.

The MPC8280 asserts this signal in response to any power on reset or hard reset condition. The effect of soft reset on the processor differs from the power on reset or hard reset and it is outlined in the *Freescale MPC8280 User's Manual* in the *Reset* chapter.

PCI Express Interface Resets

The PEX8111 receives primary resets from the PCI Express Root Complex on the PCI Express bus by the PCE_PERST# signal. This reset input is buffered on the board, and sent to the mainboard Control Logic PAL and the PEX8111. The PEX8111 interprets this signal as a Fundamental Reset. The Fundamental Reset resets all of the PEX8111 internal logic and it initializes the rest of the PCE385 logic to the Power On Reset condition. This condition remains on the MPC8280 as long as the PCE_PERST# signal is asserted to the board.

The PEX8111 supports Hot Reset due to Link training Control Reset, which is a primary reset due to the physical layer mechanism. This reset causes all transactions on the PCI Express side of the interface to stop and all of the cycle state machines to reset. The PEX8111 also supports Primary Reset due to Data Link Down in a similar manner.

All of these reset conditions generate a primary PCI Reset (PRI_PLX_PCIRST#) downstream to the PCI6466. For a complete description of the primary PCI Express reset on the PEX8111, refer to the *PLX PEX 8111 PCI Express-to-PCI Bridge Data Book*.

The PCI6466 has primary and secondary PCI resets. The primary PCI reset (PRI_PLX_PCIRST#) is driven into the PCI6466 by the PEX8111. Receipt of this signal by the PCI6466 causes the PCI6466 primary PCI bus to take a fundamental reset. In addition, the PCI6466 issues a secondary PCI reset (S_PCI_RSTOUT#) as long as the primary input is true.

The S_PCI_RSTOUT# signal is connected to the Control Logic PAL and it causes a power on reset pulse to be applied to the MPC8280. This reset is caused by receipt of the primary PCI reset and by a bit in one of two registers in the PCI6466. The registers are the Diagnostic Control register Chip Reset and Bridge Control Secondary Reset (Nontransparent mode—DCNTRL[0]=1; PCI:D9h and BCNTRL[6]=1; PCI:42h, respectively). S_RSTOUT# remains asserted until the SecondaryReset Output Mask bit is cleared (Nontransparent mode—DCNTRL[3]=0; PCI:D9h). This method is the preferred method to cause a "Software Reset" of the PCE385.

Peripheral Resets

Each peripheral chip on the PCE385 has an individual reset line. The peripheral resets are driven by the daughter board PAL logic. The resets are all set to a reset state by anything that creates PQ_SRESET # on the PCE385 board. The devices are held in reset until the appropriate bit in the general-purpose registers is set. Table 4-2, "Peripheral Resets" on page 34 describes the individual peripheral reset signals, the power up reset state and the bit that controls the device in the general-purpose registers.

The PCE385 has a Freescale MPC8280 Communications Processor Unit (CPU) on the main board portion of the assembly. This CPU is the primary controller on the PCE385. The CPU provides the PowerPC CPU core, the Communications Processor Module (CPM), and the 60X bus processor bus controller. The CPU controls the Synchronous DRAM (SDRAM) and the PCI side of the PEX8111 PCI Express Interface Controller by its direct connections. The CPU also controls all of the on-board peripheral chips by a buffered data and address bus.

Table 4-2: Peripheral Resets

Peripheral	Reset Signal Name	PQ_SRESET# State	Register Bit Name
H.100 Switch	!H100_RST	0	h100_rst-n
Quad FALC 1	!QFALC1_RST	0	qfalc1_rst_n

Memory Map

The memory map is defined by the PCE385 Address Decode Scheme. There are several levels of Address Decode built into the PCE385. The first level and primary decode is performed by the System Interface Unit (SIU) of the communication processor. One of the SIU subsections is the memory controller. The memory controller is responsible for controlling a maximum of twelve memory banks shared by a high performance SDRAM machine, a General-Purpose Chip-select Machine (GPCM). This GPCM supports several types of interface to Synchronous DRAM (SDRAM), EPROM, Flash EPROM, burstable RAM, regular DRAM devices, extended data output DRAM devices, and other peripherals. This flexible memory controller allows the implementation of memory systems with very specific timing requirements.

- The SDRAM machine provides an interface to synchronous DRAMs, using SDRAM pipelining, bank interleaving, and back-to-back page mode to achieve the highest performance.
- The GPCM provides interfacing for simpler, lower-performance memory resources and memory-mapped devices. The GPCM has inherently lower performance because it does not support bursting. For this reason, GPCM-controlled banks are used primarily for boot loading and access to low-performance memory-mapped peripherals.

The primary control of the devices served by the memory controller is through the communication processor external Chip Select lines. The specific memory controller set ups are defined for each type of device in the section of the specification that describes the device. Table 4-3: “MPC8280 Chip Select Assignments” represents the primary address decode of the external chip select lines.

Table 4-3: MPC8280 Chip Select Assignments

Chip Select Line	Controlled Device	Address Range
CS#0	Flash Boot PROM	FFF0_0000 to FFF7_FFFF h
CS#1	SDRAM	0000_0000 to 07FF_FFFF h
CS#2	Not Used	
CS#3	Application Flash	1000_0000 to 10FF_FFFF h
CS#4	PAL General Purpose Registers	2000_0000 to 2000_00ff h

Table 4-3: MPC8280 Chip Select Assignments (Continued)

Chip Select Line	Controlled Device	Address Range
CS#5	QUAD FALC	2010_0000 to 2010_7FFF h
CS#6	H.100 Switch Chip	2020_0000 to 2020_7FFF h
CS#7	Not Used	
CS#8	Not Used	2030_0000 to 2030_7FFF h
CS#9	Not Used	2040_0000 to 2040_7FFF h
CS#11	Not Used	
None	PEX8111 mapped space	

Communication Processor Interrupt Sources

Several multifunction pins are used to supply the communication processor with the interrupts from the various direct-connect board peripherals. The !IRQ0 to !IRQ7 lines are used along with some of the port C interrupt-capable pins. The interrupt sources, for the most part, have multiple interrupt conditions. For complete information about interrupt causes, refer to the individual component subsections or the component user manual. Table 4-4: “Communication Processor Interrupt Sources” provides information about the connections from the peripheral devices to the communication processor.

Table 4-4: Communication Processor Interrupt Sources

IRQ Level	Pin Number	Controlled Device
!IRQ0	T1	NMI Interrupt from the Abort Jumper P3-4 to P3-5
!IRQ1	A22	Quad FALC 1 General Interrupt
!IRQ2	E21	Not Used
!IRQ3	D21	Not Used
!IRQ4	C21	PEX8111 General Interrupt
!IRQ5	B21	H.100 Switch FAIL_A, FAIL_B, LREF0 and LREF1 Fail
!IRQ6	A21	Not Used
!IRQ7	E20	Not Used
PC0	AB26	Not Used
PC1	AD29	Not Used
PC2	AE29	Not Used
PC3	AE27	Not Used

JTAG Support

The JTAG testing port on the MPC8280 supports the EST Common On-chip Processor (COP) debugger on the P4 connector. This connector supports the extended 16-pin COP debugger signaling, but the basic 10-pin signaling devices can be used with an interposing adapter. Table 4-5: “JTAG P4 Pinouts” provides information about JTAG P4 pinouts.

Table 4-5: JTAG P4 Pinouts

Pin Number	Signal Name
1	PQ_TDO - JTAG Test Data Out Signal
2	!PQ_QACK- Quiescent State Acknowledge, not supported
3	PQ_TDI- JTAG Test Data In signal
4	!PQ_TRST- JTAG Reset and Tristate signal
5	!PQ_QREQ - Quiescent State Request-
6	V3V
7	PQ_TCK - JTAG Test Clock
8	No Connection
9	PQ_TMS-JTAG Test Mode Select
10	No Connection
11	PQ_SRESET# - MPC8280 Soft Reset
12	Ground
13	PQ_HRESET# - MPC8280 Hard Reset
14	No Connection
15	!CHKSTPO - Checkstop output, Not supported
16	Ground

Note: *All of the control signals are terminated to prevent false assertion when no JTAG controller is connected.*

SDRAM

The Synchronous Dynamic Random Access Memory (SDRAM) memory bank has individual chips mounted on the component and circuit sides of the base board. The SDRAM architecture provides the ability to:

- burst data, synchronously, at a high data rate with automatic column address generation
- interleave between internal banks in order to hide PRECHARGE time
- randomly change column addresses on each clock cycle during a burst access

The total SDRAM memory is 128 MB. This SDRAM memory is arranged in four parallel bytes to give the data bus a 64-bit total width. The integral SDRAM controller takes care of all low level SDRAM operations including row and column multiplexing, precharge times, and refresh.

PCI Express Interface

The PCE385 uses a PCI to PCI Express Bridge to gain connectivity to the PCI Express Root Complex. This Root Complex connects through the PCI Express connector located on the lower edge of the assembly. The PCI Express interface, a PLX PEX8111, is used in its forward mode relative to the PCI Express Root Complex. The interface is also configured in the Transparent mode relative to the root complex. The PEX8111 translates all accesses to and from the Root Complex into local 32-bit PCI accesses. These accesses are passed to a nontransparent PCI-PCI bridge (PCI6466) before they are presented to the MPC8280 on-board CPU. The nontransparent bridge allows the board assembly to hide the fact that there is a private PCI bus behind the bridge. The nontransparent mode also allows the PCE385 to identify itself to the ROOT complex with a PTI Device and Vendor ID. This configuration allows the operating system to recognize the board and load the correct system drivers. The following sections describe the interface, the two bridge connections, and the modes of operation:

Physical Layer (Layer 1)

Layer 1, the Physical Layer (PHY) defines the electrical characteristics of PCI Express. This layer is the basic transmission unit, which consists of two pairs of wires, called a “lane”. Each pair allows for unidirectional data transmission 1.25 Gbps, so the two pairs combined provide 2.5 Gbps full-duplex communication, without the risk of transmission collision.

Data Link Layer (Layer 2)

Layer 2, the Data Link Layer (DLL) defines the data control for PCI Express. This data link layer provides link management and data integrity, including error detection and correction. The layer calculates and appends a Cyclic Redundancy Check (CRC) and a sequence number to the information sent from the data packet. The CRC verifies that data has been transmitted correctly from link to link. The sequence number allows proper ordering of the data packets.

Transaction Layer (Layer 3)

Layer 3, the Transaction Layer (TL) connects the lower protocols to the upper layers. This Transaction Layer appears to the upper layers of the PCI.

The Transaction Layer packetizes and then pre-appends a header to the payload data. This layer also includes the read and write commands and prior sideband signals (for example, interrupts and power management requests).

To achieve code compatibility with PCI, PCI Express does not modify the transaction layer.

Forward Mode

In Forward Mode, the configuration cycles originate from the PCI Express link through the bridge chip and then to the PCI Bus segment.

Transparent Mode

In addition to operating as a forward bridge, PEX8111 also operates as a transparent bridge (through pin strap).

In Transparent Mode, the bridge electrically isolates the two domains (PCI Express and PCI) while preserving the command and addressing functions of the transaction.

Nontransparent Mode

The PCI6466 bridge operates as a nontransparent bridge (through pin strap).

In Nontransparent Mode, the bridge isolates processor domains on each side by providing a Type 0 Configuration Header to each CPU on either side of the bridge. Data is transferred between the domains through the bridge using address translation. This transfer can occur in either the upstream or downstream direction.

As a nontransparent bridge, configuration accesses occur on both the PCI bus and the PCI Express port. There are two “hosts” in this configuration and each can access or send data to devices on both sides of the bridge. Each host has its own memory map for the devices to which it has access.

Features from PEX8111

In the PCE385 implementation the PEX8111 supports these features:

- PCI Express Interface (one port and one lane interface)
- 2.5 Gbps transfer rate
- external RefClk input
- external PERST# input
- one-lane status indicators
- PCI interface
- JTAG interface
- 32-bit support
- clock rates of up to 66 MHz

PCI Express Interface

The PCE385 is configured as x1 interface on the PEX8111 PCI Express board interface connector. Table 4-6: “PEX8111 PCI Express Connections” describes the interface signals that are supported on the PCI Express connector.

Table 4-6: PEX8111 PCI Express Connections

PCI Express Pin Number	Signal	Description
A1	PRSNT1#	Hot Plug presence detect
A2	+12v	+12V power
A3	+12v	+12V power
A4	GND	Ground
A5	JTAG2#	TCK, Test Clock, not used
A6	JTAG3#	TDI, Test Data Input, not used, looped to TDO
A7	JTAG4#	TDO, Test Data Output, not used looped to TDI
A8	JTAG5#	TMS, Test Mode Select, not used
A9	3.3V	3.3V Power
A10	3.3V	3.3V Power
A11	PERST#	PCI Express Fundamental Reset
A12	GND	Ground
A13	REFCLK+	Reference Clock differential pair
A14	REFCLK-	
A15	GND	Ground
A16	PERp0	Receiver differential pair, Lane 0
A17	PERn0	
A18	GND	Ground
B1	+12v	+12V Power
B2	+12v	+12V Power
B3	RSVD	Reserved
B4	GND	Ground
B5	SMCLK	SMBus clock
B6	SMDAT	SMBus data
B7	GND	Ground
B8	3.3V	3.3V Power
B9	JTAG1#	JTAG Test Reset, not used.
B10	3.3Vaux	3.3V auxiliary power, not used.

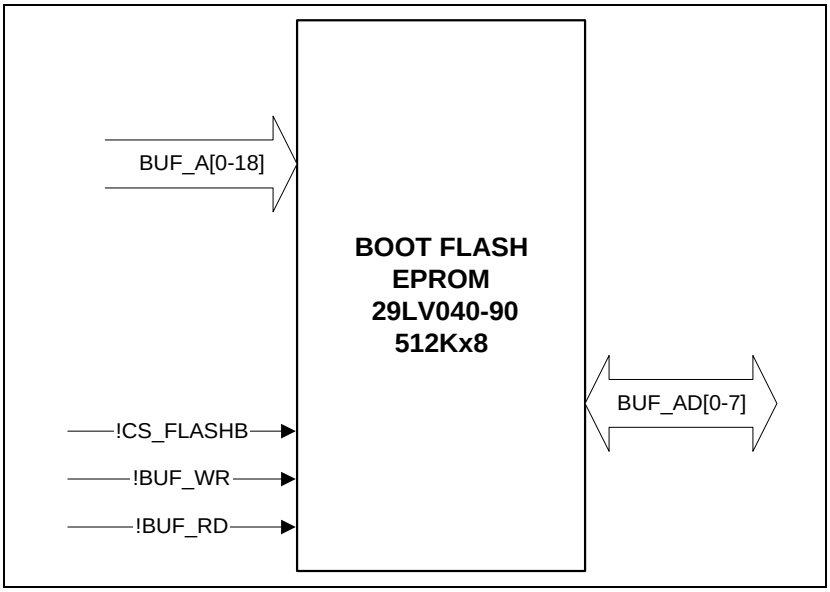
Table 4-6: PEX8111 PCI Express Connections (Continued)

PCI Express Pin Number	Signal	Description
B11	WAKE#	Signal for Link Reactivation, not used.
B12	RSVD	Reserved
B13	GND	Ground
B14	PETp0	Transmitter Differential Pair Lane 0
B15	PETn0	
B16	GND	Ground
B17	PRSNT2#	Hot Plug Presence Detect
B18	GND	Ground

JTAG Interface

The JTAG interface (see Figure 4-2: "JTAG Interface") on the PEX8111 is bypassed on the connector to preserve the remaining external chain.

Figure 4-2: JTAG Interface



Boot Flash Memory

The Boot Flash Erasable Programmable Read Only Memory (EPROM) is used to store the initial startup code for the CPU of the PCE385 (the MPC8280). This EPROM is socketed and mounted on the base board at position U11. The Boot Flash is a nonvolatile memory that has the following general characteristics.

The Boot Flash EPROM is a single power supply, 4 Mbit, 3.0 Volt-only Flash memory device organized as 524,288 bytes. The data appears on DQ0-DQ7 of the buffered memory bus.

- The device is in a 32-pin PLCC package.
- All read, erase, and application operations are accomplished using only a single power supply. Internally generated and regulated voltages are provided for the application and erase operations.
- The device is entirely command set compatible with the JEDEC single-power-supply Flash standard.

The Boot Flash EPROM is accessed by the MPC8280 through the Buffered Data bus. This Buffered Data bus supplies a buffered MPC8280 address and a bidirectional 8-bit or 16-bit data bus. The MPC8280 provides the CS_FLASHB#, which acts as the device chip enable. The Control Logic PAL logic provides the !BUF_RD, which acts as the device output enable and !BUF_WR, which acts as the write enable. The PCE385 has a write protect feature that does not allow the !BUF_WR signal to activate unless the flash_wp bit is set in the General Purpose registers. After a reset, writing to the Boot Flash EPROM is disabled, by default. The the GCPM wait state programming provides the timing for the read and write cycle. The Boot Flash EPROM does not generate any cycle termination signal.

This section provides information about:

General Boot Flash Information

Flash access in the Read mode is done as any normal PROM device.

The programming or write operations are entirely command set compatible with the Joint Electron Device Engineering Council (JEDEC) single-power-supply Flash standard. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data required for the programming and erase operations. Device programming occurs by executing the program command sequence. This sequence initiates the Embedded Program algorithm, which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin.

Device erasure occurs by executing the erase command sequence. This command initiates the Embedded Erase algorithm, an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During an erase operation, the device automatically times the erase pulse widths and verifies proper cell margin. The host system can detect whether a program or erase operation is complete by reading the DQ7 (Data/Polling) and DQ6 (toggle) status bits. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The sector erase architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors using programming equipment. Device hardware data protection measures include a low Common Collector Voltage (VCC) detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of the sectors of memory.

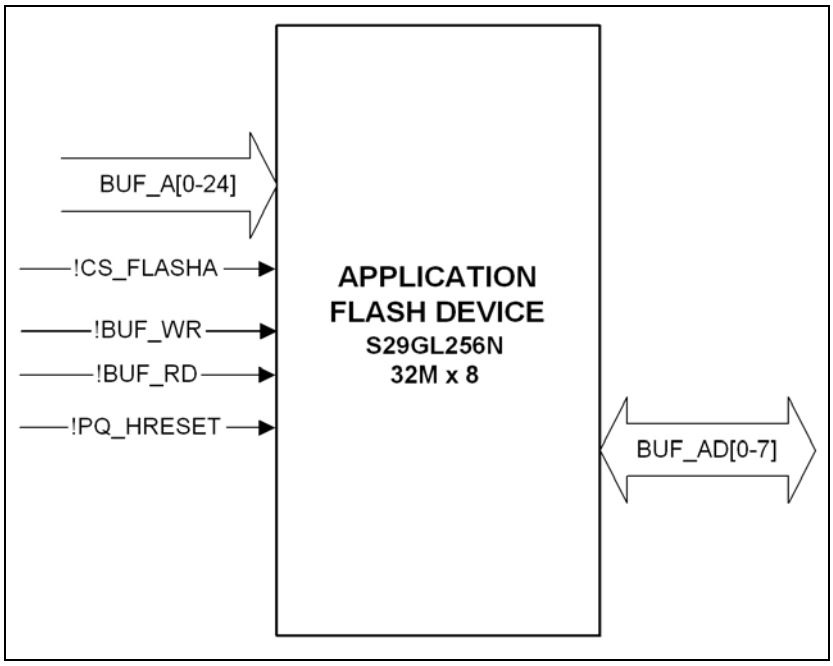
The Erase Suspend feature enables the user to put the erase operation on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

Application Flash Memory

The Application Flash PROM (see Figure 4-3, “Application Flash Memory” on page 43) stores application code that is not executed at boot time. This Application Flash PROM is permanently mounted to the main board at position U23. The Application Flash is a nonvolatile memory that has the following general characteristics:

- A single power supply, 32 MB, 3.0 Volt-only Flash memory device.
- DQ0-DQ7 on the buffered data bus for Read accesses to the device.
- 256 blocks of byte wide data storage for writing purposes. Each storage blocks has 128 KB of storage.
- Common Flash Interface (CFI) and a Scalable Command Set (SCS) blocks perform the writing and erasing.
- Internally generated and regulated voltages for the program and erase operations.
- A 64-pin FBGA.

Figure 4-3: Application Flash Memory



General Application Flash Information

Flash access in the read mode is done as any normal PROM device.

Selecting, writing and erasing the blocks is done by using a Common Flash Interface (CFI) and a Scalable Command Set (SCS). For information about the command set and the programming strategy, refer to the Intel *Spansion S29GL256N MirrorBit Flash Family Datasheet*.

TDM Clock Distribution and Control

The TDM clock distribution is centralized about the Zarlink MT90866 H.100 TDM switch located on the mezzanine I/O board. This MT90866 generates all of the local TDM Frame Pulses and data clocks. The MT90866 uses a variety of clock sources to lockup its internal Digital Phase Locked Loop (DPLL) to a system reference. This DPLL lockup ability ensures that the data stays in synchronization with the system and no timing slips occur during data transfers on the board.

H.100 DPLL

The DPLL is the core of the MT90866. This DPLL is directly driven by a 20 MHz 25 ppm signal as its primary clock input. The DPLL accuracy allows the H.100 switch to function as a Stratum 4 Enhanced clock source when it runs in a free-run mode. In a normal integration into a Telephony system, synchronized timing is maintained by locking the PLL to a system-supplied reference. Table 4-7: “H.100 DPLL Operating Specifications” provides information about some of the significant DPLL operating specifications.

Table 4-7: H.100 DPLL Operating Specifications

Parameter	Value
Acceptable Reference Clock Input Frequencies	1.544 MHz, 2.048 MHz or 8 kHz per AT&T TR62411
Skew Control	8 taps @ 1.9 ns each, allows 0 to13.3 ns total skew adjustment between reference input and clock outputs. This adjustment translates to static phase offset of 1.28 us to 1.293 us for reference clock input of 1.544 MHz. For a reference clock input of 8 kHz or 2.048 MHz, the static phase offset is 960 ns to 973 ns.
Phase Offset, dependent on reference clock frequency	For 1.544 MHz reference clock, maximum phase offset +/- 1.28 us, minimum phase adjustment 10 ns. For 8 kHz or 2.048 MHz reference clock, maximum phase offset +/- 0.96 us, minimum phase adjustment 7.5 ns.
Phase Slope Limiter	Maximum phase slope response for input transient 4.6 ns per 125 us. Meets AT&T TR62411 standard.
Loop Filter	Equivalent to a first order low pass filter with 1.52 Hz cutoff.
Intrinsic Jitter	6.25 nspp for the 80 MHz master clock.
Jitter Transfer	Rate limited by Phase Slope Limiter to 4.6 ns/125 us. Jitter Transfer Function Cutoff frequency 1.52 Hz with slope of 20 db/decade. For the actual curves and the UI calculations, refer to the *Zarlink MT90866 Data Sheet*
Frequency Accuracy	Master Clock/ppm + DPLL/ppm= 25+.03=25.03 ppm of selected frequency.
Holdover accuracy	Master Clock/ppm + DPLL/ppm= 25+.03=25.03 ppm of selected frequency.
Locking Range	+/- 273 ppm
Maximum Time Interval Error (MTIE)	21 ns for every reference switch.
Phase Continuity	Maintained to within 4.6 ns at the instance (over one frame) of all reference switches.
Phase Lock Time	Less than 25 seconds

The DPLL can choose from several input sources to obtain the signal it needs to lock to. This mechanism supplies the system synchronization. These clock sources can be selected either internally using the reference multiplexer (MUX) internal to the part or externally by the mezzanine board Phase Alternation Line (PAL) logic. For additional information, refer to the *Zarlink MT9088 WAN Access Switch Data Sheet*.

Internal Reference Clock Sources

The internal reference selector multiplexer for the DPLL has a redundant configuration. The primary and secondary muxes both have access to the same set of clock sources. These sources include any of the six local reference inputs, the A and B Computer Telephony (CT) bus clocks or the CT Netreferences from the CT bus.

Internal Reference Monitors

There are two Reference Monitor circuits: one for the primary reference (PRI_REF) and one for the secondary reference (SEC_REF). These two circuits monitor the selected input reference signals and detect failures by setting up the adequate internal fail outputs (FAIL_PRI and FAIL_SEC). These fail signals are used in the auto-detect mode as the internal LOS_PRI and LOS_SEC signals to indicate when the reference has failed. The method of generating the failure depends on the selected reference:

- The “minimum 90 ns” check is done for all references. This check is the requirement by the H.100 specifications. The low level and high level of the reference must last for minimum 90 ns each.
- The “period in the specified range” check is done for all references. The length of the period of the selected input reference is checked if it is in the specified range. For the E1 (2.048 MHz clock) or the T1 (1.544 MHz clock) reference, the period of the clock can vary within the range of 1 +/- 1/4 of the defined clock period which is 488 ns for the E1 clock and 648 ns for T1 clock. For the 8 kHz reference, the variation is from 1 +/- 1/32 period.
- The “64 periods in the specified range” check is done if the selected reference is E1 or T1. The selected reference is observed for long period (64 reference clock cycles) and checked if it is within the specified range (from 62 to 66 clock periods)

These reference signal verifications include a complete loss or a large frequency shift of the selected reference signal. When the reference signal returns to normal, the LOS_PRI and LOS_SEC signals return to logic low.

CT Clock and Frame Monitor Circuits

These monitor circuits check the period of the C8_A and the C8_B clocks and the FRAME_A and FRAME_B frame pulses. According to the H.100 signal specification, the C8 period is 122 ns with a tolerance of +/-35 ns measured between rising edges. If C8 falls outside the range (87 ns to157 ns), the clock is rejected and the fail signal (FAIL_A or FAIL_B) becomes high. The Frame pulse period is measured with respect to the C8 clock. The frame pulse period must have exactly 1024 C8 cycles. Otherwise, the fail signal (FAIL_A or FAIL_B) becomes high. These two signals are connected to the mezzanine board PAL logic and are two of the inputs that form the H.100 Interrupt to the MPC8280.

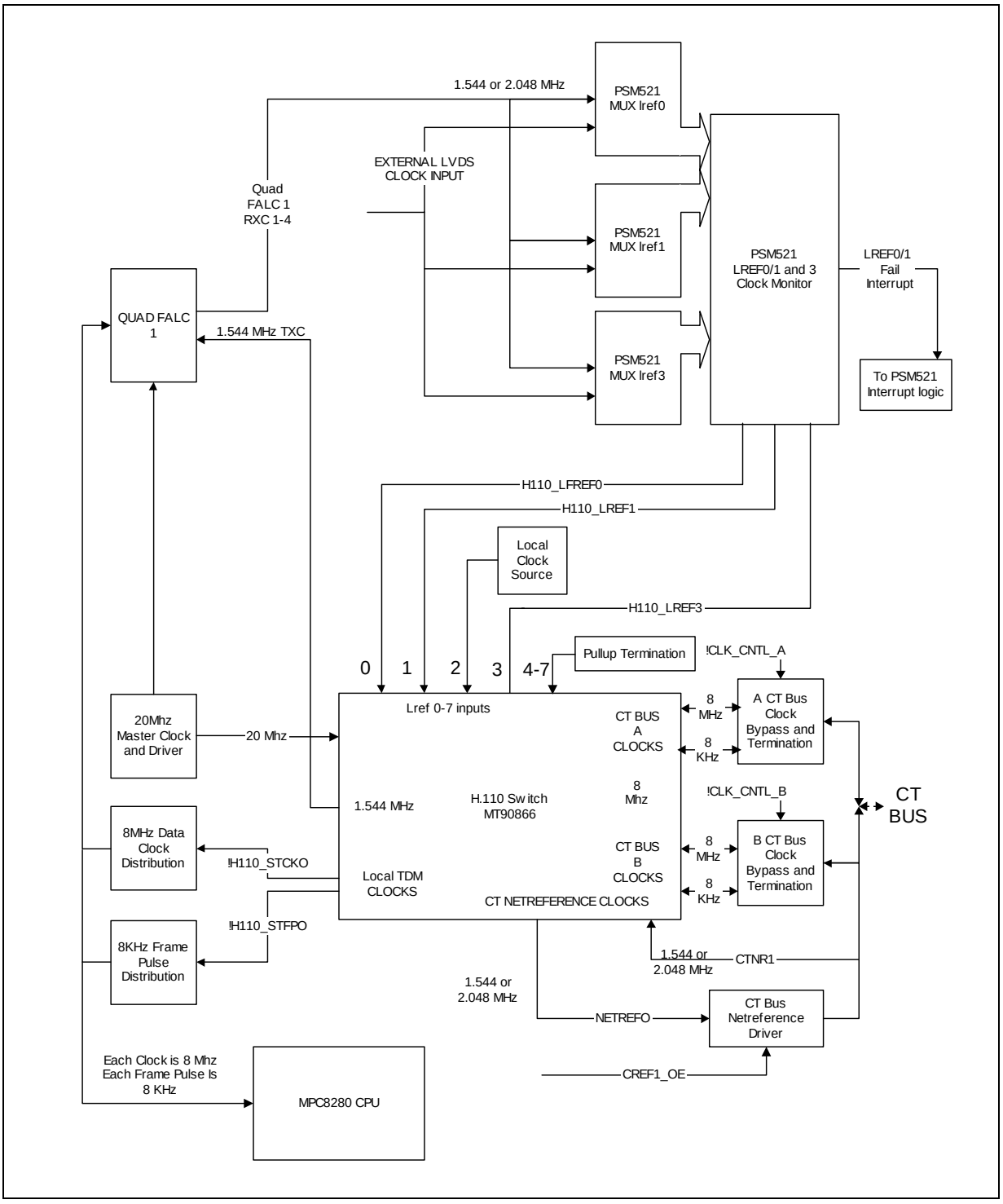
External Reference Clock Sources

These sources include any of the recovered clocks from the quad Framer and Line- interface Component (FALC) or the dual external Low Voltage Differential Signaling (LVDS) clock receivers. The recovered clocks are connected to the mezzanine board PAL logic, which is internally programmed to select one of four recovered T1 clocks from the framers or the Dual External LVDS Clock receivers. There are two of these selectors and they feed the H100_LREF0 and H100_LREF1 signals to the LREF0 and LREF1 inputs on the H.100 chip. NexusWare has provisions that allow the selection of LREF0 or LREF1 as the received clock source. For more information, refer to the *NexusWare Core Reference Manual*.

External Reference Clock Source Monitor

There is a set of clock monitors (see Figure 4-4, “External Clock Monitors” on page 47) in the mezzanine board PAL logic that check the external clock sources for validity. The Clock Timer Timeout Period Register contains a clock count value that is used to check for a valid time period for the local reference clocks, which are fed from the mezzanine board PAL select multiplexer to the H.100 Switch chip. The timer value is the maximum number of 20 MHz clocks that are allowed to elapse during the reference clock period. If the 20 MHz count is exceeded without seeing at least one valid local reference clock, the internal lrefxsts bit is set. This signal is one of the sources for the H.100 interrupt to the MPC8280. NexusWare has provisions to automatically setup the timer. For more information, refer to the *NexusWare Core Reference Manual*.

Figure 4-4: External Clock Monitors



H.100 Clock Operating Modes

Clock distribution and control circuitry support both master and slave modes of H.100 operation. The H.100 switch provides primary and secondary clock and frame synchronization sources for the local TDM streams. These sources are distributed to the MPC8280, E1/T1/J1 framers, PTMC module and clock monitoring circuitry. H.100 backplane clocks CT_C8_A and CT_C8_B are supported at 8 MHz operation exclusively. The local clocks are supported at 8 MHz operation exclusively.

In master mode, the H.100 switch accepts two of several local clock references that can be recovered by the E1/T1/J1 framers or generated by an optional local precision oscillator. These clocks can be divided to create an 8 kHz clock reference. These primary and secondary reference clocks are used to drive CTREF1 or CTREF2 to the H.100 backplane for primary or secondary master operation. The reference clocks are also provided to a PLL that generates and drives the CT_FRAME_A or CT_FRAME_B synchronization, and CT_C8_A or CT_C8_B clock, to the H.100 backplane. The selected local reference clocks are monitored and cause an interrupt upon failure. Local status and masking is provided for these interrupt sources.

In slave mode, the H.100 switch accepts CTREF1, CTREF2, CT_C8_A and CT_C8_B clocks. One CTREF and one CT_C8 clock are selected for primary operation, while the alternate pair stand-by as secondary clocks.

Support is included to allow A-side and B-side source termination resistors on CT_C8_A/B and CT_FRAME_A/B to be bypassed.

The A and B side clock and the frame synchronization are monitored by the H.100 switch and failure causes the corresponding FAIL_A or FAIL_B signal to be asserted. This signal is intercepted and provided as an interrupt to the MPC8280. Local status and masking is provided for this interrupt source. A 20 MHz crystal oscillator is distributed to provide a 20 MHz clock for each of the H.100 switch, E1/T1/J1 framers, and general-purpose logic components. These clocks are dedicated clocks without control options.

This section provides information about:

- CT Netreference Sources
- H.100 Bus and Digital Switch
- MT90866 Digital Switch Overview
- Digital Switch Local TDM Streams Connection

CT Netreference Sources

The H.100 switch can also source the CT bus Netreference signal. The H100_LREF3 signal is supplied to the switch as the reference input for this function. This signal source includes any of the recovered clocks from the Quad FALC or the Dual External LVDS Clock receivers. The recovered clocks are connected to the mezzanine board PAL logic, which is internally programmed to select one of four recovered T1 clocks from the framers or the Dual External LVDS Clock receivers. These external clock sources are configured in NexusWare API. For more information, refer to the *NexusWare Core Reference Manual*.

H.100 Bus and Digital Switch

The PCE385 uses the Zarlink MT90866 digital switch to connect the various Time Division Multiplexing (TDM) interface streams together. This digital switch resides on the mezzanine I/O board. The digital switch has local side connections to the MPC8280 TDM I/O and the Quad FALC TDM bus. It connects to the 32 bit H.100 CT Bus on the backplane. The digital switch features:

- 3.3V operation with 5V tolerant inputs and I/Os
- 5V tolerant PCI drivers on CT-Bus I/Os
- 2,432 x 2,432 non-blocking switching among local streams
- 4,096 x 2,432 blocking switching between backplane and local streams
- 2,048 x 2,048 non-blocking switching among backplane streams
- rate conversion between backplane and local streams
- rate conversion among local streams
- backplane interface accepts data rate of 8.192 Mbps
- local interface accepts data rates of 2.048 Mbps, 4.096 Mbps or 8.192 Mbps
- sub-rate switching (2 or 4 bits) configuration for local streams at a data rate of 2.048 Mbps
- per-channel variable or constant throughput delay
- fully compliant to H.100 timing specification
- per-stream input delay, programmable for local streams on a per bit basis
- per-stream output advancement, programmable for backplane and local streams
- per-channel direction control for backplane streams
- per-channel message mode for backplane and local streams
- compatible with Stratum 4 Enhanced clock switching standard
- integrated PLL conforms to Bellcore Stratum 4 Enhanced switching standard
- holdover mode with hold over frequency of 0.07 ppm
- wander attenuation from 1.5 Hz
- Time Interval Error (TIE) correction
- H.100 Bus Master and Slave mode operation
- connection memory block programming for fast device initialization
- tristate control outputs for external drivers
- Pseudo-Random Binary Sequence (PRBS) pattern generation and testing for backplane and local streams

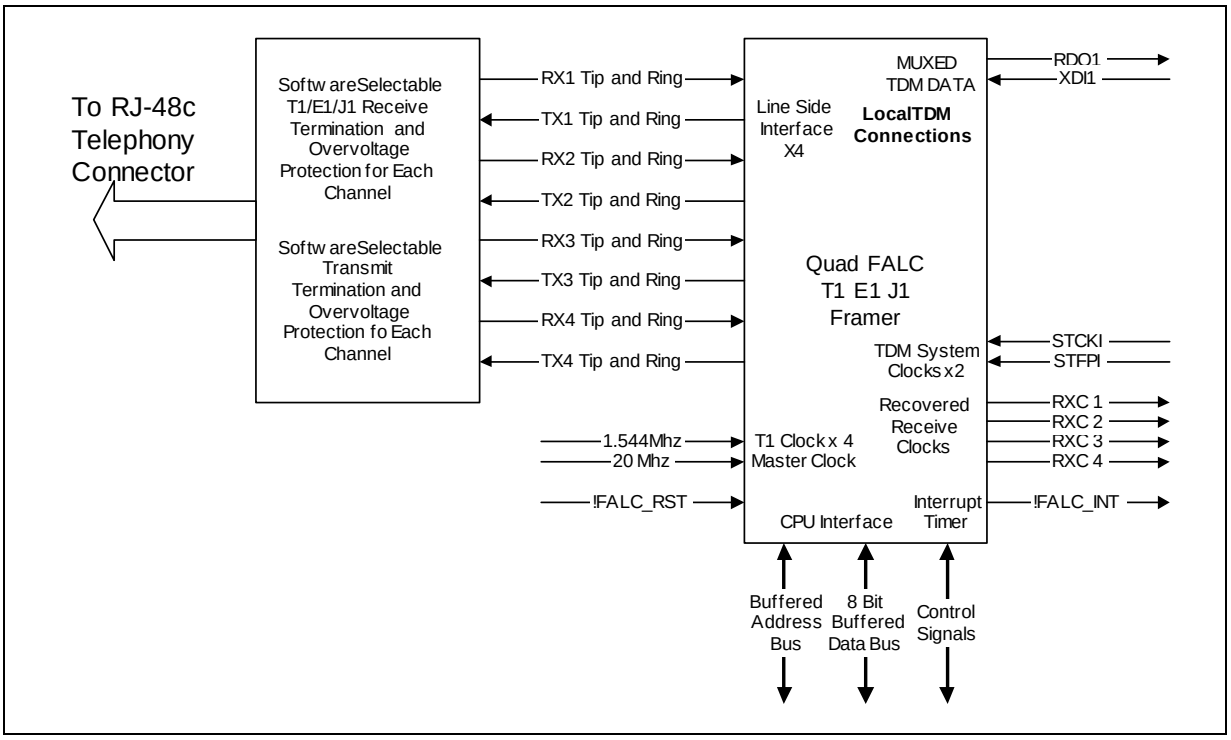
MT90866 Digital Switch Overview

The MT90866 digital switch (see Figure 4-5, “Quad Framer Block Diagram” on page 50) provides switching capacities of 4,096 x 2,432 channels between backplane and local streams, 2,432 x 2,432 channels among local streams and 2,048 x 2,048 channels among backplane streams. This digital switch has local connections to serial inputs and outputs that have 32, 64 and 128 64-kbps channels per frame with data rates of 2.048, 4.096 and 8.192 Mbps respectively. The digital switch has backplane connections to serial inputs and outputs have 128 64-kbps channels per frame with data rate of 8.192 Mbps.

The MT90866 digital switch also offers a sub-rate switching configuration that allows internal switching of two-bit wide 16 kbps data channels or four-bit wide 32-kbps data channels. This digital switch has features that are programmable on a per-stream or per-channel basis including message mode, input delay offset, output advancement offset, direction control, and high impedance output control.

The MT90866 digital switch is connected to the TDM peripherals, the CT Bus and the MPC8280. For more information, see “Digital Switch Local TDM Streams Connection” on page 50.

Figure 4-5: Quad Framer Block Diagram



Digital Switch Local TDM Streams Connection

The H.100-compatible digital switch serves as the focal point for all of the TDM streams from the various on-board peripherals. Table 4-8, “Digital Switch Local TDM Streams Connection” on page 51 provides more information about peripheral connections. The digital switch local I/O connections are grouped as inputs and outputs. The inputs and outputs are also sub-grouped in four groups. This grouping allows each sub-group to be run at one of the available data rates, 2.048, 4.096 or 8.192 Mbps. Some of the sub-groups also support two-bit and four-bit sub-rate switching when the group is run at the 2.048 Mbps data rate. The local TDM clock is

sourced from the DPLL of the digital switch and it is fixed at 8.192 MHz. The DPLL is locked to a system reference, which is programmable and chosen by the system architect. The local Frame Pulse signal is 8 kHz and is also supplied by the DPLL locked to the system reference. Table 4-8: “Digital Switch Local TDM Streams Connection” provides information about the peripheral connections for the PCE385 and the data rate at which the link operates.

Table 4-8: Digital Switch Local TDM Streams Connection

Group	Device	Switch Connection	TDM Data Rate	Interleaving Format
Group 1	Input Pulled up	STi0/STo0	8.192 Mbps	
	Input Pulled up	STi1/STo1	8.192 Mbps	
	Input Pulled up	STi2/STo2	8.192 Mbps	
	Input Pulled up	STi3/STo3	8.192 Mbps	
Group 2	Input Pulled up	Sti4/Sto4	8.192 Mbps	
	Input Pulled up	Sti5/Sto5	8.192 Mbps	
	Input Pulled up	Sti6/Sto6	8.192 Mbps	
	Input Pulled up	Sti7/Sto7	8.192 Mbps	
Group 3	Input Pulled up	Sti8/Sto8	8.192 Mbps	
	Input Pulled up	Sti9/Sto9	8.192 Mbps	
	MPC8280 TDMA through the B1 TDM Port	Sti10/Sto10	8.192 Mbps	Each DS-0 in the input stream of 127 channels is defined by the MPC8280. Each DS-0 of the output stream is defined by the connection memory.
	MPC8280 TDMB through the B2 TDM Port	Sti11/Sto11	8.192 Mbps	Each DS-0 in the input stream of 127 channels is defined by the MPC8280. Each DS-0 of the output stream is defined by the connection memory
Group 3	QUAD FALC Data Port 0-3	Sti13/ Sto13	8.192 Mbps	128 DS-0s Bidirectional
	Input Pulled up	Sti14/Sto14	8.192 Mbps	
	Input Pulled up	Sti15/Sto15	8.192 Mbps	
Group 4	Input Pulled up	Sti16/Sto16	8.192 Mbps	
	Input Pulled up	Sti17/Sto17	8.192 Mbps	
	Input Pulled up	Sti18/Sto18	8.192 Mbps	
	Input Pulled up	Sti19/Sto19	8.192 Mbps	
	Input Pulled up	Sti20/Sto20	8.192 Mbps	
	Input Pulled up	Sti21/Sto21	8.192 Mbps	
	Input Pulled up	Sti22/Sto22	8.192 Mbps	
	Input Pulled up	Sti23/Sto23	8.192 Mbps	

Table 4-8: Digital Switch Local TDM Streams Connection (Continued)

Group	Device	Switch Connection	TDM Data Rate	Interleaving Format
	Input Pulled up	Sti24/Sto24	8.192 Mbps	
	Input Pulled up	Sti25/Sto25	8.192 Mbps	
	Input Pulled up	Sti26/Sto26	8.192 Mbps	
	Input Pulled up	Sti27/Sto27	8.192 Mbps	

E1/T1/J1 Quad Framer and LIU

The PCE385 has an E1/T1/J1 quad framer with an integral Line Interface Unit (LIU, four ports total) located on the mezzanine I/O board. The Quad FALC supports a multitude of features, including:

- high density, generic interface for all E1/T1/J1 applications
- four analog receive and transmit circuits for long and short haul applications
- E1 or T1/J1 mode selectable for each channel individually
- data and clock recovery using an integrated digital phase locked loop
- maximum line attenuation to -43 dB at 1024 kHz (E1) and to -36 dB at 772 kHz (T1/J1)
- programmable transmit pulse shapes for E1 and T1/J1 pulse masks
- programmable line build-out for CSU signals according to ANSI T1. 403 and FCC68: 0 dB, -7.5 dB, -15 dB, -22.5 dB (T1/J1)
- low transmitter output impedances for high transmit return loss
- tristate function of the analog transmit line outputs
- transmit line monitor protecting the device from damage
- receive line monitor mode
- jitter specifications of ITU-T I.431, G.703, G.736 (E1), G.823 (E1) and AT&T TR62411 (T1/J1) are met
- crystal-less wander and jitter attenuation/compensation
- common master clock reference for E1 and T1/J1 (any frequency within 1.02 and 20 MHz)
- power down function per channel
- support for automatic protection switching
- selectable line codes (E1: HDB3, AMI/T1: B8ZS, AMI with ZCS)
- loss of signal indication with programmable thresholds according to ITU-T G.775, ETS300233 (E1) and ANSI T1.403 (T1/J1)
- optional data stream muting upon Loss of Signal (LOS) detection
- programmable receive slicer threshold
- clock generator for jitter free system and transmit clocks per channel
- local loop and remote loop for diagnostic purposes
- low power device, single power supply: 3.3 V with 5 V tolerant digital inputs

Frame Aligner Features

These are the Frame Aligner features:

- frame alignment/synthesis for 2,048 Kbps according to ITU-T G.704 (E1) and for1,544 Kbps according to ITU-T G.704 and JT G.704 (T1/J1)
- programmable frame formats: E1: Doubleframe, CRC Multiframe (E1)T1: 4-Frame Multiframe (F4,FT), 12-Frame Multiframe (F12, D3/4), Extended Superframe (F24, ESF), Remote Switch Mode (F72, SLC96)
- selectable conditions for recover/loss of frame alignment
- CRC4 to Non-CRC4 Interworking according to ITU-T G. 706 Annex B (E1)
- error checking using CRC4 procedures according to ITU-T G. 706 (E1)
- error checking using CRC6 procedures according to ITU-T G. 706 and JT G.706 (T1/J1)
- performs synchronization in ESF format according to NTT requirements (J1)
- alarm and performance monitoring per second: 16 bit counter for CRC-, framing errors, code violations, error monitoring using E bit and SA6 bit (E1), errored blocks, PRBS bit errors
- insertion and extraction of alarm indication signals (AIS, remote/yellow alarm,…)
- remote Alarm generation/checking according to ITU JT-G.704 in ESF-format (J1)
- IDLE code insertion for selectable channels
- single-bit defect insertion
- flexible system clock frequency for receiver and transmitter
- supports programmable system data rates with independent receive/transmit shifts: E1: 2.048, 4.096, 8.192 and 16.384 Mbps (according to H.100 bus). T1/J1: 2.048, 4.096, 8.192, 16.384 Mbps and 1.544, 3.088, 6.176, 12.352 Mbps
- system interface multiplex mode; multiplexing of four channels into an 8.192 Mbps data stream and vice versa, bit- or byte-interleaved
- elastic store for receive and transmit route clock wander and jitter compensation; controlled slip capability and slip indication
- programmable elastic buffer size: two frames, one frame/short buffer/bypass
- provides different time slot mapping modes
- supports fractional E1 or T1/J1 access
- flexible transparent modes
- programmable in-band loop code detection and generation (TR62411)
- channel loop back, line loop back, or payload loop back capabilities (TR54016)
- Pseudo Random Bit Sequence (PRBS) generator and monitor (framed or unframed)
- clear channel capabilities (T1/J1)
- loop-timed mode
- HDLC controller bit stuffing, CRC check and generation, flag generation, flag and address recognition, handling of bit oriented functions
- supports Signaling System #7 delimitation, alignment and error detection according to ITU-Q.703 processing of fill in signaling units, processing of errored signaling units
- CAS/CAS-BR controller with last look capability, enhanced CAS-register access and freeze signaling indication
- DL-channel protocol for ESF format according to ANSI T1.403 specification or according to AT&T TR54016 (T1/J1)
- DL-bit access for F72 (SLC96) format (T1/J1)
- generates periodic performance report according to ANSI T1. 403

- provides access to serial signaling data streams
- multiframe synchronization and synthesis according to ITU-T G.732
- alarm insertion and detection (AIS and LOS in time slot 16)
- transparent mode
- FIFO buffers (64 bytes deep) for efficient transfer of data packets
- time slot assignment: any combination of time slots selectable for data transfer independent of signaling mode (useful for fractional T1/J1 applications)
- time-slot 0 Sa8...4-bit handling using FIFOs (E1)
- HDLC access to any Sa-bit combination (E1)
- extended interrupt capabilities
- one-second timer (internal or external timing reference)

Chapter

5

ATM Channel Allocations

Overview

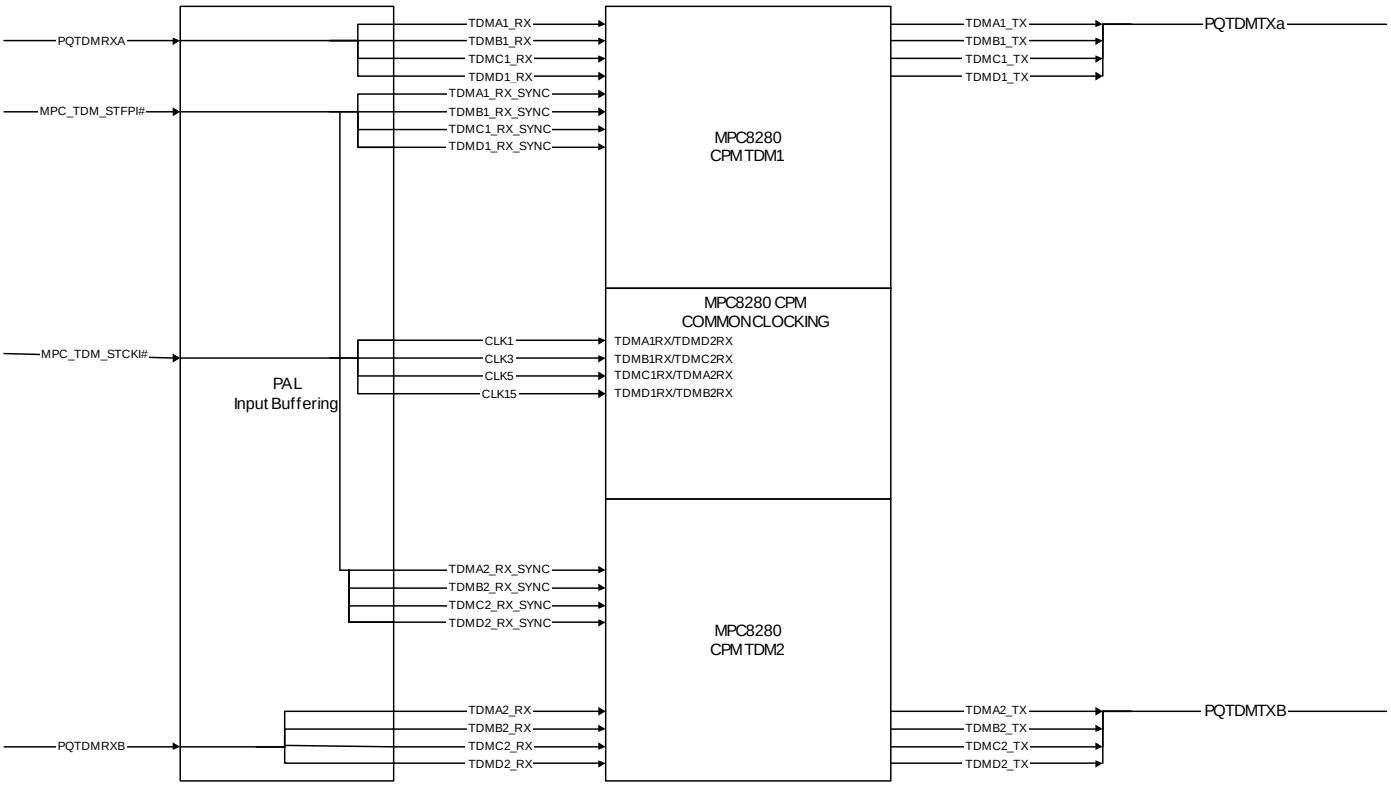
The PCE385 supports Asynchronous Transfer Mode (ATM) termination. Two full channels of eight MHz Time Division Multiplexed (TDM) data are fed from the H.100 TDM switch on the PCE385 daughter board along with the frame pulse and the TDM clock. The signals are routed into the baseboard control and logic PAL for buffering and distribution of the data, control pulses and TDM clocks to the MPC8280 TDM inputs and outputs.

Topics in this chapter include:

ATM Channel Allocations

Figure 5-1: "ATM Channel Allocations" provides an overview of ATM channel allocations.

Figure 5-1: ATM Channel Allocations



PQTDMRXA and PQTDMRXB are the multiplexed 8.192 MHz TDM data from the on-board TDM switch. MPC_TDM_STCKI# is the synchronized 8.192 MHz TDM clock from the on-board switch. MPC_TDM_STFPI# is the TDM frame pulse from the on-board TDM switch.

These signals are buffered by the PAL and connected directly to the appropriate TDM inputs. TDM connections A1, B1, C1, D1, A2, B2, C2, and D2 can be used as inputs. Because the TDM inputs can share clocking, they are grouped together to reduce the number of common clock connections inputted to the part. The grouping is as follows:

- CLK1 is mapped to TDMA1 Rx CLK and TDMD2 Rx CLK.
- CLK3 is mapped to TDMB1 Rx CLK and TDMC2 Rx CLK
- CLK5 is mapped to TDMC1 Rx CLK and TDMA2 Rx CLK
- CLK15 is mapped to TDMD1 Rx CLK and TDMB2 Rx CLK

In the SI setup, the transmit clock for each TDM channel is then set to be sourced from its own Rx CLK input.

The Frame pulse sync inputs are made to each individual Rx SYNC input of the TDM channels. The SI setup is then configured to source the Tx SYNC input from its own Rx SYNC input.

For information about the data, frame pulse and clocking connections for each port, see “MPC8280 Parallel Port Pin Assignments” on page 60.

The Switch TDM data is byte grouped so that the SI can decode it appropriately for each TDM input and pass it on the Transmission Convergence (TC) layer block in the MPC8280. The TC layer block separates ATM functions into its receive and transmit sub-blocks (see Figure 5-2, “MPC8280 ATM Transmission Convergence (TC) Layer Overview” on page 58).

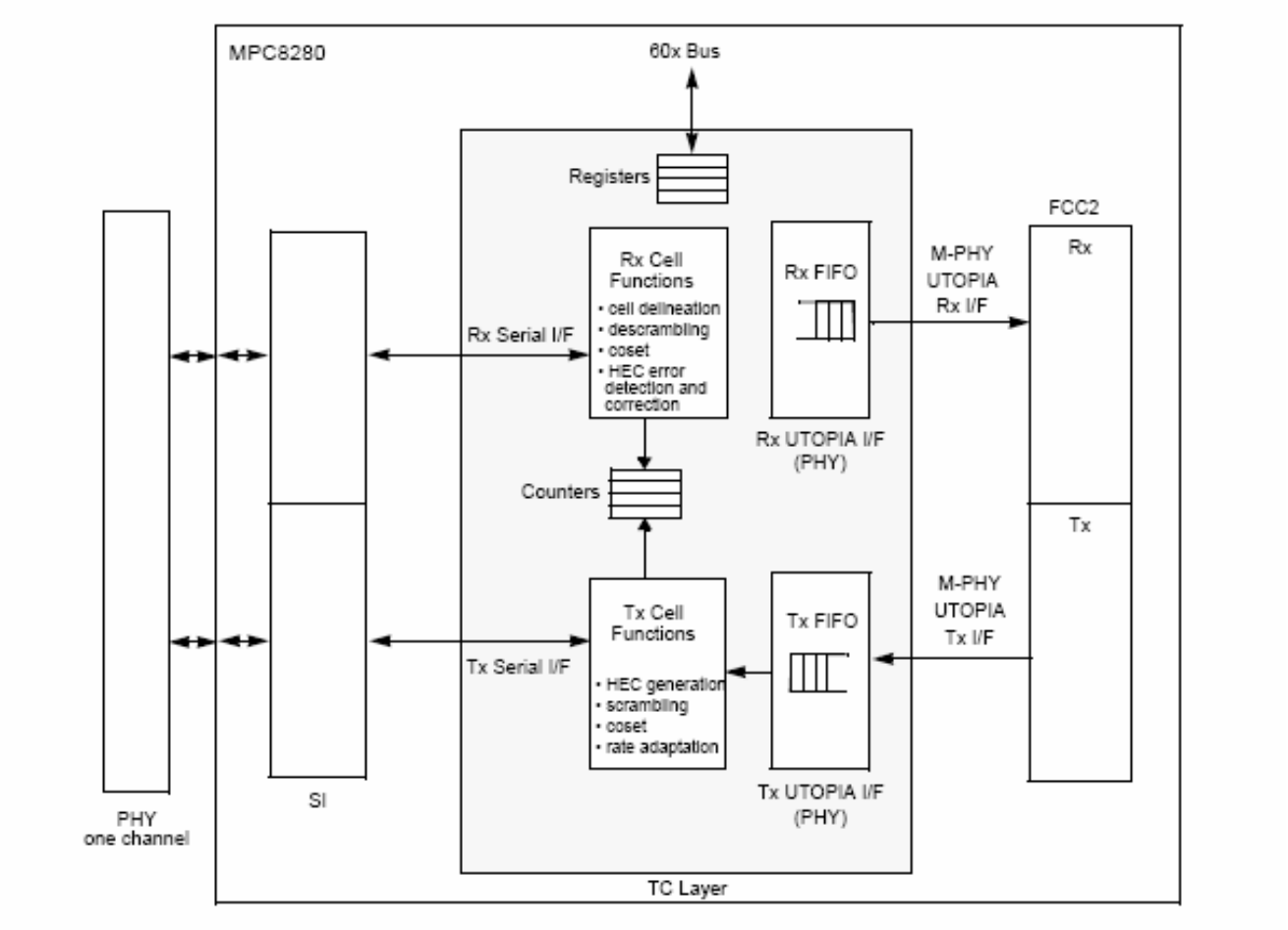
Primary features of the TC layer include the following:

- eight TDM channels routed in hardware to eight TC layer blocks
  - protocol-specific overhead bits can be discarded or routed to other controllers by the SI
  - performing ATM TC layer functions (according to ITU-T I.432)
  - transmit (Tx) updates are as follows:
    - cell Header Error Control (HEC) generation
    - payload scrambling using self synchronizing scrambler (programmable by the user)
    - coset generation (programmable by the user)
    - cell rate by inserting idle cells
  - receive (Rx) updates are as follows:
    - cell delineation using bit by bit HEC checking and programmable ALPHA and DELTA parameters for the delineation state machine
    - payload de-scrambling using self synchronizing scrambler (programmable by the user)
    - coset removing (programmable by the user)
    - filtering idle/unassigned cells (programmable by the user)
    - performing HEC error detection and single bit error correction (programmable by the user)
    - generating loss of cell delineation status/interrupt (LOC / LCD)
- operates with FCC2 (UTOPIA 8)
- serial loop back mode
- cell echo mode
- supports both FCC transmit modes:
  - external rate mode—Idle cells are generated by the FCC (microcode) to control data rate
  - internal rate mode (sub-rate)—FCC transfers only the data cells using the required data rate. The TC layer generates idle/unassigned cells to maintain the line bit rate
- supports the TC layer and Physical Medium Dependent (PMD) WIRE interface (according to the ATM-Forum AF-PHY-0063.000)

Cell counters for performance monitoring include:

- 16-bit counters count:
  - HEC error cells
  - HEC single bit error and corrected cells
  - idle/unassigned cells filtered
  - idle/unassigned cells transmitted
  - transmitted ATM cells
  - received ATM cells
  - maskable interrupt sent to the host when a counter expires
- overrun (Rx cell FIFO) and underrun (Tx cell FIFO) condition produces maskable interrupt
- can be operated at E1 and DS-1 rates. In addition, xDSL applications at bit rates up to 10 Mbps are supported.

Figure 5-2: MPC8280 ATM Transmission Convergence (TC) Layer Overview



ATM Receive Cell Functions

The ATM Receive Cell Functions (RCF) block performs the receive functions of the TC block. This block performs cell delineation, cell payload descrambling, Header Error Check (HEC) verification and correction, and idle/unassigned cell filtering.

Cell delineation is the process of framing data to ATM cell boundaries using the HEC received in the ATM cell header. The HEC is a CRC-8 calculation over the first four octets of the ATM cell header. The cell delineation algorithm assumes that repetitive correct HEC calculations over consecutive cells indicate valid ATM cell boundaries.

The receive First In, First Out (FIFO) provides FIFO management and an interface to the Universal Test and OPerations Interface for ATM (UTOPIA) receive cell interface. The receive FIFO can hold two ATM cells, thereby providing the cell rate decoupling function between the transmission system physical layer and the ATM layer.

FIFO management includes filling the FIFO, indicating to the UTOPIA interface that it contains cells, maintaining the FIFO read and write pointers, and detecting FIFO overrun (TCER[OR]) conditions.

ATM Transmit Cell Functions

The ATM Transmit Cell Functions (TCF) block performs the ATM cell payload scrambling and is responsible for the HEC generation and the idle cell generation.

The TCF scrambles (programmable by the user) the cell payload using the self-synchronizing scrambler with polynomial x43 + 1.

The HEC is generated using the polynomial x8 + x2 + x + 1. The coset polynomial x6 + x4 + x2 + 1 is added (modulo 2) (programmable by the user) to the calculated HEC octet. The result overwrites the HEC octet on the transmitted cell. When the transmit FIFO is empty, the TCF inserts idle cells, which are counted in the Idle Cell Counter (ICC). The TCF accumulates the number of transmitted assigned cells in a counter (TCC).

The transmit FIFO provides FIFO management and an interface to the UTOPIA transmit interface. The FIFO provides the cell rate decoupling between the transmission system physical layer and the ATM layer. The FIFO management includes emptying cells from the transmit FIFO, indicating to the UTOPIA interface that it is full, maintaining the FIFO read and write pointers, and detecting FIFO underrun (TCER[UR]) conditions.

Receive UTOPIA Interface

The receive UTOPIA block performs the receive interface with the FCC using the UTOPIA bus. This block implements the UTOPIA level-2 (multi-PHY) 8-bit PMD side (slave) interface.

Transmit UTOPIA Interface

The transmit UTOPIA block performs the transmit interface with the FCC using the UTOPIA bus. This block implements the UTOPIA level-2 (multi-PHY) 8-bit PMD side (slave) interface.

The remainder of the setup for the ATM block is internal to the MPC8280s FCC2 and the TC Layer. The incoming data is received by FCC2 and at this point, the data can be terminated into memory or sent to another TDM port. The transmit path is also through FCC2. For additional informations, refer to the Freescale *MPC8280 PowerQUICC II Family Reference Manual Rev.0*.

MPC8280 Parallel Port Pin Assignments

The program settings for the parallel port pins can be found in the files init.inc and hardware.c.

Note: *All unassigned channels on all ports should be programmed to be data register outputs wherever no conflicts or limitations in the part exist. This configuration prevents unwanted current draw on the unused channels.*

MPC8280 Port A Pin Assignments

Table 5-1: "MPC8280 Port A Pin Assignments" describes the MPC8280 port A pin assignments.

Table 5-1: MPC8280 Port A Pin Assignments

Pin	Pin Function					
	PPARA = 1				PPARA = 0	
	PSORA = 0		PSORA = 1			
	PDIRA = 1 Out	PDIRA = 0 In	PDIRA = 1 Out	PDIRA = 0 In	PDIRA = 1 Out	PDIRA = 0 In
PA31	Default = Unassigned					
PA30	Default = Unassigned					
PA29	Default = Unassigned					
PA28	Default = Unassigned					
PA27	Default = Unassigned					
PA26	Default = Unassigned					
PA25	Default = Unassigned					
PA24	Default = Unassigned					
PA23	Default = Unassigned					
PA22	Default = Unassigned					
PA21	Default = Unassigned					
PA20	Default = Unassigned					
PA19	Default = Unassigned					
PA18	Default = Unassigned					
PA17	Default = Unassigned					
PA16	Default = Unassigned					
PA15	Default = Unassigned					
PA14	Default = Unassigned					
PA13	Default = Unassigned					
PA12	Default = Unassigned					

Table 5-1: MPC8280 Port A Pin Assignments (Continued)

Pin	Pin Function					
	PPARA = 1				PPARA = 0	
	PSORA = 0		PSORA = 1			
	PDIRA = 1 Out	PDIRA = 0 In	PDIRA = 1 Out	PDIRA = 0 In	PDIRA = 1 Out	PDIRA = 0 In
PA11	Default = Unassigned					
PA10	Default = Unassigned					
PA9				TDMA1_TX		
PA8				TDMA1_RX		
PA7	Default = Unassigned					
PA6				TDMA1_RX_ SYNC		
PA5	Default = Unassigned					
PA4	Default = Unassigned					
PA3					EE_CS	
PA2					EE_SCL	
PA1						EE_DI
PA0					EE_DO	

MPC8280 Port B Pin Assignments

Table 5-2: “MPC8280 Port B Pin Assignments” describes the MPC8280 port B pin assignments.

Table 5-2: MPC8280 Port B Pin Assignments

Pin	Pin Function					
	PPARB = 1				PPARB = 0	
	PSORB = 0		PSORB = 1			
	PDIRB = 1 Out	PDIRB = 0 In	PDIRB = 1 Out	PDIRB = 0 In	PDIRB = 1 Out	PDIRB = 0 In
PB31				TDMB2_TX		
PB30				TDMB2_RX		
PB29				TDMB2_RX_SYNC		
PB28	Default = Unassigned					
PB27				TDMC2_TX		
PB26				TDMC2_RX		
PB25	Default = Unassigned					
PB24				TDMC2_RX_SYNC		
PB23				TDMD2_TX		
PB22				TDMD2_RX		
PB21	Default = Unassigned					
PB20				TDMD2_RX_SYNC		
PB19	Default = Unassigned					
PB18	Default = Unassigned					
PB17	Default = Unassigned					
PB16	Default = Unassigned					
PB15				TDMC1_TX		
PB14				TDMC1_RX		
PB13	Default = Unassigned					
PB12				TDMC1_RX_SYNC		
PB11				TDMD1_TX		
PB10				TDMD1_RX		
PB9	Default = Unassigned					

Table 5-2: MPC8280 Port B Pin Assignments (Continued)

Pin	Pin Function					
	PPARB = 1				PPARB = 0	
	PSORB = 0		PSORB = 1			
	PDIRB = 1 Out	PDIRB = 0 In	PDIRB = 1 Out	PDIRB = 0 In	PDIRB = 1 Out	PDIRB = 0 In
PB31				TDMB2_TX		
PB8				TDMD1_RX_ SYNC		
PB7				TDMA2_TX		
PB6				TDMA2_RX		
PB5	Default = Unassigned					
PB4				TDMA2_RX_ SYNC		

MPC8280 Port C Pin Assignments

Table 5-3: “MPC8280 Port C Pin Assignments” describes the MPC8280 port C pin assignments.

Table 5-3: MPC8280 Port C Pin Assignments

Pin	Pin Function					
	PPARC = 1				PPARC = 0	
	PSORC = 0		PSORC = 1			
	PDIRC = 1 Out	PDIRC = 0 In	PDIRC = 1 Out	PDIRC = 0 In	PDIRC = 1 Out	PDIRC = 0 In
PC31		CLK1 ASSIGNED TO TDMA1_RX_ CLK AND TDMD2_RX_ CLK				
PC30	Default = Unassigned					
PC29		CLK3 ASSIGNED TO TDMB1_RX_ CLK AND TDMC2_RX_ CLK				
PC28	Default = Unassigned					
PC27		CLK5 ASSIGNED TO TDMC1_RX_ CLK AND TDMA2_RX_ CLK				
PC26	Default = Unassigned					
PC25	Default = Unassigned					
PC24	Default = Unassigned					
PC23	Default = Unassigned					
PC22	Default = Unassigned					
PC21	Default = Unassigned					
PC20	Default = Unassigned					
PC19	Default = Unassigned					
PC18	Default = Unassigned					

Table 5-3: MPC8280 Port C Pin Assignments (Continued)

Pin	Pin Function					
	PPARC = 1				PPARC = 0	
	PSORC = 0		PSORC = 1			
	PDIRC = 1 Out	PDIRC = 0 In	PDIRC = 1 Out	PDIRC = 0 In	PDIRC = 1 Out	PDIRC = 0 In
PC17		CLK15 ASSIGNED TO TDMB2_RX_CLK AND TDMD1_RX_CLK				
PC16	Default = Unassigned					
PC15	Default = Unassigned					
PC14	Default = Unassigned					
PC13	Default = Unassigned					
PC12	Default = Unassigned					
PC11	Default = Unassigned					
PC10	Default = Unassigned					
PC9	Default = Unassigned					
PC8	Default = Unassigned					
PC7	Default = Unassigned					
PC6	Default = Unassigned					
PC5	Default = Unassigned					
PC4	Default = Unassigned					
PC3	Default = Unassigned					
PC2	Default = Unassigned					
PC1	Default = Unassigned					
PC0	Default = Unassigned					

MPC8280 Port D Pin Assignments

Table 5-4: “MPC8280 Port D Pin Assignments” describes the MPC8280 port D pin assignments.

Table 5-4: MPC8280 Port D Pin Assignments

Pin	Pin Function					
	PPARD = 1				PPARD = 0	
	PSORD = 0		PSORD = 1			
	PDIRD = 1 Out	PDIRD = 0 In	PDIRD = 1 Out	PDIRD = 0 In	PDIRD = 1 Out	PDIRD = 0 In
PD31	Default = Unassigned					
PD30	Default = Unassigned					
PD29	Default = Unassigned					
PD28	Default = Unassigned					
PD27	Default = Unassigned					
PD26	Default = Unassigned					
PD25	Default = Unassigned					
PD24	Default = Unassigned					
PD23	Default = Unassigned					
PD22	Default = Unassigned					
PD21	Default = Unassigned					
PD20	Default = Unassigned					
PD19	Default = Unassigned					
PD18	Default = Unassigned					
PD17	Default = Unassigned					
PD16	Default = Unassigned					
PD15	Default = Unassigned					
PD14	Default = Unassigned					
PD13				TDM_B1: L1TXD		
PD12				TDM_B1: L1RXD		
PD11						
PD10				TDM_B1: L1RSYNC		
PD9	SMC1: SMTXD					

Table 5-4: MPC8280 Port D Pin Assignments (Continued)

Pin	Pin Function					
	PPARD = 1				PPARD = 0	
	PSORD = 0		PSORD = 1			
	PDIRD = 1 Out	PDIRD = 0 In	PDIRD = 1 Out	PDIRD = 0 In	PDIRD = 1 Out	PDIRD = 0 In
PD8		SMC1: SMRXD				
PD7	Default = Unassigned					
PD6	Default = Unassigned					
PD5	Default = Unassigned					
PD4	Default = Unassigned					

Chapter

6

Pinouts

Overview

This chapter provides information about the pinouts and ports on the PCE385. To identify the port locations on the boards, see Figure 2-2, “PCE385 Main Board Component Layout” on page 21 and Figure 2-3, “PCE385 Daughter Board Component Layout” on page 22.

Topics in this chapter include:

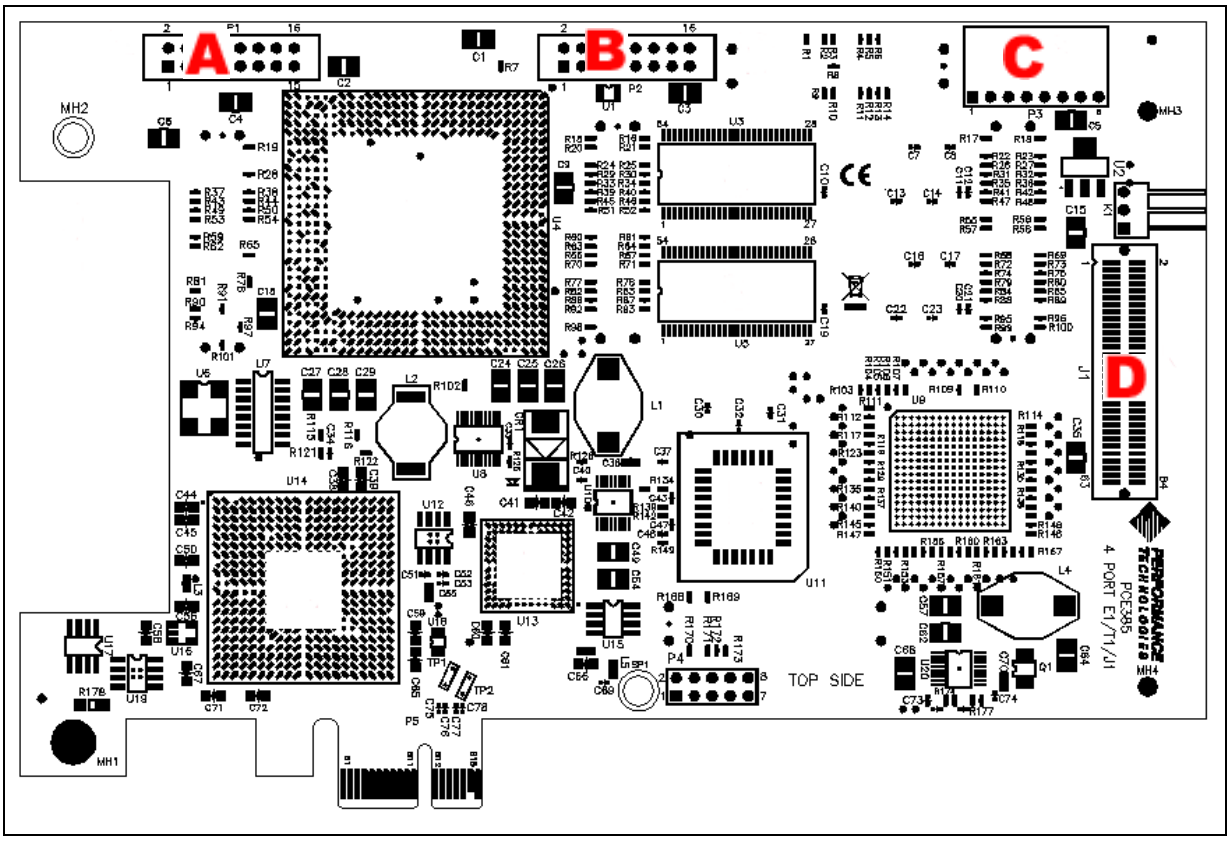
Main Board Pinouts

This section describes the pinouts of the connectors on the PCE385 main board (see Table 6-1: “PCE385 Main Board Connector Pinout Call Out Definitions” and Figure 6-1: "PCE385 Main Board Connector Pinouts").

Table 6-1: PCE385 Main Board Connector Pinout Call Out Definitions

Call Out Letter	Connector
A	MPC8280 COPS Header (P1)
B	JTAG Testing Port (P2)
C	Option Jumper Block (P3)
D	Daughter Board Interface Connector (J1)

Figure 6-1: PCE385 Main Board Connector Pinouts



MPC8280 COPS Header (P1)

The JTAG testing port on the MPC8280 is used to support the EST Common On-chip Processor (COP) debugger on the P1 connector. This connector is set up to support the extended 16-pin COP debugger signaling, but the basic 10-pin signaling devices can be used with an interposing adapter. Table 6-2: “JTAG/BDM Debug Port (P1) Pinouts” describes the P1 pinouts.

Table 6-2: JTAG/BDM Debug Port (P1) Pinouts

Pin Number	Signal Name
1	PQ_TDO - JTAG Test Data Out Signal
2	!PQ_QACK- Quiescent State Acknowledge, not supported
3	PQ_TDI - JTAG Test Data In signal
4	!PQ_TRST - JTAG Reset and Tristate signal
5	!PQ_QREQ - Quiescent State Request
6	V3V
7	PQ_TCK - JTAG Test Clock
8	No Connection
9	PQ_TMS - JTAG Test Mode Select
10	No Connection
11	PQ_SRESET# - MPC8280 Soft Reset
12	Ground
13	PQ_HRESET# - MPC8280 Hard Reset
14	No Connection
15	!CHKSTPO - Checkstop output, Not supported
16	Ground

All the control signals are pulled to V3V with a minimum 10K resistor to prevent false acutation when no JTAG controller is connected.

The mechanical requirements 16-pin Motorola connector are specified as follows.

- vertical, 16 (2 X 8) pin header
- 0.10 in. between centers of adjacent pins
- 0.025 in. square pins
- 0.23 in. height of each post

JTAG Testing Port (P2)

Two PCE385 boards can be configured as a master/slave pair using the H.100 bus provided at board edge connector P2. Connect the two boards together (in adjacent PCI slots) using the ribbon cable assembly described in Table 6-3: “Mezzanine Master/Slave PCM Expansion Connector (P2) Pinout”.

Table 6-3: Mezzanine Master/Slave PCM Expansion Connector (P2) Pinout

Pin Number	Signal Name	Signal Name	Pin Number
1	reserved	reserved	2
3	CT_D31	CT_D30	4
5	CT_D29	CT_D28	6
7	GND	CT_D27	8
9	CT_D26	CT_D25	10
11	CT_D24	GND	12
13	CT_D23	CT_D22	14
15	CT_D21	CT_D20	16
17	GND	CT_D19	18
19	CT_D18	CT_D17	20
21	CT_D16	GND	22
23	CT_D15	CT_D14	24
25	CT_D13	CT_D12	26
27	GND	CT_D11	28
29	CT_D10	CT_D9	30
31	CT_D8	GND	32
33	CT_D7	CT_D6	34
35	CT_D5	CT_D4	36
37	GND	CT_D3	38
39	CT_D2	CT_D1	40
41	CT_D0	GND	42
43	$\overline{\text{CT\_FRAME\_A}}$	GND	44
45	CT_C8_A	GND	46
47	CTNR1	GND	48
49	$\overline{\text{CT\_FRAME\_B}}$	GND	50
51	CT_C8_B	GND	52
53	reserved	GND	54

Table 6-3: Mezzanine Master/Slave PCM Expansion Connector (P2) Pinout (Continued)

Pin Number	Signal Name	Signal Name	Pin Number
55	reserved	GND	56
57	reserved	GND	58
59	reserved	GND	60
61	reserved	GND	62
63	reserved	GND	64
65	reserved	reserved	66
67	GND	reserved	68

Option Jumper Block (P3)

The P3 eight-pin header is used to set the board configuration and the mode of operation. Table 6-4: “Option Jumper Block (P3) Pinout” describes the P3 pinouts.

Table 6-4: Option Jumper Block (P3) Pinout

Pin Number	Signal Name	Operational Mode	Description
1	RSTCONF	Jumper 1-2	Tells CPU to follow normal Reset configuration procedure by reading settings from FLASH
2	GND		
3	PORESET	No Connect	When momentarily grounded this pin will force the card to take a power-on reset.
4	NMI	No Connect	When momentarily grounded this pin will force the CPU to take a non-maskable interrupt.
5	GND	No Connect	This jumper selection can be made to allow the serial console port to send a break signal to the board to reset it. It is usually only used during the debug process. This function is not normally enabled in an operational mode.
6	BREAK_DET		
7	GND	Jumper 7-8	This jumper signals the boot code to load the run time software from the on board application FLASH. If the jumper is not present the boot loader will stop and display the ok> prompt.
8	FACTORY_JMP		

Notes:

- *RSTCONF is grounded for normal operation. Jumper open uses default hardware configuration where the reset of the 60x bus components will not be configured.*
- *BREAK_DET provides a hardware reset with a serial break detect sequence.*
- *FACTORY_JMP for factory default initialization.*

Daughter Board Interface Connector (J1)

The PCE385 is connected to the media using a shielded four position RJ-48C connector on the mounting bracket. The mating plug (not supplied) can be a shielded or unshielded eight-position modular jack. Use the shielded version when you require maximum noise immunity. Table 6-5: “Mezzanine Telecom Line Interface J1 Pinout” describes the J1 pinouts.

Table 6-5: Mezzanine Telecom Line Interface J1 Pinout

Pin Number	Signal Name
A1	RRING_4
A2	RTIP_4
A3	nc
A4	TRING_4
A5	TTIP_4
A6	nc
A7	nc
A8	nc
B1	RRING_3
B2	RTIP_3
B3	nc
B4	TRING_3
B5	TTIP_3
B6	nc
B7	nc
B8	nc
C1	RRING_2
C2	RTIP_2
C3	nc
C4	TRING_2
C5	TTIP_2
C6	nc
C7	nc
C8	nc
D1	RRING_1
D2	RTIP_1
D3	nc

Table 6-5: Mezzanine Telecom Line Interface J1 Pinout (Continued)

Pin Number	Signal Name
D4	TRING_1
D5	TTIP_1
D6	nc
D7	nc
D8	nc

Chapter

7

Specifications

Overview

This chapter provides information about the system requirements for the PCE385.

Caution:
Use anti-static grounding straps and anti-static mats when you are handling the PCE335 to help prevent damage due to electrostatic discharge. Electronic components on printed circuit boards are extremely sensitive to static electricity. Ordinary amounts of static electricity generated by your clothing or work environment can damage the electronic equipment.

System Requirements

This section describes the PCE385 environmental and power requirements (see Table 7-1: “Environmental Requirements” and Table 7-2: “Power Requirements”).

Table 7-1: Environmental Requirements

Temperatures	Air Flow
Operating: 0°C to 50°C (32°F to 122°F)	Standard PC chassis airflow is acceptable.
Non-operating: -20°C to 80°C (-4°F to 176°F)	

Table 7-2: Power Requirements

Voltage	Maximum (W)
2.46A @ 3.3V	8.1
3.36 @ 12V	3.63

Chapter

8

Data Sheets and Agency Approvals

Overview

This chapter provides references to data sheets, standards, and specifications for the technology designed into PCE385. This chapter also provides the agency approvals for the PCE385.

Topics in this chapter include:

Data Sheet Reference

This section provides links to data sheets, standards, and specifications for the technology designed into the PCE385 board, including:

- CompactPCI Specifications
- User Documentation References

CompactPCI Specifications

Current CompactPCI Specifications can be purchased from PICMG (PCI Industrial Computers Manufacturers Group) for a nominal fee. Short form specifications in Adobe Acrobat format (PDF) are also available on PICMG’s website at:

http://www.picmg.org

User Documentation References

This guide has been created for the installation, maintenance, configuration, and use of the PCE385. The latest PCE385 product information and manuals are available on the Performance Technologies Website at http://www.pt.com.

Refer to the following manuals for more information about the software components that might be used with your system.

- **NexusWare® Core** NexusWare® Core is a comprehensive, highly integrated, Linux-based development, integration and management environment, for system engineers using Performance Technologies' embedded products to build packet-based wireless and IP telephony systems. NexusWare Core is the foundation environment for Performance Technologies' existing and future value-add NexusWare software packages, including NexusWare C7, NexusWare Wide Area Network (WAN), NexusWare Information Systems Management (ISM).
- **WAN Protocol Software** Our suite of Wide Area Networking (WAN) protocols provides all the critical pieces required for timely application development. With a wide range of WAN protocols, high performance controllers and servers and comprehensive operating system support, we provide a complete application solution for Original Equipment Manufacturer (OEM).

  All of our WAN protocols adhere to a common Application Programming Interface (API). The API contains information useful to programmers developing applications that interact with Performance Technologies' Executive for STREAMS Applications (xSTRa) or its NexusWare® Service Layer (NWSL).

  This software architecture ensures customer investments in application development will be fully portable across industry-standard hardware bus architectures, TCP/IP and operating systems. This portability represents a significant reduction in WAN application development efforts, system integration costs and time-to-market.
- **NexusWare C7** NexusWare C7 is a comprehensive, highly-integrated Linux-based development, integration and management environment. This environment is intended for system engineers using Performance Technologies' embedded products to build packet-based systems, including next-generation wireless and Internet Protocol (IP) telephony platforms.

  In the past, systems depended on the conventional Peripheral Component Interconnect (PCI) bus for system integration, forcing a low-level and time-consuming process for developing IP telephony, datacom, and telecom systems. The Ethernet capabilities of Performance Technologies' IPnexus® hardware products, coupled with the strong Linux operating system (OS) foundation of NexusWare C7, offers a simple and rapid path to newer, IP-based PCI PICMG® 2.16 systems, while providing developers with a simplified way to design-in current, PCI-based systems.

  NexusWare C7, which is a loadable module within NexusWare Core, provides SS7 MTP2 layer data processing above the NexusWare Core API.
- **ChanneLink** T1/E1/J1 Driver (Solaris) Our ChanneLink™ T1/E1/J1 Driver provides users of our high performance family of T1/E1 communications adapters an easy way to run a variety of SunSoft™ communications protocols in either a channelized or non-channelized mode.

  ChanneLink is architected to provide a totally transparent link between the SunSoft protocols and our T1/E1 communications adapters. ChanneLink is capable of transmitting and receiving T1/E1 data, and sustaining high speed data rates for a variety of protocols used in telecommunications and data communications applications.

  ChanneLink can also be used as a standard API and Solaris® driver for non-SunSoft applications.

  Users of Sun's suite of communication protocols, such as X.25, Frame Relay, PPP, Internetwork Router (IR), and so on, can quickly and easily integrate our communications adapters for PCI, CompactPCI®/PICMG® 2.16, or PMC based systems with the desired SunSoft protocol.

Agency Approvals

This section presents agency approval and certification information for the PCE385:

CE Certification

The PCE385 meets the intent of *Directive 89/336/EEC* for electromagnetic compatibility (amended by *92/31/EEC*, *93/68/EEC*, *98/13/EEC*, *2004/108/EC*), *R&TTE Directive 1999/5/EC*, and the *Low-Voltage Directive 72/23/EEC* for product safety (amended by *73/23/EEC*, *93/68/EEC*, *2006/95/EC*). Compliance was demonstrated to the following specifications as listed in the *Official Journal of the European Communities*:

Compliance with RoHS and WEEE Directives

In February 2003, the European Union issued Directive 2002/95/EC about the Restriction of the use of certain Hazardous Substances in electrical and electronic equipment (RoHS) and Directive 2002/96/EC about Waste Electrical and Electronic Equipment (WEEE).

This product is compliant with Directive 2002/95/EC. It may also fall under the Directive 2002/96/EC.

Performance Technologies' complete position statements on the RoHS and WEEE Directives can be viewed on the Web at http://www.pt.com/rohs/position.html.

Safety

Table 8-1: Safety Compliance

Specification	Compliance
EN/IEC 60950	Safety of Information Technology Equipment with UL Certification
CB Report Scheme	CB certificate and Report
CSA C22.2 No. 950-1	Safety of Information Technology Equipment

Emissions Test Regulations

Table 8-2: Emissions Test Regulations Compliance

Specification	Compliance
FCC	Part 15, Subpart B, Class A
EN 55022	Class A Radiated
EN 55022	Class A Conducted Emissions
EN 61000-3-2	Power Line Harmonics
EN 61000-3-3	Power Line Flicker

Immunity Test Regulations

Table 8-3: Immunity Test Regulations Compliance

Specifications	Compliance
EN 61000 4-2	Electrostatic Discharge (ESD)
EN 61000 4-3	Radiated Immunity
EN 61000 4-4	Electrical Fast Transient Burst Immunity
EN 61000 4-5	Surge Immunity
EN 61000 4-6	Radio -frequency common mode
EN 61000 4-11	Voltage dips, and Interrupt Immunity
ETSI EN 300 386 V1.3.1	Electromagnetic Compatibility and Radio Spectrum Matters (ERM)

Note: *Additional Radiated Emissions and ESD test limits were tested in accordance with GR-1089-core, issue 3.*

Regulatory Information

This section provides regulatory information for the PCE385 including:

FCC (USA)

This product has been tested and found to comply with the limits for a Class B digital device pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment.

This product generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Note: *This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:*

- This device may not cause harmful interference.
- This device must accept any interference received, including interference that may cause undesired operation.

Caution:
If you make any modification to the equipment not expressly approved by Performance Technologies, you could void your authority to operate the equipment.

Industry Canada (Canada)

Cet appareil numérique respecte les limites bruits radioélectriques applicables aux appareils numériques de Classe B prescrites dans la norme sur le matériel brouilleur: “Appareils Numériques”, NMB-003 édictée par le Ministre Canadien des Communications.

This digital apparatus does not exceed the Class B limits for radio noise emissions from digital apparatus set out in the interference-causing equipment standard entitled: “Digital Apparatus,” ICES-003 of the Canadian Department of Communications.

Chapter

9

Product Safety

Overview

This chapter provides safety information for the PCE3285 product.

Product Safety Information

This section provides safety information for the PCE385 including:

Safety Precautions

Review the following precautions to avoid injury and prevent damage to this product, or any products to which it is connected. To avoid potential hazards, use the product only as specified.

Read all safety information provided in the component product user manuals and understand the precautions associated with safety symbols, written warnings, and cautions before accessing parts or locations within the unit. Save this document for future reference.

Caution:
To Avoid Electric Overload: *To avoid electrical hazards (heat shock and/or fire hazard), do not make connections to terminals outside the range specified for that terminal. Refer to the product user manual for correct connections.*

Caution:

To Avoid the Risk of Electric Shock: *When supplying power to the system, always make connections to a grounded main. Always use a power cable with a grounded plug (third grounding pin). Do not operate in wet, damp, or condensing conditions.*

Caution:

System Airflow Requirements: *Platform components such as processor boards, Ethernet switches, etc., are designed to operate with external airflow. Components can be destroyed if they are operated without external airflow. Chassis fans normally provide external airflow when components are installed in compatible chassis. Filler panels must be installed over unused chassis slots so that airflow requirements are met. Please refer to the product data sheet for airflow requirements if you are installing components in custom chassis.*

Caution:

Microprocessor Heatsinks May Become Hot During Normal Operation: *To avoid burns, do not allow anything to touch processor heatsinks.*

Caution:

Do Not Operate Without Covers: *To avoid electric shock or fire hazard, do not operate this product with any removed enclosure covers or panels.*

Caution:

To Avoid the Risk of Electric Shock: *Do not operate in wet, damp, or condensing conditions.*

Caution:

Do Not Operate in an Explosive Atmosphere: *To avoid injury, fire hazard, or explosion, do not operate this product in an explosive atmosphere.*

Caution:

If Your System Has Multiple Power Supply Sources: *Disconnect all external power connections before servicing.*

Warning:

Power Supplies Must Be Replaced by Qualified Service Personnel Only.

Caution:

Lithium Batteries Are Not Field-Replaceable Units: *There is a danger of explosion if a battery is incorrectly replaced or handled. Do not disassemble or recharge the battery. Do not dispose of the battery in fire. When the battery is replaced, the same type or an equivalent type recommended by the manufacturer must be used. Used batteries must be disposed of according to the manufacturer's instructions. Return the unit to Performance Technologies for battery service.*

AC or DC Power Safety Warning

The AC or DC power cord is your unit's main AC or DC disconnecting device, and must be easily accessible at all times. Auxiliary AC or DC On/Off switches or circuit breaker switches are for power control functions only (NOT THE MAIN DISCONNECT).

For your safety, use only a power cord with a grounded plug. The enclosure is also provided with a separate earth ground connection/stud. The earth ground connection should be installed prior to the application of power or peripheral connections and should never be disconnected while power or peripheral connections exist.

To reduce the possibility of electric shock from a telephone or Ethernet system, plug your enclosure into the power source before making these connects. Disconnect these connections before unplugging your enclosure from the power source.

Warning:

Verify Power Cord and Outlet Compatibility. *Check to ensure you are using the appropriate power cords for your power outlet configurations. Visit the following website for additional information: http://kropla.com/electric2.htm.*

Caution:

Hot surface. Avoid contact: *Surfaces are hot and may cause personal injury if touched.*

DC Power Safety Warning (DC Powered Units)

Caution:

This equipment has a connection between the earthed conductor of the DC supply circuit and the earthing conductor.

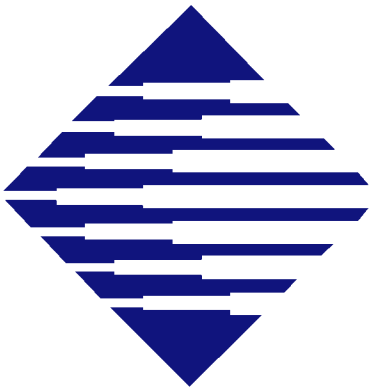
1. This equipment shall be connected directly to the DC supply system earthing electrode conductor or to a bonding jumper from an earthing terminal bar or bus to which the DC supply system earthing electrode is connected.
2. This equipment shall be located in the same immediate area (such as, adjacent cabinets) as any other equipment that has a connection between the earthed conductor of the same DC supply circuit and the earthing conductor, and also the point of earthing of the DC system. The DC system shall not be earthed elsewhere.
3. The DC supply source is to be located within the same premises as the equipment.
4. Switching or disconnecting devices shall not be in the earthed circuit conductor between the DC source and the point of connection of the earthing electrode conductor.

Rack Mount Enclosure Safety

Your enclosure may be intended for stationary rack mounting. Mount in a rack designed to meet the physical strength requirements of NEBS GR-63-CORE and NEBS GR 487. Your system may have multiple power sources. Disconnect all power sources and external connections/cables prior to installing or removing your system from a rack frame.

Caution:

Avoid Electric Overload: *To avoid electric shock or fire hazard, only connect your system to an input voltage source as specified in the product user manual.*



Glossary

A

Term	Definition
address	**Address** is a sequence of digits that uniquely identify an endpoint.
ANSI	**American National Standards Institute** is an organization of American industry groups. ANSI works with the standards committees of other nations to develop standards to facilitate international trade and telecommunications.
architecture	**Architecture** is system specification of how subcomponents interconnect, interact, and interoperate.
asynchronous transmission	**Asynchronous transmission** is a type of synchronization where there is no defined time relationship between transmission of frames.

B

Term	Definition
bit	**Bit** is the smallest unit of information that a computer can process. Typically, a bit represents two states: 1 or 0.
bit rate	**Bit rate** is the number of bits transmitted over a telephone line for each second.
bps	**Bit Per Second** is a data transmission speed measurement unit.
byte	**Byte** is a group of bits and is a unit that represents a character in some coding system. Eight bits equal one bite.

C

Term	Definition
central office	**Central office** is a building that houses switching equipment and serves as the primary operating and service center for all telephones in its geographical area. Sometimes used interchangeably with *exchange*.
CO	See central office.
CompactPCI®	**Compact Peripheral Component Interface** is a combination of the PCI bus contained on a Eurocard form factor. The Eurocard provides more rugged packaging and a more secure plug and socket for embedded systems than the standard PCI board used in desktop computers. This interface supports hot swapping and provides higher performance (32-bit, 33MHz) than the ISA bus in the PC/104 architecture. CompactPCI also provides modularity as Eurocard comes in several sizes.

D

Term	Definition
database	**Database** is a collection of related information on a computer that is arranged for ease of retrieval.

E

Term	Definition
E1	**E1** is the European equivalent to the North American T1. E1 carries information at the rate of 2.048 million bits per second (E1 supports 30 channels, 2.048 Mbps).
Ethernet	**Ethernet** is a 10 Mbps Local Area Network (LAN) medium-access method that uses Carrier Sense Multiple Access to allow the sharing of a bus-type network. IEEE 802.3 is the standard that specifies Ethernet.

F

Term	Definition
FCC	**Federal Communications Commission** is a USA federal regulatory agency charged with regulation of frequency spectrum use.
flag	**Flag** is variable such as a symbol, character or digit in software used for identification.

I

Term	Definition
ID	**Identifier** is one or more characters used to specify or identify a user, a network element, managed object, and others.
IP	**Internet Protocol** is a standardized method of transporting information across the Internet in packets of data. This data contains a network address and is used to route a message to a different network or subnetwork.
IP address	**IP address** is a numerical designation of a network node. Under IP version 4 (IPv4), this is a 32-bit number that is typically written as four byte values separated by periods (for example, 127.0.0.1).
ITU	**International Telecommunication Union** is a United Nations organization that co-ordinates global telecommunications activities.
ITU-T	**International Telecommunications Union-Telecommunication Standardization Sector** is one of three sectors of ITU, and is an international body that develops worldwide standards for telecommunication technologies.

J

Term	Definition
J1	**J1** is Japanese version of the T1 carrier system of North America (J1 supports 24 channels, 1.544 Mbps).

K

Term	Definition
kbps	**Kilo Bits Per Second** is a unit of measurement for data transfer. One kbps is equal to 1000 bits transmitted for each second.

L

Term	Definition
LED	**Light Emitting Diode** is a display technology that uses a semiconductor diode to emit infrared or visible light when this diode is charged. LEDs require very little power and are often used as indicator lights.
link	**Link** (or circuit) is the physical connection of channels, conductors, and equipment between two given signaling points through which electrical current can be established. A link has both sending and receiving capabilities.

M

Term	Definition
Mbps	**Megabits Per Second** is a unit measure of data transmission speed (one million bits per second).
MTP	**Message Transfer Part** is a component of the SS7 protocol stack that provides SS7 routing and is divided into three levels: Message Transfer Part Level 1 (MTP1), MTP2, MTP3, and MTP4.
MTP1	**Message Transfer Part Level 1** is a protocol layer that defines the physical, electrical, and functional characteristics of the digital signaling link. Physical interfaces defined include E-1 (2048 kbps; 32 64 kbps channels), DS-1 (1544 kbps; 24 64kbps channels), DS-0 (64 kbps), and DS-0A (56 kbps).
MTP2	**Message Transfer Part Level 2** is a protocol layer that provides end-to-end transmission of a message across a signaling link. Level 2 implements flow control, message sequence validation, and error checking. When an error occurs on a signaling link, the message(s) is retransmitted.
MTP3	**Message Transfer Part Level 3** is a protocol layer that provides message routing between signaling points in the SS7 network. MTP Level 3 reroutes traffic away from failed links and signaling points and controls traffic when congestion occurs.

N

Term	Definition
NEBS	**Network Equipment Building System** is a standard issued by Telcordia (formerly Bellcore) that defines central office standards for grounding and cabling, power and operations interfaces, and techniques for surviving fire and earthquake.
network	**Network** is a group of interconnected computers that can exchange information. These computers can be connected at the same physical location (LAN) or at different locations connected by modem, telephone lines, or other form of long distance communication method.
node	**Node** is a point of communication on a data network and refers to a specific interface or address on a specific host.

O

Term	Definition
OEM	**Original Equipment Manufacturer**

P

Term	Definition
packet	**Packet** is a logical grouping of information that includes a header. This header contains control information and (usually) user data. Packets most often are used to refer to network layer units of data.
path	**Path** is the route data travels through a network. Paths are usually characterized by their speed, latency, the number of hops and the rate of packet loss.
PCI	**Peripheral Component Interconnect** is an interface used on computer backplanes to connect interface cards and peripheral devices to the processor bus. PCI is typically used for video display cards, network interfaces such as Ethernet, and peripheral interfaces such as Small Computer System Interface (SCSI) or universal serial bus (SB).
PICMG® 2.16	**PCI Industrial Computer Manufacturers Group® 2.16** is a specification that overlays a packet-based switching architecture on top of CompactPCI®, enabling an Ethernet-based dual-star topology to exist within the CompactPCI® chassis.
PMC	**PCI Mezzanine Board** is a board adapted to VME bus, CompactPCI® and PCI cards. Small and compact (74 mm x 149 mm) and providing 32- or 64-bit data paths, PMC cards enable a large variety of PCI products to be retrofitted to other bus environments.
protocol	**Protocol** is a set of communication rules that govern the format of sending and receiving data.

R

Term	Definition
router	**Router** is a device or a piece of software that connects two or more networks. A router functions as a sorter and interpreter as it looks at addresses and passes bits of information to their proper destinations. Software routers are sometimes referred to as gateways.

S

Term	Definition
SCCP	**Signaling Connection Control Part** is a signaling protocol that provides connectionless and connection-oriented network services above MTP3.
SI	**Signaling Indicator** shows the level of service relevant to a particular message. Valid options are: ISUP or SCCP.
signaling	**Signaling** is the exchange of information in a network for call setup, control, and termination.
SS7	**Signaling System 7**, defined by the ITU-T, provides a suite of protocols that enables circuit and non-circuit related information to be routed about and between networks.

Term	Definition (Continued)
subnetwork	**Subnetwork** or subnet is the part of a network that shares a common address component. These networks are segmented to provide a hierarchical routing structure while shielding the subnetwork form the addressing complexities of the attached networks.
switch	**Switch** is a device that connects segmented elements within a LAN.

T

Term	Definition
T1	**T1** is a 1.544 Mbps point-to-point dedicated, digital circuit provided by the North American telephone companies. T1supports 24 channels. See E1 and J1 for European and Japanese counterparts, respectively.
TCP	**Transmission Control Protocol** is a protocol that enables two hosts to establish a connection and exchange streams of data. TCP guarantees delivery of data and also guarantees that packets will be delivered in the same order in which they were sent.
TCP/IP	**Transmission Control Protocol over Internet Protocol** is a set of rules that establish the method for transmitting data between two computers over the Internet.
telecommunication	**Telecommunication** is long distance communication using systems that transmit messages electronically (radio, satellite, Internet, and others).

U

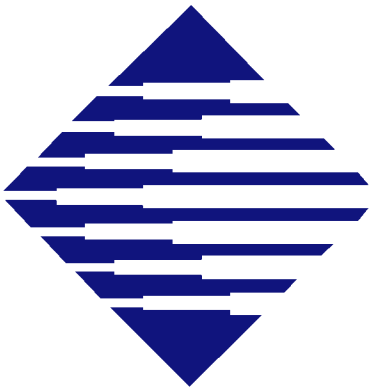
Term	Definition
UDP/IP	**User Datagram Protocol** is a rudimentary transport protocol built on top of IP. UDP adds the functionality of port numbers to distinguish between different applications on the same host. All systems that support TCP/IP also support UDP/IP.

V

Term	Definition
VoIP	**Voice over Internet Protocol** is a term used in IP telephony for a set of facilities for managing the delivery of voice information using the IP. This means sending voice information in digital form in discrete packets rather than in the traditional circuit-committed protocols of the public switched telephone network (PSTN). A major advantage of VoIP and Internet telephony is that it avoids the tolls charged by ordinary telephone service.

W

Term	Definition
WAN	**Wide-Area Network** is a network that connects computers over long distances using telephone lines or satellite links. In a WAN, the computers are physically and sometimes geographically far apart.



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