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88C196EC Microcontroller

Specification Update

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88C196EC Microcontroller Specification Update

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Contents

Revision History

Date	Version	Description
11/11/98	003	Added Errata #20, Stack Overflow Module.
08/12/98	002	Added Errata #18 and #19 and Documentation Changes #25 and #26
03/16/98	001	This is the new Specification Update document. It contains all identified errata published prior to this date.

Preface

As of July, 1996, Intel's Computing Enhancement Group has consolidated available historical device and documentation errata into this new document type called the Specification Update. We have endeavored to include all documented errata in the consolidation process, however, we make no representations or warranties concerning the completeness of the Specification Update.

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order #
88C196EC CHMOS 16-Bit Microcontroller datasheet (Automotive)	272889
88C196EC Microcontroller User's Manual	272890

Nomenclature

Errata are design defects or errors. These may cause the 88C196EC microcontroller's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 88C196EC microcontroller product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark)	
or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

‖	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

No.	Steppings				Page	Status	ERRATA
	A3	B0	B1	B2			
1	X				11	Fixed	Unable to read EPA/eEPA SFR registers
2	X				11	Fixed	PLLEN pin not latched on rising edge of reset
3	X				11	Fixed	Flash High-Byte Access
4	X				11	Fixed	CS0# Strong Pull-Up Enabled with EA# = 1
5	X				12	Fixed	P5.4 Medium Pull-Up Enabled During TROM Execution mode.
6	X				12	Fixed	Reset Source CFD Bit
7	X				12	Fixed	SCNEN Pin ESD
8	X				12	Fixed	eEPA Transmitter
9	X				12	Fixed	PIH Lost Interrupts
10	X				12	Fixed	V_{IL} Specification Marginality
11	X				12	Fixed	NMI Pull-Up Strength
12	X				13	Fixed	AD15 Bus Control
13	X	X	X		13	Fixed	Port Initialization
14	X	X	X	X	13	NoFix	Odd Uprom Bit Read from TROM
15	X	X	X	X	13	NoFix	eEPA Concatenation
16	X	X	X	X	14	NoFix	NMIE Interrupt Lost when PIH Interrupt Pending
17		X	X	X	14	NoFix	ICE CS0# Functionality
18	X	X	X	X	14	NoFix	RSTSRC Register Clear on VCC Power-up
19	X	X	X	X	14	NoFix	Reset During Code RAM Read Operation
20	X	X	X	X	14	NoFix	Stack Overflow Module

Specification Changes

No.	Steppings				Page	Status	SPECIFICATION CHANGES
	A3	B0	B1	B2			
1	X	X	X	X	15	Doc	Flash Program/Erase Temperature Spec
2	X	X	X	X	15	Doc	I_{OH2} Specification
3		X	X	X	15	Doc	PLLEN pin latched on reset

Specification Clarifications

No.	Steppings				Page	Status	SPECIFICATION CLARIFICATIONS
	A3	B0	B1	B2			
							None in this revision.

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
1	User's Manual	17	Doc	Page 6-3, Figure 6-2, Interrupt Service Flow Diagram
2	User's Manual	17	Doc	Page A-20, Table A-6, IDLPD Instruction Definition
3	User's Manual	18	Doc	Page 11-10, Figure 11-5, A/D Command (AD_COMMAND) Register
4	User's Manual	18	Doc	Page 11-11, Section 11.5, Determining A/D Status and Conversion Results
5	User's Manual	18	Doc	Page 16-1, Figure 16-1, SDU Block Diagram
6	User's Manual	18	Doc	Page 16-3, Figure 16-2, SDU Functional Block Diagram
7	User's Manual	19	Doc	Page 16-6, Section 16.3.3, Minimizing Latency
8	User's Manual	19	Doc	Page 17-22, Section 17.9, Erasing the Flash Memory Block
9	User's Manual	19	Doc	Page C-122, Table C-16, EPA13_TIME SFR
10	User's Manual	19	Doc	Page C-65, Table C-11, Px_DIR Addresses and Reset States
11	User's Manual	20	Doc	Page C-66, Table C-12, Px_MODE Addresses and Reset States
12	User's Manual	20	Doc	Page C-67, Table C-13, Px_PIN Addresses and Reset States
13	User's Manual	20	Doc	Page C-69, Table C-14, Px_REG Addresses and Reset States
14	User's Manual	20	Doc	Pages C-7-8, Table C-2, Register Name, Address, and Reset Value
15	User's Manual	20	Doc	Page 2-20, Figure 2-9, CCR1 Register
16	User's Manual	20	Doc	Page 15-19, Figure 15-7, CCR1 Register
17	272889	21	Doc	Page 18, Section 6.0, Electrical Characteristics
18	272889	21	Doc	Page 18-19, Table 6.1, DC Characteristics
19	User's Manual	21	Doc	Page 9-22, Section 9.5.1, Consistent MSB bit length procedure in SSIO
20	User's Manual	21	Doc	Page 10-28, Figure 10-21, Timer x Control (TxCONTROL) Register
21	User's Manual	21	Doc	Page 10-7, Figure 10-2, EPA Timer/Counters
22	User's Manual	22	Doc	Page 10-15, Figure 10-7, EPAPWM Receive/Transmit Channel
23	User's Manual	22	Doc	Page 10-24, Section 10.7, Generating a 32-Bit Time Value
24	User's Manual	22	Doc	Page 10-38, Figure 10-25, EPAPWMx Control Register
25	User's Manual	22	Doc	Page 13-13 Figure 13-11, RSTSRC Register
26	User's Manual	22	Doc	Page C-86, RSTSRC Register

Identification Information

Markings

Bottom mark: NG88C196EC

Errata

1.   Unable to read EPA/eEPA SFR registers

Problem: During a read of the EPA and eEPA SFR registers, there was contention found in the data bus that these two modules share. This contention caused the values in both the EPA and eEPA registers to be read simultaneously. Therefore, the data was invalid.

Implication: Affected applications that read from these registers.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

2.   PLLEN pin not latched on rising edge of reset

Problem: The target specification for this device stated that "the state of the PLLEN pin is latched at the rising edge of reset. Thus, any transitions during operation will have no effect upon the PLL." The A-3 silicon did not contain the necessary logic to behave in this manner.

Implication: Noisy applications could cause the PLLEN pin to switch states during execution.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

3.   Flash High-Byte Access

Problem: Odd addresses in the Flash could not be accessed. This is because the block lock bits which control access to the Flash are only read by the even byte sense amps. When programming, erasing, or executing a flash function the lock bits are read first. If the address of the function to be performed was an odd address then the odd byte sense amps were used so the lock bits were not accessed and the read from the even byte sense amps returned a logic "1". This caused the device to think the block lock bits were programmed which disabled the Flash functions.

Implication: Unable to run code from on-chip Flash.

Workaround: Use external memory option.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

4.   CS0# Strong Pull-Up Enabled with EA# = 1

Problem: The CS0# pin had a strong pull-up enabled when running internally and from test ROM execution mode.

Implication: A strong driver is needed to overdrive CS0# to a low voltage level to allow entry into certain test ROM execution modes including: SIO RISM mode, Auto Programming mode, Slave Dump/ Programming mode, and Uprom Dump/Programming mode.

Workaround: Provide a strong driver in application to overdrive the CS0# pin to a low voltage.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

5. P5.4 Medium Pull-Up Enabled During TROM Execution mode.

Problem: The P5.4 pin had a medium pull-up enabled when executing from test ROM execution mode.

Implication: A strong driver is needed to overdrive P5.4 to a low voltage to enter all test ROM execution modes excluding SDU mode.

Workaround: Provide strong driver in application to overdrive the P5.4 pin to a low voltage.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

6. Reset Source CFD Bit

Status: The CFD bit was not correctly set in the reset source SFR register. The bit was set to a "1" even though a reset due to the oscillator fail detect circuitry did not occur. This problem occurred when the power supply ramp from 0 V to 5 V was too fast.

Implication: Affects applications that use the CFD bit to determine application flow. Since nodes ND1 and PURS control reset signals which in turn control many different functions in the device, other application uses may also be adversely affected.

Workaround: Add external capacitors to the V_{CC} supply to slow the voltage ramp from 0 V to 5 V.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

7. SCNEN Pin ESD

Problem: The SCNEN pin did not meet Intel's qualification requirements for ESD protection.

Implication: The SCNEN pin was sensitive to ESD.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

8. eEPA Transmitter

Problem: An eEPA would not reset its associated pin if a match within the same eEPA occurred "simultaneously".

Implication: eEPA events may be missed.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

9. PIH Lost Interrupts

Problem: When a read from the PIH interrupt pending register occurred at the same time as an incoming interrupt, the new interrupt was lost.

Implication: Interrupts may be lost.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

10. V_{IL} Specification Marginality

Problem: V_{IL} was marginal to target specifications causing yield fallout.

Implication: Device may not work with other devices depending on how clean their input low signal is.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

11. NMI Pull-Up Strength

Problem: NMI Pull-Up Strength was not strong enough to meet target specifications.

Implication: NMI pin could cause an interrupt by going low due to weak pull-up.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

12. AD15 Bus Control

Problem: Address Data pin 15 may intermittently fail after the execution of a Ljmp instruction. This pin may be read as a one instead of a zero because of a glitch that occurs when the pin output driver is turned off. The glitch is caused by the data changing before the output driver is completely turned off. The AD15 pin is the farthest pin from the driving logic. Under extreme conditions, the AD14 pin may also fail.

Implication: May affect applications that use the Ljmp instruction.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

13. Port Initialization

Problem: Depending on which phase the device is brought out of reset, a race condition may occur between the reset signal and the data input into the port SSEL and DIR registers. This affects ports 2, 6, 7, 8, and 9. Instead of the registers being initialized to their default reset settings, they may get initialized to whatever was last on the internal PDB.

Implication: May affect applications that depend on the pins on these ports to come up in their defined reset state.

Status: Fixed. Refer to Summary Table of Changes to determine the affected stepping(s).

14. Odd Uprom Bit Read from TROM

Problem: The test ROM code used to read the status of the "Uprom" bits utilizes the Cobra FACE commands. The Cobra FACE command for reading the "Uprom" (or block lock bit) status outputs the status on AD0. However, the bus controller only outputs AD8-AD15 when reading from odd addresses. Therefore, when accessing the odd block lock bit addresses (Uprom bits DEI and CLK1), the status will always read as "programmed" regardless of the state of the bits.

Implication: May affect applications that program and verify the Uprom bits DEI and CLK1.

Workaround: Read the UPROM Special Function Register (1FF6h) to determine the status of the Uprom bits. (Refer to *88C196EC Microcontroller User's Manual*, P. 17-40.)

Status: NoFix. Refer to Summary Table of Changes to determine the affected stepping(s).

15. eEPA Concatenation

Problem: In the EPAPWM control registers (figure 10-25 in User's Manual), bit 0 is defined as the Enable Module Concatenation bit. This feature does not work on the device. This bit should be set to a "0".

Status: NoFix. Refer to Summary Table of Changes to determine the affected stepping(s).

16.   NMIE Interrupt Lost when PIH Interrupt Pending

Problem: When a PIH interrupt is pending, a NMIE interrupt will not be serviced. Instead, the pending PIH interrupt will be serviced even if it is globally disabled.

Implication: Interrupts will be incorrectly serviced under above described conditions. Affects in-circuit emulator designs only.

Status: NoFix. Refer to Summary Table of Changes to determine the affected stepping(s).

17.   ICE CS0# Functionality

Problem: CS0# functionality is disabled while in ICE mode.

Implication: CS0# pin cannot be emulated on emulator.

Status: NoFix. Refer to Summary Table of Changes to determine the affected stepping(s).

18.   RSTSRC Register Clear on V_{CC} Power-up

Status: The four least-significant bits in the RSTSRC register (CFDRST, WDTRST, SFWRST, and EXTRST) are supposed to be cleared when V_{CC} is powered up. The CFDRST, WDTRST, and SFWRST bits may be erroneously set on V_{CC} power-up and cannot be guaranteed to be cleared.

Implication: Applications that rely on these bits to be cleared on V_{CC} power-up may be adversely affected.

Status: NoFix. Refer to the Summary Table of Changes to determine the affected stepping(s).

19.   Reset During Code RAM Read Operation

Problem: During the time that the device is reading data from code RAM, a code RAM corruption may occur if:

- a device reset occurs from a falling edge on the RESET# pin

- a watchdog time-out event occurs or

- a clock fail detect event occurs

Implication: Code RAM data corruption may occur as a result of the reset event.

Workaround: If code RAM data integrity must be maintained after the reset event, prevent external resets, watchdog time-out events, and clock fail detect events from occurring during a code RAM read operation

Status: NoFix. Refer to Summary Table of Changes to determine the affected stepping(s).

20.   Stack Overflow Module

Problem: Writing an address to location 001C18h in the Upper Register File that is less than or equal to the lower stack boundary (STACK_BOTTOM) or greater than or equal to the upper boundary (STACK_TOP) generates a stack overflow interrupt.

Implication: Inadvertent stack overflow interrupts may occur during normal code execution.

Status: NoFix. Refer to the Summary Table of Changes to determine the affected stepping(s).

Specification Changes

1.   Flash Program/Erase Temperature Spec

Issue: Operating temperature specifications for programming and erasing the on-chip Flash on the 88C196EC has been changed from -40°C – 125°C to 0°C – 70°C.

Implication: Intel does not guarantee that the Flash programming and erasing capabilities will function correctly above 70°C and below 0°C.

Affected Docs: *88C196EC CHMOS 16-Bit Microcontroller* datasheet - 272889

2. I_{OH2} Specification

Issue: The I_{OH2} specification has been changed in the following manner:

- Old

  -30 µA to -120 µA ($V_{OH2} = V_{CC}$ - 1.0 V)
  -75 µA to -240 µA ($V_{OH2} = V_{CC}$ - 2.5 V)
  -90 µA to -280 µA ($V_{OH2} = V_{CC}$ - 4.0 V)

- New

  -30 µA to -140 µA ($V_{OH2} = V_{CC}$ - 1.0 V)
  -65 µA to -280 µA ($V_{OH2} = V_{CC}$ - 2.5 V)
  -75 µA to -350 µA ($V_{OH2} = V_{CC}$ - 4.0 V)

Affected Docs: *88C196EC CHMOS 16-Bit Microcontroller* datasheet - 272889

3.   PLLEN pin latched on reset

Issue: On the 88C196EC A-step, the PLLEN pin was not latched on reset. On the B-step, a latch was added to the PLLEN pin so that the state of the PLL can only be changed at the time of reset.

Affected Docs: *88C196EC Microcontroller User's Manual*

Specification Clarifications

None for this revision of the specification update.

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Documentation Changes

1. **Page 6-3, Figure 6-2, Interrupt Service Flow Diagram**

Issue: Interrupt service flow diagram is incorrect. A normal interrupt will not be serviced if the PTSSEL.x bit is set to 1. To make correct, the following change needs to be made: Add "PTSSEL.x bit = 0?" conditional branch after yes branch of "Interrupts Enabled?" If conditional answer is "yes," continue to "priority resolver" block. If conditional answer is "no," then continue to "return".

Affected Docs: *88C196EC Microcontroller User's Manual*

2. **Page A-20, Table A-6, IDLPD Instruction Definition**

Issue: Illegal key definition is incorrect. Key = 3 is not considered an illegal key by the device and will not cause the device to reset. Only keys greater than 3 are considered illegal.

Old Definition:

IDLE/POWERDOWN. Depending on the 8-bit value of the KEY operand, this instruction causes the device to:

- enter idle mode, if KEY = 1,

- enter powerdown mode, if KEY = 2,

- execute a reset sequence, if KEY = any value other than 1 or 2.

The bus controller completes any prefetch cycle in progress before the CPU stops or resets.

        If KEY = 1 then
            enter idle
        else if KEY = 2 then
            enter powerdown
        else
            execute reset

PSW Flag Settings					
Z	N	C	V	VT	ST
Key = 1 or 2					
—	—	—	—	—	—
Key = any value other than 1 or 2					
0	0	0	0	0	0

- New Definition:

  IDLE/POWERDOWN. Depending on the 8-bit value of the KEY operand, this instruction causes the device to:

  > enter idle mode, if KEY = 1,
  >
  > enter powerdown mode, if KEY = 2,
  >
  > execute a reset sequence, if KEY = any value greater than 3.

  The bus controller completes any prefetch cycle in progress before the CPU stops or resets.

  If KEY = 1 then
  > enter idle

  else if KEY = 2 then
  > enter powerdown
  > else if KEY > 3 then
  > execute reset

PSW Flag Settings					
Z	**N**	**C**	**V**	**VT**	**ST**
Key = 1 or 2					
—	—	—	—	—	—
Key = any value greater than 3					
0	0	0	0	0	0

Affected Docs: *88C196EC Microcontroller User's Manual*

3. **Page 11-10, Figure 11-5, A/D Command (AD_COMMAND) Register**

Issue: Added sentence to "GO bit" note: "GO bit must be set to 0 for A/D SCAN to work."

Affected Docs: *88C196EC Microcontroller User's Manual*

4. **Page 11-11, Section 11.5, Determining A/D Status and Conversion Results**

Issue: The last sentence of the first paragraph is incorrect.

- Old: "If you read the AD_RESULT or AD_RESULTx before the conversion is complete, the result is not guaranteed to be accurate."

- New: "If you read the AD_RESULT register before the conversion is complete, the result is not guaranteed to be accurate. The AD_RESULTx register can be read at any time."

Affected Docs: *88C196EC Microcontroller User's Manual*

5. **Page 16-1, Figure 16-1, SDU Block Diagram**

Issue: Code RAM size in SDU block diagram is incorrect. The diagram should specify 2.75 Kbytes of Code RAM, not 3 Kbytes.

Affected Docs: *88C196EC Microcontroller User's Manual*

6. **Page 16-3, Figure 16-2, SDU Functional Block Diagram**

Issue: Code RAM size and Test ROM size in SDU Functional Block Diagram is incorrect. The diagram should specify 2.75 Kbytes of Code RAM, not 3 Kbytes and 4 Kbytes of Test ROM, not 1 Kbyte.

Affected Docs: *88C196EC Microcontroller User's Manual*

7.   **Page 16-6, Section 16.3.3, Minimizing Latency**

Issue: Entire section is not worded correctly.

- Old:

  The issue of latency arises when the SDU starts a cycle and the bus controller wants to use the code RAM in the next state. If any user application is executing from code RAM when the SDU is attempting to access the code RAM, you will incur a significant performance decline in your code RAM accesses. Even if the bus controller is idle, the SDU cannot access the code RAM without some small effect.

  Because accesses to the code RAM by the SDU require at least two CPU state times, it is necessary to understand what the bus controller is doing at all times to ensure that any latency will be minimized.

- New:

  The SDU can only access the code RAM when the bus controller is starting an access to memory other than code RAM (i.e., Flash or external memory). Accesses to register RAM do not count in most cases since the CPU directly accesses the register file. Therefore, it is necessary to understand what the bus controller is doing in the user application at all times to minimize latency.

Affected Docs: *88C196EC Microcontroller User's Manual*

8.   **Page 17-22, Section 17.9, Erasing the Flash Memory Block**

Issue: The second paragraph in section 17.9 is incorrect. P2.0 does not go low if an erase failure occurs.

- Old: "The erase routine has the effect of driving pin P2.6 to a "logic 0" if the erase failed, and driving pin P2.0 to a "logic 0" for a period of 15 state times."

- New: "The erase routine has the effect of driving pin P2.6 to a "logic 0" if the erase failed."

Affected Docs: *88C196EC Microcontroller User's Manual*

9.   **Page C-122, Table C-16, EPA13_TIME SFR**

Issue: Register location for EPA13_TIME is incorrect. The correct location is 1F3Eh.

- Old:

Register Mnemonic	Memory Location	32-Byte WSR	Windows Direct Address	64-Byte WSR	Windows Direct Address	128-Byte WSR	Windows Direct Address
EPA13_TIME	1F2Ah	79H	EAH	3CH	EAH	1EH	AAH

- New:

Register Mnemonic	Memory Location	32-Byte WSR	Windows Direct Address	64-Byte WSR	Windows Direct Address	128-Byte WSR	Windows Direct Address
EPA13_TIME	1F3Eh	79H	FEH	3CH	FEH	1EH	BEH

Affected Docs: *88C196EC Microcontroller User's Manual*

10.   **Page C-65, Table C-11, Px_DIR Addresses and Reset States**

Issue: P6_DIR register address is incorrect. It should be 1FE3h, not 1FD3h.

Affected Docs: *88C196EC Microcontroller User's Manual*

11.   **Page C-66, Table C-12, Px_MODE Addresses and Reset States**

Issue: P6_MODE register address is incorrect. It should be 1FE1h, not 1FD0h.

Affected Docs: *88C196EC Microcontroller User's Manual*

12.   **Page C-67, Table C-13, Px_PIN Addresses and Reset States**

Issue: P6_PIN register address is incorrect. It should be 1FE7h, not 1FD7h.

Affected Docs: *88C196EC Microcontroller User's Manual*

13.   **Page C-69, Table C-14, Px_REG Addresses and Reset States**

Issue: P6_REG register address is incorrect. It should be 1FE5h, not 1FC4h.

Affected Docs: *88C196EC Microcontroller User's Manual*

14.   **Pages C-7-8, Table C-2, Register Name, Address, and Reset Value**

Issue: The following register addresses need to be corrected:

P6_DIR should be 1FE3h, not 1FD3h

P6_MODE should be 1FE1h, not 1FD0h

P6_PIN should be 1FE7h, not 1FD7h

P6_REG should be 1FE5h, not 1FC4h

Affected Docs: *88C196EC Microcontroller User's Manual*

15.   **Page 2-20, Figure 2-9, CCR1 Register**

Issue: CFD bit definition is incorrect. The enable and disable bits are reversed.

- Old:
  0 = enables clock-failure detection circuitry
  1 = disables clock-failure detection circuitry

- New:
  0 = disables clock-failure detection circuitry
  1 = enables clock-failure detection circuitry

Affected Docs: *88C196EC Microcontroller User's Manual*

16.   **Page 15-19, Figure 15-7, CCR1 Register**

Issue: CFD bit definition is incorrect. The enable and disable bits are reversed.

- Old:
  0 = enables clock-failure detection circuitry.
  1 = disables clock-failure detection circuitry.

- New:
  0 = disables clock-failure detection circuitry.
  1 = enables clock-failure detection circuitry.

Affected Docs: *88C196EC Microcontroller User's Manual*

17. Page 18, Section 6.0, Electrical Characteristics

Issue: Added Note 4 to T_C under Operating Conditions. Note 4 states "Flash programming and erase operations only guaranteed to work from $0\,℃$ to $+70\,℃$".

Affected Docs: *88C196EC CHMOS 16-Bit Microcontroller* datasheet - 272889.

18. Page 18-19, Table 6.1, DC Characteristics

Issue: Changed the following DC Characteristic Parameters:

1. I_{PD}: Typical changed from 20 µA to 50 µA. Max value no longer specified.

2. I_{OH2} Max with $V_{OH2} = V_{CC}$ - 1.0 V changed from -120 µA to -140 µA.

3. I_{OH2} Min with $V_{OH2} = V_{CC}$ - 2.5 V changed from -75 µA to -65 µA.

4. I_{OH2} Max with $V_{OH2} = V_{CC}$ - 2.5 V changed from -240 µA to -280 µA.

5. I_{OH2} Min with $V_{OH2} = V_{CC}$ - 4.0 V changed from -90 µA to -75 µA.

6. I_{OH2} Max with $V_{OH2} = V_{CC}$ - 4.0 V changed from -280 µA to -350 µA.

Affected Docs: *88C196EC CHMOS 16-Bit Microcontroller* datasheet - 272889

19. Page 9-22, Section 9.5.1, Consistent MSB bit length procedure in SSIO

Issue: Inserted "Disable Interrupts" between steps 1 and 2 in procedure for achieving a consistent MSB bit length.

Affected Docs: *88C196EC Microcontroller User's Manual*

20. Page 10-28, Figure 10-21, Timer x Control (TxCONTROL) Register

Issue: UD bit description incorrectly states that the T2CONTROL direction bit controls the direction of both timers 1 and 2 when in concatenation mode. T1CONTROL direction bit actually controls the direction of both timers 1 and 2 when in concatenation mode.

- Old:

  If T2CONTROL.7 is set, this bit in T2CONTROL controls the direction of both timers 2 and 1.

- New:

  If T2CONTROL.7 is set, this bit in T1CONTROL controls the direction of both timers 2 and 1.

Affected Docs: *88C196EC Microcontroller User's Manual*

21. Page 10-7, Figure 10-2, EPA Timer/Counters

Issue: When timer concatenation is enabled, the OVRTM1 signal from timer 1 does not go through the timer 2 prescalar module. To fix the diagram, the 2x1 multiplexer for T2CONTROL.7 should be switched with the Prescalar module. The input to the prescalar module will now be the output from the 2x1 multiplexer for T2CONTROL.4:3 and the output will go into the 2x1 multiplexer for T2CONTROL.7 along with the OVRTM1 signal. The output of the 2x1 multiplexer for T2CONTROL.7 will go to clock.

Affected Docs: *88C196EC Microcontroller User's Manual*

22.   **Page 10-15, Figure 10-7, EPAPWM Receive/Transmit Channel**

Issue: EEPA concatenation does not function on 88C196EC. Dotted line entitled "Concatenate" connecting EN_EPAx_CON to EPAPWM pin should be deleted in Figure 10-7.

Affected Docs: *88C196EC Microcontroller User's Manual*

23.   **Page 10-24, Section 10.7, Generating a 32-Bit Time Value**

Issue: EEPA concatenation does not function on the 88C196EC. Remove last sentence in first paragraph on section 10.7, "You can also use timers 1 and 2 and any pair of adjacent EPAPWM channels in this same manner."

Affected Docs: *88C196EC Microcontroller User's Manual*

24.   **Page 10-38, Figure 10-25, EPAPWMx Control Register**

Issue: EEPA concatenation does not function on the 88C196EC. Change bit 0 definition of EPAPWMx Control register from EMC to Reserved bit. "EMC" in column 2 will change to "-". Column 3 should change to "Reserved; always write as zero."

Affected Docs: *88C196EC Microcontroller User's Manual*

25.   **Page 13-13 Figure 13-11, RSTSRC Register**

Issue: The reset state of register is not 00h. It is xxh.

- Old
  Reset state: 00h

- New
  Reset state: xxh

Affected Docs: 88C196EC Microcontroller User's Manual

26.   **Page C-86, RSTSRC Register**

Issue: The reset state of register is not 00h. It is xxh.

- Old
  Reset state: 00h

- New
  Reset state: xxh