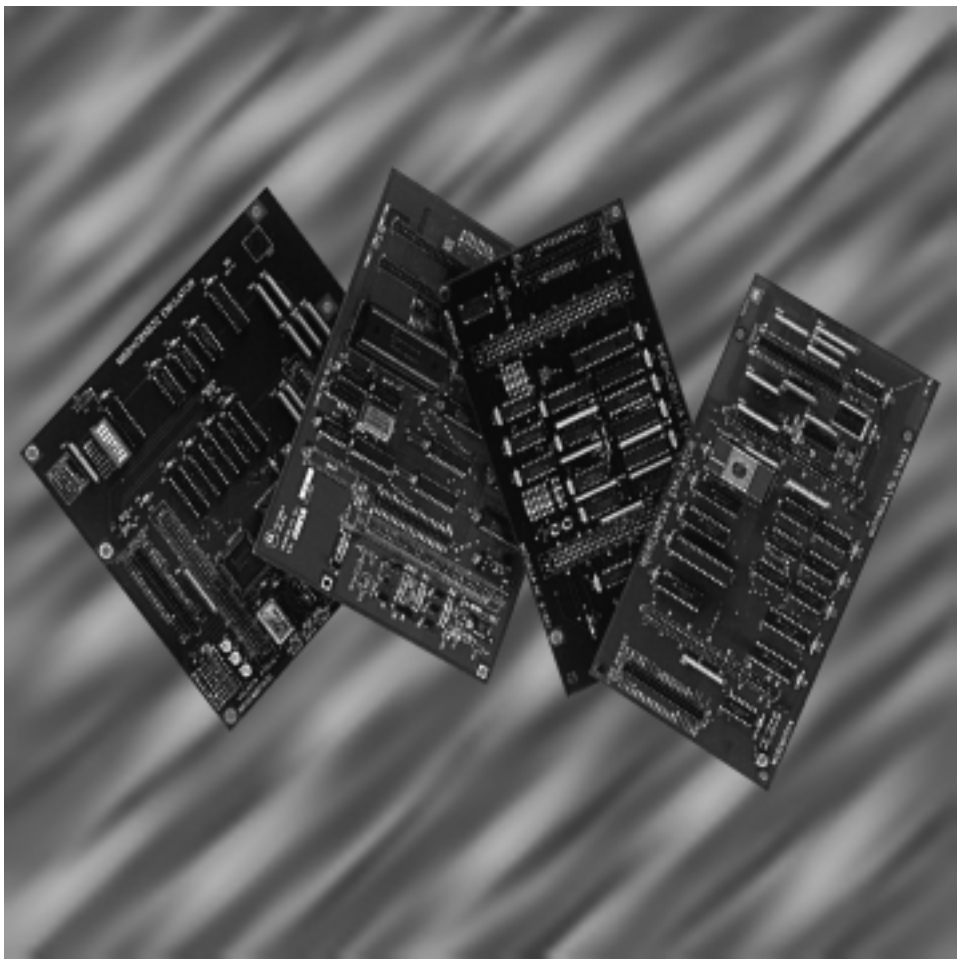
M68EM08JB8UM/D
REV. 1

M68EM08JB8

EMULATION MODULE
USER'S MANUAL



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Section 1. General Description

1.1 Contents

1.2 Introduction

This user's manual explains connection, configuration, and operation information specific to the M68EM08JB8 emulator module (JB8EM). The JB8EM lets you emulate and debug target systems based on the MC68HC908JB8 microcontroller unit (MCU):

This section describes Motorola's two development systems that use the JB8EM, and it explains the JB8EM's layout.

1.3 Development Systems

The JB8EM can be part of two Motorola development systems:

- MMDS0508 Motorola Modular Development System (MMDS)
- MMEVS0508 Motorola Modular Evaluation System (MMEVS)

1.3.1 Motorola Modular Development System (MMDS)

The MMDS is an emulator system that provides a bus state analyzer and real-time memory windows. The unit's integrated design environment includes an editor, an assembler, user interface, and source-level debug.

A complete MMDS consists of:

- Station module — The metal MMDS enclosure containing the control board and the internal power supply
- Emulator module (EM) — A separately purchased printed circuit board that enables system functionality for a specific set of MCUs
- Two logic clip cable assemblies — Twisted-pair cables that connect the station module to the target system, a test fixture, a clock, an oscillator, or any other circuitry useful for evaluation or analysis. One end of each cable assembly has a molded connector, which fits into station-module pod A or pod B. Leads at the other end of each cable terminate in female probe tips. Ball clips come with the cable assemblies.
- 9-lead RS-232 serial cable — Cable that connects the station module to the host computer RS-232 port
- 9- to 25-pin adapter — A molded assembly that connects the 9-pin cable to a 25-pin serial port
- System software — MCUez™ software on CD-ROM and P&E Microcomputer System, Inc. software on CD-ROM
- MMDS documentation — *MMDS Operations Manual*, Motorola document order number MMDS0508OM/D; the MCUez software manual, included with the MCUez software package; a system software manual, included with the P&E Microcomputer System, Inc.'s MMDS0508 software package; and this emulator user's manual

MMDS baud rates are selected by the user at 2400, 4800, 9600, 19,200, 38,400, or 57,600.

As mentioned, the JB8EM gives the MMDS the ability to emulate target systems based on MC68HC908JB8 MCUs. By substituting a different EM, MMDS can be enabled to emulate target systems based on a different MCU. (A local Motorola representative can explain all the EMs available.)

1.3.2 Motorola Modular Evaluation System (MMEVS)

An MMEVS is an economical, two-board tool for designing, debugging, and evaluating target systems based on MC68HC05 or MC68HC08 MCUs.

A complete MMEVS consists of:

- Platform board (PFB) — The bottom board, which supports the emulator module; has connectors for power and for a terminal or host computer
- Emulator module (EM) — A separately purchased printed circuit board that enables system functionality for a specific set of MCUs; fits onto the PFB
- RS-232 serial cable — A separately purchased cable that connects the PFB to the host computer RS-232 port
- System software — MCUez™ software on CD-ROM and P&E Microcomputer System, Inc. software on CD-ROM
- MMEVS documentation — *MMEVS Operations Manual*, Motorola document order number MMEVSOM/D; the MCUez software manual, included with the MCUez software package; a system software manual, included with the P&E Microcomputer System, Inc.’s MMDS0508 software package; and this emulator user's manual

An MMEVS features automatic selection of the communication baud rate from these choices: 2400, 4800, 9600, 19,200, 38,400, or 57,600.

With a JB8EM, the MMEVS emulates target systems based on MC68HC908JB8 MCUs. By substituting a different EM, the MMEVS can be enabled to emulate target systems based on a different MCU. (A local Motorola representative can explain all the EMs available.)

Section 2. Configuration and Operation explains how to configure and use the JB8EM as part of an MMDS or MMEVS system.

1.4 EM Layout

Figure 1-1 shows the layout of the JB8EM.

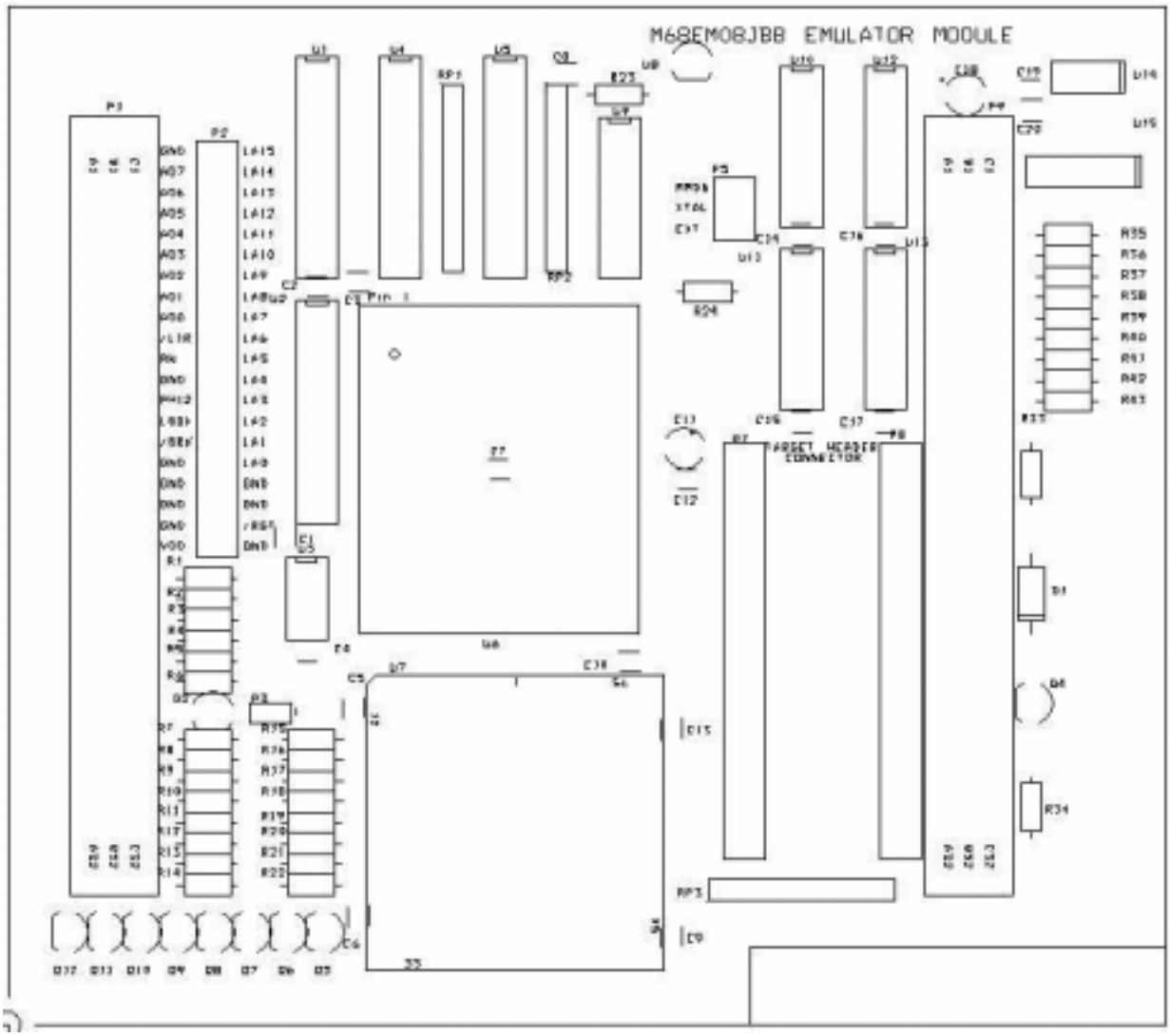


Figure 1-1. M68EM08JB8 Emulator Module

The main elements of the JB8EM are:

- DIN connectors P1 and P9 — Connect the EM to the MMDS control board or the MMEVS platform board
- Connector P2 — Permits connection to a logic analyzer
- Jumper header P3 — Connect a 1MΩ resistor between D– pin of MC68HC908JB8 and ground.
- Jumper header P5 — Selects the MCU clock source
- Connectors P7 and P8 — Customer-specific interfaces to the target system

The JB8EM requires a user-supplied 80-lead target cable and target head adapter to connect the target system to connectors P7 and P8.

1.5 Specifications

Table 1-1 lists JB8EM specifications.

Table 1-1. M68EM08JB8 Specifications

Characteristics	Specifications
MCU extension I/O ports	HCMOS compatible
Operating temperature	0° to 40°C
Storage temperature	–40° to +85°C
Relative humidity	0 to 90% (non-condensing)
Power requirements	+5 V dc and +12 V dc (charge pump), provided from the MMDS control board or MMEVS platform board
Dimensions	5.5 x 4.9 inches; 140 x 125 mm
Weight	5.8 ounces; 164 g

General Description

Section 2. Configuration and Operation

2.1 Contents

2.2 Introduction

This section explains configuration and operation of the JB8EM when it is installed in an MMDS (Motorola modular development system) or MMEVS (Motorola modular evaluation system). For other parts of system installation or configuration, see the MMDS or MMEVS hardware manuals.

NOTE: *A JB8EM already installed in an MMDS station module can be reconfigured. To do so, switch off station-module power, then follow the guidance in this section. Similarly, JB8EM that is already installed on the MMEVS platform board can be reconfigured, provided that platform-board power is disconnected.*

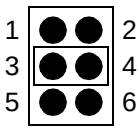
CAUTION: *Be sure to switch off or disconnect power when reconfiguring an installed EM. Reconfiguring EM jumper headers with the power on can damage system circuits.*

ESD CAUTION: *Ordinary amounts of static electricity from clothing or the work environment can damage or degrade electronic devices and equipment. For example, the electronic components installed on printed circuit boards are extremely sensitive to electrostatic discharge (ESD). Wear a ground wrist strap whenever handling any printed circuit board. This strap provides a conductive path for safely discharging static electricity to ground.*

2.3 Setting Jumper Headers

The JB8EM has two jumper headers. **Table 2-1** contains a summary of settings for these headers. **2.3.1 Pulldown Enable Jumper (P3)** and **2.3.2 Clock Source Header (P5)** give additional information about each jumper header.

Table 2-1. Jumper Headers

Jumper Header	Type	Description
P3		Jumper between pins 1 and 2; connects a 1MΩ resistor between the D– pin of the MC68HC908JB8 and ground. This prevents a USB reset when the D– signal from the target system is in a high impedeance state.
P5		Jumper between pins 1 and 2; selects the clock signal from the MMDS control board or MMEVS platform board Jumper between pins 3 and 4 (factory default); selects the onboard 6MHz crystal oscillator Jumper between pins 5 and 6; selects an external clock source for the OSC1 input signal from target head connectors

2.3.1 Pulldown Enable Jumper (P3)

Install a jumper on jumper header P3 to connect a 1MΩ resistor between D– of MC68HC908JB8 and ground. DO NOT remove this jumper; if removed, proper operation of the system cannot be guaranteed. **Figure 2-1** shows the default factory jumper header configuration, which has a fabricated jumper installed on jumper header P3 between pins 1 and 2.

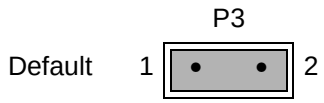


Figure 2-1. Jumper Header P3

2.3.2 Clock Source Header (P5)

Jumper header P5 in **Figure 2-2** determines the clock signal source. The factory configuration (the fabricated jumper between pins 3 and 4) selects the on-board 6MHz crystal oscillator at location Y1.

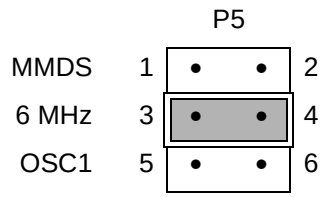


Figure 2-2. Jumper Header P5

Alternately, two other clock signal sources can be selected, as shown in **Figure 2-2**.

- To select the clock signal from the MMDS control board or MMEVS platform board install the fabricated jumper between pins 1 and 2. Then use the system software to select a frequency.
- To select the target system as the clock source, install the fabricated jumper between pins 5 and 6. Ensure that the clock source (OSC1) is connected to the EM through the target cable, connector P7 pin 3.

NOTE: *Only one jumper should be inserted on jumper header P5 at a time. Inserting multiple jumpers in P5 might damage the JB8EM.*

2.4 Remaining System Installation

When both jumper headers are configured, follow these steps to complete the JB8EM installation:

- To install the JB8EM in an MMDS station module, remove the entire top half of the station-module enclosure. Fit together EM connectors P1 and P9 (on the bottom of the board) and control-board connectors P1 and P2. Snap the corners of the EM onto the plastic standoffs.
- To install the JB8EM on an MMEVS platform board, fit together EM connectors P1 and P9 (on the bottom of the board) and platform-board connectors P3 and P4. Snap the corners of the EM onto the plastic standoffs.
- Copy the personality file from the provided P&E or MCUez CD-ROMs to the directory that contains the debugging software. The personality file for the MC68HC908JB8 MCU are:
  - 00C57Vxx.MEM - MCUez personality file
  - 00457Vxx.MEM - P&E personality file

At this point, make any system cable connections and restore power. For instructions, consult the MMDS or MMEVS operations manuals.

Section 3. Connector Information

3.1 Contents

3.2 Introduction

This section consists of pin assignments and signal descriptions for M68EM08JB8 target and logic analyzer connectors.

3.3 Logic Analyzer Connector (P2)

Connector P2 is the JB8EM logic analyzer connector.

Figure 3-1 shows the pin assignments for connector P2. **Table 3-1** gives the signal descriptions.

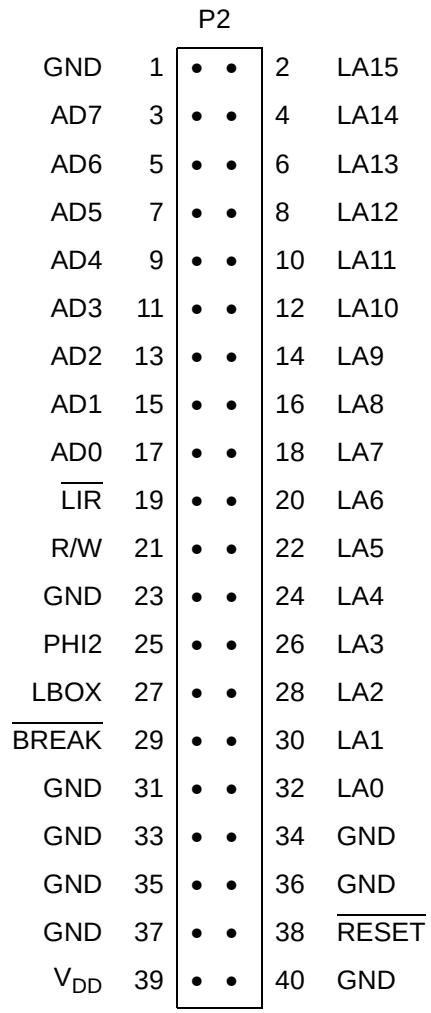


Figure 3-1. Logic Analyzer Connector P2 Pin Assignments

Table 3-1. Logic Analyzer Connector P2 Signal Descriptions

Pin	Mnemonic	Signal
1	GND	GROUND
2	LA15	Address bus bit 15 — MCU output address bus
3	AD7	Data bus bit 7 — MCU bidirectional data bus
4	LA14	Address bus bit 14 — MCU output address bus
5	AD6	Data bus bit 6 — MCU bidirectional data bus
6	LA13	Address bus bit 13 — MCU output address bus
7	AD5	Data bus bit 5 — MCU bidirectional data bus
8	LA12	Address bus bit 12 — MCU output address bus
9	AD4	Data bus bit 4 — MCU bidirectional data bus
10	LA11	Address bus bit 11 — MCU output address bus
11	AD3	Data bus bit 3 — MCU bidirectional data bus
12	LA10	Address bus bit 10 — MCU output address bus
13	AD2	Data bus bit 2 — MCU bidirectional data bus
14	LA9	Address bus bit 9 — MCU output address bus
15	AD1	Data bus bit 1 — MCU bidirectional data bus
16	LA8	Address bus bit 8 — MCU output address bus
17	AD0	Data bus bit 0 — MCU bidirectional data bus
18	LA7	Address bus bit 7 — MCU output address bus.
19	$\overline{\text{LIR}}$	Load instruction register — Active-low output signal, asserted when an instruction starts
20	LA6	Address bus bit 6 — MCU output address bus
21	R/W	Read/Write — Output signal that indicates the direction of data transfer
22	LA5	Address bus bit 5 — MCU output address bus
23	GND	GROUND
24	LA4	Address bus bit 4 — MCU output address bus
25	PHI2	PHI2 clock — Internally generated output clock signal used as a timing reference
26	LA3	Address bus bit 3 — MCU output address bus

Table 3-1. Logic Analyzer Connector P2 Signal Descriptions (Continued)

Pin	Mnemonic	Signal
27	LBOX	Last bus cycle — Input signal that the emulator asserts to indicate that the target system MCU is in the last bus cycle of an instruction
28	LA2	Address bus bit 2 — MCU output address bus
29	$\overline{\text{BREAK}}$	$\overline{\text{BREAK}}$ — Active low signal that the EM asserts to stop the target system MCU from running user code
30	LA1	Address bus bit 1 — MCU output address bus
31	GND	GROUND
32	LA0	Address bus bit 0 — MCU output address bus
33	GND	GROUND
34	GND	GROUND
35	GND	GROUND
36	GND	GROUND
37	GND	GROUND
38	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ — Active-low bidirectional signal for starting an EVS reset
39	V_{DD}	+5 Vdc power — Input voltage (+5 Vdc @ 1A (max)) used by the EM logic circuits
40	GND	GROUND

3.4 Target Connectors (P7 and P8)

JB8EM has two target connectors: P7 and P8, each a 2-row by 20-pin connector.

Figure 3-2, **Table 3-2**, and **Table 3-3** give the pin assignments and signal descriptions for these connectors.

P7

V_{SS}	1	2	PTB2	
OSC1	3	4	V_{SS}	
PTB3	5	6	PTD0	
PTB5	7	8	PTD2	
PTB6	9	10	NC	
$\overline{\text{RESET}}$	11	12	NC	
PTA1	13	14	NC	
PTA3	15	16	NC	
PTC6	17	18	NC	
V_{SS}	19	20	NC	
NC	21	22	PTE0	
NC	23	24	V_{SS}	
NC	25	26	PTA5	
NC	27	28	PTA7	
NC	29	30	PTD6	
NC	31	32	PTD7	
NC	33	34	PTC3	
PTD4	35	36	PTC1	
PTE3	37	38	V_{SS}	
PTC0	39	40	V_{SS}	

P8

VREG	1	2	EVDD	
NC	3	4	PTB1	
V_{SS}	5	6	PTB0	
PTB4	7	8	PTD1	
V_{SS}	9	10	NC	
PTB7	11	12	NC	
PTA0	13	14	V_{SS}	
PTA2	15	16	NC	
PTC7	17	18	NC	
PTC5	19	20	NC	
NC	21	22	PTC4	
NC	23	24	PTE2	
NC	25	26	PTA4	
V_{SS}	27	28	PTA6	
NC	29	30	PTD5	
NC	31	32	V_{SS}	
NC	33	34	$\overline{\text{IRQ}}$	
PTD3	35	36	PTC2	
PTE1	37	38	V_{SS}	
PTE4	39	40	V_{SS}	

Figure 3-2. Target Connectors P7 and P8 Pin Assignments

Table 3-2. Target Connector P7 Signal Descriptions

Pin	Mnemonic	Signal
1	V_{SS}	EM GROUND — Ground signal of the EM board
2	PTB2	PORT B (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
3	OSC1	OSCILLATOR — Crystal oscillator amplifier input signal
4	V_{SS}	EM GROUND — Ground signal of the EM board
5	PTB3	PORT B (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers
6	PTD0	PORT D (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
7	PTB5	PORT B (bit 5) — General-purpose I/O lines controlled by software via data direction and data registers
8	PTD2	PORT D (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
9	PTB6	PORT B (bit 6) — General-purpose I/O lines controlled by software via data direction and data registers
10	NC	No connect
11	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ — Active-low bidirectional control line that initializes the MCU
12	NC	No connect
13	PTA1	PORT A (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
14	NC	No connect
15	PTA3	PORT A (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers
16	NC	No connect
17	PTC6	PORT C (bit 6) — General-purpose I/O lines controlled by software via data direction and data registers
18	NC	No connect
19	V_{SS}	EM GROUND — Ground signal of the EM board
20	NC	No connect
21	NC	No connect

Table 3-2. Target Connector P7 Signal Descriptions (Continued)

Pin	Mnemonic	Signal
22	PTE0	PORT E (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
23	NC	No connect
24	V_{SS}	EM GROUND — Ground signal of the EM board.
25	NC	No connect
26	PTA5	PORT A (bit 5) — General-purpose I/O lines controlled by software via data direction and data registers
27	NC	No connect
28	PTA7	PORT A (bit 7) — General-purpose I/O lines controlled by software via data direction and data registers
29	NC	No connect
30	PTD6	PORT D (bit 6) — General-purpose I/O lines controlled by software via data direction and data registers
31	NC	No connect
32	PTD7	PORT D (bit 7) — General-purpose I/O lines controlled by software via data direction and data registers
33	NC	No connect
34	PTC3	PORT C (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers
35	PTD4	PORT D (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
36	PTC1	PORT C (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
37	PTE3	PORT E (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers
38	V_{SS}	EM GROUND — Ground signal of the EM board
39	PTC0	PORT C (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
40	V_{SS}	EM GROUND — Ground signal of the EM board

Table 3-3. Target Connector P8 Signal Descriptions

Pin	Mnemonic	Signal
1	VREG	VREG — the 3.3V output of the on-chip voltage regulator
2	EV_{DD}	MMDS +5 V — Used for factory testing
3	NC	No connect
4	PTB1	PORT B (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
5	V_{SS}	EM GROUND — Ground signal of the EM board
6	PTB0	PORT B (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
7	PTB4	PORT B (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
8	PTD1	PORT D (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
9	V_{SS}	EM GROUND — Ground signal of the EM board
10	NC	No connect
11	PTB7	PORT B (bit 7) — General-purpose I/O lines controlled by software via data direction and data registers
12	NC	No connect
13	PTA0	PORT A (bit 0) — General-purpose I/O lines controlled by software via data direction and data registers
14	V_{SS}	EM GROUND — Ground signal of the EM board
15	PTA2	PORT A (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
16	NC	No connect
17	PTC7	PORT C (bit 7) — General-purpose I/O lines controlled by software via data direction and data registers
18	NC	No connect
19	PTC5	PORT C (bit 5) — General-purpose I/O lines controlled by software via data direction and data registers
20, 21	NC	No connect
22	PTC4	PORT C (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
23	NC	No connect

Table 3-3. Target Connector P8 Signal Descriptions (Continued)

Pin	Mnemonic	Signal
24	PTE2	PORT E (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
25	NC	No connect
26	PTA4	PORT A (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
27	V_{SS}	EM GROUND — Ground signal of the EM board
28	PTA6	PORT A (bit 6) — General-purpose I/O lines controlled by software via data direction and data registers
29	NC	No connect
30	PTD5	PORT D (bit 5) — General-purpose I/O lines controlled by software via data direction and data registers
31	NC	No connect
32	V_{SS}	EM GROUND — Ground signal of the EM board
33	NC	No connect
34	$\overline{IRQ}$	INTERRUPT REQUEST — Active-low input line for requesting MCU asynchronous non-maskable interrupt
35	PTD3	PORT D (bit 3) — General-purpose I/O lines controlled by software via data direction and data registers
36	PTC2	PORT C (bit 2) — General-purpose I/O lines controlled by software via data direction and data registers
37	PTE1	PORT E (bit 1) — General-purpose I/O lines controlled by software via data direction and data registers
38	V_{SS}	EM GROUND — Ground signal of the EM board
39	PTE4	PORT E (bit 4) — General-purpose I/O lines controlled by software via data direction and data registers
40	V_{SS}	EM GROUND — Ground signal of the EM board

3.5 Target Cable Assembly

To connect the JB8EM to a target system, a separately purchased target cable assembly is needed, plus the appropriate target head and target-head/adapter package.

Figure 3-3 shows how one end of the flex cable plugs into the JB8EM module, and it also shows how the target head connects into the target system.

If the JB8EM is installed in the MMDS station module, run the flex cable through the slit in the station-module enclosure.

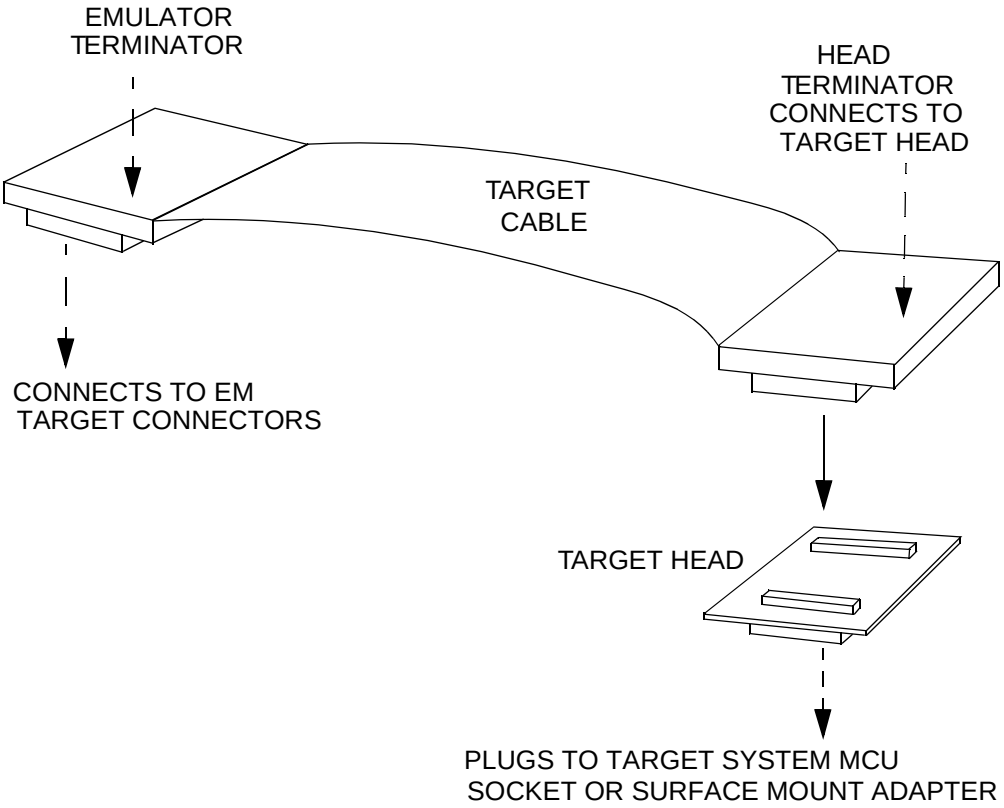
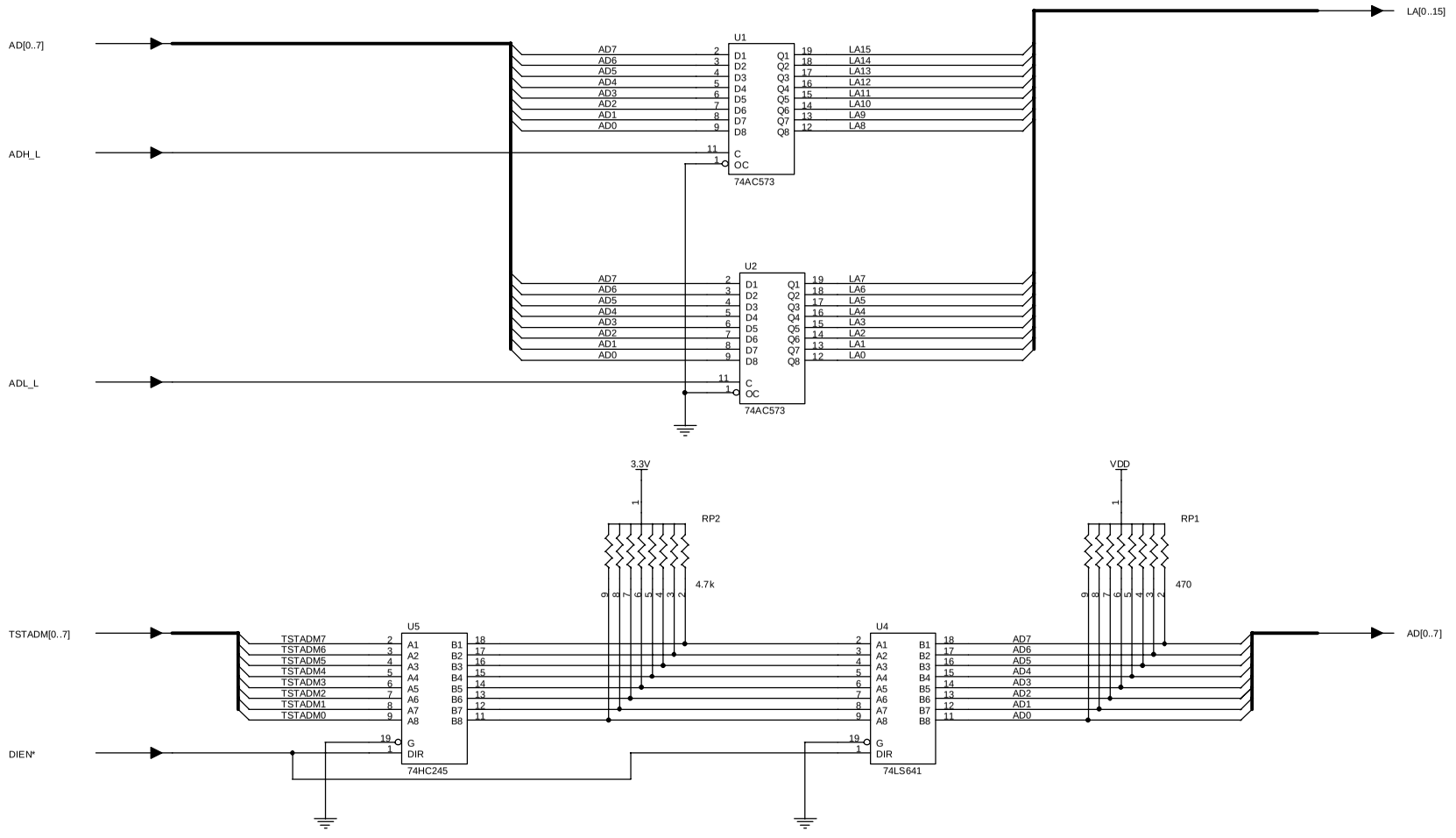


Figure 3-3. Target Cable Assembly

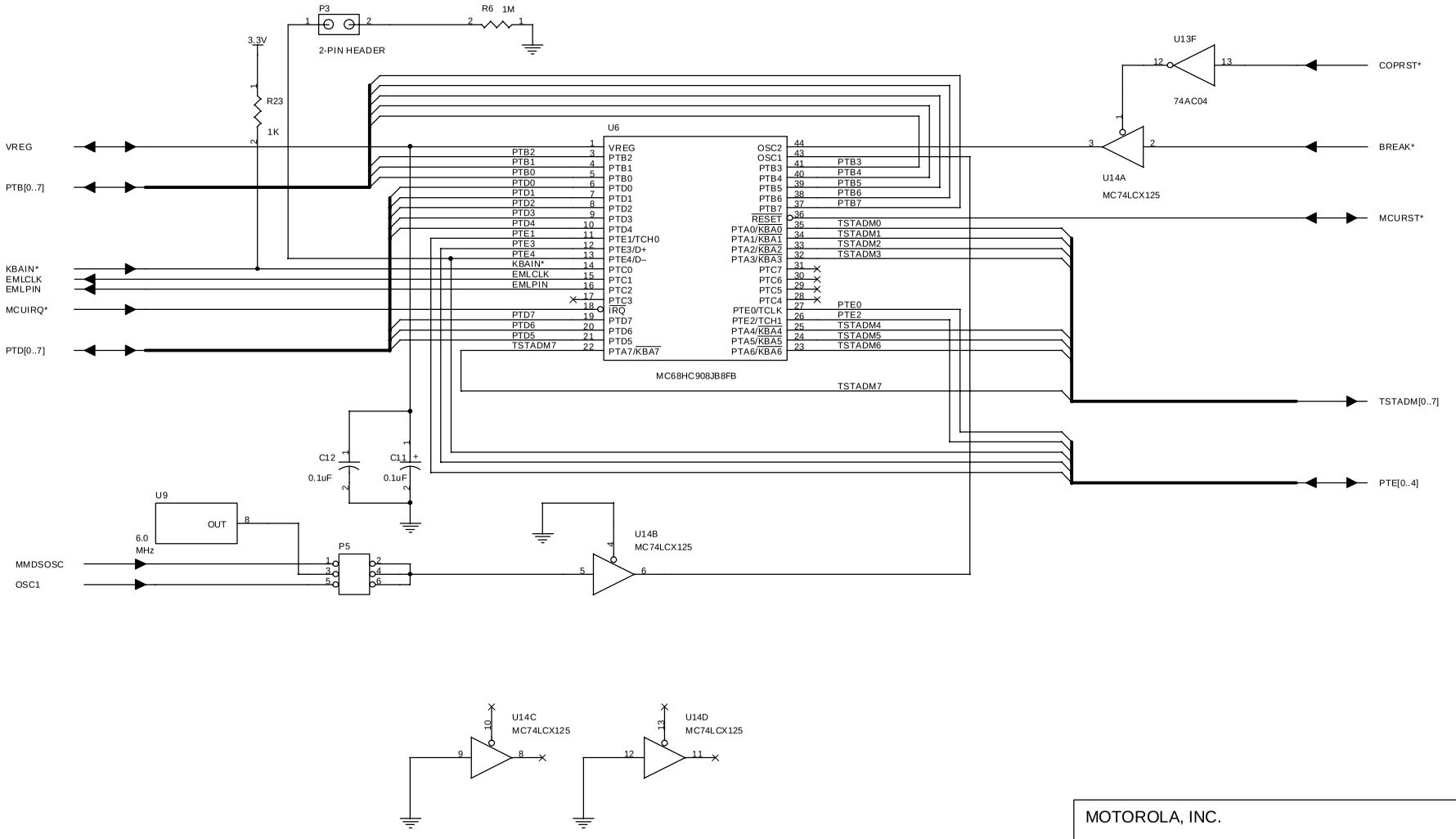
Section 4. Schematics

This chapter contains the JB8EM emulator module schematic diagrams.

These schematic diagrams are for reference only and may deviate slightly from the circuits on the JB8EM.



MOTOROLA, INC.			
Title: M68EM08JB8 Emulator Module (Address Bus Module)			
Size: B	Designed By: Kelvin Tse	Approved By: Edward Chui	Rev: B
Date: Tuesday, November 30, 1999	Sheet 1 of 9		



MOTOROLA, INC.			
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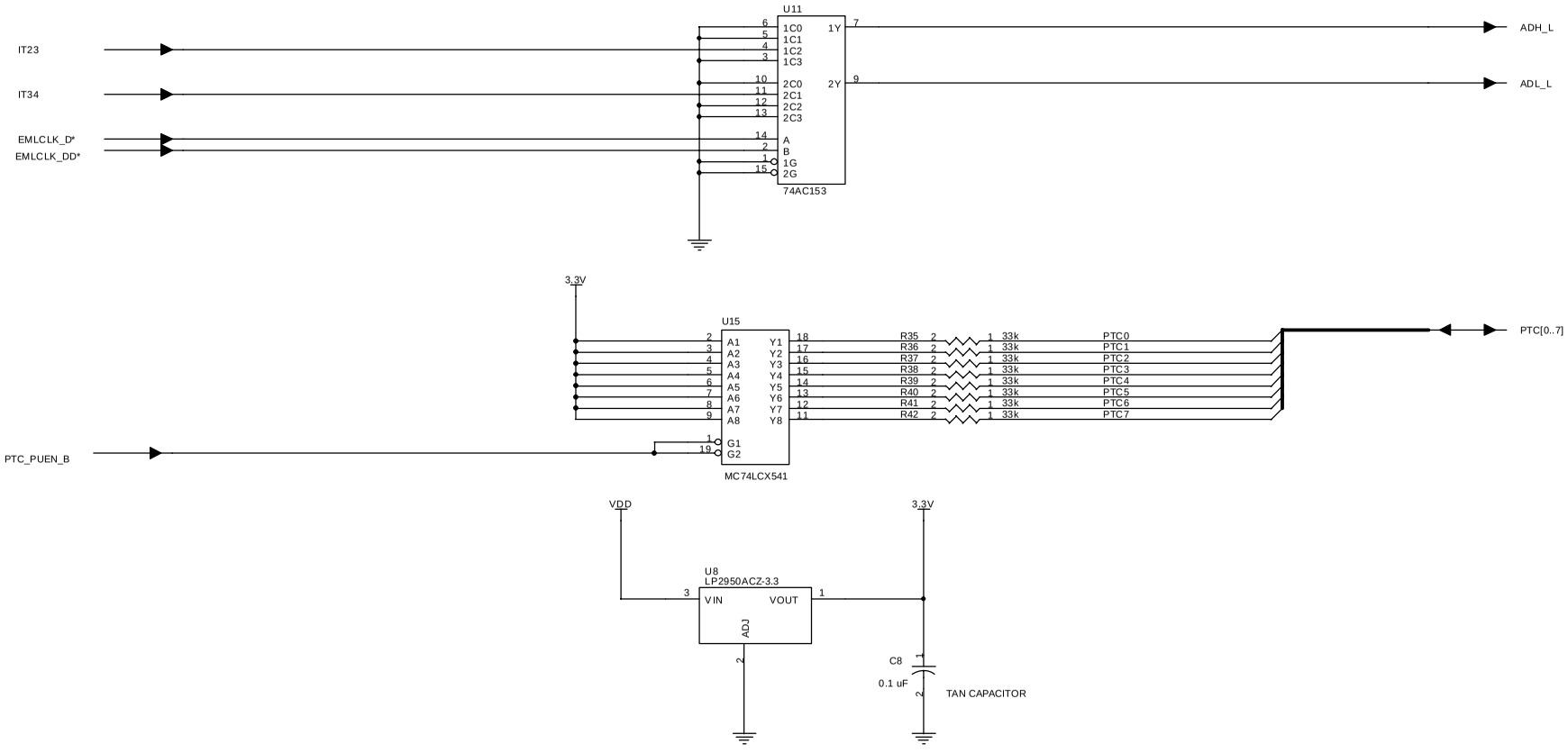
Size: B	Designed By: Kelvin Tse	Approved By: Edward Chui	Rev: B
Date: Tuesday, November 30, 1999	Sheet 2 of 9		



MOTOROLA, INC.			
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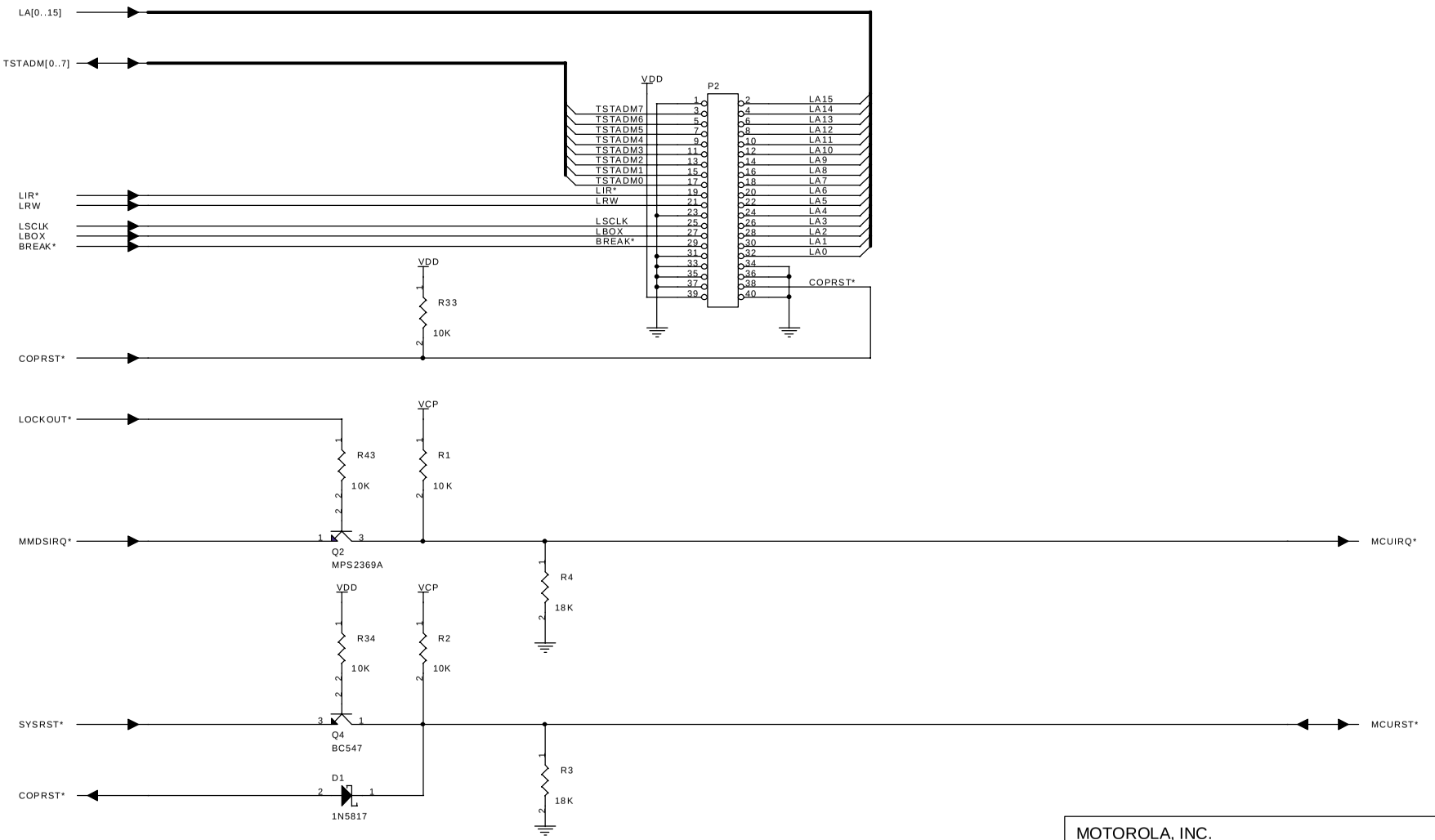
Size: B	Designed By: Kelvin Tse	Approved By: Edward Chui	Rev: A
Date: Tuesday, November 30, 1999	Sheet 3 of 9		



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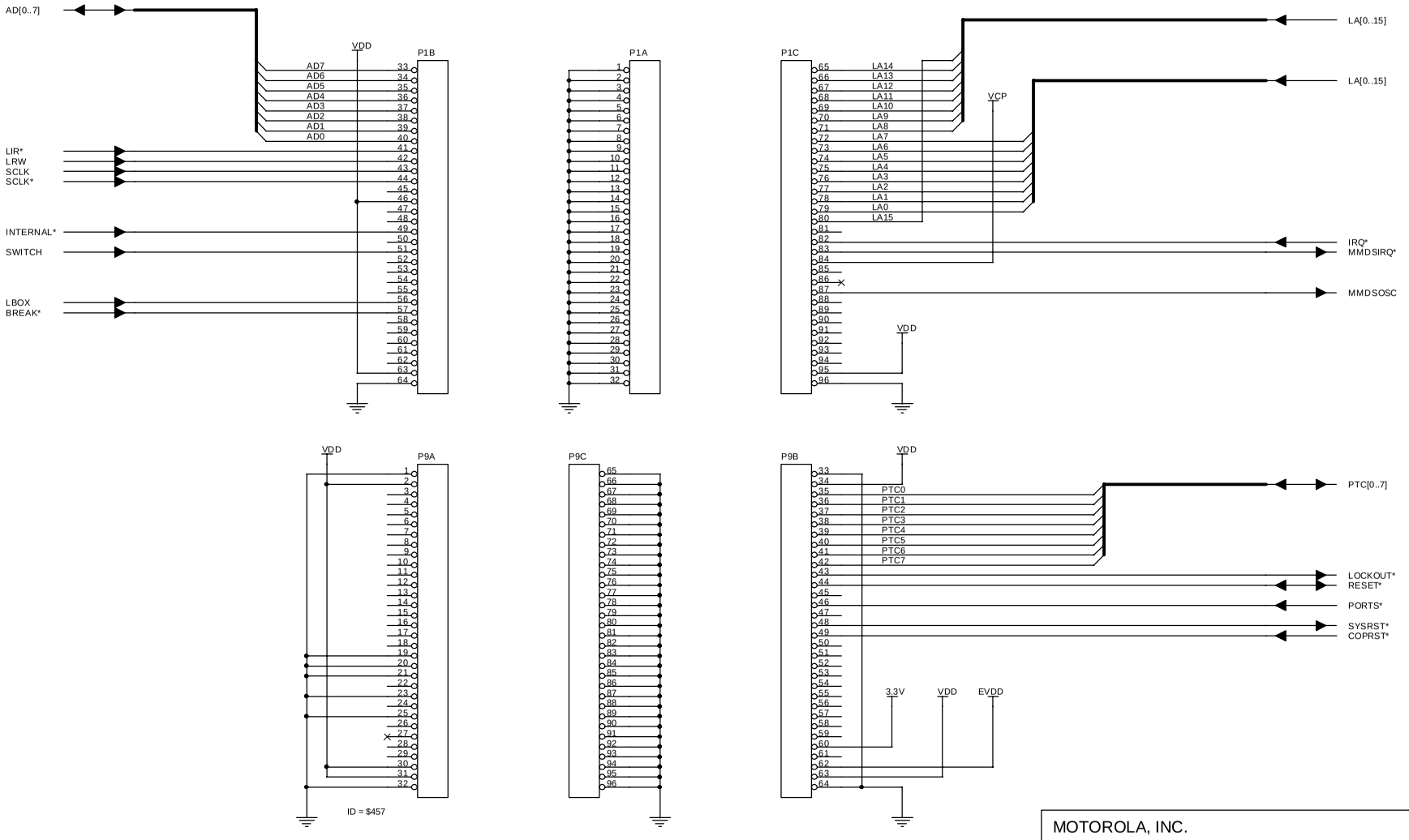
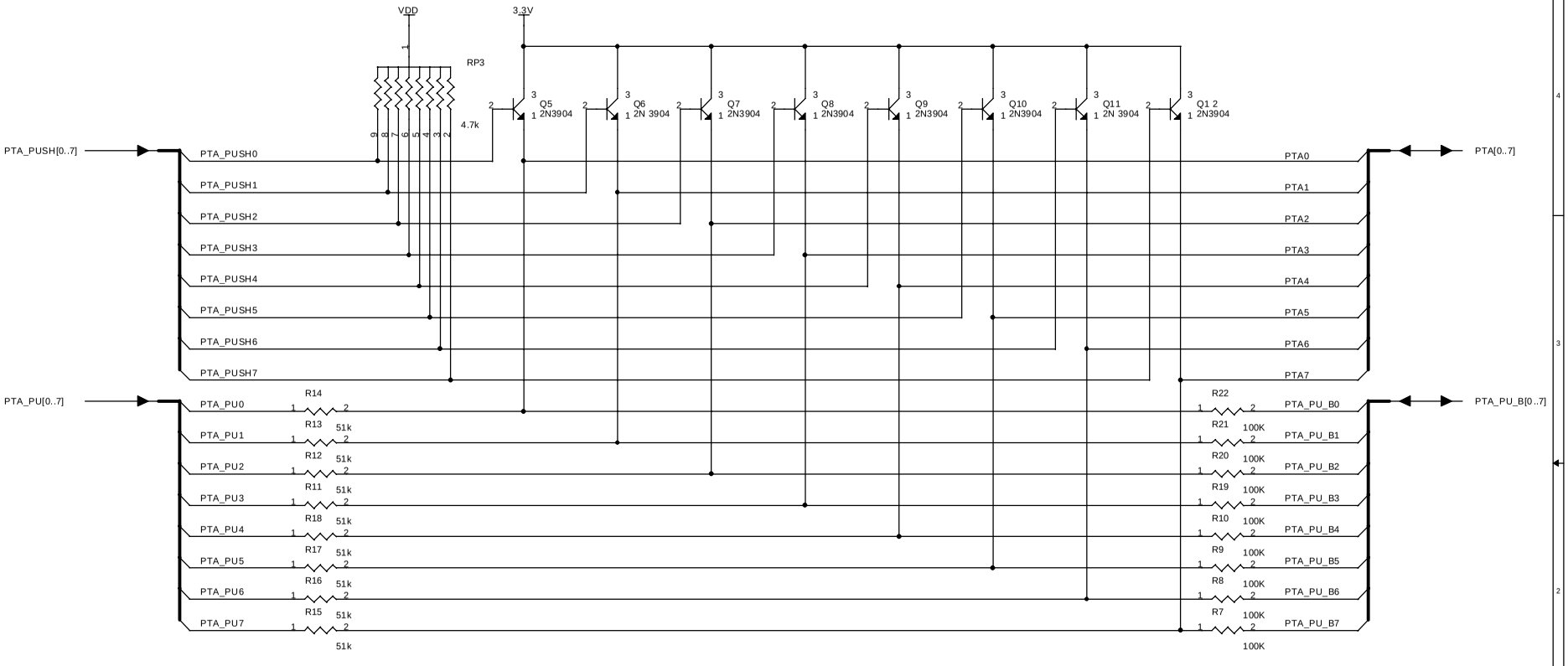


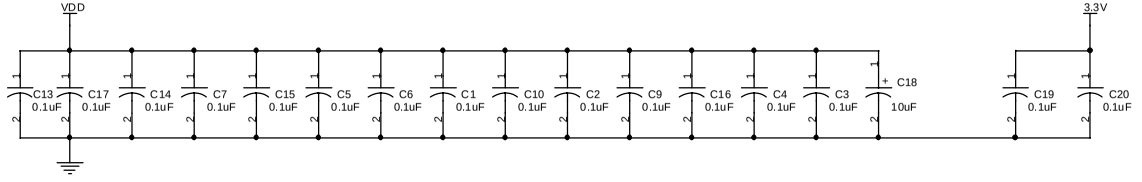
MOTOROLA, INC.

Title: M68EM08JB8 Emulator Module (Platform Board Connectors)

Size	Designed By:	Approved By:	Rev
B	Kelvin Tse	Edward Chui	A

Date: Wednesday, August 11, 1999 Sheet 5 of 9



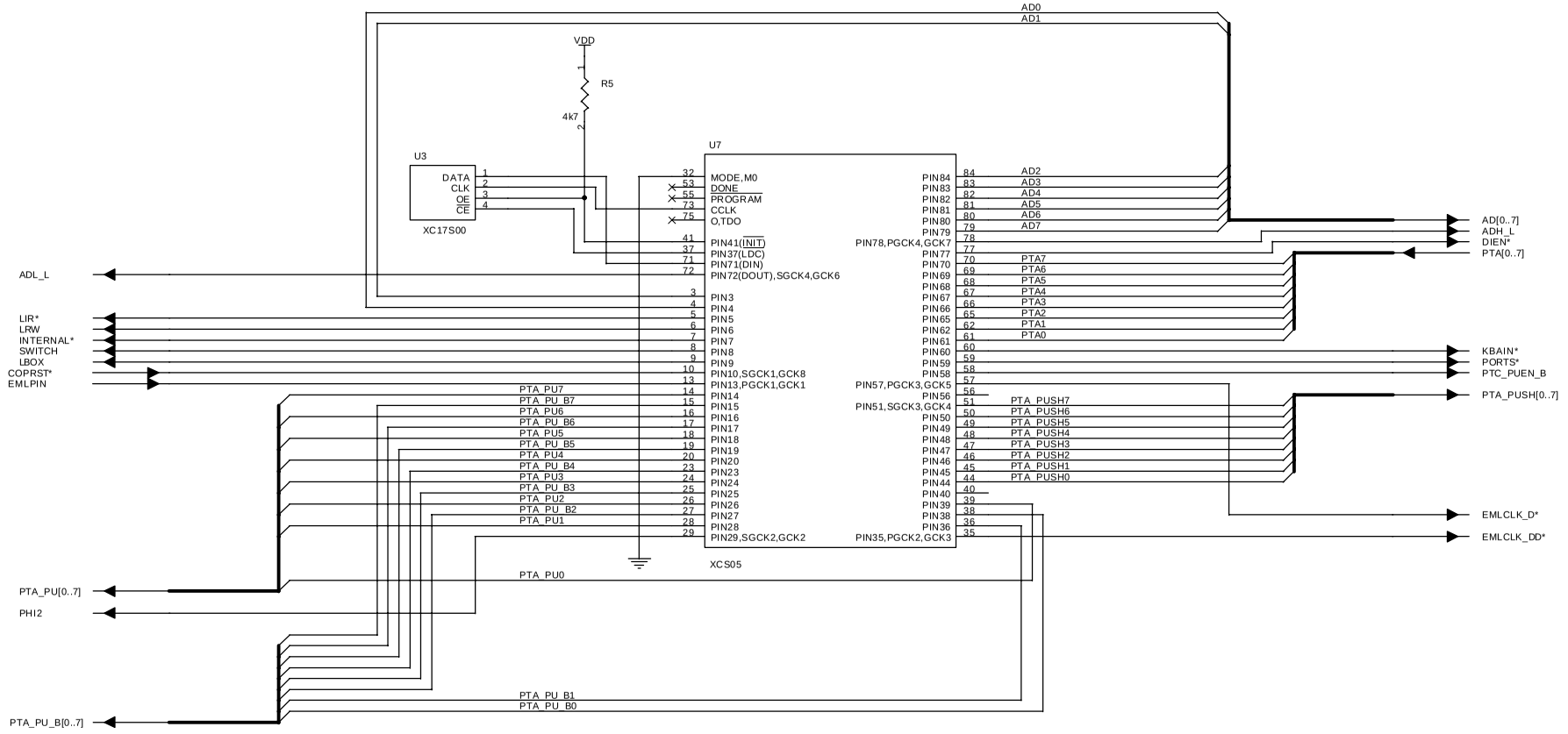


MOTOROLA, INC.

Title: M68EM08JB8 Emulator Module (Port A Pull-up)

Size	Designed By:	Approved By:	Rev
B	Kelvin Tse	Edward Chui	A

Date: Wednesday, August 11, 1999 Sheet 6 of 9

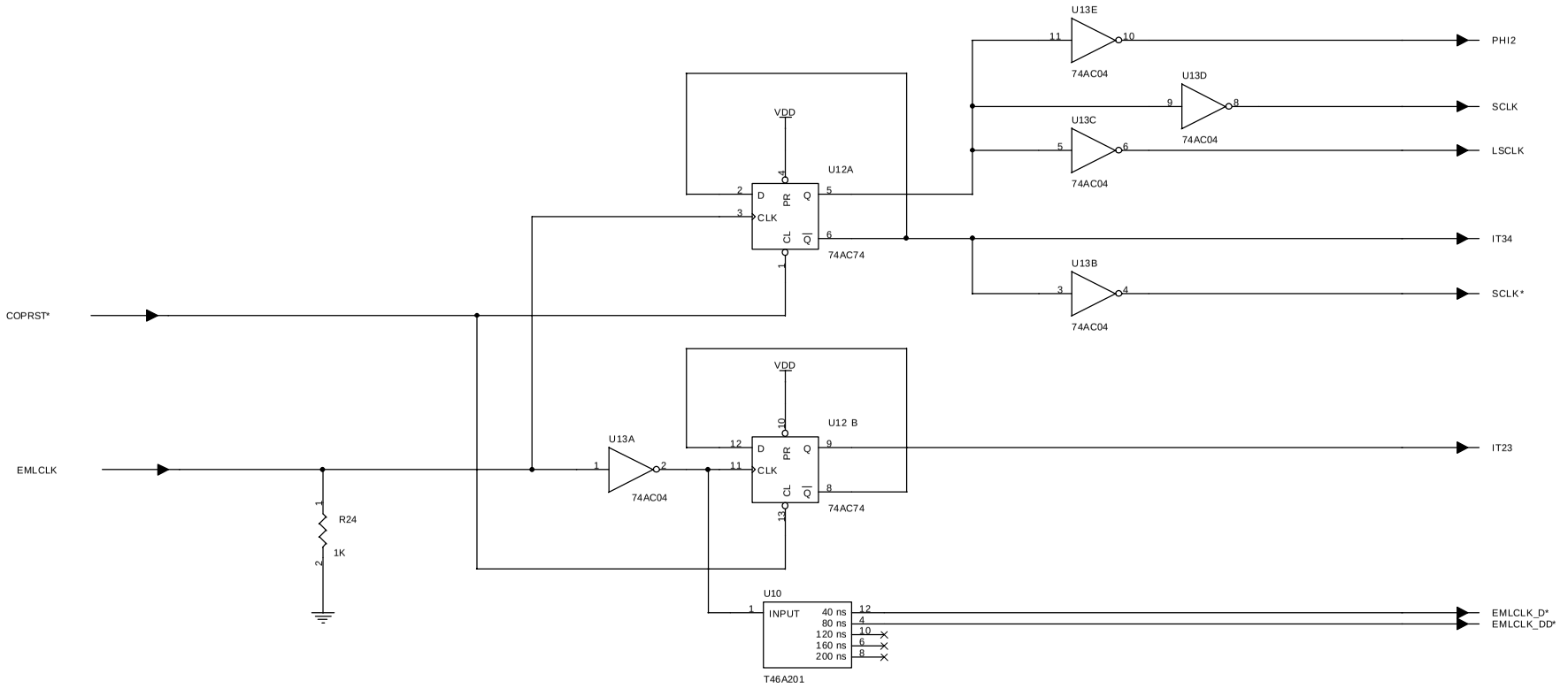


MOTOROLA, INC.

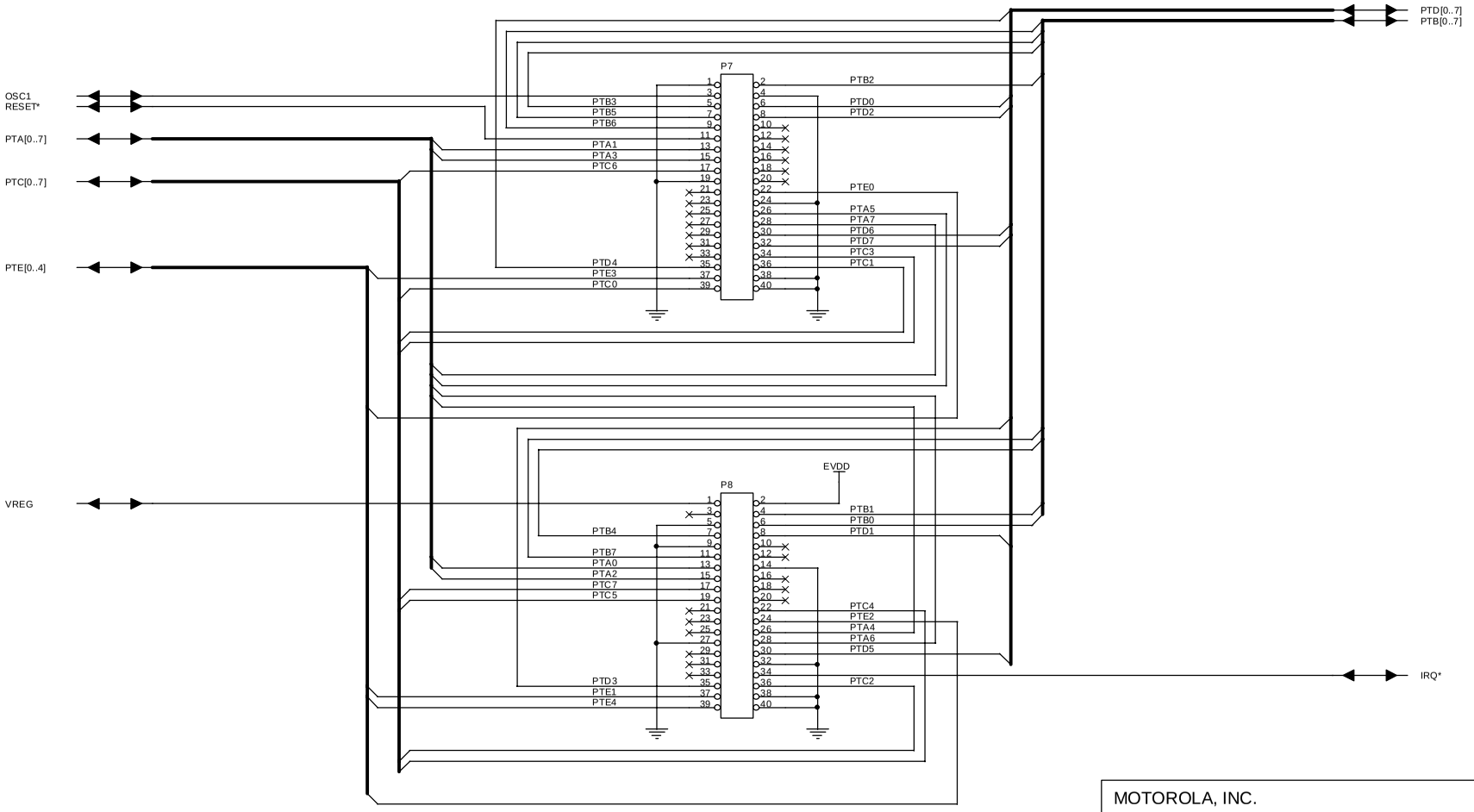
Title: M68EM08JB8 Emulator Module (Programmable Logic Module)

Size	Designed By:	Approved By:	Rev
B	Kelvin Tse	Edward Chui	A

Date: Thursday, December 02, 1999 Sheet 7 of 9



MOTOROLA, INC.			
Title: M68EM08JB8 Emulator Module (Reset and OSC)			
Size: B	Designed By: Kelvin Tse	Approved By: Edward Chui	Rev: B
Date: Tuesday, November 30, 1999	Sheet 8 of 9		



MOTOROLA, INC.			
Title: M68EM08JB8 Emulator Module (Target Head Connector)			
Size: B	Designed By: Kelvin Tse	Approved By: Edward Chui	Rev: B
Date: Tuesday, November 30, 1999	Sheet 9 of 9		

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