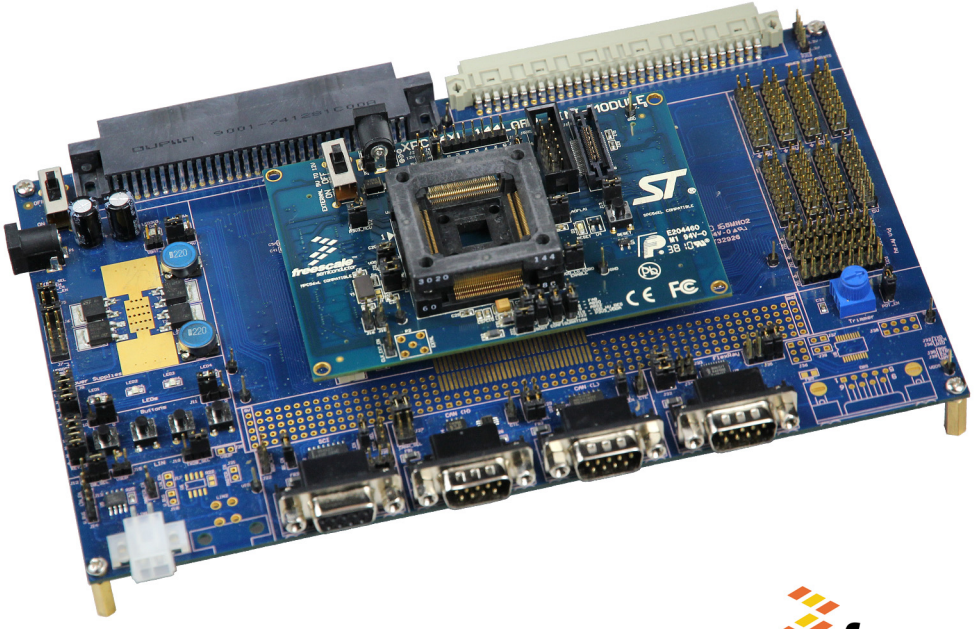
xPC564xL User Manual



XPC564xLEVBUM

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1 OVERVIEW

The xPC564L EVB is an evaluation system supporting Freescale MPC564xL microprocessors. The complete system consists of an xPC56XXMB Motherboard and an xPC564LADPT Mini-Module which plugs into the motherboard. Different Mini-Modules are available for evaluating devices with different footprints in the MPC564xL family of microprocessors. The evaluation system allows full access to the CPU, all of the CPU's I/O signals, and the motherboard peripherals (such as CAN, SCI, LIN). The Mini-Module may be used as a stand-alone unit, which allows access to the CPU, but no access to the I/O pins or any motherboard peripherals.

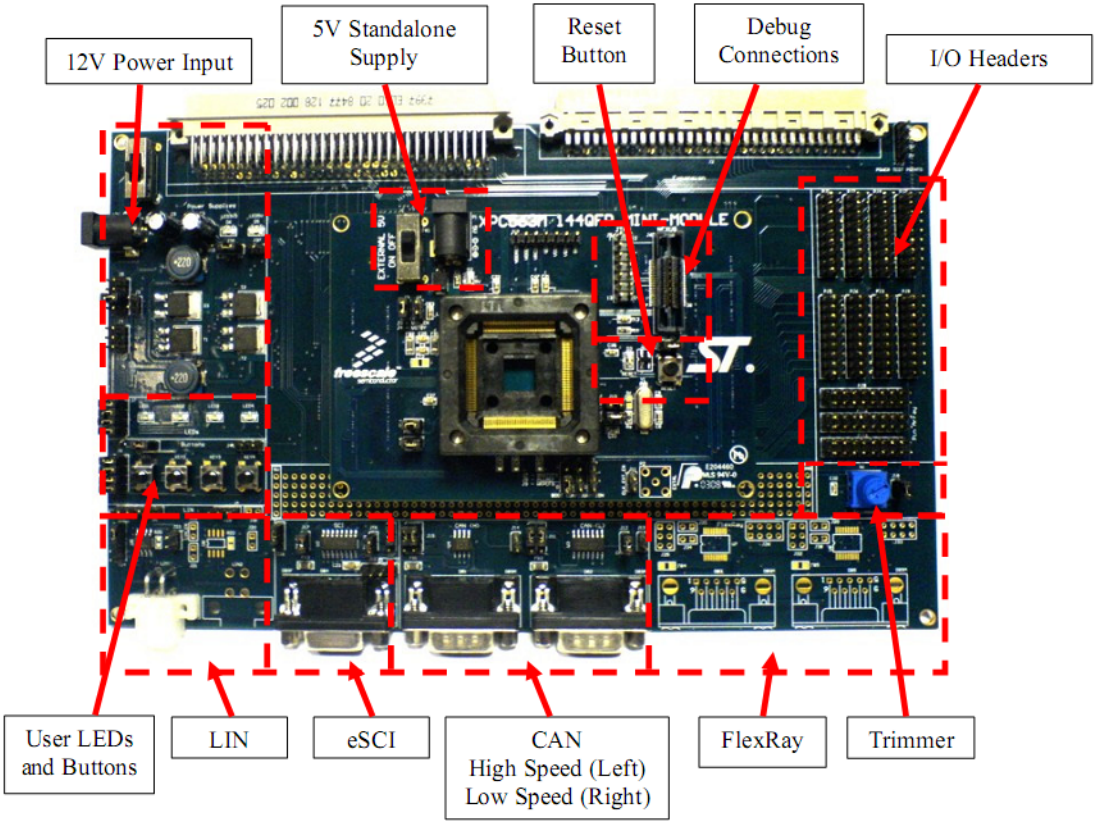


Figure 1-1: Overview of the xPC564L EVB

1.1 Package Contents

An xPC564L Evaluation Kit includes the following items:

- One xPC56XXMB Motherboard
- One One xPC564LADPT100S or xPC564LADPT144S or xPC564LADPT257S Mini-Module
- One xPC56XX Resources CD-ROM
- One P&E USB-ML-PPCNEXUS Hardware Interface Cable
- One USB A-to-B Cable
- Freescale Warranty Card

An xPC564L Adapter Package includes the following items:

- One xPC564LADPT144S Mini-Module
- One xPC56XX Resources CD-ROM
- Freescale Warranty Card

1.2 Supported Devices

The xPC564LADPT100S Mini-Module supports the following devices:

- MPC5643L (100LQFP Package)

The xPC564LADPT144S Mini-Module supports the following devices:

- MPC5643L (144LQFP Package)

The xPC564LADPT257S Mini-Module supports the following devices:

- MPC5643L (257BGA Package)

1.3 Recommended Materials

- Freescale MPC5643L Product Summary
- Freescale MPC5643L reference manual and datasheet
- xPC56XXMB schematic
- xPC564LADPT100S schematic
- xPC564LADPT144S schematic
- xPC564LADPT257S schematic

1.4 Handling Precautions

Please take care to handle the package contents in a manner such as to prevent electrostatic discharge.

2 HARDWARE FEATURES

The xPC564L EVB is an evaluation system for Freescale's MPC564xL microprocessors. A 38-pin Mictor Nexus port and/or a 14-pin JTAG port are provided on the Mini-Module to allow usage of an external PowerPC Nexus interface such as P&E USB-ML-PPCNEXUS cable and Cyclone MAX automated programmer.

2.1 xPC56XXMB Board Features

- ON/OFF Power Switch w/ LED indicators
- A 12VDC power supply input barrel connector
- Onboard STMicroelectronics L9758 regulator provides three different power voltages simultaneously: 5V, 3.3V, and 1.2V
- Onboard peripherals can be configured to operate at 5V or 3.3V logic levels
- Two CAN channels with jumper enables
  - One CAN channel with High-Speed transceiver and DB9 male connector
  - One CAN channel with Low-Speed Fault Tolerant and High-Speed transceiver (selectable with jumpers) and DB9 male connector
- Two LIN channels with jumper enables
  - One channel with transceiver and pin header connector populated
  - One channel with footprints only
- One SCI channel with jumper enables
  - Transceiver with DB9 female connector
- Two FlexRay channels with jumper enables

- One channel with transceiver and DB9 male connector
- One channel with footprint only

- Four user push buttons with jumper enables and polarity selection
- Four user LED's with jumper enables
- One potentiometer for analog voltage input
- Pin array for accessing all I/O signals
- Expansion connectors for accessing all I/O signals
- Development zone with 0.1" spacing and SOIC footprint prototyping
- Specifications:
  - Board Size 5.5" x 9.0"
  - 12VDC Center Positive power supply with 2.5/5.5mm barrel connector

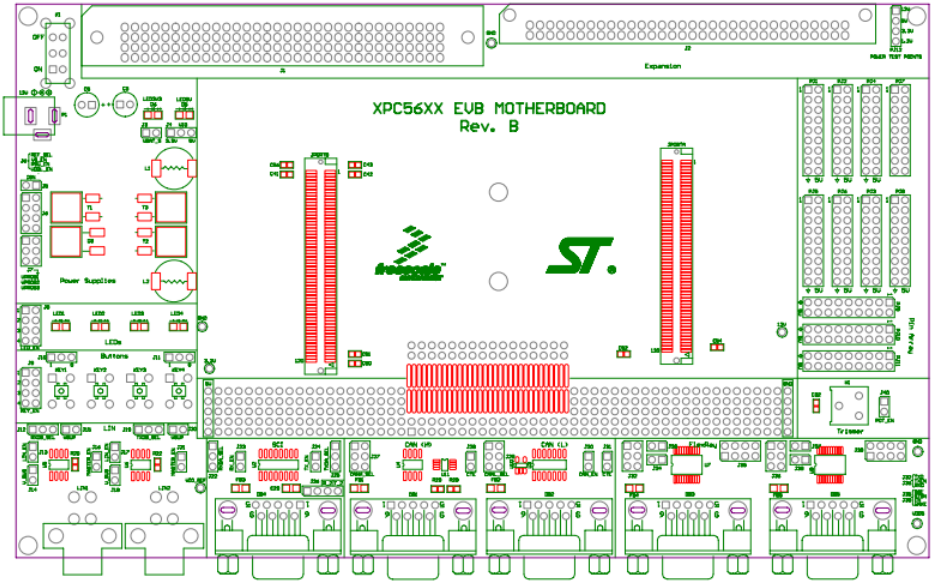


Figure 2-1: xPC56XXMB Top Component Placement

2.2 xPC564LADPT Mini-Module Board Features

- Can be used as a stand-alone board by providing external 5V power supply input
- ON/OFF Power Switch w/ LED indicator
- Reset button with filter and LED indicator
- xPC564LADPT144S has socket for MPC564xL in 144LQFP footprint
- xPC564LADPT100S has socket for MPC564xL in 100LQFP footprint
- xPC564LADPT257S has socket for MPC564xL in 257BGA footprint
- Debug ports: 38-pin Mictor Nexus port and/or 14-pin JTAG port
- Direct clock input through SMA connector (footprint only)
- Jumpers for boot configuration

2.3 Pin Numbering for Jumpers

Jumpers for both the xPC56XXMB motherboard and the xPC564L Mini-Modules have a rounded corner to indicate the position of pin 1. See examples below for the numbering convention used in this manual for jumper settings.

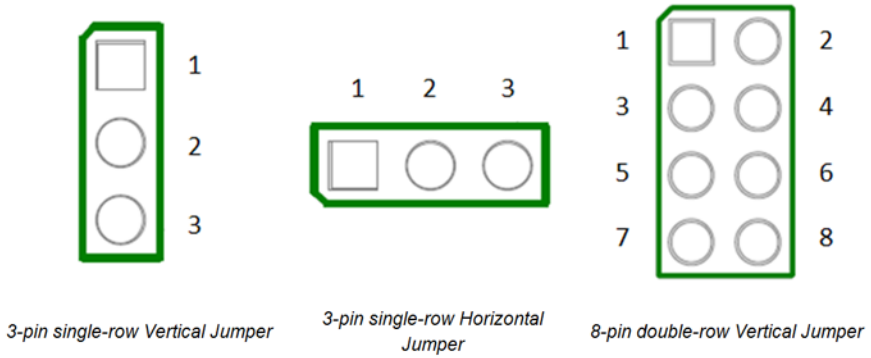


Figure 2-2: Pin Numbering

3 xPC56XXMB HARDWARE & JUMPER SETTINGS

Please note that this section of the manual is written for revision B and C of the xPC56XXMB motherboard. Revision B motherboards are indicated by the “Rev. B” silkscreen text in the center of the motherboard, and Revision C motherboards are indicated by the “Rev. C” silkscreen text in the center of the motherboard.

Revision A motherboards have different jumper numbers. These differences can be found in the table below:

Rev. A	Rev. B	Rev. C	Jumper Description
J3	J6, pins 1+2	-	VSA Tracking Regulator Configuration
-	-	J3	Slew Rate Select
J4	J7	J7	VPROG Regulators Control
J5 (pins 1+2)	J5	-	IGN Control
-	-	J5	Power Reset Pullup Voltage Select
J5, pins 3+4, 5+6, 7+8	J6, pins 3+4, 5+6, 7+8	-	Regulators Enable & Standby
-	-	J6	Power Reset Output Enable
J36	J4	J4	VIO Peripherals Logic Level
J37	J3	-	VBat low voltage detection
-	-	J41	Power Reset Pullup Enable
J7	J8	J8	LEDs Enable

J8	J9	J9	Buttons Enable
J9	J10	J10	Buttons Driving Configuration
J40	J11	J11	Buttons Idle Configuration
J22	J13	J13	LIN1 enable
J24	J14	J14	LIN1 VBUS configuration
J6	J15	J15	LIN1 VSUP configuration
J23	J16	J16	LIN1 master selection
J28	J22	J22	LIN1/SCI RxD selection
J27	J25	J25	LIN1/SCI TxD selection
J19	J17	J17	LIN2 enable
J21	J18	J18	LIN2 VBUS configuration
J31	J20	J20	LIN2 VSUP configuration
J20	J21	J21	LIN2 master selection
J30	J12	J12	LIN2/SCI RxD selection
J29	J19	J19	LIN2/SCI TxD selection
J17	J23	J23	SCI RxD Enable
J16	J24	J24	SCI TxD Enable
J27	J25	J25	LIN1/SCI TxD selection
J28	J22	J22	LIN1/SCI RxD selection
J14	J28	J28	CAN (H) Transmit Enable

J15	J27	J27	CAN (H) TxD/RxD Enable
J13	J31	J31	CAN (L) CTE
J12	J30	J30	CAN (L) Enable
J11	J29	J29	CAN (L) TxD/RxD Enable
J25	J32	J32	FlexRay Bus Driver 1 Enable
J26	J35	J35	FlexRay Bus Driver 1 Configuration
J34	J34	J34	FlexRay 1 Terminal Resistor Connection
J35	J33	J33	FlexRay 1 Terminal Resistor Connection
J32	J36	J36	FlexRay Bus Driver 2 Enable
J33	J39	J39	FlexRay Bus Driver 2 Configuration
J38	J38	J38	FlexRay 2 Terminal Resistor Connection
J39	J37	J37	FlexRay 2 Terminal Resistor Connection
J18	J40	J40	POT Enable

Table 3-1. Hardware and Jumper Settings

3.1 Power Supplies

The xPC56XXMB obtains its power from the 12VDC Center Positive input barrel connector. The following jumpers are used to configure the power supply output:

J3 – VBat low voltage detection (Revisions A & B only)

Jumper Setting	Effect

On	Low battery detection is enabled
Off (default)	Low battery detection is disabled

J3 – Slew Rate Select (Revision C only)

Jumper Setting	Effect
1+2	Regulator configured for fast slew rate
2+3	Regulator configured for slow slew rate
Off (default)	Regulator configured for medium slew rate

J4 – VIO Peripherals Logic Level

Jumper Setting	Effect
1+2	Onboard peripherals are configured for 3.3V logic
2+3 (default)	Onboard peripherals are configured for 5V logic

J5 – IGN Control (Revisions A & B only)

Jumper Setting	Effect
On (default)	The power regulator is always on
Off	If 5+6 is also OFF on J6, the power regulator is in standby

J5 – Power Reset Pullup Voltage Select (Revision C only)

Jumper Setting	Effect
1+2	If J41 is ON, regulator output reset is pulled up to 5V
2+3	If J41 is ON, regulator output reset is pulled up to 3.3V

J6 – Regulators Enable & Standby (Revisions A & B only)

Jumper Setting	Position	Effect
1+2	On	The ST L9758 tracking regulator VSA tracks the input voltage at its TRACK_REF pin.
	Off (default)	The ST L9758 tracking regulator VSA tracks 5V
3+4	On	VSB, VSC, and VSD tracking regulators are disabled
	Off (default)	VSB, VSC, and VSD tracking regulators are enabled
5+6	On (default)	The power regulator is always on
	Off	The power regulator is in standby if jumpers 1+2 are also in the “off” position
7+8	On	VDLL and VCORE regulators are disabled
	Off (default)	VDLL and VCORE regulators are enabled

J6 – Power Reset Output Enable (Revision C only)

Jumper Setting	Effect
On (default)	If regulator voltages fall below threshold, a reset is sent to the microprocessor
Off	No reset is sent to the microprocessor

J7 – VPROG Regulators Control (Revisions A & B)

Jumper Setting	Position	Effect
1+2	On	VKAM regulator output is programmed to 1V
	Off (default)	VKAM regulator output is programmed to 1.5V
3+4	On	VSTBY regulator output is programmed to 2.6V
	Off (default)	VSTBY regulator output is programmed to 3.3V
5+6	On	VDLL regulator output is programmed to 2.6V
	Off (default)	VDLL regulator output is programmed to 3.3V

J7 – VPROG Regulators Control (Revision C only)

Jumper 1+2	Jumper 3+4	Jumper 5+6	VDD3	VDDL	VKAM
Off	Off	Off	3.3 V	2.6 V	2.6 V

Off	Off	On	3.3 V	3.3 V	3.3 V
Off	On	Off	3.3 V	1.5 V	1.0 V
Off	On	On	3.3 V	3.3 V	1.0 V
On	Off	Off	3.3V standby	3.3 V	1.0 V
On	Off	On	2.0 V	3.15 V	5.0 V
On	On	Off	2.6 V standby	3.3 V	1.0 V
On	On	On	2.6 V standby	3.3 V	1.5 V

J37 – VBat low voltage detection

Jumper Setting	Effect
On	Low battery detection is enabled
Off (default)	Low battery detection is disabled

J41 – Power Reset Pullup Enable (Revision C only)

Jumper Setting	Effect
On	Regulator output reset is pulled up
Off (default)	Regulator output reset is not pulled up

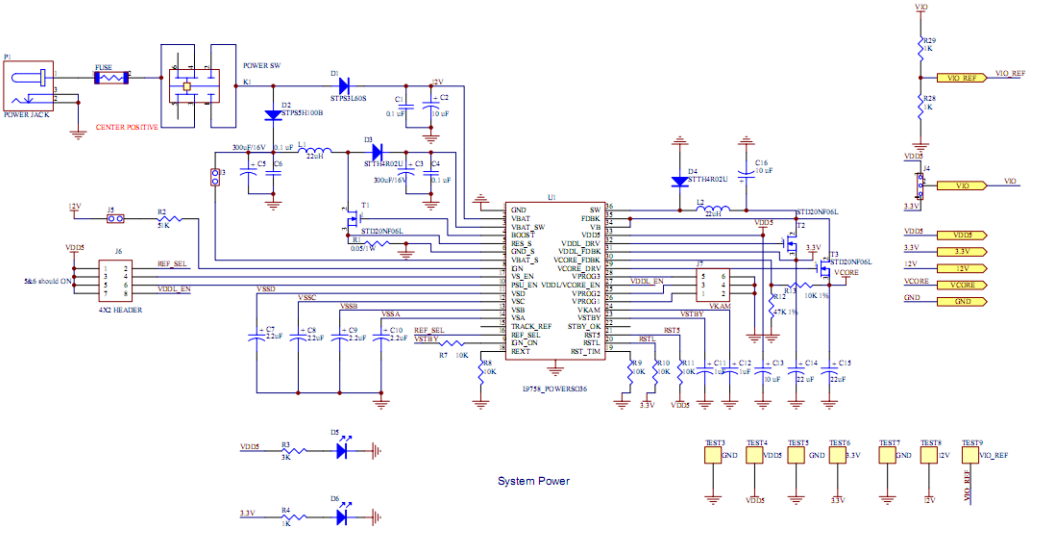


Figure 3-1: Power Supply circuitry schematic (Revisions A & B only)

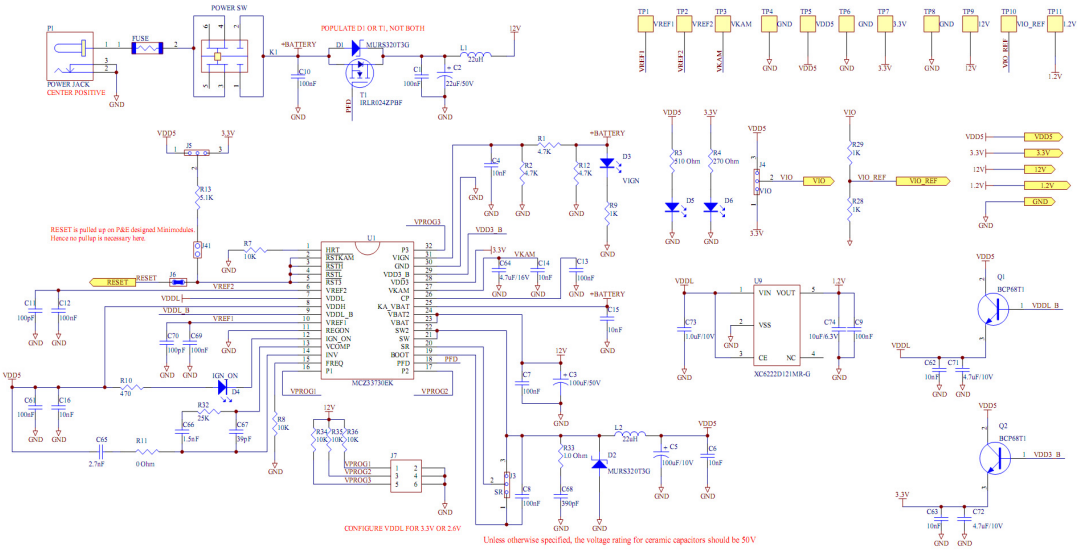


Figure 3-2: Power Supply circuitry schematic (Revision C)

3.2 LEDs

There are four user LEDs available on the xPC56XXMB. All LEDs are active low.

J8 – LEDs Enable

Controls whether the LEDs on the xPC56XXMB motherboard are connected to I/O pins of the processor. The jumpers can be removed and wires can be used to connect each LED to any processor I/O pin, if desired.

Jumper Setting	Effect
1+2 (default on)	LED1 connected to PD4
3+4 (default on)	LED2 connected to PD5
5+6 (default on)	LED3 connected to PD6
7+8 (default on)	LED4 connected to PD7

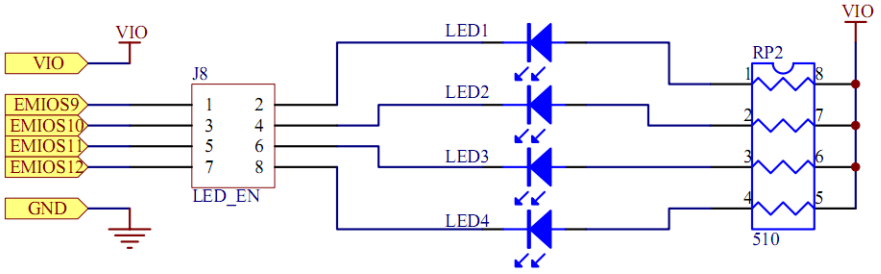


Figure 3-3: LEDs circuitry schematic

3.3 Buttons

There are four user buttons available on the xPC56XXMB.

J9 – Buttons Enable

Controls whether the buttons on the xPC56XXMB motherboard are connected to I/O pins of the processor. The jumpers can be removed and wires can be used to connect each button to any processor I/O pin, if desired.

Jumper Setting	Effect
1+2 (default on)	KEY1 connected to PD0
3+4 (default on)	KEY2 connected to PD1
5+6 (default on)	KEY3 connected to PD2
7+8 (default on)	KEY4 connected to PD3

J10 – Buttons Driving Configuration

Selects whether the buttons drive logic high or drive logic low when pressed.

Jumper Setting	Effect
1+2	When pressed, buttons will send logic high to the connected I/O pin
2+3 (default)	When pressed, buttons will send logic low to the connected I/O pin

J11 – Buttons Idle Configuration

Selects whether the I/O pins are pulled logic high or pulled logic low. This controls the default logic level of the I/O pins when the buttons are not pressed.

Jumper Setting	Effect
1+2 (default)	I/O pins connected to the buttons are pulled up to logic high
2+3	I/O pins connected to the buttons are pulled down to logic low

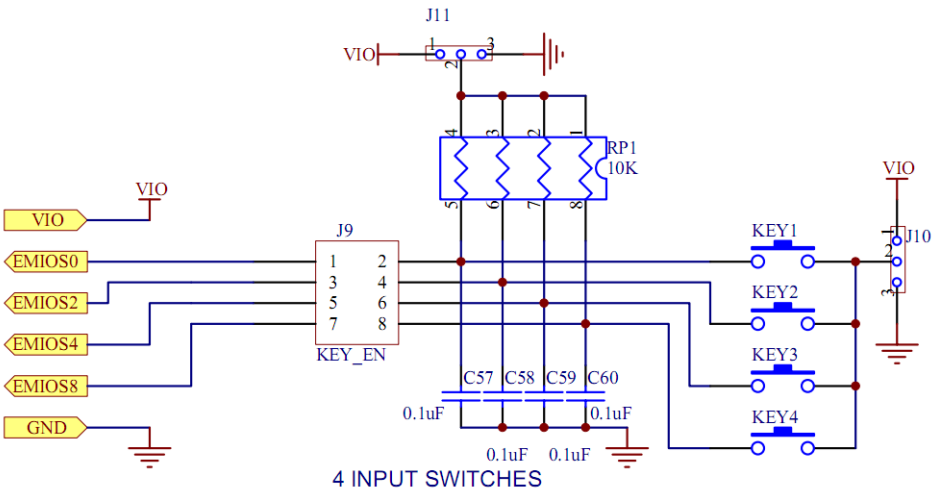


Figure 3-4: Buttons circuitry schematic

3.4 LIN

There are footprints for two LIN connections on the xPC56XXMB. By default,

one LIN circuit is assembled (LIN1) and the other circuit is left unpopulated (LIN2).

J13 – LIN1 enable

Jumper Setting	Effect
On	Enables the LIN1 transceiver
Off (default)	Disables the LIN1 transceiver

J14 – LIN1 VBUS configuration

Jumper Setting	Effect
On	LIN1 VBUS is connected to 12V
Off (default)	LIN1 VBUS is not connected to 12V

J15 – LIN1 VSUP configuration

Jumper Setting	Effect
On	LIN1 VSUP is connected to 12V
Off (default)	LIN1 VSUP is not connected to 12V

J16 – LIN1 master selection

Jumper Setting	Effect
On	LIN1 is configured as a master node
Off (default)	LIN1 is configured as a slave node

J22 – LIN1/SCI RxD selection

Controls whether the RxD pin on LIN1 or SCI is connected to the default I/O pin on the MPC564xL processor.

Jumper Setting	Effect
1+2	The LIN1 RxD pin is connected to the PB3 pin on the MPC564xL processor. This should be set if enabling LIN1.
2+3	The SCI RxD pin is connected to the PB3 pin on the MPC564xL processor.

J25 – LIN1/SCI TxD selection

Controls whether the TxD pin on LIN1 or SCI is connected to the default I/O pin on the MPC564xL processor.

Jumper Setting	Effect
1+2	The LIN1 TxD pin is connected to the PB2 pin on the MPC564xL processor. This should be set if enabling LIN1.

2+3	The SCI TxD pin is connected to the PB2 pin on the MPC564xL processor.

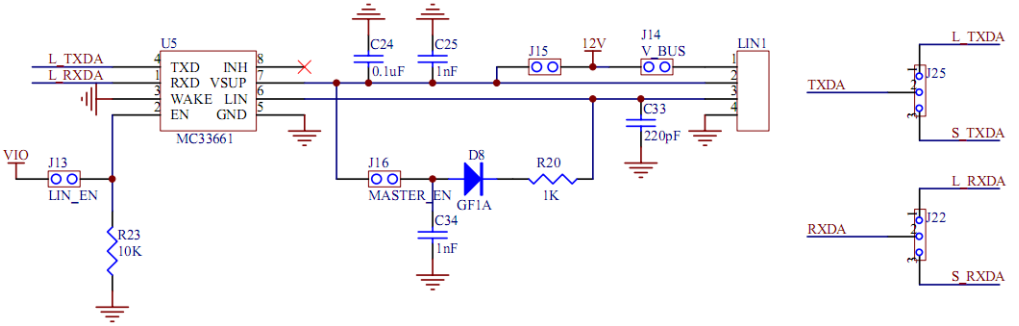


Figure 3-5: LIN1 Schematic

J17 – LIN2 enable

Jumper Setting	Effect
On	Enables the LIN2 transceiver
Off (default)	Disables the LIN2 transceiver

J18 – LIN2 VBUS configuration

Jumper Setting	Effect
On	LIN2 VBUS is connected to 12V
Off (default)	LIN2 VBUS is not connected to 12V

J20 – LIN2 VSUP configuration

Jumper Setting	Effect
On	LIN2 VSUP is connected to 12V
Off (default)	LIN2 VSUP is not connected to 12V

J21 – LIN2 master selection

Jumper Setting	Effect
On	LIN2 is configured as a master node
Off (default)	LIN2 is configured as a slave node

J12 – LIN2/SCI RxD selection

Controls whether the RxD pin on LIN2 or SCI is connected to the default I/O pin on the MPC564xL processor.

Jumper Setting	Effect
1+2	The LIN2 RxD pin is connected to the PF15 pin on the MPC564xL processor. This should be set if enabling LIN2.
2+3 (default)	The SCI RxD pin is connected to the PF15 pin on the MPC564xL processor.

J19 – LIN2/SCI TxD selection

Controls whether the TxD pin on LIN2 or SCI is connected to the default I/O

pin on the MPC564xL processor.

Jumper Setting	Effect
1+2	The LIN2 TxD pin is connected to the PF14 pin on the MPC564xL processor. This should be set if enabling LIN2.
2+3 (default)	The SCI TxD pin is connected to the PF14 pin on the MPC564xL processor.

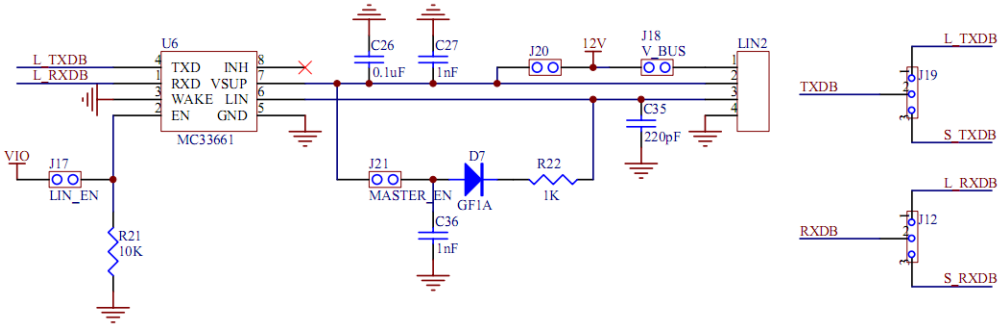


Figure 3-6: LIN2 schematic (Not populated by default)

3.5 SCI

One SCI interface is available on the xPC56XXMB.

J23 – SCI RxD Enable

Jumper Setting	Effect

On (default)	Enables SCI receive
Off	Disables SCI receive

J24 – SCI TxD Enable

Jumper Setting	Effect
On (default)	Enables SCI transmit
Off	Disables SCI transmit

J25 – LIN1/SCI TxD selection

Controls whether the TxD pin on LIN1 or SCI is connected to the default I/O pin on the MPC564xL processor.

Jumper Setting	Effect
1+2	The LIN1 TxD pin is connected to the PB2 pin on the MPC564xL processor.
2+3	The SCI TxD pin is connected to the PB2 pin on the MPC564xL processor. This should be set if enabling SCI.

J22 – LIN1/SCI RxD selection

Controls whether the RxD pin on LIN1 or SCI is connected to the default I/O

pin on the MPC564xL processor.

Jumper Setting	Effect
1+2	The LIN1 RxD pin is connected to the PB3 pin on the MPC564xL processor.
2+3	The SCI RxD pin is connected to the PB3 pin on the MPC564xLPC564xL processor. This should be set if enabling SCI.

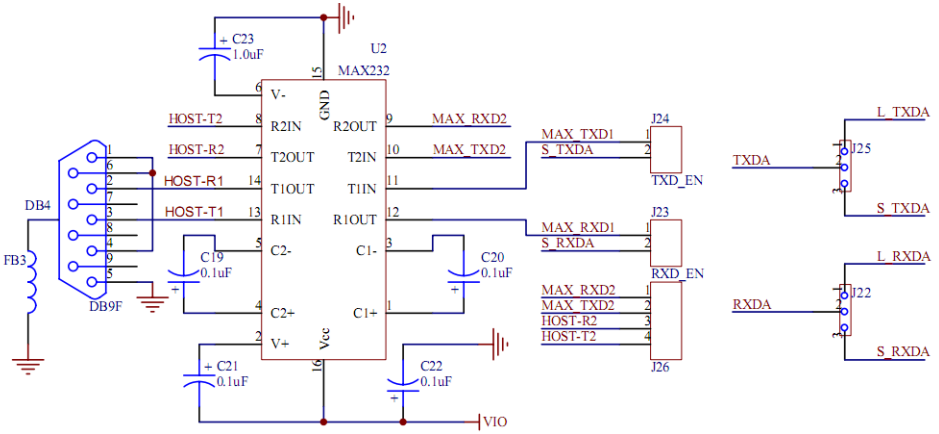


Figure 3-7: SCI schematic

3.6 CAN

Two CAN interfaces are implemented on the xPC56XXMB: a high-speed CAN interface and a low-speed CAN interface.

J28– CAN (H) Transmit Enable

Jumper Setting	Effect
On	Enables CAN transmission
Off (default)	Disables CAN transmission

J27 – CAN (H) TxD/RxD Enable

Controls which I/O pins on the MPC564xL processor are connected to the TxD and RxD pins on CAN (H). If CAN (H) is not used, it is recommended that all jumpers are removed.

Jumper Setting	Effect
1+3 (default)	The RxD pin of the CAN (H) interface is connected to the PB1 pin of the MPC564xL processor.
3+5	The RxD pin of the CAN (H) interface is connected to the PA15 pin of the MPC564xL processor.
2+4 (default)	The TxD pin of the CAN (H) interface is connected to the PB0 pin of the MPC564xL processor.
4+6	The TxD pin of the CAN (H) interface is connected to the PA14 pin of the MPC564xL processor.

J30 – CAN (L) Enable

Jumper Setting	Effect

On (default)	Enables CAN (L) transceiver
Off	Disables CAN (L) transceiver

J31 – CAN (L) CTE

Jumper Setting	Effect
On	Enables CAN transmission
Off (default)	Disables CAN transmission

J29 – CAN (L) TxD/RxD Enable

Controls which I/O pins on the MPC564xL processor are connected to the TxD and RxD pins on CAN (L). If CAN (L) is not used, it is recommended that all jumpers are removed.

Jumper Setting	Effect
1+3	The RxD pin of the CAN (L) interface is connected to the PB1 pin of the MPC564xL processor.
3+5 (default)	The RxD pin of the CAN (L) interface is connected to the PA15 pin of the MPC564xL processor.
2+4	The TxD pin of the CAN (L) interface is connected to the PB0 pin of the MPC564xL processor.
4+6 (default)	The TxD pin of the CAN (L) interface is connected to the PA14 pin of the MPC564xL processor.

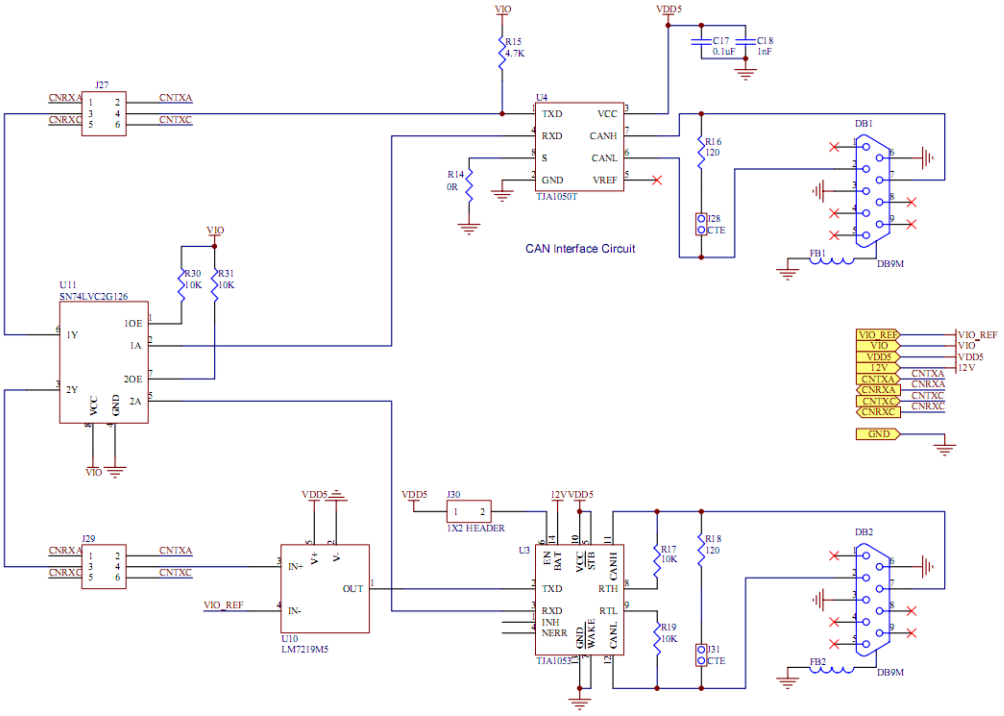


Figure 3-8: CAN schematic

3.7 FlexRay

The xPC56XXMB has footprints for two FlexRay interfaces. However, only one circuit is assembled by default. The FlexRay circuit comprises of two DB9 connectors. DB3 contains signals for both FlexRay channels and is compatible with major FlexRay tools. DB5 contains channel B signal, thereby also allowing 2 separate FlexRay connectors for channel A and channel B operation.

J32 – FlexRay Bus Driver 1 Enable

Controls whether the TxD, TxEN, RxD pins on FlexRay channel A is

connected to the default I/O pin on the MPC564xL processor.

Jumper Setting	Effect
1+2	The TxD pin of the FlexRay Channel A interface is connected to the PD0 pin of the MPC564xL processor.
3+4	The TxEN pin of the FlexRay Channel A interface is connected to the PC15 pin of the MPC564xL processor.
5+6	The RxD pin of the FlexRay Channel A interface is connected to the PD1 pin of the MPC564xL processor.

J35 – FlexRay Bus Driver 1 Configuration

Controls configuration pins on the FlexRay Bus Driver.

Jumper Setting	Effect
1+2	The BGE pin on the FlexRay Bus Driver is pulled up to 5V
3+4	The STBN pin on the FlexRay Bus Driver is pulled up to 5V
5+6 (default on)	The EN pin on the FlexRay Bus Driver is pulled up to 5V
7+8 (default on)	The WAKE pin on the FlexRay Bus Driver is pulled down to GND

J33 & J34 FlexRay 1 Terminal Resistor Connection

Jumper Setting	Effect
On	Terminal resistors connected
Off (default)	Terminal resistors not connected

J36 – FlexRay Bus Driver 2 Enable

Controls whether the TxD, TxEN, RxD pins on FlexRay channel B is connected to the default I/O pin on the MPC564xL processor.

Jumper Setting	Effect
1+2	The TxD pin of the FlexRay Channel A interface is connected to the PD3 pin of the MPC564xL processor.
3+4	The TxEN pin of the FlexRay Channel A interface is connected to the PD4 pin of the MPC564xL processor.
5+6	The RxD pin of the FlexRay Channel A interface is connected to the PD2 pin of the MPC564xL processor.

J39 – FlexRay Bus Driver 2 Configuration

Controls configuration pins on the FlexRay Bus Driver.

Jumper Setting	Effect
1+2	The BGE pin on the FlexRay Bus Driver is pulled up to 5V

3+4	The STBN pin on the FlexRay Bus Driver is pulled up to 5V
5+6	The EN pin on the FlexRay Bus Driver is pulled up to 5V
7+8	The WAKE pin on the FlexRay Bus Driver is pulled down to GND

J37 & J38 – FlexRay 2 Terminal Resistor Connection

Jumper Setting	Effect
On	Terminal resistors connected
Off (default)	Terminal resistors not connected

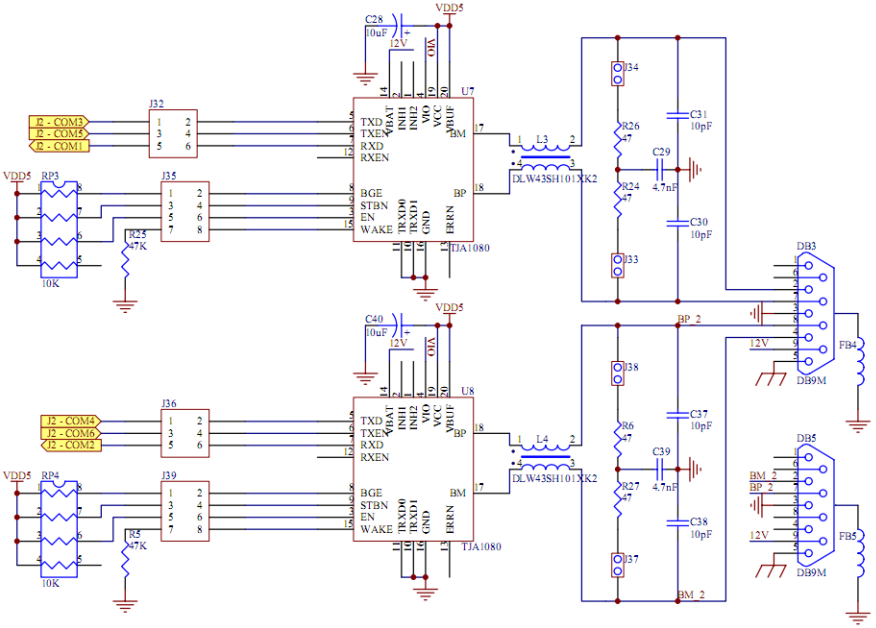


Figure 3-9: FlexRay Schematic

3.8 Potentiometer

A potentiometer is available on the xPC56XXMB to allow an analog voltage input.

J40 – POT Enable

Jumper Setting	Effect
On	The potentiometer wiper terminal is connected to the PE0 pin on the MPC564xL processor.
Off (default)	The potentiometer wiper terminal is left disconnected.

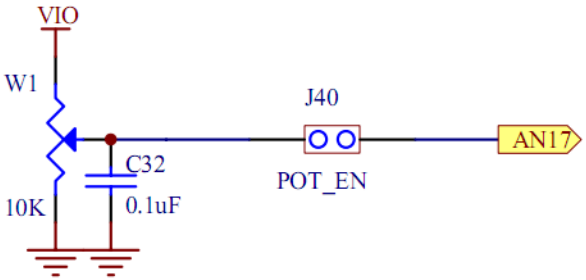
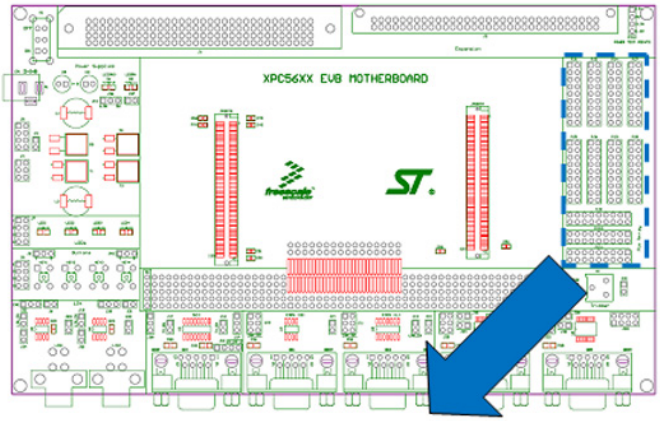


Figure 3-10: Potentiometer schematic

3.9 Pin Mapping

The following is the xPC564L EVB pin assignment for the Pin Array headers:



PJ1

RESET_MB	RESET_CPU
PB1	PA15
PB0	PA14
PC7	PC6
PC5	PC4
PE15	PD6
PB3	PB2
PF15	PF14
GND	5V

PJ2

PA4	PA2
PA3	NMI
X	X
PD5	X
FCCU F(0)	FCCU F(1)
PD1	PD2
PD0	PD3
PC15	PD4
GND	5V

PJ4 - Nexus

PF7	PF10
PF9	PF11
PF8	PB4
MDO0	PB5
PF6	TCKOUT
PF5	TMS
PF4	PI0
PI1	PI2
GND	5V

PJ7 - Port B[0:16]

PB0	PB1
PB2	PB3
PB4	PB5
PB6	PB7
PB8	PB9
PB10	PB11
PB12	PB13
PB14	PB15
X	X

PJ5 - Port E

PE0	PI3
PE2	X
PE4	PE5
PE6	PE7
X	PE9
PE10	PE11
PE12	PE13
PE14	PE15
GND	5V

PJ6 - Port F

PF0	X
X	PF3
PF4	PF5
PF6	PF7
PF8	PF9
PF10	PF11
PF12	PF13
PF14	PF15
GND	5V

PJ3 - Port C

PC0	PC1
PC2	PC3
PC4	PC5
PC6	PC7
X	X
PC10	PC11
PC12	PC13
PC14	PC15
GND	5V

PJ8 - Port D

PD0	PD1
PD2	PD3
PD4	PD5
PD6	PD7
PD8	PD9
PD10	PD12
PD11	X
PD14	X
GND	5V

PJ9 - Port A

GND	PA14	PD12	PA10	PA8	PA6	PA4	PA2	PA0
5V	PA15	PA13	PA11	PA9	PA7	PA5	PA3	PA1

PJ10 - Port G

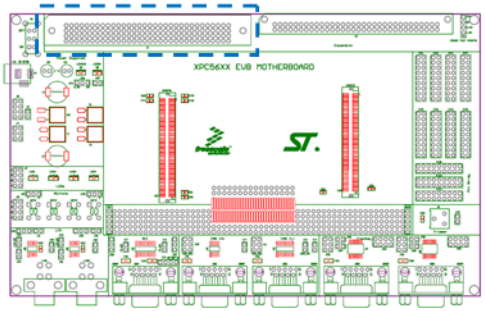
GND	PG14	PG12	PG10	PG8	PG6	PG4	PG2	FCCU (F0)
5V	PG15	PG13	PG11	PG9	PG7	PG5	PG3	FCCU (F1)

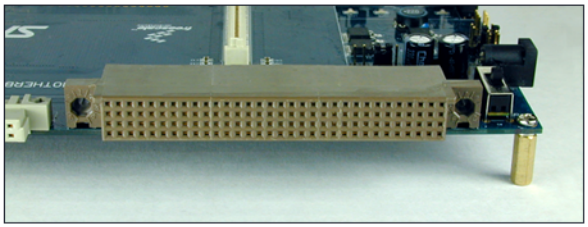
PJ11 - Port H

GND	PH14	PH12	PH10	PH8	PH6	PH4	PH2	PH0
5V	PH15	PH13	PH11	PH9	PH7	PH5	PH3	PH1

Figure 3-11: Pin Mapping

3.10 Expansion Port Pin Mapping – DIN41612 (4x32)



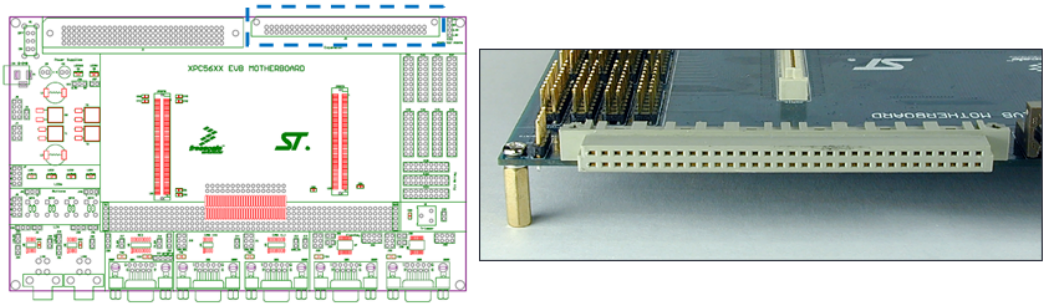


D32	D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1
C32	C31	C30	C29	C28	C27	C26	C25	C24	C23	C22	C21	C20	C19	C18	C17	C16	C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1
B32	B31	B30	B29	B28	B27	B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
A32	A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1

A1	GND	B1	GND	C1	GND	D1	GND
A2	PB1	B2	PA15	C2	PB0	D2	PA14
A3	PB3	B3	PB2	C3	PF15	D3	PF14
A4	PD1	B4	PD2	C4	PD3	D4	PD6
A5	PD3	B5	PC15	C5	PD4	D5	PE15
A6	PC7	B6	PC6	C6	PC5	D6	PC4
A7	PD5	B7	X	C7	FCCU F(0)	D7	FCCU F(1)
A8	PA4	B8	PA2	C8	GND	D8	12V
A9	RESET_MB	B9	RESET_CPU	C9	X	D9	X
A10	PA3	B10	NMI	C10	PH12	D10	PH13
A11	X	B11	X	C11	PH14	D11	PH15
A12	PC0	B12	PC1	C12	X	D12	X
A13	PC2	B13	X	C13	PC10	D13	PC11
A14	PC4	B14	PC5	C14	PC12	D14	PC13
A15	PC6	B15	PC7	C15	PC14	D15	PC15
A16	PA0	B16	PA1	C16	FCCU F(0)	D16	FCCU F(1)
A17	PA2	B17	PA3	C17	PG2	D17	PG3
A18	PA4	B18	PA5	C18	PG4	D18	PG5
A19	PA6	B19	PA7	C19	PG6	D19	PG7
A20	PA8	B20	PA9	C20	PG8	D20	PG9
A21	PA10	B21	PA11	C21	PG10	D21	PG11
A22	PA12	B22	PA13	C22	PG12	D22	PG13
A23	PA14	B23	PA15	C23	PG14	D23	PG15
A24	PB7	B24	PB8	C24	PD0	D24	PD1
A25	PC1	B25	PC2	C25	PD2	D25	PD3
A26	PE1	B26	PE2	C26	PD4	D26	PD5
A27	PE3	B27	PB13	C27	PD6	D27	PD7
A28	PB14	B28	PB15	C28	PD8	D28	PD9
A29	PC0	B29	PD15	C29	PD10	D29	PD12
A30	PE0	B30	PE8	C30	PD11	D30	X
A31	PB9	B31	PB10	C31	PD14	D31	X
A32	GND	B32	3.3V	C32	GND	D32	5V

Figure 3-12: Expansion Port Pin Mapping – DIN41612 (4x32)

3.11 Expansion Port Pin Mapping – DIN41612 (2x32)



A1	GND	B1	5V
A2	PB0	B2	PB1
A3	PB2	B3	PB3
A4	PB4	B4	PB5
A5	PB6	B5	PB7
A6	PB8	B6	PB9
A7	PB10	B7	PB11
A8	PB12	B8	PB13
A9	PB14	B9	PB15
A10	PE0	B10	PI3
A11	PE2	B11	X
A12	PE5	B12	PE4
A13	PE6	B13	PE7
A14	X	B14	PE9
A15	PE10	B15	PE11
A16	PE12	B16	PE13
A17	PE14	B17	PE15
A18	PF0	B18	X
A19	X	B19	PF3
A20	PF4	B20	PF5
A21	PF6	B21	PF7
A22	PF8	B22	PF9
A23	PF10	B23	PF11
A24	PF12	B24	PF13
A25	PF14	B25	PF15
A26	PH0	B26	PH1
A27	PH2	B27	PH3
A28	PH4	B28	PH5
A29	PH6	B29	PH7
A30	PH8	B30	PH9
A31	PH10	B31	PH11
A32	GND	B32	3.3V

Figure 3-13: Expansion Port Pin Mapping – DIN41612 (2x32)

4 xPC564LADPT HARDWARE & JUMPER SETTINGS

This chapter covers the hardware a jumper settings for the xPC564LADPT100S, xPC564LADPT144S, and xPC564LADPT257S mini-modules.

4.1 Boot Configuration

The following jumpers affect the operation of the processor as it initially comes out of the reset state:

J7 – FAB Configuration

Controls whether the FAB (force alternate boot mode) pin is set to boot in serial boot or internal boot mode.

Jumper Setting	Effect
1+2 (default)	The MPC564xL processor uses internal boot mode
2+3	The MPC564xL processor uses serial boot mode

J8 – ABS0 Configuration

Controls whether the processor boots from CAN or SCI serial interfaces when the FAB pin (J7) is set to serial boot.

Jumper Setting	Effect
1+2 (default)	The MPC564xL processor uses SCI boot mode
2+3	The MPC564xL processor uses CAN boot mode

J9 – ABS2 Configuration

Controls the status of the ABS2 pin

Jumper Setting	Effect
1+2 (default)	The ABS2 pin on the processor is pulled down
2+3	The ABS2 pin on the processor is pulled up

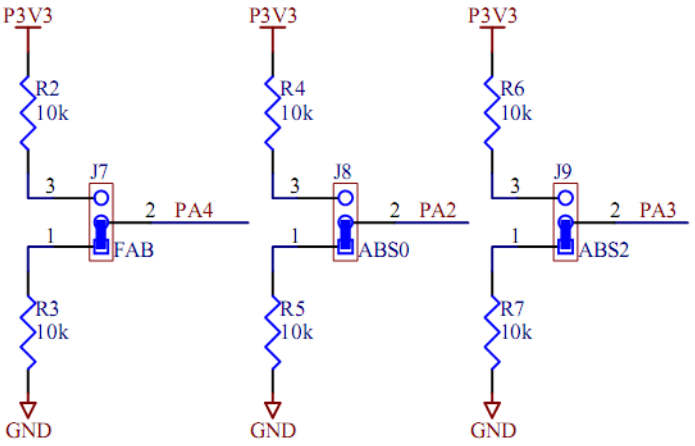


Figure 4-1: Boot Configuration Jumpers

4.2 Power Configuration

When the xPC564L Mini-Module is plugged into the xPC56XXMB motherboard, power is supplied directly by the motherboard. In this setup, the external power supply input available on the Mini-Module should NOT be used.

When the xPC564L Mini-Module is used as a stand-alone board, an external 5V-12V power supply must be used.

The following jumpers affect the power supply pins of the MPC564xL processor:

J4 – VDDARef Configuration

Controls whether the ADC0 and ADC1 high reference voltage is set to 3.3V or 5V.

Jumper Setting	Effect
1+2 (default)	The ADC high reference voltage is set to 3.3V
2+3	The ADC high reference voltage is set to 5V

J14 – I/O Supply Input Enable

Controls whether power is provided to the “I/O Supply Input” pins on the MPC564xL processor.

Jumper Setting	Effect
On (default)	MPC564xL I/O Supply Input pins are connected to 3.3V
Off	MPC564xL I/O Supply Input pins are unpowered

J15 – Voltage Regulator Supply Low Voltage Enable

Controls whether power is provided to the “Voltage Regulator Supply Low Voltage” pins on the MPC564xL processor, if you remove this jumper, connect CT6 to provide power from the motherboard.

Jumper Setting	Effect
On (default)	MPC564xL Voltage Regulator Supply Low Voltage pins are powered with 1.2V

Off	MPC564xL Voltage Regulator Supply Low Voltage pins are unpowered by the Mini-Module

J17 – Debug Ports Power Configuration

Controls whether the power pins on the debug ports (VDDE7 on the 14-pin JTAG port and VREF on the 28-pin Mictor port) are connected to 3.3V or 5V.

Jumper Setting	Effect
1+2 (default)	The power pins on the debug ports are connected to 3.3V
2+3	The power pins on the debug ports are connected to 5V

J19 – Voltage Regulator Supply High Voltage Configuration

Controls whether power is provided to the “Voltage Regulator Supply High Voltage” pins on the MPC564xL processor.

Jumper Setting	Effect
On (default)	MPC564xL Voltage Regulator Supply High Voltage pins are powered with 3.3V
Off	MPC564xL Voltage Regulator Supply High Voltage pins are unpowered

J20 – VDD_HV_FLA Configuration

Controls whether power is provided to the VDD_HV_FLA0 and

VDD_HV_FLA1 pins on the MPC564xL processor.

Jumper Setting	Effect
On (default)	The VDD_HV_FLA pins on the MPC564xL are powered with 3.3V
Off	The VDD_HV_FLA pins on the MPC564xL are unpowered

J21 – Crystal Oscillator Amplifier Supply Configuration

Controls whether power is provided to the Crystal Oscillator Amplifier on the MPC564xL processor.

Jumper Setting	Effect
On (default)	The Crystal Oscillator Amplifier pins on the MPC564xL are powered
Off	The Crystal Oscillator Amplifier pins on the MPC564xL are unpowered

J22 – VDDA Configuration

Controls whether power is provided to the VDDA pins on the MPC564xL processor.

Jumper Setting	Effect
On (default)	The VDDA pins on the MPC564xL processor are connected to 3.3V

Off	The VDDA pins on the MPC564xL processor are unpowered

CT6 – 1.2V Power Generation

Controls whether the 1.2V power supply is generated from the NPN transistor or supplied directly from the xPC56XXMB motherboard.

Jumper Setting	Effect
Connected	1.2V power is provided directly by the xPC56XXMB motherboard
Disconnected (default)	1.2V power is generated by the NPN transistor circuit on the xPC564L Mini-Module

CT8 – Mictor VEN_IO2 Configuration

Controls whether the VEN_IO2 pin on the 38-pin Mictor port is connected to the PA4 pin on the MPC564xL processor.

Jumper Setting	Effect
Connected	The VEN_IO2 pin is connected to PA4
Disconnected (default)	The VEN_IO2 pin is left disconnected

4.3 System Clock Configuration

The xPC564L Mini-Modules support the usage of crystal clock sources as

well as external clock sources.

J10 – Crystal clock source enable

Both of the jumpers below need to be installed to enable the crystal clock source.

Jumper Setting	Effect
1+2 (default)	The MPC564xL “EXTAL” signal is connected to the crystal clock source on the xPC564L Mini-Module
3+4 (default)	The MPC564xL “XTAL” signal is connected to the crystal clock source on the xPC564L Mini-Module

J11 – External clock source enable

The xPC564L Mini-Module contains a footprint for an SMA connector, which can be used to provide an external clock source to the system.

Jumper Setting	Effect
On	The MPC564xL “EXTAL” signal is connected to the SMA connector on the xPC564L Mini-Module
Off (default)	The SMA connector on the xPC564L Mini-Module is disconnected from the processor

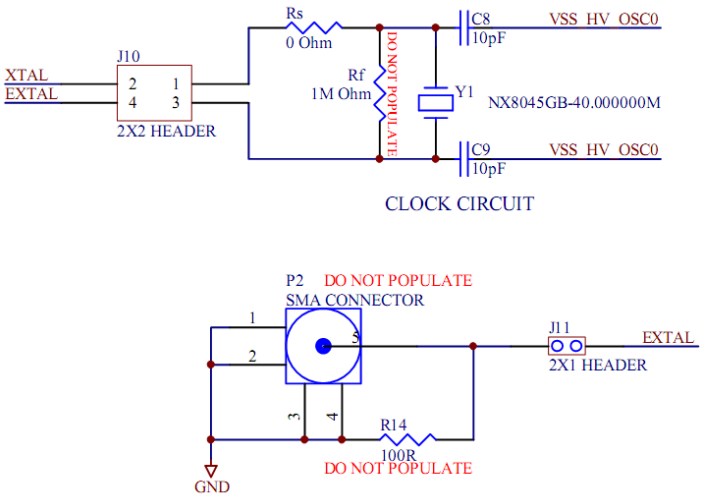


Figure 4-2: System Clock schematic

4.4 General Configuration

J13 – Reset Enable

A RESET push button on the xPC564L Mini-Module can be used to reset the processor.

Jumper Setting	Effect
On (default)	The RESET button on the xPC564L Mini-Module is enabled
Off	The RESET button on the xPC564L Mini-Module is disabled

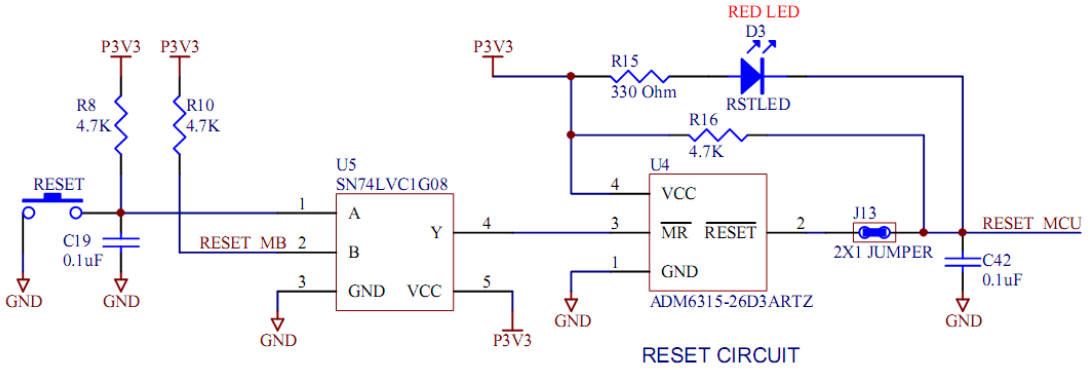


Figure 4-3: Reset circuitry schematic

J16/J18 – Fault Collection and Control Unit Connection

Two pins on the MPC564xL processor, FCCU_F0 (connected to J16) and FCCU_F1 (connected to J18), can be connected to the xPC56XXMB motherboard.

Jumper Setting	Effect
On (default)	The corresponding FCCU pin on the MPC564xL processor is connected to the xPC56XXMB motherboard
Off	The corresponding FCCU pin on the MPC564xL processor is not connected to the xPC56XXMBmotherboard

5 DEBUGGING/PROGRAMMING xPC564L EVB

P&E provides hardware and software tools for debugging and programming the xPC564L EVB system.

P&E's USB-ML-PPCNEXUS and Cyclone MAX offer two effective hardware solutions, depending on your needs. The USB-ML-PPCNEXUS is a development tool that will enable you to debug your code and program it onto your target. The Cyclone MAX is a more versatile and robust development tool with advanced features and production programming capabilities, as well as Ethernet support.

More information is available below to assist you in choosing the appropriate development tool for your needs.

5.1 Hardware Solutions At A Glance

The USB-ML-PPCNEXUS offers an affordable and compact solution for your development needs, and allows debugging and programming to be accomplished simply and efficiently. Those doing rapid development will find the USB-ML-PPCNEXUS easy to use and fully capable of fast-paced debugging and programming.

The Cyclone MAX is a more complete solution designed for both development and production. The Cyclone MAX features multiple communications interfaces (including USB, Ethernet, and Serial), stand-alone programming functionality, high speed data transfer, a status LCD, and many other advanced capabilities.

Below is an overview of the features and intended use of the USB-ML-PPCNEXUS and Cyclone MAX.

5.1.1 USB-ML-PPCNEXUS Key Features

- Programming and debugging capabilities
- Compact and lightweight
- Communication via USB 2.0
- Supported by P&E software and Freescale's CodeWarrior

5.1.2 Cyclone MAX Key Features

- Advanced programming and debugging capabilities, including:

- PC-Controlled and User-Controlled Stand-Alone Operation
- Interactive Programming via Host PC
- In-Circuit Debugging, Programming, and Testing

- Compatible with Freescale's ColdFireV2/3/4, PowerPC 5xx/8xx/55xx/56xx, and ARM7 microcontroller families
- Communication via USB, Serial, and Ethernet Ports
- Multiple image storage
- LCD screen menu interface
- Supported by P&E software and Freescale's CodeWarrior

5.2 Working With P&E's USB-ML-PPCNEXUS

Figure 5-1: P&E's USB-ML-PPCNEXUS

5.2.1 Product Features & Implementation

P&E's USB-ML-PPCNEXUS Interface (USB-ML-PPCNEXUS) connects your target to your PC and allows the PC access to the debug mode on Freescale's PowerPC 5xx/8xx/55xx/56xx microcontrollers. It connects between a USB port on a Windows 2000/XP/2003/Vista machine and a standard 14-pin JTAG/Nexus connector on the target.

By using the USB-ML-PPCNEXUS Interface, the user can take advantage of the background debug mode to halt normal processor execution and use a PC to control the processor. The user can then directly control the target's execution, read/write registers and memory values, debug code on the processor, and program internal or external FLASH memory devices. The USB-ML-PPCNEXUS enables you to debug, program, and test your code on your board.

5.2.2 Software

The USB-ML-PPCNEXUS Interface works with Codewarrior as well as P&E's in-circuit debugger and flash programmer to allow debug and flash programming of the target processor. P&E's USB-ML-PPCNEXUS Development Packages come with the USB-ML-PPCNEXUS Interface, as well as flash programming software, in-circuit debugging software, Windows IDE, and register file editor.

5.3 Working With P&E's Cyclone MAX

Figure 5-2: P&E's Cyclone MAX

5.3.1 Product Features & Implementation

P&E's Cyclone MAX is an extremely flexible tool designed for debugging, testing, and in-circuit flash programming of Freescale's ColdFireV2/3/4, PowerPC 5xx/8xx/55xx/56xx, and ARM7 microcontrollers. The Cyclone MAX connects your target to the PC via USB, Ethernet, or Serial Port and enables you to debug your code, program, and test it on your board. After development is complete the Cyclone MAX can be used as a production tool on your manufacturing floor.

For production, the Cyclone MAX may be operated interactively via Windows-based programming applications as well as under batch or .dll commands from a PC. Once loaded with data by a PC it can be disconnected and operated manually in a stand-alone mode via the LCD menu and control buttons. The Cyclone MAX has over 3Mbytes of non-volatile memory, which allows the on-board storage of multiple programming images. When connected to a PC for programming or loading it can communicate via the ethernet, USB, or serial interfaces.

5.3.2 Software

The Cyclone MAX comes with intuitive configuration software and interactive programming software, as well as easy to use automated control software. The Cyclone MAX also functions as a full-featured debug interface, and is supported by Freescale's CodeWarrior as well as development software from P&E.

P&E's Cyclone MAX is also available bundled with additional software as part of various Development Packages. In addition to the Cyclone MAX, these Development Packages include in-circuit debugging software, flash programming software, a Windows IDE, and register file editor.

Freescale Controller Continuum

68HC08/S08/RS08/(S)12(X) ColdFire® V1 ColdFire® V2/V3/V4 Power Architecture® ARM®

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