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Model 566A Acquisition Interface Module

9231107C 5/99

User's Manual

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1. Introduction

The Canberra Model 556A Acquisition Interface Module (AIM) a single-width NIM, has both 10 Base 2 and AUI Ethernet interfaces conforming to IEEE 802.2/802.3 communication standards. The module has been designed with two high-speed ADC ports and an Instrument Control Bus (ICB) for programmable front-end NIM units. Connected to an Ethernet network, the 556A allows data acquisition from any computer on the network.

The 556A is a single-processor design with overall control managed by an 80C186 16-bit microprocessor and data acquisition functions handled by a high-speed acquisition engine. An Ethernet processor is responsible for communications between the module and the Host computer.

The 556A AIM can acquire data in PHA or Loss-Free PHA mode from either ADC port independently. The AIM contains 64K, 32-bit channels of local acquisition memory and can acquire data from both ADCs at a maximum aggregate rate of 1 MHz (500 kHz for a single input). Preset and elapsed times are maintained within the module with centisecond resolution. The AIM will automatically terminate acquisition upon reaching the preset live or real time or a preset total counts in a region. If module power is lost, the spectral memory will be retained for up to three days.

An optional sample changer interface is provided for ADC 1 and optional independent start/stop functions are provided for both ADC channels.

The 556A AIM serves as a link between a host computer and signal processing NIM. This NIM can be configured with manual and/or programmable versions of Canberra's ADC, AMP, HVPS, AMX building blocks to tailor the system to the needs of any application. A single AIM in conjunction with a Genie family workstation can control a whole Bin of programmable NIM for total computer front-end configuration and control.

2. Controls and Connectors

This is a brief description of the 556A'scontrols and connectors. For more detailed information, refer to Appendix A, Specifications.

2.1 Front Panel

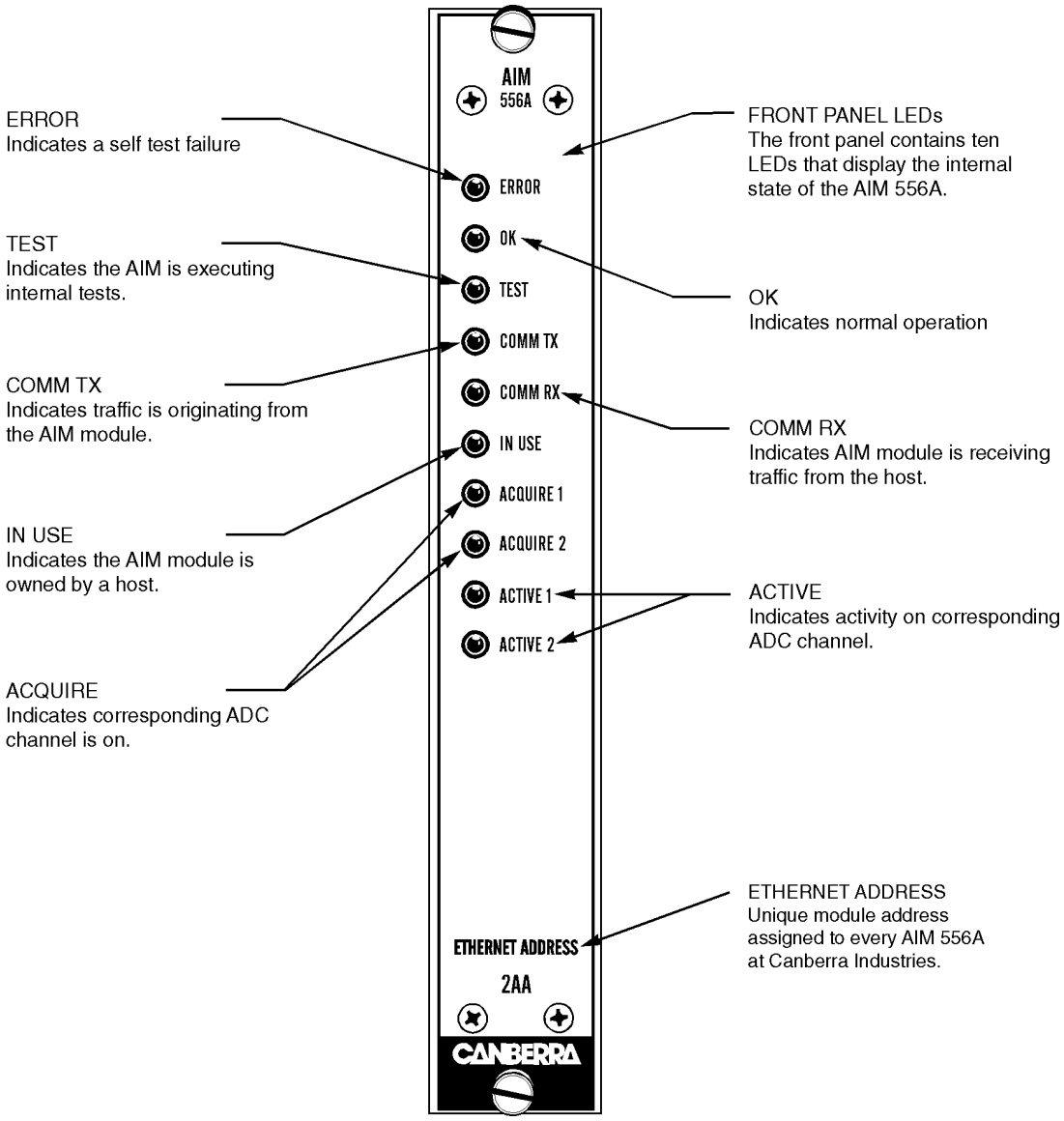


Figure 2.1 Front Panel Indicators and Connector

2.2 Rear Panel

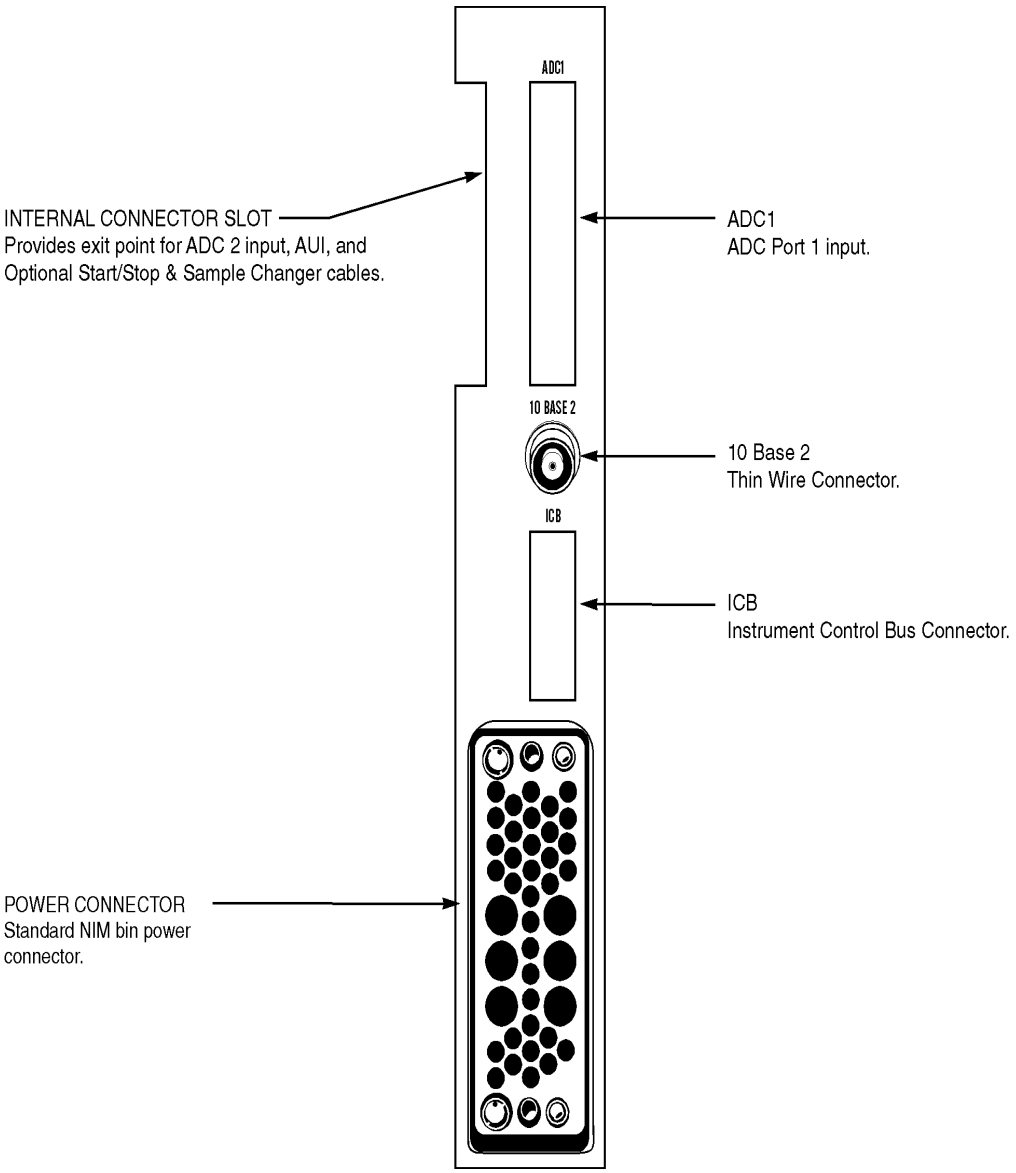


Figure 2.2 Rear Panel Connectors

2.3 Internal Controls

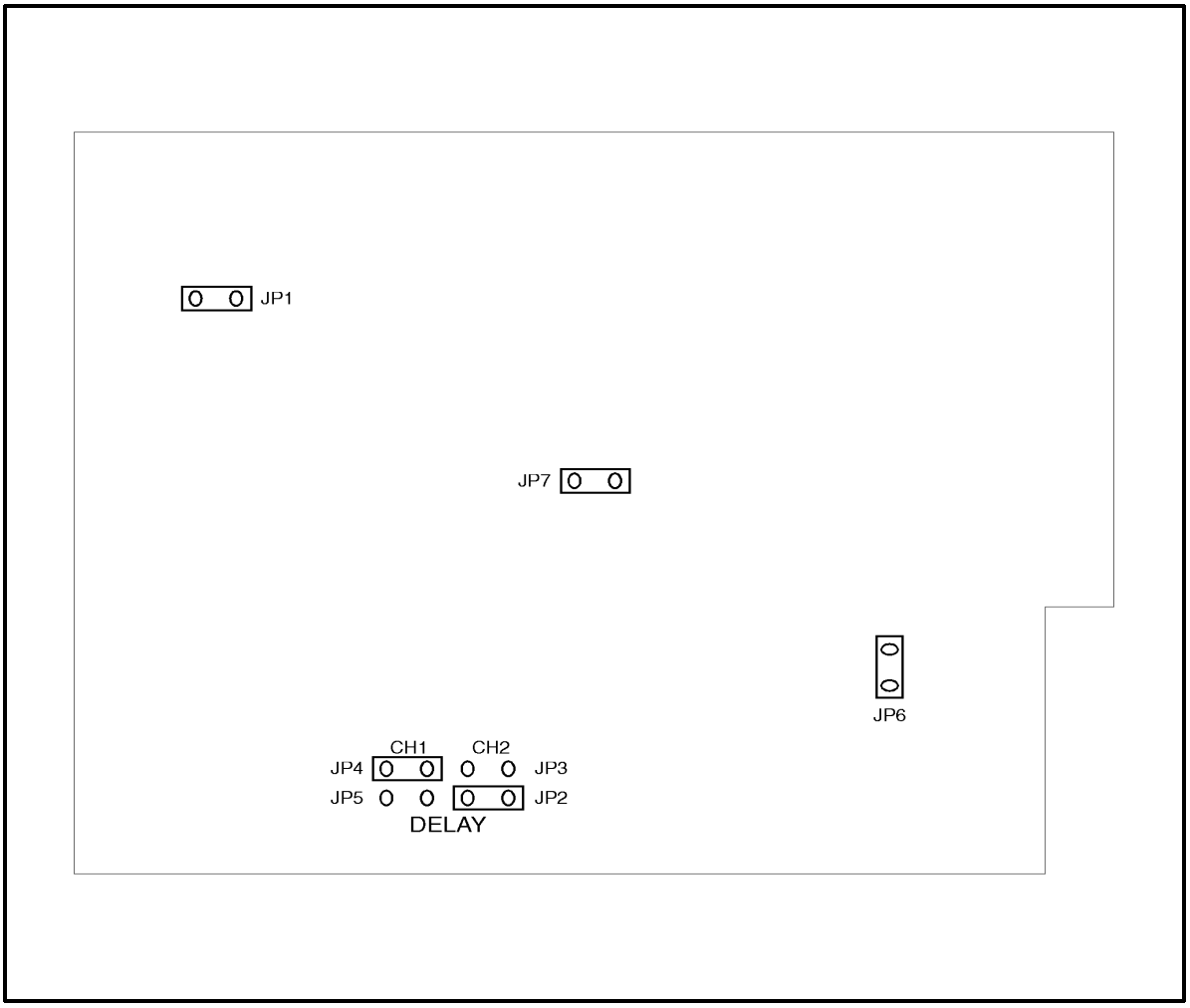


Figure 2.3 Internal Controls

Delay Settings

0.75 µs Delay. . . . Both jumpers in.
1.0 µs Delay. . . . . JP2 and JP4 in, JP3 and JP5 out (factory setting).
1.5 µs Delay. . . . . JP2 and JP4 out, JP3 and JP5 in.
2.0 µs Delay. . . . . Both jumpers out.

Note: Only jumpers JP2 through JP5 should be changed. Moving any other jumpers will affect the operation of the module.

3. Operation

Refer to the Model 9600 AIM/ICB System Setup Manual for a typical ICB installation and technical information.

3.1 Installation

The following procedure describes the installation of a Model 556A AIM module for remote acquisition in an existing system.

System Requirements

This procedure assumes that the following equipment is available:

- Host: (OpenVMS) VAX or AXP Server or Workstation
  or
  (PC) Industry standard personal computer.
- System Software: OpenVMS Version 5.5-2, AXP Version 1.5, or later, 48-0198 VMS Spectroscopy Applications Software and 48-0258 VMS Genie Display and Acquisition Software.
  or
  Windows 95/NT and S500 or S502 Genie-2000 Basic Spectroscopy Software.
  or
  OS/2 Version 2.0 or later, S400 or S402 Genie-PC Basic Spectroscopy Software and S410 Genie-PC AIM SFT Driver.
- Communications: Fully IEEE 802.3 and IEEE 802.2 compliant Ethernet interface.
- A NIM Bin which can supply sufficient power (see Appendix A.11, Power Requirements).
- Installed Ethernet Transceiver and transceiver cable for external transceiver application. (See Ethernet Transceiver manual for installation procedure.)
- An optional VT100 or compatible terminal set for 9600 baud, 8 data bits, no parity and 1 stop bit (required only for diagnostics).
- One 556A AIM module and serial diagnostics cable.

Carefully unpack the unit, verifying that you have received the Model 556A AIM module, one ADC cable, a 12-headed ICB cable, one BNC tee connector and the serial diagnostics cable. Thoroughly inspect all equipment for damage that may have occurred during transit. If there are no problems with the equipment, proceed with the following steps:

1. When the AIM is shipped from the factory, the transfer times for both ADCs are set at 1 µs. This will allow a maximum cable length of 4.5 m (15 ft). If these are the desired settings, go to step two. If you'd like to change the transfer time settings, remove the 556A's right side-panel. Referring to Figure 2.3 on page 4, change jumpers JP2-JP5 then replace the right side-panel.

Use the following guidelines to select the transfer rate: If the cables between the AIM and the ADCs are short, (i.e., less than 2 m (6 ft)), the fastest transfer rate can be selected. If the cables are long (i.e., more than 4.5 m (15 ft)), the slowest rate should be selected.

2. Turn off the NIM Bin's power, then install the 556A in the NIM Bin.

3. For External Transceiver applications, connect the Ethernet transceiver cable between the rear of the AIM module and the Ethernet transceiver box.

   For 10 Base 2 applications, connect the thinwire network to the 556A's 10 Base 2 port with a "T"-connector.

   The AIM connects to any IEEE 802.3 compliant transceiver, such as DEC DESTA and H4000. The external transceiver must have the Heartbeat function enabled. Refer to the Heartbeat section below for details. Each AIM has a unique network address in the form 00-00-AF-00-nn-nn. The last three digits are assigned to the AIM at the factory and are printed on a label on the module's front panel. You will need this address to specify which AIM you want to access. The AIM will operate in any legal Ethernet configuration. However, use caution if you run the AIM through an Ethernet bridge due to the large amount of traffic generated by the AIM. Bridges can be set up to ignore any message with the AIM address prefix "00-00-AF".

4. Orient the cable from the ADC or AMX (see Figure C.1, C.2 or C.3 starting on page 28) so that its pin one indicator (an arrow on the connector itself or a highlighted colored cable) is up and connect it to one of the keyed 34-pin ADC connectors on the AIM's rear panel. See Figure 2.2 on page 3 for location of the connectors.

5. Within two seconds of power on, the TEST and OK LEDs will turn on. Within 10 seconds, the IN USE LED will begin flashing. TEST and OK will stay on with IN USE Flashing for approximately 10 seconds. During this time, The 556A is waiting for a Bootstrap Enter Command. If this command is not received within 10 seconds, the unit will exit to the Main Application. This is indicated by all of the front panel LEDs flashing then turning off. Within 10 seconds the OK LED will turn on. This indicates that the Module has entered the Main Application and is ready to accept Host Commands. If any other LED turns on, this indicates an error condition, meaning that the Module may not be ready to accept host commands.

Heartbeat

In IEEE 802.3 networks, the heartbeat is a short burst of collision signal that is transmitted from the Medium Attachment Unit (MAU) to the Data Terminal Equipment (DTE) at the end of every packet. Because communications on a Ethernet LAN relies on collision-detection, the heartbeat generator creates a pseudo collision to ensure that the collision circuitry is functioning correctly. This pseudo collision consists of a 1 microsecond burst of 10 mhz oscillation at the line-driver outputs approximately 1 microsecond after the end of the transmission. This test is also referred to as the Signal Quality Error (SQE) test.

In most cases, the heartbeat can be enabled or disabled via a switch or jumper at the Attachment Unit Interface (AUI) device. In some cases, the switch or jumper can be accessed without removing the AUI's cover. In others cases, internal access to the AUI is required and the unit's operator manual should be consulted.

Both the AIM556A and DSA2000 modules require that the heartbeat operation be enabled in order to pass their internal loopback diagnostic whenever a AUI device is used. If the

heartbeat in the AUI is not present or enabled, the internal self-test cannot operate properly, thereby making it impossible to automatically determine the attached medium. The heartbeat is enabled automatically in the internal transceiver to satisfy the condition when the module is used in 10Base2 (Thinnet) applications because no external AUI device is required.

System Installation

The next few sections describe how to install the 556A on your Genie System and verify its operation.

- Genie-VMS Installation is described in Section 3.1.1.
- Genie-2000 Installation is described on page 7.
- Genie-PC Installation is described on page 8.

3.1.1 Genie-VMS Installation

This section tells you how to install and verify the operation of the 556A AIM on a Genie-VMS system with Model 48-0258 Integrated MCA Control Software package.

1. Log on to a host OpenVMS system. Enter the following command:

```
CONFIGURATION/DEVICES NI
```

A report which shows the status of all AIMs on the network is generated. The new AIM should be included in the report, as shown in the following example. (The report is updated every 20 seconds.)

		Memory Allocation	Input Usage				Owned by Node
Address	Status		1	2	3	4	
NI19B	Reachable						FLAME
NI58B	Reachable	80000000	Free	Free	N/A	N/A	
NI7A3	Reachable	80000000	Free	Free	N/A	N/A	
NI622	Reachable	80000000	Free	Free	N/A	N/A	

2. Set up acquisition for the first ADC connected to the AIM with the command:

```
MCA CREATE TEMP NInnnn:1/CHANNELS=2K
```

Where *nnnn* are the least significant digits of the AIM's address. Omit the leading zeros. For example, module address 2B1 would be written as "NI2B1".

After you enter this command, the AIM's "In-Use" LED will turn on.

3. Turn on acquisition with the command:

```
MCA ON TEMP
```

The ACQUIRE LED for the first ADC should turn on. If you have display capability, you will see a spectrum acquiring.

4. Release the AIM with the command:

```
MCA DEL TEMP
```

3.1.2 Genie-2000 Installation

This section tells you how to install and verify the operation of the 556A AIM on a Genie-2000 system.

1. Use the MID Wizard or the MID Editor to create a definition containing an AIM MCA. For details, refer to the section titled “Defining an AIM MCA” in Chapter 3, *MCA Input Definition Editor*, in your Genie-2000 Operations Binder.

2. Start the Gamma Acquisition and Analysis application and open the AIM datasource by selecting **File** | **Open datasource**, then choosing the AIM datasource. Now click on the ‘Acquire On’ button to start data acquisition. The AIM’s ACQUIRE LED for the selected ADC should turn on and you should see a spectrum acquiring.

3. Click on the Acquire Off button to stop acquisition. Select **File** | **Close** to close the datasource and release the AIM.

3.1.3 Genie-PC Installation

This section tells you how to install and verify the operation of the 556A AIM on a Genie-PC system.

1. Use the MID Editor to create a definition containing an AIM MCA. For details, refer to the section titled “Defining an AIM MCA” in Chapter 3, *MCA Input Definition Editor*, in your Genie-PC Basic Operation Binder.

2. Start Genie-PC’s Spectroscopy Assistant application. For more information, refer to Chapter 4, *Spectroscopy Assistant Tutorial* and Chapter 7, *Spectroscopy Assistant Reference*, in your Genie-PC Basic Operation Binder.

3. Start the MCA View Control application by selecting it from the Spectroscopy Assistant’s Applications menu. In the MCA View Control window, open the AIM datasource by selecting **File** | **Open datasource**, then choosing the AIM datasource. Now click on the ‘Acquire On’ button to start data acquisition. The AIM’s ACQUIRE LED for the selected ADC should turn on and you should see a spectrum acquiring.

4. Click on the MCA View Control’s Acquire Off button to stop acquisition. Select **File** | **Close** to close the datasource and release the AIM.

3.2 Operating Procedures at the Host

Always turn off the power to a NIM bin which contains an AIM module before inserting or removing any modules or connecting an Ethernet transceiver cable or 10 Base 2 cable.

The host system updates the status of the AIMs on the network every 20 seconds; therefore you may have to wait a few seconds for the host to recognize a new AIM.

If an AIM is reset (via power up or local terminal command), the host system reconfigures the AIM automatically.

Genie-PC or Genie-2000

For a Genie-PC or Genie-2000 system, refer to its User's Manual for AIM operation.

Genie-VMS

For a host OpenVMS system, refer to the Model 48-0198 Genie-VMS Spectroscopy System manual. A few commands are given below to get you started with a host OpenVMS system.

To view the status of all the networked modules, type the following command:

```
CONFIGURATION/DEVICE NI
```

A report will be generated which shows the addresses of all the AIMs on the network.

The CREATE command creates an MCA configuration. The format is:

```
MCA CREATE [configuration name] [ADC input device]
```

The following example causes the MCA configuration TEMP to be set up for the first ADC connected to the AIM module (2B1). Note that dashes and leading zeroes in the AIM's address were omitted in the command.

```
MCA CREATE TEMP NI2B1:1/CHANNELS=2K
```

Where:

MCA	Utility which allows access to the facilities of the Integrated MCA control system, which controls all 9900 acquisition and display resources.
CREATE	Creates an MCA configuration.
TEMP	Name of the new configuration being created.
NI	Prefix identifies the ADC as networked.
2B1	AIM network address.
:1	Indicates data is to be acquired from the first ADC port.

The following qualifiers were used in this command:

/CHANNELS	Specifies the number of channels per group for the new MCA configuration. In this case, the number of channels is 2048 (2K).

The "MCA Commands" chapter in the *Model 48-0198 Genie-VMS Command Descriptions Manual* has more information on this command and its qualifiers.

Next, to begin collecting data, you must turn on acquisition with the following command:

```
MCA ON TEMP
```

If you have display capability, you should see a spectrum.

When you are finished acquiring data, turn acquisition off with the following command:

```
MCA OFF TEMP
```

Analyze the data by performing the following command:

```
PEAK
```

After analysis is complete, a report of the peaks which were found will be printed on the screen. (You can specify a listing file name using the /LIST qualifier, as follows: PEAK/LIST=[filename]).

Now you can save the data on disk by performing the MOVE command. For example

```
MOVE TEMP SAVE
```

Where TEMP is the name of the source MCA configuration and SAVE is the name of the destination file. If the destination file already exists, a new version is created. Now that the data is saved to disk under the file name SAVE, you can release the AIM by deleting the MCA configuration TEMP.

```
MCA DEL TEMP
```

3.3 Start Up Sequence

When the 556A's power is first turned on, the Test and Ok LEDs will turn on and within 10 seconds, the In Use LED will begin flashing. The Test and Ok LEDs will stay on and the In Use LED will continue to flash for approximately 10 seconds.

During this initialization period, the 556A will wait for a Bootstrap Enter command. If this command is not received within 10 seconds the 556A will exit to the Main Application. This is indicated by all of the front panel LEDs flashing and then turning off.

Within 30 seconds of power on, the Test LED will turn on, indicating that the 556A has entered the Main Application and is conducting its power on test sequence. If no errors are encountered within 30 seconds, the Ok LED will turn on, indicating that the 556A is ready to honor Host Commands.

If any other LED turns on, this indicates an error condition and the Module may or may not be ready to honor host commands. In the case of an error condition being encountered on start up the failure(s) will be displayed on the local terminal (if connected). If no errors are encountered, the 556A Main Menu will be displayed on the local terminal, if connected, after the power on sequence is complete.

4. Circuit Description

Each of the major sections of the Model 556A described here refers to the appropriate sheet of the schematic, which can be ordered from Canberra with the Schematics Request Form at the end of this manual.

Figure 4.1 shows a block diagram of the Model 556A.

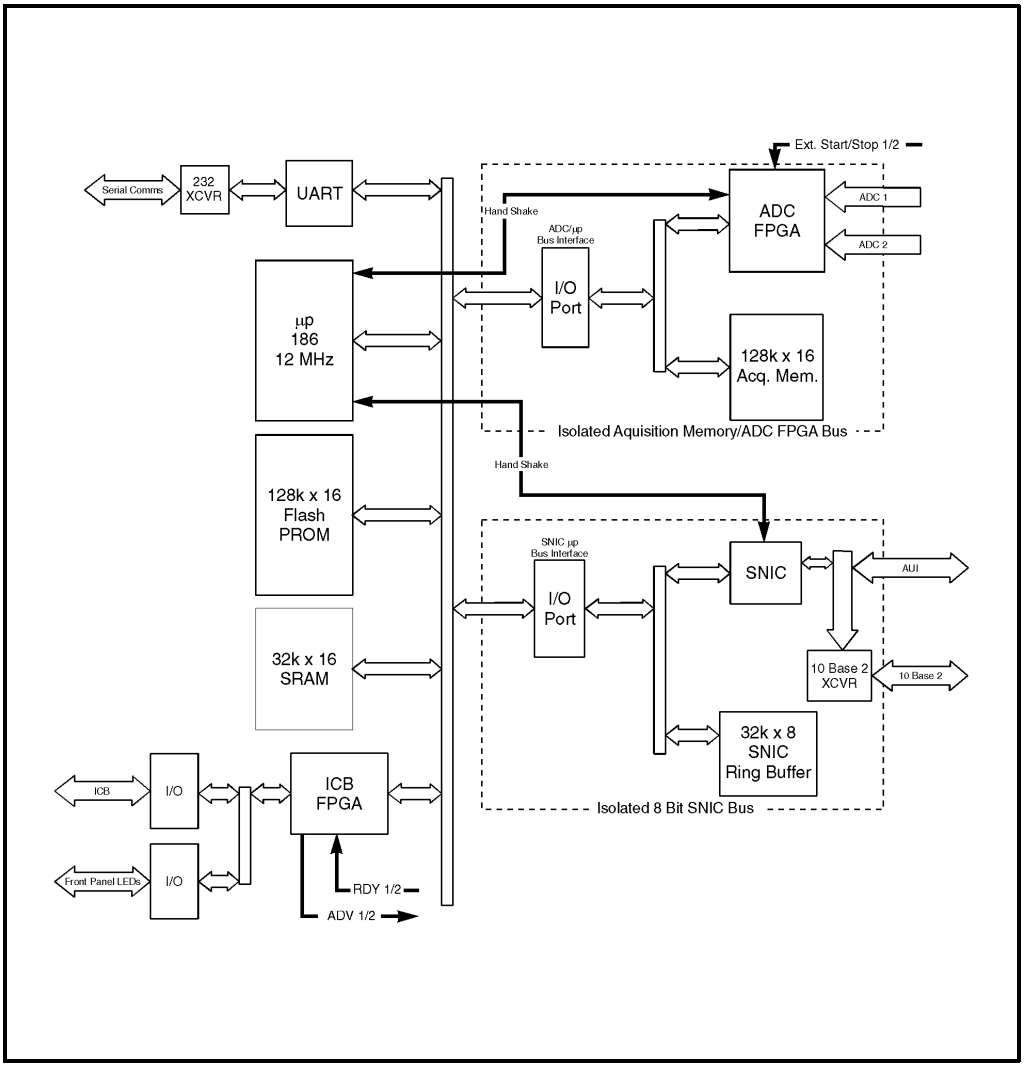


Figure 4.1 AIM Block Diagram

4.1 NIM Input Power Section

(Schematic sheet 2).

All dc power required by the AIM is provided by this section. The +24.0 V and +6.0 V dc supplied by the NIM bin is used to derive the +5.0 V required by the AIM logic. RV1 is used to adjust the +5.0 V to be within the specified tolerance. The +12.0 V supplied by the NIM bin is filtered then used to provide power to the external AUI transceiver via J-1.

4.2 CPU Section

(Schematic sheets 4 and 6).

The CPU section is based upon the Intel 80C186XL-12 Microprocessor (U47). The microprocessor operates at 12 MHz, which is derived from U58, a 24 MHz oscillator. The microprocessor code executes out of two AM29F010 Flash Memories (U52 and U57). Each Flash is 8 bits by 128k with the two providing a memory space 16 bits by 128k. The Microprocessor STACK and other volatile memory is provide by two static RAMs. Each SRAM is 8 bits by 32k, with the two providing a 16 bit by 32k memory space. Both SRAMs are backed up via U59, a DS1210, using C26, a Super Capacitor, as a backup power source.

U49 is a DS1232 Watch Dog Timer. This chip functions as a power on reset generator, power failure detector, and microprocessor out of control detector. U48 is a PAL, which provides decode logic required for ARDY generation, chip selects, and read/write strobes.

The Live Time for each ADC channel is provided by the two externally controllable microprocessor timers. U5 and U6 provide the serial diagnostics port of the AIM. U13 is an Actel 1010B. This FPGA provides decode logic for the Ethernet Section, a state machine that allows ICB communications, sample changer logic, ADC delay selection via JP-2 through JP-5, and front panel LED control. U14 provides the ACTIVE1 and ACTIVE2 front panel LED function derived from the ADC ACCEPT signals.

4.3 Acquisition Section

(Schematic sheets 2 and 3)

This section interfaces the AIM to the two ADC input ports. The Acquisition Section operates on an independent data and address bus from the microprocessor. The ADC FPGA (U42) provides the state machine that allows data acquisition from each ADC port. The ADC FPGA also contains logic required to arbitrate access to the acquisition data bus by the microprocessor.

Acquisition memory is provided by two static RAMs (U27 and U28). Each SRAM is 128k by 8 bits, with two providing a 128k by 16 bit acquisition data bus. It should be noted that this memory space is only addressable on even word boundaries by the microprocessor. It should also be noted that a channel is composed of two consecutive words, which provides the required 32-bit channel representation.

The Acquisition Memory is backed up using the Super Capacitor (C26) via U25, a DS-1210. U29 and U30 are 74HC244s that provide a buffering to isolate the microprocessor address bus from the Acquisition Section when the microprocessor has not been granted access.

U31 and U32 isolate the microprocessor data bus from the Acquisition Section until it is granted access. U37 and U38 are latches used to demultiplex the ADC FPGA address from the Acquisition Section multiplexed address/data bus.

U46, U45, U44, U43, U39 and U38 provide buffering between the ADC FPGA and the associated ADC Ports. The Sample Changer / Start-Stop Interface is provided by the ADC and ICB FPGAs. The LS14 buffers provided by U60 isolate the FPGAs from external connector J-7 and provide signal conditioning.

4.4 Ethernet Section

(Schematic sheets 5 and 7)

The Ethernet Section provides Host communications that are compliant with IEEE 802.3 and 802.2. This section is based upon the Serial Network Interface Controller (SNIC DP83901A, U16). U24 is a 20 MHz oscillator used for the 10 Mbps Ethernet. The SNIC is configured to operate on an 8-bit multiplexed data and address bus. The Ethernet Section is also isolated from the microprocessor bus. This allows the SNIC to service Ethernet traffic as fast as possible.

Isolation is provided by two 74HC652s (U18 and U21). These buffers are controlled via ICB FPGA logic and PAL logic. They allow slave mode control of the SNIC and remote DMA operation of the SNIC. A 32k by 8-bit static RAM provides the transmit and receive ring buffers required by the SNIC. The address into the ring buffers is demultiplexed from the Ethernet data bus via two 74HC373 latches (U19 and U20). AUI and 10 Base 2 Ethernet Interfaces are provided in this section.

The AUI Interface is provided via a pulse transformer (U22) to a 15-pin header (J-1). The 10 Base 2 Interface is provided via another pulse transformer (U3) and a DP8392 (U1). The DP8392 provides the AUI to 10 Base 2 conversion (J-2). AUI and 10 Base 2 selection is made via control logic in the ICB FPGA. A +5.0 V to -9.0 V dc to dc converter (U2), which turns on for 10 Base 2 and off for AUI is controlled via the processor through the ICB PFGA.

5. Diagnostics Monitor Mode

This section describes the 556A's Power On Diagnostics, executed every time the unit is powered on. The TEST LED will be on when the diagnostics function is executing. The test descriptions in this section assume that the Internal Serial Diagnostics Port (J-3) is connected to a local terminal.

A Soft Error will be indicated by the ERROR LED flashing for 60 seconds before entering the main application. This is a recoverable error, which allows Host Commands to be honored. A Hard Error will be indicated by a constantly illuminated ERROR LED, this is a fatal error, which keeps the AIM from honoring Host Commands. It also forces the AIM into the Diagnostics Mode.

5.1 Power On Diagnostics

The following tests are performed by the AIM 556A at power up. The designator (SOFT/HARD) indicates the type of error if encountered.

1. UART (SOFT): Tests the AIM's serial communications channel.
2. Microprocessor SRAM (HARD): Tests the 32k x 16 microprocessor SRAM.
3. Flash (HARD): Tests the 128k x 16 microprocessor flash memory. The ERROR, TEST and OK LEDs will all turn on at power up.
4. Acquisition SRAM (HARD): Tests the 128k x 16 ADC SRAM.
5. ADC (HARD): Tests the ADC FPGA.
6. ICB (HARD): Tests the ICB FPGA.
7. SNIC (HARD): Tests the SNIC Ethernet controller.
8. Ethernet DMA (HARD): Tests the DMA channel to the SNIC from the microprocessor.
9. TDR (HARD if both Ethernet ports fail): Determines the Ethernet port in use (AUI or 10 BASE 2).

During the startup initialization of the main application, the AIM module puts itself into diagnostics command monitor mode. This allows startup diagnostics messages to be displayed to the VT-100 terminal. When the diagnostics have finished, a detailed account of the working status of all hardware components on the board will be presented.

After the diagnostics have finished, you'll see the menu shown below:

Mode	Keys
Command Monitor On	CTRL + N
Command Monitor Off	CTRL + F
Erase Local Terminal	CTRL + E
Ethernet Monitor	CTRL + L
Diagnostic Monitor	CTRL + D

The menu will appear on startup and when exiting from Command Monitor, Ethernet Monitor, and Diagnostic Monitor modes.

5.2 Command Monitor Mode

The Command Monitor mode displays the Ethernet command being processed and the final status of the command. This mode is entered with the CTRL + N key combination. The layout for the message is:

> Ethernet Type – Message Type – Command Type – Status (only failure will be indicated)

For example:

> UI – Packet Message – Return ADC Status
> or
> UI – Packet Message – Return ADC Status – FAIL

This mode scrolls the messages on the screen as they are received and processed by the AIM. To exit this mode, enter CTRL + F from the terminal. Exiting from this mode will return you to the main menu.

5.3 Erase Local Terminal

The Erase Local Terminal command will send the escape sequence to the terminal that will delete all text from the screen. This is only available at the top level of the menu tree and during the Command Monitor mode. It will not be accessible in Ethernet Monitor Mode or Diagnostic Monitor Mode.

5.4 Ethernet Monitor Mode

Ethernet Monitor Mode displays the current Ethernet statistics for the module. These statistics indicate the number of receive, transmit, and miscellaneous errors. It also indicates the number of received messages, transmitted messages, and multicast messages processed. A typical Ethernet Error Monitor display is shown in Figure 5.1.

To update the display, press L. To clear the counters, press Z. Pressing Q will return you to Command Monitor Mode if it is enabled, otherwise it will return you to the Main Menu.

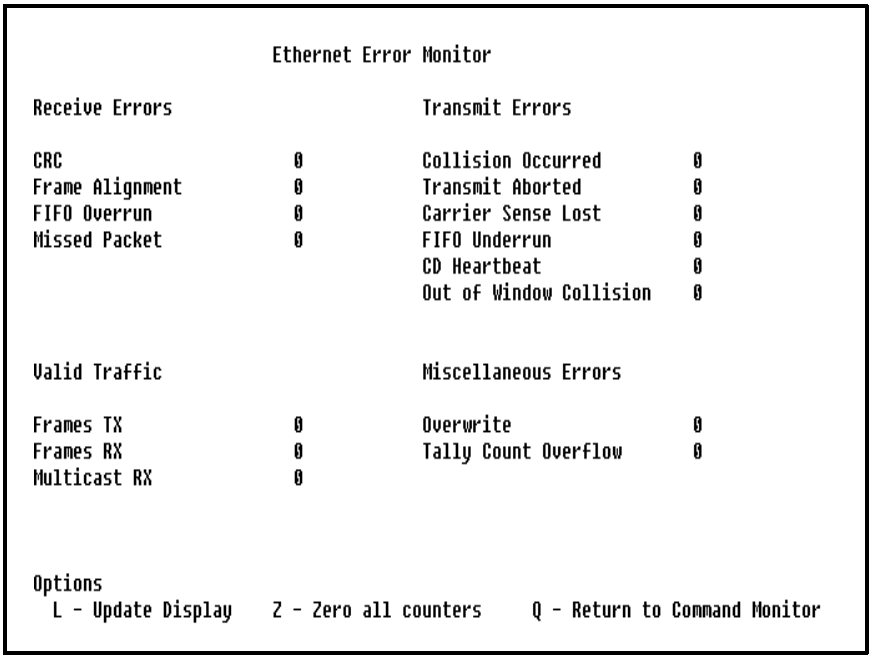


Figure 5.1 The Ethernet Error Monitor Display

5.5 Diagnostic Monitor Mode

Diagnostic Monitor mode is a user interactive diagnostics mode which presents a menu of diagnostics tests that can be run on the module. This mode cannot be entered while the module is owned. The reason for this is that some tests are time intensive and would cause communications between a host and the module to fail. Also, the acquisition memory tests perform write/read tests which during an acquisition have the potential to corrupt a spectrum being collected.

The Diagnostic Monitor Mode menu is shown in Figure 5.2. This screen is divided into two parts, the menu, enclosed by the graphical outline, and the scrolling output region below it which consists of six lines available for output. When running tests multiple times, the output will be displayed at the bottom and will scroll up as space is needed.

Options A, B, C, D, I, J, K, L, M, and N will ask you to enter the number of times the test is to be run; the value must be in the range 1–999.

A. Test SRAM

This test uses a reserved area of the SRAM to perform read/write tests to ensure its ability to perform these tasks. The test writes a few bytes to the reserved area and then verifies the values read back from the same locations. It should be noted that for the AIM to enter the main application, SRAM would have to be valid due to the fact that the bootstrap program runs completely out of the SRAM.

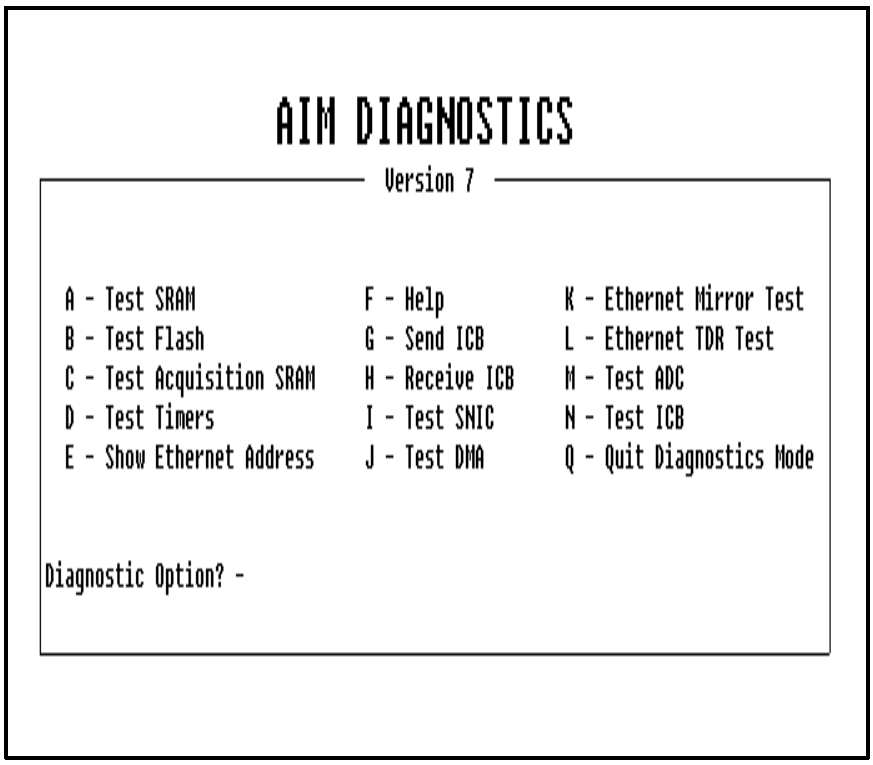


Figure 5.2 The Diagnostic Monitor Mode Menu

B. Test Flash

The flash test verifies the checksums of the parameters sector of the flash to ensure the flash is programmed correctly. The test calculates the checksums on each of the sectors and compares them to those stored in the parameters sector. The test will pass only if all checksums for sectors 0–5 are identical to those stored.

C. Test Acquisition SRAM

This test writes values to specific areas of the acquisition SRAM and then verifies that those values have been written. The previous values at those locations before the test are saved and restored after the test. The test is considered passed if the values written are equivalent to the values read.

D. Test Timers

This test verifies the ability of the timers to count correctly. The test reconfigures Timers 0 and 1 to count at the same rate as Timer 2. Interrupts are disabled during the setup process and when enabled, Timer 2 counts for 10 time ticks or 100 ms. At the end of this count, the contents of Timers 0 and 1 checked for a value greater than or equal to 9. The value of 9 is used in the event that the last timer interrupt for one of the timers is not processed, leaving its count at 9. The test is considered passed if both timer channels have a count of 9 or greater.

E. Show Ethernet Address

This option displays the Ethernet address for the module in the output area of the screen. The address is displayed separated by dashes; for example: 00–00–AF–00–AA–CC. The last two are the ID used by the host when setting up the module.

F. Help

This menu option will give help on any of the menu options. You will be prompted to enter the option for which help is wanted. An incorrect entry will return to the initial option prompt after displaying an error. If a valid entry is made, the help text for that option will be displayed in the output area of the screen.

G. Send ICB

This menu option will enable you to send a one byte value (00–FF hex) over the ICB bus to an address between 00 and FF hex. You will first be prompted for the ICB address. When that value has been entered, you will be prompted to enter the value to send to that address. The function will occur and a status message will appear in the output area of the screen.

H. Receive ICB

The Receive ICB command will prompt you for an address to receive data from the ICB bus. Once entered, the function will be performed and a request for data will be made across the ICB bus. The status of the function will be displayed in the output area of the screen. If the function was successful, the value for the specified address will be displayed. If a timeout error occurs, the appropriate error message will be displayed.

I. Test SNIC

This option will perform a loopback test on the SNIC. This test will perform loopback tests 1 and 2. These are internal tests for the SNIC to ensure the internal integrity of the Ethernet controller. These tests are part of the initial hardware startup tests that are performed when entering the main application.

J. Test DMA

The Test DMA option performs a test to ensure the ability of the microprocessor to perform a DMA transfer properly. Values are put into a buffer which is then transferred, using a DMA write, to the SNIC's ring buffer. The values are then read back into a separate buffer using a DMA read operation, then the two buffers are compared to ensure that the values read back are the same as those written to the ring buffer. The test is passed if the values read back are identical to those written.

K. Ethernet Mirror Test

The Ethernet mirror test requires another module or node that understands 802.2 messages of type TEST. The mirror test composes and transmits a TEST type message over the Ethernet and waits for a response. The responses to 802.2 TEST messages are just a reply to the message with the same data, and the reversal of the destination and source addresses by the receiver. This test requires a test for timeout in the event that no response is received. If no response is received or the response received is not what is expected, the appropriate error message will be displayed, otherwise the pass condition message will be displayed.

L. Ethernet TDR Test

This option performs the 3rd loopback test on the SNIC. The first two are internal tests of the SNIC. This test requires one of the Ethernet ports to be connected to a valid network. The SNIC transmits data out onto the Ethernet network and receives it at the same time. The data received is then compared to that transmitted. The test passes if the data is identical.

M. Test ADC

The test ADC option tests that the status register of the ADC FPGA for a value of 0 for the overflow bits on channels 1 and 2 and a 0 for the acquisition status for both channels, as well. If this is not the case, the test indicates a failure.

N. Test ICB

To test the integrity of the ICB FPGA, the status word is read and a test of the enable remote write bit are made. The test passes if and only if this value is a 0.

Q. Quit Diagnostics Mode

This option will exit from diagnostics mode and return you to the Command Monitor mode.

5.6 Preventive Maintenance

Preven tive maintenance is not required for this unit.

When needed, the front panel of the unit may be cleaned. Disconnect the unit's power before cleaning. Use only a soft cloth dampened with warm water and make sure the unit is fully dry before restoring power. Because the NIM wrap is not water tight, *do not* use liquids to clean any part of the unit.

A. Specifications

A.1 Inputs/Outputs

ADC1 and ADC2 (Data acquisition) – 34 pin ADC standard.

Ethernet – AUI or 10 Base 2: Provides connection to Ethernet; IEEE 802.2 and 802.3 compliant.

ICB (Instrument Control Bus) – Provides Host access to ICB Bus.

RS-232 – Terminal I/O for diagnostic functions.

A.2 Manual Controls

ADC Transfer Time – Internal jumper plugs to select transfer times compatible with cable length to each ADC. Factory set for 1 μs (≤4.6 m). Other selections are: 0.75 μs, 1.5 μs, 2 μs. Can be set independently for ADC1 and ADC2.

A.3 Front Panel Indicators

ERROR – LED indicates a hard, non-recoverable error (continuously lit) or soft error (blinks for 60 s on startup) in the module.

OK – LED; indicates module is operational.

TEST – LED; indicates module is in internal test mode.

COMM TX – LED; indicates module is sending data to host.

COMM RX – LED; indicates module is receiving data from host.

IN USE – LED; indicates host has put module on-line.

ACQUIRE – LEDs for ADC ports 1 and 2; indicates corresponding port is acquiring data.

ACTIVE – LEDs for ADC ports 1 and 2; indicates activity on corresponding ADC port.

A.4 Performance

ETHERNET INTERFACE

AIMS/NETWORK – Unlimited.

Communication Standard – IEEE 802.2 and 802.3.

Network Address – 00-00-AF-nn-nn-nn, where nn-nn-nn is a unique address factory set for each Model 556A.

A.5 ADC Interface Port

Number of Ports – 2.

Total Memory in AIM module – 64K channels.

Memory per Port – 0 to 64K Channels.

Counts per Channel – 2^{31}–1 (>2 x 10^9).

Groups per Port – 64, maximum.

Channels per Group – 0 to 32K in 256 channel increments.

A.6 Acquisition Modes

PHA – Read, +1, Write.

PHA/LFC – Read, +N, Write.

A.7 Acquisition Cycle Time

Jumpers set for a transfer time of 1 µs:

PHA – 2 µs.

PHA/LFC – 2 µs.

A.8 PHA Preset

Control – Live and/or true time; counts in an ROI; overflow in any channel.

Time Resolution – 0.01 s.

Time Range – 0.01 to >21 x 10^6 s.

Count Range – 1 to 2^{31}-1 counts

A.9 Environmental

Operating Temperature – 0-50 °C

Operating Humidity – 0-80% Relative, Non-condensing

Tested to the environmental conditions specified by EN 61010, Installation Category I, Pollution degree 2

A.10 Connectors

ADC1 and ADC2 – 34-pin male ribbon headers; ADC1: rear panel; ADC2: internal connector accessed through rear panel cutout.

AUI – 15-pin female D-connector with slide locks; accessed through rear panel cutout.

10 Base 2 – 50 Ω isolated BNC; rear panel.

ICB – 20-pin male ribbon; rear panel.

Local Terminal – Internal 10-pin ribbon connector header.

A.11 Power Requirements

+24 V dc – 2 mA
+12 V dc – 225 mA (typical)
+6 V – 750 mA

A.12 Physical

SIZE – Standard single-width NIM module 3.43 x 22.12 cm (1.35 x 8.71 in.) per DOE/ER-0457T.

NET WEIGHT – 0.9 kg (1.91 lb).

SHIPPING WEIGHT – 1.8 kg (4 lb).

A.13 Accessories

C1560 – 12-unit ICB connecting cable.

C1703-2 – One 60 cm (2 ft) AIM to ADC/AMX cable.

C1720 – Sample changer cable.

C1721 – Local terminal cable.

C1722 – Start/stop cable.

B. Signal Connectors

This section describes signals and pinouts for the 556A's front panel (Local Terminal) and rear panel (Data Interface, ICB Interface, Ethernet Interface and NIM Power) connectors.

B.1 Local Terminal Connector

The internal Local Terminal connector supports a standard RS-232 interface to a terminal, which can be used to run local AIM diagnostics and monitor the status of the module. All input and output signal levels are RS-423 compatible; Output is > +5 V space and < –5 V mark. Input is +0.4 V to +15 V space and –0.4 V to –15 V mark.

Pin Number		Signal	Description
J3 9-pin	25-pin EIA Adapter		
1,4,6,7,8,9	1,5,6,8-19 21-25	NC	No connection.
2	3	TXDB+	Transmitted data to terminal.
3	2	RXDB+	Received data from terminal.
5	7	GND	Signal ground.
N/A	4-20	RTS/DTR	Request To Send and Data Terminal Ready are connected together in the 25-pin EIA Adapter.

Communications Parameters

The local terminal connector's serial character protocol is fixed at:

9600 baud
8 data bits
no parity
1 stop bit

B.2 Data Interface Connnectors

These two rear panel 34-pin ribbon conectors (ADC1 and ADC2) provide all the necessary signals for connection to the ADC. Negative true signals are shown with a trailing asterisk (ACEPT*); all other signals are positive true.

Pin	Signal	Pin	Signal
1	GND	2	ACEPT*
3	GND	4	ENDATA*
5	GND	6	CDT* or CDT
7	GND	8	ENC* or ENC
9	GND	10	READY*
11	GND	12	INB* (INV*)
13	NC	14	ADC00*
15	ADC07*	16	ADC01*
17	ADC08*	18	ADC02*
19	ADC09*	20	ADC03*
21	ADC10*	22	ADC04*
23	ADC11*	24	ADC05*
25	ADC12*	26	ADC06*
27	ADC14*	28	ADC15*
29	NC	30	NC
31	NC	32	NC
33	NC	34	ADC13X*

Data Interface Signal Functions

This section describes the function of each data interface signal in detail. All input and output signals are TTL compatible with 2.2 kΩ resistors to +5 V. Unless otherwise noted, the input signal levels are:

Low = 0 to 0.8 volts
High = 2.0 to 5.0 volts

And the output signal levels are:

Low = 0 to 0.5 volts
High = 3.0 to 5.0 volts

Signal	Pin	Description
ADC00*	14	INPUT: Binary data 2^0 (LSB).
ADC01*	16	INPUT: Binary data 2^1.
ADC02*	18	INPUT: Binary data 2^2.

ADC03*	20	INPUT: Binary data 2^3.
ADC04*	22	INPUT: Binary data 2^4.
ADC05*	24	INPUT: Binary data 2^5.
ADC06*	26	INPUT: Binary data 2^6.
ADC07*	15	INPUT: Binary data 2^7.
ADC08*	17	INPUT: Binary data 2^8.
ADC09*	19	INPUT: Binary data 2^9.
ADC10*	21	INPUT: Binary data 2^{10}.
ADC11*	23	INPUT: Binary data 2^{11}.
ADC12*	25	INPUT: Binary data 2^{12}.
ADC13X*	34	INPUT: Binary data 2^{13}.
ADC14*	27	INPUT: Binary data 2^{14}.
ADC15*	28	INPUT: Binary data 2^{15} (MSB).
ENDATA*	4	OUTPUT (Enable Data): Used to enable the tri-state buffers driving the 16-bits of data onto the lines ADC00* through ADC15*.
READY*	10	INPUT (Data Ready): Indicates that data is available for transfer from the ADC. High level > 3.5 V.
ACEPT*	2	OUTPUT (Data Accepted): Signals the ADC that the data has been accepted.
INB*	12	INPUT (Inhibit): In non-LFC mode or State 2 of the LFC transfer cycle, this signal indicates that the data available for transfer from the ADC is to be discarded. In LFC mode, this signal indicates that the number transferred during State 1 is the LFC increment ($1 \rightarrow 255$). High level > 3.5 V.
ENC*	8	OUTPUT (Enable Converter): This signal enables or disables the ADC module. ENC* = logic 0 enables ADC operation.
CDT*	6	INPUT (Composite Dead Time): This signal indicates the time when the ADC or connected amplifier is busy and cannot accept another input event. It is used to gate the live time clock circuit in the MCA. High level > 3.5 V.
NC	13	No connection.
NC	29	No connection.
NC	33	No connection.
NC	31	No connection.
NC	32	No connection.
NC	30	No connection.
GND	1,3,5,7,9,11	DC common for all interface signals.

B.3 ICB Interface Connector

This rear panel 20-pin ribbon connector (ICB) provides all the necessary signals for connecting the 556A to the Instrument Control Bus (ICB). Negative true signals are shown with a trailing asterisk (LWE*); all other signals are positive true.

Pin	Signal	Pin	Signal
1	GND	2	LD0
3	LD1	4	GND
5	LD2	6	LD3
7	GND	8	LD4
9	LD5	10	GND
11	LD6	12	LD7
13	GND	14	LWE*
15	GND	16	LDS*
17	GND	18	LAS*
19	GND		

ICB Interface Signal Functions

This section describes the function of each ICB interface signal in detail. All input and output signals are TTL compatible with a 2.2 kΩ resistor to +5 V. Unless otherwise noted, the input signal levels are:

Low = 0 to 0.8 volts
High = 2.0 to 5.0 volts

And the output signal levels are:

Low = 0 to 0.5 volts
High = 3.0 to 5.0 volts

SIGNAL	PIN	DESCRIPTION
LD0	2	INPUT/OUTPUT: Address/Data line 0 (LSB).
LD1	3	INPUT/OUTPUT: Address/Data line 1.
LD2	5	INPUT/OUTPUT: Address/Data line 2.
LD3	6	INPUT/OUTPUT: Address/Data line 3.
LD4	8	INPUT/OUTPUT: Address/Data line 4.
LD5	9	INPUT/OUTPUT: Address/Data line 5.
LD6	11	INPUT/OUTPUT: Address/Data line 6.
LD7	12	INPUT/OUTPUT: Address/Data line 7. (MSB)
LWE*	14	OUTPUT (Write Enable): This signal is active when the AIM is writing to the ICB.

LDS*	16	OUTPUT (Data Strobe): Used to latch the data into a slave during a write cycle or gate the data onto the bus during a read cycle.
LAS*	18	OUTPUT (Address Strobe): Used to latch the address which the AIM is accessing from the slave unit.
GND	1, 4, 7, 10, 13, 15, 17, 19	DC common for all interface signals.

B.4 Ethernet Interface Connector

The AIM, which is capable of operating with any IEEE 802.3-compliant Ethernet transceiver, uses this 15-pin connector for the electrical interface to the Ethernet transceiver cable (AUI).

Pin	Signal	Function
1, 4, 6, 11, 14	GND	Common dc line for all interface signals.
2 9	ECLN+ ECLN–	COLLISION PAIR: A differentially driven input pair tied to the collision-presence pair of the Ethernet transceiver cable. The collision-presence signal is a 10-MHz square wave.
3 10	ETRMT+ ETRMT–	TRANSMIT PAIR: A differential output driver pair that drives the transmit pair of the transceiver cable.
5 12	ERCV+ ERCV–	RECEIVE PAIR: A differentially driven input pair which is tied to the receive pair of the Ethernet transceiver cable.
13	E12V	+12 volt output supplying power to the Ethernet Transceiver.
7, 8, 15	NC	No connection.

10 Base 2, or thinwire, connection is through an isolated BNC.

B.5 NIM Power Connector

+24 V . . . . . pin 28
+12 V . . . . . pin 16
–12 V . . . . . pin 17
+6 V . . . . . pin 10
Power return to ground . . . . pin 34

C. Setup Diagrams

These diagrams, which include several of the more common systems, are provided to help you set up a system using the 556A AIM.

C.1 Typical ICB Bus Installation

Figure C.1 shows a single-input system with a Model 556A AIM controlling the Models 9635, 9615 and 9645.

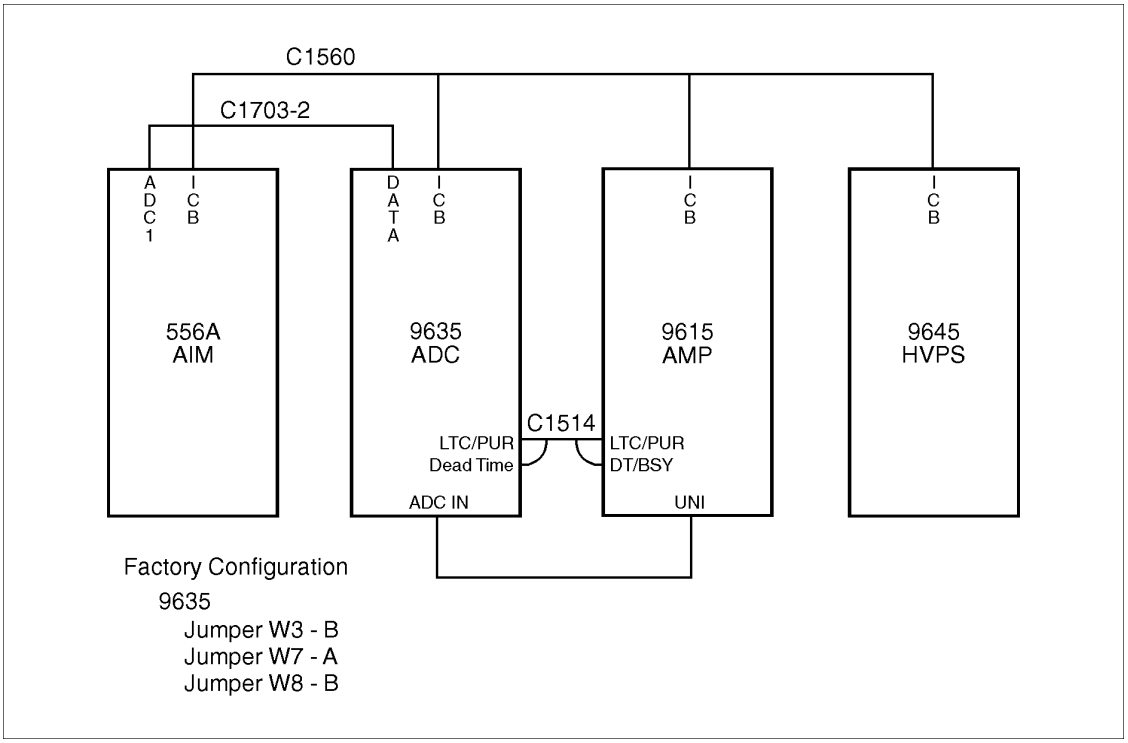


Figure C.1 Typical ICB Bus Installation

C.2 Multiple 556A AIMs in a Network

Figure C.2 shows a system employing several AIM modules in a network, each controlling more than one ICB ADC.

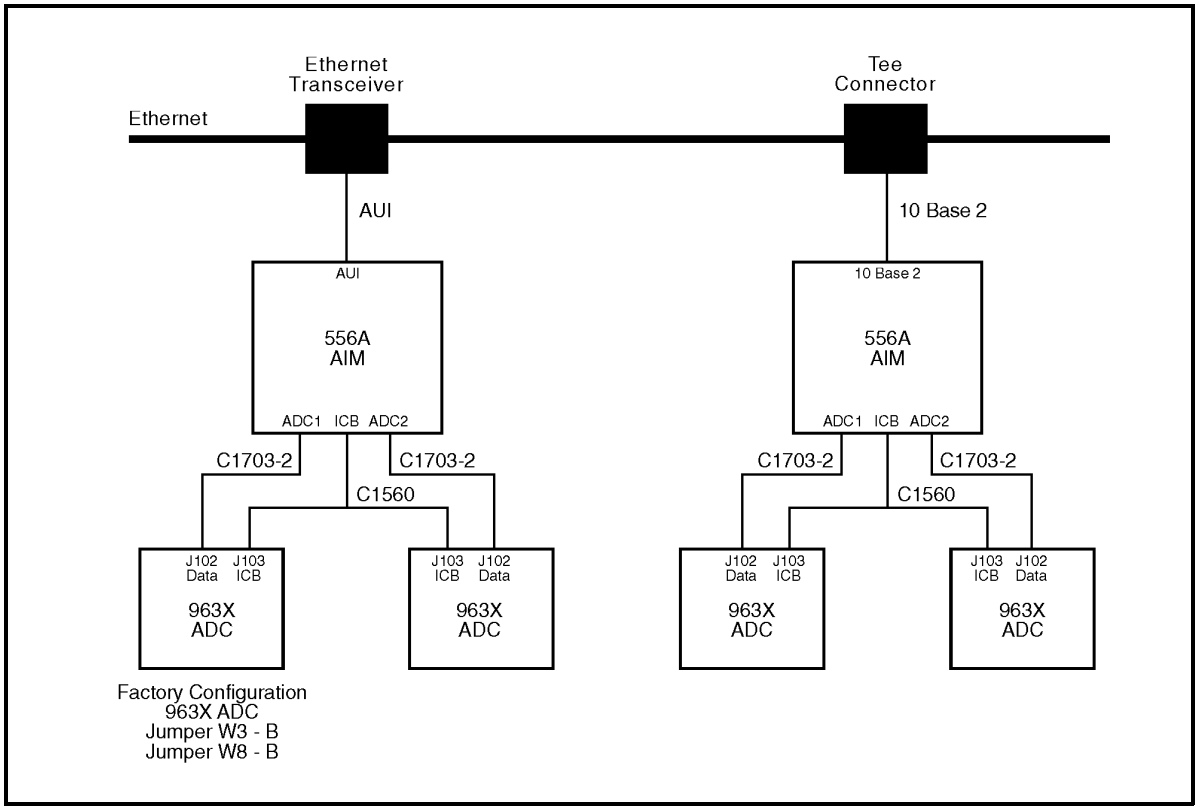
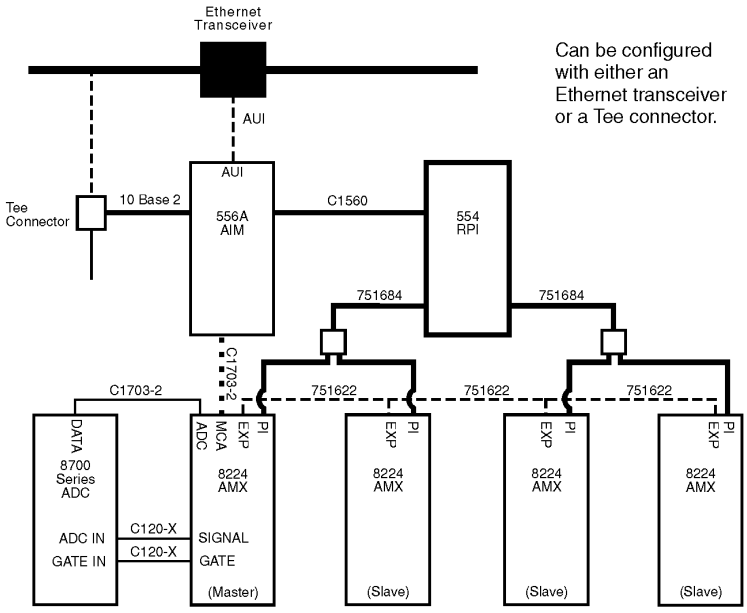


Figure C.2 Multiple 556 AIMs in a Network

C.3 556A AIM with 554 RPI and AMX Modules

Figure C.3 shows a multi-input system implemented with a 556A AIM module and 554 RPI and AMX modules.



AIM-AMX Connection
Each AIM is supplied with two C1703-2 Interface Cables.

ADC-AMX Connections
Each 8224 AMX is supplied with one C1703-2 Interface Cable.

The C120-X Coax Cables for the Signal and Gate connections must be purchased separately.

AMX Master-Slave Connection
Each slave requires a 751622 Expansion Cable, which must be purchased separately.

Independent Start/Stop for the 8224 AMXs
This option requires the purchase of a Model 554 Remote Parallel Interface (RPI) and at least one 751684 cable assembly. Each 751684 Cable Assembly supports two 8224s and each RPI supports 2 such cable assemblies. If independent start/stop is not required, 8223 AMXs may be substituted.

Note: The number and type of AMX modules supported is limited by the software platform being used. Please refer to the appropriate manual for information.

Internal Jumpers

8223	8224	8701	8706	8713/8715/9633/9635	96XX ADC can be Substituted with the Addition of the ICB Cable C1560 Connection.
W1 - Installed W2 - B Internal Switches set for Group Size, Number of Inputs, etc. Refer to 8223 Manual.	J1 - ENC* W1 - Removed W2 - Installed Internal Switches set for Group Size, Number of Inputs, etc. Refer to 8224 Manual.	J1 - ENC* J3 - NEG J8 - B PHA/SVA - SVA AUTO/DELAYED - Delayed COINC/ANTI - Coinc ADJ - Full CCW	J4 - B J5 - ENC* J9 - NEG PHA/SVA - SVA AUTO/DELAYED - Delayed COINC/ANTI - Coinc ADJ - Full CCW	W3 - B W8 - B PHA/SVA - SVA AUTO/DELAYED - Delayed COINC/ANTI - Coinc ADJ - Full CCW	

Figure C.3 556 AIM Setup with 554 RPI

D. Field Installing the Option Cables

The cables for either the Start/Stop Option or the Sample Changer Option are normally installed at the factory. If you need to install either of these cables in the field, follow the steps in ”Installing the Cable”, below, then proceed to the final two steps for the option, which tell you how to connect the cables.

Installing the Cable

1. Remove the five screws holding the 556A side cover to the Module frame, then remove the side cover.
2. At the rear of the module remove the two screws holding the Cable Clamp for the ADC2 cable to the Module frame.
3. Remove the Cable Clamp.
4. Insert the 10-pin header of the Sample Changer cable or Start/Stop cable into J7 (labeled SAMP CHG on the circuit board).
5. Place the cable’s two BNC connectors on top of the 34-pin ribbon cable of ADC2 outside of the Module.
6. Place the Cable Clamp in place over the two screw holes in the Module frame.
7. Insert the screws and tighten lightly.
8. Make sure in the process of tightening the screws that the two BNC cables are spread apart.
9. Replace the Module cover and its five screws.

Connecting the Sample Changer Cables

1. Connect the Sample Changer’s READYOUT connector to the 556A’s READY connector.
2. Connect the 556A’s ADVANCE connector to the Sample Changer ADVANCE IN connector.

Connecting the Start/Stop Cables

1. Connect the START/STOP OUTPUT for ADC Port 1 to the 556A’s SS1 input.
2. Connect the START/STOP OUTPUT for ADC Port 2 to the 556A’s SS2 input.

E. Interface Technical Information

The 556A has two Sample Changer–Start/Stop interfaces for each ADC input channel. This appendix is a technical description of each interface. See Appendix F, “Ethernet Command Set”, for further information.

Interface Toggle Rate

This interface is interrupt driven with a maximum toggle rate (change rate) of 100 Hz (10 ms). This rate is the result of the latency of the 80C186 interrupts and the resolution of the time clocks of the 556A (10 ms).

E.1 Interface Signals

The Sample Changer–Start/Stop Interface includes the following signals:

READY IN

Input pulse of programmable polarity used by the Sample Changer Interface to begin acquisition. Normally TTL logic 1 will indicate a ready condition.

STOP*

Negative edge used to start and stop acquisition. Each negative edge of this signal shall cause acquire to toggle on/off for the given ADC channel.

ADVANCE

Output used by the Sample Changer Interface to change sample positions. Duration is 150 ms (active state) the polarity of this signal is user programmable. Normally TTL logic 0 will indicate an advance condition out to the sample changer.

Interface Selection and Polarity

Interface Selection and Polarity is user programmable. The Sample Changer option is provided only for channel 1 by way of an option cable. The Start/Stop option is provided through another cable with Start/Stop signals provided for both channels.

E.2 Sample Changer Timing

This function is Host driven. The hardware provides only the interface logic/registers required for communicating with the Sample Changer.

1. MCA arms channel by turning acquire on.
2. READYIN pulse turns acquire on (Host will poll READYIN to determine this).
3. Acquire runs to preset.
4. ADVANCE is issued for 150 ms, return to 1 (Host will set/reset ADVANCE).

E.3 Start/Stop Timing

The logic supports either firmware-driven acquisition control or hardware-driven acquisition control. Currently acquisition control is firmware-driven.

1. MCA arms channel by turning acquire on.
2. Each negative edge of STOP* changes the ADC channel acquire state as follows:

   Start Mode: Negative edge of STOP* starts and runs acquisition to preset.

   Stop Mode: Negative edge of STOP* stops acquisition.

   Start/Stop Mode: Each Negative edge of STOP* toggles the MCA Acquire on/off.

F. Ethernet Command Set

This appendix defines the Ethernet command set for both the Sample Changer and Start/Stop AIM options.

F.1 Sample Changer Interface

The Sample Changer interface is Host controlled via the Ethernet Commands given below. Ready Input and Advance Output signal polarities are host programmable. The default signals are:

Ready Input – active TTL high.
Advance Output – active TTL Low.

Set Sample Changer Command (To AIM)

Channel	(0 = Channel 1, 1 = Channel 2)
Advance Polarity	(0 = non-invert, 1 = invert)
Ready Polarity	(0 = non-invert, 1 = invert)

Return Sample Changer Status (To AIM)

Channel	(0 = Channel 1, 1 = Channel 2)

Sample Changer Status Response (From AIM)

Advance Polarity	(0 = non-invert, 1 = invert)
Ready Polarity	(0 = non-invert, 1 = invert)
Ready Status	(0 = not ready, 1 = ready)
Advance Status	(0 = advance off, 1 = advance on)

Return Ready Status (To AIM)

Channel	(0 = Channel 1, 1 = Channel 2)

Ready Status Response (From AIM)

Status	(0 = Not ready, 1 = Ready)

Advance (To AIM)

Channel	(0 = Channel 1, 1 = Channel 2)
State	(1 = On, 0=Off)

F.2 Start/Stop Interface

The Start/Stop interface is a negative TTL edge signal.

Set Start/Stop Status Command (To AIM)

Channel	(0 = Channel 1, 1 = Channel 2)
State	(0 = none, 1 = start only, 2 = stop only, 3 = start/stop)

Return Start/Stop Status (To AIM)

Channel	(0 = Channel 1, 1 = Channel 2)

Start/Stop Status Response (From AIM)

Mode	(0 = none, 1 = start only, 2 = stop only, 3 = start/stop)
Status	(Bit 0 indicates waiting for start: 1 – waiting, 0 – not waiting. Bit 1 indicates acquisition on 1 – on, 0 off)
Time Difference	(Time difference between arming and actual external start)

F.3 Old/New AIM Differentiation

To make use of the Start/Stop Sample Changer Interfaces we can use the Hardware/Firmware Revisions that are returned in the Module Inquiry Ethernet Message.

Old AIM Hardware Revision: 0
Old AIM Firmware Revision: 6 or 5

Any other return values implies a New AIM is in Use. The new AIM will use hardware 1 and firmware 7.

G. Environmental Considerations

This unit complies with all applicable European Union requirements.

Compliance testing was performed with application configurations commonly used for this module; i.e. a CE compliant NIM Bin and Power Supply with additional CE compliant application-specific NIM were racked in a floor cabinet to support the module under test.

During the design and assembly of the module, reasonable precautions were taken by the manufacturer to minimize the effects of RFI and EMC on the system. However, care should be taken to maintain full compliance. These considerations include:

- a rack or tabletop enclosure fully closed on all sides with rear door access
- single point external cable access
- blank panels to cover open front panel Bin area
- compliant grounding and safety precautions for any internal power distribution
- the use of CE compliant accessories such as fans, UPS, etc.

Any repairs or maintenance should be performed by a qualified Canberra service representative. Failure to use exact replacement components, or failure to reassemble the unit as delivered, may affect the unit’s compliance to the specified EU requirements.

Warranty

Canberra's product warranty covers hardware and software shipped to customers within the United States. For hardware and software shipped outside the United States, a similar warranty is provided by Canberra's local representative.

DOMESTIC WARRANTY

Canberra (we, us, our) warrants to the customer (you, your) that equipment manufactured by us shall be free from defects in materials and workmanship under normal use for a period of one (1) year from the date of shipment.

We warrant proper operation of our software only when used with software and hardware supplied by us and warrant that our software media shall be free from defects for a period of 90 days from the date of shipment.

If defects are discovered within 90 days of receipt of an order, we will pay for shipping costs incurred in connection with the return of the equipment. If defects are discovered after the first 90 days, all shipping, insurance and other costs shall be borne by you.

LIMITATIONS

EXCEPT AS SET FORTH HEREIN, NO OTHER WARRANTIES, WHETHER STATUTORY, WRITTEN, ORAL, EXPRESSED, IMPLIED (INCLUDING WITHOUT LIMITATION, THE WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE) OR OTHERWISE, SHALL APPLY. IN NO EVENT SHALL CANBERRA HAVE ANY LIABILITY FOR ANY SPECIAL, INDIRECT OR CONSEQUENTIAL LOSSES OR DAMAGES OF ANY NATURE WHATSOEVER, WHETHER AS A RESULT OF BREACH OF CONTRACT, TORT LIABILITY (INCLUDING NEGLIGENCE), STRICT LIABILITY OR OTHERWISE.

EXCLUSIONS

Our warranty does not cover damage to equipment which has been altered or modified without our written permission or damage which has been caused by abuse, misuse, accident or unusual physical or electrical stress, as determined by our Service Personnel.

We are under no obligation to provide warranty service if adjustment or repair is required because of damage caused by other than ordinary use or if the equipment is serviced or repaired, or if an attempt is made to service or repair the equipment, by other than our personnel without our prior approval.

Our warranty does not cover detector damage due to neutrons or heavy charged particles. Failure of beryllium, carbon composite, or polymer windows or of windowless detectors caused by physical or chemical damage from the environment is not covered by warranty.

We are not responsible for damage sustained in transit. You should examine shipments upon receipt for evidence of damage caused in transit. If damage is found, notify us and the carrier immediately. Keep all packages, materials and documents, including the freight bill, invoice and packing list.

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