Modbus protocol

DEIF

ALL multi-line 2 TYPES

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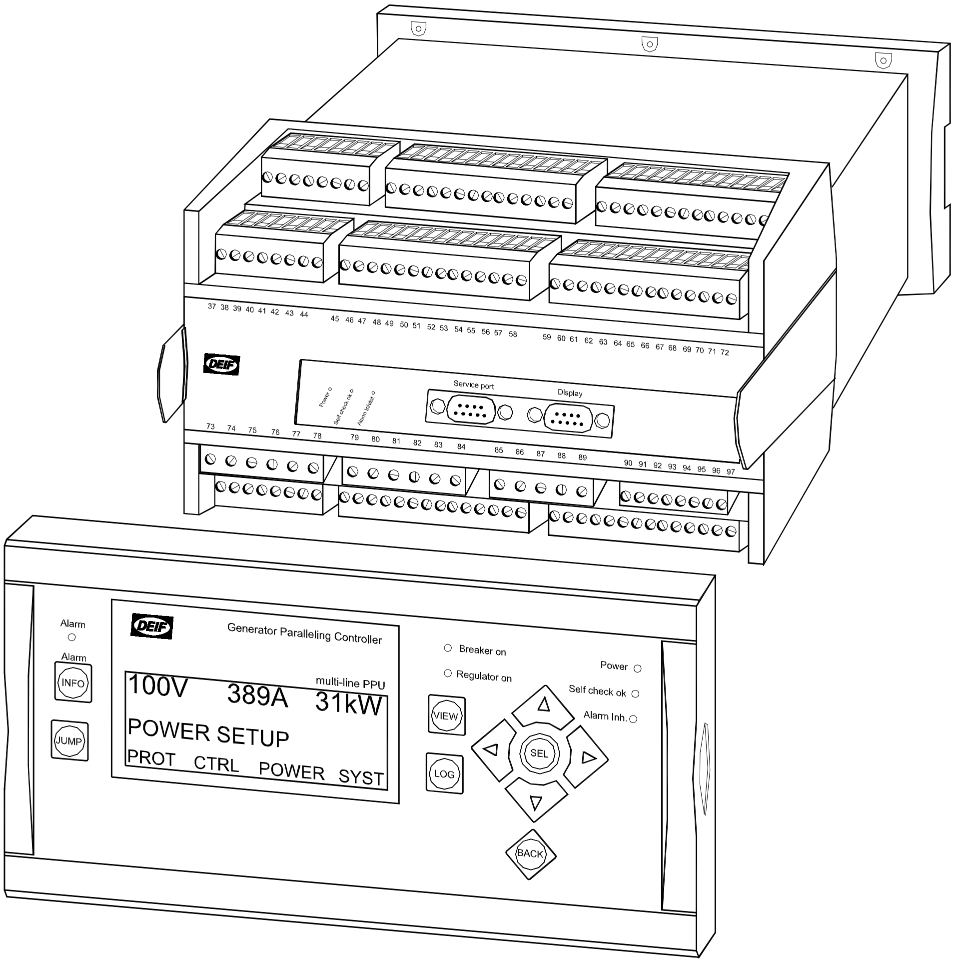

- *RS-485: Modbus RTU*

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CONTENTS

1 General information

1.1 General introduction to *multi-line 2* Modbus

Each message must be transmitted in a continuous stream. Only the RTU mode can be used on *multi-line 2* communication. Broadcast function is not implemented in *multi-line 2* and is therefore not allowed.

Error check field
- Cyclical Redundancy Check (CRC)

***multi-line 2* RS-485 hardware settings**
- 9600 or 19200 bps
- 8 data bits
- None parity
- 1 stop bit

1.2 Transactions on *multi-line 2* Modbus Protocol

Standard Modbus ports on *multi-line 2* use an RS-485 compatible serial interface that defines connector pinouts, cabling, signal levels, transmission baud rates.
Controllers communicate using a master-slave technique in which only one device (the master) can initiate transactions (called "queries"). The other devices (the slaves) respond by supplying the requested data to the master or by taking the action requested in the query.

The Modbus Protocol establishes the format for the master's query by placing into it the device address, a function code defining the requested action, any data to be sent and an error checking field. The slave's response message is also constructed using Modbus Protocol. It contains fields confirming the action taken, any data to be returned and an error checking field. If an error occurred on receipt of the message, an exception response is generated in the slave.

1.3 The query-response cycle

Query
Device address
Function
Eight-bit data byte
Error check (CRC)

Response
Device address
Function
Eight-bit data byte
Error check (CRC)

The query
The function code in the query tells the addressed slave device what kind of action to perform. The data bytes contain any additional information that the slave will need to perform the function. For example, function code 03 will query the slave to read registers and respond with their contents. The data field must contain the information telling the slave which register to start at and how many registers to read. The error check field provides a method for the slave to validate the integrity of the message contents.

The response

If the slave makes a normal response, the function code in the response is an echo of the function code in the query. The data bytes contain the data collected by the slave, such as register values or status. If an error occurs, the function code is modified to indicate that the response is an error response and the data bytes contain a code that describes the error. The error check field allows the master to confirm that the message contents are valid.

1.4 RTU framing

In RTU mode messages start with a silent interval of at least 3.5 character times. This is most easily implemented as a multiple of character times at the baud rate that is being used on the network (shown as T1-T2-T3-T4 in the table below).
The first field then transmitted is the device address.
The allowable characters transmitted for all fields are hexadecimal 0-9, A-F.
Networked devices monitor the network bus continuously, including during the "silent" intervals. When the first field (the address field) is received, each device decodes it to find out if it is the addressed device.
Following the last transmitted character, a similar interval of at least 3.5 character times marks the end of the message. A new message can begin after this interval.
The entire message frame must be transmitted as a continuous stream. If a silent interval of more than 1.5 character times occurs before completion of the frame, the receiving device flushes the incomplete message and assumes that the next byte will be the address field of a new message.
Similarly, if a new message begins earlier than 3.5 character times following a previous message, the receiving device will consider it a continuation of the previous message. This will set an error, as the value in the final CRC field will not be valid for the combined messages. A typical message frame is shown below.

Start	Address	Function	Data	CRC check	End
T1-T2-T3-T4	8 bits	8 bits	N x 8 bits	16 bits	T1-T2-T3-T4

1.5 How the address field is handled

The address field of a message frame contains eight bits. Valid slave device addresses are in the range of 1-247 decimal.
A master addresses a slave by placing the slave address in the address field of the message. When the slave sends its response, it places its own address in the address field of the response to let the master know which slave is responding.
Address 0 is used for the broadcast address.
Broadcasts are not allowed.

1.6 Contents of the error checking field

The RTU mode error checking field contains a 16 bit value implemented as two eight bit bytes. The error check value is the result of Cyclical Redundancy Check calculation performed on the message contents. The CRC field is appended to the message as the last field in the message. When this is done, the low-order byte of the field is appended first, followed by the high-order byte. The CRC high-order byte is the last byte to be sent in the message.
Additional information about error checking follows later in this chapter.

1.7 How characters are transmitted serially

When messages are transmitted on standard Modbus serial networks, each character or byte is sent in this order (left to right):

Least Significant Bit (LSB) ... Most Significant Bit (MSB).

With RTU character framing, the bit sequence is:
Without parity checking.

Start	1	2	3	4	5	6	7	8	Stop

Note: No even or odd parity checking is supported.

1.8 Error checking methods

In RTU mode messages include an error checking field that is based on a Cyclical Redundancy Check (CRC) method. The CRC field checks the contents of the entire message. The CRC field is two bytes, containing a 16 bit binary value. The CRC value is calculated by the transmitting device which appends the CRC to the message.
The receiving device recalculates a CRC during receipt of the message and compares the calculated value to the actual value it received in the CRC field. If the two values are not equal, an error results.
Only the eight bits of data in each character are used for generating the CRC. Start and stop bits do not apply to the CRC.
When the CRC is appended to the message, the low-order byte is appended first, followed by the high-order byte. The master is configured by the user to wait for a predetermined time-out interval before aborting the transaction. This interval is set to be long enough for any slave to respond normally. If the slave detects a transmission error, the message will not be acted upon. The slave will not construct a response to the master. Thus the time-out will expire and allow the master's program to handle the error.
Note that a message addressed to a non-existent slave device will also cause a time-out.

2 Functions

2.1 Function 01(01hex) read flag status

Reads the ON/OFF status of discrete flags in the slave.

Address area for reading of status flags

multi-line 2 **Data to request**	***multi-line 2*** **Table**	**Address area**
Status	Status table	0-499
Alarm active	Set-point table	500-999
Alarm acknowledge	Set-point table	1000-1499
Digital input	Digital input table	1500-1599
Digital output	Digital output table	2000-2499
Timer output	Set-point table	2500-2999
Timer running	Set-point table	3000-3499
Enable	Set-point table	3500-3999

*) The max. number of data query is limited of the length of the actual table.

The query message specifies the stating flag and quantity of flags to be read. Example of a query to read 10...22 from *multi-line 2* slave device 4:

Index	Field name	Example
0	Slave address	04h
1	Function	01h
2	Starting address Hi	00h
3	Starting address Lo	0Ah
4	Number of flags Hi	00h
5	Number of flags Lo	0Dh
6	Error check (CRC) Lo	C4h
7	Error check (CRC) Hi	0Bh

Response
The flag status response message is packed as one flag per bit of the data field. Status is indicated as: 1 is the value ON, and 0 is the value OFF. The LSB of the first data byte contains the flag addressed in the query. The other flags follow toward the high-order end of this byte and from low order to high order in subsequent bytes. If the returned flag quantity is not a multiple of eight, the remaining bits in the final data byte will be padded with zeroes (toward the high-order end of the byte). The byte count field specifies the quantity of complete bytes of data.

Example of a response to the query:

Index	Field name	Example
0	Slave address	04h
1	Function	01h
2	Byte count	02h
3	Data (flags 17...10)	CDh
4	Data (flags 27...20)	1Bh
8	Error check (CRC) Lo	C4h
9	Error check (CRC) Hi	0Bh

The status of flags 17...10 is shown as the byte value CD hex or binary 1100 1101. Flag 17 is the MSB of this byte, and flag 10 is the LSB. Left to right, the status of flags 17...10 is:
ON-ON-OFF-OFF-ON-ON-OFF-ON.

2.2 Function 03(03hex) read registers

Reads the binary of registers in the slave.

Address area for reading of registers

multi-line 2 **Data to request**	***multi-line 2*** **Table**	**Address area**
Measuring values	Measuring values table	0-499
Timers used	Set-point table	500-999
Timers minimum	Set-point table	1000-1499
Timers maximum	Set-point table	1500-1599
Values used	Set-point table	2000-2499
Values minimum	Set-point table	2500-2999
Values maximum	Set-point table	3000-3499
Output a	Set-point table	5000-5499
Output b	Set-point table	9000-9499

*) The max. number of data query is limited of the length of the actual table or max. 100.

Query
The query message specifies the stating register and quantity of registers to be read. Example of a request to read 0...1 from *multi-line 2* slave device 1:

Index	**Field name**	**Example**
0	Slave address	01h
1	Function	03h
2	Starting address Hi	00h
3	Starting address Lo	00h
4	Number of registers Hi	00h
5	Number of registers Lo	02h
6	Error check (CRC) Lo	C4h
7	Error check (CRC) Hi	0Bh

Response
The register data in the response message are packed as two bytes per register, with the binary contents right justified within each byte. For each register the first byte contains the high-order bits, and the second contains the low-order bits.

Example of a response to the query:

Index	Field name	Example
0	Slave address	01h
1	Function	03h
2	Byte count	04h
3	Data Hi	00h
4	Data Lo	06h
5	Data Hi	00h
6	Data Lo	05h
7	Error check (CRC) Lo	C4h
8	Error check (CRC) Hi	0Bh

The contents of register 0 are shown as the two byte values of 00 06 hex. The contents of register 1 are 00 05 hex.

2.3 Function 15(0Fhex) write multiple flags

Writes each flag (0 x reference) in a sequence of flags to either ON or OFF.

Address area for writing of status flags

multi-line 2 **Data to request**	***multi-line 2*** **Table**	**Address area**
Commands	Command table	0-499
Alarm acknowledge	Set-point table	1000-1499
Enable	Set-point table	3500-3999

*) The max. number of data query is limited of the length of the actual table.

Query
The query message specifies the flag references to be forced.
The requested ON/OFF status is specified by contents of the query data field. A logical 1 in a bit position of the field requests the corresponding flag to be ON – A logical = requests it to be OFF. The following page shows an example of a request to force a series of ten flags stating a flag in slave device 1. The query data contents are two bytes: 01 04 hex (1001 0000 binary). The binary bits correspond to the flags in the following way:
Bit: 0 1 1 0 0 0 0 0 1 0 0 1 0 0 0 0
Flag: 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
The first byte transmitted (0 hex) addresses flags 7...0, with the least significant bit addressing the lowest flag (0) in this set.
The next byte transmitted (01 hex) addresses flags 14 and 8, with the least significant bit addressing the lowest flag (8) in the set. Unused bits in the last data byte should be zero-filled.

Example for *multi-line 2* slave device 1:

Index	Field name	Example
0	Slave address	01h
1	Function	0Fh
2	Flag address Hi	01h
3	Flag address Lo	00h
4	Number of flags Hi	00h
5	Number of flags Lo	0Fh
6	Byte count	02h
7	Force data (7...0)	90h
8	Force data (14...8)	60h
9	Error check (CRC) Lo	C4h
10	Error check (CRC) Hi	0Bh

Response
The normal response returns the slave address, function code, starting address and quantity of flags forced. Here is an example of a response to the query shown above.

Index	Field name	Example
0	Slave address	01h
1	Function	0Fh
2	Flag address Hi	01h
3	Flag address Lo	00h
4	Number of flags Hi	00h
5	Number of flags Lo	0Fh
6	Error check (CRC) Lo	14h
7	Error check (CRC) Hi	33h

2.4 Function 16(10hex) write register

Writes values into a sequence of registers.

Address area for writing of registers

multi-line 2 **Data to request**	***multi-line 2*** **Table**	**Address area**
Control	Control table	0-499
Timers used	Set-point table	500-999
Values used	Set-point table	2000-2499

*) The max. number of data query is limited of the length of the actual table and max. 100.

Example of a request to preset two registers starting at timer no to 00 60 and 00 70 hex, in slave *multi-line 2* device 1:

Index	Field name	Example
0	Slave address	01h
1	Function	10h
2	Starting address Hi	01h
3	Starting address Lo	28h
4	Number of registers Hi	00h
5	Number of registers Lo	02h
6	Byte count	04h
7	Data Hi	00h
8	Data Lo	60h
9	Data Hi	00h
10	Data Lo	70h
11	Error check (CRC) Lo	FCh
12	Error check (CRC) Hi	FBh

Response

The normal response returns the slave address. Function code, starting address and quantity of registers preset.

Example of a response to the query shown above:

Index	Field name	Example
0	Slave address	01h
1	Function	10h
2	Starting address Hi	01h
3	Starting address Lo	28h
4	Number of registers Hi	00h
5	Number of registers Lo	02h
6	Error check (CRC) Lo	C0h
7	Error check (CRC) Hi	3Ch

3 Exception

3.1 Exception reception

When a master device sends a query to a slave device, it expects a normal response. One of four possible events can occur from the master's query:

If the slave device receives the query without a communication error and can handle the query normally, it returns a normal response.

If the slave does not receive the query due to a communication error, no response is returned. The master program will eventually process a time-out condition for the query.

If the slave receives the query, but detects a communication error (CRC), no response is returned. The master program will eventually process a time-out condition for the query.

If the slave receives the query without a communication error, but cannot handle it (for example if the request is to read a non-existent register), the slave will return an exception response informing the master of the nature of the error.

The exception response message has two fields that differentiate it from a normal response:

Function code field: In a normal response the slave echoes the function code of the original query in the function code field of the response. All function codes have a most-significant bit (MSB) of 0. This makes the function code value in an exception response exactly 80 hexadecimal higher than the value would be for a normal response.
With the function code's MSB set, the master's application program can recognize the exception response and can examine the data field for the exception code.

Data field: In a normal response the slave may return data or statistics in the data field (any information that was requested in the query). In an exception response the slave returns an exception code in the data field. This defines the slave condition that caused the exception.

Example of a master query and slave exception response:

Query

Index	Field name	Example
0	Slave address	01h
1	Function	03h
2	Starting address Hi	07h
3	Starting address Lo	03h
4	Number of registers Hi	00h
5	Number of registers Lo	02h
6	Error check (CRC) Lo	C0h
7	Error check (CRC) Hi	3Ch

Response

Index	Field name	Example
0	Slave address	01h
1	Function	83h
2	Exception code	02h
7	Error check (CRC) Lo	C0h
8	Error check (CRC) Hi	F1h

The master addresses a query to slave device 01h. The function code (03) is for a *Read Registers*, it requests the status of the register at an address which is out of range.

3.2 Exception codes

Code	Field name	Meaning
01h	Illegal function	The function code received in the query is not an allowable action for the slave
02h	Illegal data address	The data address received in the query is not an allowable address for the slave
03h	Illegal data value	A value contained in the query data fields is not an allowable value for the slave

4 Data tables

4.1 Measurement table (read only)

Address	Content	Type
0		Application version
1	U_{L1-L2}	Generator voltage. Measured in [V]
2	U_{L2-L3}	Generator voltage. Measured in [V]
3	U_{L3-L1}	Generator voltage. Measured in [V]
4	U_{L1-N}	Generator voltage. Measured in [V]
5	U_{L2-N}	Generator voltage. Measured in [V]
6	U_{L3-N}	Generator voltage. Measured in [V]
7	F_{GEN}	Generator frequency. Measured in [Hz/100]
8	I_{L1}	Generator current. Measured in [A]
9	I_{L2}	Generator current. Measured in [A]
10	I_{L3}	Generator current. Measured in [A]
11	Cos-phi	-99...0...100 Generator cosinus-phi. Measured in cos-phi:100 Negative value means capacitive cos-phi
12	P_{GEN}	Generator active power. Measured in [W]. Negative value means reverse power
13	Q_{GEN}	Generator reactive power. Measured in [var]. Positive value means generated inductive reactive power
14	$U_{BBL1-L2}$	Busbar. Measured in [V]
15	F_{BB}	Busbar frequency L1. Measured in [Hz/100]
16 [HI]	Exp. U_{GEN}	Exponent generator voltage
16 [LO]	Exp. I_{GEN}	Exponent generator current
17 [HI]	Exp. P/Q_{GEN}	Exponent generator power/reactive power
17 [LO]	Exp. U_{BB}	Exponent busbar voltage
18 [HI] 19 [LO]	E_{GEN}	Energy counter. Measured in [kWh]. Max. 300000MWh NOT YET IMPLEMENTED. (Version 1.42)
20	Alarms	Bit 0 1010. U-BB High step 1 Bit 1 1020. U-BB High step 2 Bit 2 1030. U-BB Low step 1 Bit 3 1040. U-BB Low step 2 Bit 4 1050. f-BB High step 1 Bit 5 1060. f-BB High step 2 Bit 6 1070. f-BB Low step 1 Bit 7 1080. f-BB Low step 2 Bit 8 1090. Reverse power Bit 9 1100. High current step 1 Bit 10 1110. High current step 2 Bit 11 1120. High power step 1 Bit 12 1130. High power step 2 Bit 13 Unbalance current Bit 14 Unbalance voltage

Address	Content	Type
21	Alarms	Bit 0 Q import Bit 1 Q export Bit 2 df/dt Bit 3 Vector jump Bit 4 2030. Sync. fail. Bit 5 4220. Supply alarm Bit 6 Breaker close fail. Bit 7 Breaker open fail. Bit 8 Breaker position feedback fail. Bit 9 Phase sequence error
22	Alarms	Bit 0 3010. U-DG High step 1 Bit 1 3020. U-DG High step 2 Bit 2 3030. U-DG Low step 1 Bit 3 3040. U-DG Low step 2 Bit 4 3050. f-DG High step 1 Bit 5 3060. f-DG High step 2 Bit 6 3070. f-DG Low step 1 Bit 7 3080. f-DG Low step 2
23	Reserved	
24	Reserved	
25	Reserved	
26	Status	Bit 0 Mode 1 Bit 1 Mode 2 Bit 2 Mode 3 Bit 3 Mode 4 Bit 4 Mode 5 Bit 5 Mode 6 Bit 6 De-load Bit 7 Start sync./reg. Bit 8 Alarm inhibit Bit 9 Breaker position ON Bit 10 Reserved Bit 11 Reserved Bit 12 Reserved Bit 13 Reserved Bit 14 Reserved Bit 15 Reserved
27		Number of alarms
28		Number of unacknowledged alarms
29	U_{DG-max}	Generator max. voltage. Measured in [V]
30	U_{DG-min}	Generator min. voltage. Measured in [V]
31	$U_{BBL2-L3}$	Busbar voltage. Measured in [V]
32	$U_{BBL3-L1}$	Busbar voltage. Measured in [V]
33	U_{BB-max}	Busbar max. voltage. Measured in [V]
34	U_{BB-min}	Busbar min. voltage. Measured in [V]
35	U_{BBL1-N}	Busbar voltage. Measured in [V]
36	U_{BBL2-N}	Busbar voltage. Measured in [V]
37	U_{BBL3-N}	Busbar voltage. Measured in [V]

Address	Content	Type
38	Reserved	
39	Reserved	
40	S_{GEN}	Generator seeming power. Measured in [VA]
41	PHI_{L1-L2}	0...359 Generator phase angle. Measured in [deg]
42	PHI_{L2-L3}	0...359 Generator phase angle. Measured in [deg]
43	PHI_{L3-L1}	0...359 Generator phase angle. Measured in [deg]
44	$PHI_{BBL3-L1}$	0...359 Busbar phase angle. Measured in [deg]
45	$PHI_{BBL1-DGL1}$	0...359 Busbar/generator phase angle. Measured in [deg]
46	df/dt_{BB-L1}	df/dt [Hz/100/s]
47	U_{SUPPLY}	Supply voltage. Measured in [V/10]

4.2 Control register table (write only)

Address	Content	Description
0	Power regulator set-point	0...100% of nominal power Activated in menu 4041
1	PF regulator set-point	60...100 stated as PF value/100. The value 100 means PF = 1 Activated in menu 4045
2	Control command	Bit 0 This bit must be 1 when writing the command word If the bit is 0, the control command is don't care Bit 1 Mode 1 Bit 2 Mode 2 Bit 3 Mode 3 Bit 4 Mode 4 Bit 5 Mode 5 Bit 6 Mode 6 Bit 7 De-load Bit 8 Start sync./reg. Bit 9 Alarm inhibit Bit 10 Alarm ack. This bit is automatically reset in *multi-line 2*
3	Frequency regulator set-point	-50...50Hz/10. Based on nominal frequency Activated in menu 4042
4	Voltage regulator set-point	-100...100%/10 of nominal voltage Activated in menu 4043
5	Reactive power regulator set-point	-100...100% of nominal power. A negative value means capacitive reactive power, and a positive value means inductive reactive power Activated in menu 4044

If terminal 26 "Control via external communication" is activated, the regulators are controlled via the Modbus.
The digital inputs "Alarm ack" and "Alarm inhibit" are always handled even if terminal 26 = ON.
In menu 4040 it is selected, if a set-point is to be controlled by analogue input or by the control registers. (Mode 3 and/or Mode 4 must be on).
It is possible to write to the control registers also when terminal 26 = OFF.
The content of the control registers is not lost in case of supply failure, so frequent updates are not necessary.

Example how to control the frequency via the Modbus:

- Activate terminal 26
- Activate frequency control register in menu 4042
- Write the control command address 2. Bit 1 = ON, Bit 3 = ON, Bit 8 = ON
- Write in the control register address 3 the desired frequency offset

4.3 Command flags table (write only)

Address	Content	Description
0	Mode 1	
1	Mode 2	
2	Mode 3	
3	Mode 4	
4	Mode 5	
5	Mode 6	
6	De-load	
7	Start sync./reg.	
8	Alarm inhibit	
9	Alarm ack.	This bit is automatically reset in *multi-line 2*

Same function as address 2 in the control register table.

4.4 Status flags table (read only)

Address	Content	Description
0	Mode 1	
1	Mode 2	
2	Mode 3	
3	Mode 4	
4	Mode 5	
5	Mode 6	
6	De-load	
7	Start sync./reg.	
8	Alarm inhibit	
9	Breaker pos. on	

Same content as address 26 in the measurement table.

4.5 Parameter table

Offset address	Ch. no.	Content	Unit	Delay	Output a	Output b	Enable
0	-	-	-	-	-	-	-
1	1010	U-BB High step 1	%/10	y	y	y	y
2	1020	U-BB High step 2	%/10	y	y	y	y
3	1030	U-BB Low step 1	%/10	y	y	y	y
4	1040	U-BB Low step 2	%/10	y	y	y	y
5	1050	f-BB High step 1	%/10	y	y	y	y
6	1060	f-BB High step 2	%/10	y	y	y	y
7	1070	f-BB Low step 1	%/10	y	y	y	y
8	1080	f-BB Low step 2	%/10	y	y	y	y
9	1090	Reverse power	%/10	y	y	y	y
10	1100	Over current 1	%/10	y	y	y	y
11	1110	Over current 2	%/10	y	y	y	y
12	1160	Over load 1	%/10	y	y	y	y
13	1170	Over load 2	%/10	y	y	y	y
14	1220	Unbalance curr.	%/10	y	y	y	y
15	1230	Unbalance volt.	%/10	y	y	y	y
16	1240	var import	%/10	y	y	y	y
17	1250	var export	%/10	y	y	y	y
18	1260	df/dt (ROCOF)	Hz/10/s	y	y	y	y
19	1262	df/dt (ROCOF) time	Per	n	y	y	y
20	1270	Vector jump	Deg/10	n	y	y	y
21	1310	DG high volt 1	%/10	y	y	y	y
22	1320	DG high volt 2	%/10	y	y	y	y
23	1330	DG low volt 1	%/10	y	y	y	y
24	1340	DG low volt 2	%/10	y	y	y	y
25	1350	DG high freq 1	%/10	y	y	y	y
26	1360	DG high freq 2	%/10	y	y	y	y
27	1370	DG low freq 1	%/10	y	y	y	y
28	1380	DG low freq 2	%/10	y	y	y	y
29		Reserved	-	-	-	-	-
30		Reserved	-	-	-	-	-
31		Reserved	-	-	-	-	-
32		Reserved	-	-	-	-	-
33		Reserved	-	-	-	-	-
34		Reserved	-	-	-	-	-
35		Reserved	-	-	-	-	-
36		Reserved	-	-	-	-	-

Offset address	Ch. no.	Content	Unit	Delay	Output a	Output b	Enable
37		Reserved	-	-	-	-	-
38		Reserved	-	-	-	-	-
39		Reserved	-	-	-	-	-
40	2016	Sync. df max.	Hz/10	n	n	n	n
41	2017	Sync. df min.	Hz/10	n	n	n	n
42	2018	Sync. DU max.	%	n	n	n	n
43	2019	Sync. t CB	ms	n	n	n	n
44	2026	Blackout df max.	Hz/10	n	n	n	n
45	2027	Blackout dU max.	%	n	n	n	n
46	2028	Blackout enable	n0	n	n	n	y
47	2036	General failure	n1	y	y	y	n
48	2055	Freq. control droop	%/10	n	n	n	n
49	2056	Freq. control DB	%/10	n	n	n	n
50	2057	Freq. control gain	None	n	n	n	n
51	2058	Freq. control time	ms	n	n	n	n
52	2066	Power control DB	%/10	n	n	n	n
53	2067	Power control gain	None	n	n	n	n
54	2068	Power control time	ms	n	n	n	n
55	2076	Power ramp up speed	%/10/s	n	n	n	n
56	2077	Power ramp up point	%	n	n	n	n
57	2086	Power ramp down speed	%/10/s	n	n	n	n
58	2087	Power ramp down point	%	n10	n	n	n
59	2096	P/f control mix factor	None	n	n	n	n
60	2106	Volt control DB	%/10	n	n	n	n
61	2107	Volt control gain	None	n	n	n	n
62	2108	Volt control time	ms	n	n	n	n
63	2116	var control DB	%/10	n	n	n	n
64	2117	var control gain	None	n	n	n	n
65	2118	var control time	ms	n	n	n	n
66	2126	Q/U control mix factor	None	n	n	n	n
67	2136	PF control DB	None	n	n	n	n
68	2137	PF control gain	None	n	n	n	n
69	2138	PF control time	ms	n	n	n	n
70		Reserved	-	-	-	-	-
71		Reserved	-	-	-	-	-
72		Reserved	-	-	-	-	-
73		Reserved	-	-	-	-	-
74		Reserved	-	-	-	-	-

Offset add-ress	Ch. no.	Content	Unit	Delay	Output a	Output b	Enable
75		Reserved	-	-	-	-	-
76		Reserved	-	-	-	-	-
77		Reserved	-	-	-	-	-
78		Reserved	-	-	-	-	-
79		Reserved	-	-	-	-	-
80	3010	Start next					
81	3020	Stop next					
82	4016	Nom. frequency	Hz/10	n	n	n	n
83	4017	Nom. power	kW	n	n	n	n
84	4018	Nom. current	A	n	n	n	n
85	4019	Nom. voltage	V	n	n	n	n
86	4026	Volt prim.	V	n	n	n	n
87	4027	Volt sec.	V	n	n	n	n
88	4028	Current prim.	A	n	n	n	n
89	4029	Current sec.	A	n	n	n	n
90	4031	Control settings P	%	n	n	n	n
91	4032	Control settings var	%	n	n	n	n
92	4033	Control settings PF	None	n	n	n	n
93	4041	Comm. bus control P	n0	n	n	n	y
94	4042	Comm. bus control f	n0	n	n	n	y
95	4043	Comm. bus control U	n0	n	n	n	y
96	4044	Comm. bus control Q	n0	n	n	n	y
97	4045	Comm. bus control P	n0	n	n	n	y
98	4051	Ext. comm. ID	None	n	n	n	n
99	4052	19200 Baud	n0	n	n	n	y
100		Reserved	-	-	-	-	-
101	4090	Ext. comm. error	n1	y	y	y	y
102	4110	Auto det. run	n0	n	n	n	y
103		Reserved	-	-	-	-	-
104		Reserved	-	-	-	-	-
105		Reserved	-	-	-	-	-
106		Reserved	-	-	-	-	-
107		Reserved	-	-	-	-	-
108		Reserved	-	-	-	-	-
109		Reserved	-	-	-	-	-
110		Reserved	-	-	-	-	-
111		Reserved	-	-	-	-	-
112		Reserved	-	-	-	-	-

Offset add-ress	Ch. no.	Content	Unit	Delay	Output a	Output b	Enable
113	4220	Battery low V	V/10	y	y	y	n
114	4231	German language	n0	n	n	n	y
115		Reserved	-	-	-	-	-
116		Reserved	-	-	-	-	-
117		Reserved	-	-	-	-	-
118		Reserved	-	-	-	-	-
119		Reserved	-	-	-	-	-
120	4502	P output type	0 or 4	n	y	n	n
121	4512	S output type	0 or 4	n	y	n	n
122	4522	Q output type	0 or 4	n	y	n	n
123	4532	PF output type	0 or 4	n	y	n	n
124	4542	f output type	0 or 4	n	y	n	n
125	4552	U output type	0 or 4	n	y	n	n
126	4562	I output type	0 or 4	n	y	n	n
127	4503	P output max.	kW	n	n	n	n
128	4513	S output max.	kVA	n	n	n	n
129	4523	Q output max.	var	n	n	n	n
130	4533	PF output max.	None	n	n	n	n
131	4543	f output max.	Hz/10	n	n	n	n
132	4553	U output max.	V	n	n	n	n
133	4563	I output max.	A	n	n	n	n
134	4504	P output min.	kW	n	n	n	n
135	4514	S output min.	kVA	n	n	n	n
136	4524	Q output min.	kvar	n	n	n	n
137	4534	PF output min.	None	n	n	n	n
138	4544	f output min.	Hz/10	n	n	n	n
139	4554	U output min.	V	n	n	n	n
140	4564	I output min.	A	n	n	n	n
141		Reserved	-	-	-	-	-
142		Reserved	-	-	-	-	-
143		Reserved	-	-	-	-	-
144		Reserved	-	-	-	-	-
145		Reserved	-	-	-	-	-
146		Reserved	-	-	-	-	-
147		Reserved	-	-	-	-	-
148	4976	Password	None	n	n	n	n
149		Reserved	-	-	-	-	-

Refer to the user's manual of your *multi-line* for information on:

- Availability of channels
- Min./max. settings
- Factory settings

Note that several channels also depend on the options.

However, it is possible to write to channels where the option is not set, it is not possible to enable the channel. E.g. if an attempt is made to write a "1" to the enable flag, the "1" will be discarded, and the enable flag remains "0".
It is not possible to write to offset 0. These values are used for DEIF internal version control.

"y" means that the channel is writeable.
"n" means that a "0" can be written to the channel only.
"n10" means that only the value 10 can be written.

Examples:

- Write nominal frequency (4016) 60Hz

ID = 1, 60Hz = 600Hz/10 = 0258h
Address 2000 + 80 = 2080d = 0820h
Tx: 01h 10h 08h 20h 00h 01h 02h 02h 58h 28h 6Ah
Rx: 01h 10h 08h 20h 00h 01h 02h 63h

- Read nominal frequency (4016) 60Hz

Tx: 01h 03h 08h 20h 00h 01h 87h A8h
Rx: 01h 03h 02h 02h 58h B8h DEh
Read 0258h = 600d

4.6 Digital input table

Address	Terminal	Description
1500 - 27	-	Reserved for digital input PCB 1 - 4
1528	43	De-load
1529	44	Man. governor up
1530	45	Man. governor down
1531	46	Man. AVR up
1532	47	Man. AVR down
1533	48	Mode 1
1534	49	Mode 2
1535	50	Mode 3
1536	51	Mode 4
1537	52	Mode 5
1538	53	Mode 6
1539	54	Breaker position off
1540	55	Breaker position on
1541	23	Alarm inhibit
1542	24	Alarm acknowledge
1543	25	Sync. start
1544	26	Control via external communication
1545	27	Block loss of mains

4.7 Digital output table

Address	Terminal	Description
2000 - 2001	-	Not used
2002	126/127	AVR down
2003	128/129	AVR up
2004 - 2015	-	Not used
2016	57/58	Governor up
2017	59/60	Governor down
2018	Depends on type	Start
2019	Depends on type	Stop
2020	-	Not used
2021	-	Not used
2022	-	Not used
2023	-	Not used
2024	-	Not used
2025	5/6	Relay 1
2026	8/9	Relay 2
2027	11/12	Relay 3
2028	14/15	Relay 4
2029	17/18	Relay 5 (on in short time)

Errors and changes excepted