ROBO-8210VG2AR

Single Board Computer

User's Manual

Version 1.1

Table of Contents

How to Use This Manual

How to Use This Manual

The manual describes how to configure your ROBO-8210VG2AR system to meet various operating requirements. It is divided into five chapters, with each chapter addressing a basic concept and operation of Single Board Computer.

Chapter 1 : System Overview. Presents what you have in the box and give you an overview of the product specifications and basic system architecture for this model of single board computer.

Chapter 2 : Hardware Configuration. Shows the definitions and locations of Jumpers and Connectors that you can easily configure your system.

Chapter 3 : System Installation. Describes how to properly mount the CPU, main memory and M-systems flash disk to get a safe installation and provides a programming guide of Watch Dog Timer function.

Chapter 4 : BIOS Setup Information. Specifies the meaning of each setup parameters, how to get advanced BIOS performance and update new BIOS. In addition, POST checkpoint list will give users some guidelines of trouble-shooting.

Chapter 5 : Troubleshooting. Provides you a few useful tips to quickly get your ROBO-8710VLA running with no failure. As basic hardware installation has been addressed in Chapter 3, this chapter will basically focus on system integration issues, in terms of backplane setup, BIOS setting, and OS diagnostics.

The content of this manual and EC declaration document is subject to change without prior notice. These changes will be incorporated in new editions of the document. **Portwell** may make supplement or change in the products described in this document at any time.

Updates to this manual, technical clarification, and answers to frequently asked questions will be shown on the following web site : http://www.portwell.com/.

Chapter 1
System Overview

1.1 Introduction

ROBO-8210VG2AR, the PICMG 1.3 SHB (Single Host Board) combined with either the Intel® Core i7-620M/i5-520M/P4500 processor. The attractive Core i processor does not only posses amazing parallel computing power but also generates only 35W TDP (Thermal Design Power). That makes the system more powerful and reliable with smaller and quieter cooling fan.

The SHB adopted Intel® QM57 chipset. The QM57 embedded Graphics Media Accelerator HD is the latest generation Intel integrated graphics controller that can supports 3D multimedia capabilities including Microsoft DirectX 10, Shader Model 4.0, MPEG-2 and OpenGL 2.1. More than that, user could utilize even higher-end, the latest PCI Express x16 interface graphics card via backplane. Based on the low-power/high-performance Nehalem micro-architecture, the processor is designed for a two-chip platform, as opposed to the traditional three chip platforms (processor, GMCH, and ICH).

ROBO-8210VG2AR built with dual Intel® Gigabit Ethernet. Two DDR3 DIMM sockets support system memory up to 8GB. Six SATA 300 ports (dual ports via backplane) support RAID 0, 1, 5, 10.

To meet bandwidth of storage and expansion cards requirement, the ROBO-8210VG2AR was designed flexible with five PCI Express lanes via backplane. Those PCI Express lanes could be one PCI Express x16(or two PCI Express x8 links) from CPU and four PCI Express x1 links(or one PCI Express x4 link) from PCH. Four PCI Express x1 links configuration can support more PCI Express x1 devices via backplane and one PCI Express x4 link configuration can support RAID card or special add-on cards such as image processing board. In addition, the flexible configuration can be leveraged with bridge on backplane to support more PCI or PCI-X slots that benefits industries with legacy support.

Advanced Management Technology (AMT) 6.0 is feature that ROBO-8210VG2AR equipped. This technology provides remote access capability via Intel® Gigabit Ethernet controller. The new technology is a hardware-based solution that uses out-of-band communication for system management access to client systems. Beside that, the hardware and software information can be gathering by 3rd party software then storage in SPI interface EEPROM. Therefore, asset management could be done at the same time. ROBO-8210VG2AR also supports iTPM (Intel Trusted Platform Module) function for applications.

ROBO-8210VG2AR features:

- Support Intel i7-620M/i5-520M/P4500 processors in rPGA988 package
- Delivers up to 8GB maximum DDR3 1066/800 on two DIMM sockets
- Support dual display by DVI-I port on bracket
- Support iAMT 6.0 and external TPM via TPM module
- High speed dual Gigabit Ethernet based on PCI Express x1, high bandwidth I/O interface
- Rich I/O connections such as FDD, two Gigabit Ethernet, serial ports, parallel port, USB 2.0
- Four on-board SATA ports support RAID 0,1,5,10

The PICMG 1.3 SHB is the best solution of applications such like flight simulation, image processing, broadcasting and so on that need performance of display and storage.

1.2 Check List

The ROBO-8210VG2AR package should cover the following basic items:

- One ROBO-8210VG2AR single host board
- One dual Serial ports cable kit
- One single Parallel port cable kit
- One FDD cable
- Two 7-pin SATA signal cables
- One DVI-I cable
- One Installation Resources CD-Title

Optional: One bracket with PS/2 keyboard and mouse

If any of these items is damaged or missing, please contact your vendor and keep all packing materials for future replacement and maintenance.

1.3 Product Specification

- **Main processor**

- Intel® Core i7-620M/i5-520M/P4500 Processor

- **BIOS**

AMI system BIOS with SPI Serial CMOS EEPROM with easy upgrade function ACPI, DMI, Green function and Plug and Play Compatible

- **Main Memory**

- Support dual-channel DDR3 memory interface
- Non-ECC, non-buffered DIMMs only
- Two DIMM sockets support 1066/800 DDR3-SDRAM up to 8GB System Memory

- **L2 Cache Memory**

Built-in Processor

- **Chipset**

Intel® QM57 chipset

- **Bus Interface**

- Follow PICMG 1.3 Rev 1.0 standard (PCI Express and PCI)
- Support four PCI Express x1 (can be aggregated as one PCI Express x4) through backplane
- Support one PCI Express x16(can be separated as two PCI Express x8) through backplane
- Support four PCI devices through backplane

- **SATA**

- Four SATA 300 ports on-board and dual SATA 300 ports via backplane
- Support Intel® Matrix Storage Technology based on Intel® QM57

- **Floppy Drive Interface**

Support one FDD port up to two floppy drives and 5-1/4"(360K, 1.2MB), 3-1/2" (720K, 1.2MB, 1.44MB, 2.88MB) diskette format and 3-mode FDD

- **Serial Ports**

Support two high-speed 16C550 compatible UARTs with 16-byte T/R FIFOs

- **Parallel Port**

Support one parallel port with SPP, EPP and ECP modes

- **USB Interface**

Support twelve USB (Universal Serial Bus) ports (two USB ports on bracket that dedicated to keyboard & mouse; six USB ports on-board and four USB ports via backplane) for high-speed I/O peripheral devices

- **PS/2 Mouse and Keyboard Interface**

Support one 10-pin header for external PS/2 keyboard/mouse connection

- **Auxiliary I/O Interfaces**

System reset switch, external speaker, Keyboard lock and HDD active LED, etc

- **Real Time Clock/Calendar (RTC)**

Support Y2K Real Time Clock/Calendar with battery backup for 7-year data retention

- **Watchdog Timer**

- Support WDT function through software programming for enable/disable and interval setting
- Generate system reset

- **On-board VGA**

GMCH integrated graphics, 400MHz core frequency; share system memory up to 1GB for system with greater than or equal to 192MB of system memory

- **On-board Ethernet LAN**

Dual Intel® PCI Express x1 interface based Gigabit Ethernet to support RJ-45 connector

- **High Driving GPIO**

Support 8 programmable high driving GPIO

- **Cooling Fans**

Support one 4-pin power connector for CPU fan and one 3-pin power connector for system fan

- **System Monitoring Feature**

Monitor CPU temperature, system temperature and major power sources, etc.

- **Bracket**

Support dual Ethernet port with 2 indicators, dual USB ports and one DVI port

- **Outline Dimension (L X W):**

338.5mm (13.33") X 126.39mm (4.98")

- **Power Requirements:**

- +12V (CPU)@ 1.37A
- +12V (System)@ 0.31A
- +5V @ 3.58A
- Test Programs: BurnIn Test V5.3
- Run Time: Full loading

- **- Test configuration:**

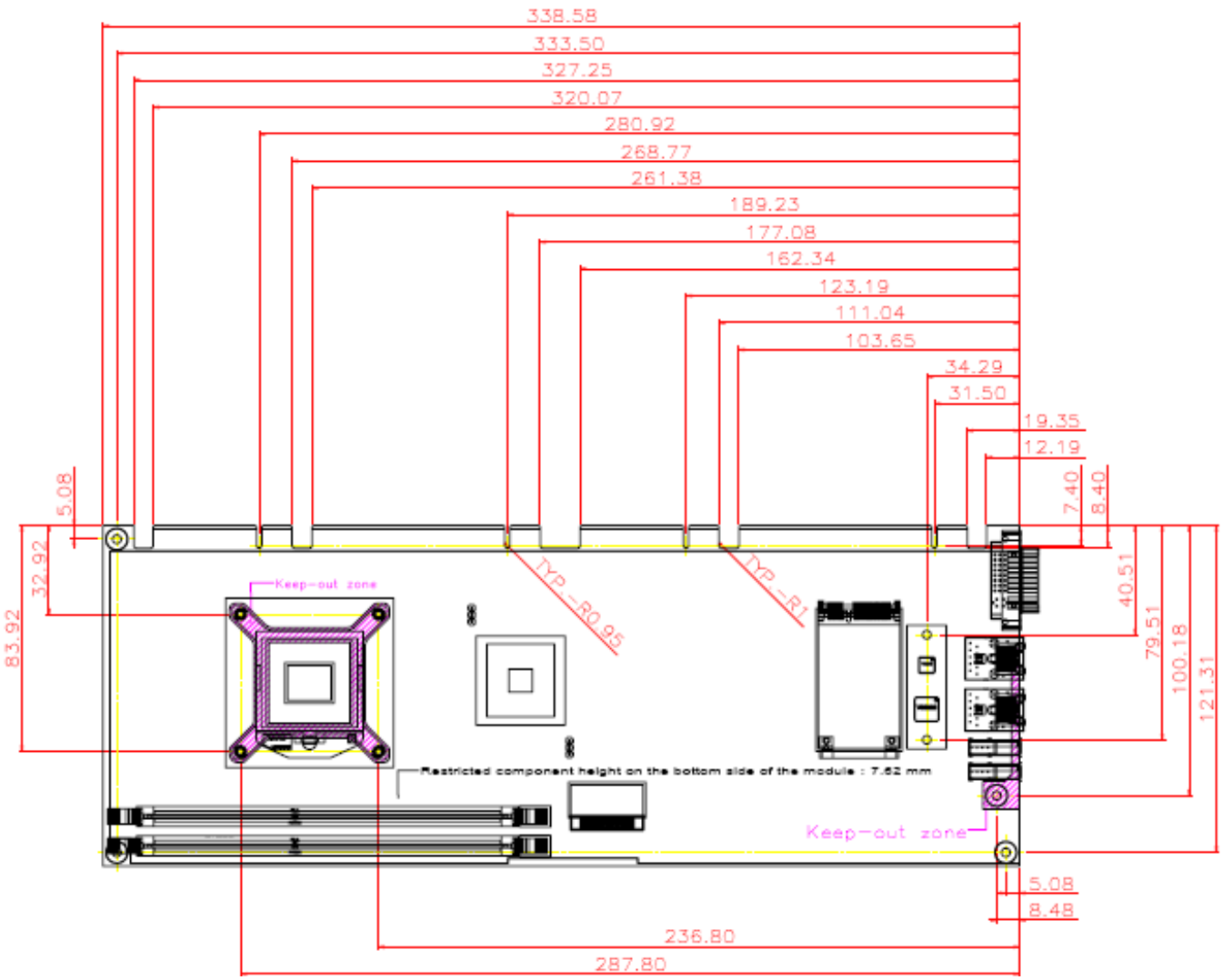
System Configuration	
CPU Type	Intel® Core™ i7 CPU M620 @2.67GHz L3:4MB Bus Speed:133
SBC BIOS	Portwell ,Inc. ROBO-8210VG2AR BIOS Rev.: R1.00.E0 (07142010)
Memory	DDR3 1066 1GB (ELPIDA J1108BABG-DJ-E)
VGA Card	Onboard Intel® QM57
VGA Driver	Intel® Graphics Media Accelerator HD Version 6.14.10.5189
LAN Card #1	Onboard Intel® 82577LM Gigabit Network Connection
LAN Driver	Intel® 82577LM Gigabit Network Connection Version 11.5.10.0
LAN Card #2	Onboard Intel® 82583V Gigabit Network Connection
LAN Driver	Intel® 82583V Gigabit Network Connection Version 11.4.7.0
Audio Card	Onboard Realtek ALC662 Audio
Audio Driver	Realtek High Definition Audio Version 5.10.0.5043
Chip Driver	Intel® Chipset Device Software Version 9.1.1.1025
SATA HDD	Seagate ST3808110AS 80GB
CDROM	LITE-ON LH-20A1S DVD-ROM
Power Supply	Sunpower SPX-6500P1 500W
Back plane	PBPE-13A8 Z201

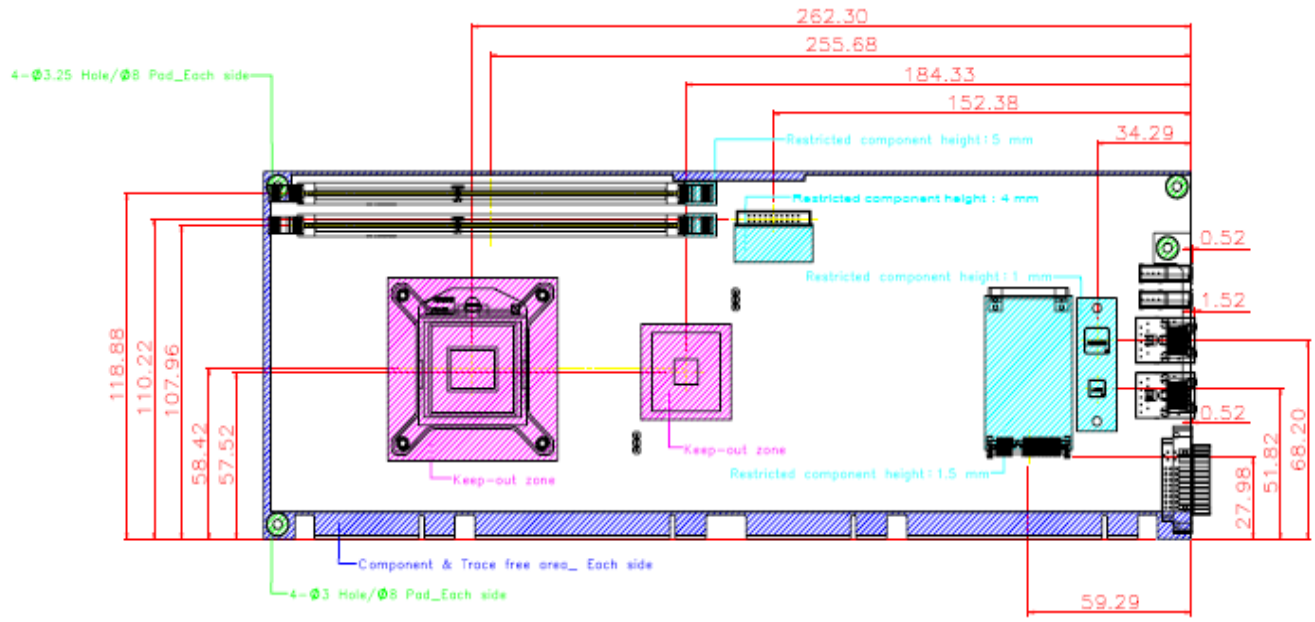
- **Operating Temperature:**
  0°C ~ 60°C (23°F ~ 140°F)

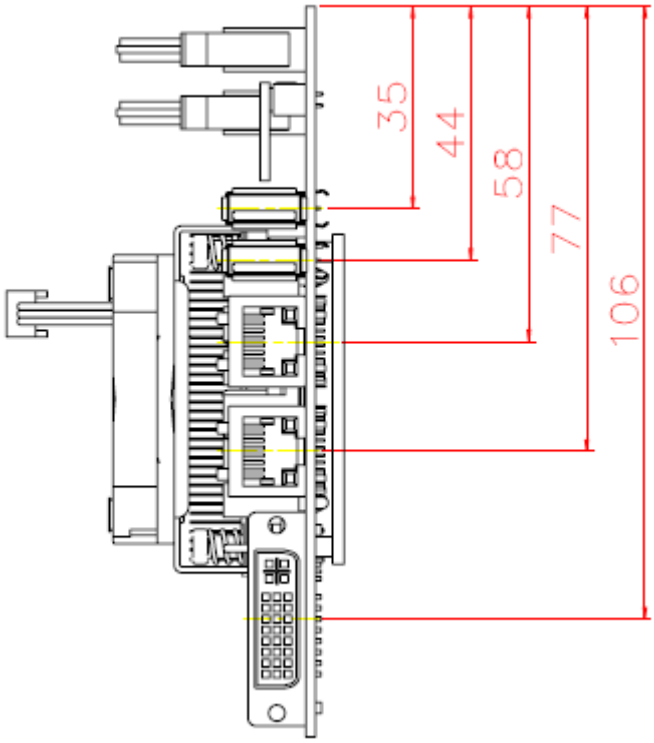
- **Storage Temperature:**
  -20°C ~ 80°C

- **Relative Humidity:**
  5% ~ 90%, non-condensing

1.3.1 Mechanical Drawing



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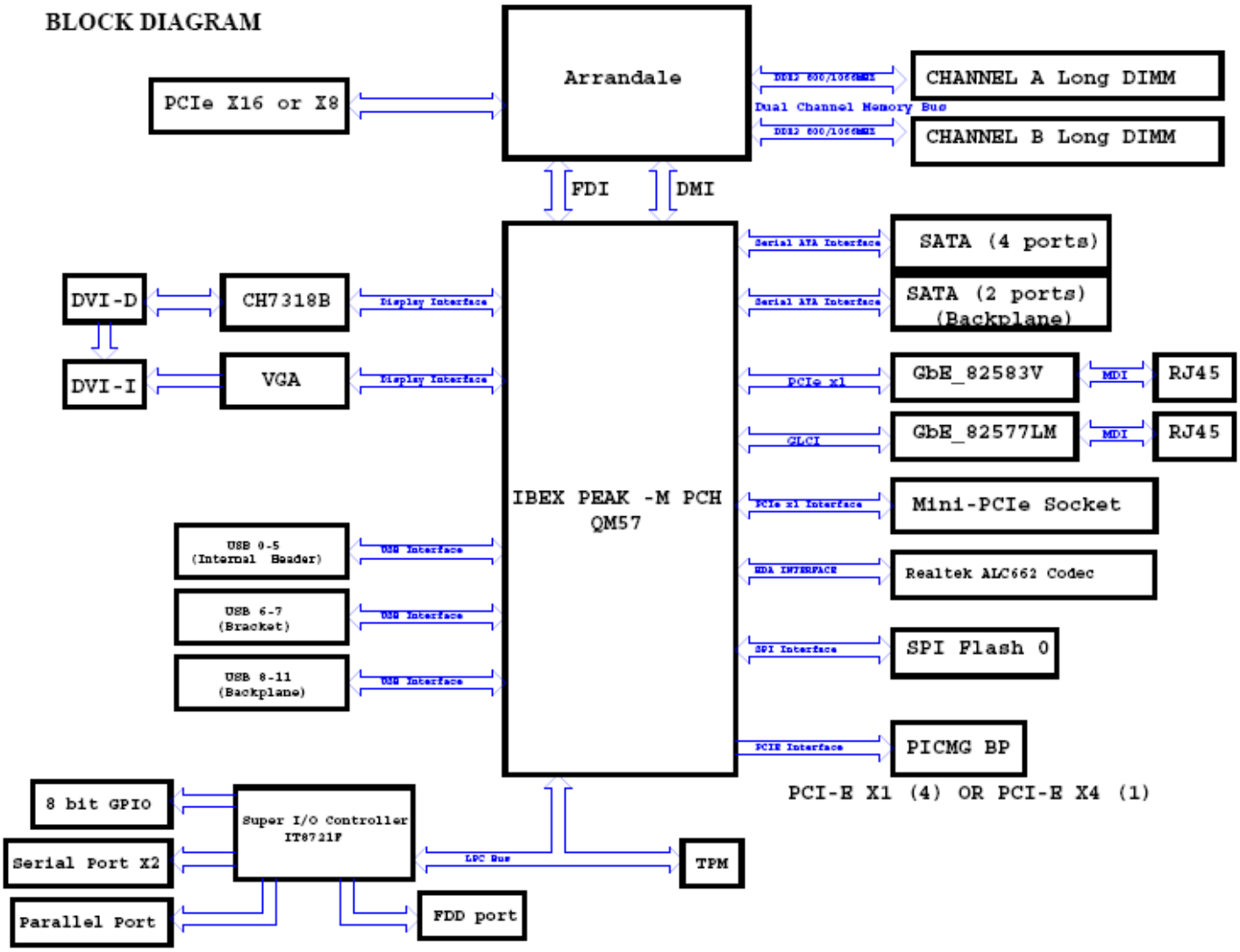
1.4 System Architecture

All of details operating relations are shown in ROBO-8210VG2AR series System Block Diagram



ROBO-8210VG2AR System Block Diagram

Chapter 2
Hardware Configuration

This chapter indicates jumpers', headers' and connectors' locations. Users may find useful information related to hardware settings in this chapter. The default settings are indicated with a star sign (★).

2.1 Jumper Setting

In the following sections, **Short** means covering a jumper cap over jumper pins; **Open** or **N/C** (Not Connected) means removing a jumper cap from jumper pins. Users can refer to Figure 2-1 for the Jumper locations.

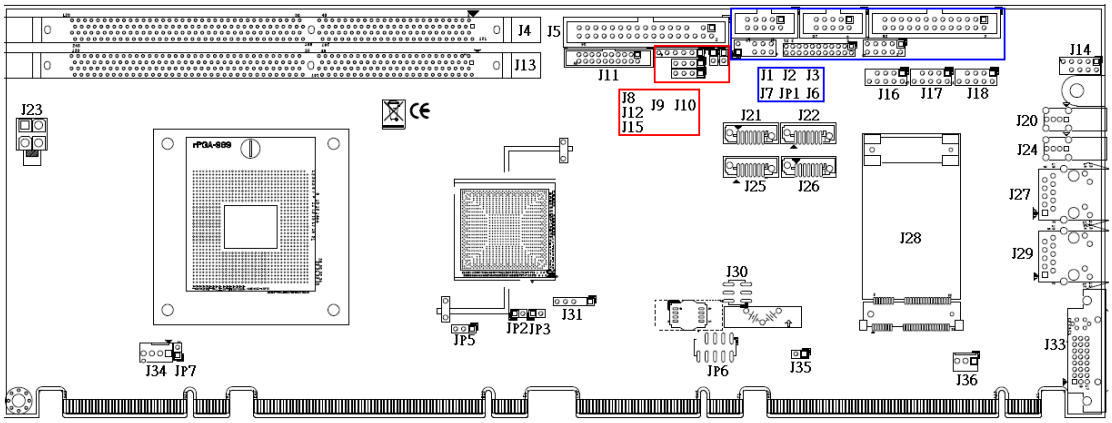


Figure 2-1 ROBO-8210VG2AR Jumper and Connector Locations

The jumper settings are schematically depicted in this manual as follows:

JP1: COM2 RS232, 422, 485 Selection

JP1	Function
5-6,9-11,10-12,15-17,16-18 Short	RS-232
3-4,7-9,8-10,13-15,14-16,21-22 Short	RS-422
1-2,7-9,8-10,19-20 Short	RS-485

JP3: CMOS Clear Header

JP3	Function
1-2 Open	Normal Operation
1-2 Short	Clear CMOS Contents

JP5: PCI_VIO_Selection

JP5	Function
1-2 Short	VCC3
2-3 Short	VCC

JP7: PCI_Express X16 X8_Selection

JP7	Function
1-2 Open	1 x16 PEG
1-2 Short	2 x8 PEG

J35: Auto Power On_Selection

J35	Function
1-2 Open	Normal
1-2 Short	Auto Power On

2.2 Connector Allocation

I/O peripheral devices are connected to the interface connectors.

Connector Function List

Connector	Function	Remark
JP6	LPC Debug Pin header	
J1	COM2 Pin Header	
J2	COM1 Pin Header	
J3	Parallel Port Pin Header	
J4	DDR3 CHB Slot	
J5	FDC Interface Pin Header	
J6	8-bit GPIO Pin Header	
J7	PS2 KB/MS Pin Header	
J8	IR Pin Header	
J9	HDD LED Pin Header	
J10	SUS LED Pin Header	
J11	TPM Pin Header	
J12	Buzzer Pin Header	
J13	DDR3 CHA Slot	
J14	Audio MIC/Line-in/Line-out Pin Header	
J15	LAN LED Pin Header	
J16,J17,J18	USBx2 Pin Header	
J20,J24	Rear USB Connector	
J21,J22,J25,J26	SATA CONNECTOR	
J23	ATX 4P CONNECTOR	

J27, J29	LAN CONNECTOR	
J28	Mini-PCI Express socket	
J30	Second SPI Pin Header	
J31	SM_BUS Pin Header	
J33	DVI-I Connector	
J34	CPU FAN Pin Header	
J36	SYS FAN Pin Header	

Pin Assignments of Connectors

JP6: LPC Debug Pin header

PIN No.	Signal Description	PIN No.	Signal Description
1	LAD0	2	VCC3
3	LAD1	4	PLT_RST#
5	LAD2	6	LFRAME#
7	LAD3	8	CLOCK
9	KEY	10	GND

J1 : COM2 232/422/485 Pin Header

PIN No.	Signal Description			PIN No.	Signal Description		
	RS-232	**RS-422**	**RS-485**		**RS-232**	**RS-422**	**RS-485**
1	DCD#	TX-	DATA-	2	DSR#	TX+	DATA+
3	RXD#	RX+	N/C	4	RTS#	RX-	N/C
5	TXD#	GND	GND	6	CTS#	N/C	N/C
7	DTR#	N/C	N/C	8	RI#	N/C	N/C
9	GND	N/C	N/C	10	NC	N/C	N/C

J2: COM1 Port Pin Header

PIN No.	Signal Description	PIN No.	Signal Description
1	DCD#	2	DSR#
3	RXD#	4	RTS#
5	TXD#	6	CTS#
7	DTR#	8	RI#
9	GND	10	NC

J3: Parallel Port Pin Header

PIN No.	Signal Description	PIN No.	Signal Description
1	Strobe#	2	Auto Form Feed#
3	Data 0	4	Error#
5	Data 1	6	Initialization#
7	Data 2	8	Printer Select IN#
9	Data 3	10	Ground
11	Data 4	12	Ground
13	Data 5	14	Ground
15	Data 6	16	Ground
17	Data 7	18	Ground
19	Acknowledge#	20	Ground
21	Busy	22	Ground
23	Paper Empty	24	Ground
25	Printer Select	26	N/C

J5: FDC Interface Pin Header

PIN No.	Signal Description	PIN No.	Signal Description
1	Ground	2	Density Select 0
3	Ground	4	NC
5	KEY	6	NC
7	Ground	8	Index#
9	Ground	10	Motor ENA#
11	Ground	12	NC
13	Ground	14	Drive Select A#
15	Ground	16	NC
17	Ground	18	Direction#
19	Ground	20	Step#
21	Ground	22	Write Data#
23	Ground	24	Write Gate#
25	Ground	26	Track 0#
27	Ground	28	Write Protect#
29	NC	30	Read Data#
31	Ground	32	Head Select#
33	NC	34	Disk Change#

J6: 8-bit GPIO

PIN No.	Signal Description	PIN No.	Signal Description
1	GPIO11	2	GPIO32
3	GPIO12	4	GPIO33
5	GPIO30	6	GPIO36
7	GPIO31	8	GPIO37
9	GND	10	VCC

J7: PS2 KB/MS Pin Header

PIN No.	Signal Description	PIN No.	Signal Description
1	Mouse Data	2	Keyboard Data
3	KEY	4	KEY
5	GND	6	GND
7	PS2 Power	8	PS2 Power
9	Mouse Clock	10	Keyboard Clock

J8: IR Pin Header

PIN No.	Signal Description
1	VCC
2	NC
3	IRRX
4	GND
5	IRTX
6	NC

J9: HDD LED Pin Header

Pin No.	Signal Description
1	VCC(pull up 330 ohm)
2	HD_LED#

J10: SUS LED Pin Header

Pin No.	Signal Description
1	5VSB(pull up 330 ohm)
2	SUS_LED#

J11: TPM Pin Header

PIN No.	Signal Description	PIN No.	Signal Description
1	Clock	2	GND
3	LFRAME#	4	NC
5	PLT_RST#	6	VCC
7	LAD3	8	LAD2
9	VCC3	10	LAD1
11	LAD0	12	GND
13	SMB_CLK	14	SMB_DATA
15	3V_DUAL	16	SERIRQ
17	GND	18	NC
19	NC	20	NC

J12: Buzzer Pin Header

PIN No.	Signal Description
1	VCC
2	NC
3	NC
4	BUZZER

J14: Audio MIC/Line-in/Line-out Pin Header

PIN No.	Signal Description	PIN No.	Signal Description
1	MIC with Reference Voltage	2	Analog GND
3	Line-in Left Channel	4	Analog GND
5	Line-in Right Channel	6	Analog GND
7	Line-out Left Channel	8	Analog GND
9	Line-out Right Channel	10	KEY

J15: Buzzer Pin Header

PIN No.	Signal Description
1	+V3.3M(pull up 330 ohm)
2	82577LM_Active#
3	82583V_Active#
4	3V_DUAL(pull up 330 ohm)

J16 & J17 & J18: USBx2 Pin Header

PIN No.	Signal Description	PIN No.	Signal Description
1	5V_DUAL	2	5V_DUAL
3	DATA -	4	DATA -
5	DATA +	6	DATA +
7	GND	8	GND
9	KEY	10	GND

J30: Second SPI Pin Header

PIN No.	Signal Description	PIN No.	Signal Description
1	SPI_CS#1	2	+V3.3M
3	SPI_SO	4	SPI_CLK
5	GND	6	SPI_SI

J31: SM_BUS Pin Header

PIN No.	Signal Description
1	SMB_CLK
2	NC
3	GND
4	SMB_DATA
5	VCC

J34: CPU Fan Pin Header

Pin No.	Signal Description
1	GND
2	+12V
3	PWM_CONTROL
4	SENSE

J36: SYS FAN Pin Header

Pin No.	Signal Description
1	PWM_CONTROL
2	+12V
3	SENSE

Chapter 3
System Installation

This chapter provides you with instructions to set up your system. The additional information is enclosed to help you set up onboard PCI device and handle Watch Dog Timer (WDT) and operation of GPIO in software programming.

3.1 Intel® i7/i5/P4500 PGA

ROBO-8210VG2AR has equipped the most advanced Intel® Core i7/i5/i3 series CPUs which has built-in Intel® HD Graphics Controller providing a total solution of multi-purpose operation.
Further more, the leading-edge Intel® Core™ processor delivers unmatched technology for intelligent performance on the most demanding tasks, such as creating digital video and playing intense games. With building into ROBO-8210VG2AR module, it can be applied in many different uses depending on the function of carrier board.

CPU Support List	Intel® Core i7-620M Intel® Core i5-520M Intel® P4500

3.2 Main Memory

ROBO-8210VG2AR provide 2 x 240pin Long-DIMM sockets which supports 800/1066 DDR3-SDRAM as main memory Non-ECC, non-register type of functions. The maximum memory can be up to 8GB. Memory clock and related settings can be detected by BIOS via SPD interface.

For system compatibility and stability, do not use memory module without brand. Memory configuration can be set to either one double-sided DIMM in one DIMM socket or two single-sided DIMM in both sockets.

Beware of the connection and lock integrity from memory module to socket. Inserting improperly it will affect the system reliability.
Before locking, make sure that all modules have been fully inserted into the card slots.

Memory Frequency	Single Channel DDR Bandwidth
800	12.8 GB/s
1066	17 GB/s

Note:
To insure the system stability, please do not change any of DRAM parameters in BIOS setup to modify system the performance without acquired technical information.

3.3 Installing the Single Board Computer

To install your ROBO-8210VG2AR into standard chassis or proprietary environment, please perform the following:

Step 1 : Check all jumpers setting on proper position

Step 2 : Install and configure CPU and memory module on right position
Step 3 : Place ROBO-8210VG2AR into the dedicated position in the system
Step 4 : Attach cables to existing peripheral devices and secure it

WARNING

Please ensure that SBC is properly inserted and fixed by mechanism.

Note:

Please refer to section 3.3.1 to 3.3.4 to install INF/VGA/LAN/Audio drivers.

3.3.1 Chipset Component Driver

ROBO-8210VG2AR uses state-of-art Intel® QM57 chipset. It's a new chipset that some old operating systems might not be able to recognize. To overcome this compatibility issue, for Windows Operating Systems such as Windows XP/Vista/Win7, please install its INF before any of other Drivers are installed. You can find very easily this chipset component driver in ROBO-8210VG2AR CD-title.

3.3.2 Intel® Integrated HD Graphics Controller

Unlike the other structure, ROOB-8210 has integrated HD Graphics derived from Intel® Core series CPU (i5/i7). It's the most advanced design to gain an outstanding graphic performance. Shared 8 accompany it to 256MB system DDR3-SDRAM with Total Graphics Memory. ROBO-8210VG2AR supports VGA, DVI. This combination makes ROBO-8210VG2AR an excellent piece of multimedia hardware.

With no additional video adaptor, this onboard video will usually be the system display output. By adjusting the BIOS setting to disable on-board VGA, an add-on PCI-Express graphic card can take over the system display.

Drivers Support

Please find all the drivers in the ROBO-8210VG2AR CD-title. Drivers support , Windows XP/Vista/Win7.

3.3.3 Intel Gigabit Ethernet Controller

Drivers Support

Please find INTEL 82577LM & 82583V LAN driver in /Ethernet directory of ROBO-8210VG2AR CD-title. The drivers support Windows XP/Vista/Win7.

3.3.4 Audio Controller

Please find Intel® High Definition Audio driver form ROBO-8210VG2AR CD-title. The drivers support Windows XP/Vista/Win7.

3.4 Clear CMOS Operation

The following table indicates how to enable/disable Clear CMOS Function hardware circuit by putting jumpers at proper position.

JP3: CMOS Clear Header

	Function
1-2 Open	Normal Operation ★
1-2 Short	Clear CMOS Contents

3.5 WDT Function

The working algorithm of the WDT function can be simply described as a counting process. The Time-Out Interval can be set through software programming. The availability of the time-out interval settings by software or hardware varies from boards to boards.

ROBO-8210VG2AR allows users control WDT through dynamic software programming. The WDT starts counting when it is activated. It sends out a signal to system reset or to non-maskable interrupt (NMI), when time-out interval ends. To prevent the time-out interval from running out, a re-trigger signal will need to be sent before the counting reaches its end. This action will restart the counting process. A well-written WDT program should keep the counting process running under normal condition. WDT should never generate a system reset or NMI signal unless the system runs into troubles.

The related Control Registers of WDT are all included in the following sample program that is written in Assembly language. User can fill a non-zero value into the Time-out Value Register to enable/refresh WDT. System will be reset after the Time-out Value to be counted down to zero. Or user can directly fill a zero value into Time-out Value Register to disable WDT immediately. To ensure a successful accessing to the content of desired Control Register, the sequence of following program codes should be step-by-step run again when each register is accessed.

Additionally, there are maximum 2 seconds of counting tolerance that should be considered into user' application program. For more information about WDT, please refer to ITE8721 data sheet.

There are two PNP I/O port addresses that can be used to configure WDT,
1) 0x2E:Test 1 Register
2) 0x2F:Test 2 Register
Below are some example codes, which demonstrate the use of WDT.

```
        .model small
        .386p
        .stack
        .data
        ADDRESS         dw      0FFFFh
        .code

pgm:
mov     ADDRESS,002eh           ; I suppose 2Eh that is the address of SIO
mov     dx, ADDRESS             ; enter MB PnP mode in 2Eh
mov al, 87h
out     dx, al
mov al, 01h
out dx, al
mov al, 55h
out dx, al
mov al, 55h
out dx, al

mov al, 20h                     ; read the Chip ID to check the address of SIO
out dx, al
inc dx
in  al, dx                      ; default =87h
mov bl, al
mov al, 21h
mov dx, ADDRESS
out dx, al
inc dx
```

```
in  al, dx                      ; default =21h
mov bh, al


cmp bx,  2187h                  ;cmp CHIP ID
je                  L1

mov ADDRESS,4eh                 ; SIO in 4Eh

mov     dx, ADDRESS             ; enter MB PnP mode in 4Eh
mov al, 87h
out     dx, al
mov al, 01h
out dx, al
mov al, 55h
out dx, al
mov al, 0AAh
out dx, al

mov al, 20h                     ; read the Chip ID to check the address of SIO
out dx, al
inc dx
in  al, dx                      ; default =87h
mov bl, al
mov al, 21h
mov dx, ADDRESS
out dx, al
inc dx
in  al, dx                      ; default =21h
mov bh, al

cmp bx, 2187h
je  L1

xor     bx, bx
mov     ah, 0Eh
mov     al, 'S'
int     10h
mov     al, 'I'
int     10h
mov     al, 'O'
int     10h
mov     al, ' '
int     10h
mov     al, 'F'
```

```
int     10h
mov     al, 'a'
int     10h
mov     al, 'i'
int     10h
mov     al, 'l'
int     10h
mov     al, 0dh                 ;CR
int     10h
mov     al, 0ah
int     10h                     ;LF
jmp stop

L1 :
 mov dx, ADDRESS                ;set WDT state
 mov al, 07h
 out dx, al
 inc dx
 out dx, al
 mov dx, ADDRESS
 mov al, 71h
 out dx, al
 inc dx
 mov al, 00h
 out dx, al
        mov dx, ADDRESS
        mov al, 72h
        out dx, al
        inc dx
        mov al, 0C0h
        out dx, al

        xor     bx, bx          ; show the potion
        mov     ah, 0Eh

        mov     al, 'W'
        int     10h
        mov     al, 'D'
        int     10h
        mov     al, 'T'
        int     10h
        mov     al, ':'
        int     10h
        mov     al, 'T'
        int     10h
```

```
mov     al, 'e'
int     10h
mov     al, 's'
int     10h
mov     al, 't'
int     10h
mov     al, ' '
int     10h
mov     al, 's'
int     10h
mov     al, 't'
int     10h
mov     al, 'a'
int     10h
mov     al, 'r'
int     10h
mov     al, 't'
int     10h
mov     al, 0dh             ;CR
int     10h
mov     al, 0ah
int     10h                 ;LF

mov     al, '5'
int     10h
mov al, ' '
int 10h
mov     al, 'S'
int     10h
mov     al, 'e'
int     10h
mov al, 'c'
int 10h
mov     al, 'o'
int     10h
mov     al, 'n'
int     10h
mov     al, 'd'
int     10h
mov al, ' '
int 10h
mov     al, 'w'
int     10h
mov     al, 'i'
int     10h
```

```
        mov     al, 'l'
        int     10h
        mov     al, 'l'
        int     10h
        mov al, ' '
        int 10h
        mov al, 'b'
        int 10h
        mov al, 'e'
        int 10h
        mov al, ' '
        mov     al, 'r'
        int     10h
        mov     al, 'e'
        int     10h
        mov     al, 's'
        int     10h
        mov al, 'e'
        int 10h
        mov     al, 't'
        int     10h
        mov     al, 0dh             ;CR
        int     10h
        mov     al, 0ah
        int     10h                 ;LF

        mov     dx, ADDRESS
        mov al, 73h
        out dx, al
        inc dx
        mov al, 05h
        out dx, al
        mov     dx, ADDRESS
        mov al, 74h
        out dx, al
        inc dx
        mov al, 00h
        out dx, al

stop :
        mov     dx, ADDRESS
        mov     al, 02h
        out     dx, al
        inc dx
        mov al, 02h
```

```
        out dx, al

        mov ah, 4ch
int 21h     ;return dos

        end pgm
```

3.6 GPIO

The ROBO-8210VG2AR provides 8 programmable input or output ports that can be individually configured to perform a simple basic I/O function. Users can configure each individual port to become an input or output port by programming register bit of I/O Selection. To invert port value, the setting of Inversion Register has to be made. Port values can be set to read or write through Data Register.

3.6.1 Pin assignment

J6: 8-bit GPIO

PIN No.	Signal Description	PIN No.	Signal Description
1	GPIO11	2	GPIO32
3	GPIO12	4	GPIO33
5	GPIO30	6	GPIO36
7	GPIO31	8	GPIO37
9	GND	10	VCC

All General Purpose I/O ports can only apply to standard VCC3=3.3 ± 5% signal level (0V/3.3V), and each source sink capacity up to 8mA.

3.6.2 ROBO-8210VG2AR GPIO Programming Guide

There are 8 GPIO pins on ROBO-8210VG2AR. These GPIO pins are from SUPER I/O (IT8721) GPIO pins, and can be programmed as Input or Output direction.

J16 pin header is for 8 GPIO pins and its pin assignment as following :

J6_Pin1=GPIO0:from SUPER I/O_GPIO11 with Ext. 4.7K PH
J6_Pin2=GPIO1:from SUPER I/O_GPIO32 with Ext. 4.7K PH
J6_Pin3=GPIO2:from SUPER I/O_GPIO12 with Ext. 4.7K PH
J6_Pin4=GPIO3:from SUPER I/O_GPIO33 with Ext. 4.7K PH
J6_Pin5=GPIO4:from SUPER I/O_GPIO30 with Ext. 4.7K PH
J6_Pin6=GPIO5:from SUPER I/O_GPIO36 with Ext. 4.7K PH
J6_Pin7=GPIO6:from SUPER I/O_GPIO31 with Ext. 4.7K PH
J6_Pin8=GPIO7:from SUPER I/O_GPIO37 with Ext. 4.7K PH

<<<<< Be careful Pin9=GND , Pin10=VCC >>>>>

There are several Configuration Registers (CR) of IT8721 needed to be programmed to control the GPIO direction, and status(GPI)/value(GPO). 25h ~ 29h are common (global) registers to all Logical Devices (LD) in IT8721. LDN=07h contains the Logical Device Number that can be changed to access the LD as needed. LD7 contains the GPIO11,32,12,33,30,36,31,37 registers.

Programming Guide:

For example,
LD7_CR25h_Bit1.P1; Let Function select GPIO11
LD7_CRC0h_Bit1.P1; Let GPIO11 as Simple I/O Function
LD7_CRC8h_Bit2.P1; Let GPIO12 as Output
LD7_CRCAh_Bit3.P0; Let GPIO33 as Input

How to access IT8721 CR?

In ROBO-8210VG2AR, the Test 1 = 002Eh, and Test 2 = 002Fh.
Test 1 and Test 2 are 2 IO ports needed to access IT8721 CR.
Test 1 is the Index Port, Test 2 is the Data Port.
CR index number needs to be written into Test 1 first,
Then the data will be read/written from/to Test 2.

To R/W IT8721 CR, it is needed to Enter/Enable Configuration Mode first.
When completing the programming, it is suggested to Exit/Disable Configuration Mode.
Enter Configuration Mode: Write 87h to IO port Test 1 twice.
Exit Configuration Mode: Set bit 1 of the configure control register (index=02h) to "1" to exit.

3.6.3 Example

```
        .model small
        .386p
        .stack
        .data
        ADDRESS         dw      0FFFFh
        .code

pgm:
mov     ADDRESS,002eh                   ; I suppose 2Eh that is the address of SIO
mov     dx, ADDRESS                     ; enter MB PnP mode in 2Eh
mov al, 87h
out     dx, al
mov al, 01h
out dx, al
nop
mov al, 55h
out dx, al
nop
mov al, 55h
out dx, al
```

```
mov al, 20h                         ; read the Chip ID to check the address of SIO
out dx, al
inc dx
in  al, dx      ; default =87h
mov bl, al
mov al, 21h
mov dx, ADDRESS
out dx, al
inc dx
in  al, dx      ; default =21h
mov bh, al

cmp bx,  2187h                              ;cmp CHIP ID
je                  L1

mov ADDRESS,4eh                             ; SIO in 4Eh

mov     dx, ADDRESS                         ; enter MB PnP mode in 4Eh
mov al, 87h
out     dx, al
mov al, 01h
out dx, al
mov al, 55h
out dx, al
mov al, 0AAh
out dx, al

mov al, 20h                         ; read the Chip ID to check the address of SIO
out dx, al
inc dx
in  al, dx                                  ; default =87h
mov bl, al
mov al, 21h
mov dx, ADDRESS
out dx, al
inc dx
in  al, dx                          ; default =21h
mov bh, al

cmp bx, 2187h
je  L1

xor     bx, bx
mov     ah, 0Eh
mov     al, 'S'
```

int 10h

```
mov     al, 'I'
int     10h
mov     al, 'O'
int     10h
mov     al, ' '
int     10h
mov     al, 'F'
int     10h
mov     al, 'a'
int     10h
mov     al, 'i'
int     10h
mov     al, 'l'
int     10h
mov     al, 0dh    ;CR
int     10h
mov     al, 0ah
int     10h        ;LF
jmp L6

L1:
mov dx, ADDRESS             ; Switch to LDN=03h
mov al, 07h
out dx, al
nop
inc dx
mov al, 03h
out dx, al
nop

mov dx, ADDRESS             ; Set F0 bit3=1
mov al, 0F0h
out dx, al
nop
inc dx
in  al, dx
or  al, 08h             ;POST Data Port ==>Disable
out dx, al
nop

mov dx, ADDRESS             ; Set 30 bit0=0
mov al, 30h
out dx, al
nop
inc dx
```

```
and al, 00h             ; Parallel Port Disable
```

```
out dx, al
nop

; mov dx, ADDRESS          ; Set 31h =00
; mov al, 31h
; out dx, al
; inc dx
; and al, 00h
; out dx, al

mov dx, ADDRESS
mov     al, 07h    ;Switch to Logic Device 07 & LDN=07h
out     dx, al
nop
inc dx
out dx, al
nop

mov dx, ADDRESS                 ;Set E9 bit5 =1
mov al, 0E9h
out dx, al
nop
inc dx
in  al, dx
or  al, 20h
out dx, al
nop

mov dx, ADDRESS
mov al, 25h
out dx, al                      ; The GPIO11 & GPIO12 be set GP function
nop
inc dx
in  al, dx
or      al, 06h
out     dx, al
nop

mov dx, ADDRESS
mov al, 27h
out dx, al                      ; The GPIO30 31 32 33 36 37 be set GP function
nop
inc dx
in  al, dx
or      al, 0CFh
```

```
out     dx, al
```

```
nop

mov dx, ADDRESS
mov al, 0C0h
out dx, al                      ; set GPIO11 & GPIO12 Simple I/O function
nop
inc dx
in  al, dx
or      al, 06h
out     dx, al
nop

mov dx, ADDRESS
mov al, 0C2h
out dx, al                      ; set GPIO30 31 32 33 36 37 Simple I/O function
nop
inc dx
in  al, dx
or      al, 0CFh
out     dx, al
nop

mov dx, ADDRESS
mov al, 0C8h
out dx, al                      ; set GPIO11 & GPIO12 output(1)
nop
inc dx
in  al, dx
or      al, 06h
out     dx, al
nop

mov dx, ADDRESS
mov al, 0CAh
out dx, al                      ; set GPIO30 31 output (1)
nop
inc dx
in  al, dx
or      al, 03h
out     dx, al
nop

mov dx, ADDRESS
mov al, 0CAh
out dx, al                      ; set GPIO32 33 36 37 input (0)
```

nop

```
inc dx
in  al, dx
and     al, 33h
out     dx, al
nop

mov dx, ADDRESS                 ;load the base address MSB
mov al, 62h
out dx, al
nop
inc dx
in  al, dx
mov ah, al

mov dx, ADDRESS                 ;load the base address LSB
mov al, 63h
out dx, al
nop
inc dx
in  al, dx

mov bx, ax
mov dx, ax      ; go to gpio1 address
in  al, dx
or  al, 06h             ; set high to input
out dx, al
nop
nop

add bx, 02h  ; 0A42
mov dx, bx
nop
in  al, dx
or  al, 03h  ; set high to input
and al, 33h
out dx, al

in  al, dx              ; read the gpio output
and al, 0CFh
cmp al, 0CFh
jnz     L5

sub bx, 02h
mov ax, bx
mov dx, ax      ; go to gpio1 address
```

```
in  al, dx
```

```
and al, 0F9h          ; set low to gpio11 & GPIO12
out dx, al

add bx, 02h
mov ax, bx
mov dx, ax      ; go to gpio3 address
in  al, dx
and al, 0FCh          ; set high to input
out dx, al

in  al, dx            ; read the gpio output
or  al, 30h
cmp al, 30h
jnz         L5

mov dx, ADDRESS
mov al, 0C8h
out dx, al                          ; set GPIO11 & GPIO12 input(0)
inc dx
in  al, dx
and         al, 0F9h
out         dx, al

mov dx, ADDRESS
mov al, 0CAh
out dx, al                          ; set GPIO30 & 31 input (0)
inc dx
in  al, dx
and         al, 0FCh
or          al, 0CCh            ; set GPIO32 33 36 37 output (1)
out         dx, al

mov ax, bx
mov dx, ax
in  al, dx
or  al, 0CCh          ; set high to input
out dx, al


in  al, dx            ; read the gpio output
or  al, 30h
cmp al, 0FFh
jnz         L5

sub bx, 02h
```

mov ax, bx

```
mov dx, ax
in  al, dx
or  al, 0F3h
cmp al, 0FFh
jnz         L5

add bx, 02h
mov dx, bx
out dx, ax      ; go to gpio3 address
in  al, dx
and al, 33h             ; set high to input
out dx, al


in  al, dx
or  al, 30h
cmp al, 30h
jnz         L5

sub bx, 02h
mov ax, bx
mov dx, ax
in  al, dx
or  al, 0FCh
cmp al, 0FCh
jnz         L5
jmp L4

L5 :
xor         bx, bx
mov         ah, 0Eh
;out        dx, al
mov         al, 'F'
int         10h
mov         al, 'a'
int         10h
mov         al, 'i'
int         10h
mov         al, 'l'
int         10h
mov         al, 0dh    ;CR
int         10h
mov         al, 0ah
int         10h         ;LF
jmp L6
```

```
L4 :
xor     bx, bx
mov     ah, 0Eh
;out    dx, al
mov     al, 'P'
int     10h
mov     al, 'a'
int     10h
mov     al, 's'
int     10h
mov     al, 's'
int     10h
mov     al, 0dh    ;CR
int     10h
mov     al, 0ah
int     10h        ;LF

L6:
;Save the register value
mov     dx, Address
mov     al, 07h
out     dx, al

mov     al, 03h
inc     dx
out     dx, al

mov     al, 030h
mov     dx, address
out     dx, al

mov     al, 001h
inc     dx
out     dx, al

mov     al, 0f0h
mov     dx, address
out     dx, al

mov     al, 000h
inc     dx
out     dx, al


mov     dx, ADDRESS
```

```
mov     al, 02h
out     dx, al
```

```
inc dx
mov al, 02h
out dx, al

; xor       ah, ah
; int       16h

;Gasym mov     ax,4c00h
;Gasym int     21h

exitp:  mov ah, 4ch
      int 21h       ;return dos
            end pgm
```

Chapter 4
BIOS Setup Information

ROBO-8210VG2AR uses AMI BIOS structure stored in Flash ROM. These BIOS has a built-in Setup program that allows users to modify the basic system configuration easily. This type of information is stored in CMOS RAM so that it is retained during power-off periods. When system is turned on, ROBO-8210VG2AR communicates with peripheral devices and checks its hardware resources against the configuration information stored in the CMOS memory. If any error is detected, or the CMOS parameters need to be initially defined, the diagnostic program will prompt the user to enter the SETUP program. Some errors are significant enough to abort the start up.

4.1 Entering Setup -- Launch System Setup

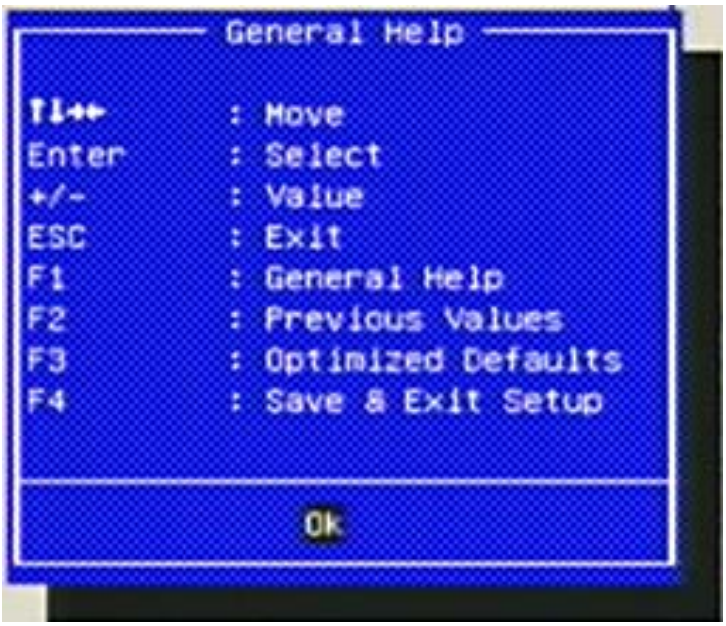
Power on the computer and the system will start POST (Power On Self Test) process. When the message below appears on the screen, press <Del> key will enter BIOS setup screen.

Press <Del> to enter SETUP

If the message disappears before responding and still wish to enter Setup, please restart the system by turning it OFF and On or pressing the RESET button. It can be also restarted by pressing <Ctrl>, <Alt>, and <Delete> keys on keyboard simultaneously.

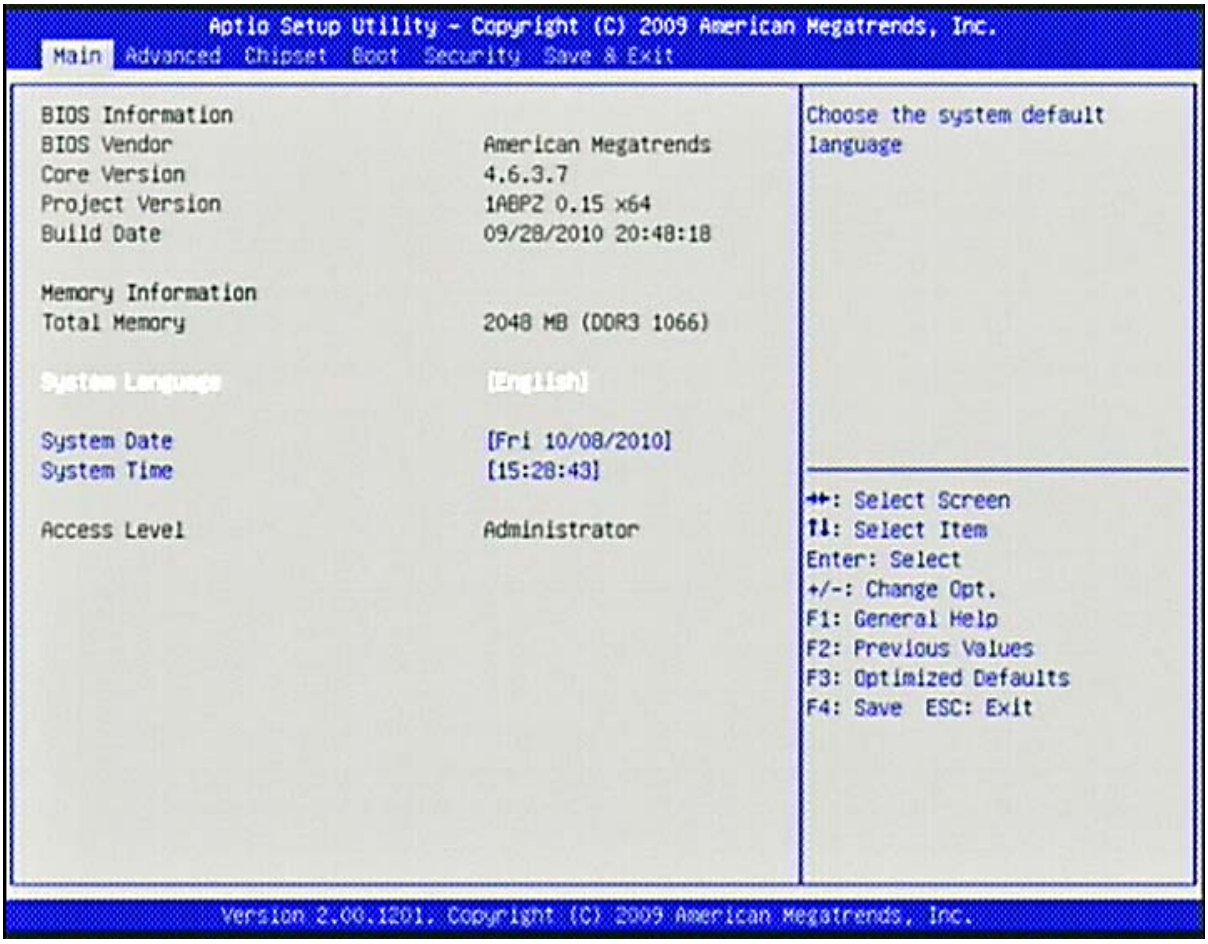
Press <F1> to Run SETUP or Resume

The BIOS setup program provides a General Help screen. The menu can be easily called up from any menu by pressing <F1>. The Help screen lists all the possible keys to use and the selections for the highlighted item. Press <Esc> to exit the Help screen.



4.2 Main

Use this menu for basic system configurations, such as time, date etc.



BIOS Information, Memory Information

These items show the firmware and memory specifications of your system. Read only.

System Time

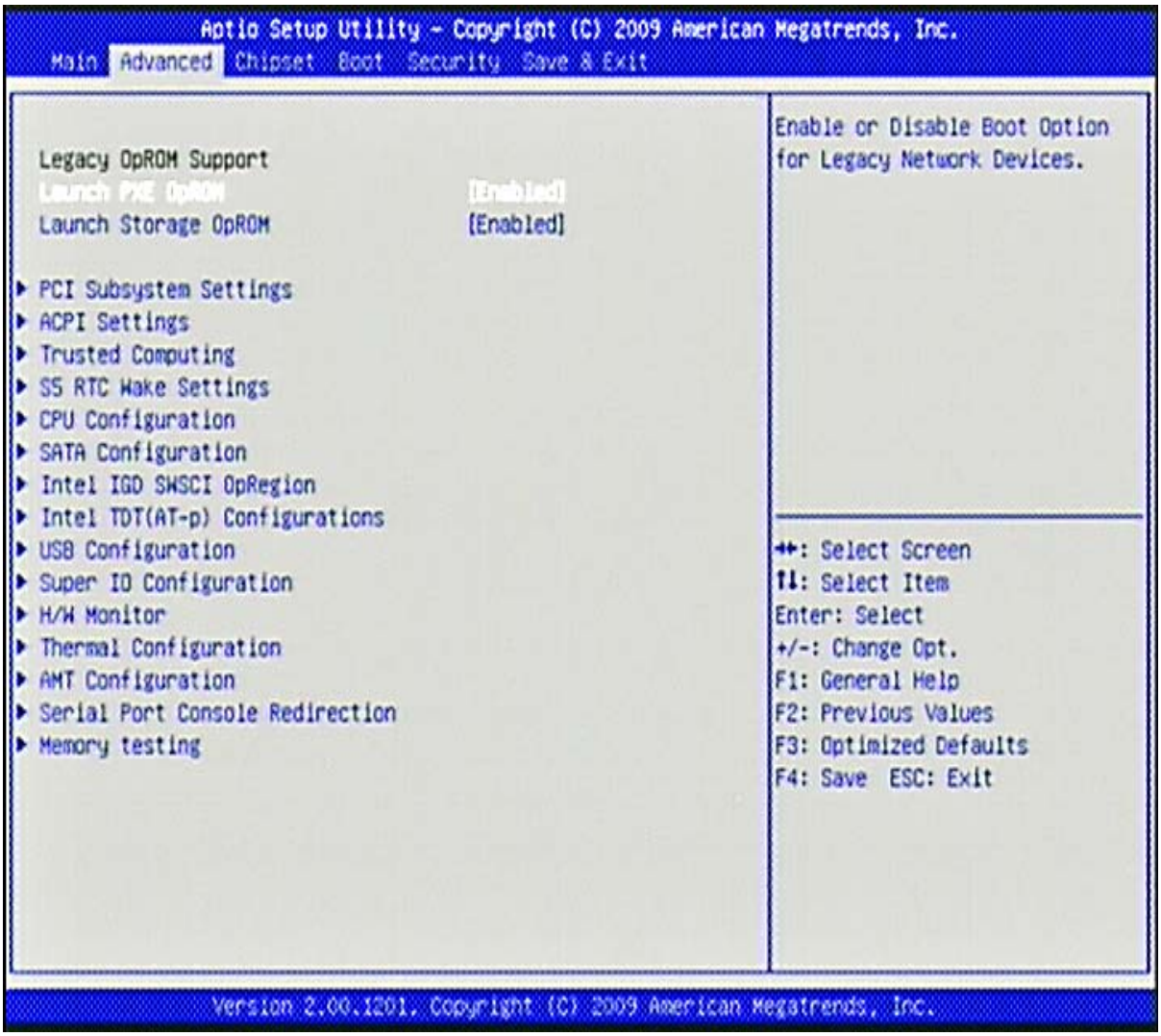
The time format is <Hour> <Minute> <Second>. Use [+] or [−] to configure system Time.

System Date

The date format is <Day>, <Month> <Date> <Year>. Use [+] or [−] to configure system Date.

4.3 Advanced

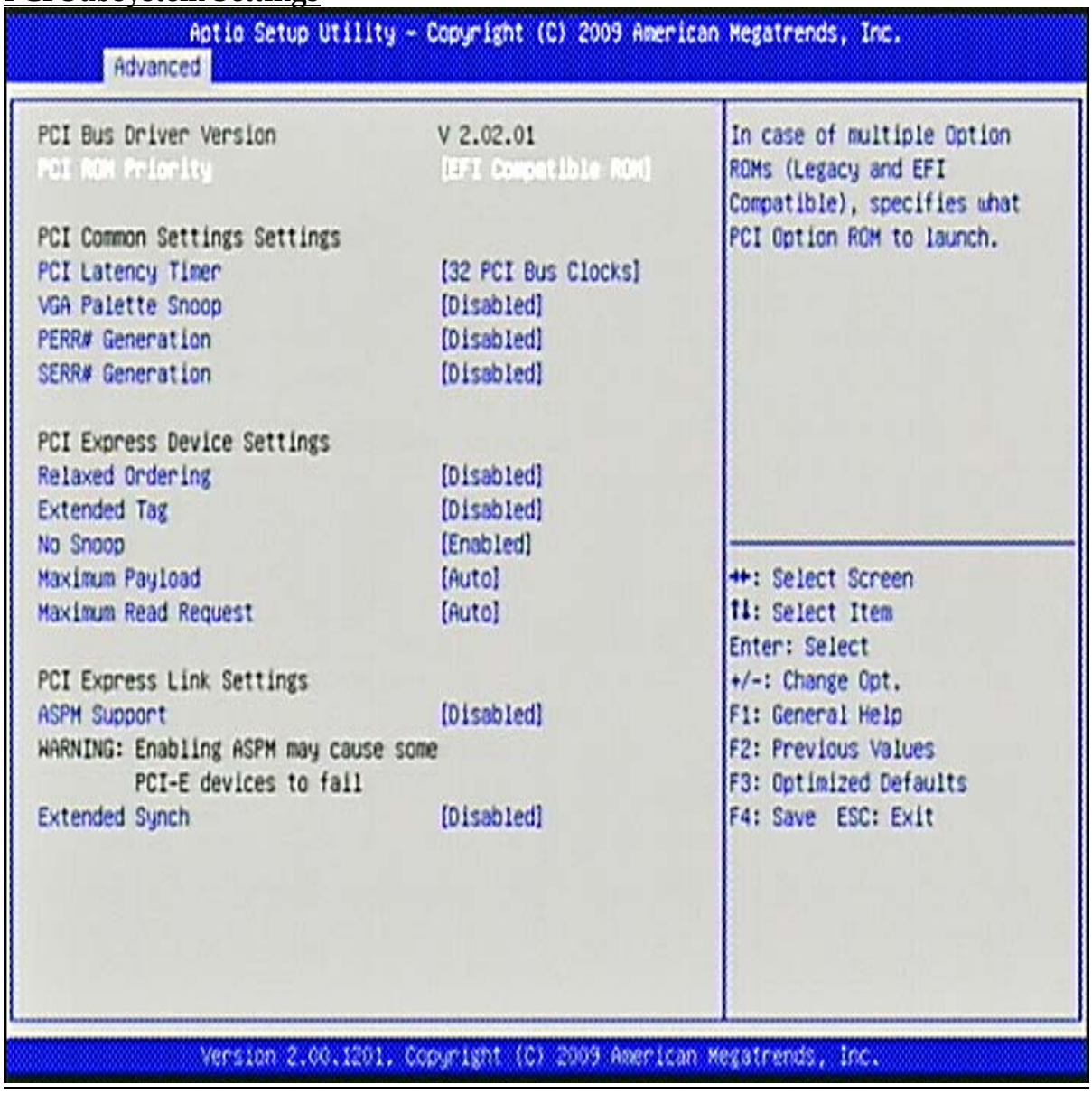
Use this menu to set up the items of special enhanced features.



Launch PXE OpROM
Enable or Disable Boot Option for Lagacy Network Devices.
Choices: Disabled, Enabled

Launch Storage OpROM
Enable or Disable Boot Option for Lagacy Mass Storage devices.
Choices: Disabled, Enabled

PCI Subsystem Settings



PCI ROM Priority
Choices: Legacy ROM, EFI Compatible ROM

PCI Latency Timer
Choices: 32 PCI, 64 PCI, 96 PCI, 128 PCI, 160 PCI, 192 PCI, 224 PCI, 248 PCI Bus Clocks

VGA Palette Snoop
Choices: Disabled, Enabled

PERR# Generation
Choices: Disabled, Enabled

SERR# Generation
Choices: Disabled, Enabled

Relaxed Ordering
Choices: Disabled, Enabled

Extended Tag
Choices: Disabled, Enabled

No Snoop
Choices: Disabled, Enabled

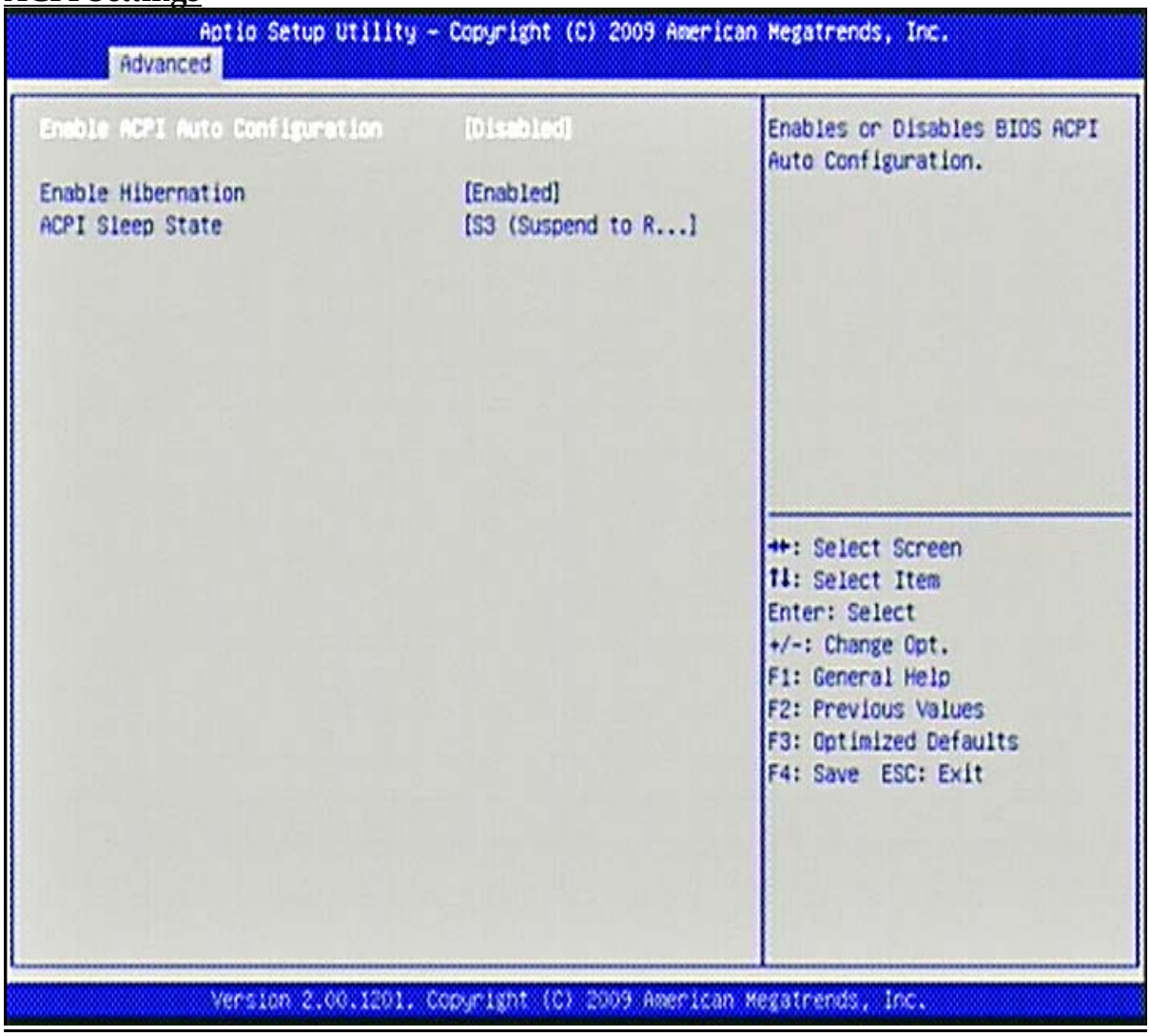
Maximum Payload
Choices: Auto, 128 Bytes, 256 Bytes, 512 Bytes, 1024 Bytes, 2048 Bytes, 4096 Bytes

Maximum Read Request
Choices: Auto, 128 Bytes, 256 Bytes, 512 Bytes, 1024 Bytes, 2048 Bytes, 4096 Bytes

ASPM Support
Choices: Disabled. Auto, Force L0

Extended Synch
Choices: Disabled, Enabled

ACPI Settings

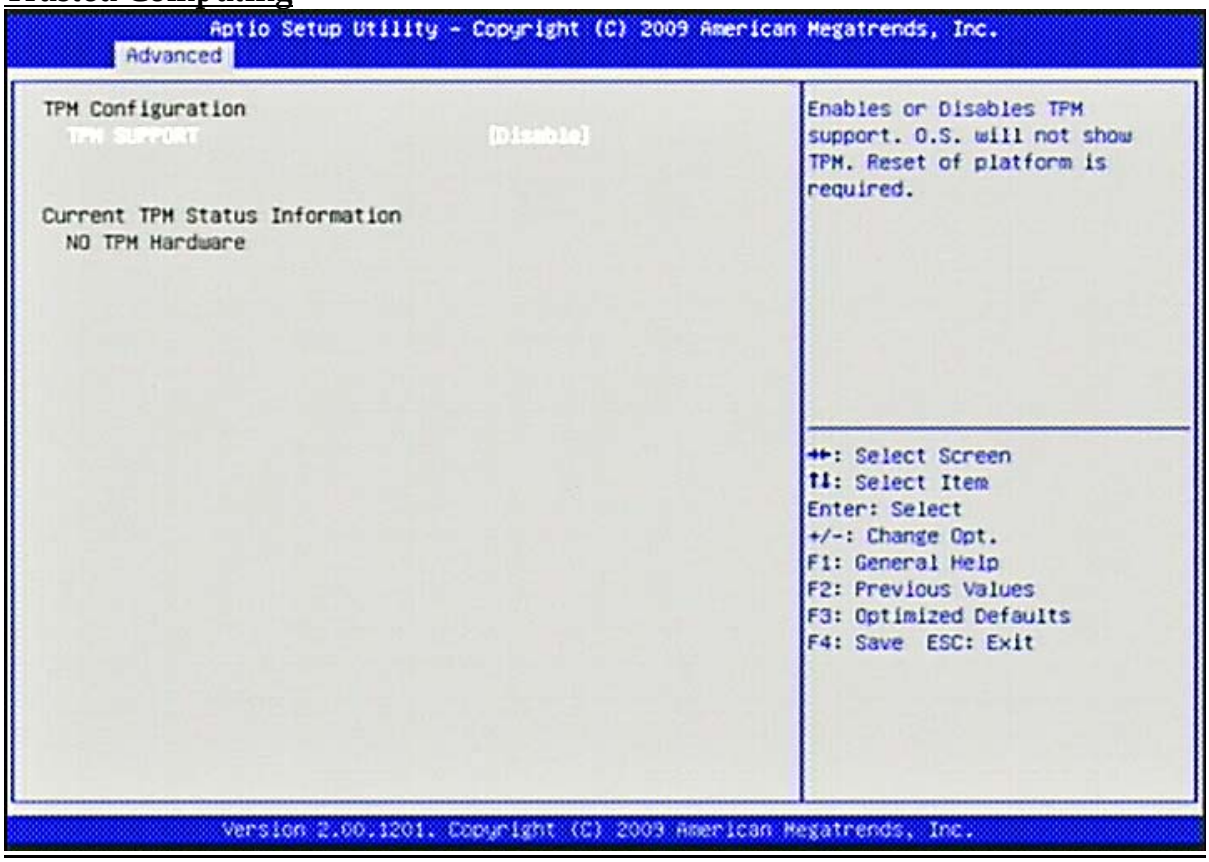


Enable ACPI Auto Configuration
Choices: Enabled, Disabled.

Enable Hibernation
Choices: Enabled, Disabled.

ACPI Sleep State
Choices: Suspend Disabled, S1 (CPU Stop Clock), S3 (Suspend to RAM)

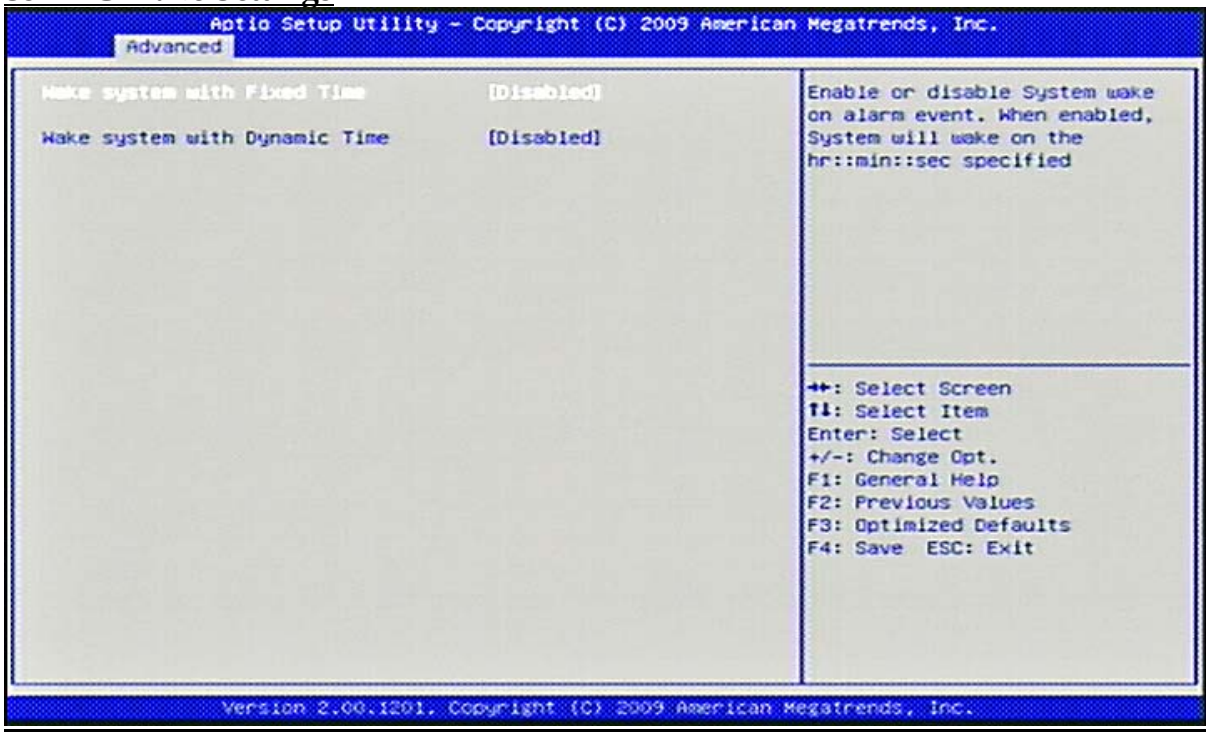
Trusted Computing



TPM SUPPORT

Choices: Enabled, Disabled

S5 RTC Wake Settings

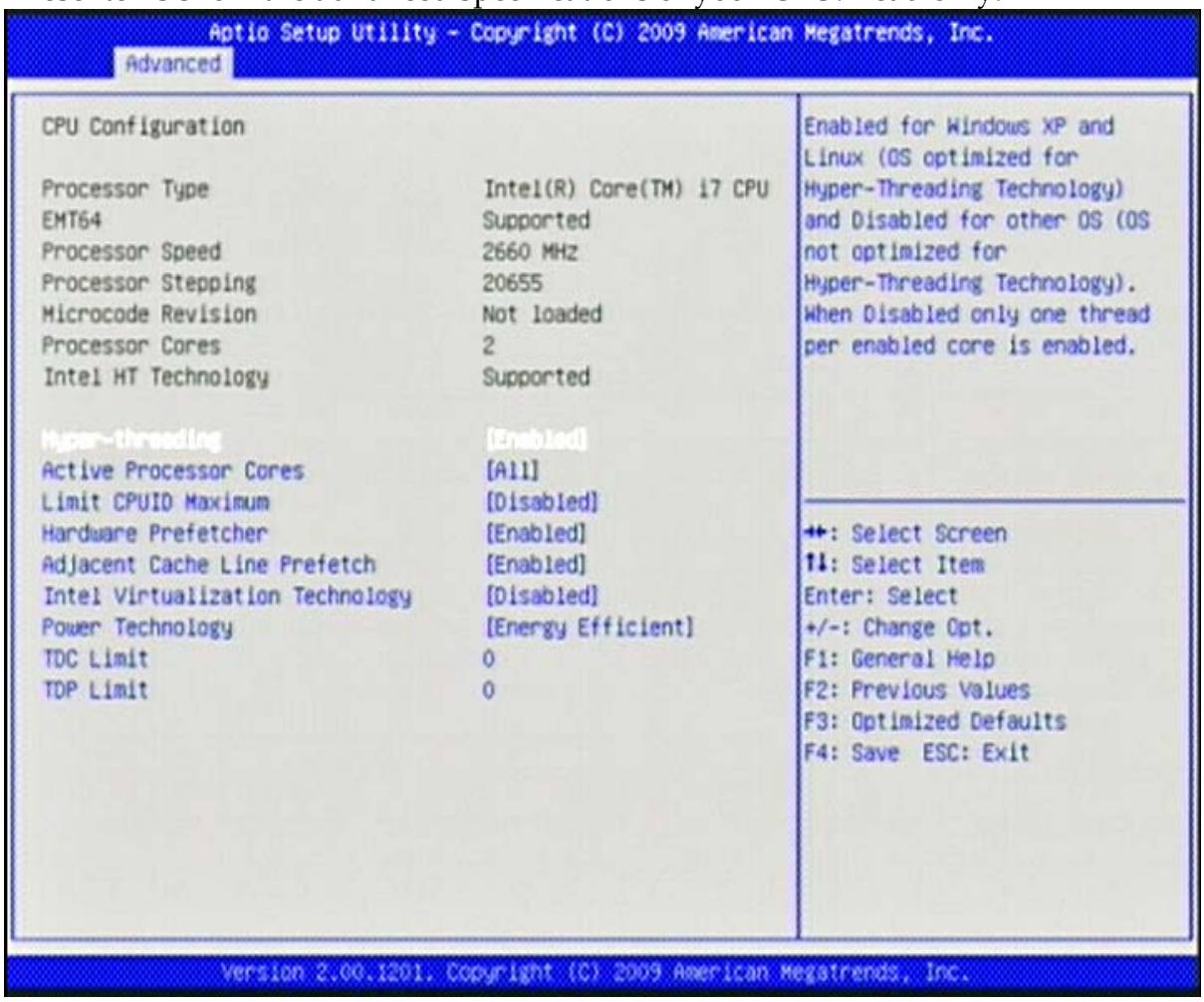


Wake System with Fixed Time
Choices: Disabled, Enabled

Wake System with Dynamic Time
Choices: Disabled, Enabled

CPU Configuration

These items show the advanced specifications of your CPU. Read only.



Hyper-Threading
Choices: Disabled, Enabled.

Active Processor Cores
Choices: All, 1, 2

Limit CPUID Maximum

Disabled for Windows XP

Choices: Disabled, Enabled.

Hardware Prefetcher

For UP platforms, leave it enabled. For DP/MP servers, it may use to tune performance the specific application.

Choices: Disabled, Enabled.

Adjacent Cache Line Prefetch

For UP platforms, leave it enabled. For DP/MP servers, it may use to tune performance the specific application.

Choices: Disabled, Enabled.

Intel Virtualization Technology

Choices: Disabled, Enabled.

Power Technology

Choices: Disabled, Energy Efficient, Custom

TDC Limit

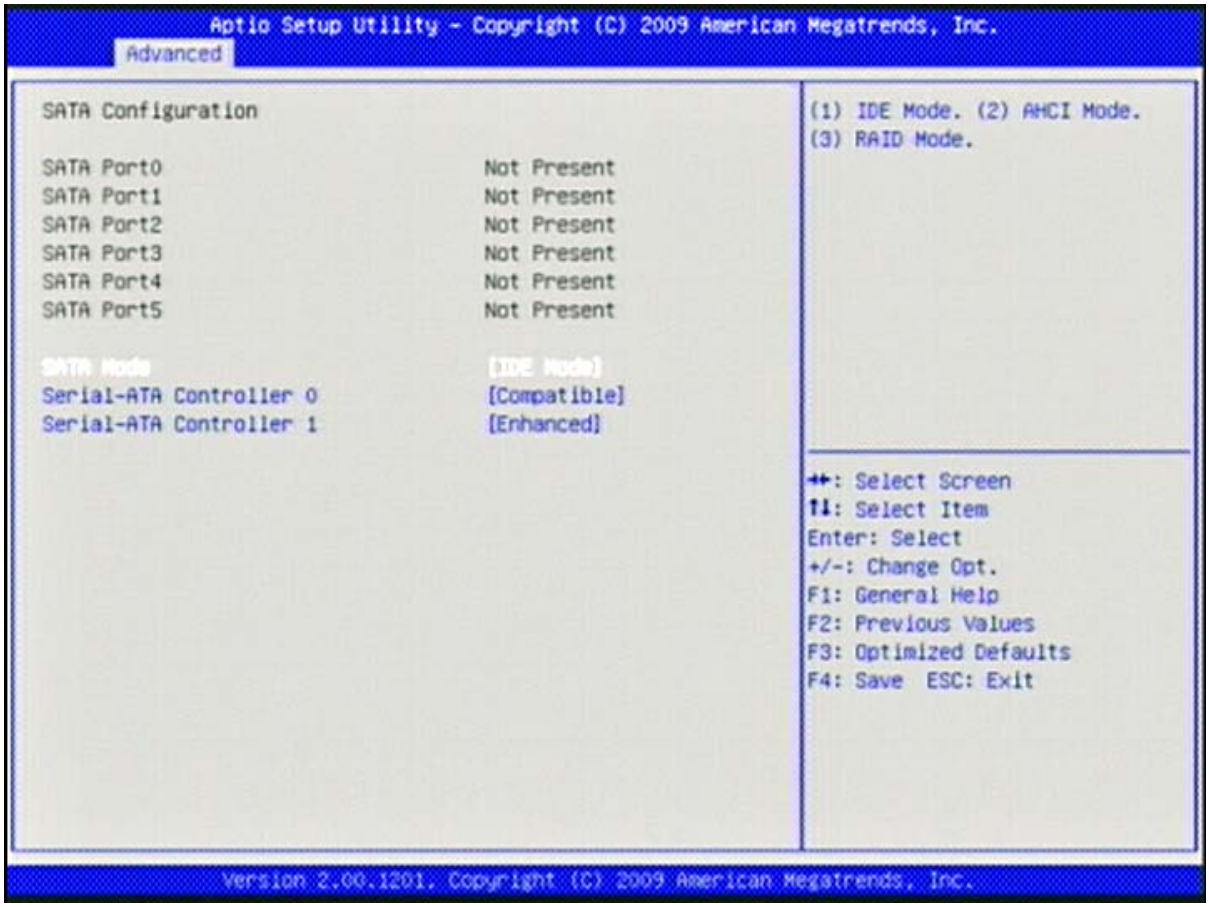
Turbo-XE Mode Processor TDC Limit in 1/8 A granularity, 0 means using the factory-configured value.

TDP Limit

Turbo-XE Mode Processor TDP Limit in 1/8 W granularity, 0 means using the factory-configured value.

SATA Configuration

The SATA Configuration the SATA devices, such as hard disk drive or CD-ROM drive.



SATA Mode

This setting specifies the function of the on-chip SATA controller.

Choices: Disabled, IDE Mode, RAID Mode, AHCI Mode.

Serial_ATA Controller 0

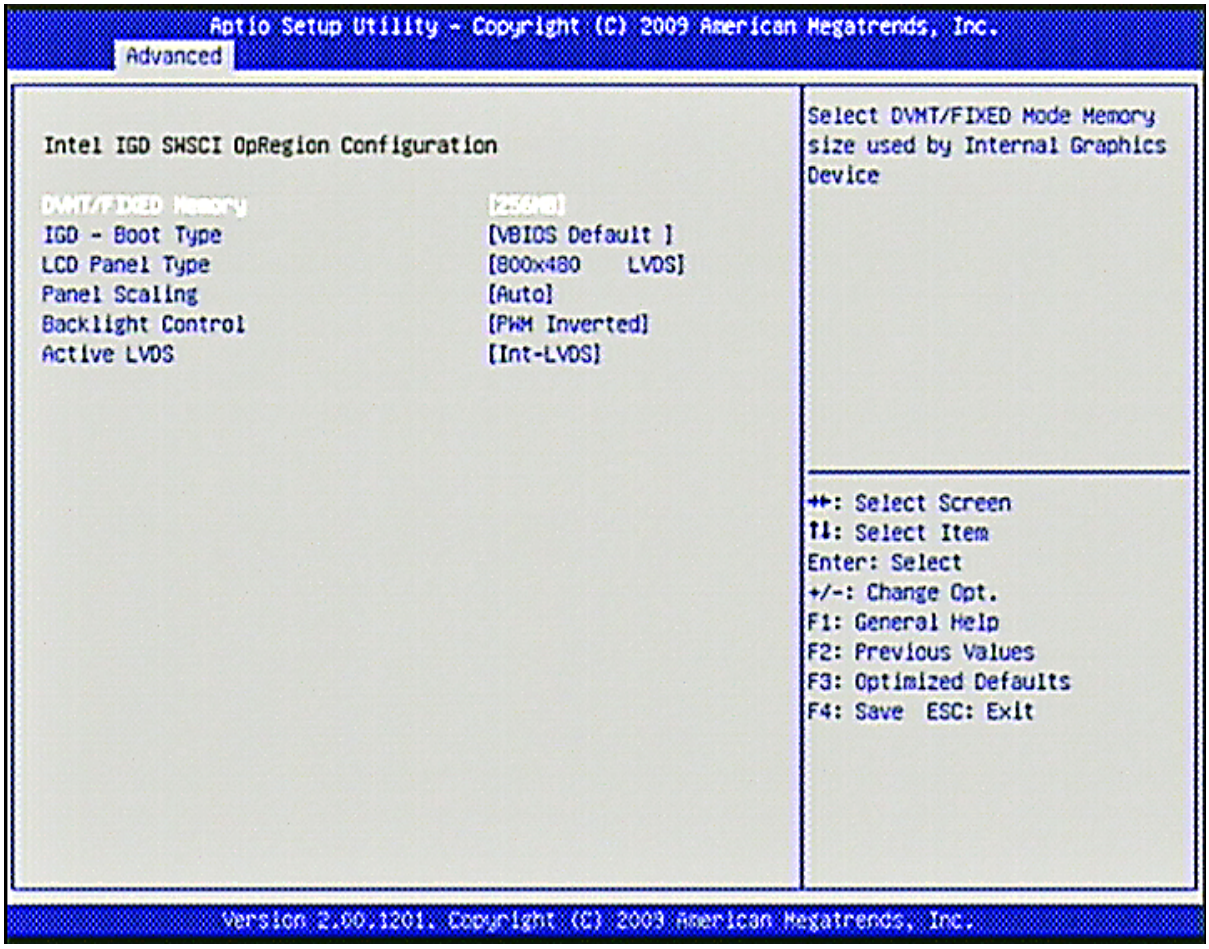
Choices: Disabled, Compatible, Enabled.

Serial_ATA Controller 1

Choices: Disabled, Compatible, Enabled.

Intel IGD SWSCI OpRegion

These option contains all the Intel® IGD setting for graphic output.



DVMT/FIXED Memory

Choices: 128M, 256MB, Maximum

IGD – Boot Type

Select the Video Device which will be activated during POST.
Choices: VBIOS Default, CRT, LVDS, CRT+LVDS, DVI, CRT+DVI.

LCD Panel Type

Choices: 800x480 LVDS, 800x600 LVDS, 1024x768 LVDS, 1280x1024 LVDS.

Panel Scaling

Choices: Auto, Force Scaling, Off, Maintain Aspect Ratio.

Backlight Control

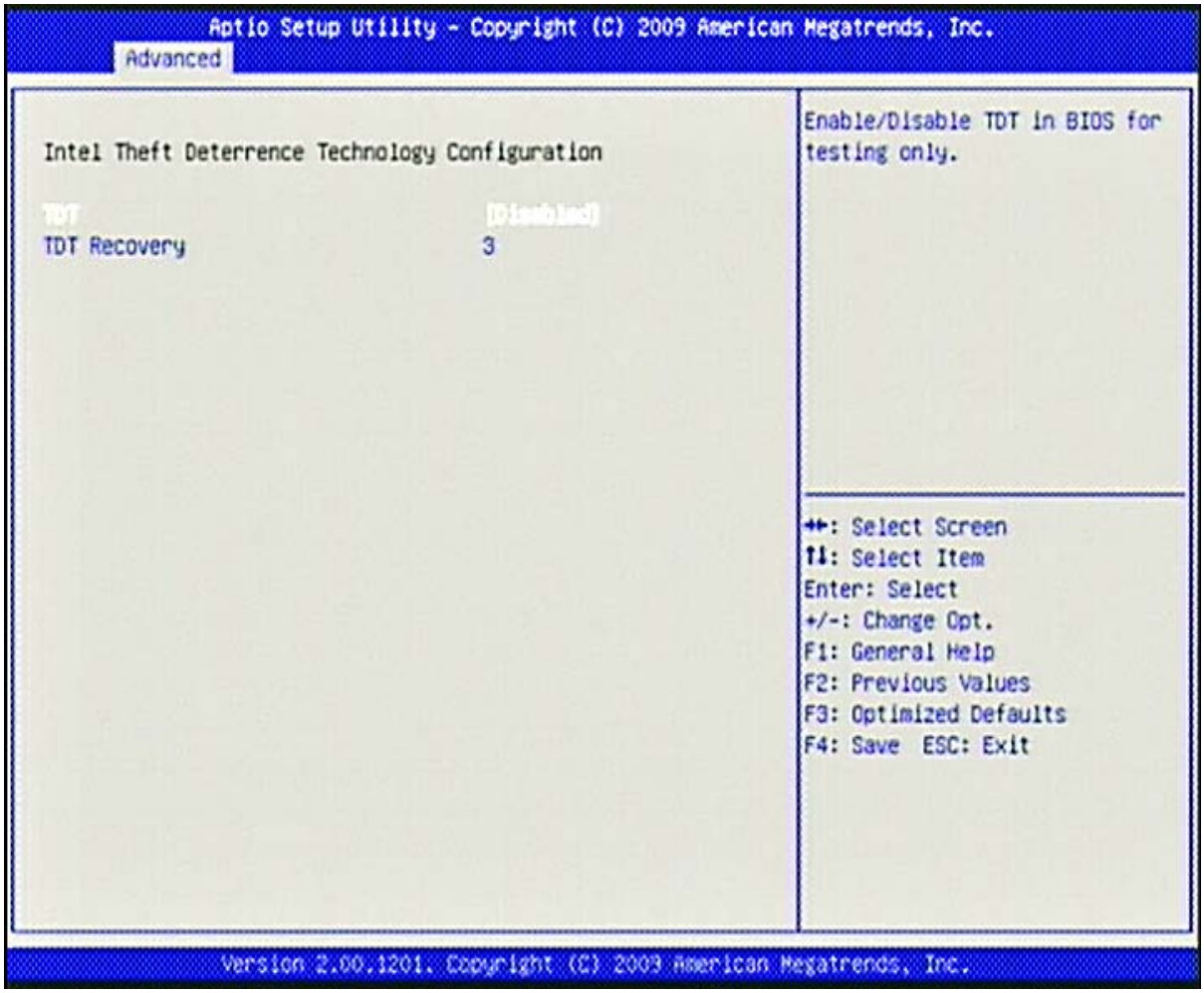
Choices: PWM Intverted, PWM Normal, GMBus Inverted, GMBus Normal.

Active LVDS

Choices: No LVDS, Int-LVDS.

Intel TDT(AT-p) Configurations

Inter Theft Deterrence Technology Configuration



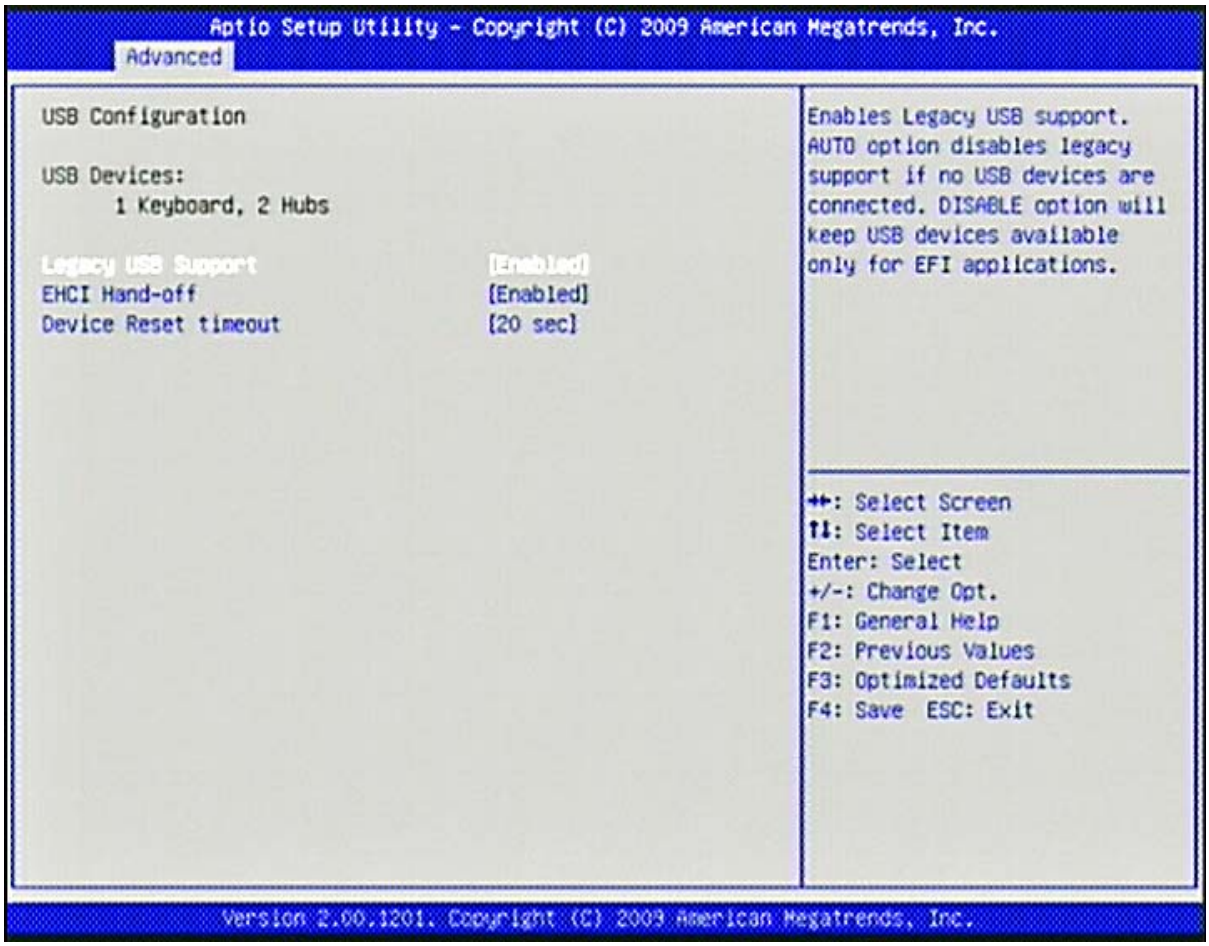
TDT

Choices: Disabled, Enabled.

TDT Recovery

Choices: 1-64

USB Configuration



Legacy USB Support

Set to [Enabled] if you need to use any USB 1.1/2.0 device in the operating system that does not support or have any USB 1.1/2.0 driver installed, such as DOS and SCO Unix.

Choices: Disabled, Enabled, Auto.

EHCI Hand-Off

This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should claim by EHCI driver.

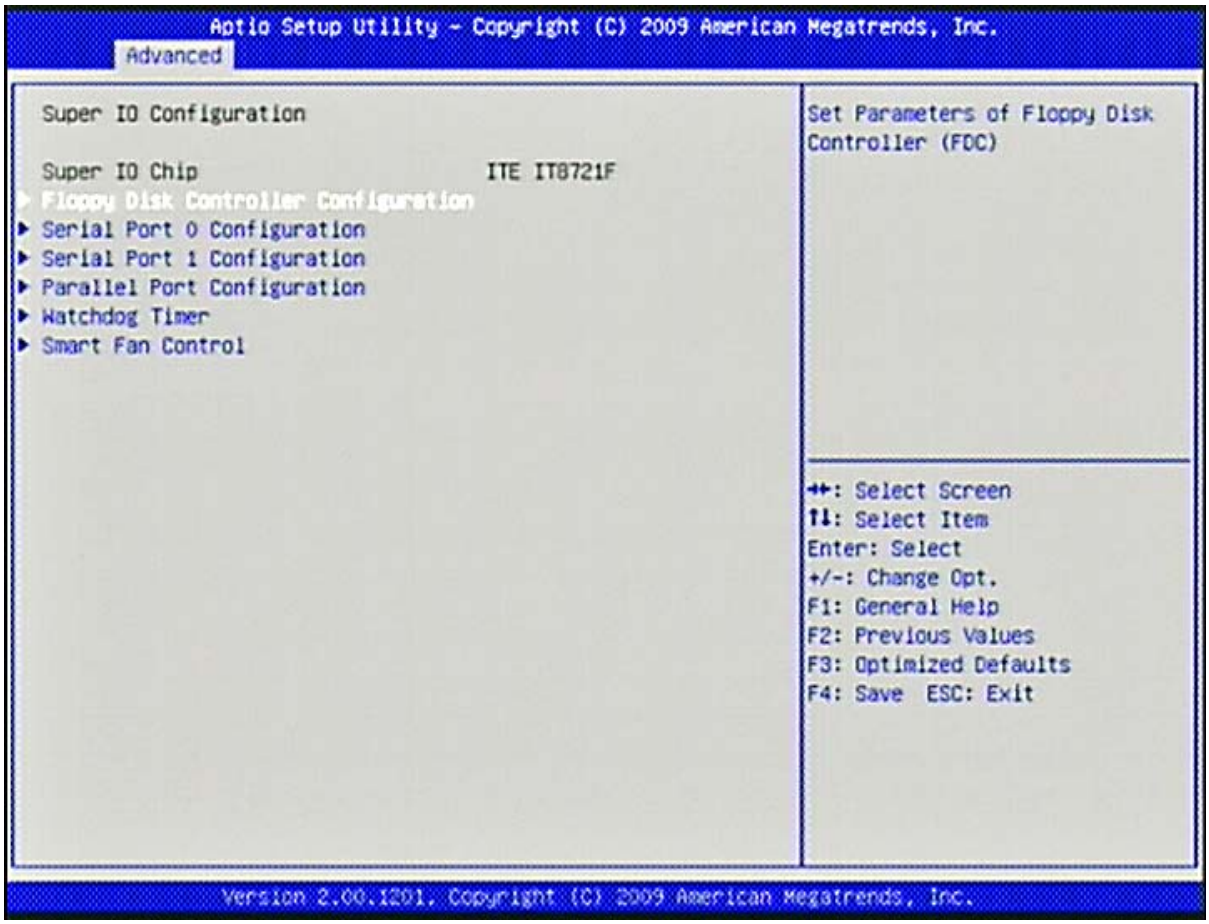
Choices: Disabled, Enabled.

Device Reset timeout

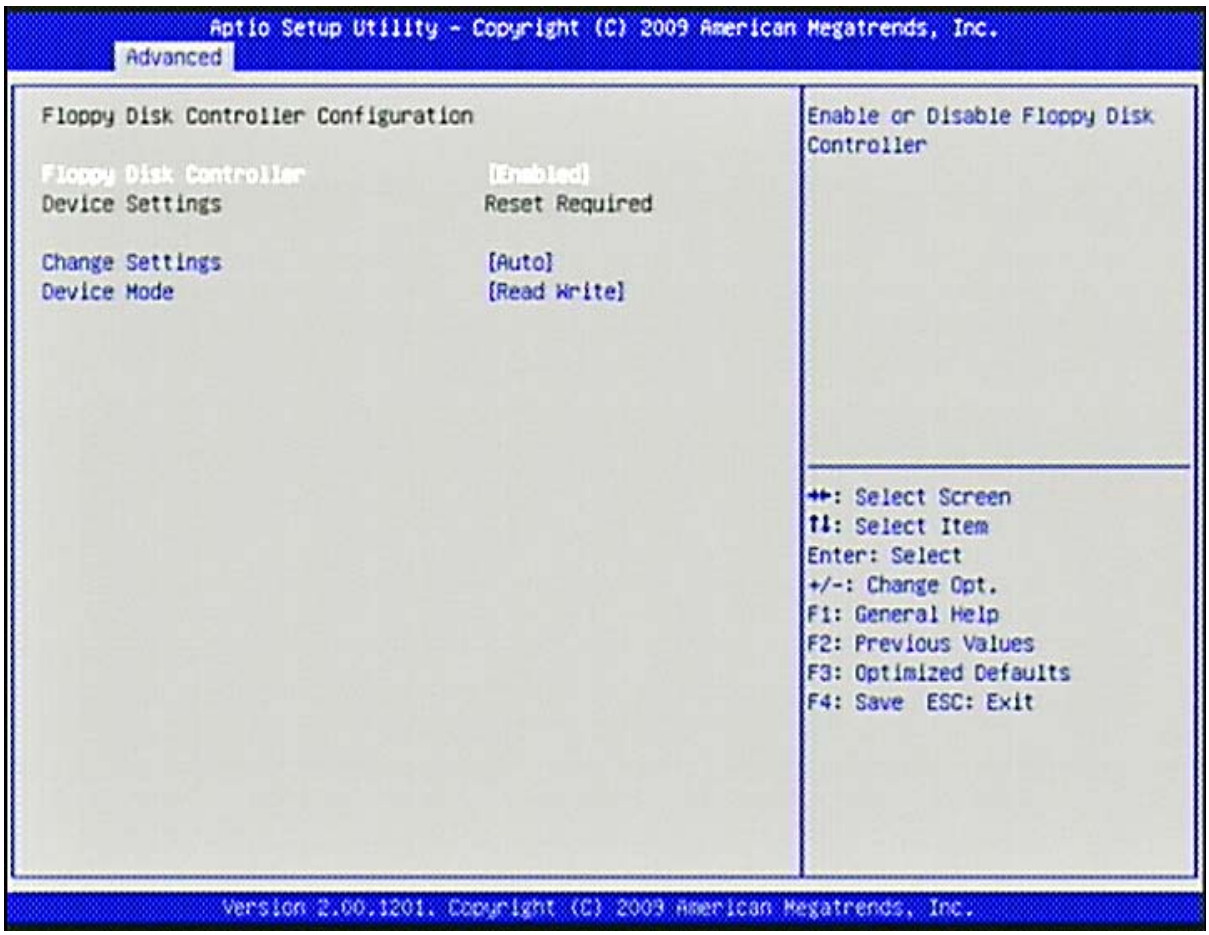
Choices: 10 sec, 20 sec, 30 sec, 40 sec

Super IO Configuratoin

List all the option that can be set of Super I/O.
Including Floppy Disk control, Serial Port 0,1 Configuration and Parallel Port configuration,



Floppy Disk Controller Configuration

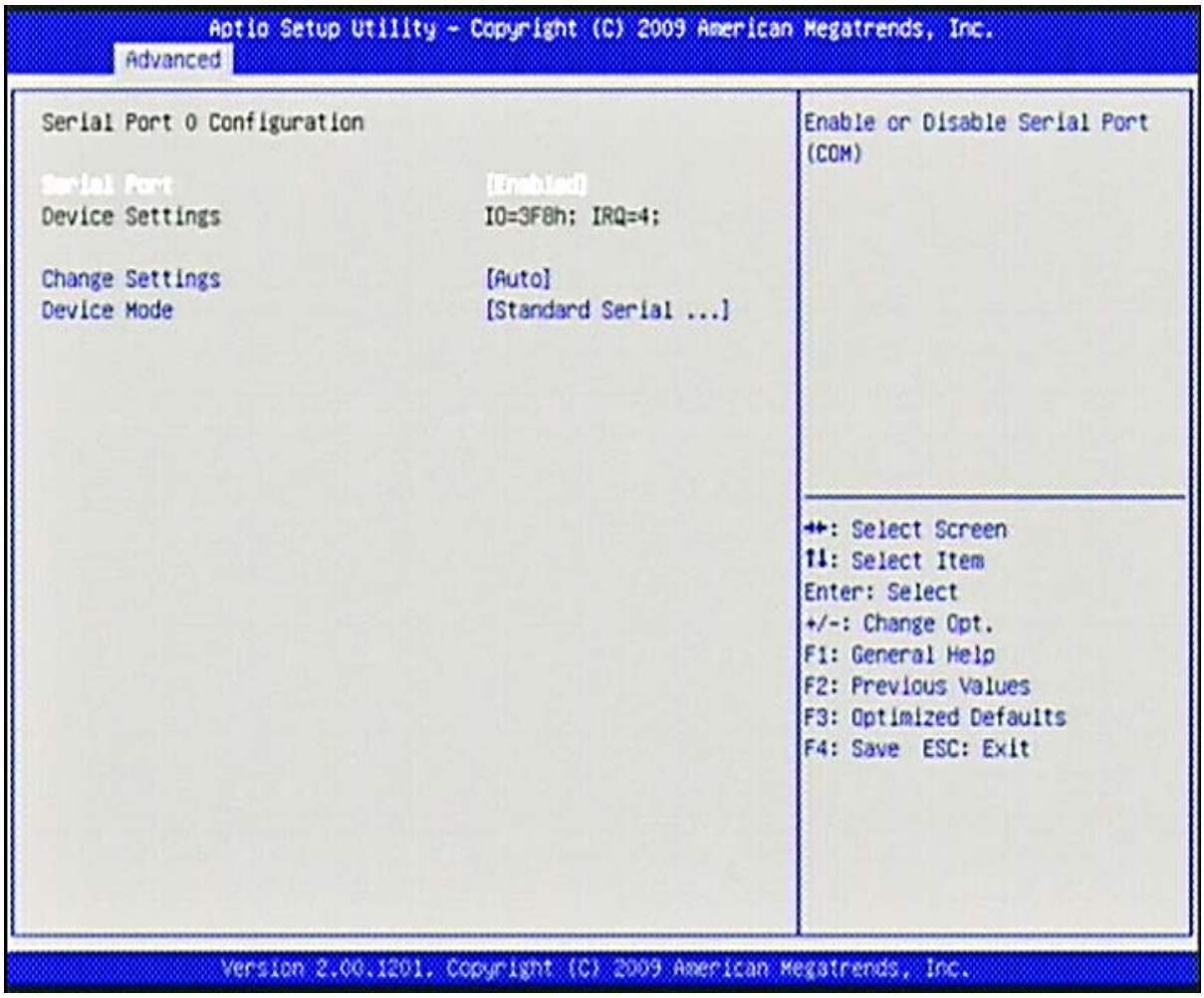


Floppy Disk Controller
Choices: Disabled, Enabled

Change Settings
Choices: Auto, IO=3F0h; IRQ=6, DMA=2;
IO=3F0h; IRQ=3,4,5,6,7,10,11,12, DMA=2, 3;
IO=370h; IRQ=3,4,5,6,7,10,11,12, DMA=2, 3;

Device Mode
Choices: Read Write, Write Protect

Serial Port 0/1 Configuration

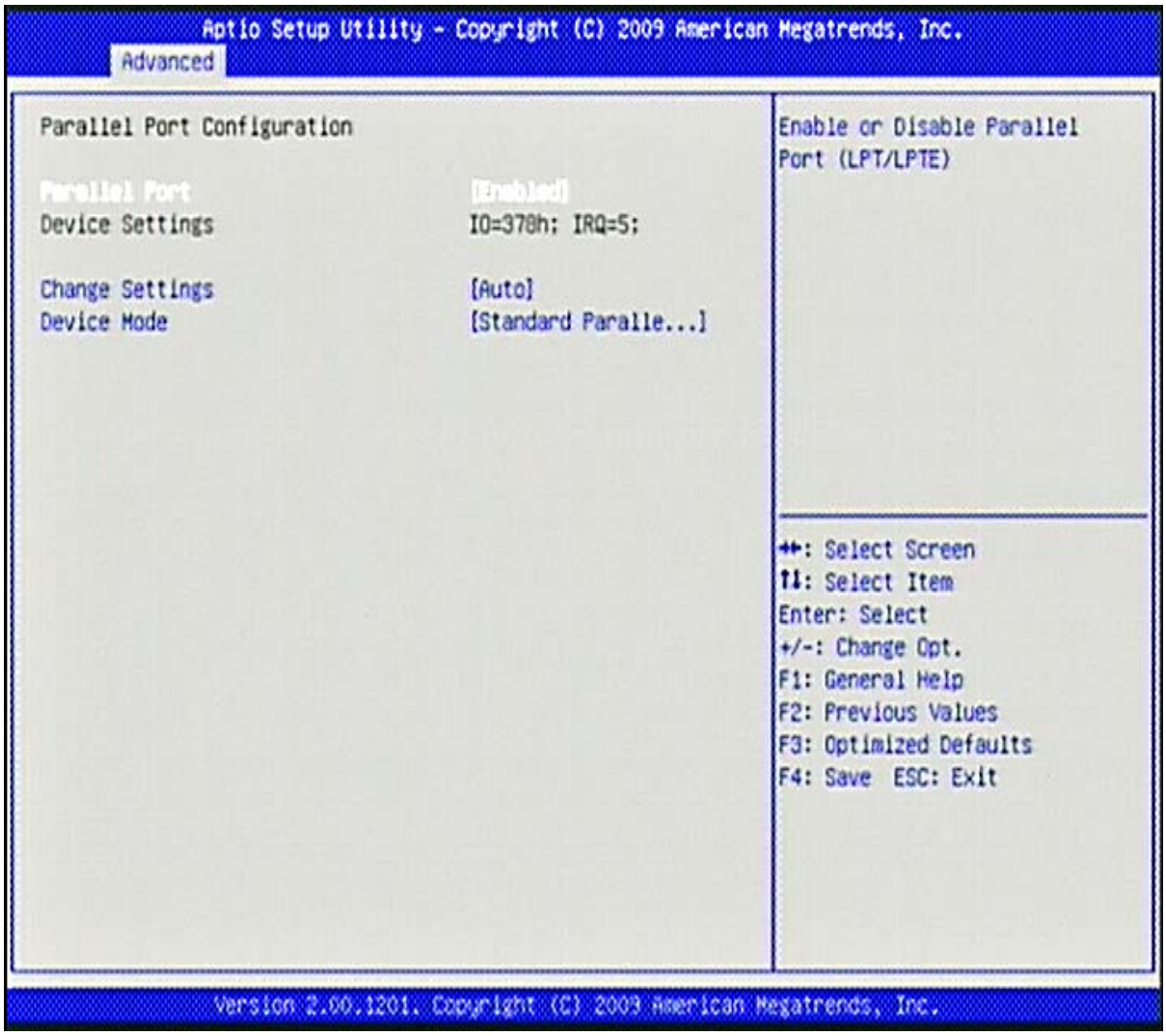


Serial Port
Choices: Disabled, Enabled,

Change Settings
Choices: Auto. IO=3F8h; IRO=4, IO=3F8h; IRO=3,4,5,6,7,10,11,12, IO=2F8h; IRO=3,4,5,6,7,10,11,12, IO=3E8h; IRO=3,4,5,6,7,10,11,12, IO=2E8h; IRO=3,4,5,6,7,10,11,12,

Device Mode
Choices: Standard Serial Port Mode, IrDA 1.0 (HP SIR) Mode, ASK IR Mode.

Parallel Port Configuration

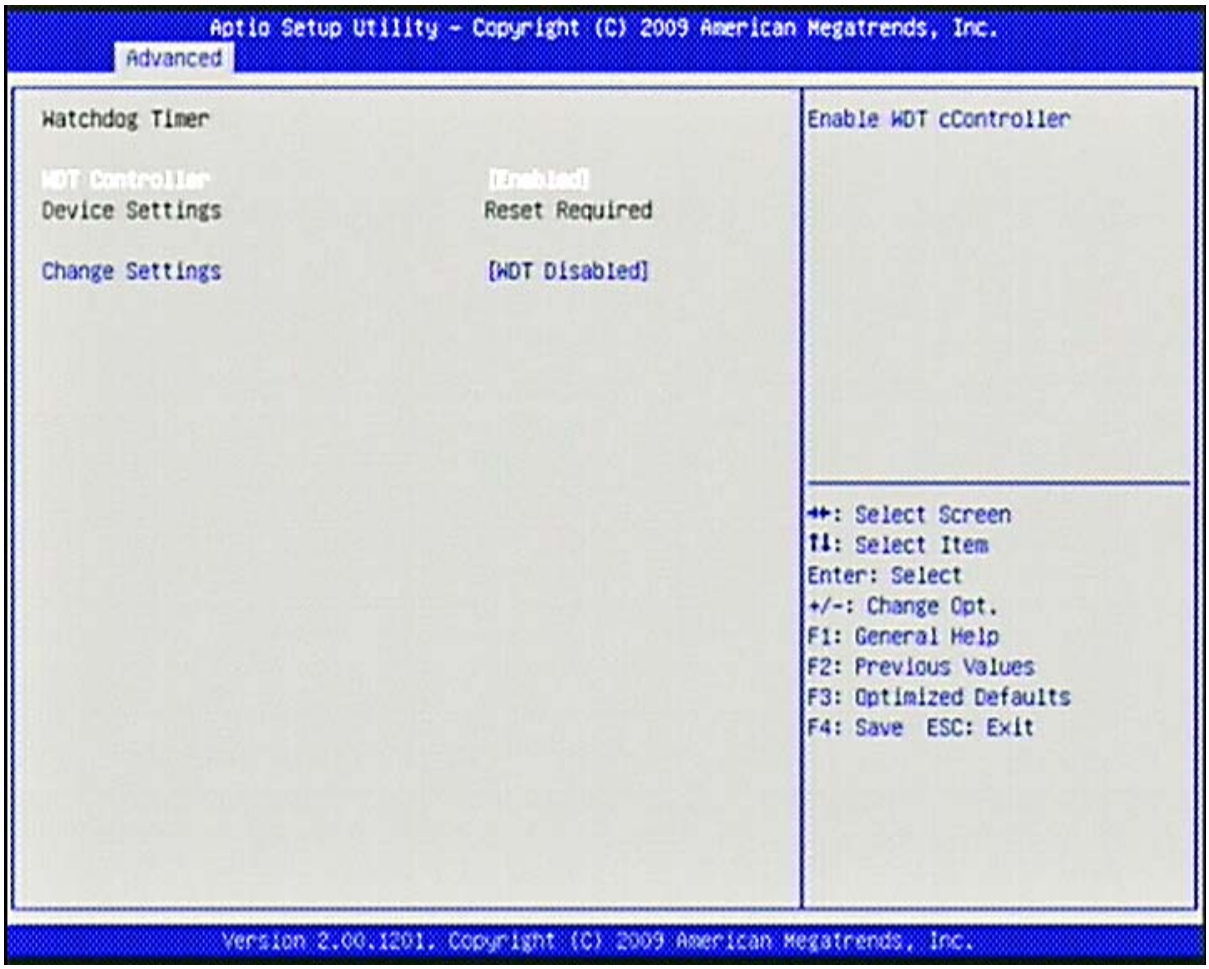


Parallel Port
Choices: Disabled, Enabled,

Change Settings
Choices: Auto. IO=378h; IRQ=5, IO=378h; IRO=5,6,7,10,11,12, IO=378h; IRQ=5,6,7,10,11,12, IO=278h; IRQ=5,6,7,10,11,12, IO=38Ch; IRQ=5,6,7,10,11,12,

Device Mode
Choices: STD printer mode, SPP mode, EPP-1.9 and SPP mode, EPP-1.7 and SPP mode, ECP mode, ECP and EPP-1.9 mode, ECP and EPP-1.7 mode.

Watchdog Timer



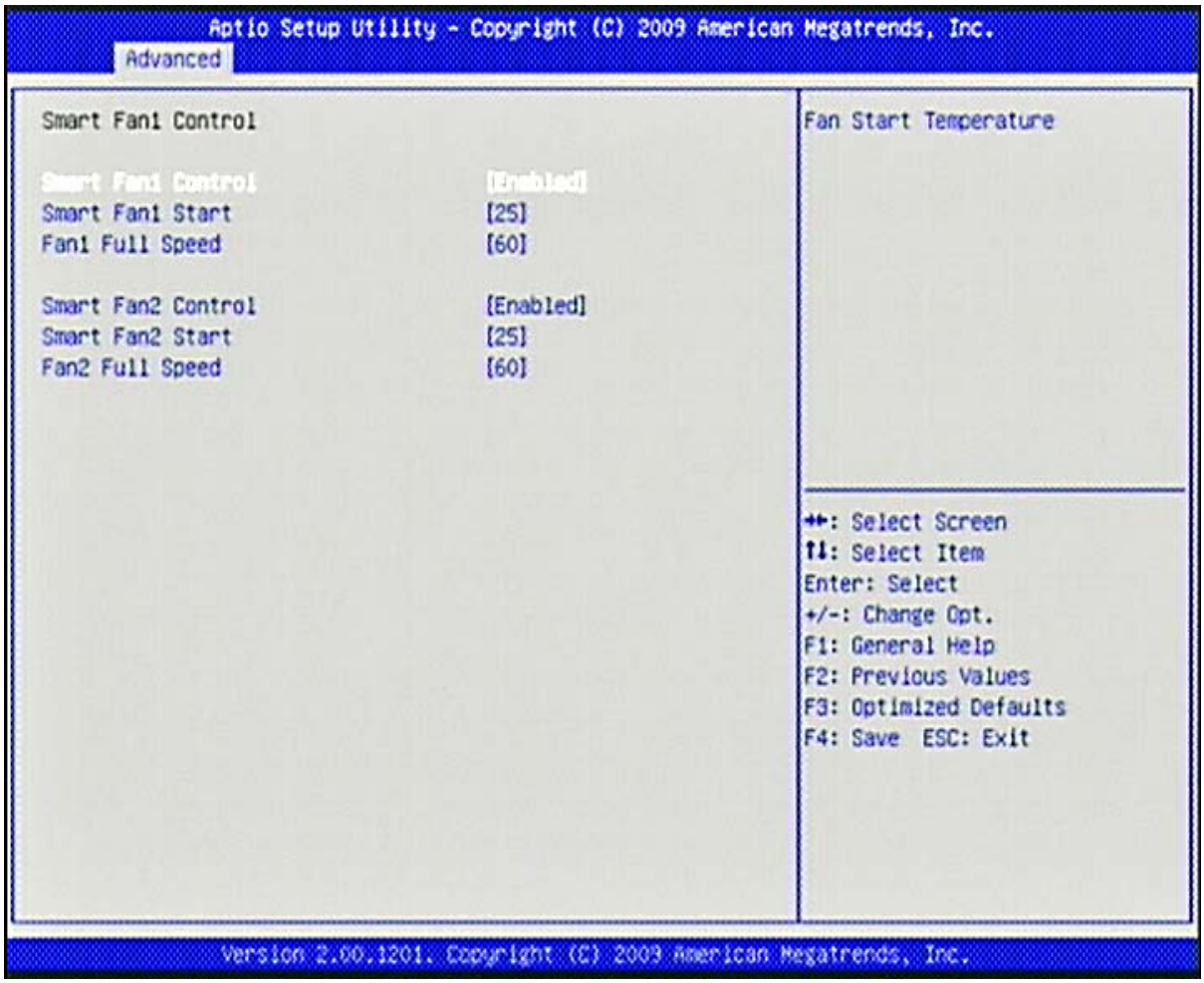
WDT controller

Choices: Disabled, Enabled.

Change Settings

Choices: WDT Disabled, 10 Seconds, 20 Seconds, 30 Seconds, 40 Seconds, 50 Seconds, 60 Seconds.

Smart Fan control

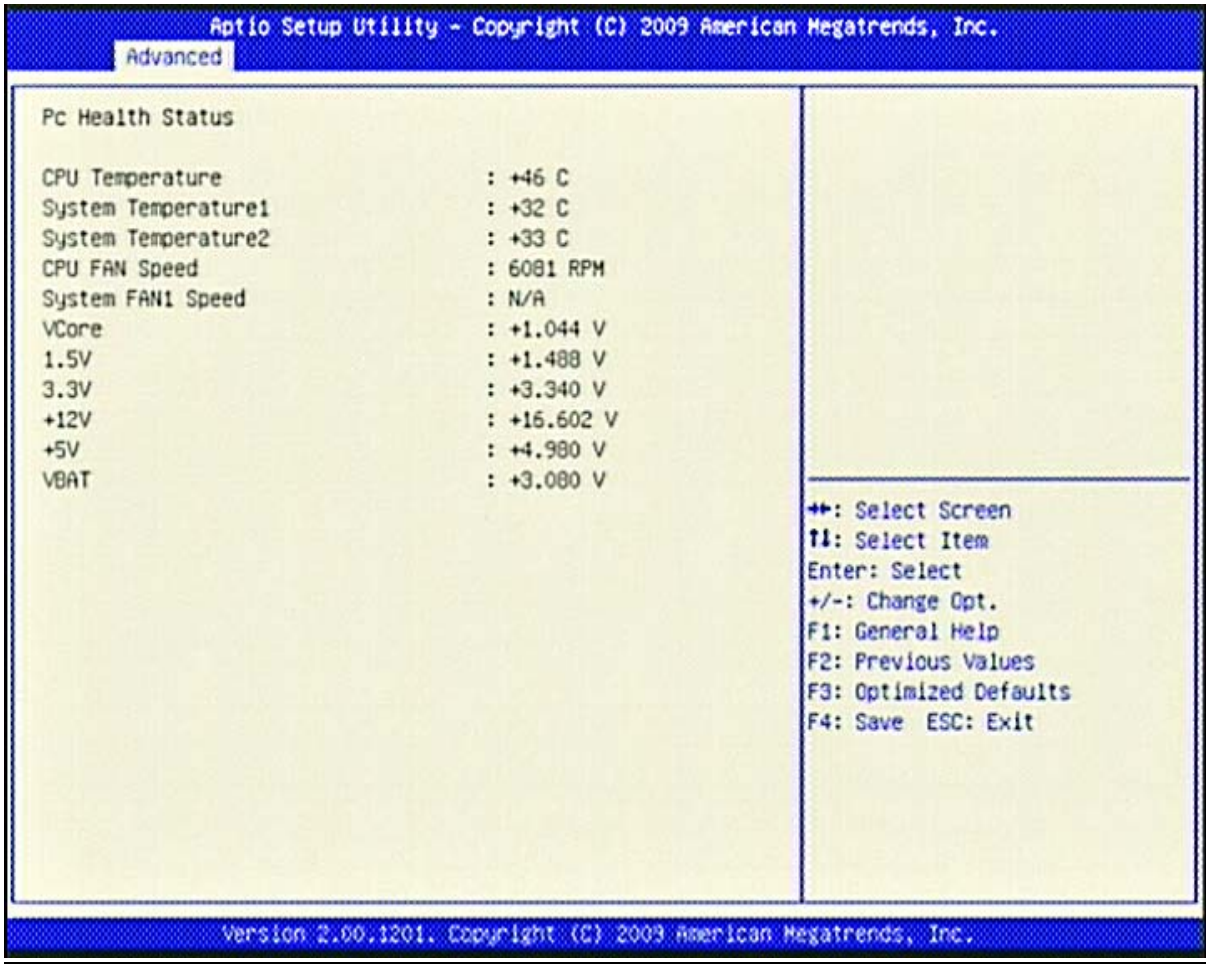


Smart Fan1/2 control
Choices: Disabled, Enabled.

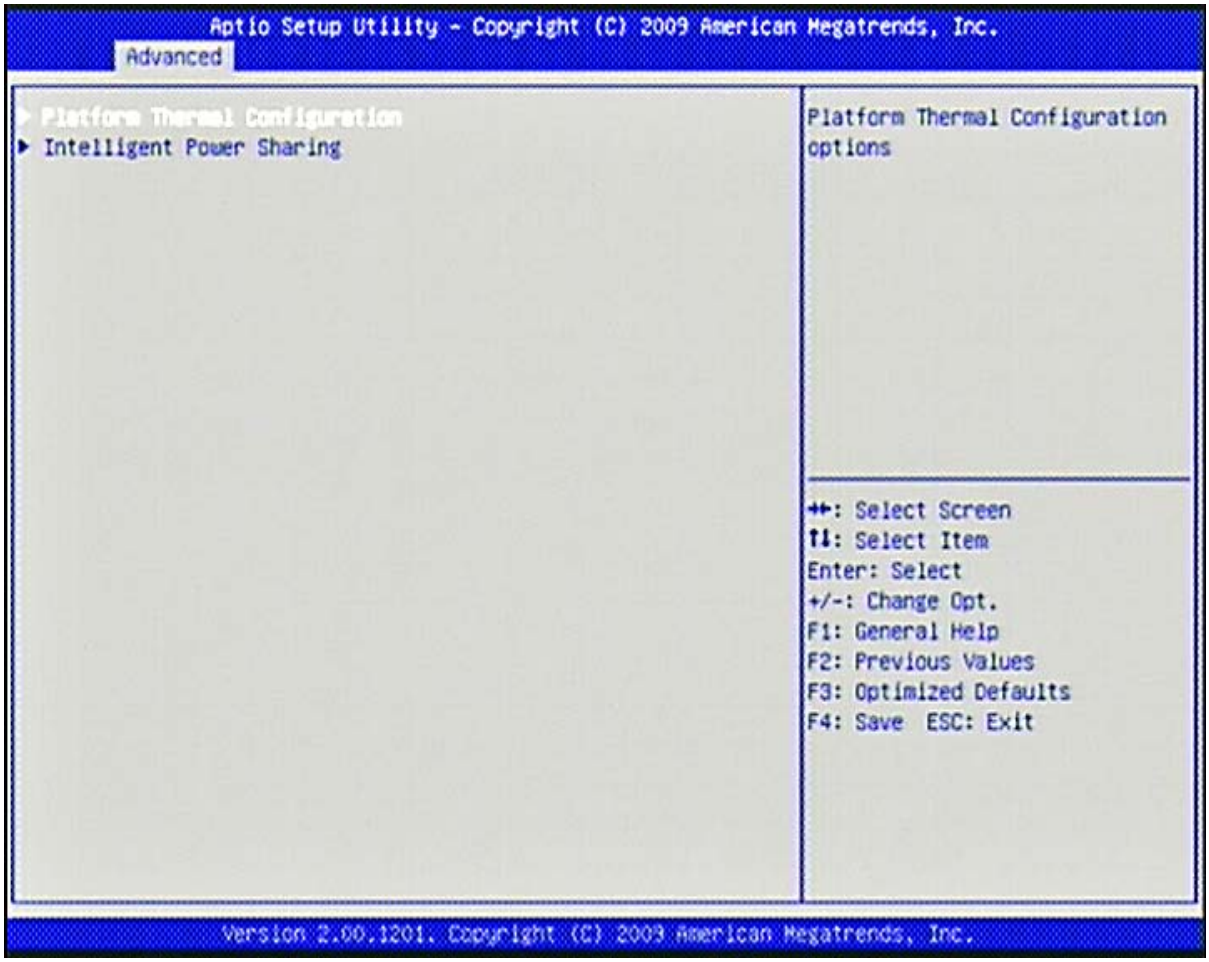
Smart Fan1/2 Start
Choices: 25, 30, 35, 40, 45, 50, 55, 60, 65, 70.

Fan1/2 Fill Speed
Choices: 60, 65, 70, 75.

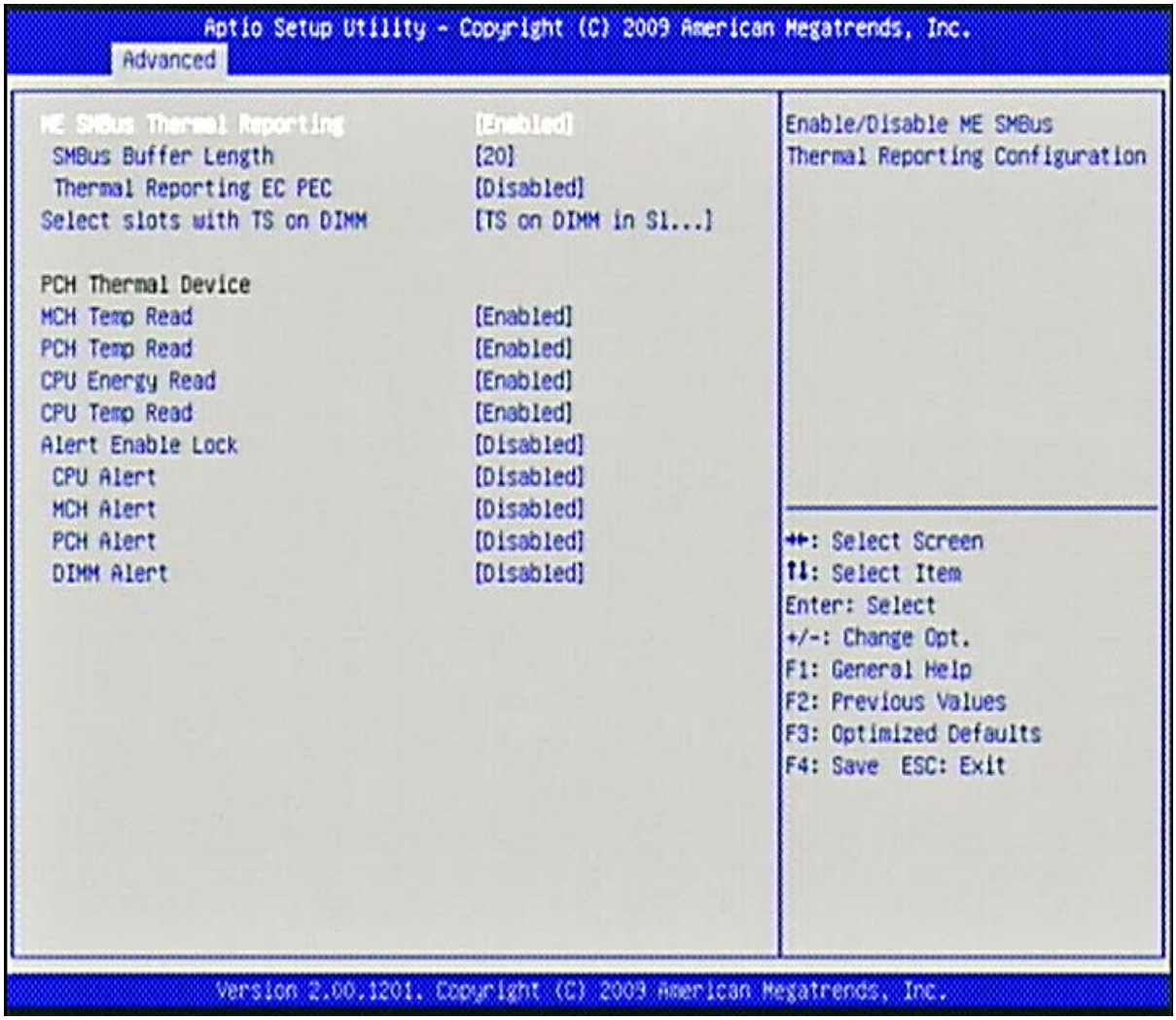
H/W monitor


Aptio Setup Utility – Copyright (C) 2009 American Megatrends, Inc.
Advanced
Pc Health Status
CPU Temperature : +46 C
System Temperature1 : +32 C
System Temperature2 : +33 C
CPU FAN Speed : 6081 RPM
System FAN1 Speed : N/A
VCore : +1.044 V
1.5V : +1.488 V
3.3V : +3.340 V
+12V : +16.602 V
+5V : +4.980 V
VBAT : +3.080 V
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save ESC: Exit
Version 2.00.1201. Copyright (C) 2009 American Megatrends, Inc.

Thermal Configuration



Platform Thermal Configuration



ME SMBus Thermal Reporting
Choices: Disabled, Enabled,

SMBus Buffer Length
Choices: 1,2,5,9,10,14,20

Thermal Reporting EC PEC
Choices: Disabled, Enabled,

Select Slots with TS on DIMM
Choices: NO TS on DIMM. TS on DIMM in Slot DIMM0, TS on DIMM in Slot DIMM1, TS on DIMM in Slot DIMM0 and DIMM1

MCH Temp Read
Choices: Disabled, Enabled,

PCH Temp Read
Choices: Disabled, Enabled,

CPU Energy Read
Choices: Disabled, Enabled,

Alert Enable Lock
Choices: Disabled, Enabled,

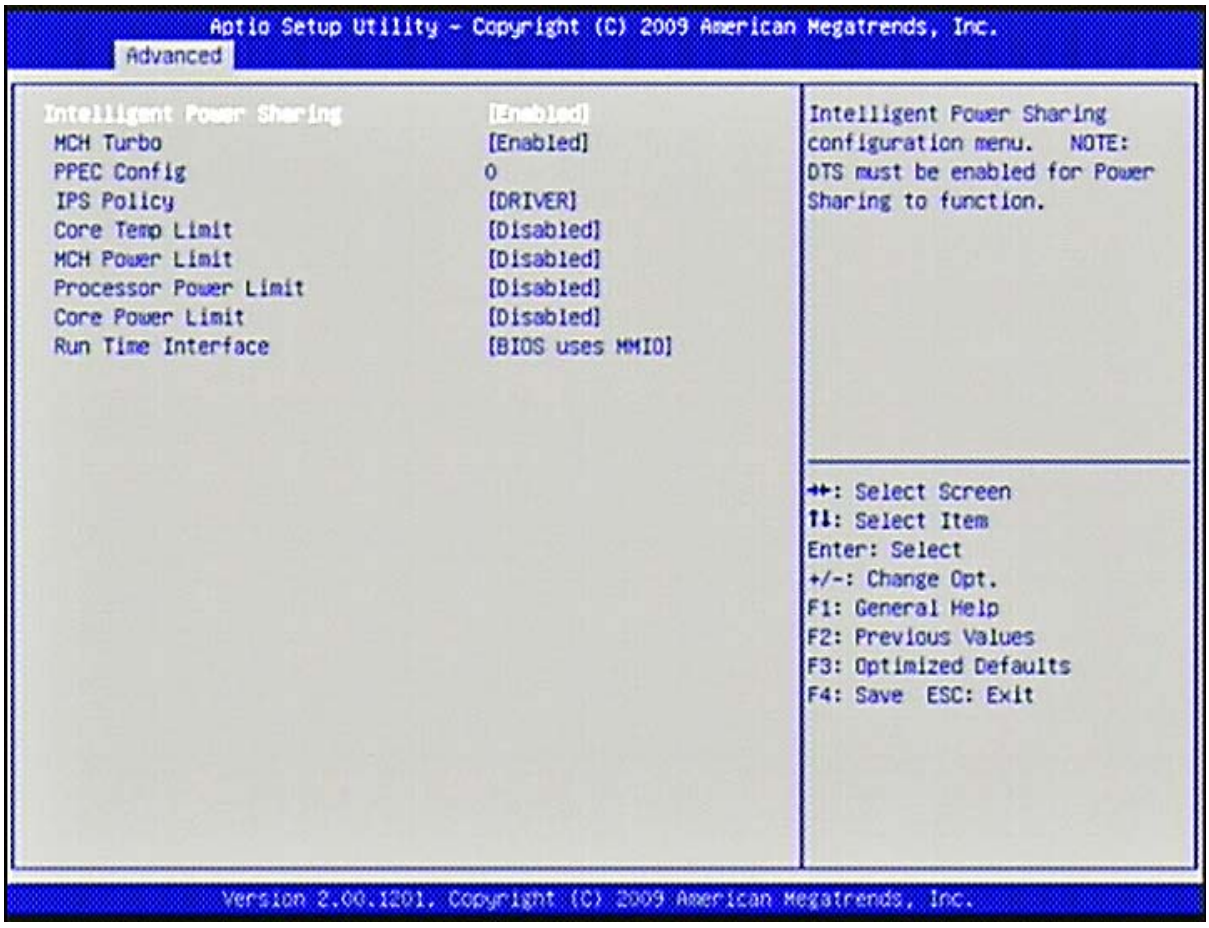
CPU Alert
Choices: Disabled, Enabled,

MCH Alert
Choices: Disabled, Enabled,

PCH Alert
Choices: Disabled, Enabled,

DIMM Alert
Choices: Disabled, Enabled,

Intelligent Power Sharing



Intelligent Power Sharing
Choices: Disabled, Enabled,

MCH Turbo
Choices: Disabled, Enabled,

PPEC Config
Processor Power Error Correction

Choices: 1 to 50

IPS Policy
Choices: DRIVER, PROCESSOR, BALANCED, GRAPHICS

Core Temp Limit
Choices: Disabled, Enabled,

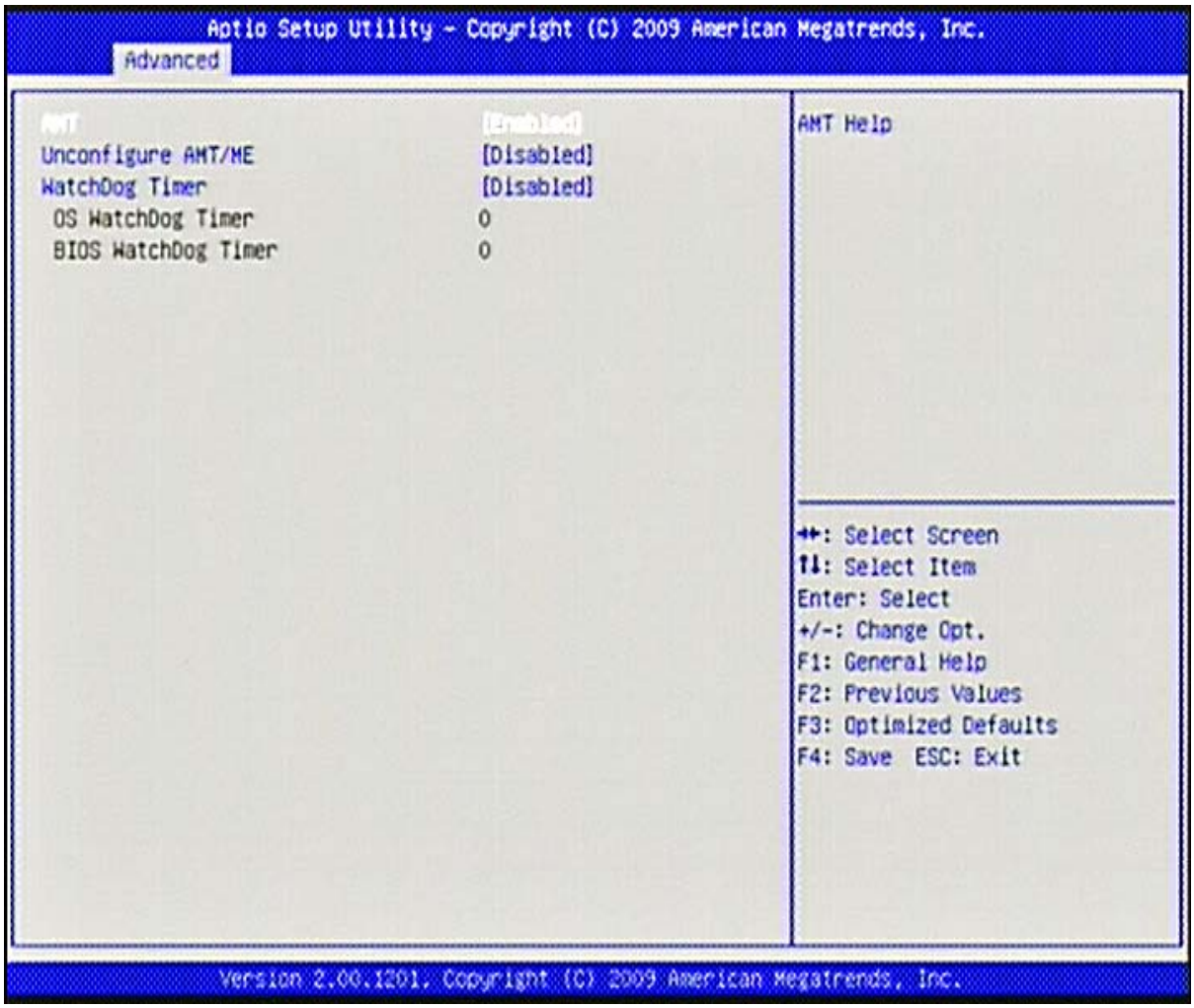
MCH Power Limit
Choices: Disabled, Enabled,

Processor Power Limit
Choices: Disabled, Enabled,

Core Power Limit
Choices: Disabled, Enabled,

Run Time Interface
Choices: BIOS with MMIO, EC uses SMBug

AMT Configuration

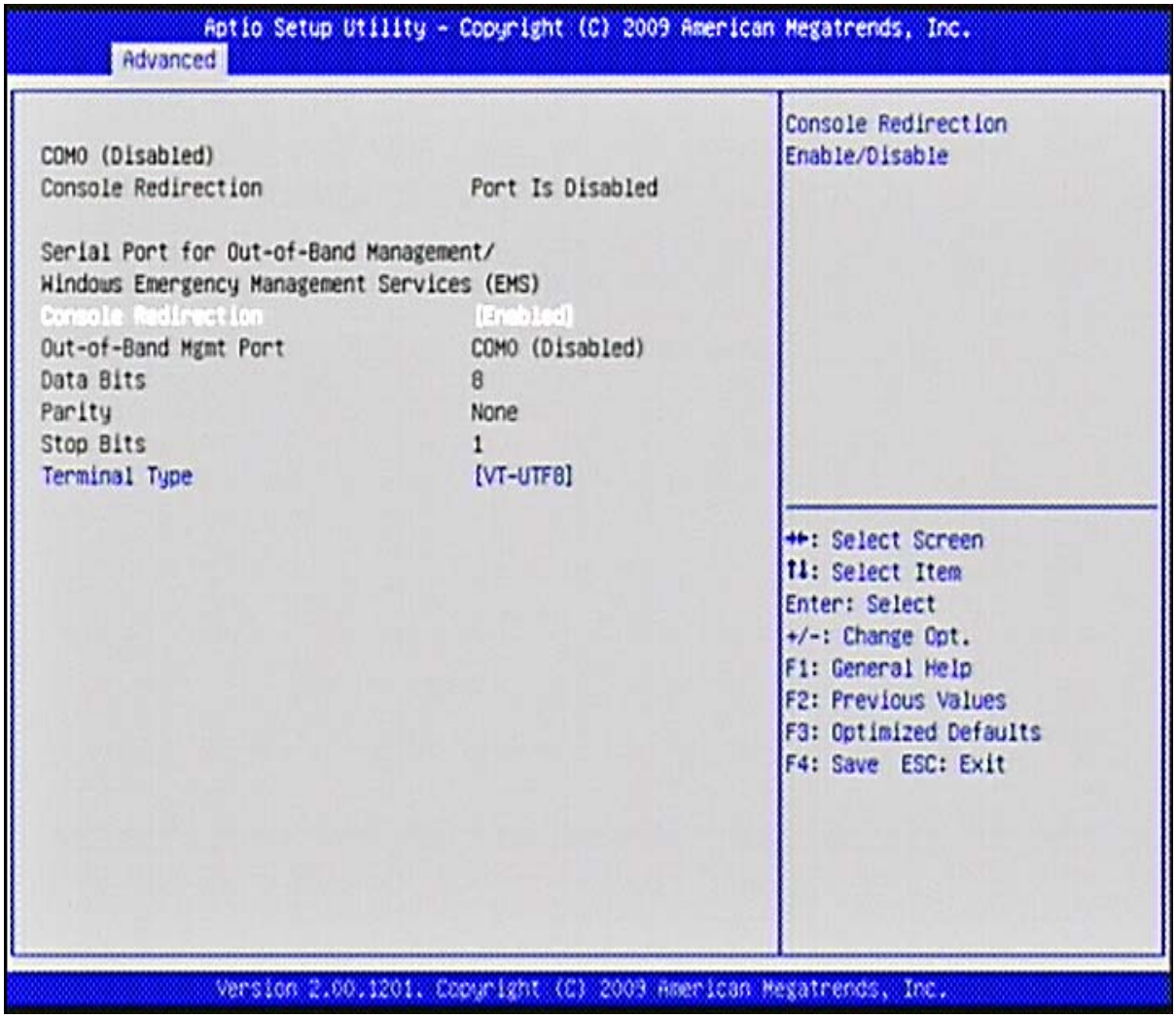


AMT
Choices: Disabled, Enabled,

Unconfigure AMT/ME
Choices: Disabled, Enabled,

WatchDog Timer
Choices: Disabled, Enabled

Serial Port Console Redirection



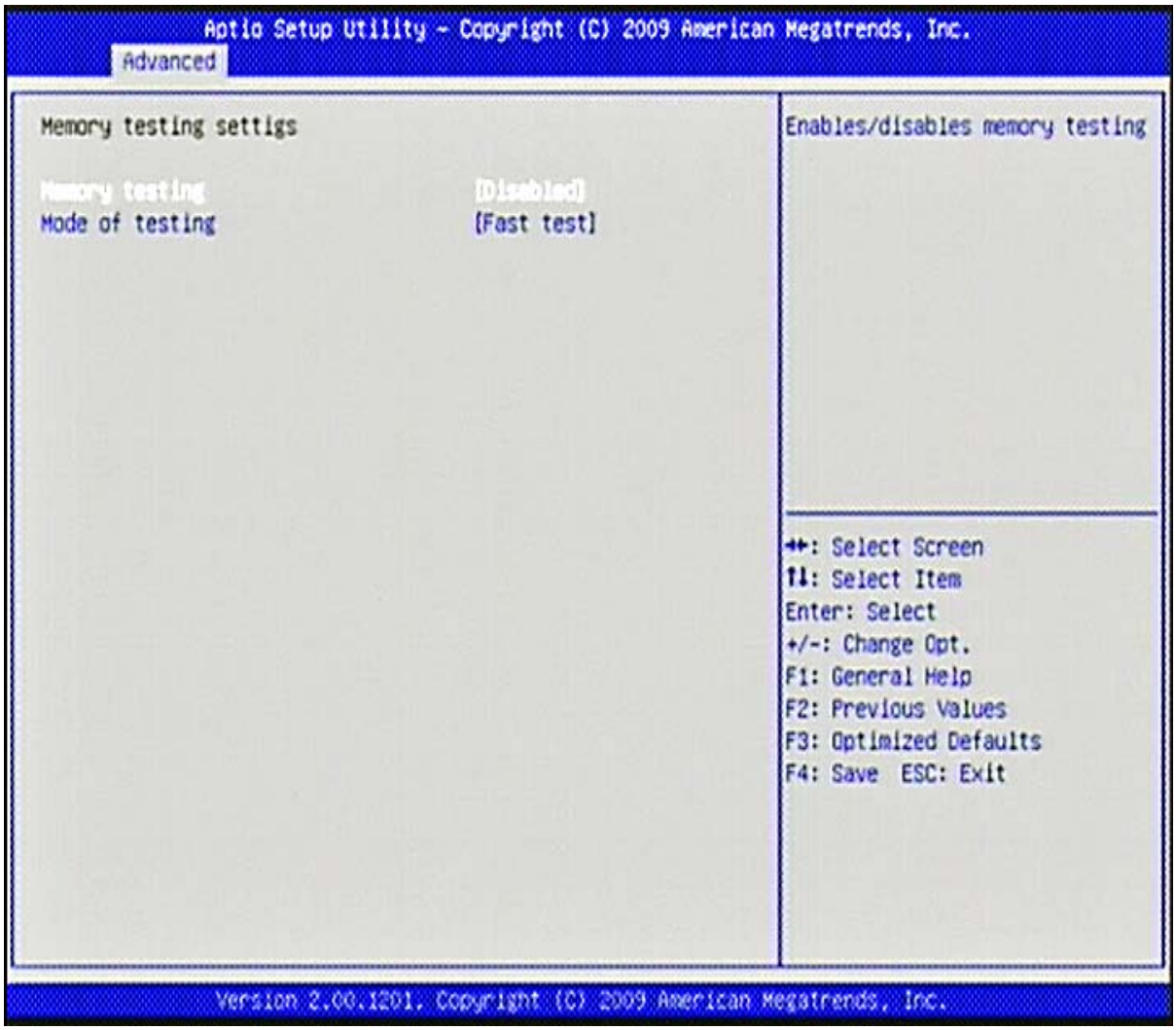
Console Redirection

Choices: Disabled, Enabled,

Terminal Type

Choices: VT100, VT100+, VT-UTF8, ANSI

Memory testing

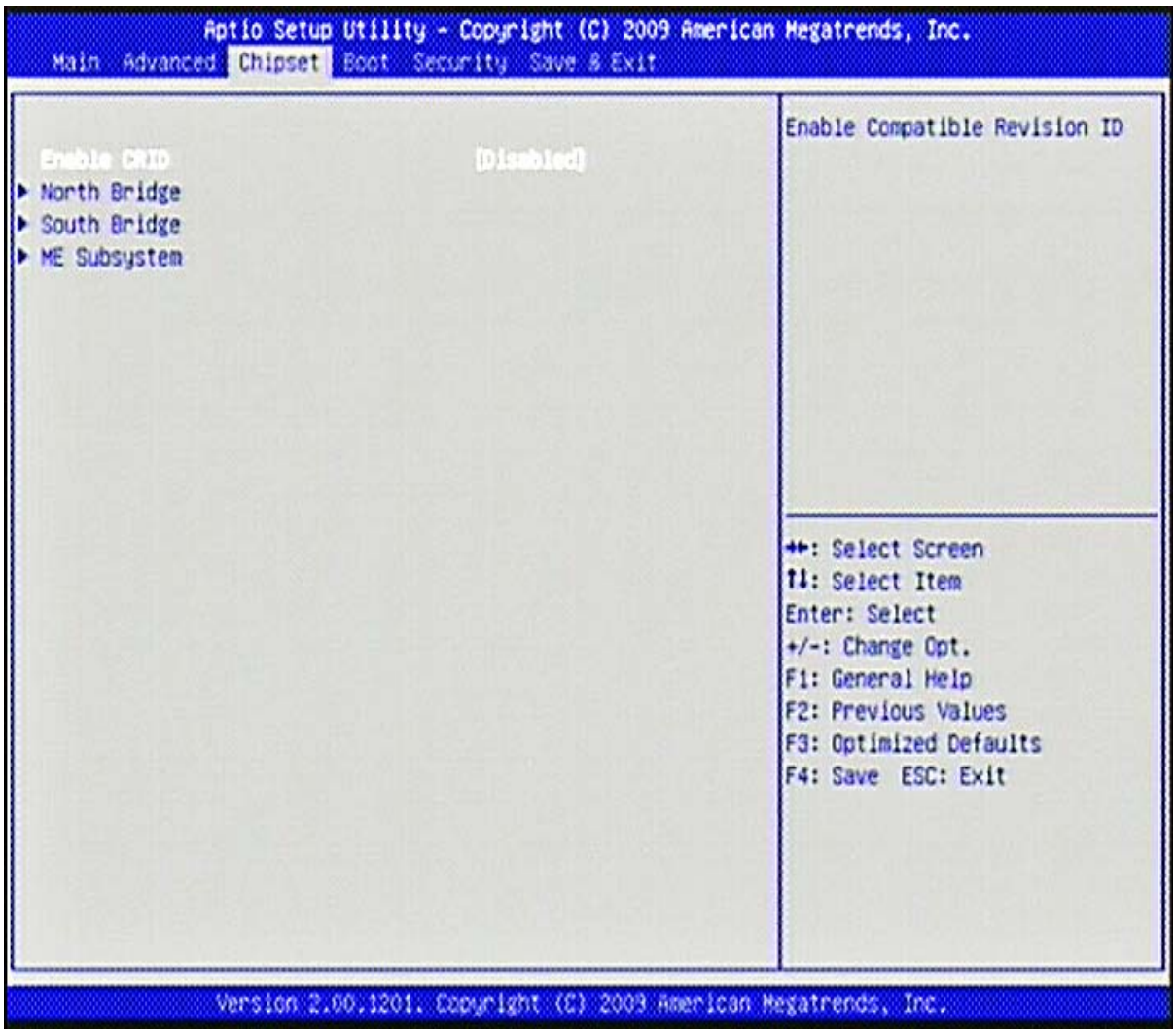


Memory testing
Choices: Disabled, Enabled,

Mode of testing
Choices: Normal test, Fast test.

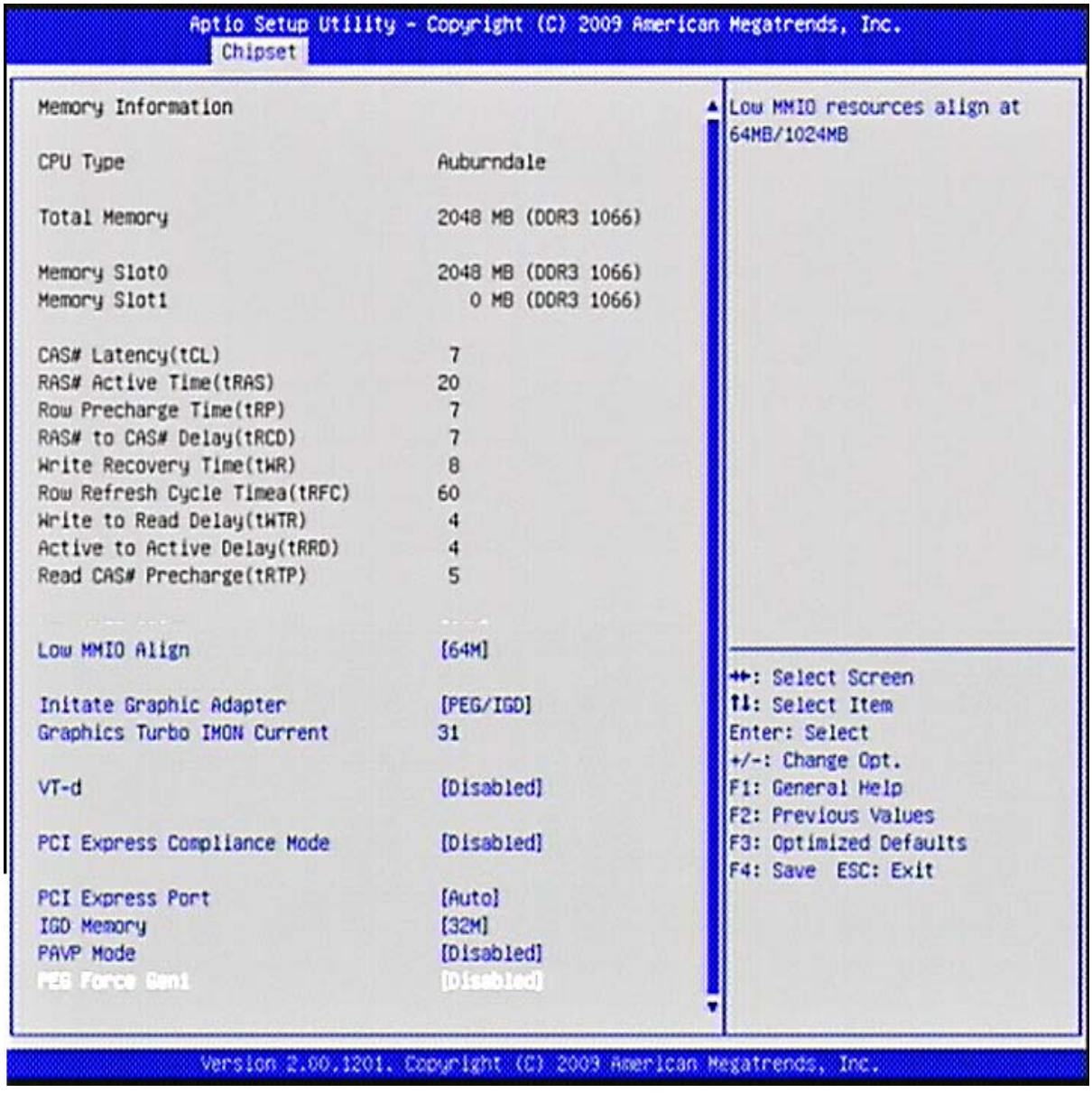
4.4 Chipset

This menu controls the advanced features of the onboard Northbridge and Southbridge.



Enable CRID
Choices: Disabled, Enabled,

North Bridge Chipset Configuration



Low MMIO Align
Choices: 64MB/1024MB

Initate Graphic Adapter
Select which graphics controller to use as the primary boot device.

Choices: IGD, PCI/IGD, PCI/PEG, PEG/IGD, PEG/PCI.

Graphics Turbo IMON Current
Choices: 14-31

VT-d
Choices: Disabled, Enabled.

PCI Express Compliance Mode
Choices: Disabled, Enabled,

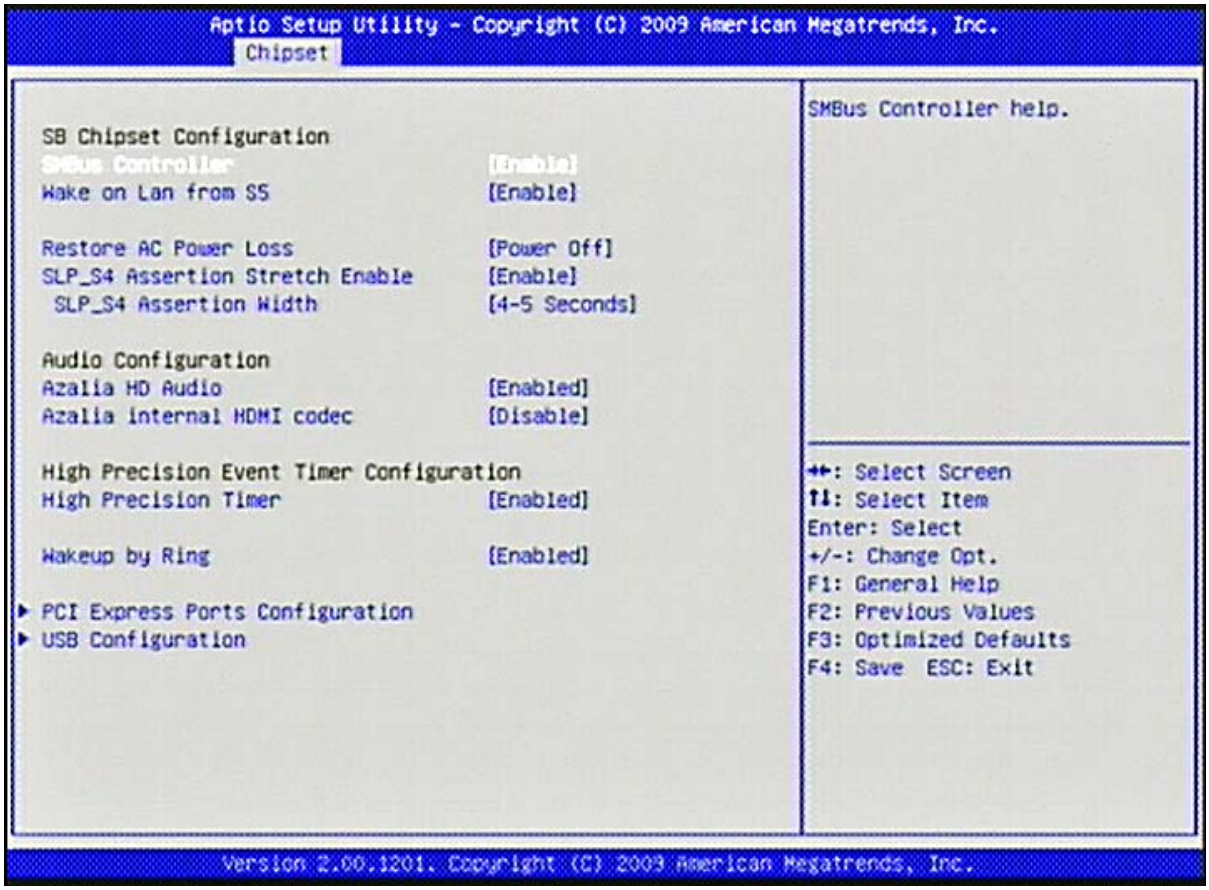
PCI Express Port
Choices: Disabled, Enabled, Auto

IGD Memory
Choices: Disabled, 32M, 64M, 128M

PAVP Mode
Choices: Disabled, Enabled,

PEG Force Gen1
Choices: Disabled, Enabled,

South Bridge Configuration



SMBus Controller
Choices: Disabled, Enabled,

Wake on Lan from S5
Choices: Disabled, Enabled,

Restore AC Power Loss
Choices: Power Off, Power On, Last State

SLP_S4 Assertion Stretch Enable
Choices: Disabled, Enabled,

SLP_S4 Assertion Width
Choices: 1-2, 2-3. 3-4, 4-5 seconds

Azalia HD Audio
Choices: Disabled, Enabled,

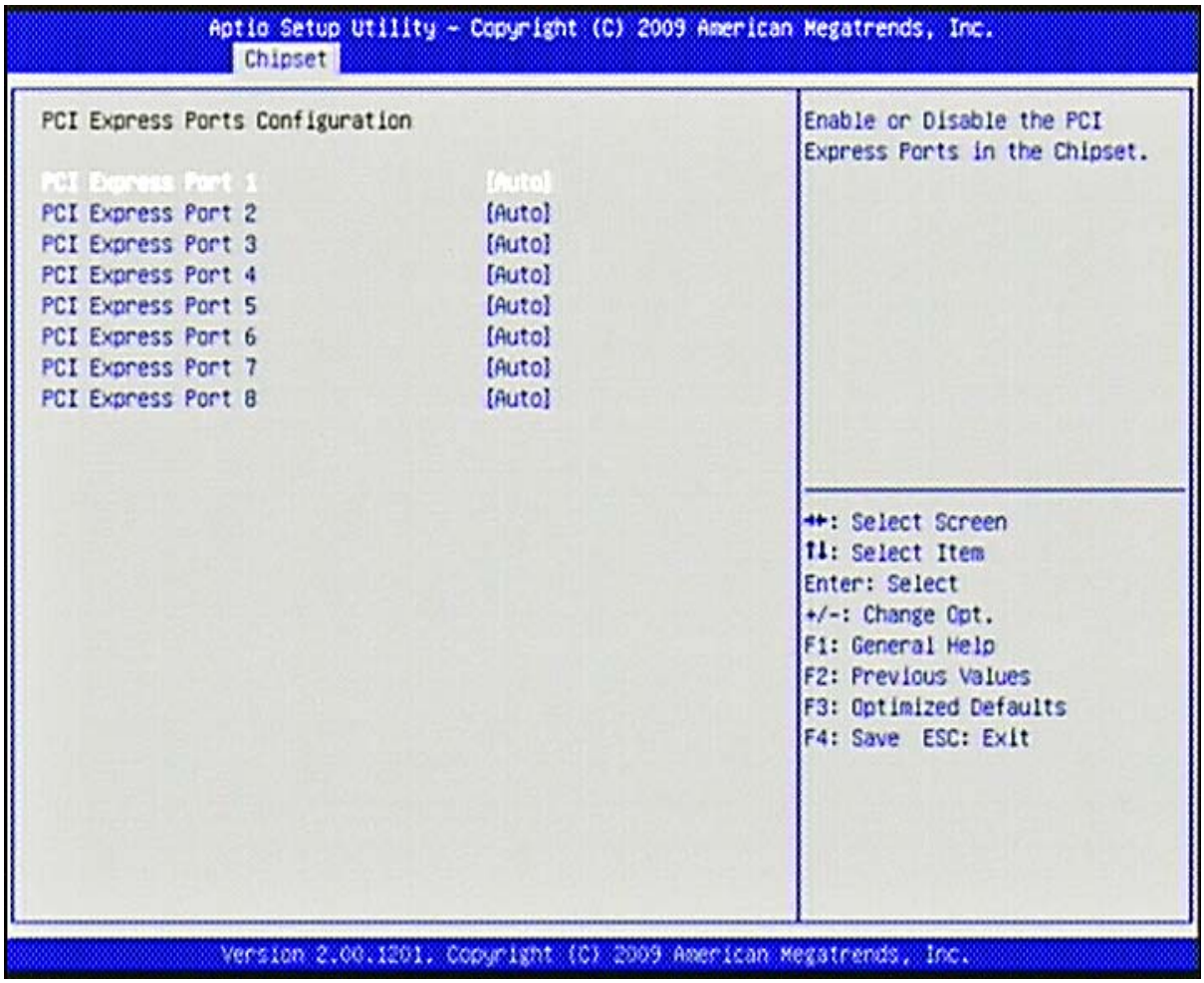
Azalia Internal HDMI Codec
Choices: Disabled, Enabled,

High Precision timer
Choices: Disabled, Enabled,

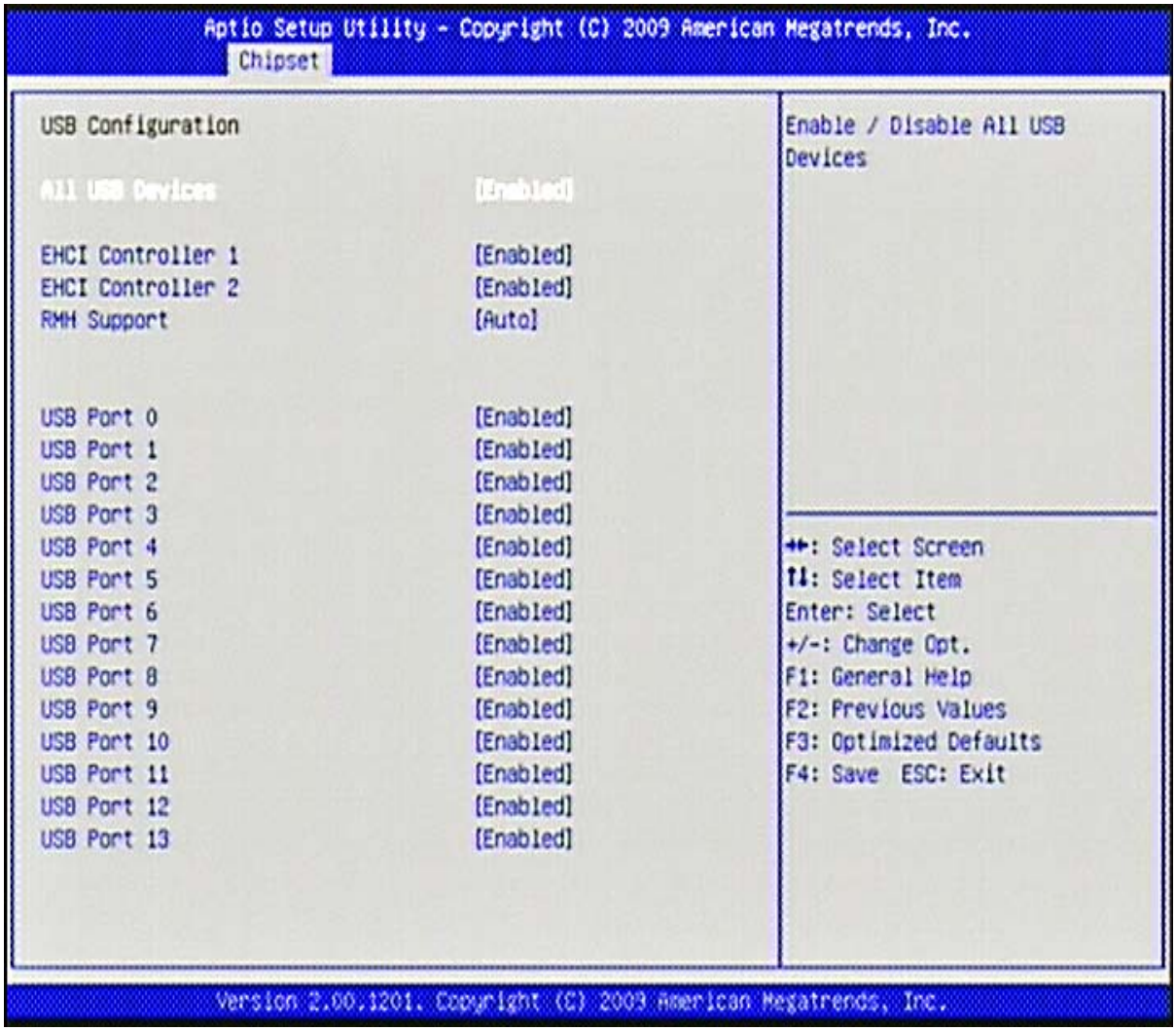
Wakeup by Ring
Choices: Disabled, Enabled,

PCI Express Ports Configuration

All PCI Express Ports can be set as choices: Disabled, Enabled, Auto



USB Configuration



ALL USB Devices
Choices: Disabled, Enabled

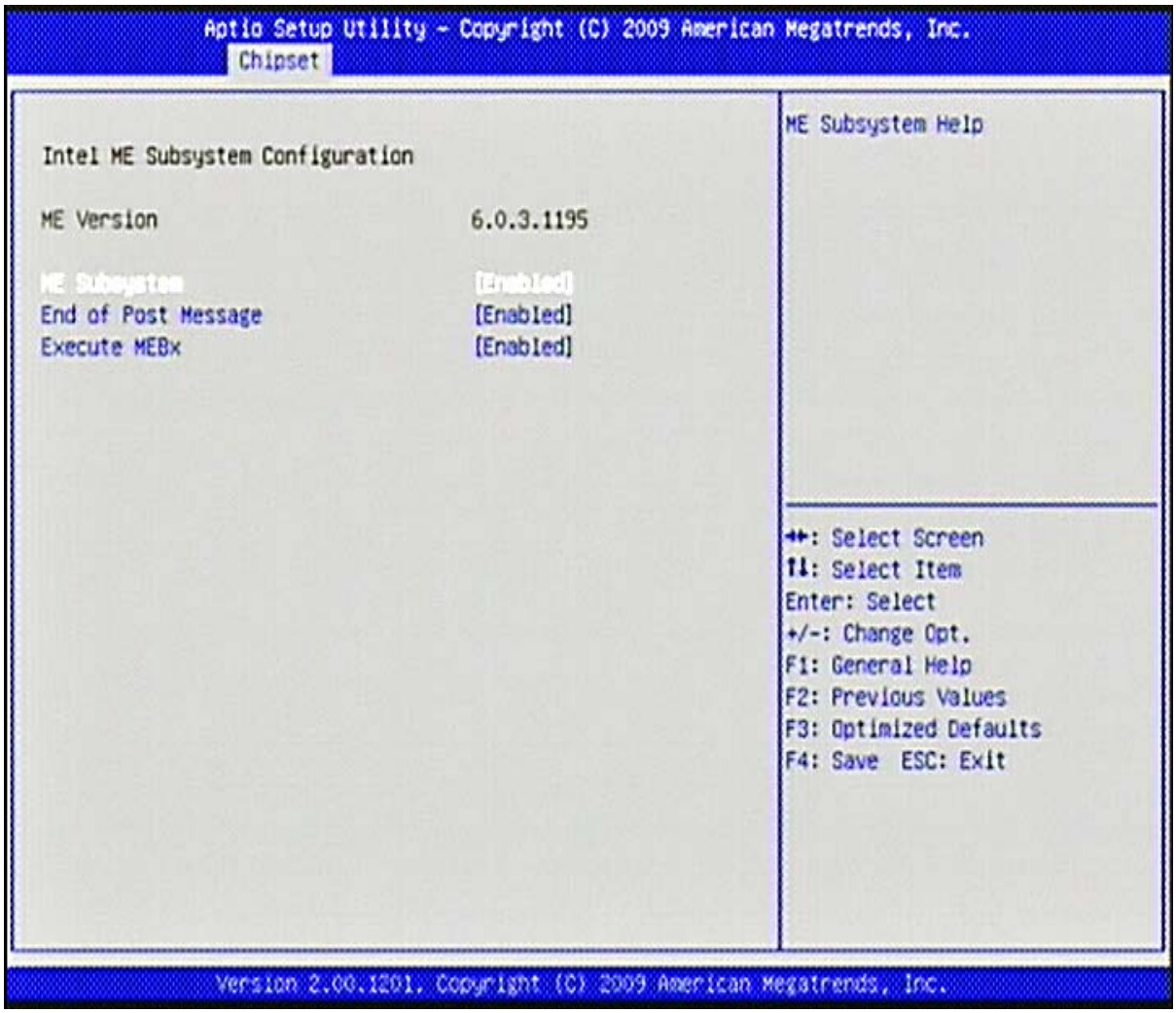
EHCI Controller 1
Choices: Disabled, Enabled

EHCI Controller 2
Choices: Disabled, Enabled

RHM Support
Choices: Disabled, Enabled, Auto

USB Port 0/1/2/3/4/5/6/7/8/9/10/11/12/13
Choices: Disabled, Enabled

ME Subsystem Configuration



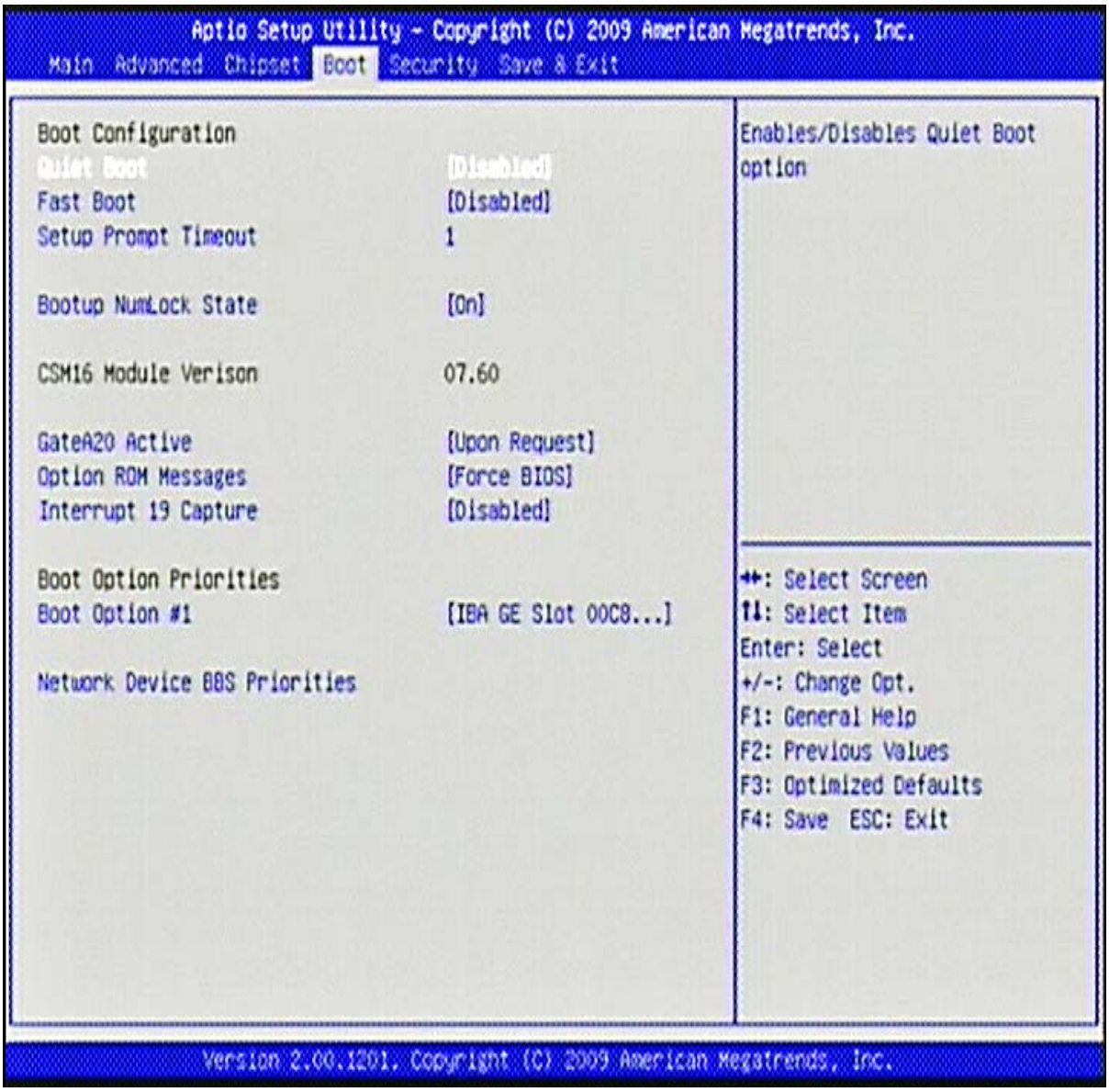
ME Subsystem
Choices: Enabled, Disabled.

End of Post Message
Choices: Enabled, Disabled.

Execute MEBx
Choices: Enabled, Disabled.

4.5 Boot

Use this menu to specify the priority of boot devices.



Quiet Boot

This BIOS feature determines if the BIOS should hide the normal POST messages with the motherboard or system manufacturer's full-screen logo. When it is enabled, the BIOS will display the full-screen logo during the boot-up sequence, hiding normal POST messages.

When it is disabled, the BIOS will display the normal POST messages, instead of the full-screen logo.

Please note that enabling this BIOS feature often adds 2-3 seconds of delay to the booting sequence. This delay ensures that the logo is displayed for a sufficient amount of time. Therefore, it is recommended that you disable this BIOS feature for a faster boot-up time.

Choices: Disabled, Enabled.

Fast Boot

Enabling this setting will cause the BIOS power-on self test routine to skip some of its tests during boot up for faster system boot.

Choices: Disabled, Enabled.

Setup Prompt Timeout
Choices: 1-65535

Bootup Num-Lock State

This setting is to set the Num Lock status when the system is powered on. Setting to [On] will turn on the Num Lock key when the system is powered on. Setting to [Off] will allow users to use the arrow keys on the numeric keypad.

Choices: On, Off.

GateA20 Active
Choices: Upon Request, Always

Option ROM Messages
This item is used to determine the display mode when an optional ROM is initialized during POST. When set to [Force BIOS], the display mode used by AMI BIOS is used. Select [Keep Current] if you want to use the display mode of optional ROM.

Choices: Force BIOS, Keep Current.

Interrupt 19 Capture

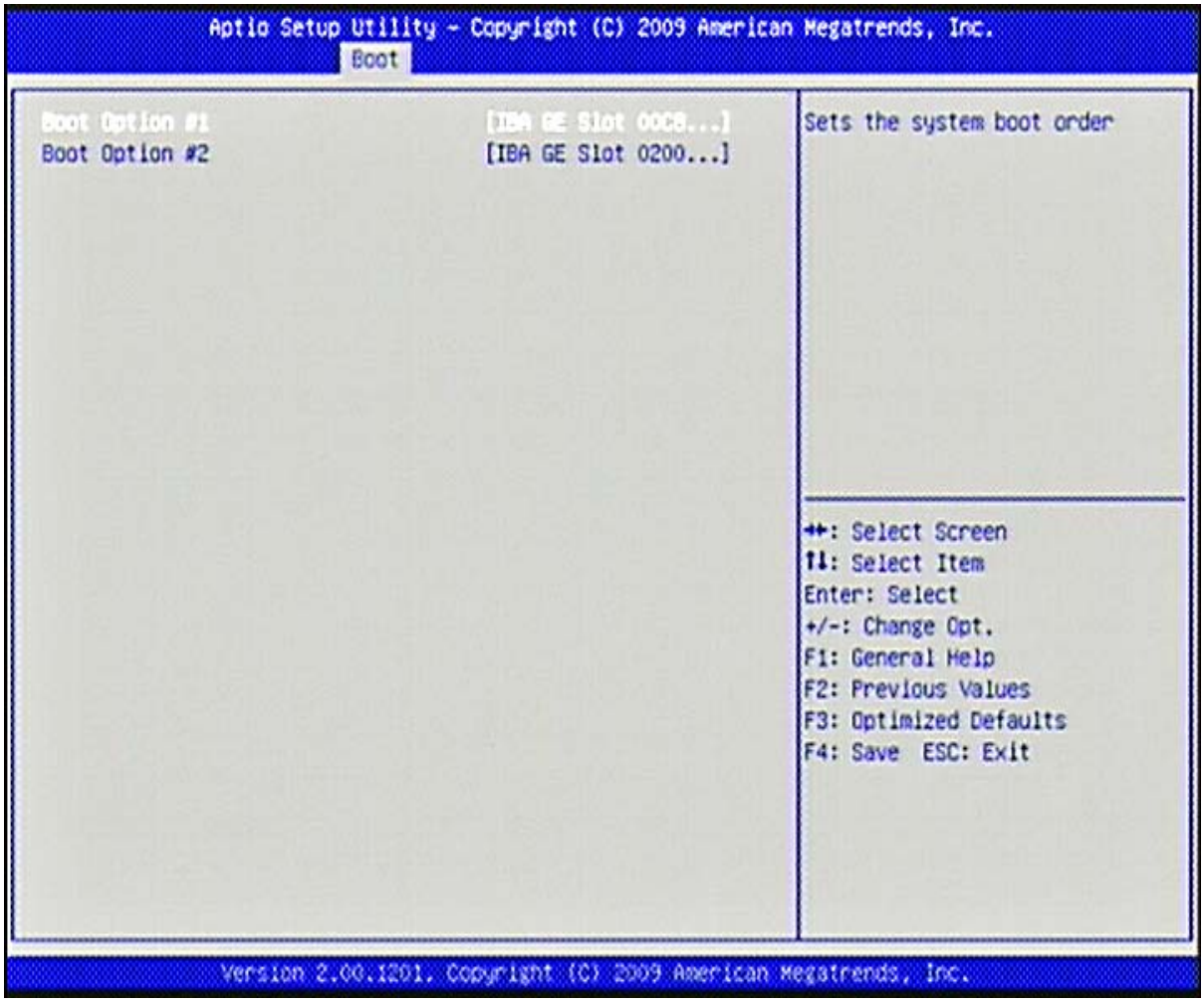
Interrupt 19 is the software interrupt that handles the boot disk function. When enabled, this BIOS feature allows the ROM BIOS of these host adaptors to "capture" Interrupt 19 during the boot process so that drives attached to these adaptors can function as bootable disks. In addition, it allows you to gain access to the host adaptor's ROM setup utility, if one is available.

When disabled, the ROM BIOS of these host adaptors will not be able to "capture" Interrupt 19. Therefore, you will not be able to boot operating systems from any bootable disks attached to these host adaptors. Nor will you be able to gain access to their ROM setup utilities.

Choices: Disabled, Enabled.

Boot Option # 1
Choices: Built-in EFI Shell

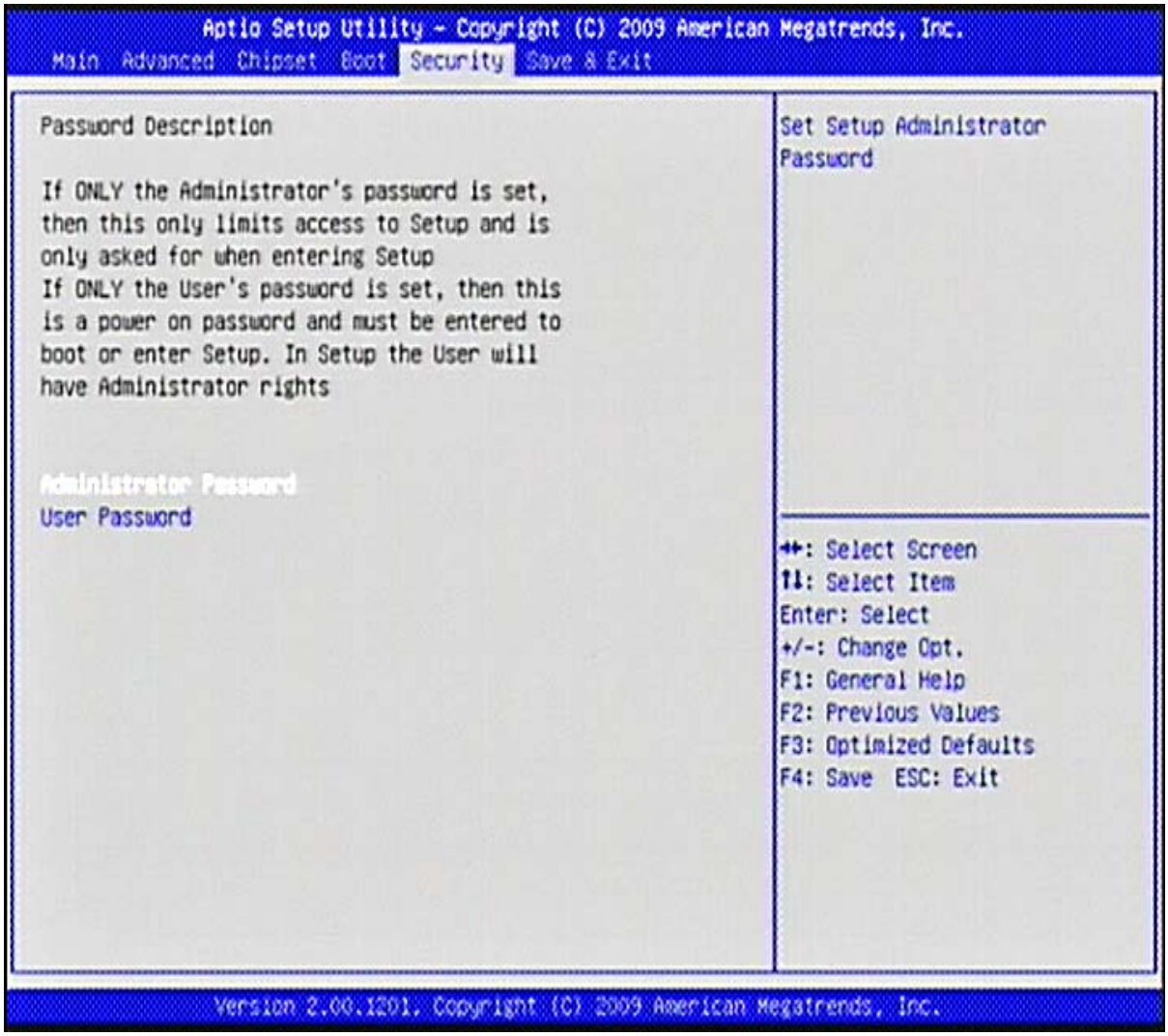
Network Device BBS Priorities



Boot Option # 1/2
Choices: IBA GE Slot 00C8 v1336, IBA GE Slot 0200 v1336, Disabled.

4.6 Security

Use this menu to set supervisor and user passwords.



Administrator Password

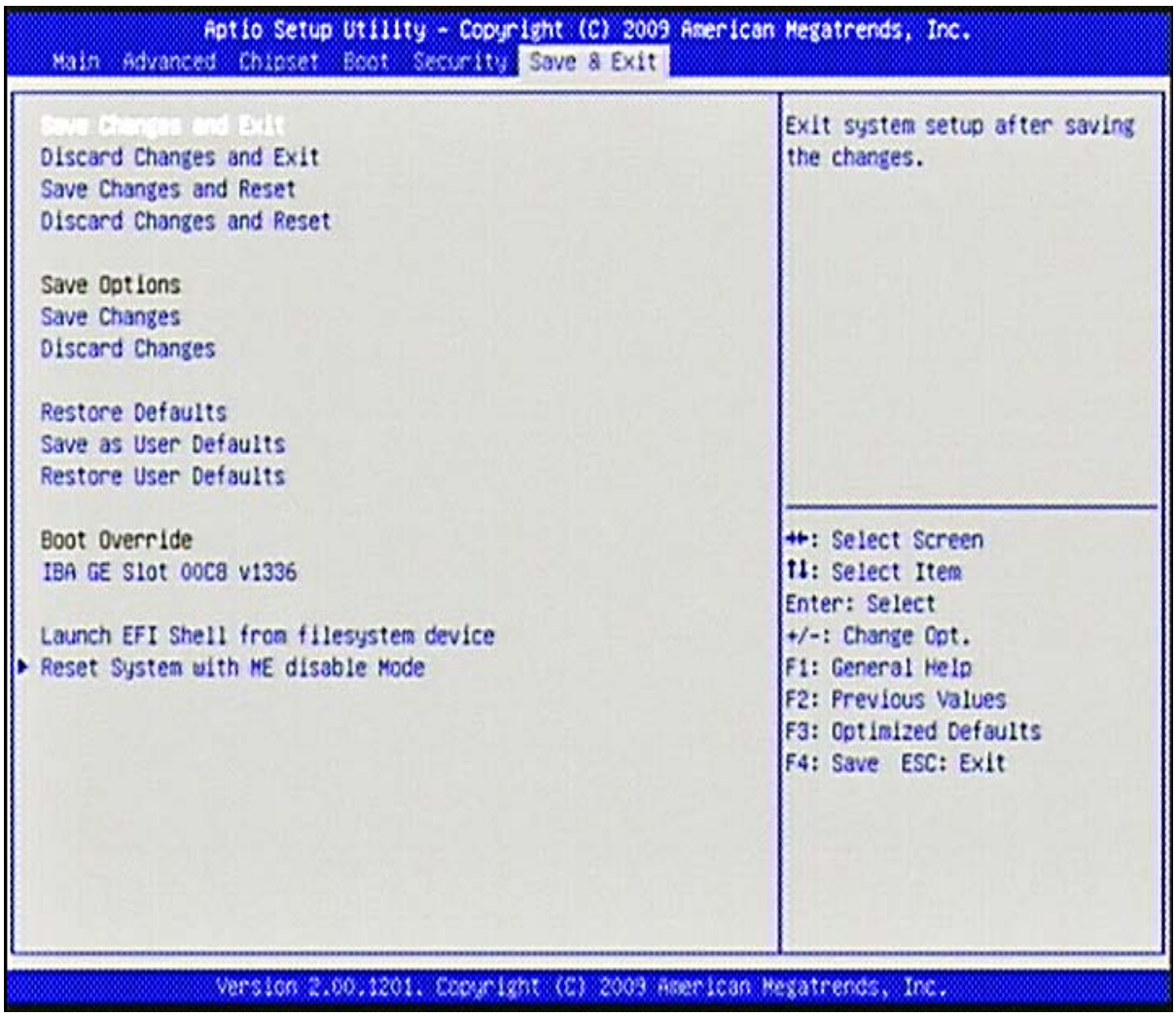
Administrator Password controls access to the BIOS Setup utility. These settings allow you to set or change the supervisor password.

User Password

User Password controls access to the system at boot. These settings allow you to set or change the user password.

4.7 Save & Exit

This menu allows you to load the BIOS default values or factory default settings into the BIOS and exit the BIOS setup utility with or without changes.



Save Changes and Exit

Exit System Setup and save your changes to CMOS. Pressing <Enter> on this item asks for confirmation: Save changes to CMOS and exit the Setup Utility.

Discard Changes and Exit

Abandon all changes and exit the Setup Utility.

Save Changes and Reset

Exit System Setup and save your changes to CMOS then reboot.

Discard Changes and Reset

Abandon all changes and exit the Setup Utility then reboot

Save Changes
Save all changes and continue with the Setup Utility.

Discard Changes
Abandon all changes and continue with the Setup Utility.

Restore Defaults
Use this menu to load the default values set by the SBC manufacturer specifically for optimal performance of the SBC.

Save as User Defaults
Save all changes and considers as User's default.

Restore User Default
Restore the setting according to User's default

Launch EFI Shell from filesystem device
To enter the Built-in EFI shell for further modification such as upgrade BIOS.

Reset System with ME disable Mode
Reset the system with ME disabled.

Chapter 5
Troubleshooting

This chapter provides a few useful tips to quickly get ROBO-8210VG2AR running with success. As basic hardware installation has been addressed in Chapter 2, this chapter will primarily focus on system integration issues, in terms of BIOS setting, and OS diagnostics.

5.1 Hardware Quick Installation

ATX Power Setting
Unlike other Single board computer, ROBO-8210VG2AR supports ATX only and therefore is only able to run on PICMG 1.3 backplane. To know whether your backplane is PICMG 1.3 backplane, please contact with vendor or manufacturer.

Serial ATA Hard Disk Setting for IDE/RAID/AHCI
Unlike IDE bus, each Serial ATA channel can only connect to one SATA hard disk at a time; there are total four connectors, SATA1~4 port. The installation of Serial ATA is simpler and easier than IDE, because SATA hard disk doesn't require setting up Master and Slave, which can reduce mistake of hardware installation. All you need to operate IDE, RAID (0/1/5/10) and AHCI application for system, please follow up setting guide in BIOS programming (Table 5-1).

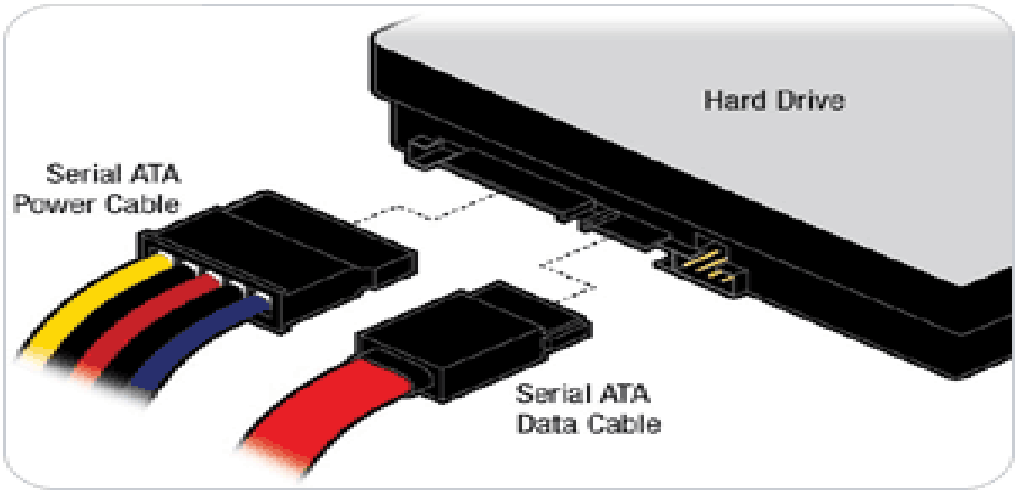
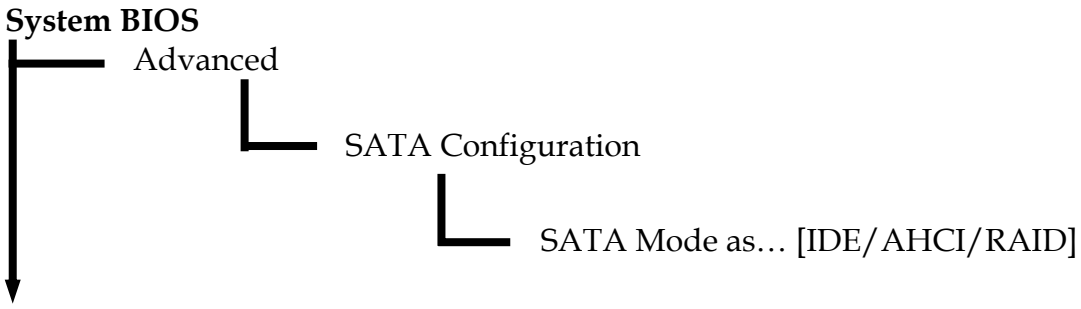


Table. 5-1 SATA Mode setting guide



5.2 BIOS Setting

It is assumed that users have correctly adopted modules and connected all the devices cables required before turning on ATX power. CPU, CPU Fan, 240-pin DDR3 SDRAM, keyboard, mouse, floppy drive, SATA hard disk, DVI-I connector, device power cables, ATX accessories are good examples that deserve attention. With no assurance of properly and correctly accommodating these modules and devices, it is very possible to encounter system failures that result in malfunction of any device.

To make sure that you have a successful start with ROBO-8210VG2AR, it is recommended, when going with the boot-up sequence, to hit "DEL" key and enter the BIOS setup menu to tune up a stable BIOS configuration so that you can wake up your system far well.

Loading the default optimal setting

When prompted with the main setup menu, please scroll down to "**Load Optimal Defaults**", press "Enter" and "Y" to load in default optimal BIOS setup. This will force your BIOS setting back to the initial factory configuration. It is recommended to do this so you can be sure the system is running with the BIOS setting that Portwell has highly endorsed. As a matter of fact, users can load the default BIOS setting any time when system appears to be unstable in boot up sequence.

Auto Detect Hard Disks

In the BIOS => Standard CMOS setup menu, pick up any one from Primary/Secondary Master/Slave IDE ports, and press "Enter". Setup the selected IDE port and its access mode to "Auto". This will force system to automatically pick up the IDE devices that are being connected each time system boots up.

Improper disable operation

There are too many occasions where users disable a certain device/feature in one application through BIOS setting. These variables may not be set back to the original values when needed. These devices/features will certainly fail to be detected.

When the above conditions happen, it is strongly recommended to check the BIOS settings. Make sure certain items are set as they should be. These include the COM1/ COM2 ports, USB ports, external cache, on-board VGA and Ethernet.

It is also very common that users would like to disable a certain device/port to release IRQ resource. A few good examples are

Disable COM1 serial port to release IRQ #4
Disable COM2 serial port to release IRQ #3

Etc…

A quick review of the basic IRQ mapping is given below for your reference.

IRQ#	Description
IRQ #0	**System Timer**
IRQ #1	**Keyboard Event**
IRQ #2	**Usable IRQ**
IRQ #3	**COM2**
IRQ #4	**COM1**
IRQ #5	**Usable IRQ**
IRQ #6	**Diskette Event**
IRQ #7	**Usable IRQ**
IRQ #8	**Real-Time Clock**
IRQ #9	**Usable IRQ**
IRQ #10	**Usable IRQ**
IRQ #11	**Usable IRQ**
IRQ #12	**IBM Mouse Event**
IRQ #13	**Coprocessor Error**
IRQ #14	**Hard Disk Event**
IRQ #15	**Usable IRQ**

It is then very easy to find out which IRQ resource is ready for additional peripherals. If IRQ resource is not enough, please disable some devices listed above to release further IRQ numbers.

5.3 FAQ

Installation Problem

Question:I forget my password of system BIOS, what am I supposed to do?

Answer: You can simply short 1-2 pins on JP3 to clean your password.

Note:
Please visit our technical web site at
http://www.portwell.com.tw
For additional technical information, which is not covered in this manual, you can mail to tsd@mail.portwell.com.tw or you can also send mail to our sales, they wull be very delighted to forward them to us.

System Memory Address Map

Each On-board device in the system is assigned a set of memory addresses, which also can be identical of the device. The following table lists the system memory address used.

Memory Area	Size	Description
0000-003F	**1K**	**Interrupt Area**
0040-004F	**0.3K**	**BIOS Data Area**
0050-006F	**0.5K**	**System Data**
0070-0E2E	**54K**	**DOS**
0E2F-0F6B	**5K**	**Program Area**
0F6C-9B7F	**562K**	**【Available】**
First Meg	**-- Conventional memory end at 624K --**	
9C00-9D3F	**5K**	**Extended BIOS Area**
9D40-9FFF	**11K**	**Unused**
A000-AFFF	**64K**	**VGA Graphics**
B000-B7FF	**32K**	**Unused**
B800-BFFF	**32K**	**VGA Text**
C000-CFDF	**63K**	**Video ROM**
CFC0-EFFF	**129K**	**Unused**
F000-FFFF	**64K**	**System ROM**
HMA	**64K**	**First 64K Extended**

Interrupt Request Lines (IRQ)

Peripheral devices can use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

IRQ#	Current Use	Default Use
IRQ 0	System ROM	System Timer
IRQ 1	System ROM	Keyboard Event
IRQ 2	【Unassigned】	Usable IRQ
IRQ 3	System ROM	COM2
IRQ 4	System ROM	COM1
IRQ 5	【Unassigned】	Usable IRQ
IRQ 6	System ROM	Diskette Event
IRQ 7	【Unassigned】	Usable IRQ
IRQ 8	System ROM	Real-Time Clock
IRQ 9	【Unassigned】	Usable IRQ
IRQ 10	【Unassigned】	Usable IRQ
IRQ 11	Video ROM	Usable IRQ
IRQ 12	System ROM	IBM Mouse Event
IRQ 13	System ROM	Coprocessor Error
IRQ 14	System ROM	Hard Disk Event
IRQ 15	【Unassigned】	Usable IRQ