RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SH7-A827A/E	Rev.	1.00	
Title	SH7455 Group, SH7456 Group User's N Hardware Errata Rev.A	lanual	Information Category	Technical Notification	1		
		Lot No.					
Applicable Product	SH7455 Group, SH7456 Group		Reference Document	SH7455 Group, SH74 User's Manual: Hardv (R01UH0030EJ0110)	ware Rev		

Since we changed the following contents of "SH7455 Group, SH7456 Group User's Manual: Hardware Rev.1.10(Published on September 22, 2011)", we announce you.

Please use attached errata in the case of use of SH7455 Group, SH7456 Group User's Manual: Hardware Rev.1.10.

Appending Document: "SH7455 Group, SH7456 Group User's Manual: Hardware Rev.1.10" errata REV.A – 2 sheets



Rev.	Page	Part		Contents				
			Incorrect description corrected (the 12 th line)					
Adds		25.4.6 (3)		stop receiving when MST bit =		RCVD bit ir	n the	
by	25-23	Receive	ICCR1 register to "1", then read the ICDRR register.					
REV.A		Operation		o stop receiving when MST bit			n the	
			ICCR1 register to "1", then read the ICDRR register.					
		32.7.1					CC	
Adds		FlexRay CC	Description of the bit 29 to 24 (PSL5 to PSL0 bit) in the FlexRay CC Status Vector Register (FRCCSV) corrected Error: Set to B'000100 when leaving HALT state.					
by		Status Vector						
REV.A	Register	······································						
	Register							
				riving Ability Set to "Increased"	: Incorre	ct descriptio	n	
			corrected.					
			Error:		T	T		
			Item		Symbol	Min.	Uni	
			Output	PAO to PA13, PB0,PB1,PB3,	V _{OH}	<u>Vcc –1.1</u>	V	
			high-level	PC0 to PC3,PC5,PC6,PC14,				
			voltage	PD0 to PD10,PE15,PF0,PF1,				
			(normal	PF4,PF5,PG0 to PG4,PH0 to PH15, PJ0 to PJ7,PJ10 to PJ15,				
			output and driving	PH15, PJ0 to PJ7,PJ10 to PJ15, PK0,PK5,PK6,PK8 to PK14,				
			ability)*1	PL2 to PL6,PL8,PL9				
		Table 38.6 DC	dointy) i					
			Correct:					
			Item		Symbol	Min.	Uni	
			Output	PAO to PA13, PB0,PB1,PB3,	V _{OH}	<u>Vcc –0.5</u>	V	
			high-level	PC0 to PC3,PC5,PC6,PC14,	V OH	<u>vcc –0.5</u>	v	
			voltage	PD0 to PD10,PE15,PF0,PF1,				
		Characteristics	(normal	PF4,PF5,PG0 to PG4,PH0 to				
		- Output Level	output and	PH15, PJ0 to PJ7,PJ10 to PJ15,				
Adds		Voltage: When 3.3 V is	driving	PK0,PK5,PK6,PK8 to PK14,				
by	38-6		ability)*	PL2 to PL6,PL8,PL9				
REV.A		Used with						
		Driving Ability	Error: Item		Symbol	Max.	Uni	
		Set to	Output	PAO to PA13, PB0,PB1,PB3,	V _{OL}	<u>0.9</u>	V	
		"Increased"	low-level	PC0 to PC3,PC5,PC6,PC14,	VOL	0.9	v	
			voltage	PD0 to PD10,PE15,PF0,PF1,				
			(normal	PF4,PF5,PG0 to PG4,PH0 to				
			output and	PH15, PJ0 to PJ7,PJ10 to PJ15,				
			driving	PK0,PK5,PK6,PK8 to PK14,				
			ability)*1	PL2 to PL6,PL8,PL9				
			Correct: Item		Symbol	Max.	Uni	
			Output	PAO to PA13, PB0,PB1,PB3,			V	
			low-level	PC0 to PC3,PC5,PC6,PC14,	V _{OL}	<u>0.4</u>	v	
			voltage	PD0 to PD10,PE15,PF0,PF1,				
			(normal	PF4,PF5,PG0 to PG4,PH0 to				
			output and	PH15, PJ0 to PJ7, PJ10 to PJ15,				
			driving	PK0,PK5,PK6,PK8 to PK14,				
		1	ability)*1	PL2 to PL6, PL8, PL9	1		1	



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			Table 38.25 RSPI Timing :	Incorrect d	lescript	ion corr	ected.	
			Error:	•				1
		Table 38.25 RSPI Timing			Min.	Max	k. Ur	
			Data input Slave t	_{SU} 25 +	2 x t _{cyc}		n	
Adds	00.00		setup time					38.23
by	38-22							
REV.A	Korrining	Correct:						
					Min.	Max		
			Data input Slave t	_{SU} 25 -	2 x t _{cyc}	-	n	
			setup time					38.23
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Adds	38-27	Table 38.28	Table 38.28 DRI Timing (W	vnen Specia	ai wode	is On)	: Inco	rrect
by		DRI Timing	description corrected.					
REV.A		(When Special	Error:	C) mails - I	N #1	N / ~··	11.	i+ []:
	Mode is On)	Item	Symbol	Min.	Max.			
			DIN3, DIN4 sampling edge undefined time before	tar	8	-	ns	38.25 to 38.28
			DIN1 initialization level					30.20
			release (when direct reset					
			is selected)					
		DIN3, DIN4 sampling edge	tbr	12	-	ns	5	
		undefined time before						
		DIN1 initialization level						
		release		l				
		Correct:			1	.		
		Item	Symbol	Min.	Max.	Uni		
		DIN3, DIN4 sampling edge	tar	8	-	ns		
		undefined time before					38.28	
			DIN1 initialization level release					
		DIN3, DIN4 sampling edge	tbr	12	-	ns	2	
			Ding, Ding sampling cuge				115	
			undefined time after DIN1		•-			,
			undefined time after DIN1 initialization level release					,
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