Date: 12/27/2011

RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-SH7-A827A/E	Rev.	1.00
Title	SH7455 Group, SH7456 Group User's Manual Hardware Errata Rev.A		Information Category	Technical Notification		
Applicable Product	SH7455 Group, SH7456 Group	Lot No.	Reference Document	SH7455 Group, SH7456 Group User's Manual: Hardware Rev.1.10 (R01UH0030EJ0110)		

Since we changed the following contents of "SH7455 Group, SH7456 Group User's Manual: Hardware Rev.1.10(Published on September 22, 2011)", we announce you.

Please use attached errata in the case of use of SH7455 Group, SH7456 Group User's Manual: Hardware Rev.1.10.

Appending Document:" SH7455 Group, SH7456 Group User's Manual: Hardware Rev.1.10" errata REV.A – 2 sheets

* In the following, the portion of net credit ( ) or an underline is a portion with an addition/change.

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<tr><td>Adds by REV.A</td><td>25-23</td><td>25.4.6 (3) Receive Operation</td><td>Incorrect description corrected (the 12th line)
Error: 4. To stop receiving when MST bit = "1xx", set RCVD bit in the ICCR1 register to "1", then read the ICDRR register.
Correct: 4. To stop receiving when MST bit = "1", set RCVD bit in the ICCR1 register to "1", then read the ICDRR register.</td></tr>
<tr><td>Adds by REV.A</td><td>32-76</td><td>32.7.1 FlexRay CC Status Vector Register</td><td>Description of the bit 29 to 24 (PSL5 to PSL0 bit) in the FlexRay CC Status Vector Register (FRCCSV) corrected
Error: Set to B'000100 when leaving HALT state.
Correct: Set to B'000000 when leaving HALT state.</td></tr>
<tr><td>Adds by REV.A</td><td>38-6</td><td>Table 38.6 DC Characteristics - Output Level Voltage: When 3.3 V is Used with Driving Ability Set to "Increased"</td><td>Table 38.6 DC Characteristics - Output Level Voltage: When 3.3 V is Used with Driving Ability Set to "Increased" : Incorrect description corrected.
Error:
<table>
<tr><th>Item</th><th></th><th>Symbol</th><th>Min.</th><th>Unit</th></tr>
<tr><td>Output high-level voltage (normal output and driving ability)*1</td><td>PA0 to PA13, PB0,PB1,PB3, PC0 to PC3,PC5,PC6,PC14, PD0 to PD10,PE15,PF0,PF1, PF4,PF5,PG0 to PG4,PH0 to PH15, PJ0 to PJ7,PJ10 to PJ15, PK0,PK5,PK6,PK8 to PK14, PL2 to PL6,PL8,PL9</td><td>V_{OH}</td><td>Vcc –1.1</td><td>V</td></tr>
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<tr><td>DIN3, DIN4 sampling edge undefined time before DIN1 initialization level release</td><td>tbr</td><td>12</td><td>-</td><td>ns</td><td></td></tr>
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Error: DINn (n=2,3,4)
Correct: DINn (n=3,4)</td></tr>
<tr><td>Adds by REV.A</td><td>38-34</td><td>Table 38.34 AUDR Module Timing (Vcc=5.0V)</td><td>Table 38.34 AUDR Module Timing (Vcc=5.0V) : Incorrect description corrected.
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