# AD500 User's Manual

Real Time Devices

ISO9001 and AS9100 Certified

# AD500 User's Manual

A User's Guide to the AD500
12 Bit Data Acquisition System

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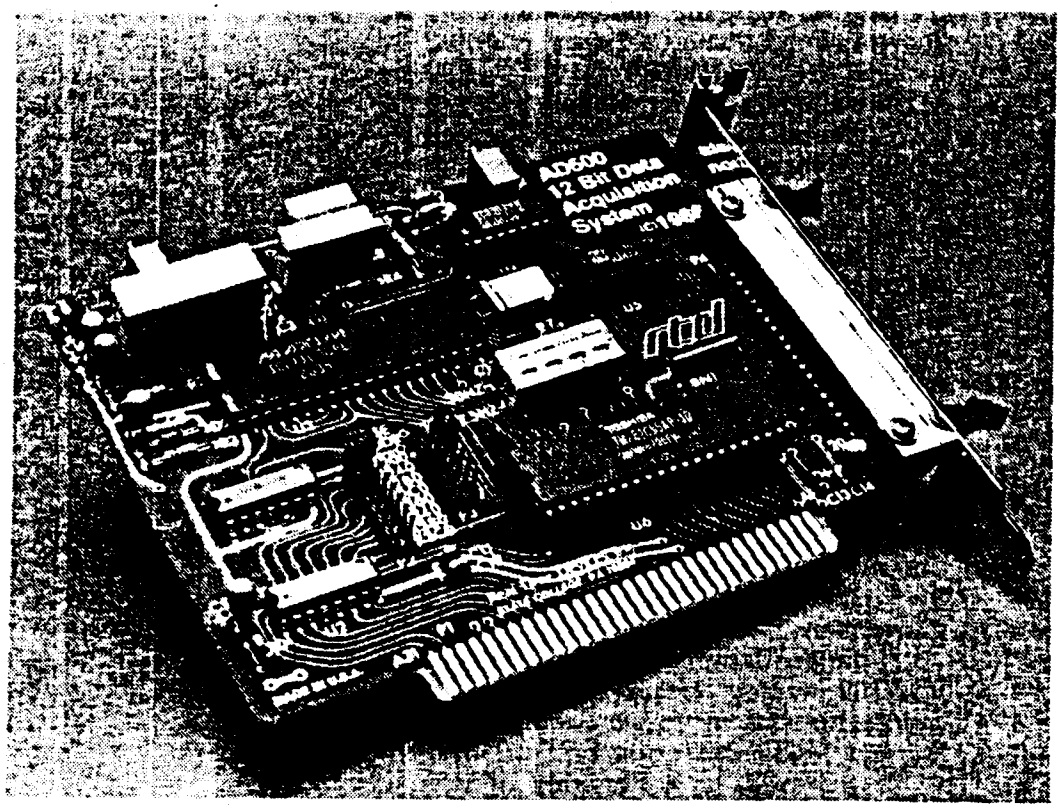

AD600
12 Bit Data
Acquisition
System

# Chapter 1

## Introduction

Many computer applications today require real-time input of real world signals. To connect a computer to the real physical world, specialized analog interfaces are used to digitize voltages. These voltages often represent the outputs of transducers or analytical instruments. Transducers are devices that convert a real world physical quantity into an electrical signal that accurately reflects the value of a particular real world phenomena such as temperature, humidity, or sunlight. An analog-to-digital converter interface (abbreviated A/D or ADC) is simply a piece of electrical hardware that permits a computer to read, or digitize, the value of a voltage.

Real Time Devices' AD500 is an 8-channel, 12-bit analog interface board based on the ICL7109 CMOS A/D converter and designed for use in an IBM PC/XT/AT, or compatible, computer. The AD500 is highly accurate, stable, and resistant to interference from common noise sources. A 7.5 Hz conversion rate provides 60 dB rejection of 60 Hz line noise. Its high immunity to interference also makes the AD500 ideal for industrial, environmental, or laboratory data acquisition.

The AD500 is switch selectable for either a 7.5 Hz or 30 Hz conversion rate. A 7.5 Hz conversion rate will provide significant rejection of 60 Hz line noise. If line noise is not a consideration in your application, a 30 Hz rate will allow maximum conversion speed. Chapter 2 describes how to select either the 7.5 Hz or 30 Hz rate.

Eight analog inputs are software selectable and overvoltage protection circuitry prevents transients from damaging the inputs. A programmable gain amplifier (PGA) eliminates the need to preamplify the input signals and permits measurement of a wide range of voltages. The input ranges selectable by the PGA are +/-5 volts, +/-500 millivolts, and +/-50 millivolts.

The seven digital I/O lines are TTL compatible and are configured as two groups consisting of 5 lines and 2 lines. The group of 2 lines may be assigned as input or output, while the remaining 5 lines are configured as output only.

The analog and digital lines, as well as +/-12 volts, the PC's reset signal, and digital and analog grounds, are accessible through a 40-pin header connector at the end of the board. This connector is compatible with Real Time Devices' XB40 I/O extender board and XC40 expansion cable. The XB40 consists of two 20-pin screw terminals and a prototype area. The screw terminals allow easy connection of signals to the AD500 and the prototype area allows development of unique analog front end circuitry. The XC40 is a cable assembly which terminates in a 40-pin wire wrap header connector. This connector is suitable for installation in standard perf-board material.

The Program Disk included with your AD500 contains software routines to control the A/D converter, input multiplexer, PGA, and digital I/O lines. Detailed information is also provided to permit you to write your own routines for controlling the AD500.

This manual has been organized into five main chapters, with a group of Appendices that contain information that you may need to refer to from time to time.

CHAPTER 1 briefly describes the AD500 operating features, I/O capability, and software.

CHAPTER 2 explains how to install the AD500 in your computer. This includes selecting the base address, interrupt capability and conversion speed, and connecting signals to the I/O connector.

CHAPTER 3 describes, in detail, the procedure for programming the AD500, which includes controlling the multiplexer, PGA, A/D converter, and digital I/O lines. Some considerations are also given if you require the use of interrupts.

CHAPTER 4 explains the theory of operation of the various components which comprise the AD500. A discussion of the characteristics of the integrating A/D converter technique as well as the performance of the multiplexer and PGA are included.

CHAPTER 5 provides the procedure for calibrating the AD500. This may be used for checking the operation of your AD500 or for fine tuning its performance for your particular application.

APPENDICES contain technical information related to your AD500. This includes the AD500 and component specifications, the P4 I/O connector pin assignment, and connector types. References and warranty information are also provided.

Every effort has been made to design a quality, easy to use, yet low cost A/D converter interface board. We are certain that you will find the AD500 to be a valuable interfacing tool for your PC.

# Chapter 2

## Installation

The AD500 plugs into any expansion slot, including a short slot, of an IBM PC/XT/AT or compatible computer. It may be advantageous, therefore, to choose an available short slot inside your computer.

The board's I/O address and interrupt channel are jumper selectable. Preventing possible contention with other devices simply involves changing two jumpers. If the board address is unjumpered or incorrect, the AD500 will not operate. The conversion speed of the A/D converter must also be selected with the switch. Before installing the board into your computer the jumper selections and switch settings must be made.

All connections to external signals are made through one 40-pin I/O connector, which can be accessed through the rear of the computer after the board is installed.

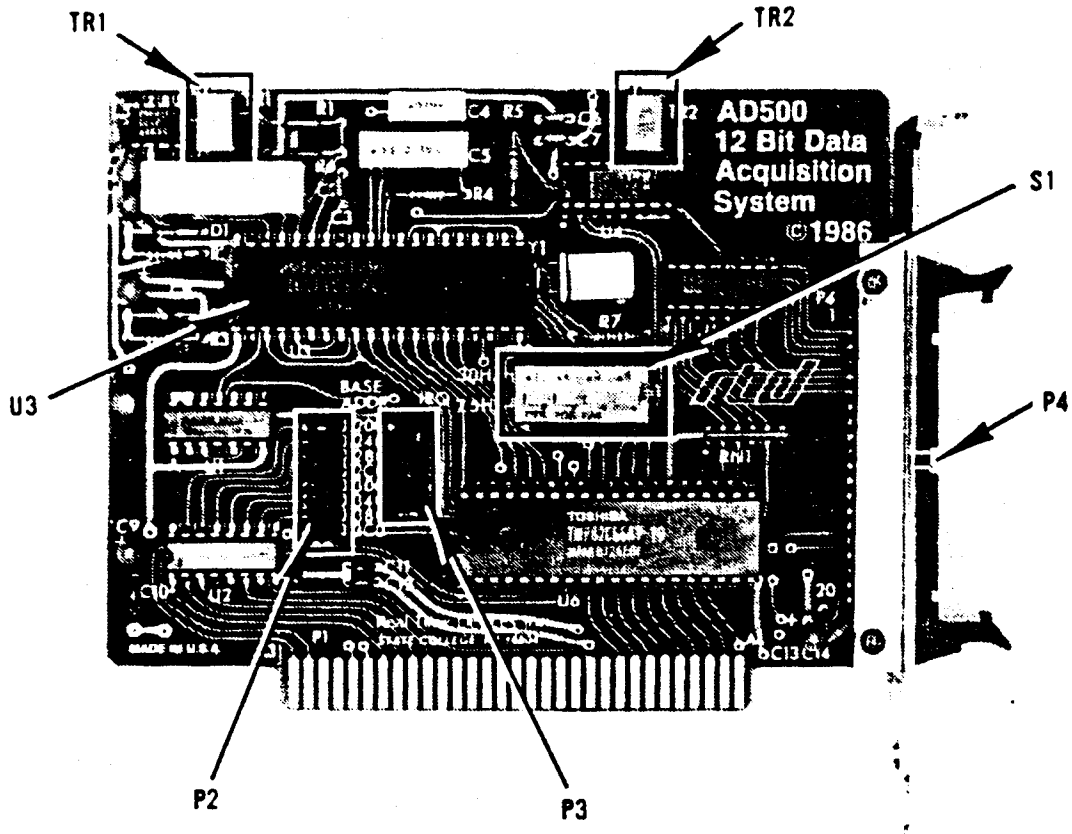



Fig. 2-1 AD500 Component Locations

**Base Address Selection - Connector P2**

To select the board's base I/O address, the jumper on the connector labeled P2 must be positioned to correspond to the address desired. The jumper should be placed horizontally across the pair of header pins beside the base address you select (see Figure 2-1). The base addresses labeled beside connector P2 are hexadecimal values.

When choosing a base address, be careful not to use one that will cause contention with another peripheral. The AD500 occupies 16 addresses beginning with the base address selected, however only four addresses are actually used. Chapter 3 "Programming the AD500" explains the function of these four addresses. Figure 2-2 shows how the PC's I/O port address bits are decoded by the AD500.

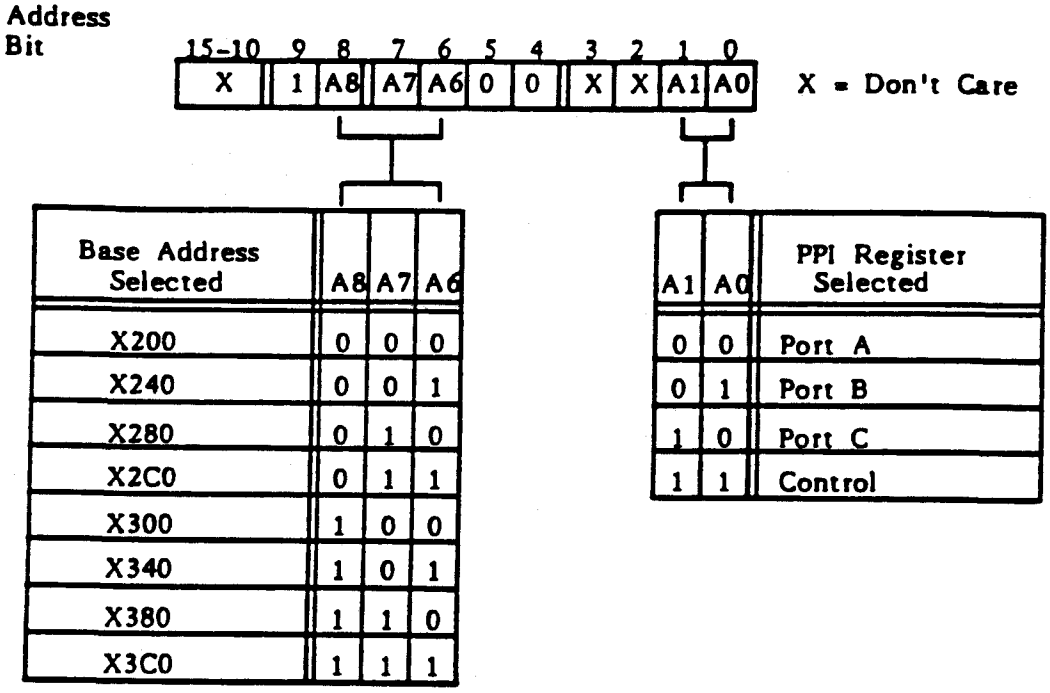



**Fig. 2-2 AD500 I/O Port Address Decode**

The AD500 base address has been preset to X'200'. For future reference, you may wish to record the base address you selected in Table 2-1. If the base address is changed from the preset value of X'200', the example software provided with the AD500 will need to be modified to reflect the new value. The procedure to do this is explained in the comments which accompany each of the sample programs.

### Interrupt Channel Selection - Connector P3

The AD500 may be configured to generate an interrupt upon completion of an A/D conversion. To select which PC interrupt channel is used to service the interrupt, position the jumper on the connecter labeled P3 to correspond to the desired interrupt channel number. The jumper should be placed horizontally across the pair of header pins beside the interrupt channel number. If interrupts are not used, this jumper must be set as shown in Figure 2-3.

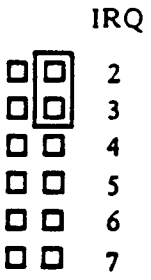



**Fig. 2-3 Interrupt Disable Jumper Position**

The AD500 interrupt is preset to the disabled position. For future reference you may wish to record the interrupt channel used in Table 2-1.

| Table 2-1 AD500 User-Selected Options |
|---|
| I/O Base Address<br>_____ (hex) _____ (decimal) |
| INTR/IRQ Channel Selection<br>INTR IRQ _____ |

Chapter 3 describes considerations for using the AD500 interrupts.

## SELECTING CONVERSION SPEED - SWITCH S1

Your AD500 will perform A/D conversions at either a 7.5 Hz or 30 Hz rate. A 7.5 Hz rate provides maximum rejection of 60 Hz line noise, while a 30 Hz rate will allow maximum speed of conversions.

To select a 7.5 Hz rate, all four positions of switch S1 must be towards the bottom of the switch, labeled "7.5" (see Figure 2-1). A 30 Hz rate is selected by sliding all four switch positions towards the top of the switch, labeled "30". The conversion speed must be selected before the board is installed in the computer; the switch setting should not be changed while the AD500 is operating.

Your board is factory calibrated and configured for the 7.5 Hz rate. If you will be using a 30 Hz rate, you may need to recalibrate the AD500. Refer to Chapter 5, "Calibration", for details on calibrating the A/D converter.

## BOARD INSTALLATION

After selecting the base address and interrupt capability, the AD500 may be installed inside the computer.

1. TURN OFF THE POWER TO YOUR COMPUTER FIRST. Refer to the owner's manual for your computer, and remove the top cover.
2. Select the expansion slot you wish to use and remove the corresponding blank bracket from the rear panel of the computer.

3. Close both ejector latches on the AD500 P4 I/O connecter, and orient the board inside the computer so that the connector protrudes through the rear of the computer, and the card edge connector lines up with the selected expansion slot connector.

4. After you are certain the board lines up correctly, push down on the metal bracket tab and the top of the board until the board is seated firmly in the expansion slot connector.

5. Reinstall the screw that was removed with the blank bracket and replace the cover to your computer.

## EXTERNAL CONNECTIONS - Connector P4

All external connections to the AD500 are made to the I/O connector, labeled P4 (see Figure 2-1), which is accessible through the rear panel of the computer. The P4 mating connector type is listed in Appendix B as well as the pin assignment of all signals associated with the AD500.

To attach the mating connector, first open the ejector tabs on the AD500 I/O connector. Then, observing the keying of both connectors, install the mating connector and push firmly until the ejector tabs snap closed, securing the connector in place.

The AD500uses a CMOS programmable peripheral interface chip. The digital I/O lines of this device may be permanently damaged if they are subjected to high energy electrostatic fields. When making connections to the associated P4 pins, be careful that they are not exposed to electro-static discharge (ESD).

## CALIBRATION

Two trimpots are located near the top of the AD500 (see Figure 2-1). These trimpots are used for calibrating the A/D converter. The AD500 is factory calibrated to maximize the performance of the A/D converter over all three gain ranges: 1, 10 and 100. However, if your application will require only one or two gain settings, you may wish to recalibrate your board for a particular gain. You may also need to recalibrate the A/D converter if you will be using the 30 Hz conversion rate. The procedure is straightforward and is described in Chapter 5, "Calibration".

# Chapter 3

## Programming the AD500

The AD500 uses an 8255 Programmable Peripheral Interface (PPI) chip to control the on-board A/D converter, input multiplexer, programmable gain amplifier, and 7 TTL compatible digital I/O lines. By utilizing a PPI, the chip count of the design is minimized without sacrificing any loss of performance.

The software included with your AD500 performs all the necessary interfacing functions with the PPI. These routines allow you to initialize the AD500, take readings, select the input channel, change gain, and control the digital I/O lines.

### USING THE AD500 APPLICATION SOFTWARE

Before you begin to use the software, be sure to make a backup copy of the Program Disk included with your AD500, and store your original disk in a safe place. You may make as many copies of the Program Disk as you need.

A description of the software included with your AD500 is given in the file README.DOC on the Program Disk. Considerations for programming the AD500 are also included.

Specific documentation for the language interfaces is contained in all files having the extension ".DOC". This documentation may be printed using the DOS "TYPE" command or any word processor which utilizes standard text document files.

## PROGRAMMING THE 8255 PPI

Although the software included with your AD500 will satisfy many of your application requirements, it may be necessary for you to become more familiar with the details of controlling the PPI. Figure 3-1 illustrates how the PPI I/O ports are interfaced with the other components of the AD500.

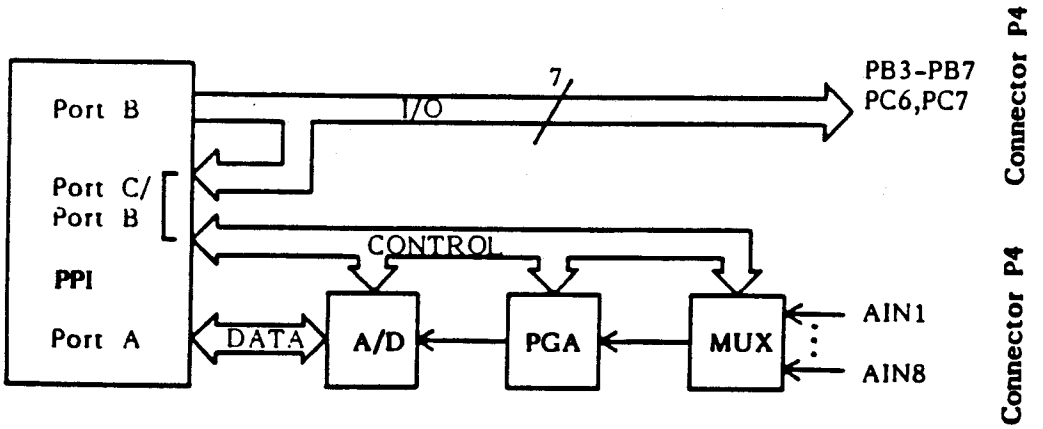



**Fig. 3-1 AD500 PPI Interface Configuration**

The PPI contains four registers which are used to communicate with its three 8-bit I/O ports (see Table 3-1). These registers are located at the I/O addresses determined by the base address you selected in Chapter 2, however, all the BASICA examples presented use a base address of X'200'.

**Table 3-1 AD500 PPI Internal Register Definition**

| 8255 PPI Function | AD500 Function | Base Address + |
|---|---|---|
| Port A Read | Read Data From A/D | 0 |
| Port B Write | Select Analog Input<br>Write Digital I/O | 1 |
| Status Word Read/<br>Port C Read | Read A/D Status/<br>Port C Digital Input | 2 |
| Write Mode to Control Word/<br>Port C Bit Set/Reset | Configure AD500<br>Write A/D, Gain Control<br>Port C Digital Output | 3 |

## INITIALIZING THE PPI

Before the PPI can be used to control the components it interfaces with, its operating modes must first be initialized. This is required only once by the software after power-up and each time the digital I/O ports are to be reconfigured, and is done by writing data to the Control Word, as shown in Figure 3-2.

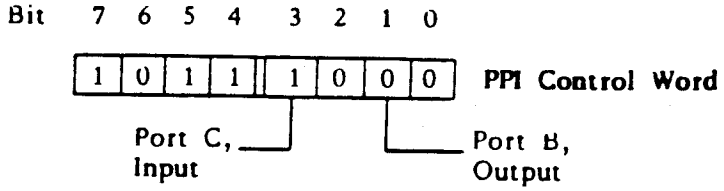



**Figure 3-2 AD500 PPI Control Word Initialization Data**

Whenever data is written to the Control Word with bit 7 set, the PGA will be set to a gain of 1, and the multiplexer will select analog input AIN1.

Using BASICA, executing the OUT statement

**OUT &H203,&HB8**

will correctly initialize the PPI.

In this example, the AD500 digital I/O lines were configured as Port B, output, and Port C, input. Refer to the section in this chapter entitled "Programming the Digital I/O Ports" Selecting the Direction of Port C to determine the data that is written to configure Port C as output.

## INTERFACING WITH THE A/D CONVERTER

The AD500 may perform A/D conversions in any of three modes: single, continuous, or strobed. Each mode offers its own unique advantages, but all three modes offer high rejection of 60 Hz line noise when converting at a rate of 7.5 Hz. The modes differ in the way the START CONVERT signal is used to initiate an A/D conversion. The mode selected also determines the speed conversions are performed. The following paragraphs explain the characteristics of each mode and will help you decide how to best utilize the AD500 for your application.

Single Convert Mode -- In this mode of operation, a single A/D conversion is performed each time the START CONVERT signal is pulsed high and low. The length of each conversion cycle is proportional to the amplitude of the analog input signal.

Continuous Convert Mode -- Conversions are initiated automatically in this mode. The START CONVERT signal is pulsed high and remains high for as long as conversions are desired. Conversion cycles are the same in length and are performed at a consistent rate.

Strobed Convert Mode -- This mode of operation allows conversions to be performed continuously at a rate proportional to the analog input signal amplitude. The START CONVERT signal is repeatedly pulsed high and low to initiate each conversion.

Your AD500 is switch-selectable to convert at a minimum rate of either 7.5 Hz or 30 Hz. Refer to Chapter 2 for details on selecting the conversion speed.

Regardless of the configuration of your AD500 or the mode used to perform A/D conversions, the data for each conversion is read back through the PPI in two 8-bit transfers consisting first of a most significant byte (MSB), then a least significant byte (LSB). These transfers are initiated automatically by the A/D converter after each conversion is finished and depend upon a sequence of handshaking signals between the PPI and A/D converter. For this reason, you should structure your application software so that two bytes of data are always read from the PPI after each conversion is completed.

Whenever you are uncertain of the state of the A/D converter data transfer, such as after breaking from a BASIC program, you should execute the sequence described in the following section before initiating more conversions.

**Initializing the A/D Converter**

Before the A/D converter can be used in any conversion mode, it must first be initialized so that the data transfers will be properly sequenced. This is required only once after power-up or whenever you need to resynchronize the A/D data transfers.

After initializing the PPI as described above, the following sequence must be performed to initialize the A/D converter:

Set START CONVERT (See Figure 3-3)
Read PPI Port A
Delay 20 microseconds
Read Status Word
Check Status Word IBF indication (See Figure 3-4)

| If IBF is reset: | If IBF is set: |
|---|---|
| Check IBF until set | Reset START CONVERT (See Figure 3-5) |
| Read PPI Port A | Delay 90 milliseconds |
| Check IBF until set | Read PPI Port A |
| Reset START CONVERT (See Figure 3-5) | |
| Delay 90 milliseconds | |
| Read PPI Port A | |

A BASICA routine for the A/D initialization is contained in the DEMO programs on the Program Disk.

**Single Convert Mode**

An A/D conversion of the input voltage is performed each time the START CONVERT signal is pulsed high. This is done by setting and resetting bit PC2 of the PPI. Using the Port C Bit Set/Reset feature of the PPI, the START CONVERT signal is set by writing the data shown in Figure 3-3 to the Control Word.

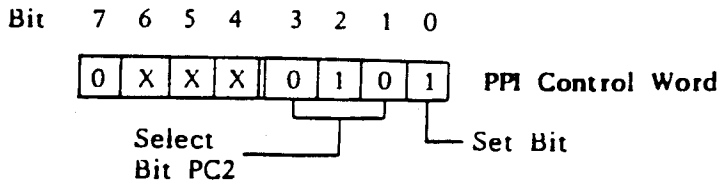



**Fig. 3-3 Control Word Data to Set START CONVERT**

Once the START CONVERT signal is set, conversion of the analog input begins. When the conversion is completed, the A/D converter will strobe the most significant byte (MSB) of data into Port A of the PPI. When this occurs, the PPI Input Buffer Full (IBF) signal, PC5, will be set. The status of the IBF signal is checked by reading the PPI Status Word, as shown in Figure 3-4.

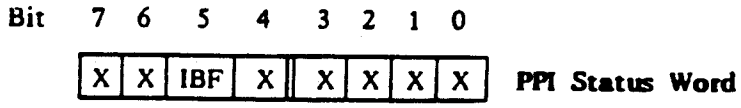



**Fig. 3-4 PPI Status Word IBF Indication**

Remember to mask off all but bit 5 of the status word, if necessary, when checking the IBF signal. Once the IBF signal is set, reset the START CONVERT signal as shown in Figure 3-5.

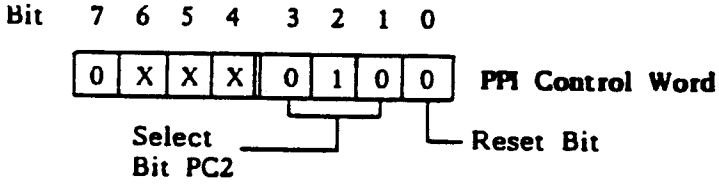



**Figure 3-5 Control Word Data to Reset START CONVERT**

The MSB of data is now read from the AD500 by inputting the contents of the PPI Port A using the I/O address defined in Table 3-1.

After the MSB of data is read, the IBF signal will go low until the A/D converter automatically transfers the least significant byte (LSB) of data to the PPI Port A. When the IBF signal is again set, the LSB of data can now be input by reading the contents of the PPI Port A a second time.

The timing diagram in Figure 3-6 illustrates the handshaking signals required to perform a single A/D conversion and to read the results.

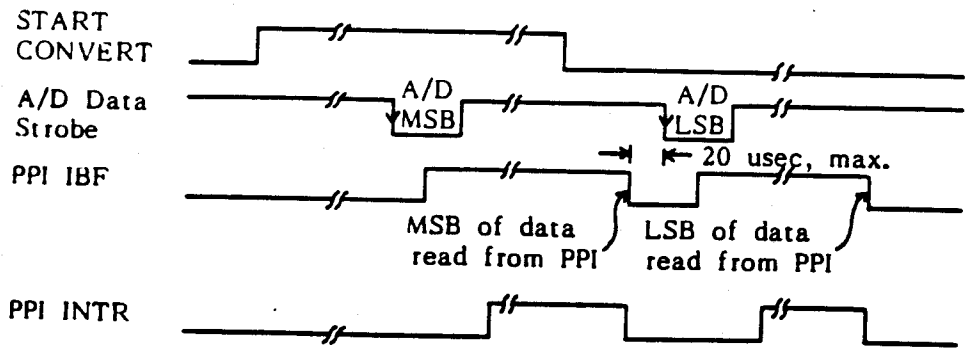



**Fig. 3-6 AD500 Single Convert Mode Timing Diagram**

The following programming model summarizes the sequence of events required to perform a conversion in the Single Convert Mode.

Set START CONVERT
Check IBF until set
Reset START CONVERT
Read A/D MSB data
Check IBF until set
Read A/D LSB data

A sample BASICA program for using the AD500 in the Single Convert Mode is contained on the Program Disk.

### Continuous Convert Mode

This mode of operation automatically allows for an A/D conversion to be performed after each conversion result is read. The conversion cycles will be a fixed length of time and, provided the data is read promptly after each conversion is completed, conversions will be performed at a constant rate of 7.5 or 30 Hz, depending on the hardware configuration of your AD500. Refer to Chapter 2 for details on selecting the conversion speed. New data will not be strobed into the PPI by the A/D converter until both bytes of the previous conversion are read. This ensures that the A/D data will not be corrupted.

### Starting Conversions

To utilize the Continuous Convert Mode, the START CONVERT signal is set high and should remain high as long as conversions are desired. The START CONVERT signal is set by writing the data shown in Figure 3-3 to the PPI Control Word. Each time a conversion is completed, the A/D converter strobes the MSB of data into Port A of the PPI. The PPI Input Buffer Full (IBF) signal will indicate when this data is available to be read from Port A. The status of the IBF signal is checked by reading the PPI Status Word, as shown in Figure 3-4.

## Reading the A/D Data

After the MSB of data is read from the PPI Port A (see Table 3-1), the IBF signal will then indicate when the LSB of A/D data is available. Once the LSB of data is read, the A/D converter will automatically strobe the MSB of the next conversion result into the PPI. New data will not be strobed into the PPI until both an MSB and LSB are read, therefore, the PPI data that is read will always be of the first conversion performed after the last PPI read operation.

## Terminating Conversions

When the Continuous Convert Mode is to be terminated, the START CONVERT signal should be reset after detecting the IBF signal for the MSB of the last A/D conversion desired. The START CONVERT signal is reset by writing the data shown in Figure 3-5 to the PPI Control Word.

The timing diagram in Figure 3-7 illustrates the handshaking signals required to perform A/D conversions and read the results in the Continuous Convert Mode.

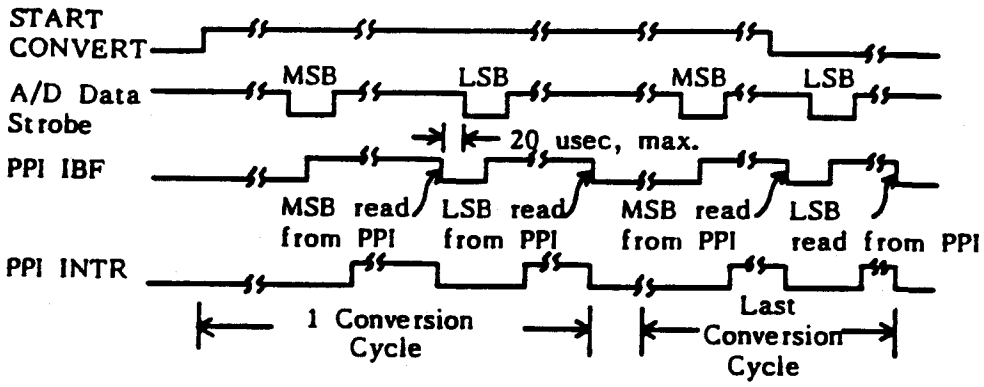



**Fig. 3-7 AD500 Continuous Convert Mode Timing Diagram**

The following programming model summarizes the sequence of events required to perform conversions in the Continuous Convert Mode.

```
Set START CONVERT

Check IBF until set
Read A/D MSB data          Repeat to read
Check IBF until set        each conversion
Read A/D LSB data
        .
        .
        .
Check IBF until set
Reset START CONVERT
Read A/D MSB data          Used to read
Check IBF until set        last conversion
Read A/D LSB data
```

A sample BASICA program for using the AD500 in the Continuous Convert Mode is contained on the Program Disk.

### Strobed Convert Mode

The Strobed Convert Mode will perform conversions continuously at a rate proportional to the analog input voltage. This is done by taking advantage of a unique feature of the ICL7109 A/D converter. By pulsing the START CONVERT signal low, then high after a conversion is completed, the speed of the conversion cycle will be optimized. This allows another conversion to start sooner. Details on the operation of the ICL7109 A/D converter are given in Chapter 4 "Theory of Operation".

This mode is actually a series of single conversions similar to the those performed in the Single Convert Mode. First, the START CONVERT signal must be set to initiate a conversion. This is done by writing the data shown in Figure 3-3 to the PPI Control Word. When the conversion is completed, the PPI's Input Buffer Full (IBF) signal will be set. The status of the IBF signal is checked by reading the PPI Status Word as shown in Figure 3-4.

Once the IBF is set, reset, then set the START CONVERT signal by writing the data shown in Figures 3-5 and 3-3, respectively, to the PPI Control Word. This must be done after detecting the completion of each conversion. Now the MSB and LSB of A/D data can be read from Port A. Refer to the Continuous Convert Mode description for details on the procedures for reading the A/D data and terminating conversions.

The timing diagram in Figure 3-8 illustrates the handshaking signals required to perform A/D conversions and read the results in the Strobed Convert Mode.

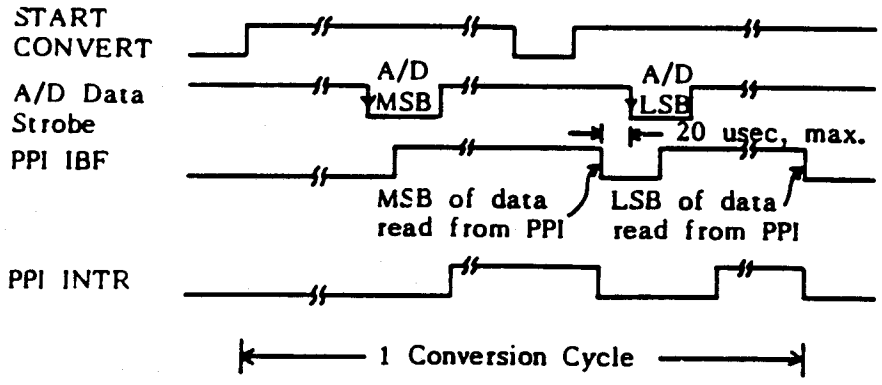



**Fig. 3-8 AD500 Strobed Convert Mode Timing Diagram**

The following programming model summarizes the sequence of events required to perform conversions in the Strobed Convert Mode.

```
Set START CONVERT

Check IBF until set
Reset START CONVERT
Set START CONVERT                    Repeat to read
Read A/D MSB data                    each conversion
Check IBF until set
Read A/D LSB data
                .
                .
                .
Check IBF until set
Reset START CONVERT
Read A/D MSB data                    Used to read
Check IBF until set                  last conversion
Read A/D LSB data
```

A sample BASICA program for using the AD500 in the Strobed Convert Mode is contained on the Program Disk.

### A/D Converter Data Format

Figure 3-8 shows the format of the MSB and LSB A/D converter data.

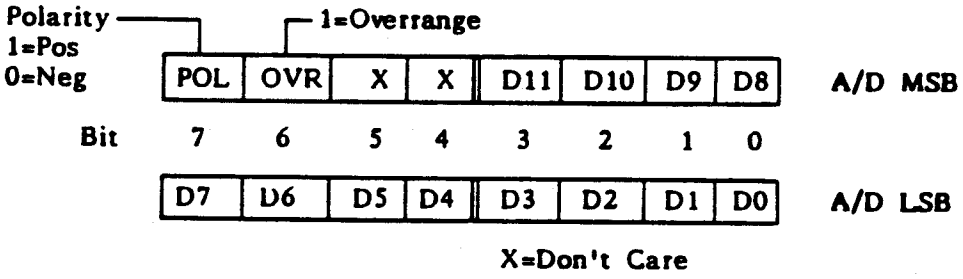



**Fig. 3-9 AD500 A/D Converter Data Byte Format**

The MSB of the A/D converter data contains polarity and overrange status indications, along with the four most significant bits of the A/D converter data. The LSB contains the eight least significant bits of the A/D converter data.

## ANALOG INPUT CHANNEL SELECTION

The analog input multiplexer channel is selected using the three least significant bits of the PPI Port B, bits PB0-PB2, as shown in Figure 3-10.

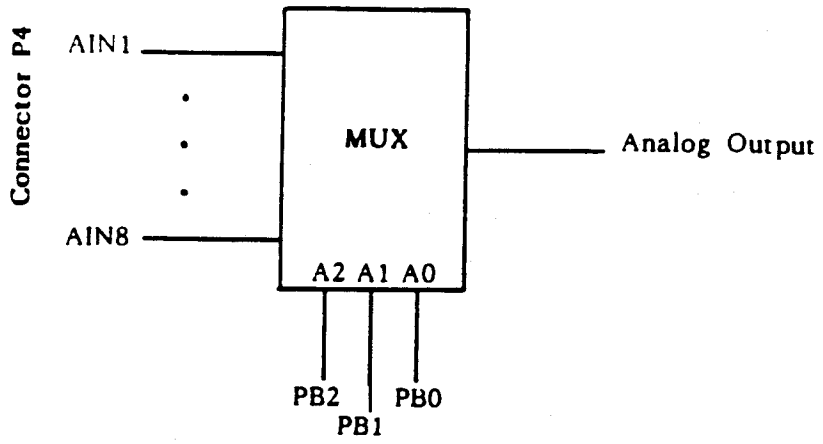



**Fig. 3-10 MUX Channel Selection Bit Assignment**

The data written to Port B for each channel selection is shown in Table 3-2.

**Table 3-2 Input Channel Selection Bit Settings**

| Analog Input | PB2 | PB1 | PB0 |
|---|---|---|---|
| AIN1 | 0 | 0 | 0 |
| AIN2 | 0 | 0 | 1 |
| AIN3 | 0 | 1 | 0 |
| AIN4 | 0 | 1 | 1 |
| AIN5 | 1 | 0 | 0 |
| AIN6 | 1 | 0 | 1 |
| AIN7 | 1 | 1 | 0 |
| AIN8 | 1 | 1 | 1 |

If your application requires changing the input channel when the AD500 is in the continuous or strobed convert modes, the new channel should be selected before reading the MSB of the most recent A/D converter value. The new channel will be in effect for all future A/D conversions until the channel is changed again. This will prevent the input channel from changing during the conversion process, which may result in an erroneous A/D reading. This procedure is illustrated in the DEMO software on the Program Disk.

After a different input channel is selected, a minimum of 5 microseconds of delay is required before initiating a conversion to allow the analog input to the A/D converter to stabilize. This is not a consideration when programming from high-level languages such as BASIC, FORTRAN, or Pascal. However, if your application program will be written in a very fast language such as assembler or FORTH, you will need to allow for a delay after changing channels.

When using any of the 5 available PPI Port B digital output bits, PB3 - PB7, you may want to preserve their logic states when changing the input channel. This can be done by first reading the Port B data, then 'AND'ing its contents with X'F8'. This will reset the 3 least significant bits. Next 'OR' this result with the data needed to select the analog channel desired (from Table 3-2) and write this value back to Port B. This ensures that the 5 most significant bits of Port B will remain stable when changing the input channel. This procedure is illustrated in the DEMO software.

## GAIN SELECTION

The programmable gain amplifier is controlled by bits PC0 and PC1 of the PPI as shown in Figure 3-11.

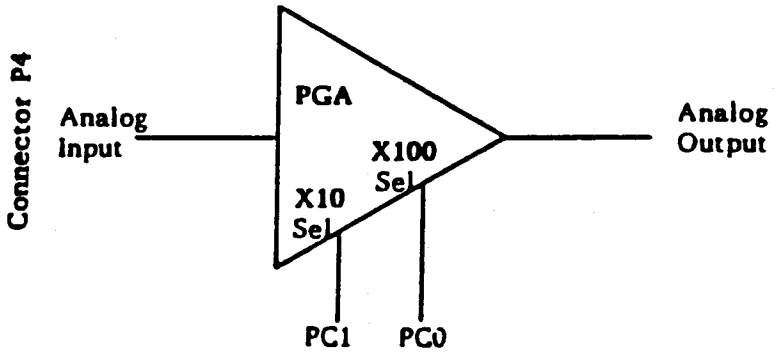



**Fig. 3-11 PGA Gain Control Bit Assignment**

These bits are controlled using the Bit Set/Reset feature of the PPI. To change PGA gain, first reset both PC0 and PC1, then set either PC0 or PC1, if necessary, by writing data to the Control Register as indicated in Tables 3-3 and 3-4.

**Table 3-3 Gain Control Bit Settings**

| Gain | PC1 | PC0 |
|---|---|---|
| x1 | 0 | 0 |
| x10 | 1 | 0 |
| x100 | 0 | 1 |

**Table 3-4 Set/Reset of PC0 and PC1**

| | PC1 | PC0 |
|---|---|---|
| SET | X'03' | X'01' |
| RESET | X'02' | X'00' |

**PPI Control Word Data**

If your application requires gain changes when the AD500 is in the continuous or strobed convert modes, the new gain should be selected before reading the MSB of the most recent A/D converter value. The new gain will be effective for all future A/D conversions. This will prevent

a gain change during the conversion process, which may result in an erroneous A/D reading. This procedure is illustrated in the DEMO software on the Program Disk.

## PROGRAMMING THE DIGITAL I/O PORTS

The seven bits of digital I/O available at the AD500 P4 connector are organized as shown in Figure 3-12.

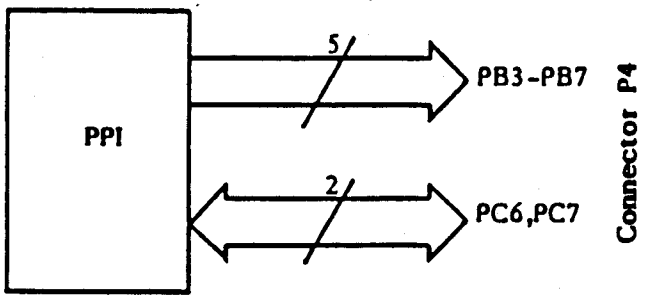
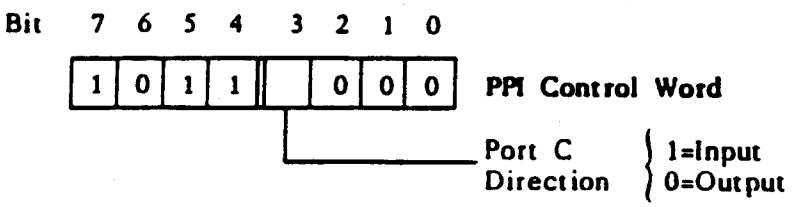



**Fig. 3-12 AD500 Digital I/O**

The group of five lines, PB3-PB7, are connected to Port B of the PPI and are programmed as all outputs on the AD500. The remaining two lines, PC6 and PC 7, are connected to Port C of the PPI and may be programmed as both inputs or both outputs. In addition, each of the Port C bits, when programmed as outputs, may be individually programmed to be set or reset, without effecting the state of the other bit.

### Selecting the Direction of Port C

Two different configurations may be used for transferring data using Ports B and C. To select the mode you wish to use, it may be necessary to write a different value to the PPI Control Word than was used in "Initializing the PPI". Figure 3-13 shows the Control Word data format for configuring Port C as input or output. This data must be written to the Control Word whenever Port C is to be reconfigured. Whenever one of these values is written to the PPI Control Word, the PGA will be set to a gain of 1 and the MUX will select analog input channel AIN1. In addition, whenever the PPI Control Word is written to with bit 7 set, all digital outputs and status flags will be reset.



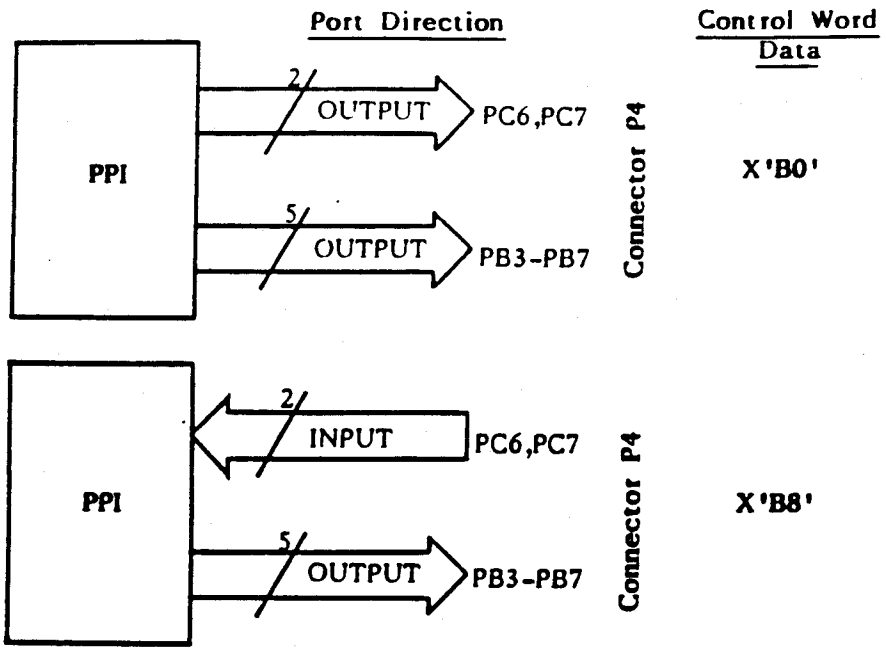



**Fig. 3-13 Selecting Port C Direction**

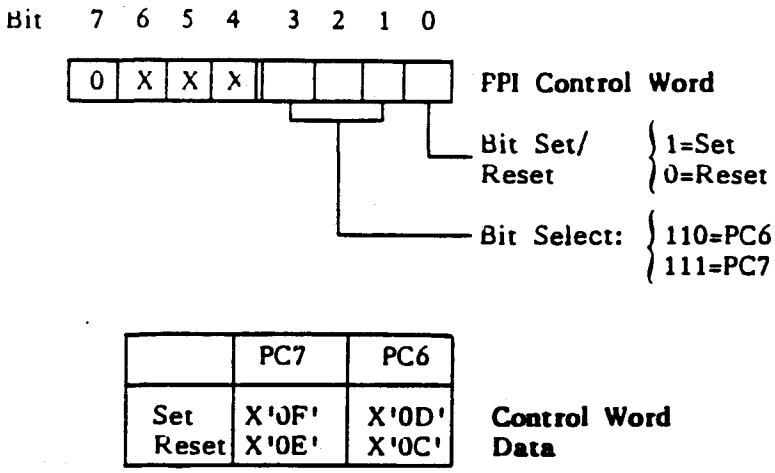
**Outputting Data on Port B and Port C**

Data is output by Port B by writing to the PPI Port B register address. This address was defined in Table 3-1. The following BASICA OUT statement will output the bit pattern "1010 1010" to Port B:

```
OUT &H201,&HAA          Output X'AA' to Port B
```

To ensure that the analog input channel to the A/D converter, which is selected with bits PB0-PB2, does not change when writing data to digital lines PB3-PB7, you will need to preserve the bit pattern on PB0-PB2 when writing to Port B. This can be done by first reading the Port B data, then 'AND'ing its contents with X'07'. This will reset the 5 most significant bits while maintaining the bit pattern on PB0-PB2. If you wish to preserve any of the other bits of Port B, add their bit weights to the value X'07' when "AND'ing the Port B data. Next 'OR' this result with the data you wish to output on PB3-PB7, after it has been properly justified to correspond to the correct Port B bit positions. Finally, this value should be written back to the Port B register. This procedure is illustrated in the DEMO software.

The two bits of Port C are programmed individually using the Bit Set/Reset function of the PPI. Figure 3-14 lists the data that must be written to the Control Word to set or reset PC6 and PC7.




| | PC7 | PC6 | |
|---|---|---|---|
| Set | X'0F' | X'0D' | Control Word |
| Reset | X'0E' | X'0C' | Data |

**Fig. 3-14 Set/Reset of PC6 and PC7**

**Inputting Data from Port C**

Data is read from Port C by reading the PPI Port C register. Its address was defined in Table 3-1. The following BASICA INP statements illustrate how the Port C data is input:

```
C = INP(&H202)     C <— Port C data
C = C AND &HC0     Mask PC6 and PC7
```

Note that the data read from the Port C address was 'AND'ed with the bit pattern 1100 0000 to mask PC6 and PC7.

Additional examples of reading and writing data with the PPI digital I/O ports are given in the DEMO software on the Program Disk.

## INTERRUPT CONSIDERATIONS

The interrupt generated by the AD500 PPI may be jumpered to any of the PC interrupt channels 2-7. The channel selection is made by jumpering pins on the AD500 P3 connector as explained in the Interrupt Channel Selection description in Chapter 2.

An interrupt occurs each time the A/D converter writes a byte of data into the PPI Port A. Therefore, two interrupts are generated for each conversion, one for the MSB data and one for the LSB data. The timing of the interrupt signal generated by the PPI is shown in the Timing Diagrams in Figures 3-6, 3-7, and 3-8.

Before using the PPI interrupt, it must first be enabled by writing a "1" to the PPI Port A Interrupt Enable bit, INTE A. This is done by setting bit PC4 using the Port C Bit Set/Reset function of the PPI. Table 3-5 lists the data that must be written to the PPI Control Word to set or reset the INTE A mask bit.

**Table 3-5 Set/Reset of INTE A**

| INTE A | Control Word Data |
|---|---|
| Set | X'09' |
| Reset | X'08' |

The INTE A mask bit is disabled during power up reset and whenever the Control Word is written to when changing the PPI mode.

Before you attempt to use interrupts, be certain you are familiar with the procedure for initializing the interrupt vectors and the PC's interrupt controller, and setting up the interrupt handling routines. Reference 1 in Appendix C contains a very good description of the PC's system interrupts.

# Chapter 4

## Theory of Operation

A block diagram of the AD500 analog circuitry is shown is Figure 4-1. Functionally, there are four major analog components: the multiplexer (MUX), programmable gain amplifier (PGA), A/D converter, and voltage reference. The PPI digital I/O ports are used to control the analog components and read data from the A/D converter.

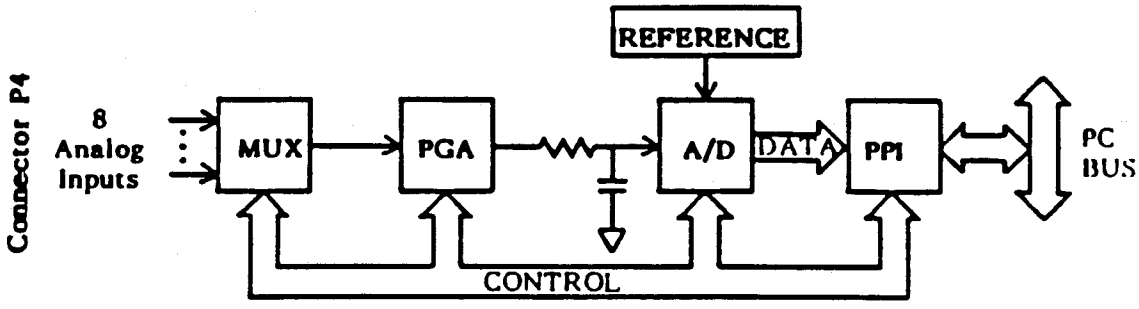



**Fig. 4-1 AD500 Analog Circuitry Block Diagram**

A brief description of each of the major components of the AD500 is outlined below.

HI-508A - An input protected single-ended analog MUX made by Harris Corporation that allows the AD500 to monitor several analog channels.

PGA102 - A very high quality PGA manufactured by Burr-Brown. Its gains are not controlled by the usual discrete feedback resistors, but by two digital lines that provide gains of 1, 10, and 100 by selecting internal precision resistors.

REF02 - A precision voltage reference manufactured by Precision Monolithics. It provides a relatively temperature independent voltage reference for the A/D converter that gives the AD500 excellent stability characteristics.

ICL7109 - A 12-bit, plus sign, dual-slope integrating CMOS A/D converter manufactured by Maxim. It digitizes the output of the PGA and converts it to a format that is read into the computer through the 8255 PPI.

8255 - A programmable peripheral interface (PPI) manufactured by many companies, but originally developed by Intel Corporation. The PPI serves as a general digital interface component to dramatically reduce the chip count of Real Time Devices' I/O boards. It buffers the data bus, selects the input channel, controls the PGA gain, starts conversions, and reads data from the A/D converter. The PPI also controls the external digital lines. Details on controlling the PPI were presented in Chapter 3.

## MULTIPLEXER

### Description

The Harris HI-508A is an eight-channel, single ended, analog multiplexer with active overvoltage protection. Analog input levels may greatly exceed either power supply (+/-12V) without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 64 volt peak-to-peak levels and typically survive static discharges beyond 4,000 volts. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur; each input presents 1 kohm of resistance under this condition. These features make the HI-508A ideal for use in systems where the analog inputs originate from separately powered circuitry. The HI-508A is fabricated with 44 volt dielectrically isolated CMOS technology.

### Control

As shown in the HI-508A Functional Block Diagram, Figure 4-2, the multiplexer is controlled using three of the PPI's Port B I/O signals. Details of controlling the channel selection were explained in Chapter 3.

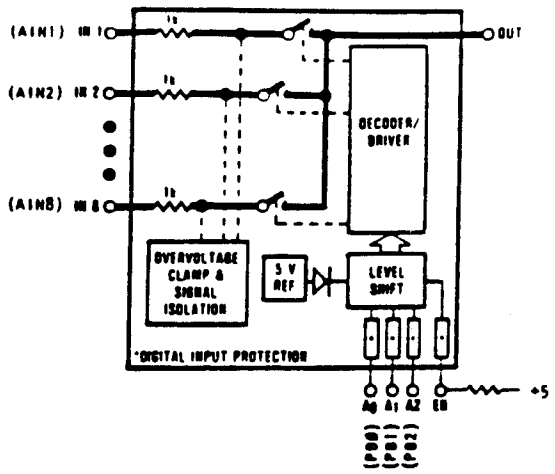



**Fig. 4-2** **HI-508A Functional Block Diagram**
(Compliments of Harris Semiconductor, copyright 1986)

### Operation

The portions of the Harris data sheet for the HI-508A which contain the specifications of concern to your application are reprinted in Appendix A "Specifications".

## PROGRAMMABLE GAIN AMPLIFIER

### Description

The Burr-Brown PGA102 is a precision digitally-programmable gain amplifier. One of three gains (1, 10, or 100) can be software selected. High performance thin-film resistors with excellent temperature tracking assure low gain drift and high stability. The high accuracy is very beneficial in test equipment and instrumentation applications where programmable or fixed gain is required.

### Control

As shown in the PGA102 Functional Block Diagram, Figure 4-3, the PGA is controlled using two of the PPI's Port C I/O signals. Details of controlling the gain setting were explained in Chapter 3.

### Operation

The portions of the Burr-Brown data sheet for the PGA102 which contain the specifications of concern to your application are reprinted in Appendix A, "Specifications".

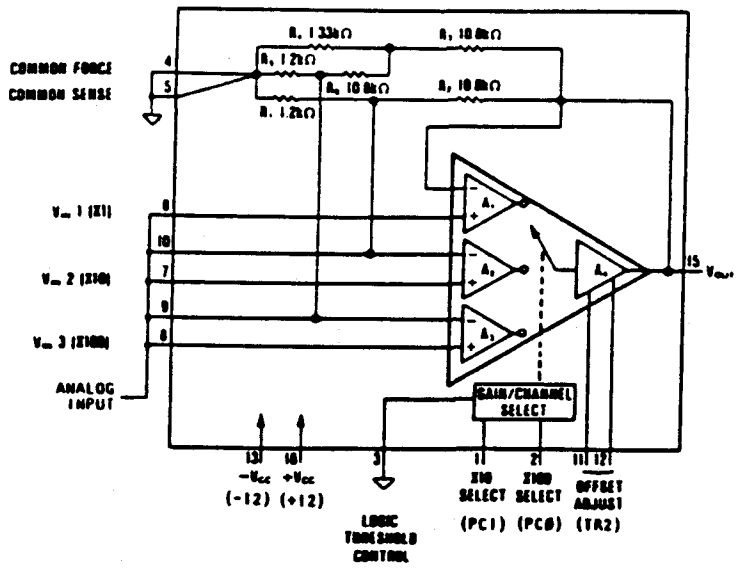



**Fig. 4-3** PGA102 Functional Block Diagram (Compliments of Burr-Brown Corporation, copyright 1986)

## REFERENCE

The Precision Monolithics REF-02 provides a stable voltage reference for the A/D converter. Its low noise and excellent temperature stability, which is achieved with a band gap design, contribute to the overall performance of the converter.

## A/D CONVERTER

### Description

The Maxim ICL7109 12-bit A/D converter digitizes an analog input signal into a 12-bit word plus a sign bit to indicate the polarity of the signal. It is a low power CMOS dual-slope integrating A/D converter. The ICL7109 has a very high input impedance reflected by its input bias current of about 1 picoamp, a sophisticated auto-zero circuit to minimize internal offset voltages, and a low input noise specification of about 15 microvolts, peak-to-peak. The integrating A/D's method of conversion is characterized by high accuracy and noise immunity.

### Control

The AD500 will perform A/D conversions continuously using the Continuous Convert or Strobed Convert Mode or on demand in the Single Convert Mode. The mode that is selected will determine the conversion rate.

Figure 4-4 shows the A/D conversion timing in the Continuous Convert Mode, i.e., when the START CONVERT signal is held high.

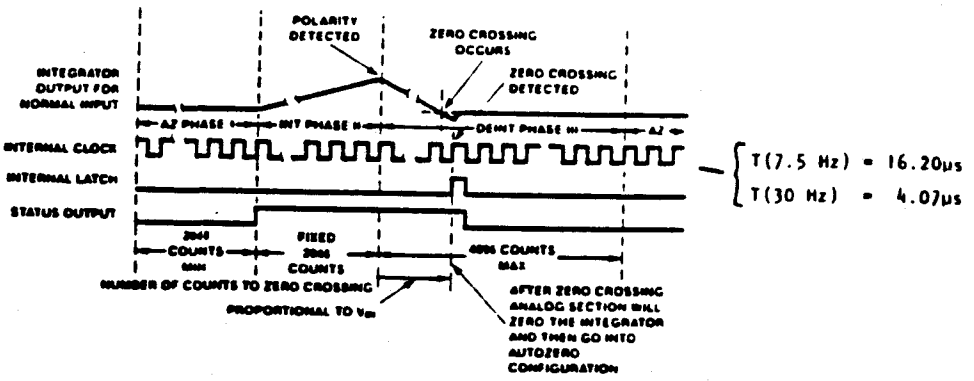



**Fig. 4-4 Conversion Timing: Continuous Convert Mode**
(Compliments of Maxim Integrated Products, Inc., copyright 1985)

In this mode of operation, a conversion cycle consists of a fixed number of 8192 clock cycles. Regardless of input signal voltage, this conversion rate is a consistant 7.5 or 30 conversions per second, depending upon the hardware configuration of the AD500. This is a period of 133.33 milliseconds for a 7.5 Hz rate or 33.33 milliseconds for a 30 Hz rate. Refer to Chapter 2 to determine how to select the conversion speed.

Figure 4-5 shows the conversion timing when the AD500 is in the Single Convert or Strobed Convert Mode. In these modes, the START CONVERT signal is pulsed high and then low to initiate each conversion.

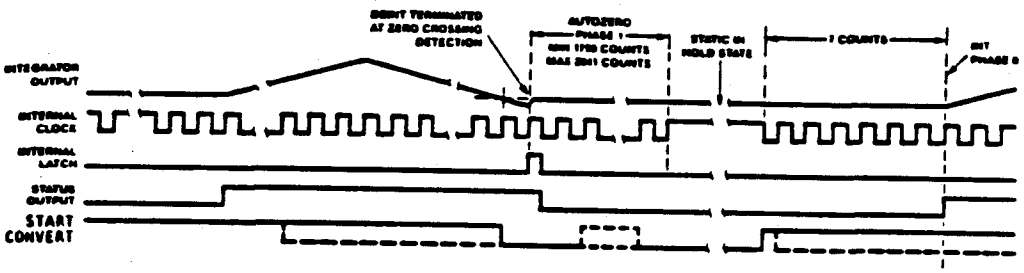



**Fig. 4-5 Conversion Timing: Single Convert and Strobed Convert Modes**
(Compliments of Maxim Integrated Products, Inc., copyright 1985)

As discussed in Chapter 3, the START CONVERT signal should remain high until the zero crossing detection occurs and the A/D result has been strobed into the PPI. This insures that the START CONVERT signal will be recognized by the A/D converter. The conversion rate in the Single Convert and Strobed Convert Modes of operation will be proportional to the magnitude of the input signal. The conversion rate will range from a maximum of 15 Hz for a 0 volt input, to a minimum of 7.5 Hz for a full scale input of +/-5 volts when switch S1 is set for 7.5, or 60 Hz to 30 Hz when switch S1 is set for 30.

To determine the actual conversion speed of the AD500 in the Single Convert and Strobed Convert modes of operation, you can monitor the ICL7109 STATUS output signal. This signal is available at pin 2 of U3, and a low to high transition will indicate the beginning of each conversion cycle. The timing diagram in Figure 4-5 illustrates the activity of the STATUS output signal in the Single Convert and Strobed Convert Modes.

## Operation

Figure 4-6 shows a block diagram of the analog section of the ICL7109 A/D converter.

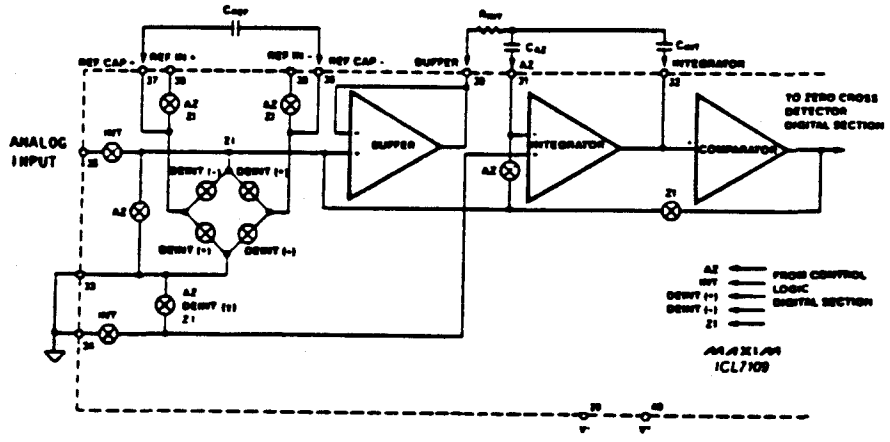



**Fig. 4-6 ICL7109 Analog Section**
(Compliments of Maxim Integrated Products, Inc., copyright 1985)

Each measurement cycle is divided into four phases:

| | |
|---|---|
| Auto-Zero | (AZ) |
| Signal Integrate | (INT) |
| De-integrate | (DE) |
| Zero Integrator | (ZI) |

The timing for these four phases is shown in Figure 4-4 or 4-5, above, depending of the AD500 conversion mode selected.

## Auto-Zero Phase

The buffer and the integrator inputs are disconnected from input high and input low and connected to analog COMMON. The reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to charge the auto-zero capacitor, Caz, to compensate for offset voltage in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. The offset referred to the input is less than 10 microvolts.

## Signal Integrate Phase

The buffer and integrator inputs are removed from COMMON and connected to input high and input low. The auto-zero loop is opened. The auto-zero capacitor is placed in series in the loop to provide an equal and opposite compensating offset voltage. The differential voltage between input high and input low is integrated for a fixed time of 2048 clock periods. At the end of this phase, the polarity of the integrated signal is determined.

## De-Integrate Phase

The reference voltage is applied to the buffer and integrator inputs. Circuitry within the chip ensures that the reference capacitor voltage will be connected with the correct polarity to cause the integrator output to return to the zero crossing (established by Auto-Zero) with a fixed slope. The time, represented by the number of clock periods counted for the output to return to zero, is proportional to the input signal.

## Zero Integrator Phase

Input low is shorted to analog Common and the reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to input high, causing the integrator output to return rapidly to zero (See Figure 4-7). This phase normally lasts between 16 and 32 clock pulses but is extended to 1552 clock pulses after an overrange conversion.

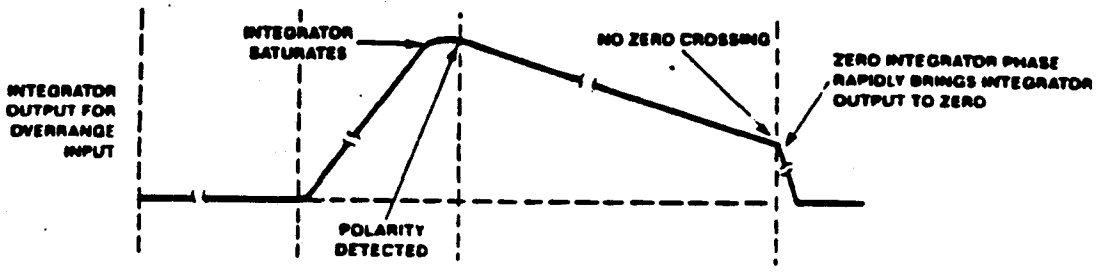



**Fig. 4-7 Integrator Output for Overrange Input**
(Compliments of Maxim Integrated Products, Inc., copyright 1985)

This phase will remcve any residual charge left on the integrator capacitor after an overload reading. This Zero Integrator phase virtually eliminates the problem of interaction or "crosstalk" between the various channels of a multiple channel data acquisition system. Without the zero integrator phase, an overload on one channel would leave charge on the integrator capacitor, which would then be transferred to the autozero capacitor during the autozero cycle, resulting in an erroneous reading for the next channel that is measured after the channel with the overload.

## Integrating Converter Features

The output of integrating A/D converters represents the integral or average of an input voltage over a fixed period of time. Compared with techniques in which the input is sampled and held, the integrating converter will average the effects of noise. A second important characteristic is that time is used to quantise the answer, resulting in extremely small nonlinearity errors and no missing output codes. The integrating converter also has very good rejection of frequencies that are an integral multiple of the measurement frequency (see Figure 4-8).

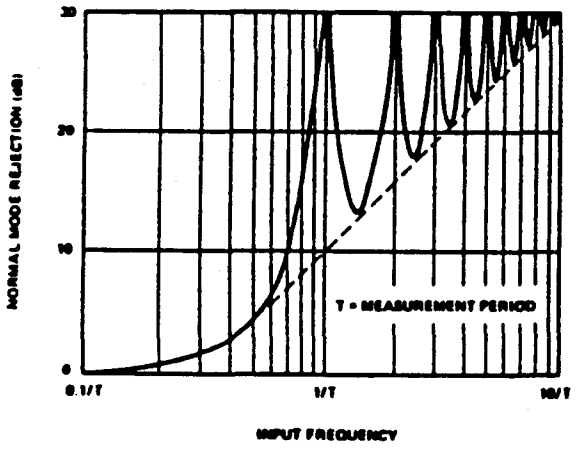



**Fig. 4-8 Normal Mode Rejection of Dual-Slope Converter as a Function of Frequency**
(Compliments of Teledyne Semiconductor)

When using an AD500 that is configured for a 7.5 Hz conversion rate, this feature can be used to advantage in reducing line frequency noise. Referring to Figures 4-4 or 4-5, you will notice that the conversion period , T, of the ICL7109 (the time spent in the Signal Integrate Phase) is 33.185 milliseconds. As shown in Figure 4-9, this is very close to two full periods of 60 Hz line frequency noise.

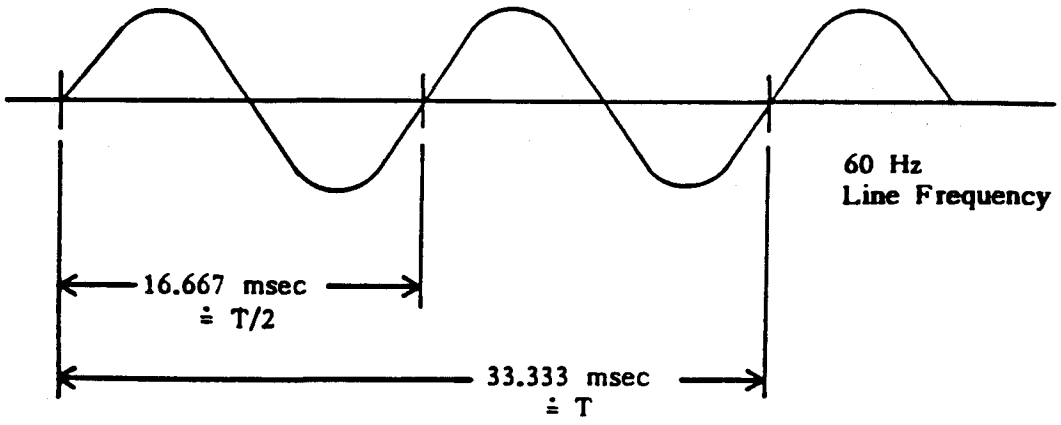



**Fig. 4-9 AD500 Conversion Period (T) Relative to 60 Hz Line Frequency (7.5 Hz AD500)**

# Chapter 5

## Calibration

The AD500 is factory calibrated to maximize its performance over all three gain ranges. The following procedure is provided to allow you to quickly verify the performance of your AD500. This should be done approximately every six months or whenever inaccurate readings are suspected.

You may want to recalibrate your AD500 if your application will require the use of only one or two gains or you will be using all positive or all negative input voltages. Also, because the AD500 is factory calibrated for a 7.5 Hz conversion rate, you may need to recalibrate your board if you select a 30 Hz rate using switch S1.

## EQUIPMENT REQUIRED

The following equipment is required for calibration:

Precision voltage source: 0 to +/- 5 volts
Digital Volt Meter (DVM): 5-1/2 digit
4" Jumper wire

A voltage source may be assembled using a 9 volt battery and precision 10-turn trimming potentiometer as shown in the following circuit, Figure 5-1.

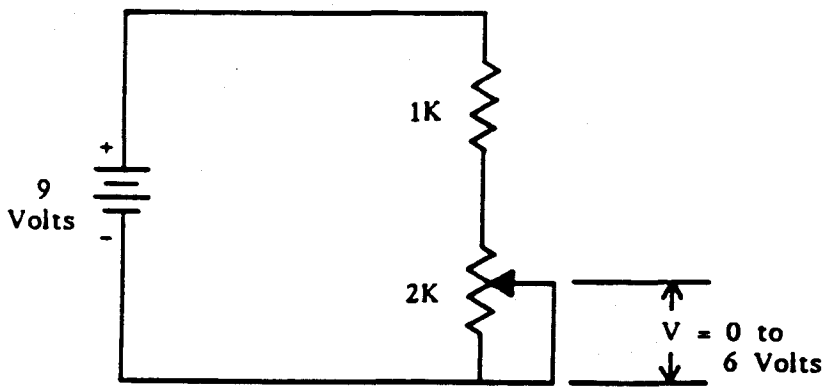



**Fig 5-1 Adjustable Voltage Source**

## CALIBRATION PROCEDURE

Calibration is performed with a properly configured AD500 installed in the PC. Apply power to the computer, and allow the AD500 circuitry to stabilize for 15 minutes. Connections will need to be made to some of the analog inputs at the P4 connector (see Figure B-1 in Appendix B).

There are only two adjustments necessary to completely calibrate the AD500. These affect the offset and full scale performance of the AD500 circuitry. Both calibration steps are performed using trimpots TR1 and TR2, which are located at the top of the AD500 PC board (see Figure 2-1 in Chapter 2). Trimpot TR1 is used for full-scale adjustment and trimpot TR2 is used to zero the offset error of the PGA.

### Offset Adjustment

The offset adjustment on the AD500 may be used to compensate for the inherent offset output voltage of the PGA. This adjustment effects the offset for all three gains: all offsets move as the potentiometer is adjusted. By compromising, you can adjust for the average offset of all three gains, or a compromise for just the X10 and X100 gains can be made, considering the unity gain channel's offset is insignificant for high-level inputs.

The AD500 is factory calibrated to minimize the effect of the offset voltage when a gain of X100 is selected. However, your application may require that the offset be minimized for another gain setting. To adjust the offset error of the AD500, the analog input will be connected to analog ground, and trimpot TR2 will be adjusted while continuously taking A/D conversions. The Program Disk contains a calibration routine that will allow the gain to be changed interactively while displaying the results of each A/D conversion. Refer to the description in the README.DOC file on the Program Disk for details on using this routine.

To perform the offset adjustment, jumper AIN1 (P4-6) to analog ground (P4-1) at the P4 connector. Refer to Appendix B for the pin assignment of the P4 connector. Run the calibration routine and adjust potentiometer T2 to trim the offset voltage to minimize its effect for the gain(s) of interest.

Because the offset voltage is related soley to the performance of the PGA, its adjustment will be independent of input channel. However, the offset adjustment will effect the rollover performance of the A/D converter. Rollover is the difference in the conversion results between voltages having the same amplitude but different polarities. Any gains which do not have a zero offset will give readings that are shifted from an ideal zero reference, causing positive and negative readings of the same voltage to be slightly different. This difference is a direct effect of the offset adjustment.

### Full Scale Adjustment

The full scale adjustment calibrates the reference voltage used by the A/D converter to compensate for the analog input circuitry of the AD500. It is performed while a voltage equal to (Full Scale - 1½ Least Significant Bit) is applied to the analog input of the AD500 I/O connector. This voltage represents the ideal input voltage corresponding to the last code change between a Full Scale reading and 1½ LSB below FS. The A/D converter will be calibrated by monitoring the conversion results while adjusting trimpot TR1.

Place the A/D converter in the Continuous Convert Mode with a gain of 1, and display the conversion results. The Program Disk contains a routine that can be used while performing the full scale adjustment. Apply the output of the voltage source between analog input AIN1 (P4-6) and analog ground (P4-1). Use the DVM and adjust the voltage source so that a full scale voltage minus 1½ LSB is applied at the P4 connector.

Table 5-1 lists the voltages that correspond to this input for a 12-bit A/D converter for gains of 1, 10, and 100. The A/D converter results for these input voltages and gain settings should flicker between all ones, X'FFF', and X'FFE'. Adjust trimpot TR1 until the values 4095 and 4094 are displayed.

Also listed in Table 5-1 are the ideal voltages that correspond to each bit weight of a 12-bit A/D converter. Refer to the analog input and A/D specifications for the AD500 in Appendix A when checking the performance of your AD500 with these input voltages.

| Table 5-1 12-Bit A/D Converter Bit Weights | | | |
|---|---|---|---|
| A/D Bit Weight | Ideal Input Voltage (mV) | | |
| | X1 | X10 | X100 |
| 4095 | 4998.8 | 499.88 | 49.987 |
| (FS - 1½ LSB) | 4998.2 | 499.82 | 49.982 |
| 2048 | 2500.0 | 250.00 | 25.000 |
| 1024 | 1250.00 | 125.000 | 12.500 |
| 512 | 625.00 | 62.500 | 6.2500 |
| 256 | 312.50 | 31.250 | 3.1250 |
| 128 | 156.250 | 15.6250 | 1.5625 |
| 64 | 78.125 | 7.8125 | 0.7813 |
| 32 | 39.063 | 3.9063 | 0.3906 |
| 16 | 19.5313 | 1.9531 | 0.1953 |
| 8 | 9.7656 | 0.9766 | 0.0977 |
| 4 | 4.8828 | 0.4883 | 0.0488 |
| 2 | 2.4414 | 0.2441 | 0.0244 |
| 1 | 1.2207 | 0.1221 | 0.0122 |

# Appendix A

Specifications

AD500 SPECIFICATIONS

**Interface**

IBM PC/XT/AT compatible

Jumper-selectable base address,

| | | | |
|---|---|---|---|
| I/O mapped: | (hex) | 200 | 300 |
| | | 240 | 340 |
| | | 280 | 380 |
| | | 2C0 | 3C0 |

Jumper-selectable interrupt

PC IRQ channels supported: 2 - 7

**Analog Inputs**

8 channels, single-ended

| | |
|---|---|
| Impedance: | 700 Megohms |
| Gains -- software programmable: | 1, 10, 100 |
| Gain error: | 0.5% typ., 1% max. |
| Input range: | +/-5 V, +/-500 mV, +/-50 mV |
| Zero shift with gain change: | 5 bits, max. |
| Overvoltage protection: | +/-35 Vdc |
| Settling time: | 5 usec, max. |

**A/D Specifications**

| | | |
|---|---|---|
| Type: | Dual-slope integrating with auto-zero, ICL7109 | |
| Resolution: | 12 bits plus sign | |
| Conversion rate: (Min., Hz) | 7.5/30, switch selectable | |
| Relative accuracy: | +/-1 bit, gain=1 | |
| Linearity: (gain=1) | +/-1 bit | (7.5 Hz) |
| | +/-3 bits | (30 Hz) |
| Rollover error: | +/-1 bit | |

**Digital I/O**

7 TTL compatible lines:

Input or output -- 2 lines

Output -- 5 lines

**Miscellaneous Outputs** (PC-bus sourced)

Reset Driver

+/-12 Vdc

Digital ground

**Software Features**

Interactive programs are included that allow immediate verification of the operation of the AD500. BASIC examples are provided which demonstrate the control of the A/D converter, input MUX, and gain selection.

A complete directory of all software included with the AD500 is listed on the accompanying disk.

**Electrical**

Current requirements:

| | |
|---|---|
| +5V | 20 mA |
| +12V | 15 mA |
| -12V | 13 mA |

**Mechanical**

Connectors:

40-pin, right angle, shrouded header with ejector tabs
Edge-connector -- IBM PC/XT/AT compatible

Environmental:

| | |
|---|---|
| Operating temperature: | 0 to +50 deg. Centigrade |
| Storage temperature: | -20 to +70 deg. Centigrade |
| Humidity: | 0 to 90%, non-condensing |

Size: 3.875"H X 5.25"W (Short slot)

Warranty: 1 year

intel

## ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias. . . . . 0°C to 70°C
Storage Temperature . . . . . –65°C to +150°C
Voltage on Any Pin
With Respect to Ground . . . . . –0.5V to +7V
Power Dissipation . . . . . 2501mW

*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## D.C. CHARACTERISTICS ($T_A$ = 0°C to 70°C, $V_{CC}$ = +5V ± 5%, GND = 0V)

| Symbol | Parameter | Min. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | -0.3 | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | 2.2 | 5.5 | V | |
| $V_{OL}$ (DB) | Output Low Voltage (Data Bus) | | 0.45 | V | $I_{OL}$ = 2.5mA |
| $V_{OL}$ (PER) | Output Low Voltage (Peripheral Port) | | 0.45 | V | $I_{OL}$ = 1.7mA |
| $V_{OH}$ (DB) | Output High Voltage (Data Bus) | 2.4 | | V | $I_{OH}$ = -400μA |
| $V_{OH}$ (PER) | Output High Voltage (Peripheral Port) | 4.2 | | V | $I_{OH}$ = -100μA |
| $I_{DAR}$[1] | Darlington Drive Current | -1.0 | -5.0 | mA | $R_{EXT}$ =1.1KΩ; $V_{EXT}$ = 1.5V |
| $I_{CC}$ | Power Supply Current | | 5.0 | mA | |
| $I_{IL}$ | Input Load Current | | ±10 | μA | $V_{IN}$ = $V_{CC}$ to 0V |
| $I_{OFL}$ | Output Float Leakage | | ±10 | μA | $V_{OUT}$ = $V_{CC}$ to 0V |

**NOTE:**
1. Available on any 8 pins from Port B and C.

## CAPACITANCE ($T_A$ = 25°C, $V_{CC}$ = GND = 0V)

| Symbol | Parameter | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 10 | pF | fc = 1MHz |
| $C_{I/O}$ | I/O Capacitance | | | 20 | pF | Unmeasured pins returned to GND |

## A.C. CHARACTERISTICS ($T_A$ = 0°C to 70°C, $V_{CC}$ = +5V ± 5%, GND = 0V)

**Bus Parameters**

**READ**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{AR}$ | Address Stable Before READ | 0 | | ns |
| $t_{RA}$ | Address Stable After READ | 0 | | ns |
| $t_{RR}$ | READ Pulse Width | 150 | | ns |
| $t_{RD}$ | Data Valid From READ[1] | | 100 | ns |
| $t_{DF}$ | Data Float After READ | 0 | 40 | ns |
| $t_{RV}$ | Time Between READs and/or WRITEs | 150 | | ns |

## A.C. CHARACTERISTICS (Continued)

**WRITE**

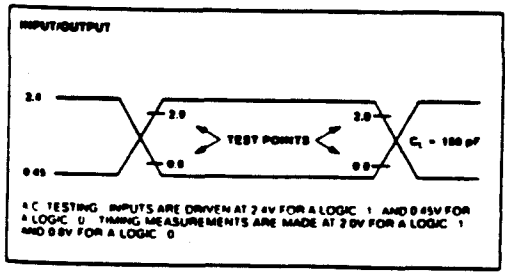
| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{AW}$ | Address Stable Before WRITE | 0 | | ns |
| $t_{WA}$ | Address Stable After WRITE | 20 | | ns |
| $t_{WW}$ | WRITE Pulse Width | 120 | | ns |
| $t_{DW}$ | Data Valid to WRITE (T.E.) | 100 | | ns |
| $t_{WD}$ | Data Valid After WRITE | 30 | | ns |

**OTHER TIMINGS**

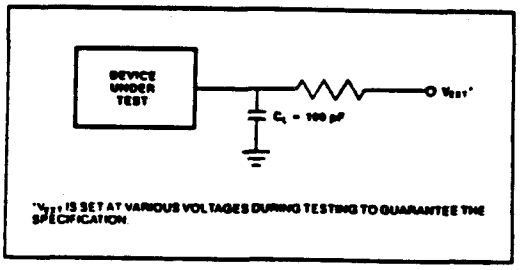
| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{WB}$ | WR = 1 to Output[1] | | 350 | ns |
| $t_{IR}$ | Peripheral Data Before RD | 0 | | ns |
| $t_{HR}$ | Peripheral Data After RD | 0 | | ns |

**NOTES:**
1. Test Conditions: $C_L$ = 150pF.
2. Period of Reset pulse must be at least 50μs during or after power on. Subsequent Reset pulse can be 500 ns min.

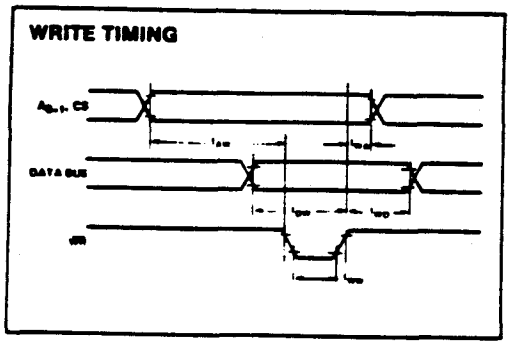
### A.C. TESTING INPUT, OUTPUT WAVEFORM



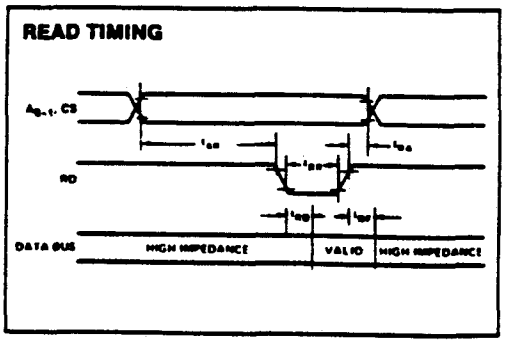

### A.C. TESTING LOAD CIRCUIT




### WRITE TIMING

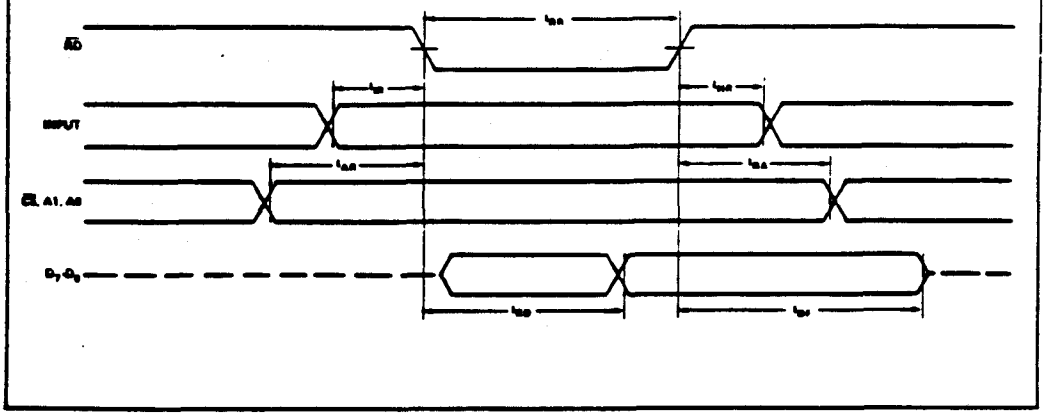



### READ TIMING

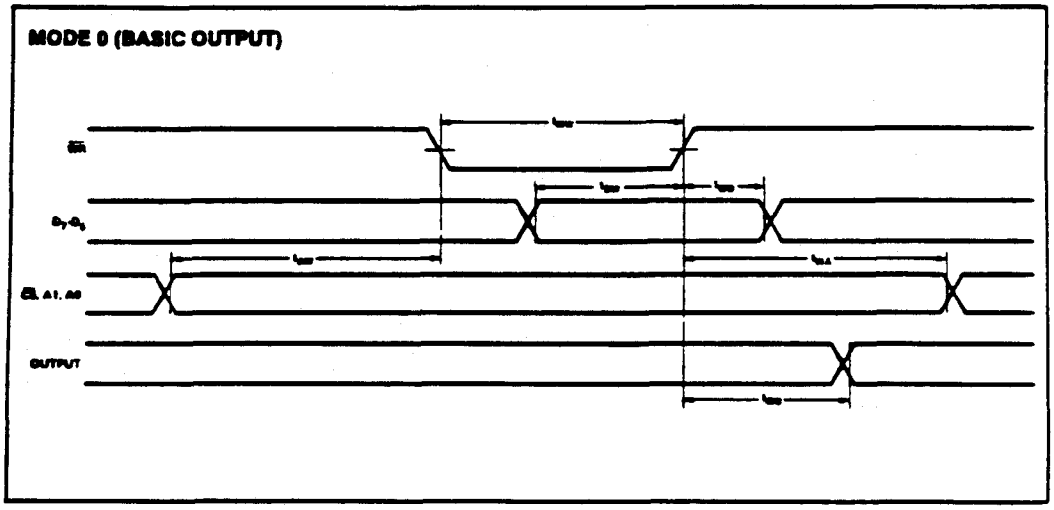


## WAVEFORMS

**MODE 0 (BASIC INPUT)**



**MODE 0 (BASIC OUTPUT)**

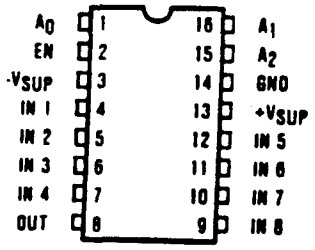


Harris HI-508A
Analog Input Multiplexer

SPECIFICATIONS

## Pinout

Top View




HI3-508A (plastic)

### ABSOLUTE MAXIMUM RATINGS (Note 1)

| | | | |
|---|---|---|---|
| Voltage between Supply Pins | 44 V | Continuous Current, S or D: | 20 mA |
| V+ to Ground | 22 V | Peak Current, S or D (Pulsed at 1 ms, 10% duty cycle max): | 40 mA |
| V− to Ground | 25 V | Power Dissipation* (CERDIP) | 1.28 W |
| Analog Input Overvoltage: | | Operating Temperature Range: HI-508A-5 | 0°C to +75°C |
| $V_S$ { $V_{Supply(+)}$ | +20 V | Storage Temperature Range | −65°C to +150°C |
| $V_S$ { $V_{Supply(-)}$ | −20 V | | |

*Derate 12.8 mW/°C above $T_A$ = 75°C

### ELECTRICAL CHARACTERISTICS

Supplies = +15 V, −15 V; $V_{AH}$ (Logic Level High) = +4.0 V, $V_{AL}$ (Logic Level Low) = +0.8 V (unless otherwise specified).
For Test Conditions, consult Performance Characteristics Section.

| PARAMETER | TEMP. | HI-508A/508A-5 MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|
| ANALOG CHANNEL CHARACTERISTICS | | | | | |
| *$V_S$, Analog Signal Range | Full | −15 | | +15 | V |
| *$R_{ON}$, On Resistance (Note 2) | +25°C | | 15 | 18 | kΩ |
| | Full | | 18 | 20 | kΩ |
| *$I_S$ (OFF), Off Input Leakage Current (Note 3) | +25°C | | 003 | | nA |
| | Full | | | 50 | nA |
| *$I_D$ (OFF), Off Output Leakage Current (Note 3) | +25°C | | 01 | | nA |
| HI-508A | Full | | | 200 | nA |
| *$I_D$(OFF) with Input Overvoltage Applied (Note 4) | +25°C | | 40 | | nA |
| | Full | | | | μA |
| *$I_D$ (ON), On Channel Leakage Current (Note 3) | +25°C | | 01 | | nA |
| HI-508A | Full | | | 200 | nA |
| "OFF Isolation" (Note 5) | +25°C | 50 | 88 | | dB |
| $C_S$ (OFF), Channel Input Capacitance | +25°C | | 5 | | pF |

*100% tested for Dash 8. Leakage currents not tested at +55°C

NOTES: 1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. $V_{OUT}$ = ±10V, $I_{OUT}$ = −1mA
3. Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Analog Overvoltage = ±33 V
5. $V_{EN}$ = 0.8 V, $R_L$ = 1 kΩ, $C_L$ = 15 pF, $V_S$ = 7 $V_{RMS}$, f = 100 kHz. Worst Case isolation occurs on channel 4 due to proximity of the output pins.

### TRUTH TABLE

HI-508A

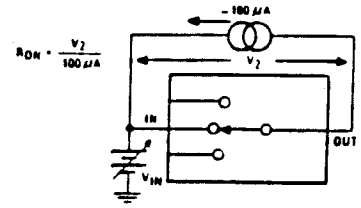
| $A_2$ | $A_1$ | $A_0$ | EN | "ON" CHANNEL |
|---|---|---|---|---|
| X | X | X | L | NONE |
| L | L | L | H | 1 |
| L | L | H | H | 2 |
| L | H | L | H | 3 |
| L | H | H | H | 4 |
| H | L | L | H | 5 |
| H | L | H | H | 6 |
| H | H | L | H | 7 |
| H | H | H | H | 8 |

## *Performance Characteristics and Test Circuits*

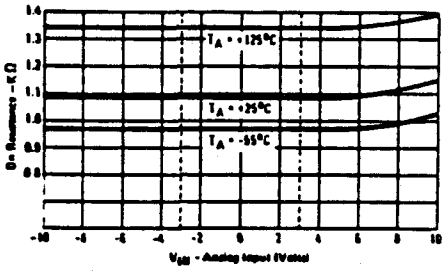
Unless Otherwise Specified $T_A$ = 25°C, $V_{Supply}$ = ±15 V, $V_{AH}$ = +4 V, $V_{AL}$ = 0.8 V

ON RESISTANCE vs
INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

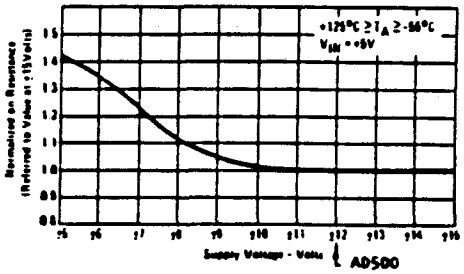
TEST CIRCUIT
NO. 1




ON RESISTANCE
vs. ANALOG INPUT VOLTAGE

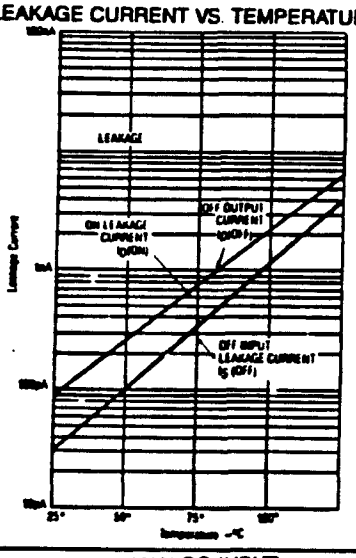



NORMALIZED ON RESISTANCE
vs. SUPPLY VOLTAGE

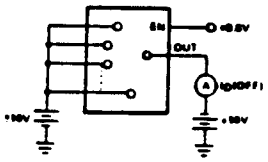



AD500

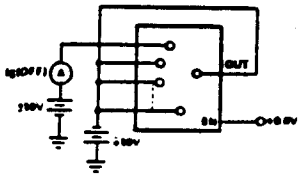
LEAKAGE CURRENT VS. TEMPERATURE



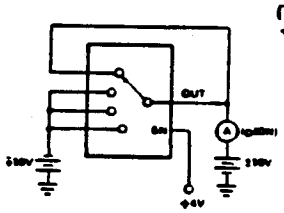

TEST CIRCUIT
NO. 2*




TEST CIRCUIT
NO. 3*

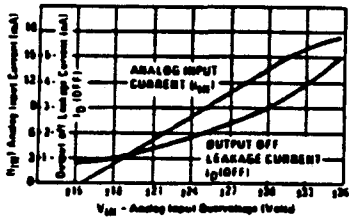



TEST CIRCUIT
NO. 4*



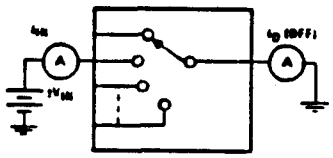

*Two measurements per channel:
+10 V/−10 V and −10 V/+10 V.
(Two measurements per device for $I_D$(OFF):
+10 V/−10 V and −10 V/+10 V.)

ANALOG INPUT
OVERVOLTAGE CHARACTERISTICS

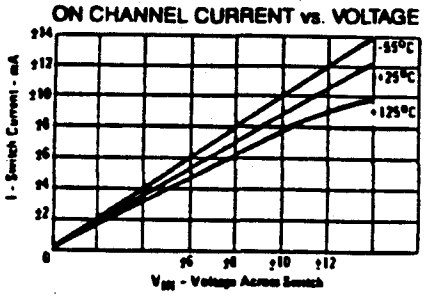



TEST CIRCUIT
NO. 5

ANALOG INPUT
OVERVOLTAGE CHARACTERISTICS

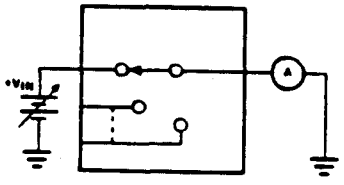



ON CHANNEL CURRENT vs. VOLTAGE

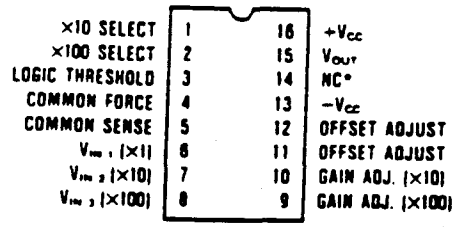



TEST CIRCUIT
NO. 6

ON CHANNEL CURRENT
vs. VOLTAGE



## PIN CONFIGURATION




*NO INTERNAL CONNECTION

# SPECIFICATIONS

## ELECTRICAL

At +25°C, ±$V_{cc}$ = 15VDC unless otherwise specified

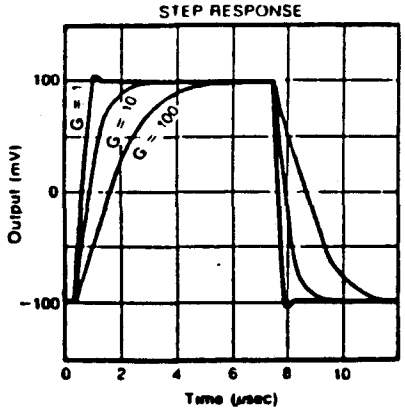
| PARAMETER | CONDITIONS | PGA102KP MIN | PGA102KP TYP | PGA102KP MAX | UNITS |
|---|---|---|---|---|---|
| **GAIN** | | | | | |
| Inaccuracy[1] | $R_L$ = 2kΩ, G = 1 | | 0.007 | 0.02 | % |
| | G = 10 | | 0.015 | 0.05 | % |
| | G = 100 | | 0.02 | 0.08 | % |
| vs Temperature | G = 1 | | 0.4 | 5 | ppm/°C |
| | G = 10 | | 2 | 7 | ppm/°C |
| | G = 100 | | 9 | 20 | ppm/°C |
| Nonlinearity | $R_L$ = 2kΩ, G = 1 | | 0.001 | 0.003 | % of FS |
| | G = 10 | | 0.002 | 0.005 | % of FS |
| | G = 100 | | 0.003 | 0.01 | % of FS |
| **INPUT OFFSET VOLTAGE** | | | | | |
| Initial[2] | G = 1 | | 200 | 1500 | µV |
| | G = 10 | | 70 | 600 | µV |
| | G = 100 | | 70 | 600 | µV |
| vs Temperature | G = 1 | | 7 | 50 | µV/°C |
| | G = 10 | | 3 | 10 | µV/°C |
| | G = 100 | | 2 | 7 | µV/°C |
| vs Supply Voltage | ±5 < $V_{cc}$ < ±18V | | | | |
| | G = 1 | | 30 | 70 | µV/V |
| | G = 10 | | 8 | 30 | µV/V |
| | G = 100 | | 8 | 30 | µV/V |
| **INPUT NOISE** | | | | | |
| Voltage Noise | $f_B$ = 0.1Hz to 10Hz | | | | |
| | G = 1 | | 4.5 | | µV p-p |
| | G = 10 | | 1.5 | | µV p-p |
| | G = 100 | | 0.6 | | µV p-p |
| Voltage Noise Density | $f_O$ = 1Hz, G = 1 | | 490 | | nV/√Hz |
| | G = 10 | | 178 | | nV/√Hz |
| | G = 100 | | 83 | | nV/√Hz |
| | $f_O$ = 10Hz, G = 1 | | 155 | | nV/√Hz |
| | G = 10 | | 56 | | nV/√Hz |
| | G = 100 | | 20 | | nV/√Hz |
| Current Noise | $f_B$ = 0.1Hz to 10Hz | | 76 | | pA p-p |
| Current Noise Density | $f_O$ = 1Hz | | 8.8 | | pA/√Hz |
| | $f_O$ = 10Hz | | 2.8 | | pA/√Hz |
| | $f_O$ = 100Hz | | 0.99 | | pA/√Hz |
| | $f_O$ = 1kHz | | 0.43 | | pA/√Hz |
| **TEMPERATURE RANGE** | | | | | |
| Specification | $T_{A\ min}$ to $T_{A\ max}$ | 0 | | +70 | °C |
| Operating | | −25 | | +85 | °C |
| Storage | | −55 | | +125 | °C |
| Thermal Resistance | $\theta_{JA}$ | | 100 | | °C/W |

NOTES: (1) Gain inaccuracy is the percent error between the actual and ideal gain selected. It may be externally adjusted to zero for gains of 10 and 100. (2) Offset voltage can be adjusted for any one channel. Adjustment affects temperature drift by approximately ±0.3µV/°C for each 100µV of offset adjusted.

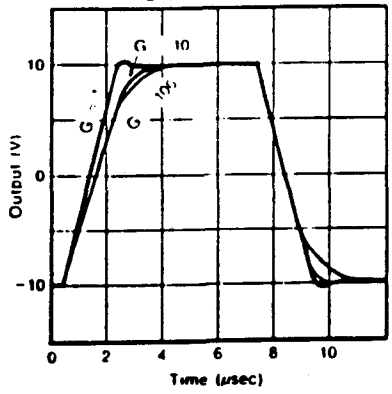
# TYPICAL PERFORMANCE CURVES (CONT)

$T_A$ = 25°C, $\pm V_{CC}$ = ±15VDC unless otherwise noted

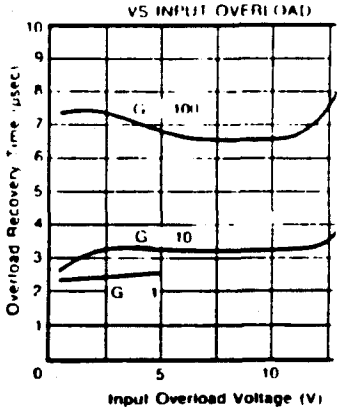
SMALL SIGNAL
STEP RESPONSE



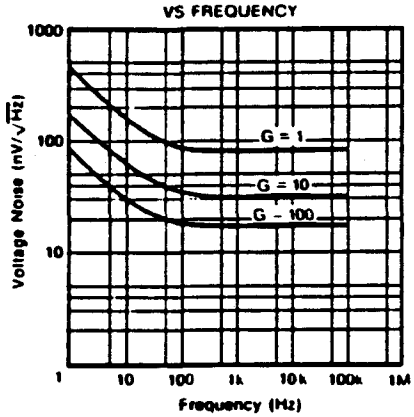

LARGE SIGNAL
STEP RESPONSE



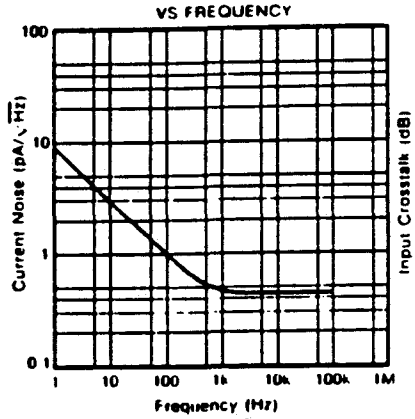

OVERLOAD RECOVERY
VS INPUT OVERLOAD



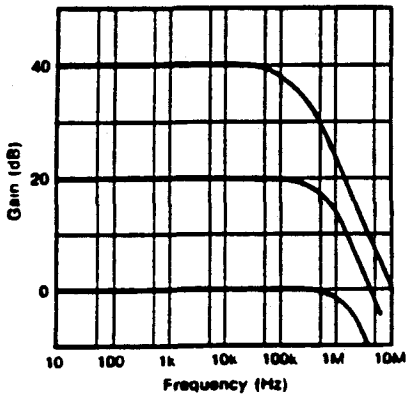

INPUT VOLTAGE NOISE
VS FREQUENCY



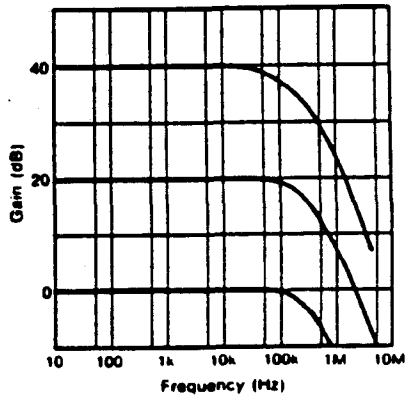

INPUT CURRENT NOISE
VS FREQUENCY



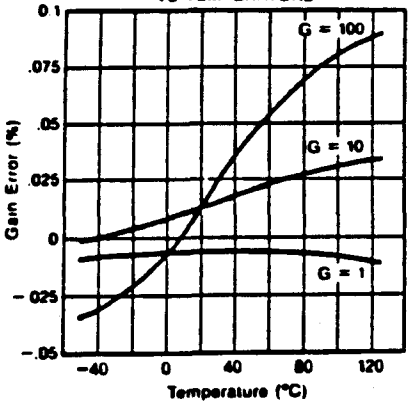

SMALL SIGNAL
FREQUENCY RESPONSE



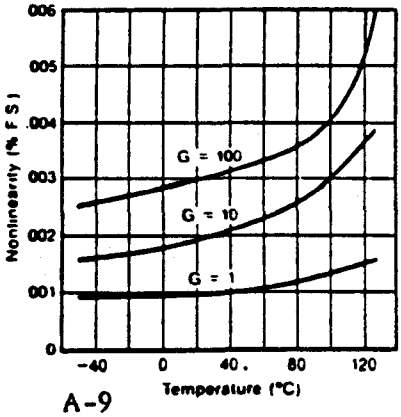

LARGE SIGNAL
FREQUENCY RESPONSE




GAIN ERROR
VS TEMPERATURE




NONLINEARITY
VS TEMPERATURE



# Appendix B

I/O Connector

| | | | |
|---|---|---|---|
| 1 | Analog Gnd | 21 | |
| 2 | AIN8 | 22 | AIN7 |
| 3 | AIN6 | 23 | AIN5 |
| 4 | Analog Gnd | 24 | AIN4 |
| 5 | AIN3 | 25 | AIN2 |
| 6 | AIN1 | 26 | Analog Gnd |
| 7 | | 27 | |
| 8 | | 28 | |
| 9 | | 29 | |
| 10 | | 30 | |
| 11 | PC7 | 31 | PC6 |
| 12 | | 32 | |
| 13 | | 33 | |
| 14 | | 34 | |
| 15 | PB7 | 35 | PB6 |
| 16 | PB5 | 36 | PB4 |
| 17 | PB3 | 37 | |
| 18 | | 38 | |
| 19 | +12 Volts | 39 | RESET DRV |
| 20 | -12 Volts | 40 | Digital Gnd |

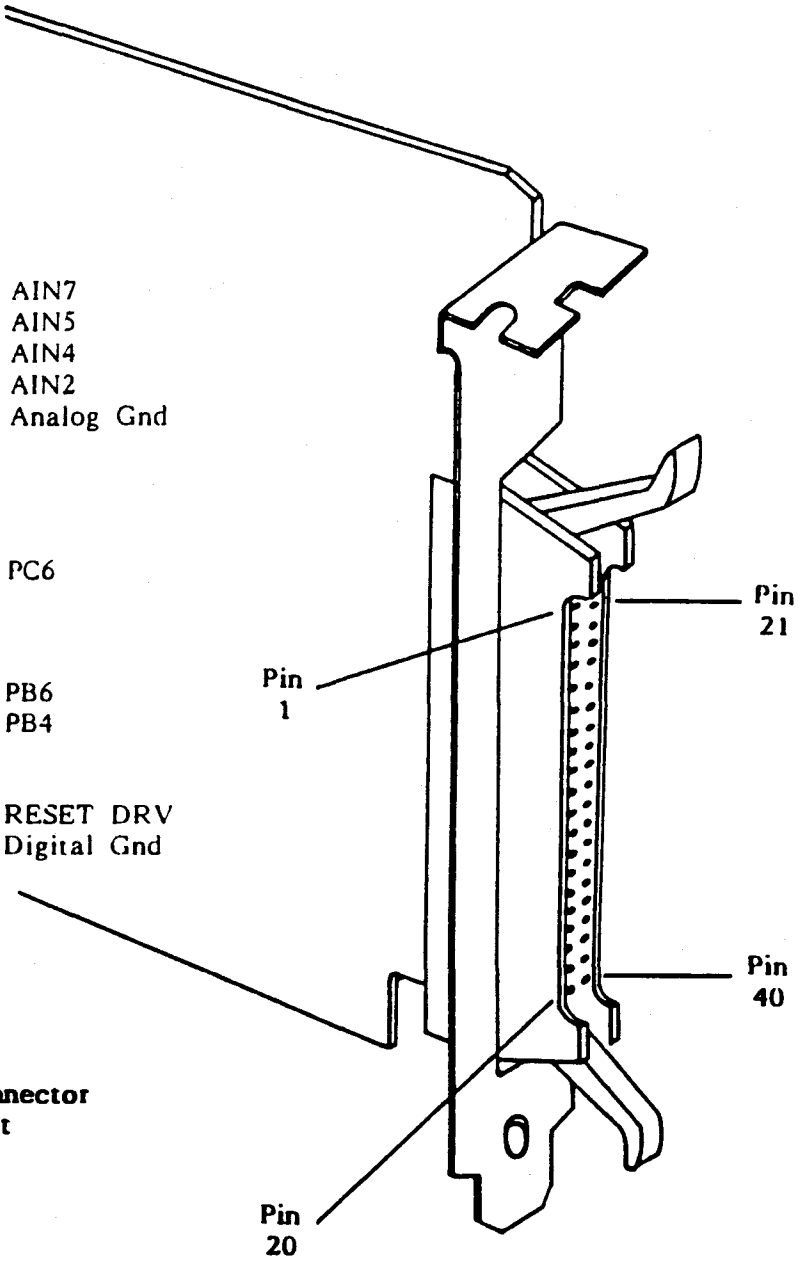



**Fig. B-1 AD500 P4 Connector Pin Assignment**

| Table B-1 AD500 P4 Connector/Mating Connector | | |
|---|---|---|
| Manufacturer | AD500 P4 Connector | P4 Mating Connector |
| KEL-AM Inc.<br>3M<br>Robinson Nugent<br>MIL C-83503 | 6201-040-258 | 6230-040-601<br>3417-7040<br>IDS-C40PK-C-SR-TG<br>M83503/7-09 |

# Appendix C

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# Appendix D

Warranty

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