TC1766

32-Bit Single-Chip Microcontroller

Microcontrollers

Never stop thinking

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TC1766 Documentation Addendum

Revision History: V1.2 2007-04

Previous Version: V1.1

Page	Subjects (major changes since last revision)
7	Figure 1-12 is updated.
8	The register long names for MMU_CON and D11 to D15 are corrected.
10	The desription for CRC generation and error checking is improved; the typo is corrected for EICR0.REN0, EICR0.REN1, EICR1.REN2 and EICR1.REN3
11	The typo of bit description GEEN1 is corrected.
19	The bit name and access type is corrected for bit 5 of PCP_ES register; the instruction field definition of Table 10-12 is updated.
20	Figure 10-14 is updated; the typo in the syntax description of the ST.PI instruction of the PCP is corrected
21	The typo in Figure 11-5 is corrected.
22	The description for Channel Reset Operation is improved.
23	The typo in Transaction Lost Interrupt section is corrected.
24	The typo in Move Engine Interrupt section is corrected.
28	The read and write access modes for address location F000 0804_H of Table 16-7 are corrected; the reserved column for address location F000 0850_H to F000 $08F4_H$ of Table 16-7 are split.
30	Typo in Slave Select Output Control and the description for Slave Select Register Update section are corrected.
32	A new note is added for SSOC and SSOTC registers; a new footnote is added to SSOTC.LEAD, SSOTC.TRAIL and SSOTC.INACT bit description.
33	A new paragraph is added to Receive FIFO section; the description when LEC=111B is improved; the CAN Bus State Information is updated in Table 20-8.
34, 35, 36	The typo for number of CAN interrupt outputs is corrected.
36	MLI receive clock max. frequency is corrected.
52	The formula for the timer period is corrected.

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1 Introduction

This document describes corrections, changes, and improvements for the two parts of the TC1766 User's Manual V1.1 2005-08, the System Units book (Volume 1) and the Peripheral Units book (Volume 2). These corrections will be considered with the next update of these User's Manual documents.

The referenced documents to this addendum are located at the Internet page:

- www.infineon.com/tc1766
- TC1766 System Units User's Manual (Vol.1), V1.1, Aug. 2005
- TC1766 Peripheral Units User's Manual (Vol.2), V1.1, Aug. 2005

2 User's Manual - System Units Part (Volume 1)

This section describes corrections for the System Units part of the User's Manual.

Page 1-10

The second bulleted point under Interrupt System must be corrected to "Flexible interrupt-prioritizing scheme with 25**5** interrupt priority levels."

Page 1-11

The bulleted point under Package must be corrected to "P**G**-LQFP-176-2 package, 0.5 mm pitch."

Page 1-33

Figure 1-12 should be replaced with the below figure:

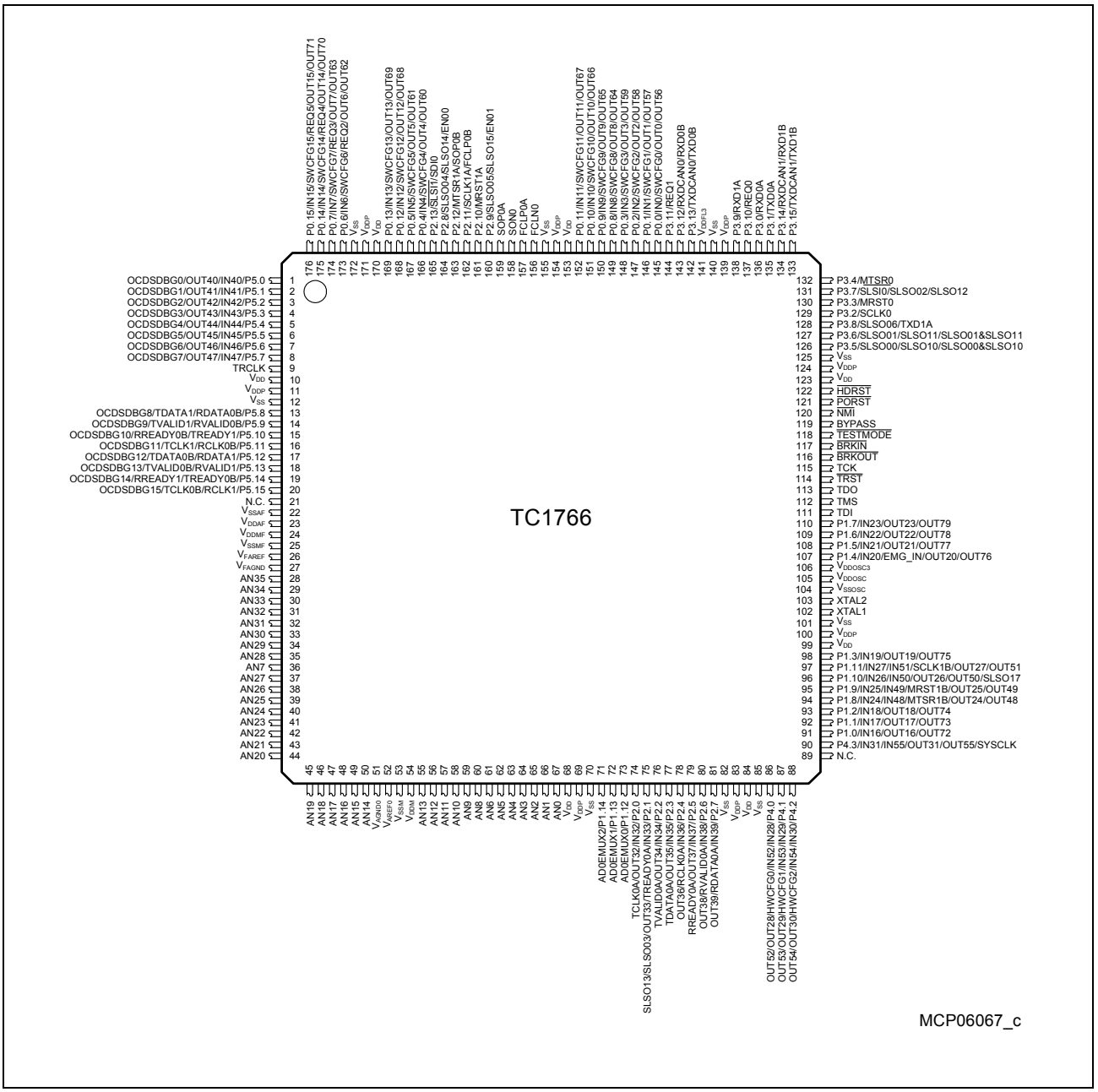

Figure 1-12 TC1766 Pinning for PG-LQFP-176-2 Package

Page 1-44

The pad driver class of pin $\overline{\text{HDRST}}$ is "A2" instead of "A1". The pad driver class of pin $\overline{\text{NMI}}$ and $\overline{\text{PORST}}$ are grouped as "A2".

Page 1-46

The footnotes 2 and 4 of Table 1-3 should be deleted.

Page 1-47

The following section has to be added after section 1.4.2:

1.4.3 Pull-Up/Pull-Down Behavior of the Pins

Table 1-5 List of Pull-up/Pull-down Reset Behavior of the Pins

Pins	$\overline{\text{PORST}}$ = 0	$\overline{\text{PORST}}$ = 1
All GPIOs, TDI, TMS, TDO	Pull-up	
HDRST	Drive-low	Pull-up
BYPASS	Pull-up	High-impedance
$\overline{\text{TRST}}$, TCK	High-impedance	Pull-down
TRCLK	High-impedance	
$\overline{\text{BRKIN}}$, $\overline{\text{BRKOUT}}$, $\overline{\text{TESTMODE}}$	Pull-up	
NMI, $\overline{\text{PORST}}$	Pull-down	

Page 2-13

The long register name of register MMU_CON must be changed to "MMU **Configuration** Register".

Page 2-15

The bit description of bit CPU_SRCn.TOS is wrong. For TOS = 1, the description must be changed from "Reserved" to "Service Provider = PCP".

Page 2-17

In Table 2-4, the register long name for D11, D12, D13, D14 and D15 must be changed to "Data Register 1**1**, Data Register 1**2**, Data Register 1**3**, Data Register 1**4** and Data Register 1**5**.

Page 2-23

The offset address for register CMP1 must be corrected in Table 2-6 from 2200_H into 2280_H.

Page 2-26

Figure 2-11 should be replaced with the below figure:

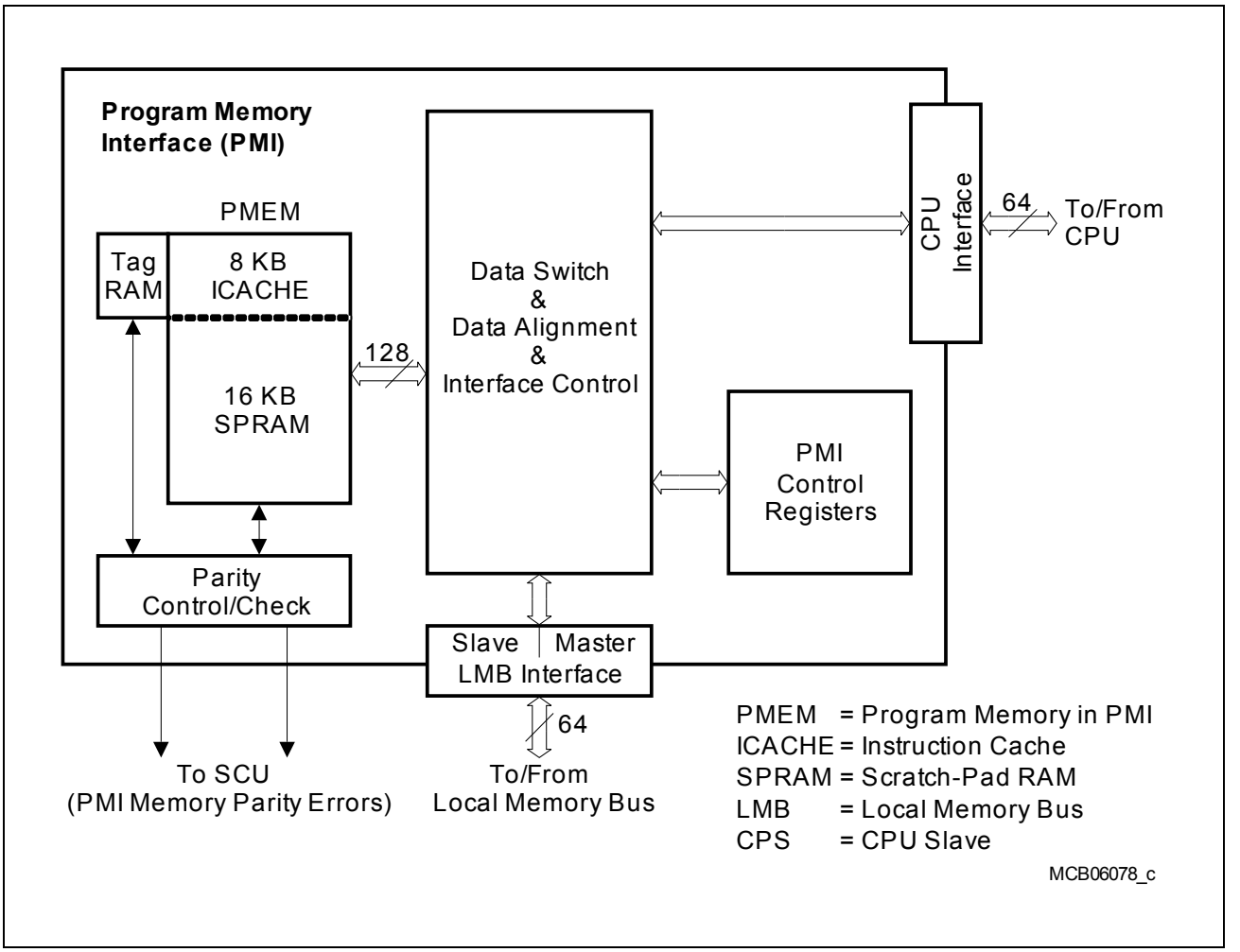

Figure 2-11 PMI Block Diagram

Page 3-18

Section 3.2.2.5: Point 3) of the actions should be executed after point 5) and not after point 2).

Page 4-25

The first sentence of Section 4.4.3 must be replaced by "Except for different connections to serial port lines of ASC0, the bootstrap loader mode 3 is identical to bootstrap loader mode **1**."

Page 4-26

The first sentence of the note at the top of the page must be extended by "For CRC generation and error checking, the BootROM software uses the TC1766 on-chip memory checker module with an initial value of FFFF $FFFF_H$ for the memory checker result register before the checksum is generated."

Page 5-18

The bit description of case "1" for EICR0.REN0 must be replaced by " The detection of a **rising edge** of IN0 generates a trigger event (INTF0 becomes set)."

Page 5-20

The bit description of case "1" for EICR0.REN1 must be replaced by " The detection of a **rising edge** of IN1 generates a trigger event (INTF1 becomes set)."

Page 5-21

The bit description of case "1" for EICR1.REN2 must be replaced by " The detection of a **rising edge** of IN2 generates a trigger event (INTF2 becomes set)."

Page 5-22

The bit description of case "1" for EICR1.REN3 must be replaced by " The detection of a **rising edge** of IN3 generates a trigger event (INTF3 becomes set)."

Page 5-28

The first sentence of the bit description of GEEN1 must be replaced by "Bit **GEEN1** enables the generation of a trigger event for output channel 1 when the result of the pattern detection changes."

Page 5-48

Figure 5-11 should be replaced with the figure shown as below.The below note must be added to the end of the last sentence of the page.

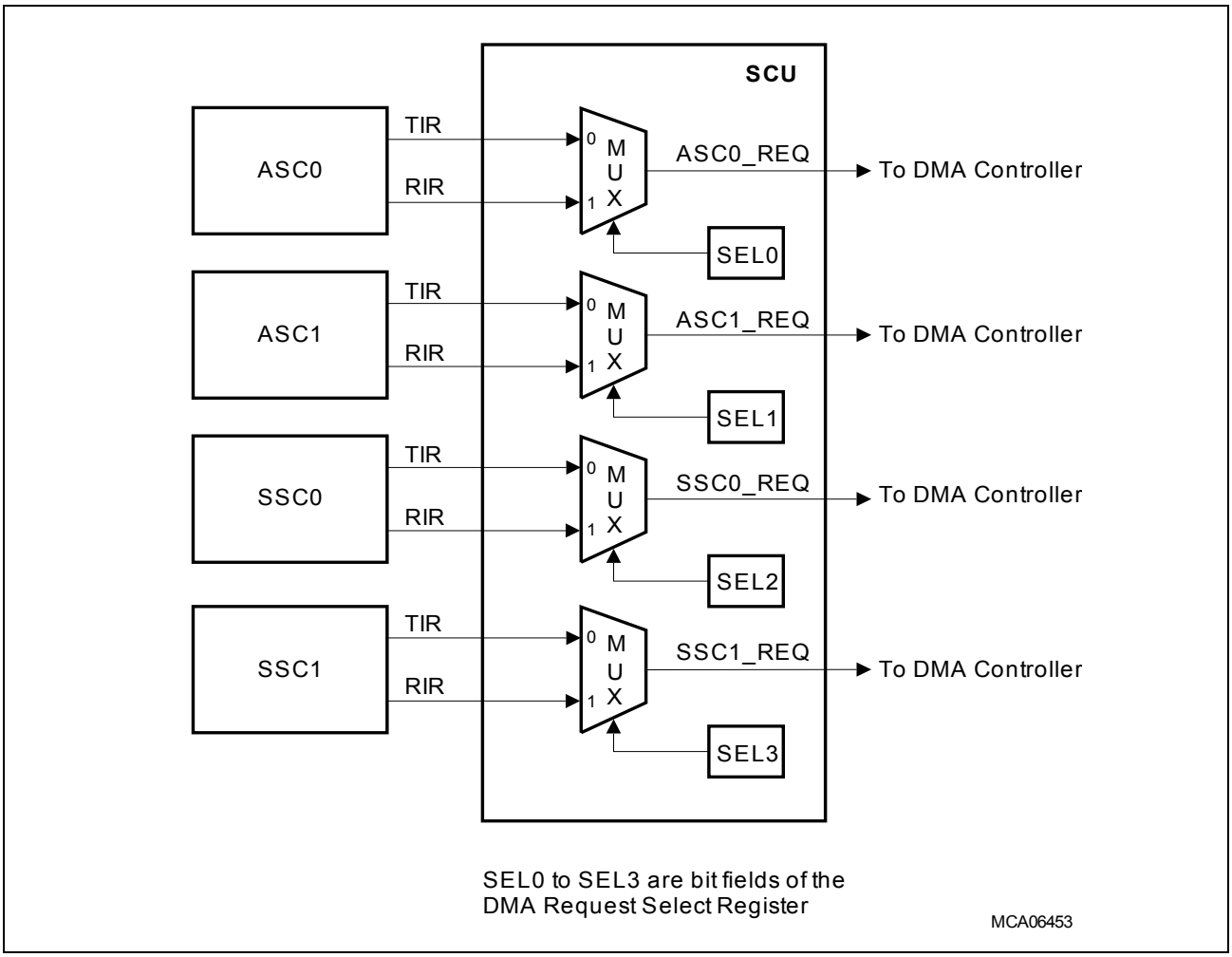

Figure 5-11 DMA Request Selection Logic

Note: By default, TIR line is selected for both ASC and SSC modules. For RIR line to be selected, SEL0.DMARS to SEL3.DMARS should be set accordingly. See DMARS register.

Page 5-58

The bit description of ENON on the bottom of the page must be corrected to:
"1 Setting of EMSF by hardware is **enabled**."

Page 5-64

The sentence "This bit is set with any reset." in the description of bit PARAV must be changed into "This bit is set after a power-on reset".

Page 6-4

Figure 6-2 should be replaced with the below figure:

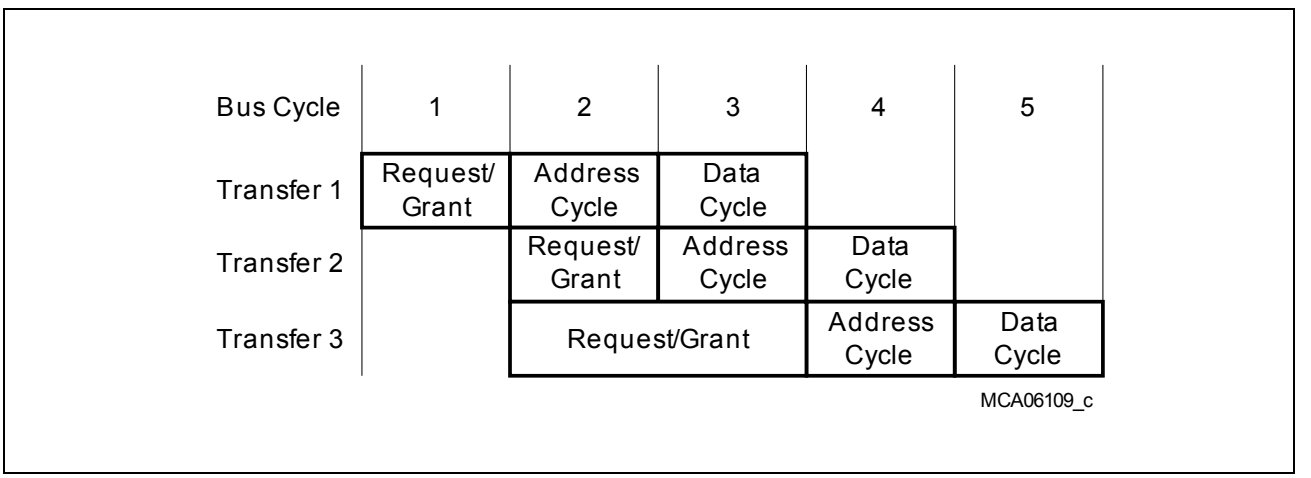

Figure 6-2 Basic LMB Transactions

Page 6-6

In the second paragraph of Section 6.2.3, second bulleted point, the register short name for LMB Error Data Registers should be replaced with "LEDATL/LEDATH".

Page 6-7

In the bit description of bit LEC, the text "When writing a 0 to LEC" must be replaced by "When writing a 1 to LEC".

Page 6-19

The second sentence of the first paragraph of Section 6.4.3 should be replaced with:

"The requesting FPI Bus master releases the FPI Bus for one cycle after the FPI Bus transaction request, in order to allow the **FPI** Bus slave to indicate if it is ready to handle the requested **FPI** Bus transaction."

Page 6-20

Figure 6-7 should be replaced with the below figure:

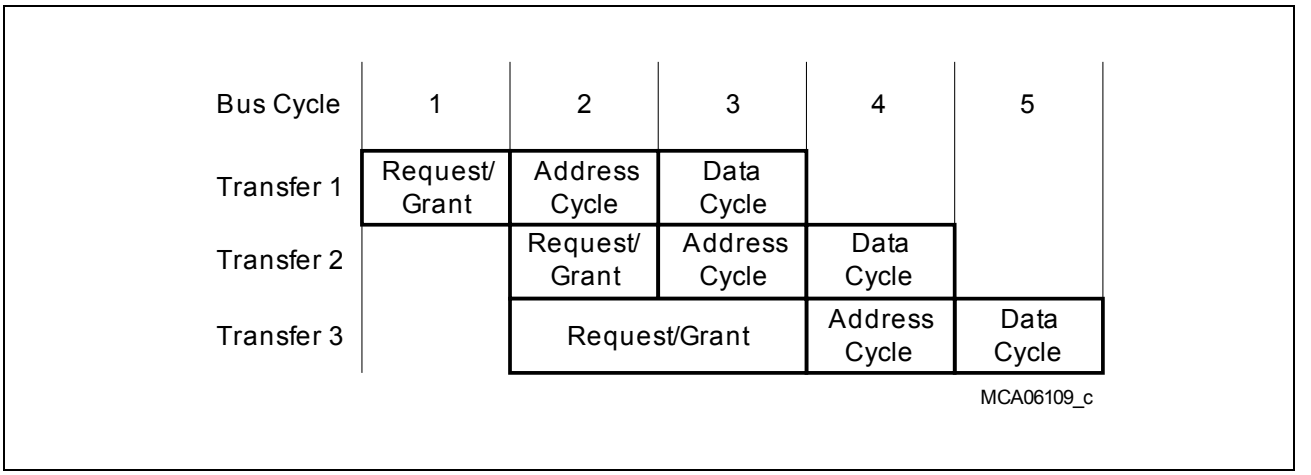

Figure 6-7 Basic FPI Bus Transactions

Page 6-29

Figure 6-12 should be replaced with the below figure:

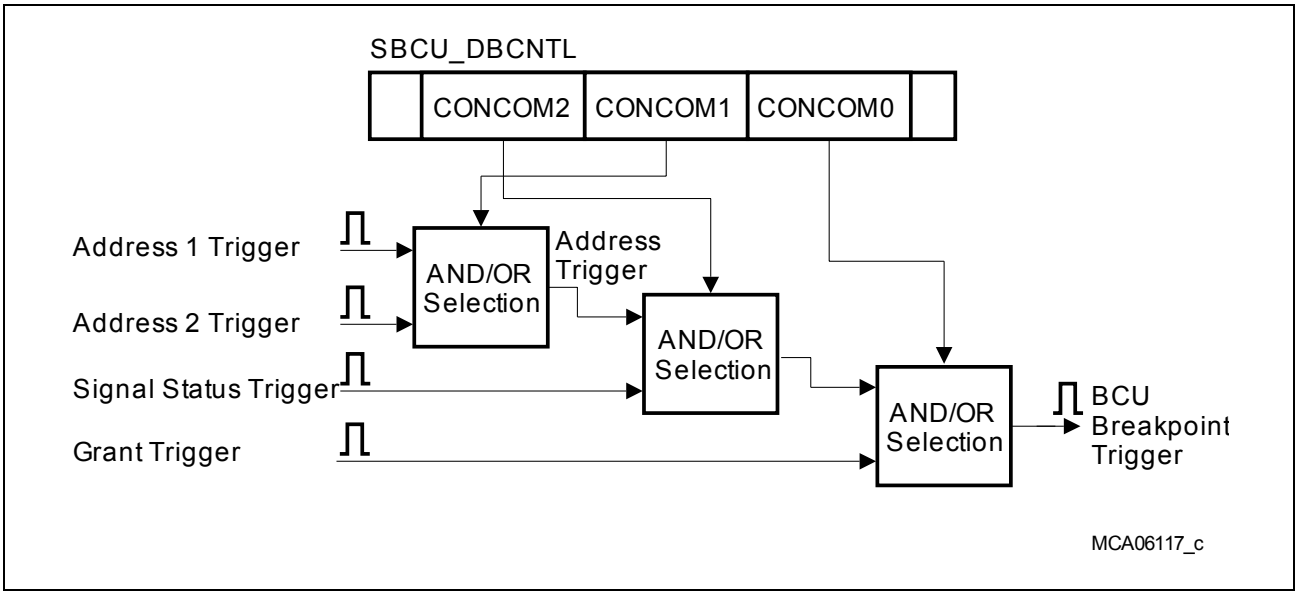

Figure 6-12 BCU Breakpoint Trigger Combination Logic

Page 7-16

In Table 7-7, 32-bit Load Page Buffer Command, the DFLASH address for DB1 AFE1 $55F4_H$ must be replaced with AFE1 $55F\mathbf{0}_H$ in Cycle 1 and DFLASH address for DB0 AFE0 $55F0_H$ must be replaced with AFE0 $55F\mathbf{4}_H$ in Cycle 2.

Page 7-41

The first paragraph of column "Description" for bit FABUSY should be changed as follows:
"This status flag is a flag for test purposes that should not be used by software drivers. It indicates whether any of the Flash arrays is in busy state. FABUSY is cleared by any reset operation."

Page 7-49 to 7-51

The following footnote [1] must be added to the following FCON bits and bit fields: WSPFLASH, WSECPF, WSWLHIT, WSDFLASH, and WSECDF

[1] These bits and bit fields can be changed at any time, also with code fetched from Program Flash. A modified wait state parameter will be taken into account with the next corresponding access.

Page 8-5 to 8-7 and 8-13 to 8-14

The respective address ranges (in bold) for Segment 8 and 10 of Table 8-2 and Table 8-4 must be updated as the following :

Table 8-2 SPB Address Map of Segment 0 to 14

Segment	Address Range	Size	Description	Access Type	
				Read	Write
8	**$8FE1\ 4000_H$ - $8FE1\ FFFF_H$**	48 Kbyte	Reserved	LMBBE & SPBBE	LMBBE
	$8FE2\ 0000_H$ - $8FF1\ FFFF_H$	1 Mbyte	Reserved	LMBBE & SPBBE	LMBBE
	$8FF2\ 0000_H$ - $8FF5\ FFFF_H$	256 Kbyte	Reserved for TC1766 emulation device memory		
	$8FF6\ 0000_H$ - $8FFF\ BFFF_H$	624 Kbyte	Reserved		
	$8FFF\ C000_H$ - $8FFF\ FFFF_H$	16 Kbyte	Boot ROM (BROM)	access	

Table 8-2 SPB Address Map of Segment 0 to 14 (cont'd)

Segment	Address Range	Size	Description	Access Type	
				Read	Write
10	**AFE1 4000$_H$ - AFE1 FFFF$_H$**	48 Kbyte	Reserved	LMBBE & SPBBE	ignore
	AFE2 0000$_H$ - AFF1 FFFF$_H$	1 Mbyte	Reserved	LMBBE & SPBBE	ignore
	AFF2 0000$_H$ - AFF5 FFFF$_H$	256 Kbyte	Reserved for TC1766 emulation device memory		
	AFF6 0000$_H$ - AFFF BFFF$_H$	624 Kbyte	Reserved		
	AFFF C000$_H$ - AFFF FFFF$_H$	16 Kbyte	Boot ROM (BROM)	access	

Table 8-4 LMB Address Map

Segment	Address Range	Size	Description	Action	
				Read	Write
8[1)]	**8FE1 4000$_H$ - 8FE1 FFFF$_H$**	48 Kbyte	Reserved	LMBBET	LMBBET
	8FE2 0000$_H$ - 8FF1 FFFF$_H$	1 Mbyte	Reserved	LMBBET	LMBBET
	8FF2 0000$_H$ - 8FF5 FFFF$_H$	256 Kbyte	Reserved for TC1766 emulation device memory		
	8FF6 0000$_H$ - 8FFF BFFF$_H$	624 Kbyte	Reserved		
	8FFF C000$_H$ - 8FFF FFFF$_H$	16 Kbyte	Boot ROM (BROM)	access	

Table 8-4 LMB Address Map (cont'd)

Seg-ment	Address Range	Size	Description	Action	
				Read	Write
10[2)]	**AFE1 4000$_H$ - AFE1 FFFF$_H$**	48 Kbyte	Reserved	LMBBET	LMBBET
	AFE2 0000$_H$ - AFF1 FFFF$_H$	1 Mbyte	Reserved	LMBBET	LMBBET
	AFF2 0000$_H$ - AFF5 FFFF$_H$	256 Kbyte	Reserved for TC1766 emulation device memory		
	AFF6 0000$_H$ - AFFF BFFF$_H$	624 Kbyte	Reserved		
	AFFF C000$_H$ - AFFF FFFF$_H$	16 Kbyte	Boot ROM (BROM)	access	

1) Cached area

2) Non-cached area

Page 8-17

In Table 8-5, the four "–" of Double-word column and CRAM and PRAM rows must be replaced by "✔". "CRAM" must be replaced with "CMEM". Footnote 1 must be added to the PMI and DMI memory cells as "The module also supports LMB 2-Word and 4-Word Block read and write accesses".Footnote 2 must be added to the PCP memory cell as "The module also supports FPI 4-Word and 8-Word Block read and write accesses".

Page 9-15

The following sentence must be added at the end of paragraph "Port 0 is a general-purpose 16-bit ... software later.":

"Note that some of the P0.[7:0] lines are used for configuration purposes, too (see Page 9-25)."

Page 9-25

Section 9.3.3.3 must be changed as described below:

9.3.3.3 Reserved Port 0 Pins

Depending on the TC1766 device version used in an application, several Port 0 lines (meaning several SWOPT bits) are reserved and cannot be used for user system purposes during a HDRST reset operation. **Table 9-8** defines the reserved Port 0 lines (indicated by 0 or 1) as well as the Port 0 lines that can be used by a user program

(indicated by "user") for software configuration selection (or as GPIO pins) depending on the specific TC1766 device version.

Table 9-8 Reserved Port 0 Lines of TC1766 Devices

TC1766 Device Versions	SWOPTx Bits (x = 0-15)					
	P0. [15:8]	P0. [7:6]	P0.5	P0.4	P0.3	P0. [2:0]
TC1766	user	user	user	1	user	1)
TC1766ED (Emulation device)		XX_B 2)	0 or 1 3)			

1) The P0.[2:0] bits are only used in alternate boot modes (see Table 4-7). If alternate boot modes are not required or used in an application, P0.[2:0] can also be used for user program software configuration selection purposes during a hardware reset operation or as GPIO pins.

2) 00_B, 11_B : The USB interface of the TC1766ED is not connected to device pins.
01_B : The USB interface of the TC1766ED is connected to JTAG I/O lines.
10_B : The USB interface of the TC1766ED is connected to P2.[5:0] lines.

3) 0: Emulation device functionality is not available.
1: Emulation device functionality is fully supported.

Page 9-32

The reset value for P1_IOCR12 should be corrected as **0**020 2020_H.

Page 9-41

P2_IOCR0 should not be linked to footnote 1.

Page 9-42

The reset value for P2_IOCR12 should be corrected as **0**0**0**0 2020_H.

Page 9-49 to 9-50

In Table 9-13, P3.12 and P3.14 Input rows should be updated as below:

Table 9-13 Port 3 Functions

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P3.12	I	General-purpose input	P3_IN.P12	P3_IOCR12. PC12	$0XXX_B$
		CAN node 0 receive input 0 CAN node 1 receive input 1	RXDCAN0		
		ASC0 input (Asynchronous Mode /Synchronous Mode)	RXD0B		
	O	General-purpose output	P3_OUT.P12		$1X00_B$
		ASC0 output (Synchronous Mode)[1)]	RXD0B		$1X01_B$
		ASC0 output (Synchronous Mode)	RXD0B		$1X10_B$
		Reserved[1)]	–		$1X11_B$
P3.14	I	General-purpose input	P3_IN.P14	P3_IOCR12. PC14	$0XXX_B$
		CAN node 1 receive input 0 CAN node 0 receive input 1	RXDCAN1		
		ASC1 output (Asynchronous Mode/Synchronous Mode)	RXD1B		
	O	General-purpose output	P3_OUT.P14		$1X00_B$
		ASC1 output (Synchronous Mode)[1)]	RXD1B		$RXD0_B$
		ASC1 output (Synchronous Mode)	RXD1B		$RXD0_B$
		Reserved[1)]	–		–

1) The ALT1 and ALT2 for this pin are connected together. There are no dependencies. Either one can be chosen.

In Table 9-13, the text of the associated Reg. I/0 Line **TCD0B** of P3.13 with P3_IOCR12.PC13 = $1X10_B$ must be changed to **TXD0B**.

Page 9-55

In Table 9-15, the text of Pin Functionality **SCU input** of Pin 4.3 with P4_IOCR0.PC3 = $1X11_B$ must be replaced with **SCU output**. In Table 9-16, P4_IOCR0 should not be linked to footnote 1.

Page 9-57

Section 9.7.3.3 should be updated as below:

9.7.3.3 Port 4 Input/Output Control Register x (x=4, 8 and 12)

Port lines P4.[15:4] are not available. Therefore, PC bit fields; PC[15:4] in registers P4_IOCR4, P4_IOCR8, P4_IOCR12 are not connected.

Page 10-58

Bit 5 in the register image of register PCP_ES must be changed into 0,r (instead of ME,rh).

Page 10-59

The column "Description " for bit 5 must be corrected into: "Reserved; read as 0.

Page 10-73

The second row (RC0) of Table 10-12 must be replaced by the following row:

CNT0		**Counter Reload Value (COPY)** The COPY instruction uses an implicit counter to generate multiple data transfers. The CNT0 value given in the instruction specifies how many data transfers are to be performed by the instruction. See also **Figure 10-13** on **Page 10-73**.
	CNT0 = $001_B..111_B$	Perform 1..7 data transfers
	CNT0 = 000_B	Perform 8 data transfers
		Block Size (BCOPY) Selects the FPI block size used for a BCOPY instruction.
	CNT0 = 000_B	Use block size of 8 words.
	CNT0 = 010_B	Use block size of 2 words.
	CNT0 = 011_B	Use block size of 4 words.
	Others	Reserved

Page 10-77

Figure 10-14 must be replaced by the following figure (block "DATA Transfer" has been changed):

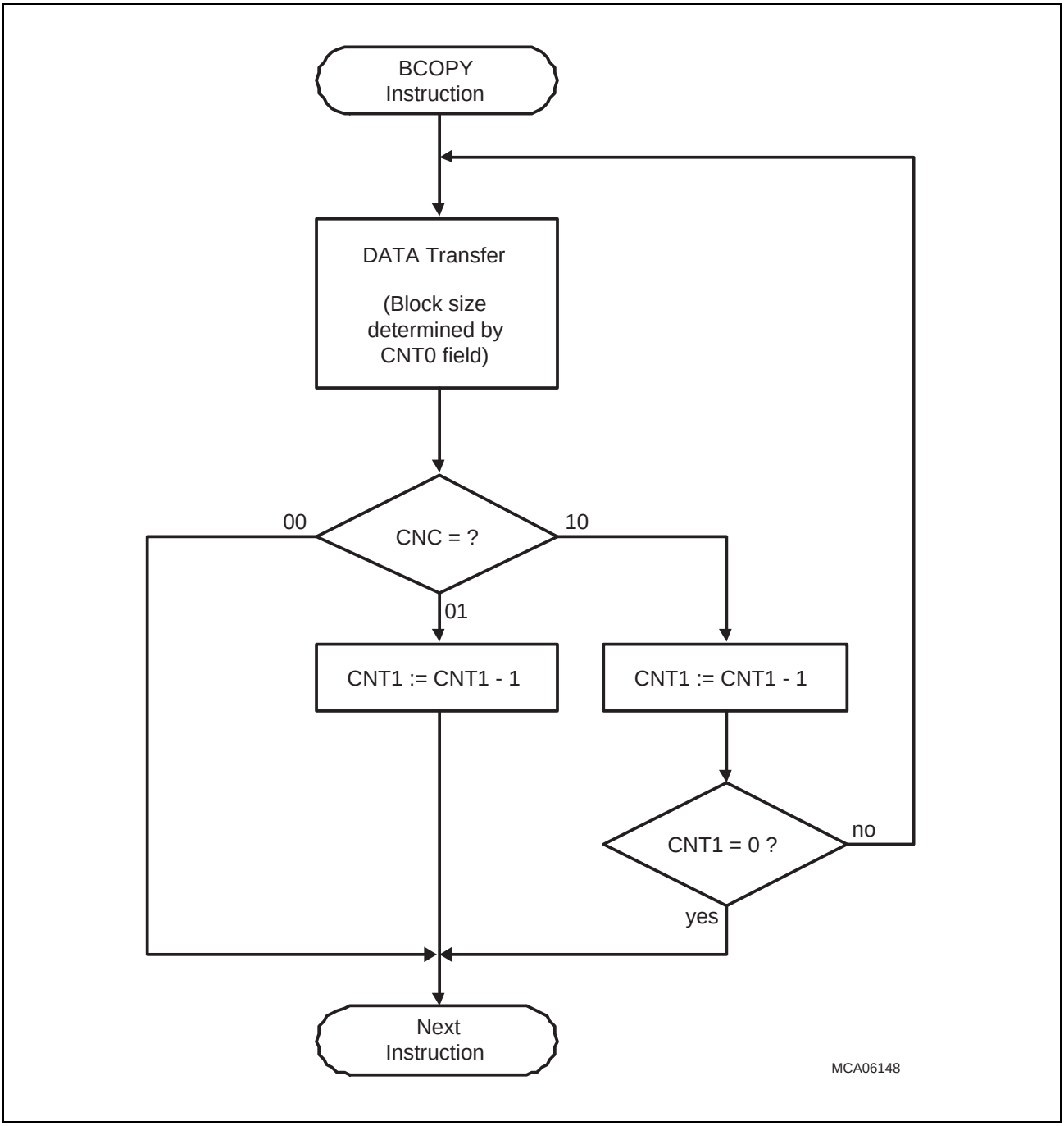

Figure 10-14 Counter Operation for BCOPY Instruction

Page 10-98

In the syntax description of the ST.PI instruction of the PCP, the register name "Ra" should be replaced by "Rb".

Page 11-9

The wordings "SHADR0n with CHCR0n.SHCT = 01_B"on the left of the first waveform from the bottom of Figure 11-5 must be replaced with "SHADR0n with ADRCR0n.SHCT = 01_B".

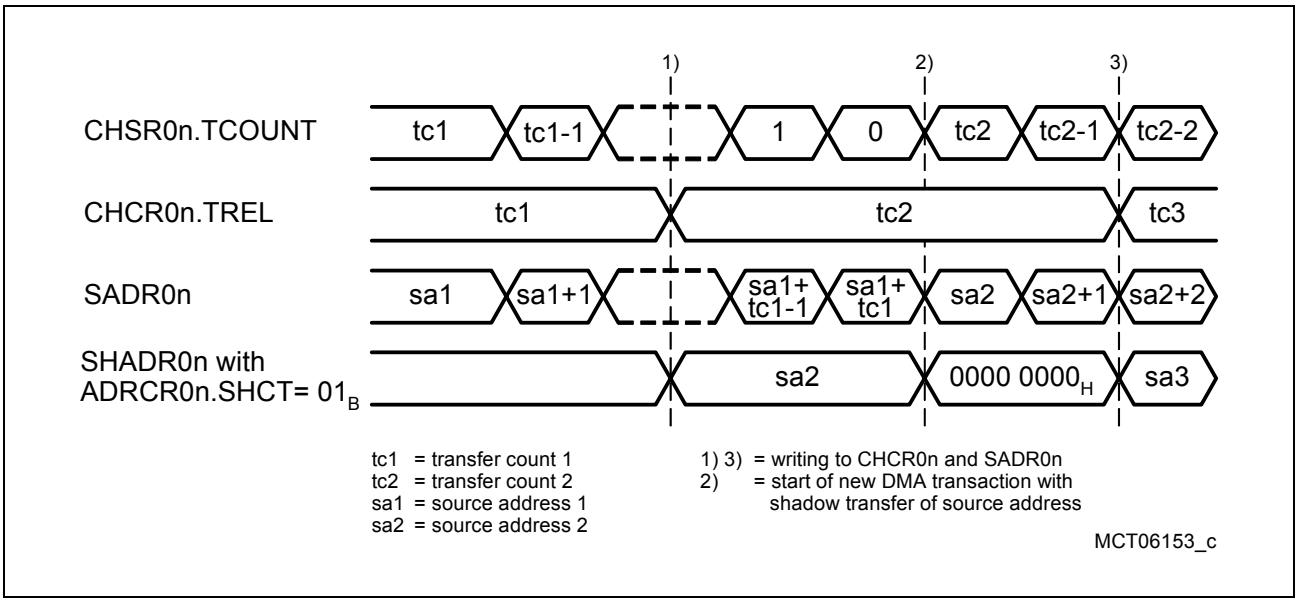

Figure 11-5 Shadow Source Address and Transfer Count Update

Page 11-10

Figure 11-6 must be updated as per the corresponding changes on pages 11-35 and 11-50.

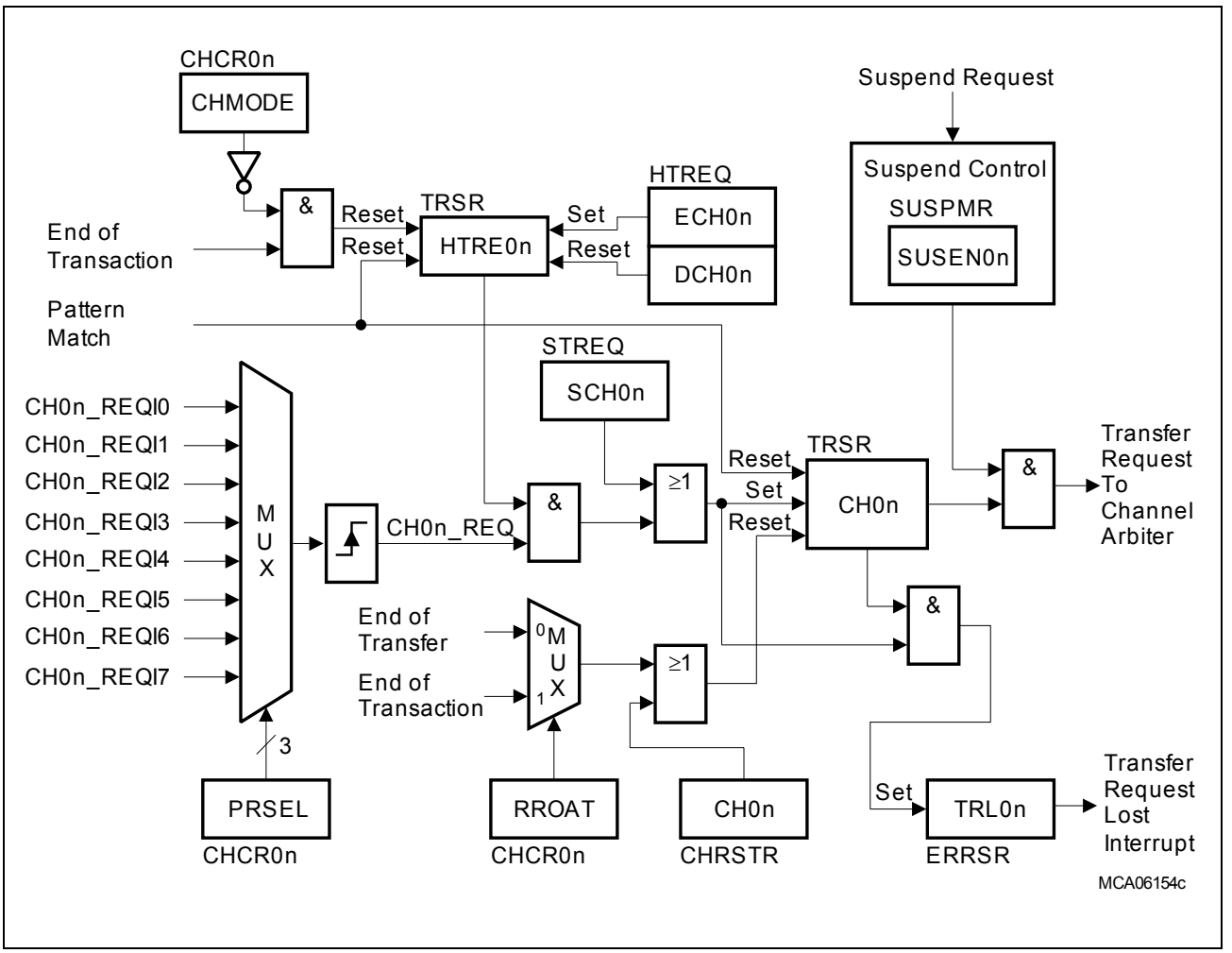

Figure 11-6 Channel Request Control

The last sentence of the second last paragraph should be replaced with:

"A software request can be generated by setting bit **STREQ.SCH0n**."

Page 11-16

The paragraphs below "When CHRST.CH0n is set to 1:" must be replaced by the following paragraphs:

- Bits TRSR.HTRE0n, TRSR.CH0n, ERRSR.TRL0n, INTSR.ICH0n, INTSR.IPM0n, WRPSR.WRPD0n, WRPSR.WRPS0n, CHSR0n.LXO, and bit field CHSR0n.TCOUNT are reset.
- Source and destination address register will be set to the wrap boundary. SHADR0n will be cleared.
- All automatic functions are stopped for channel 0n.

A user program must execute the following steps for resetting a DMA channel:

1. If hardware requests are enabled for the DMA channel 0n, disable the DMA channel 0n hardware requests by setting HTREQ.ECH0n = 0.
2. Writing a 1 to CHRST.CH0n.
3. Waiting (polling) until CHRST.CH0n = 0.

A user program should execute the following steps for restarting a DMA channel after it was reset:

1. Optionally (re-)configuring the address and other channel registers.
2. Restarting the DMA channel 0n by setting HTREQ.ECH0n = 1 for hardware requests or STREQ.SCH0n = 1 for software requests.

The value of CHCR0n.TREL is copied to CHSR0n.TCOUNT when a new DMA transaction is requested and shadow address register contents is not equal 00000000_H.

Page 11-29

In Section 11.1.8.2, the register name EERSR must be replaced by ERRSR in the third sentence of the first paragraph, first sentence of the second paragraph and within Figure 11-18. The corresponding text must be replaced by :
"If such a transaction request lost condition occurs, bit E**R**RSR.TRL0n is set." and "A transaction request lost condition of DMA channel 0n is indicated by status flag E**R**RSR.TRL0n, which can be reset by setting bit CLRE.CTL0n or CHRSTR.CH0n."

Figure 11-18 must be replaced by:

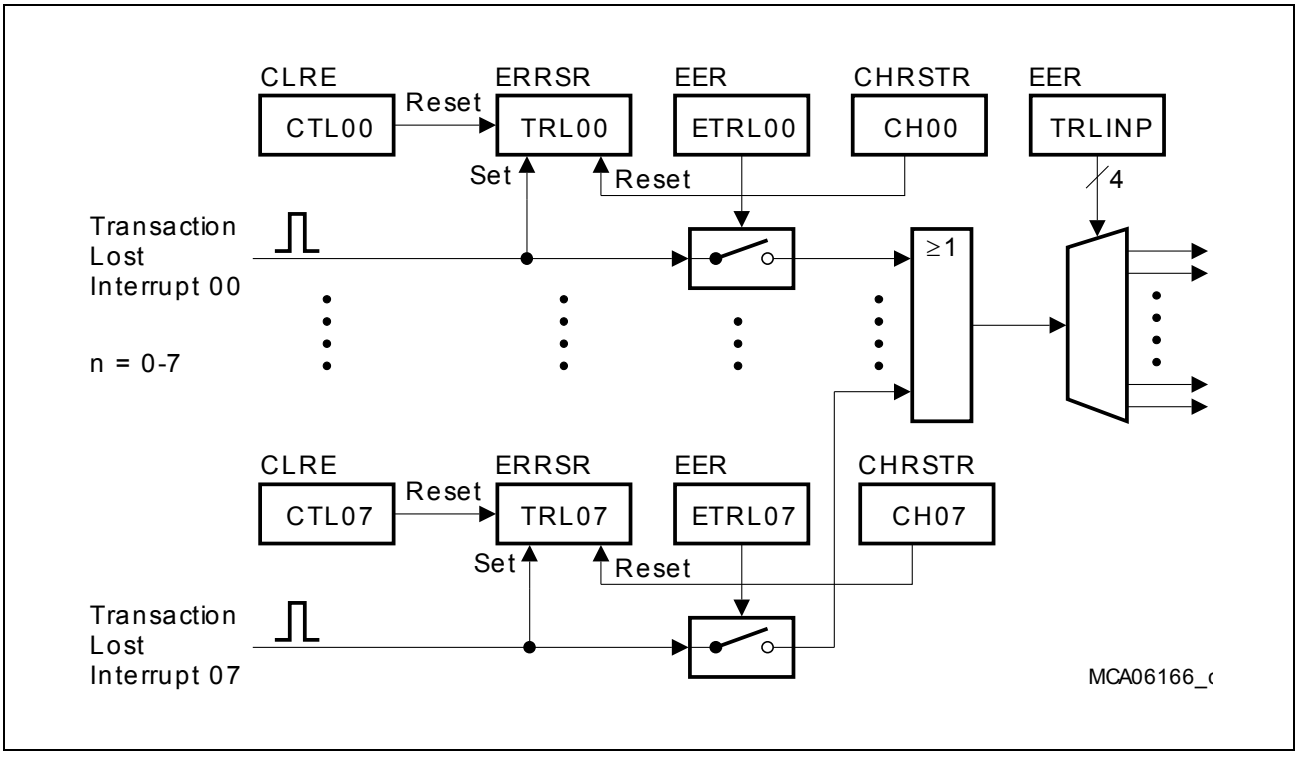

Figure 11-18 Transaction Lost Interrupt

Page 11-30

In Section 11.1.8.3, the register name EERSR must be replaced by ERRSR in the first sentence of the third paragraph and within Figure 11-19. The corresponding text must be replaced by :
"A source error of Move Engine 0 is indicated by the status flag E**R**RSR.ME0SER."

Figure 11-19 must be replaced by:

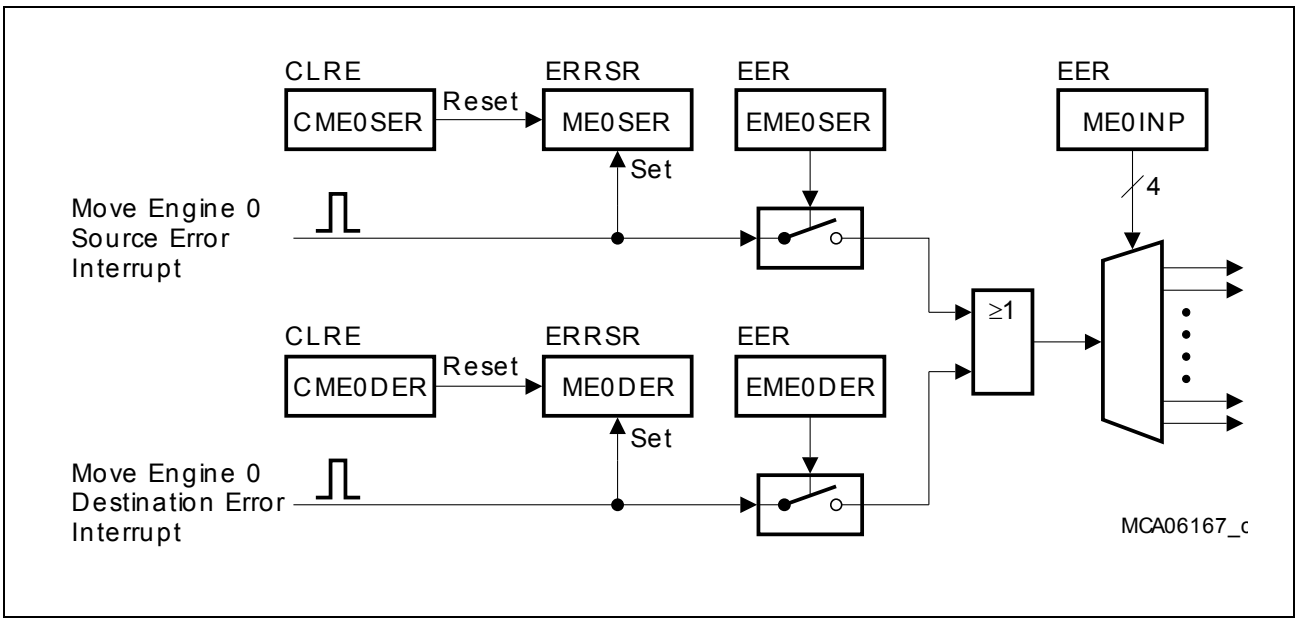

Figure 11-19 Move Engine Interrupts

Page 11-35

The following paragraphs should be added after the last paragraph("..for a specific value of CHDW") under Section 11.1.9 Pattern Detection:

Depending on CHCR0n.PATSEL and on the positive result of the comparison, two actions follow (if CHCR0n.PATSEL=00, no action will be taken when a pattern match is detected, so the wrap interrupt can be used):

- The activation of the interrupt corresponding to the current active channel 0n using the Interrupt Pointer defined in CHICR0n.WRPP.
- Reset TRSR.HTRE0n and TRSR.CH0n in order to stop the current transaction (Hardware and Software request enable). The value of CHSR0n.TCOUNT can be read out by the interrupt SW.

The software will have to service the interrupt and to activate again the channel.

Page 11-50

The description of bit field CH0n must be extended by the following sentence:
"CH0n is reset when a pattern match is detected".

The description of bit field HTRE0n must be extended by the following sentence:
"HTRE0n is reset when a pattern match is detected".

Page 11-79

The second sentence of the last paragraph should be replaced with:

"If DMA channel 0n is active when writing to SADR0n, the source address will not be written into SADR0n directly but will be buffered in the shadow register **SHADR0n** until the start of the next DMA transaction.

Page 11-80

The second sentence of the last paragraph should be replaced with:

"If DMA channel 0n is active when writing to DADR0n, the source address will not be written into DADR0n directly but will be buffered in the shadow register **SHADR0n** until the start of the next DMA transaction.

Page 11-91

Figure 11-29 must be corrected as below:

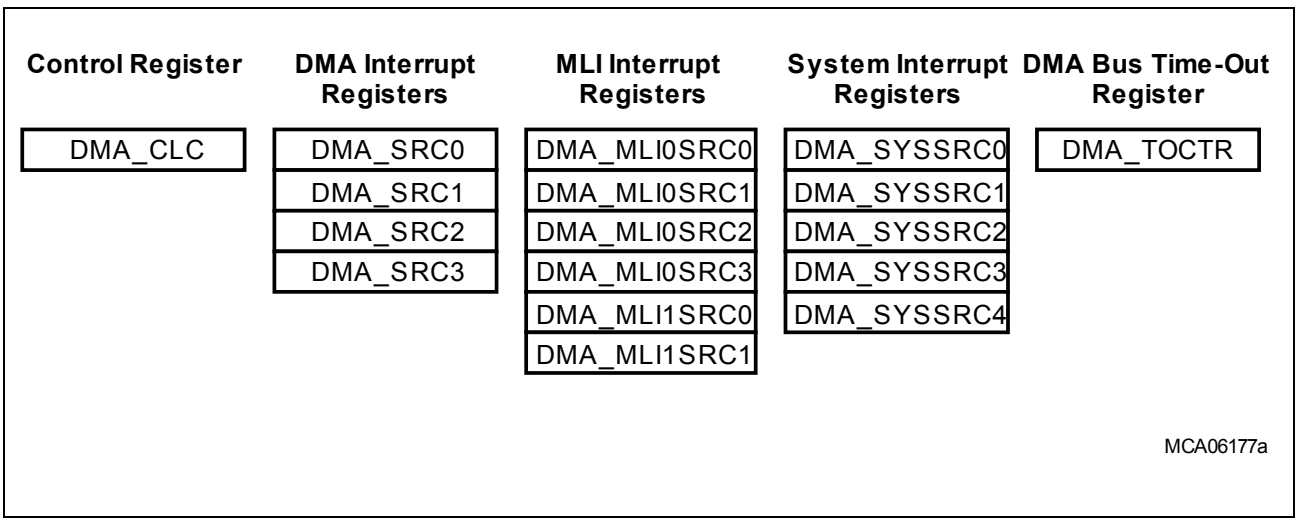

Figure 11-29 DMA Implementation-specific Registers

Page 12-26

Figure 12-5 must be updated with the following corrected drawing.

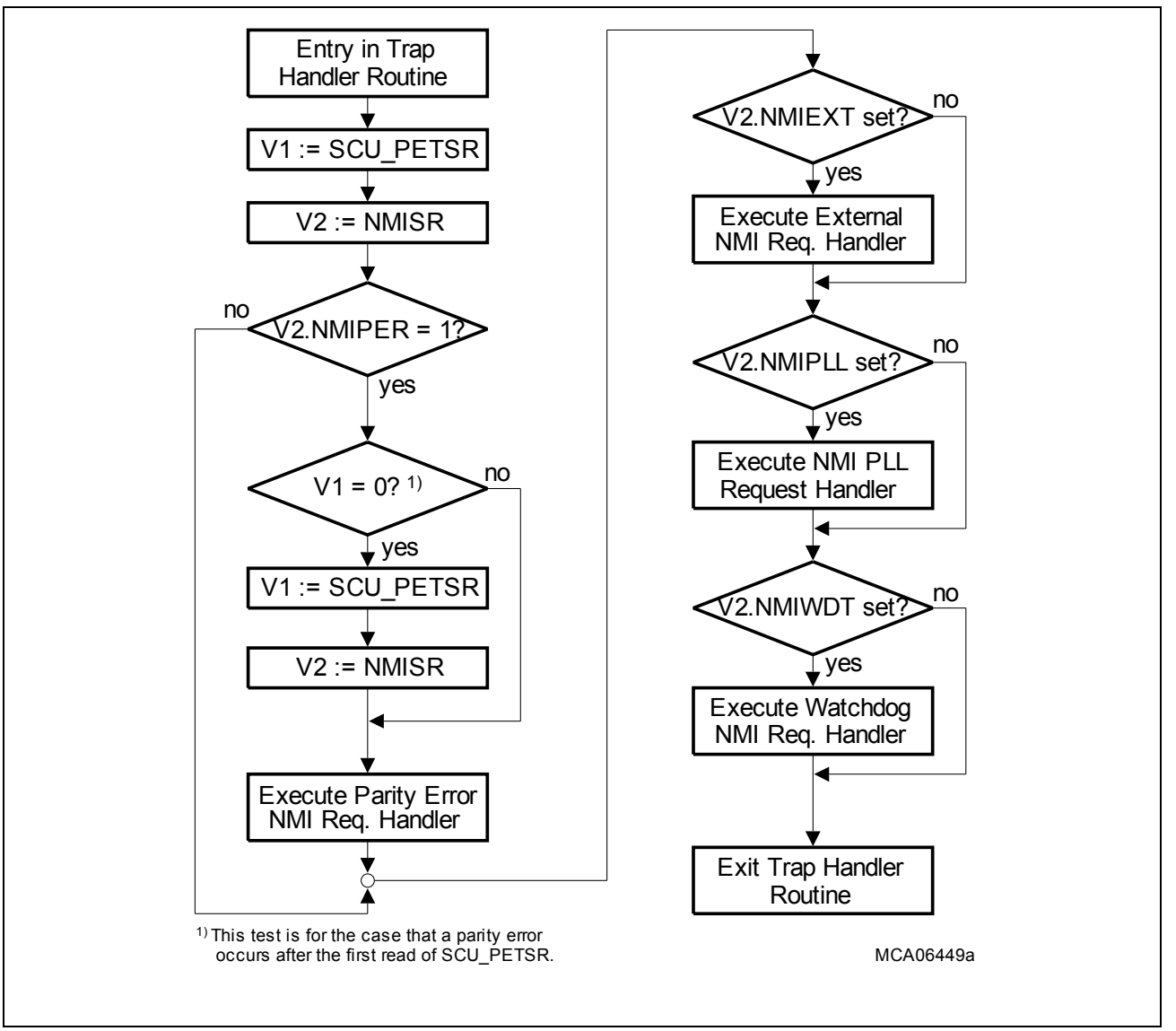

Figure 12-5 NMI Trap Handler Routine for Parity Error Handling

Page 14-4

The below note must be added to the end of the last sentence of the page.

Note: The resetting of the ENDINIT bit takes some time. Accesses to Endinit-protected registers after the resetting of the ENDINT bit must only be done when ENDINIT is really reset. As a solution, WDT_CON0 (the register with the ENDINIT bit) should be read back once before Endinit-protected registers are accessed the first time after ENDINIT has been reset.

Page 16-15

The read and write access modes for address location F000 0804_H of Table 16-7 must be changed from "nBE" to "BE".

Page 16-16

The "Reserved" column for address location F000 0850_H to F000 $08F4_H$ of Table 16-7 must be separated to two different rows of access rights. The read and write access rights for F000 0850_H -F000 0854_H are both "nBE" and F000 0858_H -F000 $08F4_H$ are both "BE".

Page 16-20 to 16-25

The write accesses for all Px_OMR registers (x = 0-5) are corrected from "U,SV" into "U,SV,32".

Page 16-69

The long name of register MMU_CON must be changed to "MMU **Configuration** Register".

Page 16-79

The contents for the short name, description and reset value columns for Table 16-26 at address locations F800 $05F0_H$, F800 $05F8_H$, and F800 $05FC_H$ must be replaced as shown in **Table 16-26**.

Table 16-26 Address Map of PMU

Short Name	Description	Address	Access Mode		Reset Value[1]
			Read	Write	
Program Memory Unit (PMU)					
–	Reserved[2]	F800 $05F0_H$	U, SV	E, U, SV	–
–	Reserved	F800 $05F4_H$	BE	BE	–
–	Reserved[2]	F800 $05F8_H$	BE	E, U, SV, 32	–
–	Reserved[2]	F800 $05FC_H$	U, SV	BE	–

1) Which Resets affect the register, see Table 4-2.

2) Do not read from or write to these address locations.

3 User's Manual - Peripheral Units Part (Volume 2)

This section describes corrections for the Peripheral Units part of the User's Manual.

Page 17-28

Figure 17-12 should be updated with the below figure:

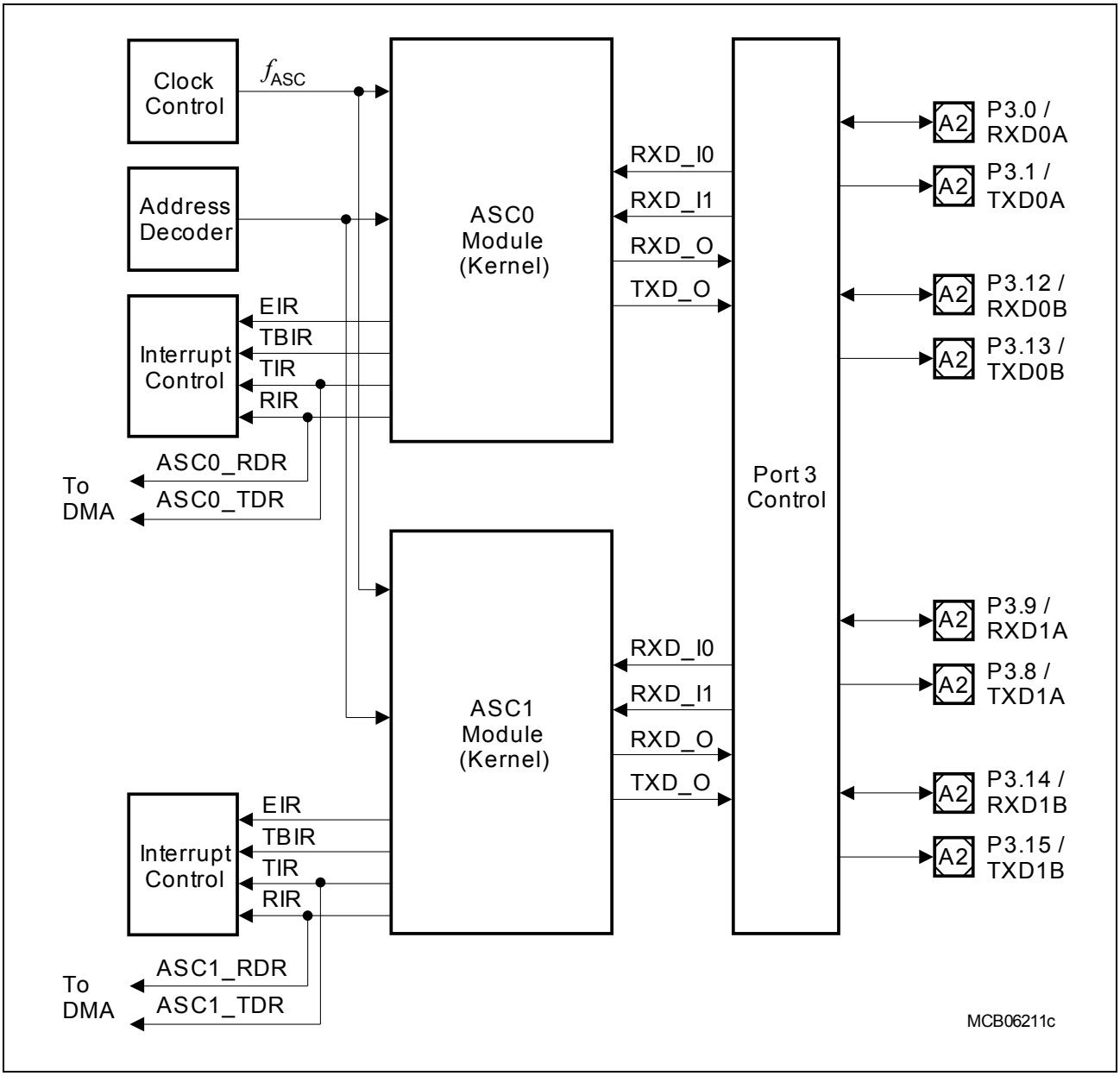

Figure 17-12 ASC0/ASC1 Module Implementation and Interconnections

Page 18-15

In Figure 18-8, the description at the bottom of the figure, "CON.PH = CON.PO = 1" must be replaced by "CON.PH = 0; CON.PO = 1".

Page 18-16

After the first sentence on the top of this page, the following sentence must be added: "With a TB write operation, all timing parameters stored in register SSOTC as well as the SSOC register are latched and remain valid for the consecutive transmission."

In the first line of the paragraph below "Slave Select Output Control", the text "SSOC.OENn = 0" must be replaced by "SSOC.OENn = 1".

Page 18-17

In the first line below heading "Slave Select Register Update", the text in brackets "with the activation of SLSOn" must be replaced by the text "with the TB register write operation".

Page 18-18

Figure 18-11 should be updated with the below figure:

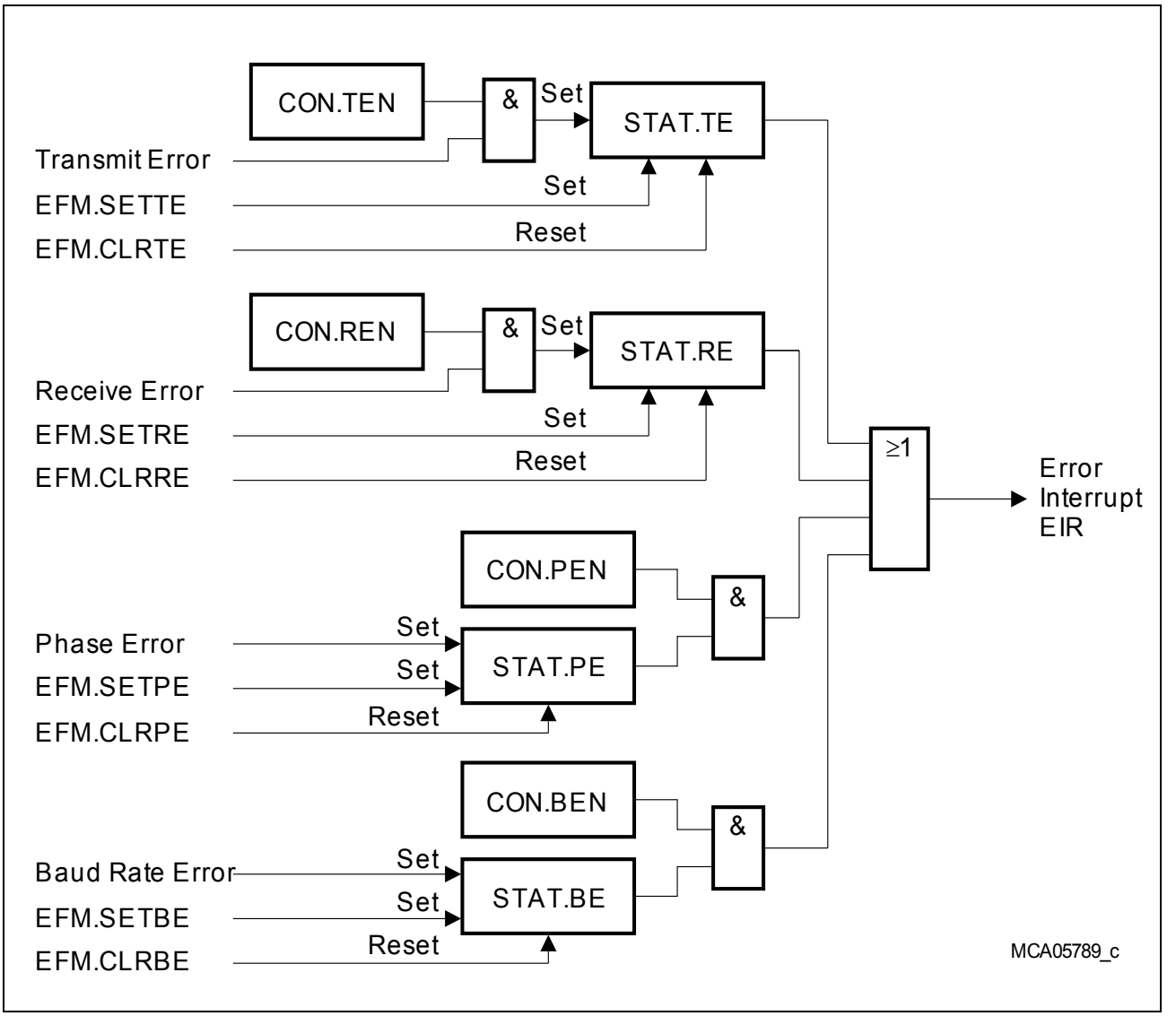

Figure 18-11 SSC Error Interrupt Control

Page 18-19

In the first note which is located at the upper part of the page, the text "CON.REN = 1" must be replaced by "CON.AREN = 1".

Page 18-19

The following note must be inserted after the first note of the page:

Note: This error can occur after any transfer if the communication is stopped. This is due to the fact that SSC supports back-to-back transfers for multiple transfers. In order to handle this, the baud rate detection logic expects a next clock cycle immediately for a new transfer after a finished transfer.

Page 18-23

In the STIP bit description, the sentence "This bit determines..." must be replaced by the following sentence:

"This bit determines the logic level of the Slave Mode transmit signal when the SSC slave select input signals are inactive (PISEL.SLSIS $\neq 000_B$)."

Page 18-25

The bit description of bit EN must be extended by the following sentence: "Note that EN should only be reset by software while no transfer is in progress (STAT.BSY = 0)".

Page 18-29

The note paragraph at the bottom of the page must be replaced by the following note paragraph:

Note: The SSOC register content is latched by each TB register write operation and remains latched during the consecutive serial transmission.

Page 18-30

In the bit description of register SSOTC a footnote [1)] must be added to the bit combinations 00_B of bit fields LEAD, TRAIL, and INACT:

"[1)] For getting a best case timing with no timing delays (see Figure 18-8), this bit field value should be set when the SLSOn outputs are disabled (SSOC.OENn bits set to 0)."

Page 18-30

The note paragraph after the SSOTC register description table must be replaced by the following note paragraph:

Note: The SSOTC register timing parameters are latched by each TB register write operation and remain latched during a consecutive serial transmission.

Page 19-20

The following sentence should be added at the end of the Section 19.1.2.6 “Note that in this case no time frame finished interrupt is generated any more.“.

Page 19-42

Description of bit field NDBH: for bit combination NDBH = 00000_B, the text “No SRH bit shifted“ should be replaced by “No SRH bit shifted; no selection bit is generated, the SRH active phase is completely skipped.“.

Page 20-49

The following paragraph should be added after the last paragraph:

"In order to avoid direct reception of a message by a slave message object, as if it was an independent message object and not a part of a FIFO, the bit RXEN of each slave object must be cleared. The setting of the bit RXEN is “don't care” only if the slave object is located in a list not assigned to a CAN node."

Page 20-50

The first paragraph should be extended by a second sentence:

"A transmit FIFO consists of one base message object and one or more slave message objects."

Page 20-54

Table 20-4: The offset addresses of the four registers must be corrected as follows:

MSIMASK = $01C0_H$
PANCTR = $01C4_H$
MCR = $01C8_H$
MITR = $01CC_H$

Page 20-75

In Table 20-6, the two sentences in column “Signification” for LEC value 111B at the bottom of the page must be replaced by the following two sentences:

"Whenever the CPU writes the value 111B to LEC, it takes the value 111B. Whenever the CPU writes another value to LEC, the written LEC value is ignored."

Page 20-85

In the first row of Table 20-8, column “CAN Bus State”, the wording “reserved bits, “ must be deleted. In the second row of Table 20-8, column “CAN Bus State”, the wording “reserved bits, “ must be inserted at: “ .....RTR, reserved bits, IDE, ...”.

Page 20-109

The paragraph after Equation (20-2) must be replaced by the following:**Equation (20-1)** applies to normal divider mode (CAN_FDR.DM = 01_B) of the fractional divider. **Equation (20-2)** applies to fractional divider mode (CAN_FDR.DM = 10_B).

Page 20-116

The first sentence of the second paragraph must be replaced by: "Each of the 136 hardware initiated interrupt sources is controlled by a 4-bit interrupt pointer that directs the interrupt source to one of the **six** interrupt outputs INT_Om (m = 0-**5**)."

Page 20-117

Figure 20-27 should be updated with the below figure:

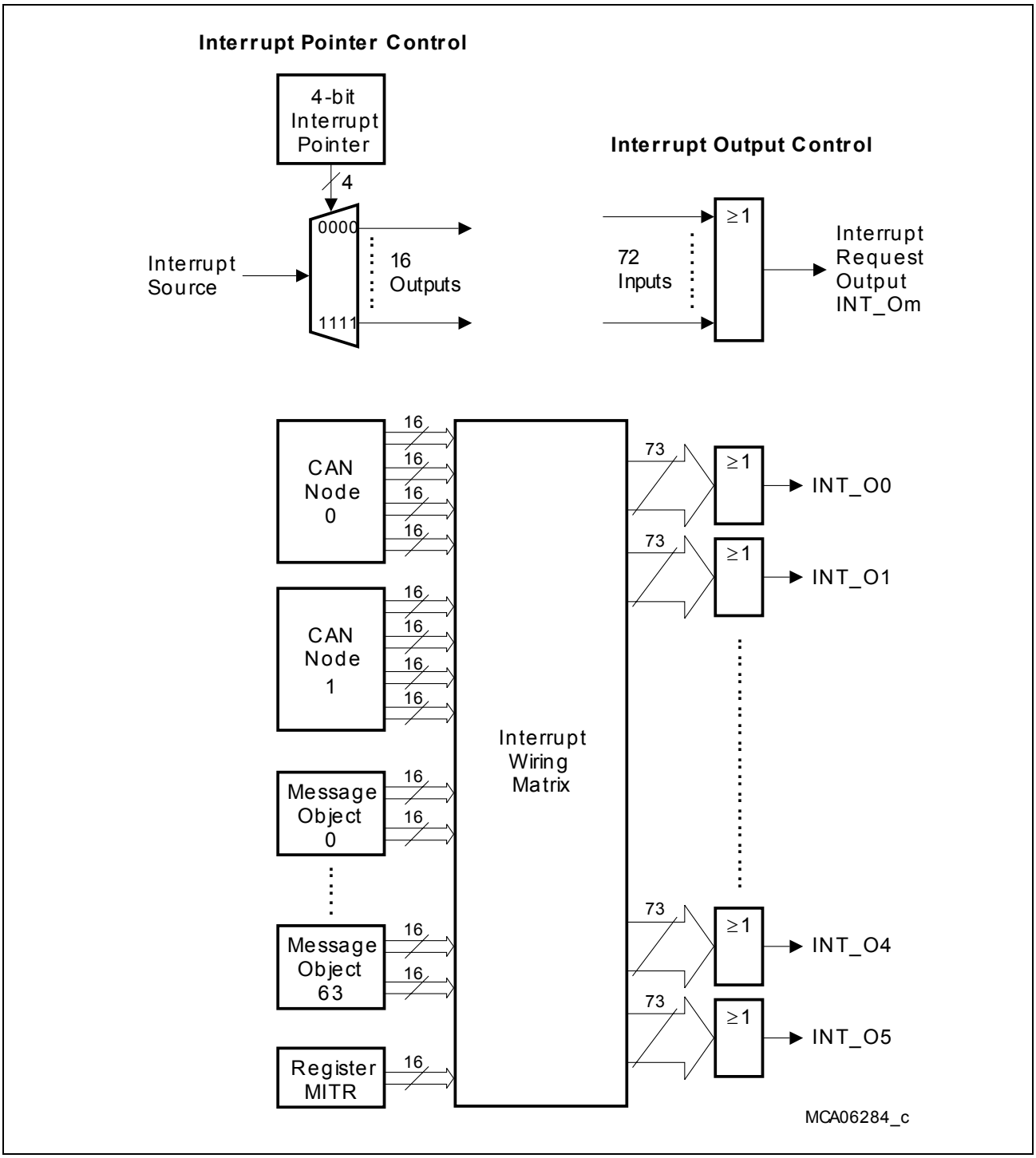

Figure 20-27 Interrupt Compressor

Page 20-118

The first sentence of the page must be replaced by: "Each of the **six** interrupt outputs INT_Om of the MultiCAN module is controlled by its service request control registers."

Page 21-2

The bullet paragraph "Programmable baud rate: ....." under "Features" must be changed as follows:

- Programmable baud rates
  - MLI transmitter baud rate: max. $f_{MLI}/2$ (= 40.0 Mbit/s @ 80 MHz module clock)
  - MLI receiver baud rate: max. f_{MLI}

Page 21-30

The following sentence must be added at the end of section "21.1.5 MLI Receiver Operation":

"The MLI receiver is able to operate with a maximum receive clock (RCLK) frequency up to the frequency of the module clock f_{MLI}.

Page 21-79

In the register table of register RPxBAR the row for bits [3:0] should be deleted. The range for ADDR bit field must be extended to [31:0].

Page 21-108

The following paragraph with the formula must be added after the last paragraph:

The receiver baud rate is defined by the following formula.

$$\text{Baud rate}_{RCLKmax} = f_{MLI} \quad (21.4)$$

Page 21-116

In the register table, P5_IOCR8 and P5_IOCR12 should be updated as below:

Field	Bits	Type	Description
PC8, **PC9,** **PC10,** **PC11**	[7:4], [15:12], [23:20], [31:28]	rw	**Port Input/Output Control for Port 5.[11:8]** [1)] Port input/output control for P5.8/RDATA0B/TDATA1 Port input/output control for P5.9/RVALID0B/TVALID1 Port input/output control for P5.10/RREADY0B/TREADY1 Port input/output control for P5.11/RCLK0B/TCLK1

1) For coding of bit field, see Table 21-9. Shaded bits and bit fields are "don't care" for MLI I/O port control.

Field	Bits	Type	Description
PC12, **PC13,** **PC14,** **PC15**	[7:4], [15:12], [23:20], [31:28]	rw	**Port Input/Output Control for Port 5.[15:12]** [1)] Port input/output control for P5.12/TDATA0B/RDATA1 Port input/output control for P5.13/TVALID0B/RVALID1 Port input/output control for P5.14/TREADY0B/RREADY1 Port input/output control for P5.15/TCLK0B/RCLK1

1) For coding of bit field, see Table 21-9. Shaded bits and bit fields are "don't care" for MLI I/O port control.

Page 21-117

In the register table, P5_PDR should be updated as below:

Field	Bits	Type	Description
PDMLI0, **PDMLI1**	[18:16], [22:20]	rw rw	**Pad Driver Mode for P5.15, P5.[13:12] and P5.10** **Pad Driver Mode for P5.14, P5.11 and P5.[9:8]**

Page 22-60

The first three sentences of the first paragraph on the top must be replaced by three extended sentences:

Old:

"Normally, a GTC is enabled by writing GTCCTRk.EOA (Enable-Of-Action) with 0. Note that bit EOA is hardware protected. Therefore, any bit operation on EOA will result in a read-modify-write access."

New:

"A GTC is enabled by writing (ST byte, word, half-word operation) GTCCTRk.EOA (Enable-Of-Action) with 0. Because bit EOA is hardware protected, read-modify-write operations (LDMST, ST.X, SWAP) only enable the GTC if bit EOA is modified from 1 to 0."

Page 22-69

In the first sentence, the wording "adjacent GTCs" must be replaced by "adjacent LTCs".

Page 22-70

Fourth bullet paragraph in section "Free-Running Timer Mode": "GTCkOUT" must be replaced by "LTCkOUT".

Page 22-71

Second bullet from the top: "GTCkOUT" must be replaced by "LTCkOUT".

Third bullet paragraph in section "Compare Mode": "GTCkOUT" must be replaced by "LTCkOUT"

The last note paragraph must be deleted.

Page 22-74

Paragraph above the figure: "GTCs" must be replaced twice by "LTCs".

Paragraph below the figure title paragraph: "GTCCTRk.OCM0" must be replaced by "LTCCTRk.OCM0".

Page 22-75

The header text "Local Capture or Compare Event" of the second column in Table 22-4 must be replaced by "Local Capture, Compare, or TImer Overflow Event".

Page 22-76

The first three sentences of the first paragraph on the top must be replaced by three extended sentences:

Old:

"Normally an LTC is enabled by writing LTCCTRk.EOA (Enable-Of-Action) with 0. Note that bit EOA is hardware protected. Therefore, any bit operation on EOA will result in a read-modify-write access."

New:

"An LTC is enabled by writing (ST byte, word, halfword operation) LTCCTRk.EOA (Enable-Of-Action) with 0 in Capture Mode or Compare Mode. Because bit EOA is hardware prodected, read-modify-write operations (LDMST, ST.X) only enable the LTC if bit EOA is modified from 1 to 0 in Capture Mode or Compare Mode. If switching to Timer Mode, the LTC cell is enabled. If in Timer Mode every write operation into bit 0..7 will enable the LTC.."

Page 22-89

The last sentence of the first paragraph should be replaced by "The GPTA module provides a total of 56 input lines and 112 output lines, assigned to **seven** I/O groups IOG[**6**:0] and **seven** output groups OG[**6**:0]."

Figure 22-59 should be updated with the below figure:

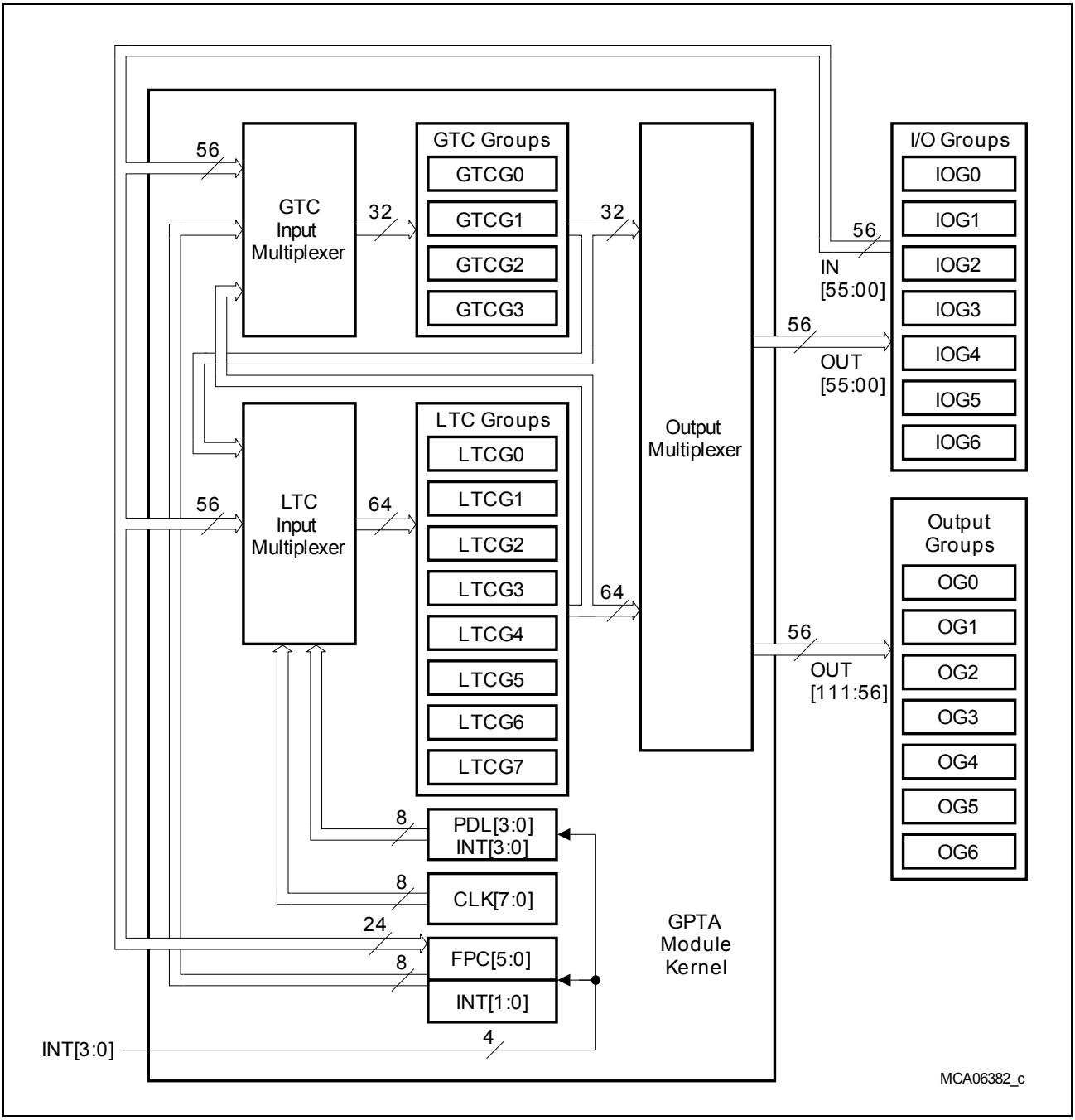

Figure 22-59 Input/Output Line Sharing Unit Overview

Page 22-90

Figure 22-60 should be updated with the below figure with the example for OG2 corrected:

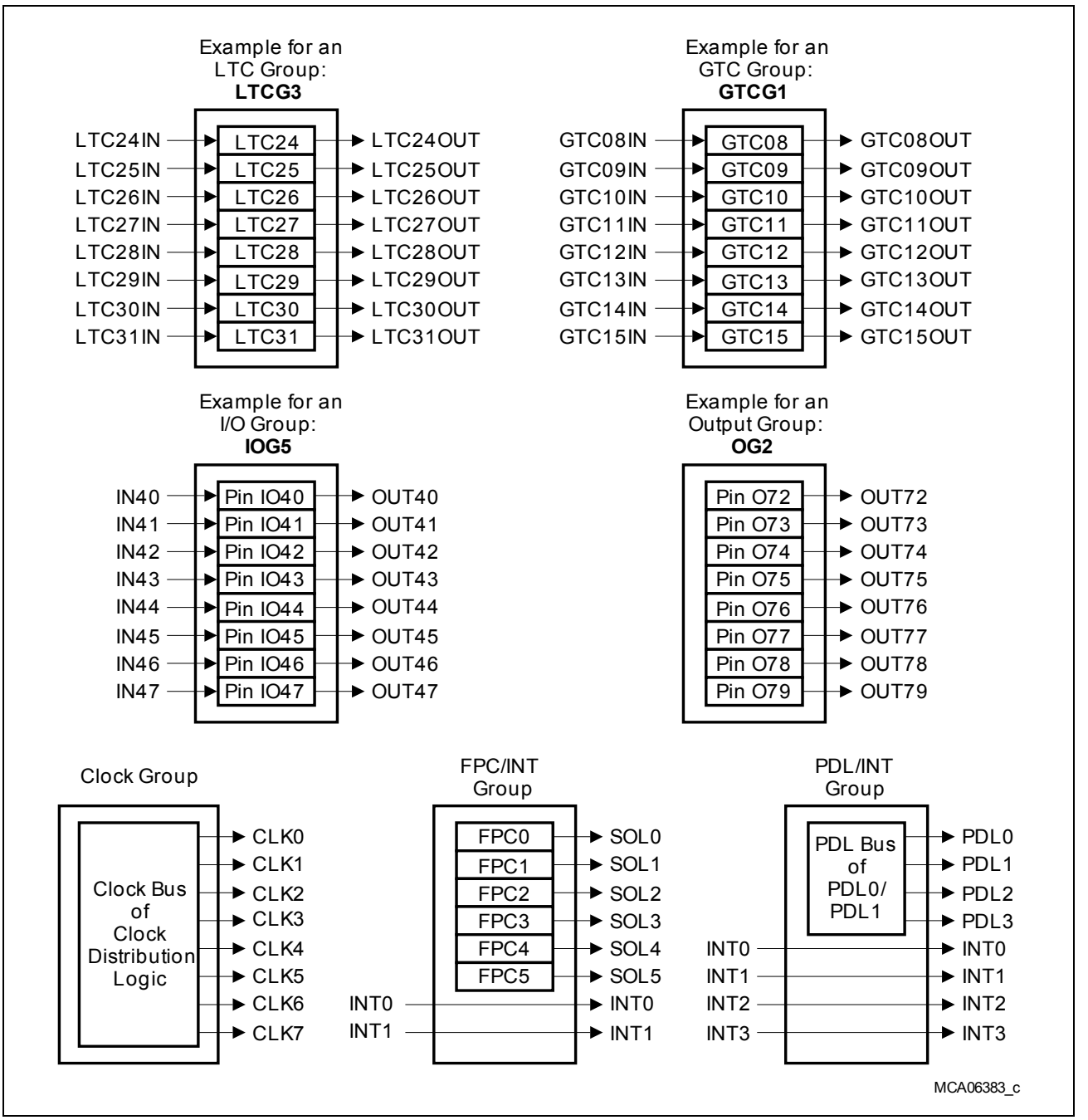

Figure 22-60 Group Definitions For I/O Line Sharing Unit

Page 22-91

The third and fourth paragraphs should be replaced by:

"An I/O group combines eight GPTA I/O lines connected to bi-directional device pins with its input and output lines. This results in **seven** I/O groups, IOG0 to **IOG6, supporting 56 I/O lines**."

"An output group combines eight GPTA output lines connected to device pins as an output. This results in **seven** output groups, OG0 to **OG6, supporting 56 output lines**."

In Table 22-8, the input and output lines assigned for I/O Groups and Output Groups should be replaced by:

Table 22-8 Group to I/O lines/Cell Assignment

Group/Module	Cell/Line	Input	Output
I/O Group			
IOG0	–	IN[07:00]	OUT[07:00]
IOG1	–	IN[15:08]	OUT[15:08]
IOG2	–	IN[23:16]	OUT[23:16]
IOG3	–	IN[31:24]	OUT[31:24]
IOG4	–	IN[39:32]	OUT[39:32]
IOG5	–	IN[47:40]	OUT[47:40]
IOG6	**–**	**IN[55:48]**	**OUT[55:48]**
Output Group			
OG0	–	–	OUT[63:56]
OG1	–	–	OUT[71:64]
OG2	–	–	OUT[79:72]
OG3	–	–	OUT[87:80]
OG4	–	–	OUT[95:88]
OG5	–	–	OUT[103:96]
OG6	–	–	OUT[111:104]

Page 22-94

The first paragraph of Section 22.2.4.2 should be replaced by "The output multiplexer shown in Figure 22-59 and Figure 22-61 below connects the 32 GTC output lines and the 64 LTC output lines with the I/O groups (**7 x 8 = 56** input/output lines) and the output groups (**7 x 8 = 56** output lines).

Figure 22-61 should be updated with the below figure:

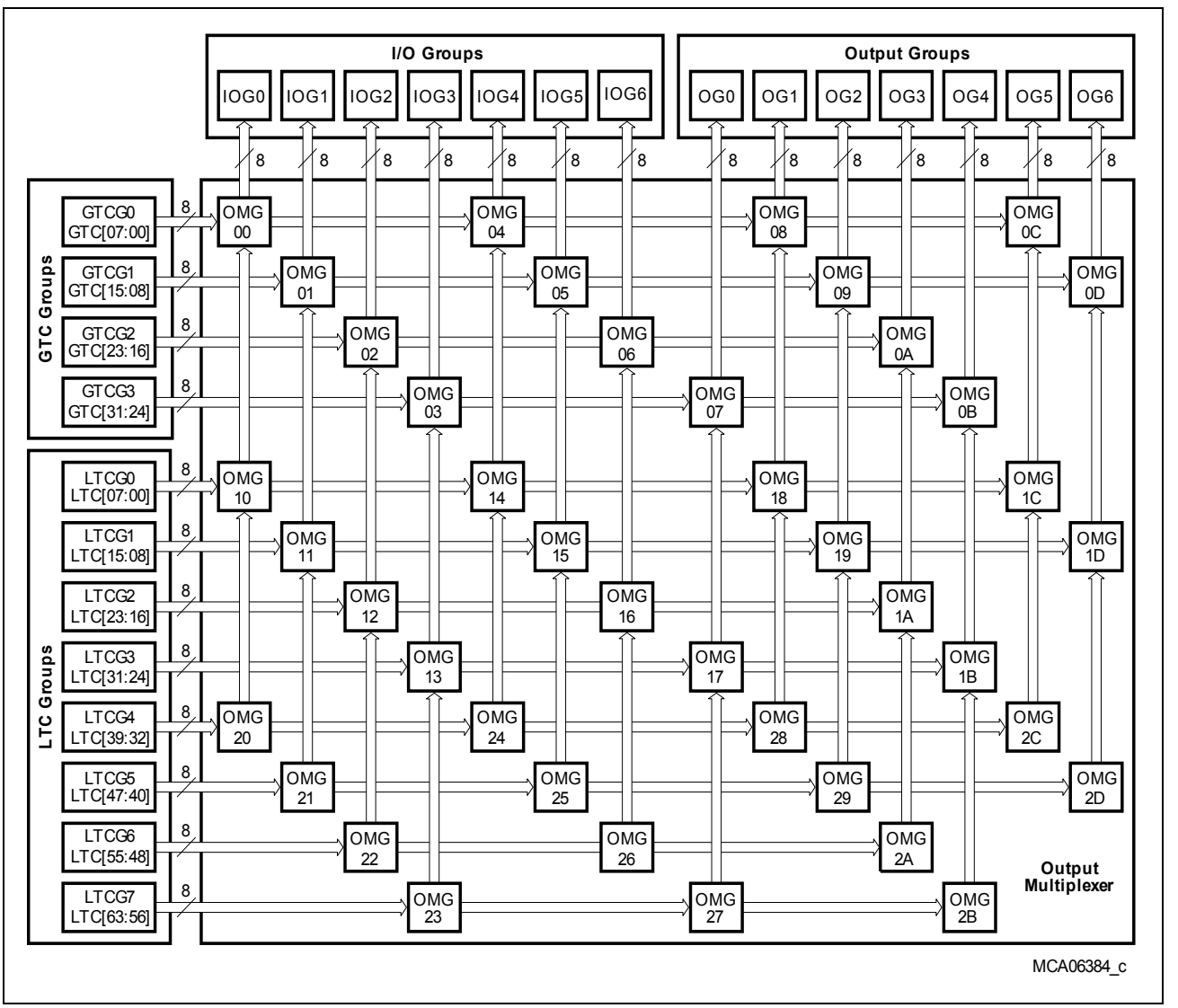

Figure 22-61 Output Multiplexer

The third sentence onwards for the paragraph below Figure 22-61 should be replaced by "In the same way, I/O groups and output groups are grouped into 14 groups (**seven** I/O groups and **seven** output groups) with 8 lines each. IOG0 and **OG0** share the same physical pins, similarly for IOG1 and **OG1**, IOG2 and **OG2**. **IOG3 and IOG6 share the same physical pins for inputs and outputs.**

Page 22-96

The second sentence of the third bulleted point should be replaced by:

"I/O groups **IOG0 to IOG6** are assigned to index variable (g = 0 to **6**) and output groups OG0 to **OG6** are assigned to index variable (g = **7** to 13)."

Figure 22-63 should be updated with the below figure:

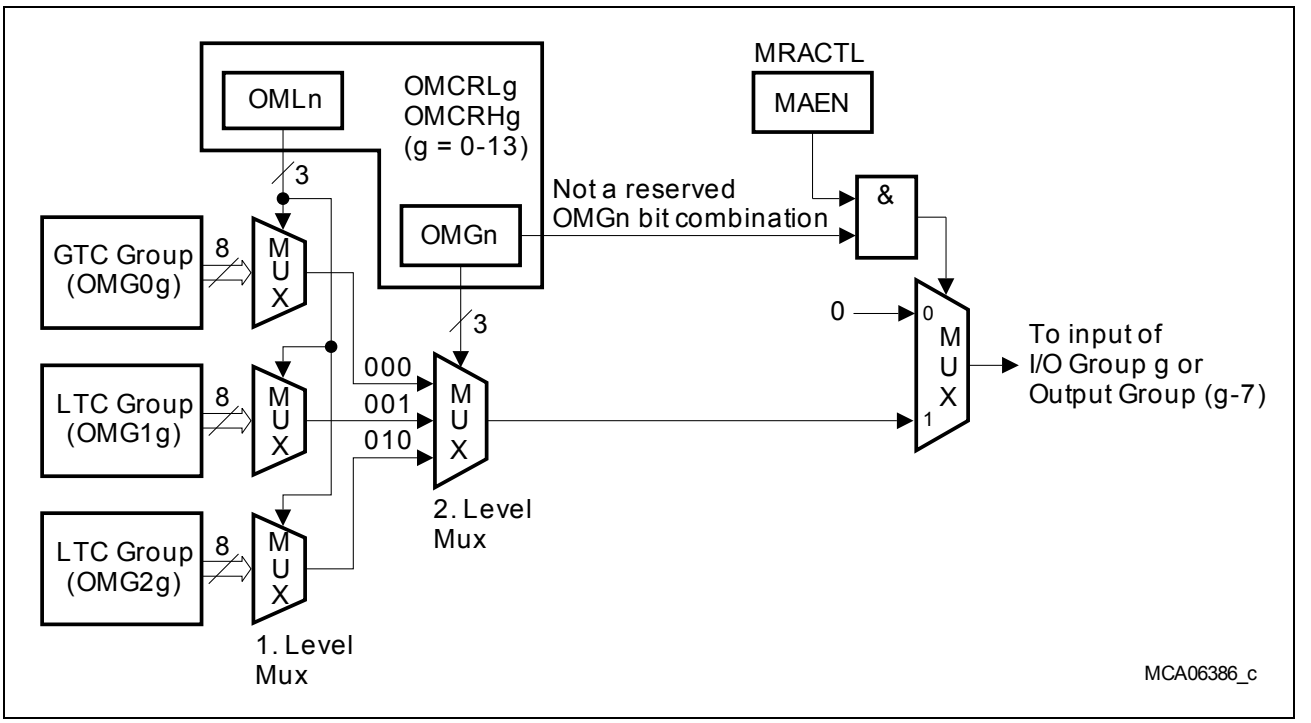

Figure 22-63 Output Multiplexer Group (Programmer's View)

Page 22-97

In Table 22-10, the input and output lines assigned for I/O Groups IOG3 and Output Groups OG0 to OG7 should be replaced by:

Table 22-8 Output Multiplexer Control Register Assignment

Input/Output Group		Controlled by Multiplexer Control Register	Selectable Groups via OMGng
IOG3	IN[27:24]/OUT[27:24]	OMCRL3	GTGG3,LTCG3, LTCG7
	IN[31:28]/OUT[31:28]	OMCRH3	
IOG6	**IN[51:48]**/OUT[51:48]	OMCRL6	GTGG2,LTCG2, LTCG6
	IN[55:52]/OUT[55:52]	OMCRH6	
OG0	OUT[59:56]	OMCRL7	GTGG3,LTCG3, LTCG7
	OUT[63:60]	OMCRH7	
OG1	OUT[67:64]	OMCRL8	GTGG0,LTCG0, LTCG4
	OUT[71:68]	OMCRH8	
OG2	OUT[75:72]	OMCRL9	GTGG1,LTCG1, LTCG5
	OUT[79:76]	OMCRH9	
OG3	OUT[83:80]	OMCRL10	GTGG2,LTCG2, LTCG6
	OUT[87:84]	OMCRH10	
OG4	OUT[91:88]	OMCRL11	GTGG3,LTCG3, LTCG7
	OUT[95:92]	OMCRH11	
OG5	OUT[99:96]	OMCRL12	GTGG0,LTCG0, LTCG4
	OUT[103:100]	OMCRH12	
OG6	OUT[107:104]	OMCRL13	GTGG1,LTCG1, LTCG5
	OUT[111:108]	OMCRH13	

Page 22-99

Figure 22-64 should be updated with the below figure:

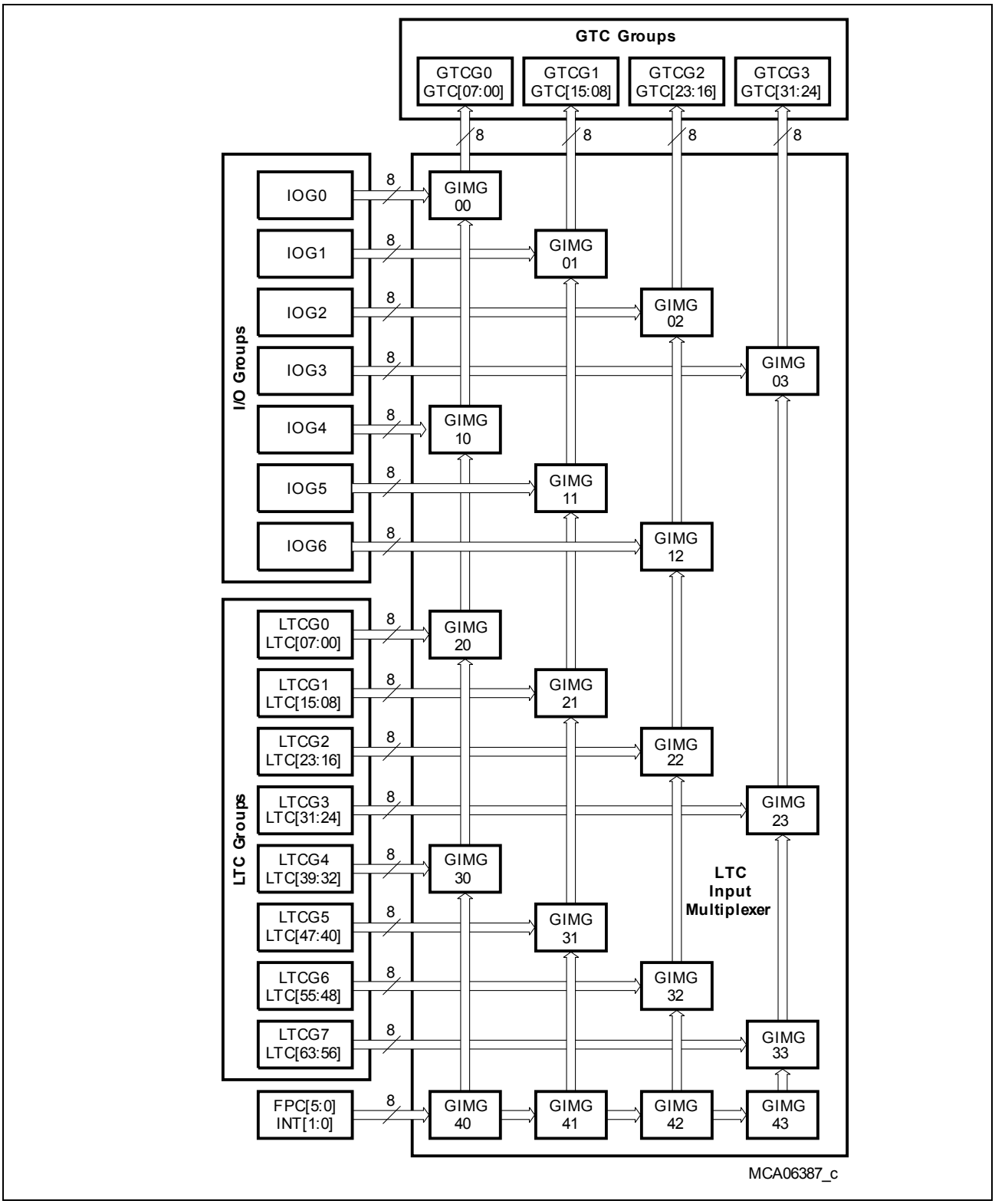

Figure 22-64 GTC Input Multiplexer

Page 22-100

The second sentence of the first paragraph should be replaced by:

"GTC input Multiplexer Group are grouped into **seven** IOGs (IOG[**6**:0]) with seven blocks of eight lines each and eight LTC groups (LTCG[7:0]) with 8 cells each."

Page 22-101

The second bulleted point should be replaced by:

"Index n is a group number. I/O groups IOG[3:0] have group number 0, I/O groups IOG[**6**:4] have group number 1, local timer cell groups LTCG[3:0] have group number 2, Local Timer Cell Groups LTCG[7:4] have group number 3, and the FPC/INT group has group number 4."

The last sentence of the next paragraph should be replaced by:

"For example, based on Figure 22-64, each of the eight GTC input multiplexer output lines to GTC group GTCG2 is connected via five **GI**MGn2 (n =0-4) with the eight outputs of two I/O group (IOG2 and IOG**6**), two LTC groups (LTCG2 and LTCG6), and the FPC/INT group."

Page 22-103

In Table 22-11, the text IOG3 of GTCG2 row should be replaced by "**IOG6**"

Page 22-104

Figure 22-67 should be updated with the below figure:

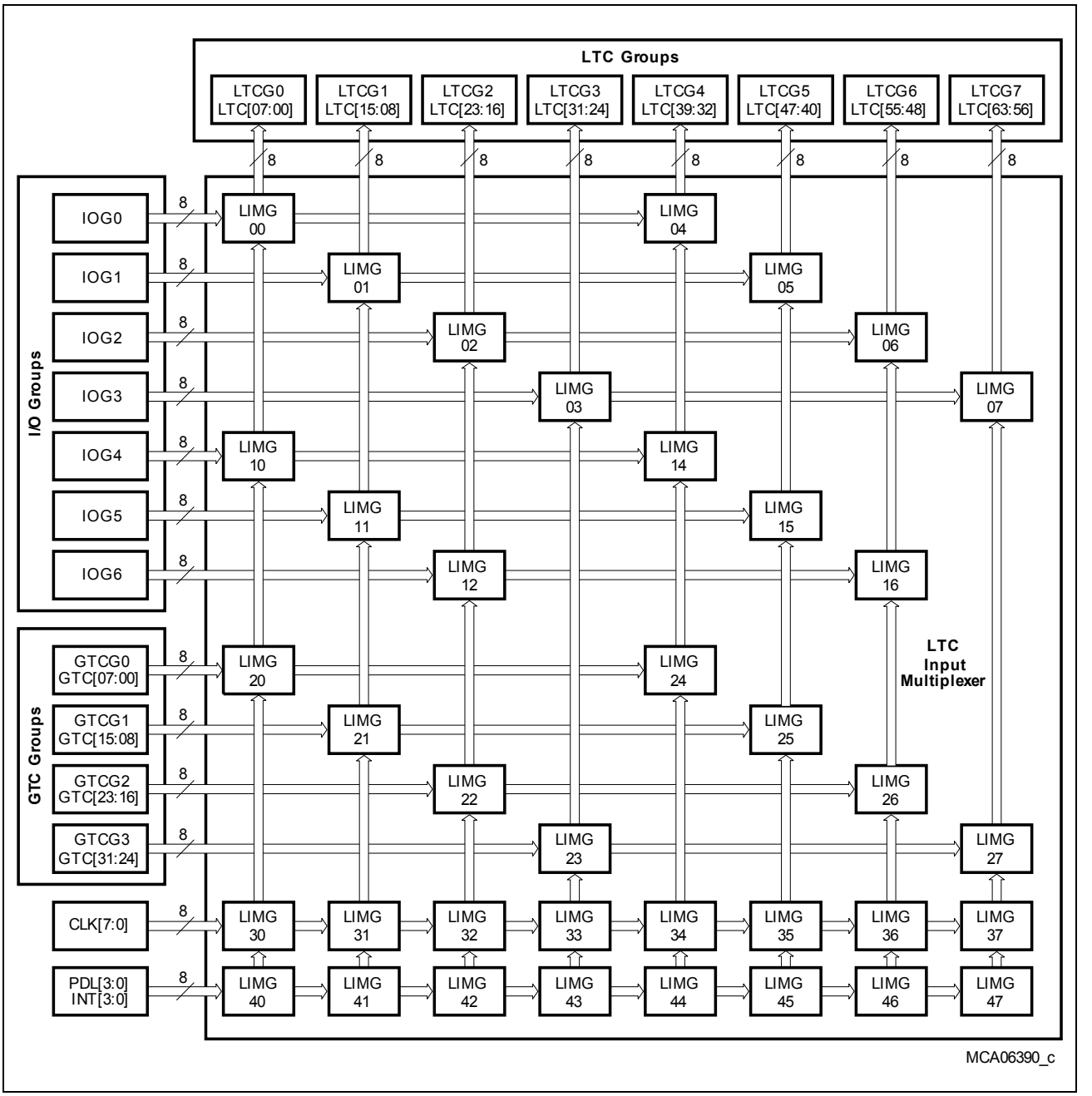

Figure 22-67 LTC Input Multiplexer

Page 22-105

The second sentence of the first paragraph should be replaced by:

"IOGs and GTCs are grouped into **seven** IOGs (IOG[**6**:0]) with seven blocks of eight lines each and four GTC groups (GTCG[3:0]) with 8 cells each."

Page 22-106

The second bulleted point of the first paragraph should be replaced by:

"Index n is a group number. I/O groups IOG[3:0] have group number 0, I/O groups IOG[**6**:4] have group number 1, Global Timer Cell Groups GTCG[3:0] have group number 2, clock bus lines CLK[7:0] have group number 3, and the PDL/INT group has group number 4."

The last sentence of the next paragraph should be replaced by:

"For example, based on Figure 22-67, each of the eight LTC input multiplexer output lines to LTC group LTCG2 is connected via five LIMGn2 (n = 0-4) with the eight outputs of two I/O group (IOG2 and IOG**6**), one GTC group (GTCG2), the clock group, and the PDL/INT group."

Page 22-108

In Table 22-12, the text IOG3 of LTCG2 row should be replaced by "**IOG6**"

Page 22-125

The text "else DCMk.Timer ++" must be included between the last two "endif" lines on the bottom.

Page 22-132

Below the second last line of the page : "GTCk.Cell_Enable = 1", the following line must be added: "GTCk.Enable_Of_Action = 0"

Pages 22-173 and 22-174

The long name of register LTCCTRk must be corrected as "Local Timer **Cell** Control Register k .....".

Page 22-178

The long name of register LTCCTR63 must be corrected as "Local Timer **Cell** Control Register 63".

Page 22-184

The text for Section Output Multiplexer Control Registers should be replaced by:

"Two registers, OMCRL and OMCRH, are assigned to each I/O Group IOG[**6**:0] and each Output Group OG[**6**:0]. OMCRL[**6**:0]/OMCRH[**6**:0] are assigned to IOG[**6**:0] and OMCRL[13:**7**]/OMCRH[13:**7**] are assigned to OG[**6**:0].

OMCRL controls the connections of group pins 0 to 3. OMCRH controls the connections of group pins 4 to 7."

Page 22-200

The first sentence of the first paragraph of Section 22.4.3.1 should be replaced by:

"In the TC1766, the **seven** I/O groups and **three** output groups of GPTA0 with their input lines IN[55:0] and output lines OUT[79:0] are assigned to five 8-bit port groups and two 4-bit port groups as shown in Figure 22-75."

Figure 22-75 should be updated with the below figure:

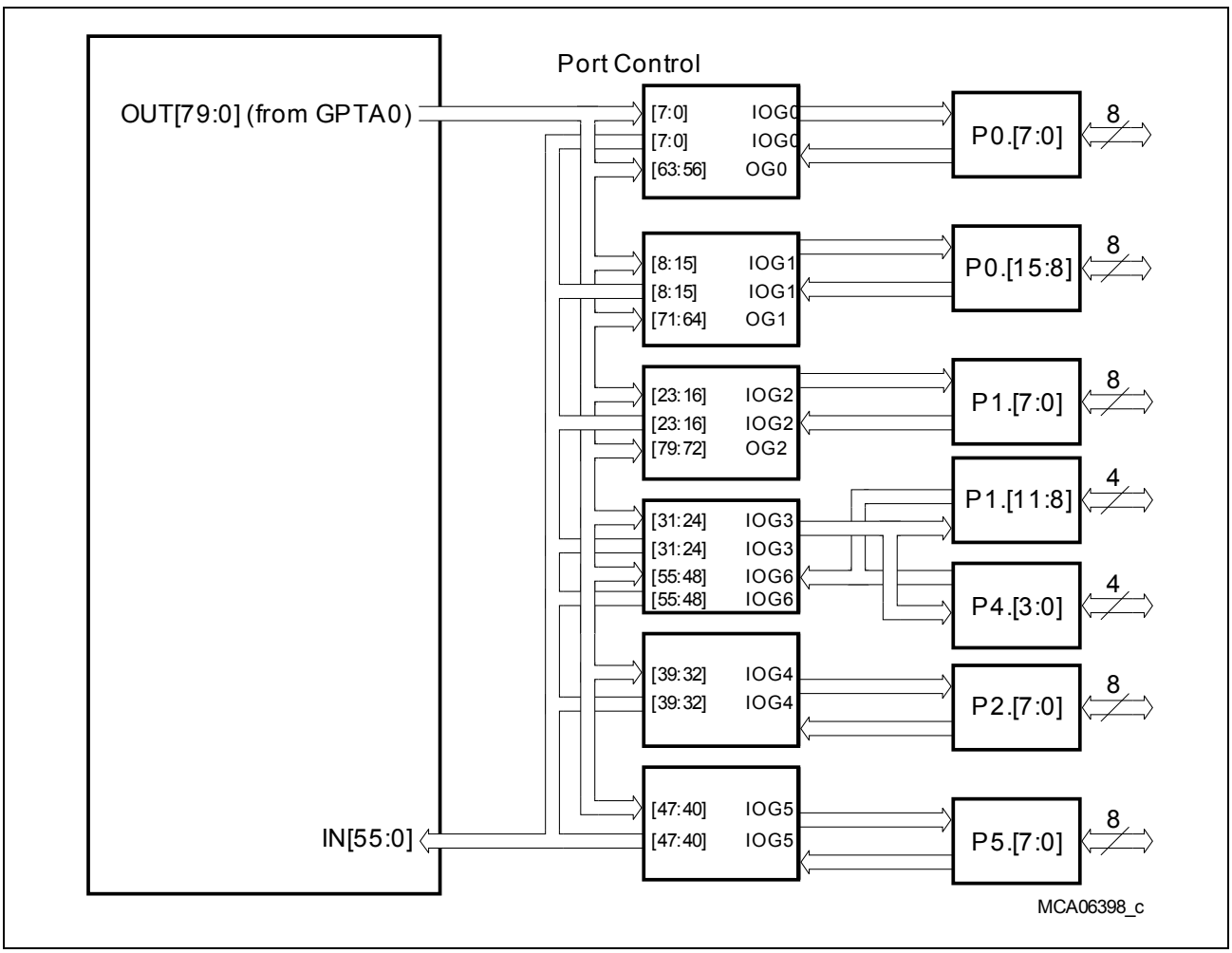

Figure 22-75 I/O Port Line Assignment

Page 22-205

The following sentence should be added above Table 22-22, " Table 22-22 also shows the assignment of the GPTA module's four OGx output group lines OGx.y to the output signals OUT[111:80]."

Table 22-22 GPTA0 to MSC Interconnection Assignment

MSC0 Input Line	Assigned GPTA0 Output Line	MSC0 Input Line	Assigned GPTA0 Output Line
ALTIN0.0	OUT80 / **OG3.0**	ALTIN1.0	OUT96 / **OG5.0**
ALTIN0.1	OUT81 / **OG3.1**	ALTIN1.1	OUT97 / **OG5.1**
ALTIN0.2	OUT82 / **OG3.2**	ALTIN1.2	OUT98 / **OG5.2**
ALTIN0.3	OUT83 / **OG3.3**	ALTIN1.3	OUT99 / **OG5.3**
ALTIN0.4	OUT84 / **OG3.4**	ALTIN1.4	OUT100 / **OG5.4**
ALTIN0.5	OUT85 / **OG3.5**	ALTIN1.5	OUT101 / **OG5.5**
ALTIN0.6	OUT86 / **OG3.6**	ALTIN1.6	OUT102 / **OG5.6**
ALTIN0.7	OUT87 / **OG3.7**	ALTIN1.7	OUT103 / **OG5.7**
ALTIN0.8	OUT88 / **OG4.0**	ALTIN1.8	OUT104 / **OG6.0**
ALTIN0.9	OUT89 / **OG4.1**	ALTIN1.9	OUT105 / **OG6.1**
ALTIN0.10	OUT90 / **OG4.2**	ALTIN1.10	OUT106 / **OG6.2**
ALTIN0.11	OUT91 / **OG4.3**	ALTIN1.11	OUT107 / **OG6.3**
ALTIN0.12	OUT92 / **OG4.4**	ALTIN1.12	OUT108 / **OG6.4**
ALTIN0.13	OUT93 / **OG4.5**	ALTIN1.13	OUT109 / **OG6.5**
ALTIN0.14	OUT94 / **OG4.6**	ALTIN1.14	OUT110 / **OG6.6**
ALTIN0.15	OUT95 / **OG4.7**	ALTIN1.15	OUT111 / **OG6.7**

Page 22-209

The following attention paragraph must be added at the bottom of the page:

Attention: If the frequency of the module timer clock f_{GPTA0} is configured to be smaller than the control clock f_{CLC} (as programmed in register GPTA0_FDR) or even disabled (as programmed in register GPTA0_EDCTR), an action initiated by a write access to a module register could be significantly delayed, because the register write access is clocked by f_{CLC} and the register content is evaluated by hardware using the slower or disabled module timer clock f_{GPTA0}.

Page 23-9

The formula on the bottom of the page must be corrected into:

$$t_{TPERIOD} = TRLD \times \frac{20}{f_{ADC}} \quad (23.1)$$

Page 23-96

Footnote 1 must be deleted from AN24 to AN31 cells.

Page 23-97

The below text must be inserted before Figure 23-30.

For safety reasons, the measurement of the ADC channels 0-15 (GRPS = 0) is always related to the reference input pin (the programmed selection is not taken into account). The measurement of the ADC channels 16-31 (GRPS = 1) is always related to the programmed reference (the programmed selection is taken into account).

Page 24-6

The two heading paragraphs must be corrected in the following way:

Replace **"Configuration 3"** with **"Configuration 2"**

Replace **"Configuration 4"** with **"Configuration 3"**

Page 24-7

The text in the leftmost column of Table 24-1 must be corrected in the following way:

Replace **"(Configuration 2)"** with **"(Configuration 1)"**

Replace **"(Configuration 3)"** with **"(Configuration 2)"**

Replace **"(Configuration 4)"** with **"(Configuration 3)"**

The last row of Table 24-1 (FAINxN | FAINxP I XX_B | 512) must be deleted.

Page 24-8

The second formula of equation (24.1) should be corrected into:

$V_{FAREFM} = V_{FAGND} + (V_{FAREF} - V_{FAGND})/2$

w w w . i n f i n e o n . c o m

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