# AC100

# User Manual

**Revision 1.0**

**2014/06/10**

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# About Documentation

This documentation of AC100 is intended to be used by board-level product designers and product software developers. The manual assumes that the reader has a background in computer engineering and/or software engineering and understands concepts of digital system design, microprocessor architecture, Input / Output (I/O) devices, industry standard communication and device interface protocols.

## Organization

This document aims to describe the AC100 from following aspects: block diagram, pin assignment, pin/signal description, electrical characteristics, typical application, system description and register description.

# Revision History

| Version | Date | Description |
| --- | --- | --- |
| V0.1 | 2014/3/3 | Complete Draft |
| V0.2 | 2014/5/14 | Modify the format |
| V1.0 | 2014/6/10 | Modify the format |
|  |  |  |

# Table of Contents

# 1. Description

The AC100 is a highly integrated audio codec and RTC subsystem designed for tablet and smart mobile application platforms. It has three I2S/PCM interface, 2 channels DAC and 2 channel ADC with a high level of mixed-signal integration. Three audio interface are available in order to provide independent and fully asynchronous connections to multiple processors, typically such as an application processor, baseband and bluetooth transceiver.

An integrated digital PLL supports a large range of input/output frequencies, and It can generate required audio clocks for codec from standard audio crystal rate such as 22.5792MHz and 24.576MHz, also can be from common reference clock frequencies such as 12MHz, 13MHz and 19.2MHz, and an internal RC oscillator can be used in Free-running Mode, where the application processor can be inactive during voice call application. The 2 ADC and 2 DAC in device use advanced multi-bit delta-sigma modulation technique to convert data between analog and digital . The SNR performance can reach 100 dB A-wight.

Five analog input paths allow diverse analog audio sources such as three sets of differential microphone, one differential or single-ended linein and one stereo FM input.

One ground-reference headphone output is provided. The output amplifier are powered from an integrated Charge Pump in order to achieve a higher quality, less power consumption in headphone playback, whist without any DC blocking capacitor and avoiding unwanted noise.

A mono, differential BTL drive amplifier is available for driving the handset receiver.

Two stereo differential speaker output is available by using an external amplifier to drive the loud-speaker. It can also be configured as single-ended output pin for some application of external single-ended amplifier.

The flexible analogue and digital mixers form a varied signal routing to support a complicated application.

AC100 is controlled through TWI (2-wire serial interface ) or RSB[①] (reduced serial bus) . It works only in the slave mode .

The integrated DRC(Dynamic Range Controller) function in AC100 provide an useful digital sound processing capability in DAC playback path to speaker . It is uesed to attenuate the peak signals and boost the low-level signals by adjusting the output signal gain in some conditions. The DRC functions can be enable or disable in the playback path .

The integrated AGC(Automatic Gain Controller) function can be used to maintain a constant recording level in ADC record path . The DRC can make an improvement in background noise by setting a programmable Noise Gate to attenuate very low-level input signals .

Note: ① The RSB is independent R&D by x-powers, supports a special protocols with a simplified two wire protocol on a push-pull bus. The transfer speed in AC100 can be up to 10MHz .

# 2. Features

The AC100 features:

- 2 ADCs and 2 DACs @ 24-bit and inter PLL processing with flexible clocking scheme

- Up to 100dB SNR during DAC playback path (A ' weight)

- Up to 95dB SNR during ADC record path (A ' weight)

- Capless stereo headphone driver

  - Integrated charge pump for 0V reference
  - 18mW @1.8V

- Mono differential earpiece driver

  - >65 mW/CH (THD+N ≤ -70dB, 16Ohm Load)

- Two stereo differential speaker outputs using external amplifier to drive the loud speaker

- Differential Line output with 1 Vrms full scale output voltage

- Five audio inputs

  - Three differential analog microphone inputs with 30dB~48dB boost amplifier gain
  - One mono differential or single-ended line-in input
  - One stereo auxiliary input for external accessory connection

- Two low noise analog microphone bias

- Audio jack insert/ button press detection

- TWI/RSB control interface

- 24-bit 8KHz ~ 192KHz I2S/PCM interface

- Support Dynamic Range Controller (DRC) adjusting the DAC playback output

- Support Automatic Gain Control (AGC) adjusting the ADC recording output

- SRC for synchronisation between audio interface or digital audio data mixing

- Soft mute circuit for pop noise suppression

- Support digital microphone interface

- RTC and Three clock output

- QFN 68-pin package, 8mm x 8mm

# 3.  Applications

• Tablets

• Smart Phone and Music phone

# 4.  Functional Block Diagram

## 4.1.  Functional Block Diagram
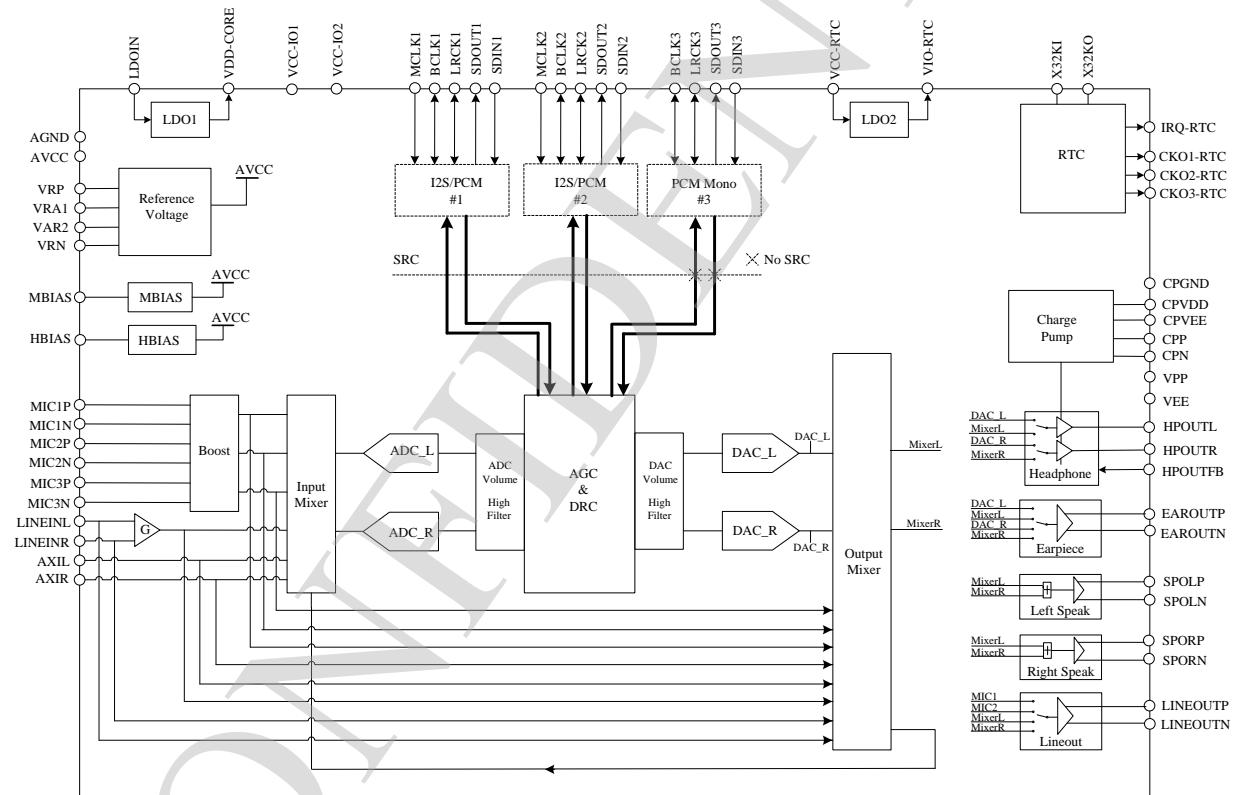


**Figure 1    Functional Block Diagram**

# 4.2. Data Path Diagram
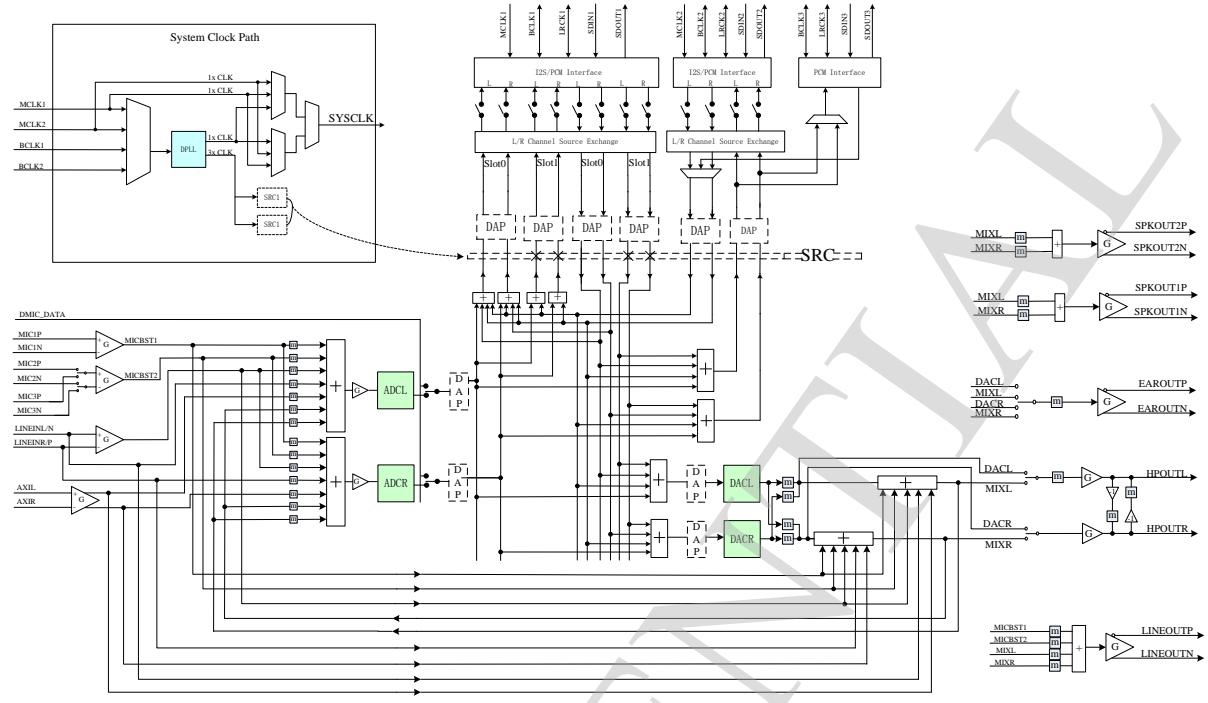


**Figure 2   Data Path Diagram**

# 5. Pin Assignment
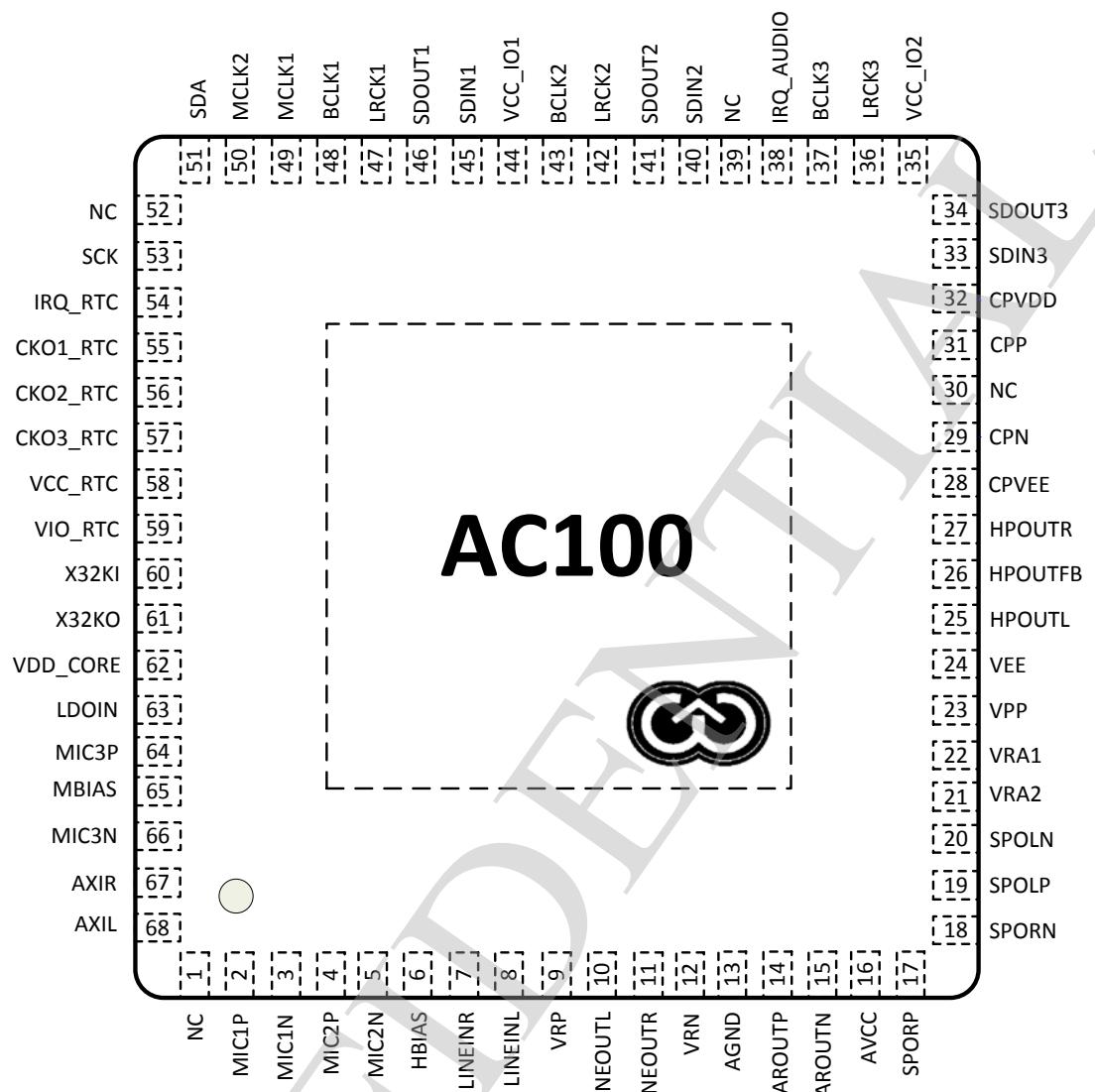


**Figure 3    Pin Assignment**

# 6. Package Dimension
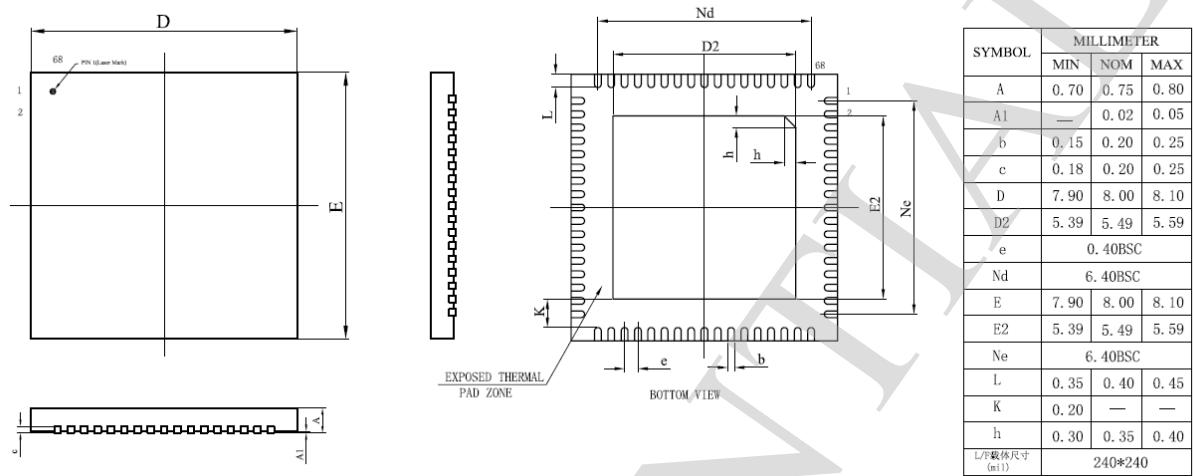


**Figure 4  Package Dimension**

| SYMBOL | MILLIMETER | | |
|--------|------|------|------|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | — | 0.02 | 0.05 |
| b | 0.15 | 0.20 | 0.25 |
| c | 0.18 | 0.20 | 0.25 |
| D | 7.90 | 8.00 | 8.10 |
| D2 | 5.39 | 5.49 | 5.59 |
| e | 0.40BSC | | |
| Nd | 6.40BSC | | |
| E | 7.90 | 8.00 | 8.10 |
| E2 | 5.39 | 5.49 | 5.59 |
| Ne | 6.40BSC | | |
| L | 0.35 | 0.40 | 0.45 |
| K | 0.20 | — | — |
| h | 0.30 | 0.35 | 0.40 |
| L/F载体尺寸(mil) | 240*240 | | |

# 7. Pin/Signal Description

This chapter describes the 68 pins of AC100 from four aspects: pin number, signal name, type, and pin definition. All the pins are classified into four groups, including digital IO pin, analog IO pin, filter/reference, and power/ground.

There are five pin types here: O for output, I for input, I/O for input/output, P for power, and G for ground.

| Pin Number | Signal Name | Type | Description |
|---|---|---|---|
| **Digital IO Pins** | | | |
| 49 | MCLK1 | I | I2S interface master input clock 1 |
| 45 | SDIN1 | I | First I2S interface serial data input |
| 46 | SDOUT1 | O | First I2S interface serial data output |
| 48 | BCLK1 | I/O | First I2S interface serial bit clock |
| 47 | LRCK1 | I/O | First I2S interface synchronous clock |
| 50 | MCLK2 | I | I2S interface master iuput clock 2 |
| 40 | SDIN2 | I | Second I2S interface serial data input |
| 41 | SDOUT2 | O | Second I2S interface serial data output |
| 43 | BCLK2 | I/O | Second I2S interface serial bit clock |
| 42 | LRCK2 | I/O | Second I2S interface synchronous clock |
| 33 | SDIN3 | I | Third I2S interface serial data input |
| 34 | SDOUT3 | O | Third I2S interface serial data output |
| 37 | BCLK3 | I/O | Third I2S interface serial bit clock |
| 36 | LRCK3 | I/O | Third I2S interface synchronous clock |
| 51 | SDA | I/O | TWI interface serial data(Open-drain) <br> RSB interface serial data |
| 53 | SCK | I | TWI interface serial clock input <br> RSB interface serial clock input |
| 38 | IRQ_AUDIO | O | IRQ for accessory insert and button detect(Open-drain) |
| 54 | IRQ_RTC | O | IRQ for RTC alarm interrupt…(Open-drain) |
| 60 | X32KI | I | The external oscillator input singal |
| 61 | X32KO | O | The external oscillator output singal |
| 55 | CKO1_RTC | O | RTC 32.768 KHz clock output(Push-pull ) |
| 56 | CKO2_RTC | O | RTC 32.768 KHz clock output(Open-drain) |
| 57 | CKO3_RTC | O | RTC 32.768 KHz clock output(Open-drain) |
| **Analog IO Pin** | | | |
| 2 | MIC1P | I | Positive differential input for MIC1 |
| 3 | MIC1N | I | Negative differential input for MIC1 |
| 4 | MIC2P | I | Positive differential input for MIC2 |
| 5 | MIC2N | I | Negative differential input for MIC2 |
| 64 | MIC3P/ <br> DMICCLK | I <br> O | Analog Positive differential input for MIC3 <br> Digital microphone clock output |
| 66 | MIC3N/ <br> DMICDAT | I <br> O | Negative differential input for MIC3 <br> Digital microphone data input |
| 8 | LINEINL | I | Left single-end or differential input for LINE-IN |

| 7 | LINEINR | I | Right single-end or differential input for LINE-IN |
|---|---------|---|---------------------------------------------------|
| 68 | AXIL | I | Auxiliary left Channel input |
| 67 | AXIR | I | Auxiliary right Channel input |
| 25 | HPOUTL | O | Headphone amplifier left channel output |
| 27 | HPOUTR | O | Headphone amplifier right channel output |
| 19 | SPOLP | O | Differential positive output to speaker1 amplifier |
| 20 | SPOLN | O | Differential negative output to speaker1 amplifier |
| 17 | SPORP | O | Differential positive output to speaker2 amplifier |
| 18 | SPORN | O | Differential negative output to speaker2 amplifier |
| 14 | EAROUTP | O | Earpiece amplifier positive differential output |
| 15 | EAROUTN | O | Earpiece amplifier negative differential output |
| 11 | LINEOUTP | O | Positive output for LINE-OUT |
| 10 | LINEOUTN | O | Negative output for LINE-OUT |
| **Filter/Reference** | | | |
| 65 | MBIAS | O | First bias voltage output for main microphone |
| 6 | HBIAS | O | Second bias voltage output for headset microphone |
| 26 | HPOUTFB | I | Pseudo differential headphone ground reference |
| 29 | CPN | I/O | Charge pump flying-back capacitor |
| 31 | CPP | I/O | Charge pump flying-back capacitor |
| 22 | VRA1 | O | Internal reference voltage |
| 21 | VRA2 | O | Internal reference voltage |
| 9 | VRP | O | Internal reference voltage |
| 12 | VRN | O | Internal reference voltage |
| **Power/Ground** | | | |
| 16 | AVCC | P | Analog power |
| 13 | AGND | G | Analog ground |
| 32 | CPVDD | P | Analog power for headphone charge pump |
| 28 | CPVEE | P | Charge pump negative decoupling Pin |
| 23 | VPP | P | Headphone PA positive voltage input |
| 24 | VEE | P | Headphone PA negative voltage input |
| 62 | VDD_CORE | P | Digital power for digital core |
| 44 | VCC_IO1 | P | Digital power for digital I/O buffer（I2S1&I2S2） |
| 35 | VCC_IO2 | P | Digital power for digital I/O buffer（I2S3） |
| 63 | LDOIN | P | Input power for Audio_LDO |
| 59 | VIO_RTC | P | Digital power for RTC |
| 58 | VCC_RTC | P | Input power for RTC_LDO |
| 69 | GND | G | Digital ground |
| **Others** | | | |
| 1,30,39,52 | NC | -- | Not connected |

# 8. Electrical Characteristics

## 8.1. Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under electrical characteristics at the test conditions specified.

| Symbol | Parameter | MIN | MAX | Unit |
|--------|-----------|-----|-----|------|
| LDO_IN | LDO Input power for AudioCODEC | -0.3 | 3.63 | V |
| VDD_CORE | Digital power for Audio digital core, it can be generate by inner LDO | -0.3 | 1.32 | V |
| VCC_IO1 | Digital power for digital I/O buffer (I2S1&I2S2) | -0.3 | 3.63 | V |
| VCC_IO2 | Digital power for digital I/O buffer (I2S1&I2S3) | -0.3 | 3.63 | V |
| CPVDD | Analog power for headphone charge pump | -0.3 | 2.0 | V |
| VCC_RTC | LDO Input power for RTC | -0.3 | 3.63 | V |
| VIO_RTC | Digital power for RTC digital core, it can be generate by inner LDO | -0.3 | 1.32 | V |
| $T_A$ | Operating Ambient Temperature | -20 | 85 | ℃ |
| $V_{ESD}$ | ESD | 4 | -- | KV |

## 8.2. Recommended Operating Conditions

| Parameter | Description | MIN | TPY | MAX | Unit |
|-----------|-------------|-----|-----|-----|------|
| LDO_IN | LDO Input power for AudioCODEC | 1.35 | 1.8/1.5 | 3.63 | V |
| VDD_CORE | Digital power for Audio digital core, it can be generate by inner LDO | 1.08 | 1.2 | 1.32 | V |
| VCC_IO1 | Digital power for digital I/O buffer (I2S1&I2S2) | -- | 1.8/3.3 | 3.63 | V |
| VCC_IO2 | Digital power for digital I/O buffer (I2S1&I2S3) | -- | 1.8/3.3 | 3.63 | V |
| CPVDD | Analog power for headphone charge pump | 1.2 | 1.8 | 1.98 | V |
| VCC_RTC | LDO Input power for RTC | 1.35 | 1.8/3.3 | 3.63 | V |
| VIO_RTC | Digital power for RTC digital core, it can be generate by inner LDO | 1.08 | 1.2 | 1.32 | V |
| GND,AGND | Ground reference | -- | 0 | -- | V |

## 8.3. Static Characteristics

| Symbol | Parameter | Test condition | Min | Typical | Max | Units |
|--------|-----------|----------------|-----|---------|-----|-------|
| $V_{IN}$ | Input Voltage Range | -- | -0.3 | -- | VCCIO1+0.3 VCCIO2+0.3 | V |
| $V_{IH}$ | High Level Input Voltage | VCCIO=3.0v | 2.4 | -- | 3.6 | V |
| | | VCCIO=1.8V | 1.4 | -- | 1.98 | |
| $V_{IL}$ | Low Level Input Voltage | VCCIO=3.0v | -0.3 | -- | 0.7 | V |
| | | VCCIO=1.8V | -0.3 | -- | 0.7 | |
| $V_{OH}$ | High Level Input Voltage | VCCIO=3.0v | 2.7 | -- | NA | V |
| | | VCCIO=1.8V | 1.5 | -- | NA | |
| $V_{OL}$ | Low Level Input Voltage | VCCIO=3.0v | NA | -- | 0.4 | V |
| | | VCCIO=1.8V | NA | -- | 0.4 | |
| $I_{OZ}$ | Tri-state Output Leakage Current | -- | TBD | TBD | TBD | uA |
| $C_{IN}$ | Input Capacitance | -- | NA | NA | 5 | pF |
| $C_{OUT}$ | Output Capacitance | -- | NA | NA | 5 | pF |

# 9. Analog Performance Characteristics

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UINT |
|---|---|---|---|---|---|---|
| **DAC Output Path Performance** | **DAC to Headphone on HPOUTL or HPOUTR(R=10kΩ)** | | | | | |
| | FScale Output Level | 0dB 1KHz | | 0.9 | | Vrms |
| | SNR(A-weighted) | 0dB 1KHz | | 100 | | dB |
| | THD+N(NO-Aweight) | 0dB 1KHz | | -84 | | dB |
| | Crosstalk（L/R） | 0dB 1KHz | | -88/-88 | | dB |
| | **DAC to Headphone on HPOUTL or HPOUTR(R=16Ω)** | | | | | |
| | FScale Output Level | 0dB 1KHz | | 0.5 | | Vrms |
| | SNR(A-weighted) | 0dB 1KHz | | 99 | | dB |
| | THD+N(P0=15mW) | 0dB 1KHz | | -81 | | dB |
| | THD+N(P0=5mW) | 0dB 1KHz | | -82 | | dB |
| | Crosstalk（L/R） | 0dB 1KHz | | -82/-82 | | dB |
| | **DAC to Headphone on HPOUTL or HPOUTR(R=32Ω)** | | | | | |
| | FScale Output Level | 0dB 1KHz | | 0.7 | | Vrms |
| | SNR(A-weighted) | 0dB 1KHz | | 100 | | dB |
| | THD+N(P0=15mW) | 0dB 1KHz | | -83 | | dB |
| | THD+N(P0=5mW) | 0dB 1KHz | | -83 | | dB |
| | Crosstalk（L/R） | 0dB 1KHz | | -86/-86 | | dB |
| | **DAC to Earpiece Driver on EAROUTP and EAROUTN(R=16Ω)** | | | | | |
| | FScale Output Level | 0dB 1KHz | | 1.0 | | Vrms |
| | SNR(A-weighted) | 0dB 1KHz | | 100 | | dB |
| | THD+N(P0=12mW) | 0dB 1KHz | | -81 | | dB |
| | DC Offset at load | 0dB 1KHz | | 2 | | mV |
| | **DAC to SPK signal on SPKOUTLP and SPKOUTLN(R=10KΩ)** | | | | | |
| | FScale Output Level | 0dB 1KHz | | 1.8 | | Vrms |
| | SNR(A-weighted) | 0dB 1KHz | | 102 | | dB |
| | THD+N | 0dB 1KHz | | -82 | | dB |
| | DC Offset at load | 0dB 1KHz | | 0.7 | | mV |
| | **DAC to LINEOUT signal on LINEOUTP and LINEOUTN(R=10KΩ)** | | | | | |
| | FScale Output Level | 0dB 1KHz | | 0.9 | | Vrms |
| | SNR(A-weighted) | 0dB 1KHz | | 98 | | dB |
| | THD+N | 0dB 1KHz | | -81 | | dB |
| | DC Offset at load | 0dB 1KHz | | 0.5 | | mV |
| **ADC Input Path Performance** | **MIC1 /2/3to ADC via ADC mixer** | | | | | |
| | FScale Input Level | 0dB Gain 1KHz | | 0.5 | | Vrms |
| | SNR(A-weighted) | -1dB 1KHz, 0dB Gain | | 96 | | dB |

| | | | | | | |
|---|---|---|---|---|---|---|
| | THD+N | -1dB 1KHz, 0dB Gain | | -85 | | dB |
| | SNR(A-weighted) | 30mV,1KHz, 30dB Gain | | 81 | | dB |
| | THD+N | 30mV,1KHz, 30dB Gain | | -76 | | dB |
| | SNR(A-weighted) | 30mV,1KHz, 39dB Gain | | 81 | | dB |
| | THD+N | 30mV,1KHz, 39dB Gain | | -76 | | dB |
| | SNR(A-weighted) | 10mV,1KHz, 48dB Gain | | 73 | | dB |
| | THD+N | 10mV,1KHz, 48dB Gain | | -72 | | dB |
| | **LINEIN to ADC via ADC mixer** | | | | | |
| | FScale Input Level | 0dB 1KHz | | 0.9 | | Vrms |
| | SNR(A-weighted) | 1KHz | | 93 | | dB |
| | THD+N | 1KHz | | -85 | | dB |
| | Crosstalk（L/R） | 1KHz | | -85/-85 | | dB |
| | **AXIIN to ADC via ADC mixer** | | | | | |
| | FScale Input Level | 0dB 1KHz | | 0.9 | | Vrms |
| | SNR(A-weighted) | 1KHz | | 92 | | dB |
| | THD+N | 1KHz | | -82 | | dB |
| | Crosstalk（L/R） | 1KHz | | -88/-88 | | dB |
| **Bypass Path Performance** | **MIC1/2/3 to Headphone via output mixer** | | | | | |
| | FScale Input Level | 0dB Gain 1KHz | | 0.5 | | Vrms |
| | SNR(A-weighted) | -1dB 1KHz, 0dB Gain | | 98 | | dB |
| | THD+N | -1dB 1KHz, 0dB Gain | | -91 | | dB |
| | SNR(A-weighted) | 30mV,1KHz, 30dB Gain | | 83 | | dB |
| | THD+N | 30mV,1KHz, 30dB Gain | | -78 | | dB |
| | SNR(A-weighted) | 30mV,1KHz, 39dB Gain | | 83 | | dB |
| | THD+N | 30mV,1KHz, 39dB Gain | | -79 | | dB |
| | SNR(A-weighted) | 10mV,1KHz, 48dB Gain | | 74 | | dB |
| | THD+N | 10mV,1KHz, 48dB Gain | | -73 | | dB |
| | **LINEIN to Headphone via output mixer** | | | | | |
| | FScale Input Level | 0dB 1KHz | | 1 | | Vrms |
| | SNR(A-weighted) | -1dB 1KHz | | 98 | | dB |
| | THD+N(-1dBFS) | -1dB 1KHz | | -92 | | dB |
| | Crosstalk（L/R） | -1dB 1KHz | | -89/-89 | | dB |
| | **AXIIN to Headphone via output mixer** | | | | | |
| | FScale Input Level | 0dB 1KHz | | 1 | | Vrms |
| | SNR(A-weighted) | -1dB 1KHz | | 102 | | dB |
| | THD+N(-1dBFS) | -1dB 1KHz | | -93 | | dB |
| | Crosstalk（L/R） | -1dB 1KHz | | -88/-88 | | dB |

# 10.    Typical Power Consumption

Default Test Conditions:

LDOIN=CPVDD=1.5V,AVCC=3.0V,VCC-IO1=VCC-IO2=1.8V,VCC-RTC=3.0V

| OPERATING MODE | TEST CONDITIONS | LDOIN | AVCC | VCC-IO1 | VCC-IO2 | CPVDD | VCC-RTC |
|---|---|---|---|---|---|---|---|
| **RTC only** | | | | | | | |
| LDO enabled XTAL enabled | LDOIN,VCC-RTC supplies, 32.768KHz clock, three output enable | 1.8V | 3V | 1.8V | 3V | 1.8V | 3V |
| | | 0uA | 0uA | 0uA | 0uA | 0uA | 12uA |
| **Standby** | | | | | | | |
| LDO enabled XTAL enabled | All supplies present, No clocks supply, Default register settings | 1.8V | 3V | 1.8V | 3V | 1.8V | 3V |
| | | 73uA | 62uA | 0uA | 0uA | 0uA | 12uA |
| **Music Playback to Headphone(32Ω load)** | | | | | | | |
| AIF1 to DAC to HPOUT(stereo) | fs=44.1KHz, SYSCLK=MCLK=24.576MHz, 24bit I2S,Slave mode | 1.8V | 3V | 1.8V | 3V | 1.8V | 3V |
| | | 1.5mA | 4.1mA | 0.013mA | 0mA | 2.4mA | 12uA |
| **Voice record to AIF1** | | | | | | | |
| MIC1 to ADC to AIF1(mono) | fs=44.1KHz, SYSCLK=MCLK=24.576MHz, 24bit I2S,Slave mode | 1.8V | 3V | 1.8V | 3V | 1.8V | 3V |
| | | 1.4mA | 4.5mA | 0.023mA | 0mA | 0mA | 12uA |
| **Analog-Analog Voice Path (eg. Analog Voice call)** | | | | | | | |
| Mic1 to Lineout, Linein to Hp, | fs=8 kHz, SYSCLK=MCLK=24.576MHz | 1.8V | 3V | 1.8V | 3V | 1.8V | 3V |
| | | 0.75mA | 4.1mA | 0mA | 0mA | 2.0mA | 12uA |

# 11.  Function Description

## 11.1.  Power

There are a Power-Reset circuit in AC100 uesed to reset all the circuit and register to a standby state after power up. The Power-Reset circuit make all the supply power need no specific timing. All the supply voltages are illustrated in the below figure.
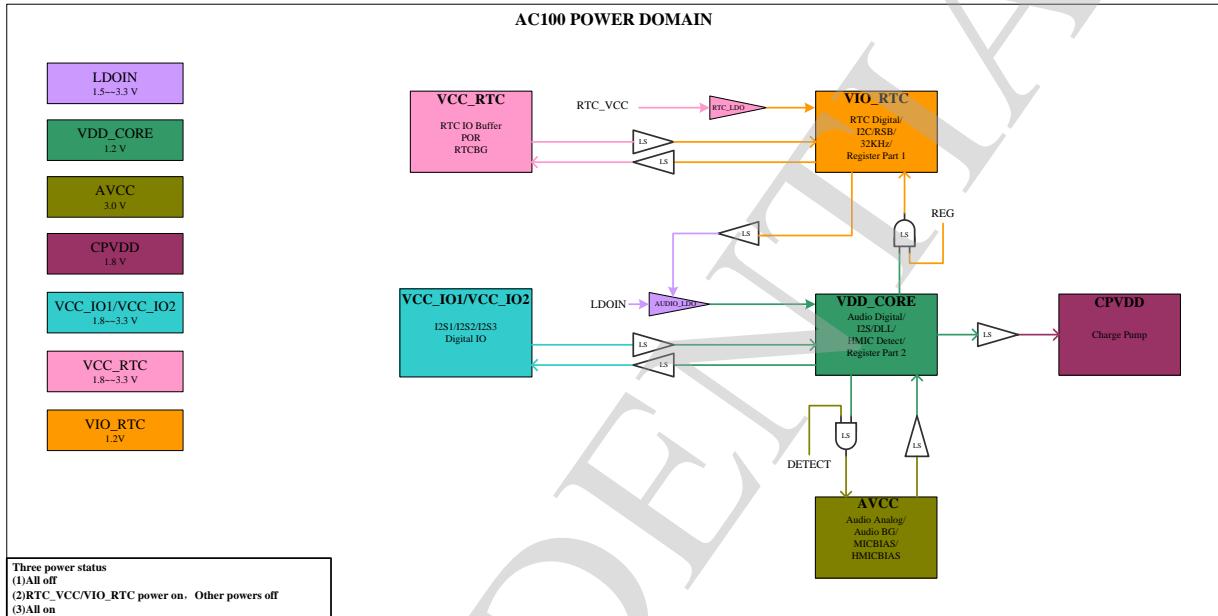


**Figure 5    Power Management**

VDD-CORE is 1.2V for audio digital core power generated from LODIN pin, which also can be direct supplied from VDD-CORE pin. VDD-IO1 is digital I/O power for I2S1 and I2S2. VDD-IO2 is digital I/O power for I2S3. AVCC is for analog power. CPVDD for charge pump power. VIO-RTC is RTC digital core power generated from VCC-RTC.

When the AC100 is not working, it need to set the supply properly to prevent power leakage. There are two settings to select. It's best to power off all the supply. The other is to make sure AVCC and CPVDD both power on.

At the setting below, AC100 has the best performance.

| LDOIN | VDD_CORE | AVCC | CPVDD | VCC-IO1 | VCC-IO2 | VCC_RTC | VIO_RTC |
|---|---|---|---|---|---|---|---|
| 1.5~~3.3 V | 1.2 V | 3 V | 1.8 V | 1.8/3.3 V | 1.8/3.3 V | 1.8/3.3 V | 1.2 V |
| Supplied | N/A | Supplied | Supplied | Supplied | Supplied | Supplied | N/A |

\* VDD_CORE and VIO_RTC generated by internal LDO.

## 11.2.    Clock

The system clock(SYSCLK) of AC100 must be 512*fs(fs=48KHz or 44.1KHz). So the system should arrange the divider to generate 24.576MHz for audio clock series of 48KHz or 22.5792MHz for series of 44.1KHz.

SYSCLK can be selected from I2S1CLK or I2S2CLK which derived from MCLK1, MCLK2 or PLL. MCLK1 and MCLK2 are always provided externally while the PLL reference clock can be select from MCLK1, MCLK2, BCLK1, BCLK2.

I2S1CLK is the reference of the first I2S clocking zone. I2S2CLK is the reference of the second I2S clocking zone. The third I2S only support master mode. Its clocking zone must be synchronized with either of the I2SnCLK(n=1,2). In master mode, LRCK and BCLK are derived internally from I2SnCLK. In slave mode, LRCK and SCLK are supplied externally and BCLK can be used as the PLL input reference.

SYSCLK is the reference of ADC, DAC, DVC, MIXER, AGC and DRC module. If SRC1 or SRC2 is used, SYSCLK must be set by PLL, then the SRCnCLK is auto provided for SRC module. If all the relevant module above is not used, the SYSCLK needn't be configured.

There are also an internal Oscillator to generate a clock signal for direct-path mode. In this mode, the oscillator supply clock to charge pump, adjustment circuit, headphone detect circuite.g... In direct-path case, no external clock need .

# AC100 CLOCK SYSTEM

SRC1CLK — SRC1

SRC2CLK — SRC2

ADCCLK — ADC_DIGITAL

DACCLK — DAC_DIGITAL

AGCCLK — HPF & AGC

DRCCLK — HPF & DRC

MUX — SYSCLK — DVCCLK — DVC/MIXER

MCLK1
MCLK2
BCLK1
BCLK2

MUX — DPLL

MUX — I2S1CLK — ACLK1 — AIF1_BCLK/LRCK_CTL — MUX — BCLK1A — AIF1_TX/RX

MUX — I2S2CLK — ACLK2 — AIF2_BCLK/LRCK_CTL — MUX — BCLK2A — AIF2_TX/RX

MUX — ACLK3 — AIF3_BCLK/LRCK_CTL — MUX — BCLK3A — AIF3_TX/RX

ADDA

CKAM

REGISTER PART 1 — REGISTER PART 2/ HMICBIAS DETECT

WCLK

TWI/RSB — RTC OSC — CK32K — RTC/ CK32K OUTPUT

SCK

X32KI

**Figure 6    Clocking Management**

## 11.3.   PLL

A Phase-Locked Loop(PLL) is used to provide a flexible input clock range from 128KHz to 24MHz. The source of the PLL can be set to MCLK1, MCLK2, BCLK1 or BCLK2 by setting register. The PLL output is always used to provide the system clock(SYSCLK) of AUDIO codec when 24.576MHz or 22.5792MHz can not be provided from MCLK.

The PLL transmit formula as below:

$$\text{FOUT} = (\text{FIN} * N) / (M * (2K+1)) ; \qquad (N = N\_i + 0.2 * N\_f)$$

**Table 1    clock setting for SYSCLK=24.576 MHz**

| FIN | M | N | K | FOUT |
|---|---|---|---|---|
| 128K | 1 | 576 | 1 | 24.576M |
| 192K | 1 | 384 | 1 | 24.576M |
| 256K | 1 | 288 | 1 | 24.576M |
| 384K | 1 | 192 | 1 | 24.576M |
| ... | .... | ... | 1 | 24.576M |
| 6M | 25 | 307.2 | 1 | 24.576M |
| 13M | 42 | 238.2 | 1 | 24.576M |
| 19.2M | 25 | 96 | 1 | 24.576M |

**Table 2    clock setting for SYSCLK=22.5792 MHz**

| FIN | M | N | K | FOUT |
|---|---|---|---|---|
| 128K | 1 | 529.2 | 1 | 22.5792M |
| 192K | 1 | 352.8 | 1 | 22.5792M |
| 256K | 1 | 264.6 | 1 | 22.5792M |
| 384K | 1 | 176.4 | 1 | 22.5792M |
| ... | .... | ... | 1 | 22.5792M |
| 6M | 38 | 429 | 1 | 22.5789M |
| 13M | 19 | 99 | 1 | 22.5789M |
| 19.2M | 25 | 88.2 | 1 | 22.5792M |

## 11.4. TWI/RSB Interface

AC100 can support two series control interface protocol for writing to or readback from registers on SCK and SDA pins . One is TWI interface, the other is RSB interface. RSB is top-priority for higher efficiency and lower power consumption.

### 11.4.1. TWI Interface

TWI is a 2-wire (SCK/SDA) half-duplex serial communication interface, supporting only slave mode. SCK is used for clock and SDA is for data. SCK clock supports up to 400 KHz rate and SDA data is a open drain structure.

A master controller initiates the transmission by sending a "start" signal, which is defined as a high-to-low transition at SDA while SCK is high. The first byte transferred is the slave address. It is a 7-bit chip address followed by a R/W bit. The chip address must be 0011010x. The R/W bit indicates the slave data transfer direction. Once an acknowledge bit is received, the data transfer starts to proceed on a byte-by-byte basis in the direction specified by the R/W bit. The master can terminate the communication by generating a "stop" signal, which is defined as a low-to-high transition at SDA while SCK is high.
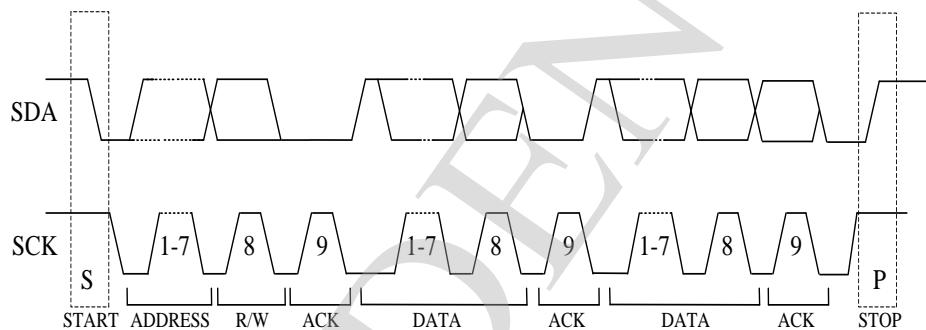


**Figure 7　TWI Interface**

The formats of "write" and "read" instructions are shown in below.
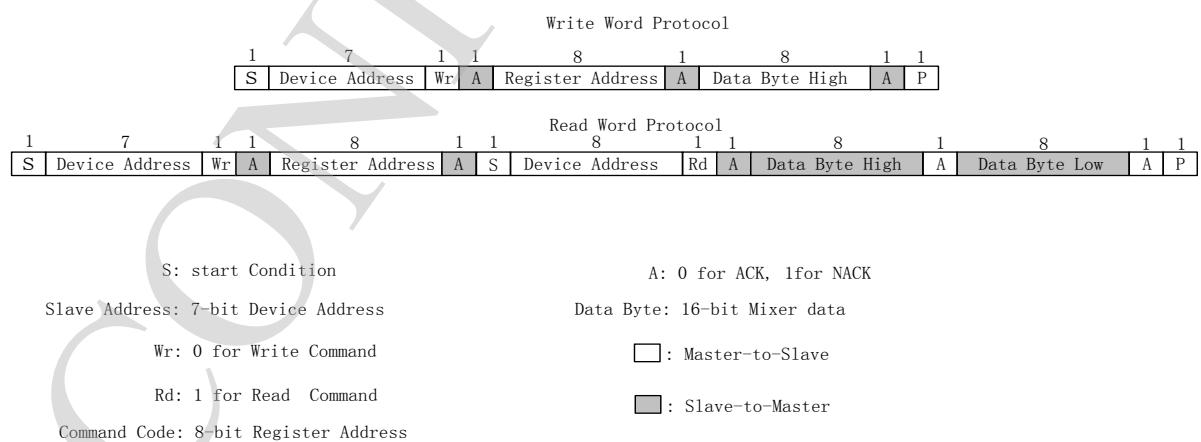


**Figure 8　TWI Read and Write**

## 11.4.2. RSB Interface

RSB interface supports a special protocols with a simplified two wire protocol on a push-pull bus. So the transfer speed can be up to 10MHz and the performance will be improved much. AC100 works only in slave mode.

RSB support multi-slaves. It uses CK as clock and uses CD to transmit command and data.the Bus Topology is showed below:
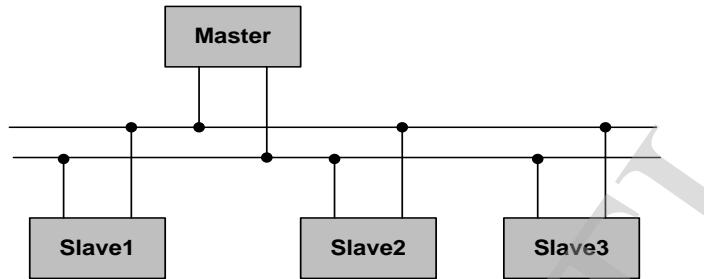
**Figure 9    RSB Bus Topology**

The start bit marks the beginning of a transaction with the slave device.When CK is high, a change from high to low on CD is defined as a start condition. This start condition notifies the selected device to start a transfer.
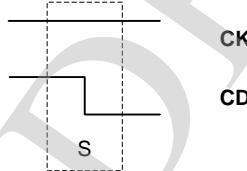
**Figure 10    Start signal**

RSB protocol uses parity bit to check the correction of every byte,The checked object is the 7, 8 or 15 bit in front of the parity bit.
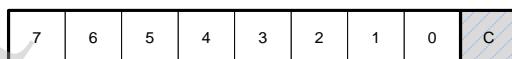
**Figure 11    Parity bit**

ACK bit is the acknowledgement from device to host, The ACK is active low. When device finds the parity bit is error, it will not send ACK to host, so host can know that an error happens in the transaction.

Set run-time slave address(RTSADDR) command. It is used to set run time slave address(RTSADDR) for different devices in the same system. There are 15 devices in a system at most. The RTSADDR can be selected from the command code set and a device 's RTSADDR can be modified many times by using set run-time slave address command.

| 1 | 7 | 1 | 15 | 1 | 7 | 1 | 2 | 1 | 2 |
|---|---|---|---|---|---|---|---|---|---|
| S | 0x74 | C | SADDR | C | RTSADDR | C | HD | A | DH |

HOST
Device

**Figure 12   RTSADDR command**

Read command is used to read data from device.It has byte,half word and word operation.When devices receives the command,they shall check if the command's RTSADDR matches their own RTSADDR.The device's RTSADDR is setted by set run-time slave address(RTSADDR) command.

| 1 | 7 | 1 | 7 | 1 | 8 | 1 | 2 | 8 | 1 | 8 | 1 | 2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | 0x45,0x4E,0x53 | C | RTSADDR | C | DADDR | C | HD | DATA0 | C | ... DATA n | C | DH |

len = 1,2,4

HOST
Device
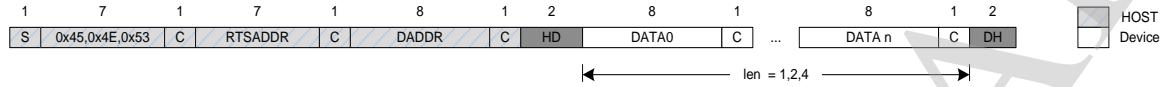
**Figure 13   Read command**

Write command is used to write data to the devices.It has byte,half word and word operation.When devices receive the command,they shall check if the command's RTSADDR matches their own RTSADDR.The device's RTSADDR is setted by set run-time slave address(RTSADDR) command.

| 1 | 7 | 1 | 7 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 2 | 1 | 2 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | 0x27,0x2c,0x31 | C | RTSADDR | C | DADDR | C | DATA0 | C | ... DATA n | C | HD | A | DH |

len = 1,2,4

HOST
Device
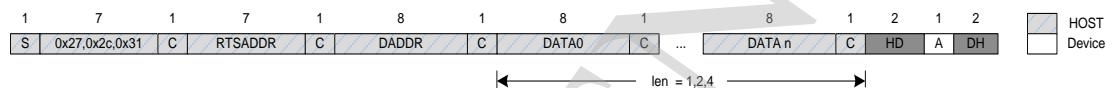
**Figure 14   Write command**

## 11.5. I2S/PCM Interface

There are three I2S/PCM interfaces which can be configured as master mode or slave mode in AC100. The three I2S/PCM interfaces provide flexible connectivity with multiple processors (e.g. Application processor, Baseband processor and Wireless transceiver ).

Interface I2S1 and I2S2 can be configured as Master or Slave, the third interface I2S3 operates in Master mode and supports PCM mode only.

In the general case, the digital audio interface uses four pins as below:

- BCLK: Bit clock for data synchronization
- LRCK: Left/Right data alignment clock
- SDOUT: output data for ADC data
- SDIN: input data for DAC data

I2S1 and I2S2 audio interface support four different data formats as below. But I2S3 supports PCM short mode only. On the first digital audio interface I2S1, TDM is available for all four farmart and AC100 can use it to transmit or receive up to four channel data on timeslot0 and timeslot1 simultaneously.

- I2S mode
- Left justified mode
- Right justified mode
- PCM short mode
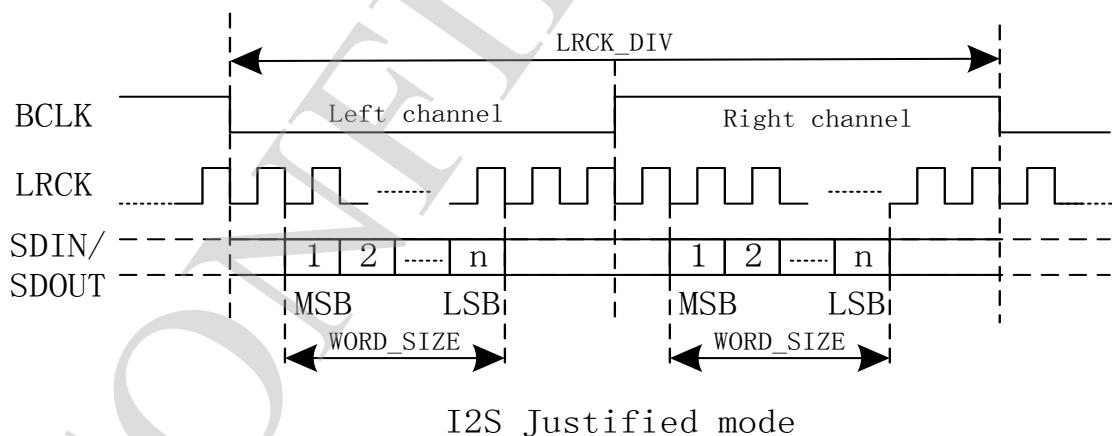


**Figure 15    I2S Justified mode**

Left Justified mode
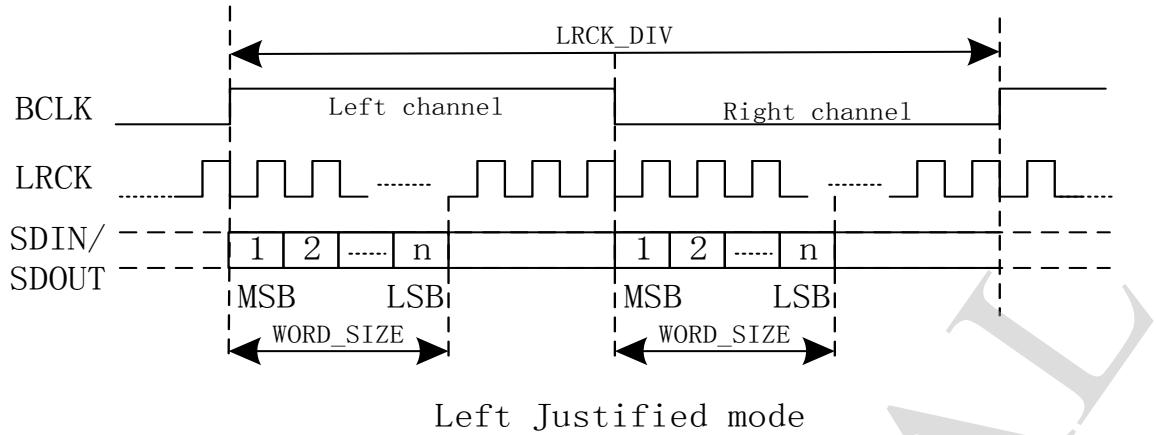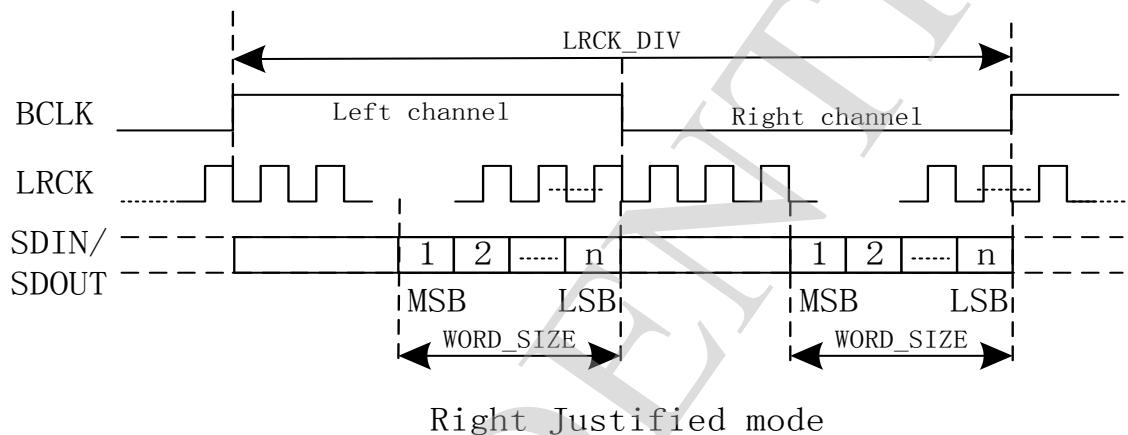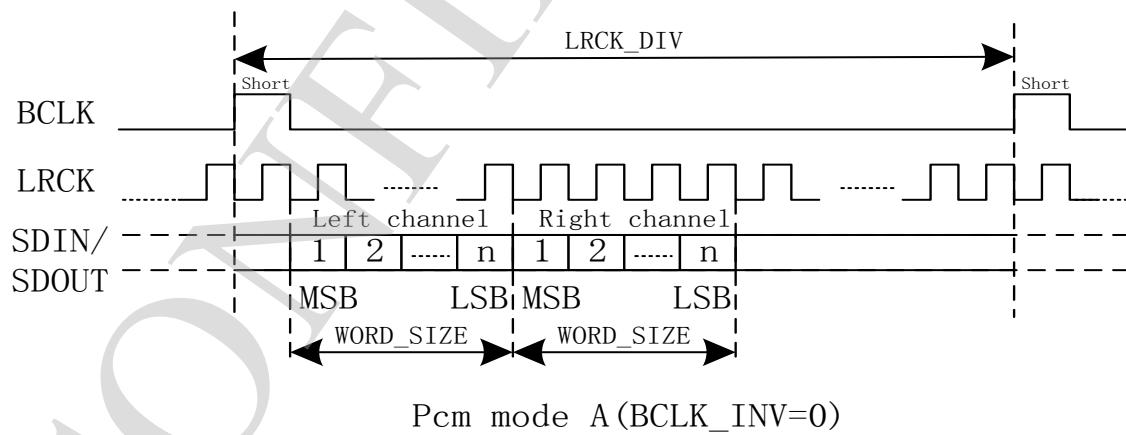
**Figure 16　Left Justified mode**



Right Justified mode

**Figure 17　Right Justified mode**



Pcm mode A(BCLK_INV=0)

**Figure 18　Pcm mode A(LRCK_INV=0)**

Pcm mode B(BCLK_INV=1)
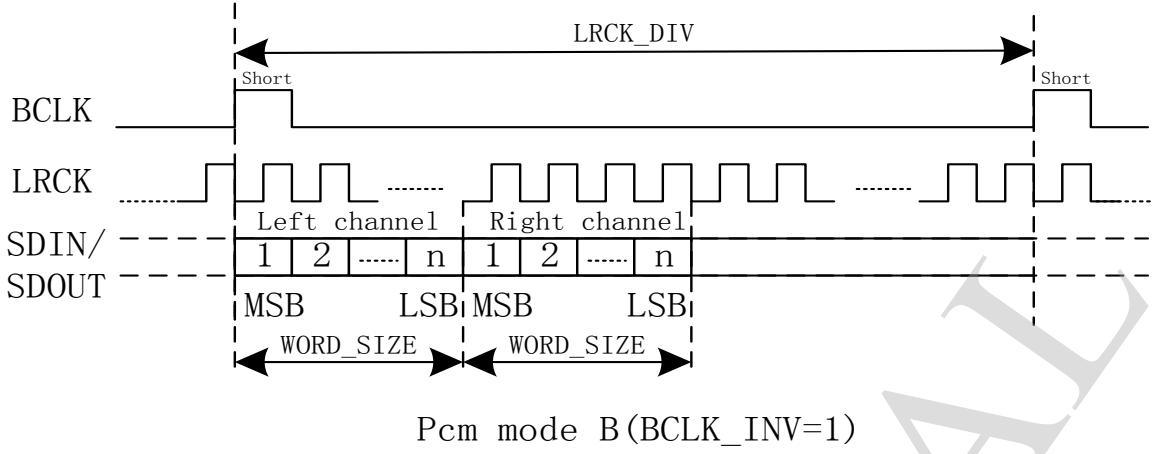
**Figure 19    Pcm mode B(LRCK_INV=1)**



Pcm mode A(BCLK_INV=0)
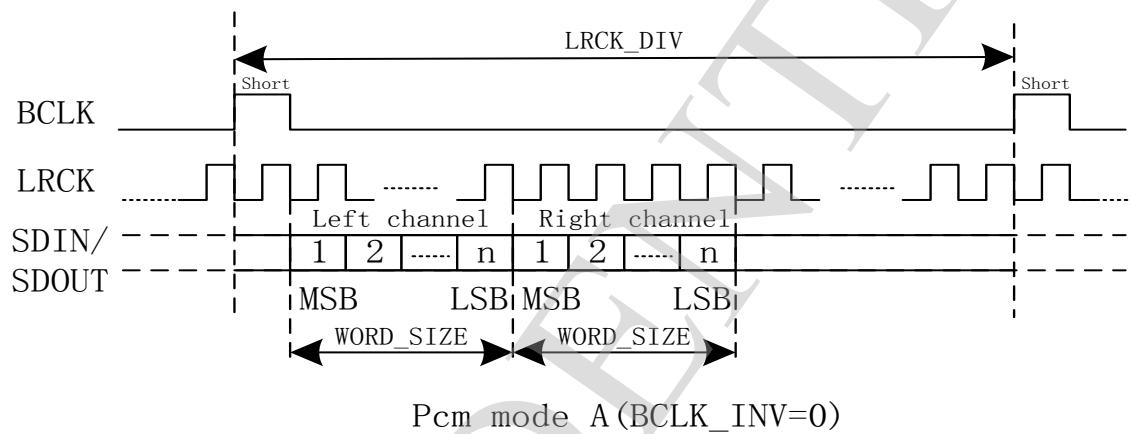
**Figure 20    Pcm mode A mono(LRCK_INV=0)**



Pcm mode B(BCLK_INV=1)
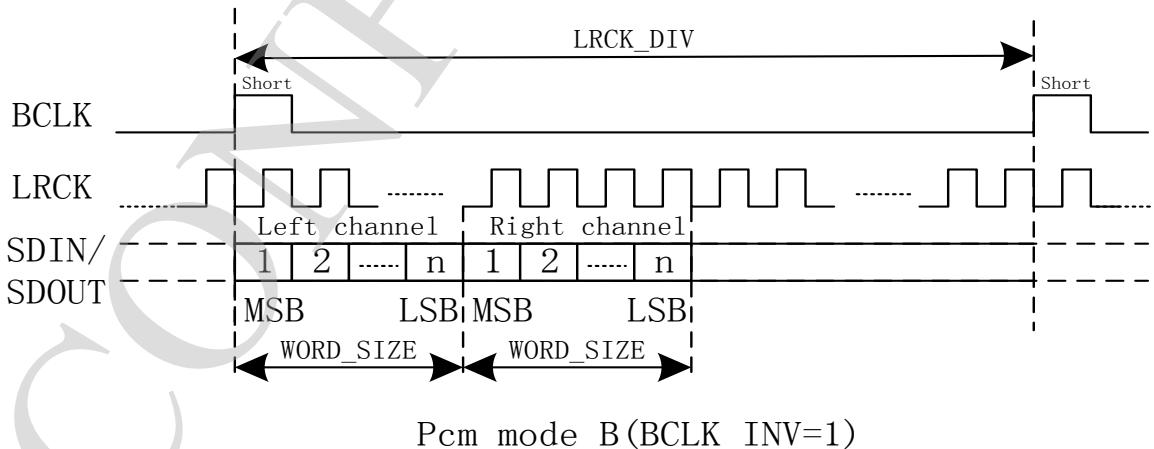
**Figure 21    Pcm mode B mono(LRCK_INV=1)**
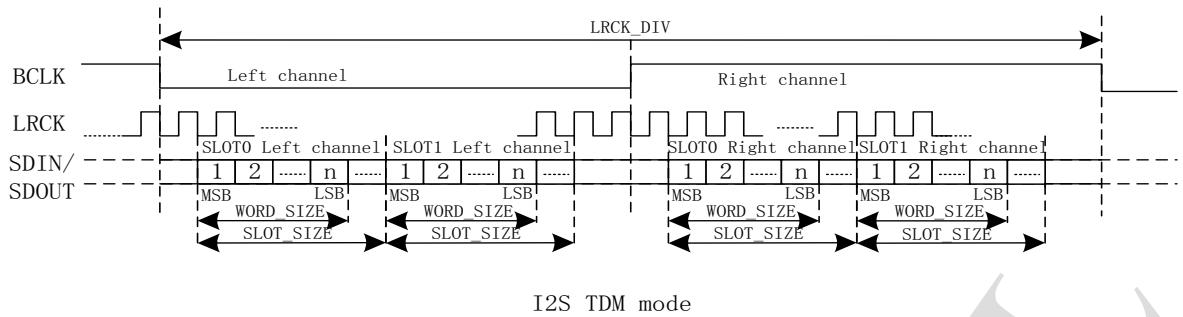
I2S TDM mode

**Figure 22　I2S TDM mode**
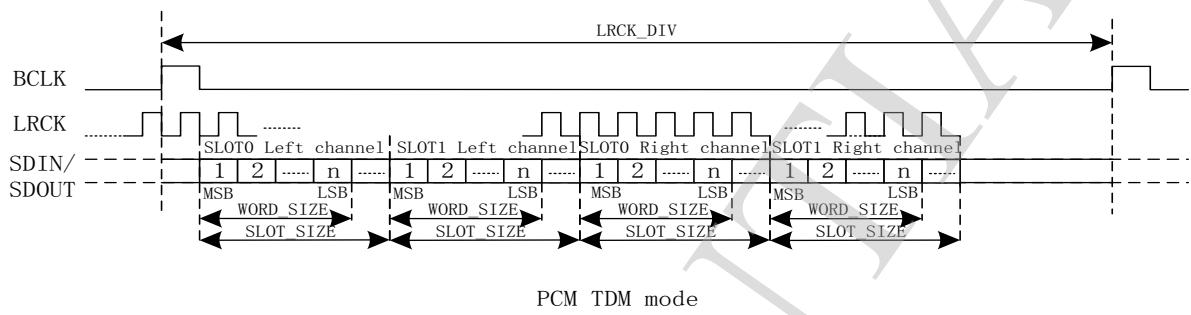


PCM TDM mode

**Figure 23　PCM TDM mode**

## 11.6.  Stereo ADC

The stereo ADC is used for recording stereo sound. The sample rate of the stereo ADC can not be independent of DAC sample rate. In other words, the stereo ADC and DAC must work at a same sample rate. The sample rate is configured by the register ADDA_FS_I2S1 or ADDA_FS_I2S2 depending on which I2SnCLK selected as the system clock(SYSCLK).

In order to save power, the left and right analog ADC part can be enabled/disabled separately by setting register ADC_APC_CTRL Bit15 & Bit11. The digital ADC part can be enabled/ disabled by ADC_DIG_CTRL Bit15.

The volume control of the stereo ADC is set via register ADC_APC_CTRL Bit14:12 & ADC_APC_CTRL Bit10:8.

## 11.7.  Stereo DAC

The stereo DAC sample rate is the same as the stereo ADC. The sample rate is configured by the register ADDA_FS_I2S1 or  ADDA_FS_I2S2 depending on which I2SnCLK selected as the system clock(SYSCLK).

In order to save power, the left and right DAC can be enabled/disabled separately by setting register OMIXER_DACA_CTRL Bit15:14. The digital DAC part can be enabled/ disabled by DAC_DIG_CTRL Bit15.

## 11.8.  Mixer

The Codec supports three series of mixers for all function requirements:

- 2 channels DAC Output mixers
- 2 channels ADC Record mixers
- Digital mixers

### 11.8.1.  DAC Output Mixers
The output mixer is used to drive analogut output, including headphone, earpiece, speaker,lineout. The following signals can be mixed into the output mixer:

- LINEINL/R
- AXIL/R
- MIC1P/N,MIC2P/N
- Stereo DAC output

### 11.8.2.  ADC Record Mixers
The ADC record mixer is used to mix analog signals as input to the Stereo ADC for recording. The following signals can be mixed into the output mixer:

- LINEINL/R
- AXIL/R

- MIC1P/N,MIC2P/N
- Stereo DAC output

### 11.8.3. Digital Mixers

The digital mixers are provided for digital audio data mixing on four I2S1 output paths, two I2S2 output paths and two paths to the stereo DAC. It's separately controlled by the register I2S1_MXR_SRC, I2S2_MXR_SRC and DAC_MXR_SRC.

DATA PATH BLOCK DIAGRAM
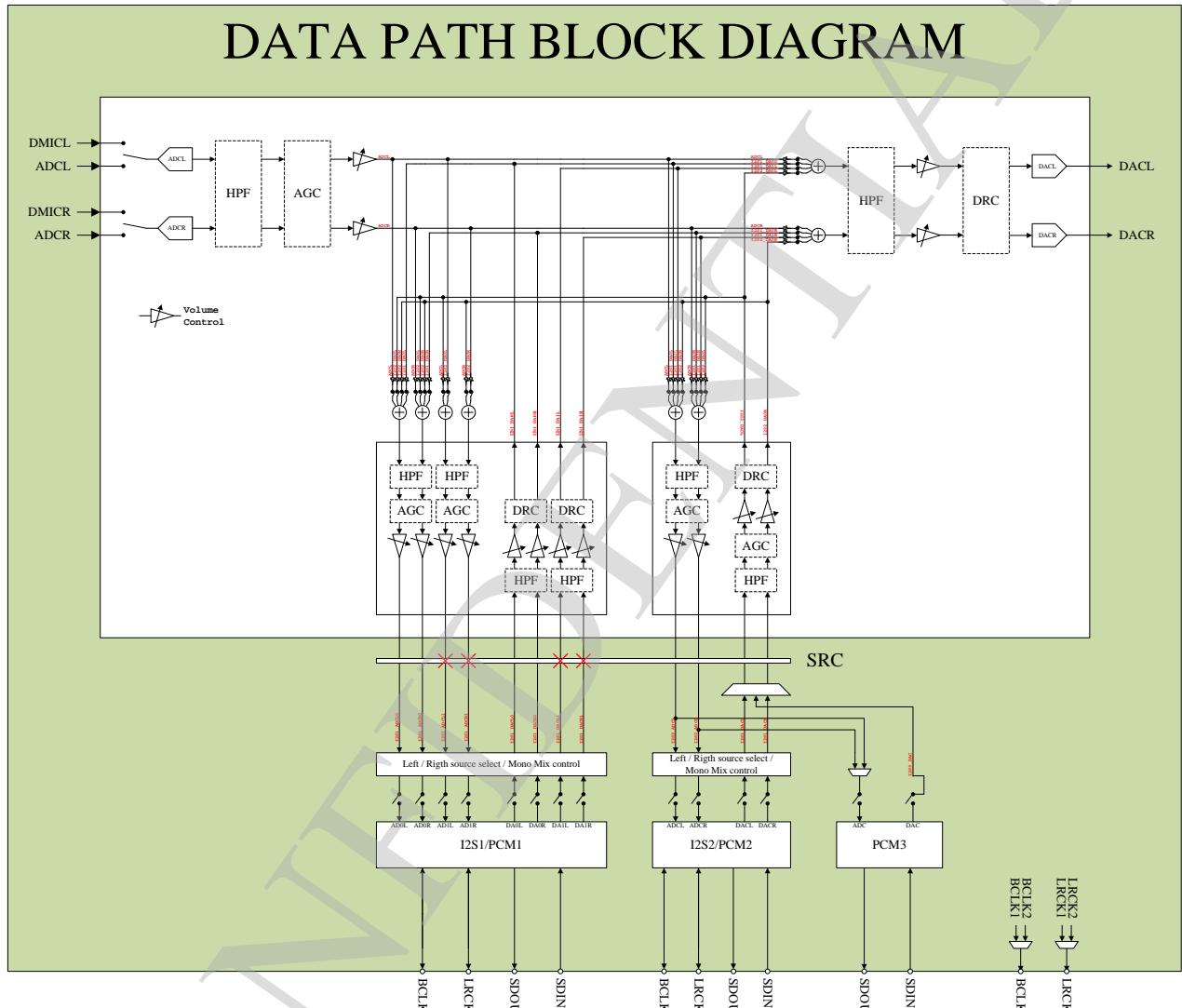
**Figure 24　Digital Data Path**

## 11.9. Analogue Audio Input Path

The Codec supports five Analogue Audio Input paths:

- LINEINL/R
- AXIL/R
- MIC1P/N,MIC2P/N,MIC3P/N

### 11.9.1. Microphone Input

MICIN1P/N, MICIN2P/N, MIC3INP/N provide differential input that can be mixed into the ADC record mixer, or DAC output mixer. MICIN is high impedance, low capacitance input suitable for connection to a wide range of differential microphones of different dynamics and sensitive. There are only two microphone pre-amplifiers for the 3 differential microphone inputs. MICIN1P/N are input to the first pre-amplifier, MICIN2P/N & MICIN3P/N are selected to input the 2nd pre-amplifier by the register ADC_SRCBST_CTRL bit7. Each microphone preamplifier has a separate enable bit, ADC_SRCBST_CTRL Bit15 & Bit11. The gain for each pre-amplifer can be set independently using MIC1BOOST, MIC2BOOST. MBIAS provide reference voltage for electret condenser type(ECM) microphones.
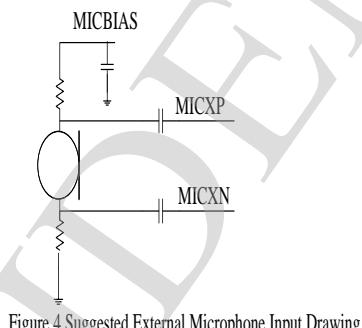


Figure 4 Suggested External Microphone Input Drawing

**Figure 25    Suggested External Microphone Input**

### 11.9.2. AXIL/R Input

Auxiliary inputs AXIL and AXIR provide 2-channel stereo single-ended input that can be mixed into the DAC output mixer and ADC record mixer. The inputs are high impedance and low capacitance, thus ideally suited to receiving line level signals from external audio equipment or audio FM module .

Both auxiliary inputs include programmable volume level adjustments and ADC input mute. The scheme is illustrated below. Passive RF and active Anti_Alias filters are also incorporated within the auxiliary inputs. These prevent high frequencies aliasing into the audio band , otherwise degrading performance.

The gain between the AXI inputs and the ADC is logarithmically adjustable from -9dB to 12dB in 1.5dB step by the register AXI_PREG set. The ADC Full Scale input is 1.0Vrms at AVCC =3.0volts. Any voltage greater than full scale will possibly overload the ADC and cause distortion. Note that the full scale input tracks directly with AVCC.
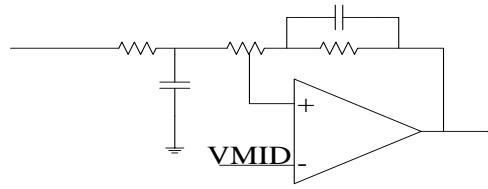
Figure 2 AXI input Schematic

**Figure 26    AXI Input Schematic**

### 11.9.3.  LINEINL/R Input

LINEINL/R provide one-channel mono differential input or stereo single-ended input that can be mixed into the ADC record mixer or the stereo output mixer. The inputs are suited to receiving line level signals such as external audio equipment or baseband module .

When the linein input is set as differential signal input LINEINL-LININR to the ADC or to DAC mixer, the linein gain is logarithmically adjustable from -9dB to 12dB in 1.5dB step by the register LINEIN_DIFF_PREG set.

## 11.10. Analogue Audio Output Path

The Codec supports five Analogue Audio Output paths:

- HPOUTL/R, HPOUTFB
- SPOLP/N
- SPORP/N
- EAROUTP/N
- LINEOUTP/N

### 11.10.1. Headphone Output

HPOUTL/R provides two-channel single-ended output to headphone driver. The HPOUTL/R PA input source can be selected from output mixer or directly from DAC by register HPOUT_CTRL Bit15 & Bit14 set. It also can be muted by register HPOUT_CTRL Bit13 & Bit12 set. The headphone PA power up or down by register HPOUT_CTRL Bit11 set.

HPOUTL/R can drive a 16R or 32R headphone load without DC capacitors by using Charge Pump to generate the negative rails. HPOUTFB is the ground loop noise rejection feedback. HBIAS provides reference voltage for electret condenser type(ECM) microphones. Audio jack insert/ button press detection function is also provided through measuring the HBIAS current.
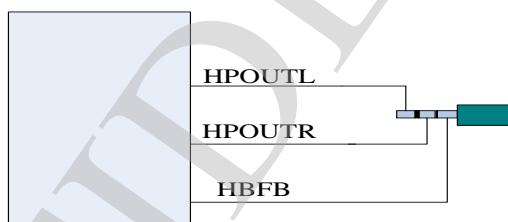


**Figure 27    Suggested Headphone Output Application**

HPOUTL/R volumes can be independently adjusted under software control using the HP_VOL[5:0] of the headphone output control registers. The adjustment is logarithmic with an 64dB rang in 1dB step from 0dB to -62dB. The headphone outputs can be muted by writing codes 0x0 to HP_VOL[5:0] bits.

There are a DC offset cancellation circuit to remove the headphone output DC offset for preventing POP noise in AC100. The function can be enabled or disabled by the register HP_DCRM_EN.   This bit must be set 0xf before headphone PA enabled, and this bit must be set 0x0 before headphone PA disabled.

A zero cross detect circuit is provided at the input to the headphones under the control of the ZCROSS_EN bit . Using these controls the volume control values are only updated when the input signal to the gain stage is close to the analogue ground level. This minimizes and audible clicks and zipper noise as the gain values are changed or the device muted.

### 11.10.2. Earpiece Output

EAROUTP/N provides one differential output to drive handset receiver. The EAROUTP/N input source can be selected from left DAC, right DAC, left output mixer or right output mixer. The earpiece volume

controlled by the register ERPOUT_CTRL Bit4:0 set. The volume control is logarithmic with an 43.5dB rang in 1.5dB step from -43.5dB to 0dB. The earpiece PA power up or down by register ERPOUT_CTRL Bit5set.

### 11.10.3. Speaker Output

SPOLP/N, SPORP/N provides two differential output without internal speaker amplifier. Using external amplifier, a stereo speakers can be implemented. The SPOLP/N input source can be selected from left output mixer or (left+right) output mixer. The SPORP/N input source can be selected from right output mixer or (left+right) output mixer. So in mono speaker application, The best choice for SPOLP/N or SPORP/N input source is selected from (left+right) output mixer avoiding sound loss. The volume control is logarithmicwith an 43.5dB rang in 1.5dB step from -43.5dB to 0dB. The left and right speaker output buffer can independently power up or down by register SPKOUT_CTRL Bit11 & Bit7 set.

### 11.10.4. Line Output

LINEOUTP/N provides one differential BTL output to drive line level signals to external audio equipment or baseband module .The LINEOUTP/N input source can be selected from MIC1 pre-amplifier output, MIC2 pre-amplifier output, left output mixer or right output mixer. The volume control is logarithmic with an 10.5dB rang in 1.5dB step from -4.5dB to 6dB. The LINEOUT output buffer power up or down by register LOUT_CTRL Bit4 set.

# 11.11. Digital Microphone Interface

AC100 supports a stereo digital micriphone interface. The DMICCLK/ DMICDAT pins are multiplexed on the MIC3P/MIC3N pins. The circuit share decimation filter with audio ADC. And DMICCLK can be output 128fs (fs= ADC sample rate).

Digital Microphone power usually falls between the range 1.6V-3.6V, typical 1.8V. And the Clock frequency is between the the range 1.0MHz-3.25MHz, typical 2.4MHz.

Digital Microphone Block Diagram as below:
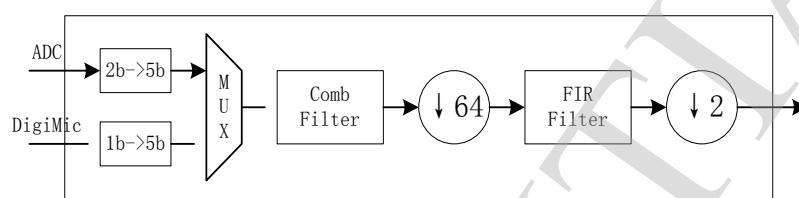


**Figure 28    Digital Microphone Block Diagram**

Digital Microphone timing as below:
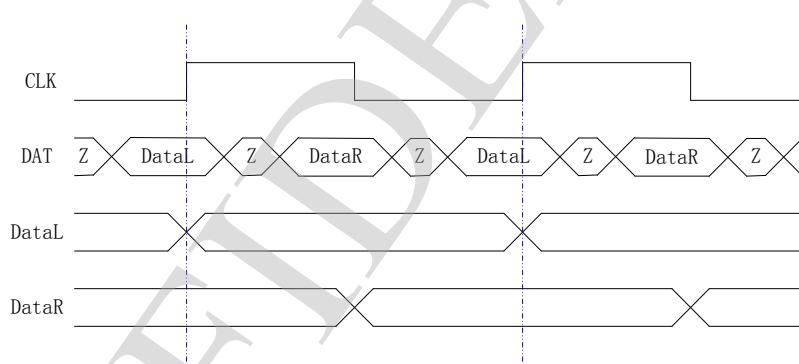


**Figure 29    Digital Microphone timing**

Digital Microphone application as below:
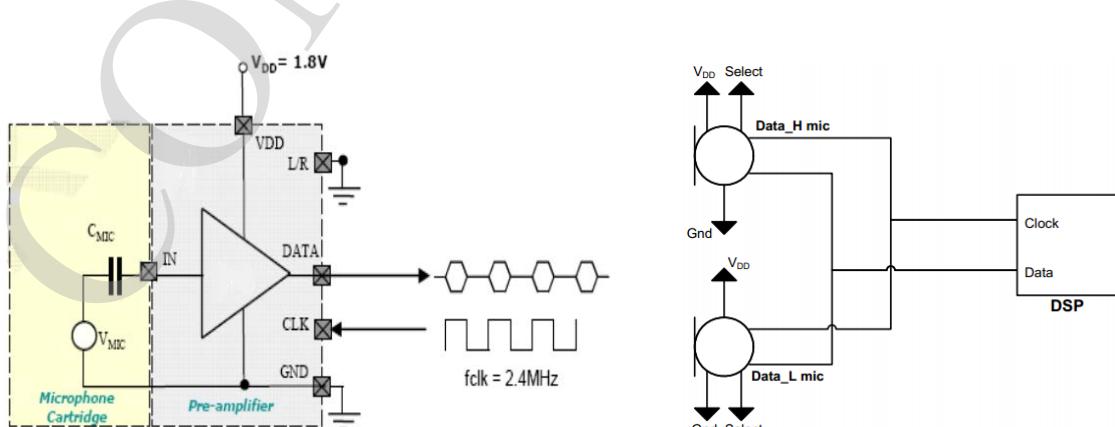


**Figure 30    Digital Microphone Application**

## 11.12. Audio Jack Detect

The microphone bias output pin HBIAS provide a low noise reference voltage suitable for biasing electrets type microphones and the associated external resistor biasing network. Hbias is designed to drive headset microphone, and a bias current detect function is provided for external accessory detection by measuring the Hbias current. In some application, it's used to detect the insertion/removal of a aduio jack and the button press. These events will cause a significant change in bias current flow, which can be detected and used to generate a signal to the processor.

When HBIAS current detect is enabled, 5 bit ADC will send out sample data at 16/32/64/128Hz clock rate. Digital logic trigger an interrupt event controlled by register setting when the data is changed.

The digital circuit generate five IRQ signals that can be disabled by register, the data from ADC can be read from register HMIC_STATUS Bit12:8.

IRQ Timing Diagram:
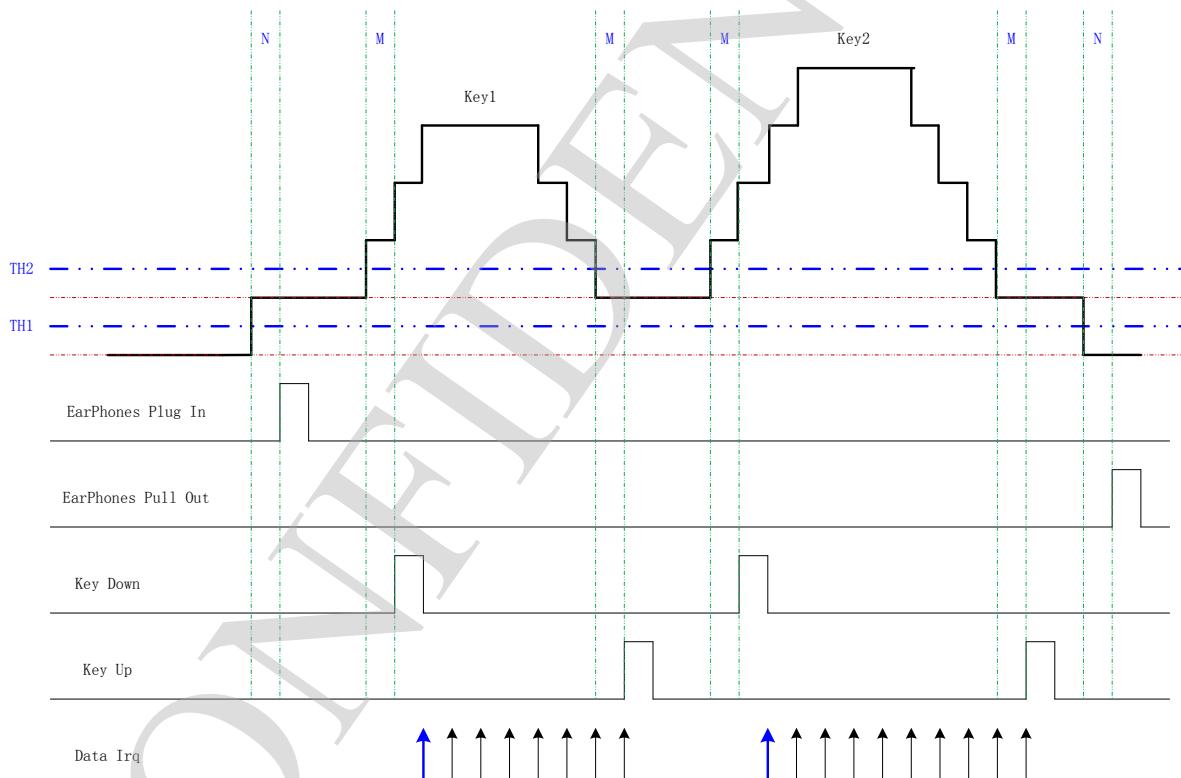


**Figure 31    HBIAS Detect IRQ Timing Diagram**

## 11.13. Interrupt

The Interrupt circuits in ac100 generate an Interrupt (IRQ) event to enable the detection of audio jack status. The Interrupt pin IRQ_AUDIO is open-drain. It's usually drives a high level voltage via the external pull-up resistor while it output a low level when the IRQ is active.

It supports the following triggered events illustrated in the figure below:
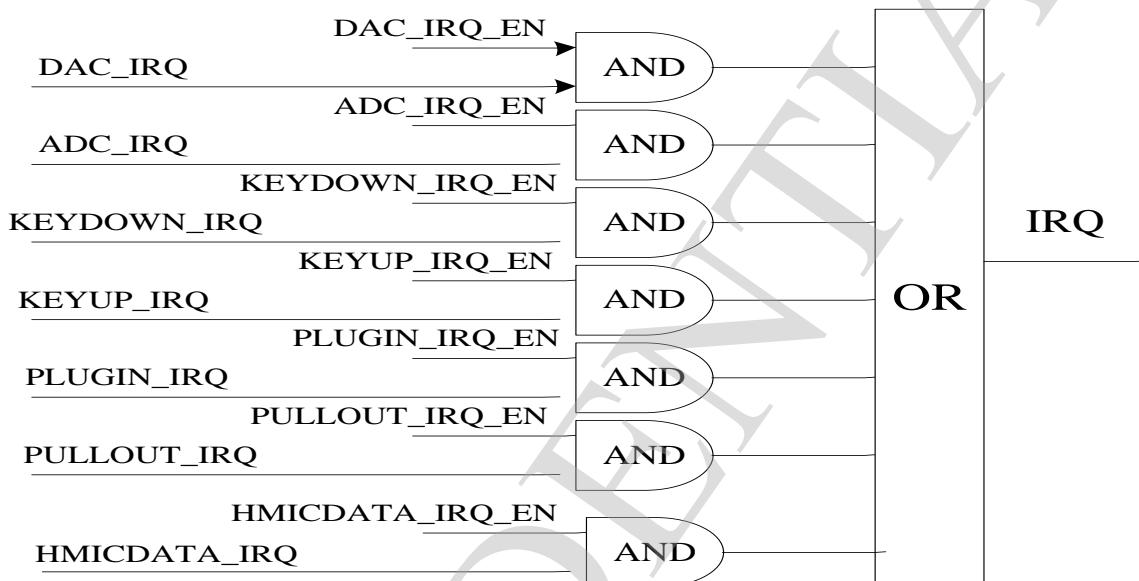


**Figure 32    Interrupt trigger Diagram**

## 11.14. Digital Audio Process for ADC

The DAP System Block Diagram For ADC.
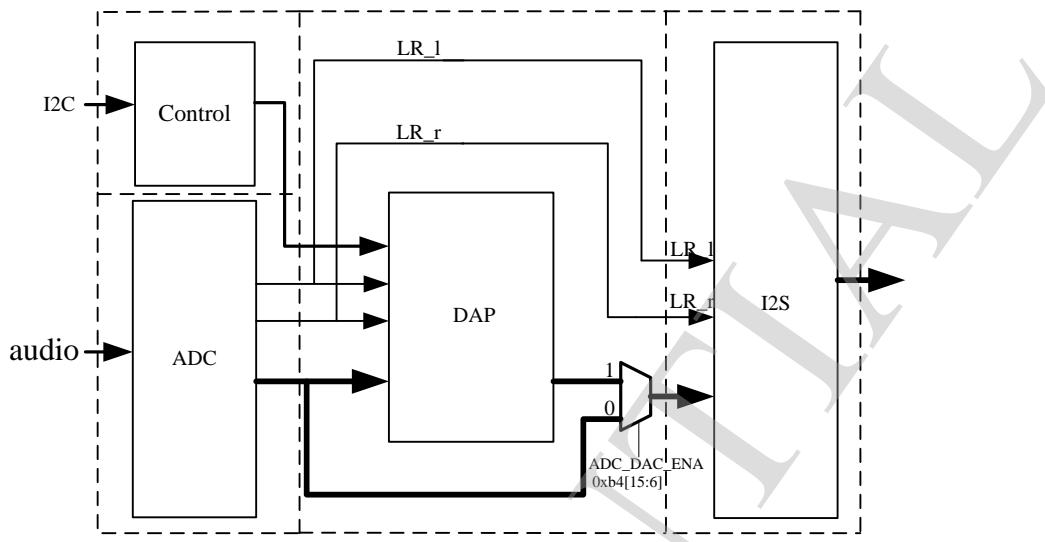


**Figure 33    ADC DAP System Block**

DAP for ADC Data Flow:
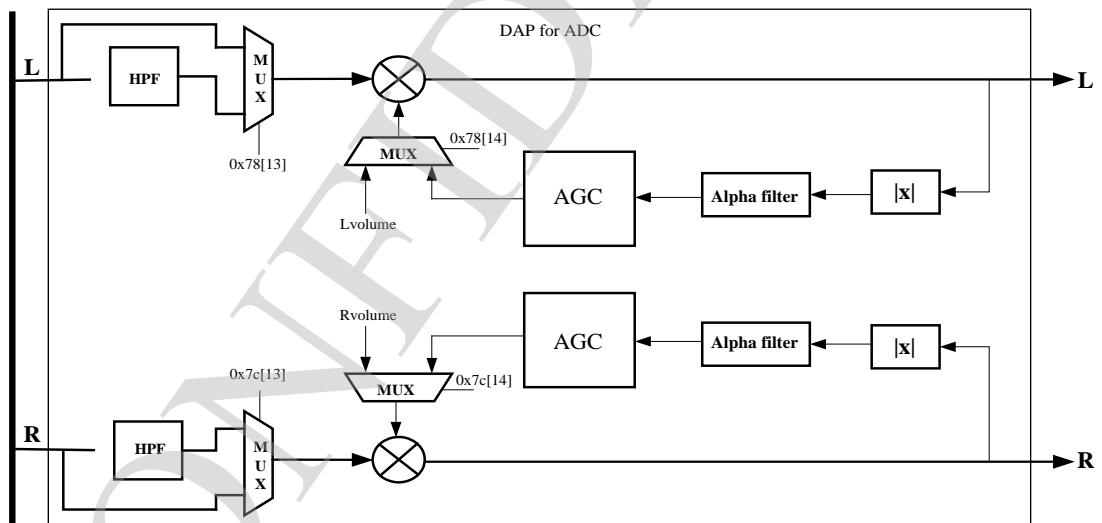


**Figure 34    ADC DAP Data Flow**

## 11.14.1. High Pass Filter

The High Pass Filter (HPF, –3dB cutoff < 1Hz) remove DC offset from ADC recording data. The HPF can also be bypassed.
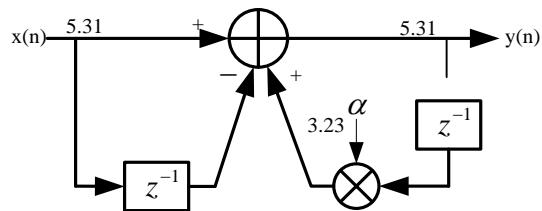


**Figure 35    HPF Characteristic in DAP**

## 11.14.2. Auto Gain Control

The automatic gain control(AGC) can be enabled in the digital recording path of AC100. It automatically adjusts the ADC recording volume gain to a target volume level.
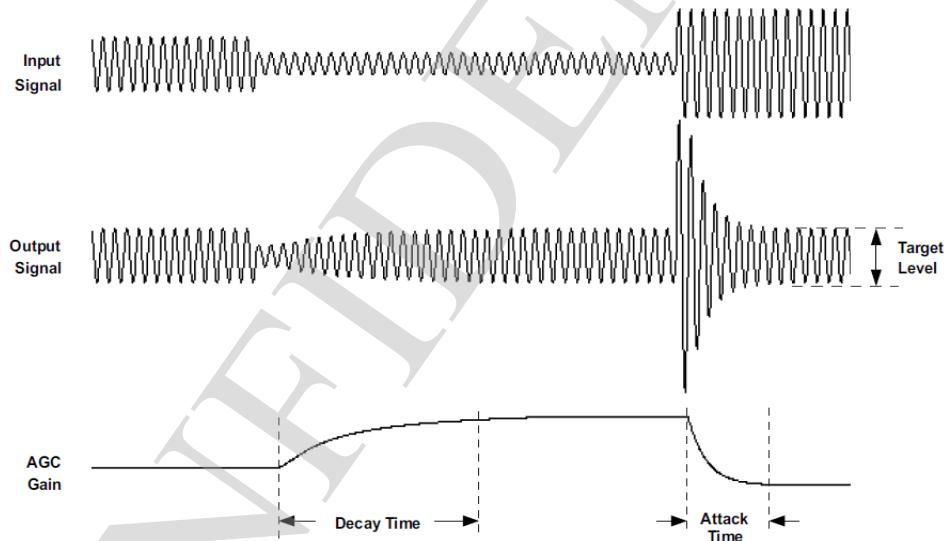


**Figure 36    AGC Response Characteristic**

The ADC Digital Part includes automatic gain control (AGC) for ADC recording. AGC can be used to maintain a nominally-constant output level when recording speech. As opposed to manually setting the PGA gain, in the AGC mode, the circuitry automatically adjusts the PGA gain as the input signal becomes overly loud or weak, such as when aperson speaking into a microphone moves closer to or farther from the microphone. The AGC algorithm has several programmable parameters, including target gain, attack and decay time constants, noise threshold, and max PGA applicable, that allow the algorithm to be fine-tuned for any particular application. The algorithm uses the absolute average of the signal (which is the average of the absolute value of the signal) as a measure of the nominal amplitude of the output signal. Because the gain can be changed at the sample interval time, the AGC algorithm operates at the ADC sample rate. The AGC programs to a wide range of attack and decay skew time from 32/fs to 2^15*32/fs.

When noise cancellation used in system, the AGC should be implement by soft because of no hardware noise cancellation. The AGC process should be after noise cancellation process.

◆ **The AGC Control Parameters**

·**Target level** represents the nominal output level at which the AGC attempts to hold the ADC output signal level. The ADC allows programming of different target levels, which can be programmed from –1dB to –30dB relative to a full-scale signal. Because the ADC reacts to the signal absolute average and not to peak levels, it is recommended that the target level be set with enough margins to avoid clipping at the occurrence of loud sounds.

·**Attack skew time** determine show quickly the AGC circuitry reduces the PGA gain when the output signal level exceeds the target level due to increase in input signal level. A wide range of attack-time programmability is supported in terms of number of samples (i.e., number of ADC sample-frequency clock cycles).

·**Decay skew time** determine show quickly the PGA gain is increased when the output signal level falls below the target level due to reduction in input signal level. A wide range of decay time programmability is supported in terms of number of samples (i.e., number of ADC sample-frequency clock cycles).

·**Noise threshold** is a reference level. If the input speech average value falls below the noise threshold, the AGC considers it as asilence and hence brings down the gain to 0dB in steps of 0.5dB every sample period and sets the noise-threshold flag. The gain stay sat 0dB unless the input speech signal average is es above the noise threshold setting. This ensures that noise is not amplified in the absence of speech. Noise threshold level in the AGC algorithm is programmable from –30dB to –90dB of full-scale. This operation includes hysteresis and debounce to avoid the AGC gain from cycling between high gain and 0dB when signals are near the noise threshold level. The noise (or silence) detection feature can be entirely disabled by the user.

·**Max PGA applicable** allows the designer to restrict the maximum gain applied by the AGC. This can be used for limiting PGA gain in situations where environmental noise is greater than the programmed noise threshold. Microphone input Max PGA applicable can be programmed from 0dB to 40dB in steps of 0.5dB.

·**Hysteresis**, as the name suggests, determines a window around the noise threshold which must be exceeded to detect that the recorded signal is indeed either noise or signal. If initially the energy of the recorded signal is greater than the noise threshold, then the AGC recognizes it as noise only when the energy of the recorded signal falls below the noise threshold by a value given by hysteresis. Similarly, after the recorded signal is recognized as noise, for the AGC to recognize it as a signal, its energy must exceed the noise threshold by a value given by the hysteresis setting. In order to prevent the AGC from jumping between noise and signal states, (which can happen when the energy of recorded signal is close to the noise threshold) a non-zero hysteresis value should be chosen. The hysteresis feature can also be disabled.

·**Debounce time** (noise and signal) determines the hysteresis in time domain for noise detection. The AGC continuously calculates the energy of the recorded signal. If the calculated energy is less than the set noise threshold, then the AGC does not increase the input gain to achieve the target level. However, to handle audible artifacts which can occur when the energy of the input signal is close to the noise threshold, the AGC checks if the energy of the recorded signal is less than the noise threshold for a time greater than the noise debounce time. Similarly, the AGC starts increasing the input-signal gain to reach the target level when the calculated energy of the input signal is greater than the noise threshold. Again, to avoid audible

artifacts when the input-signal energy is close to noise threshold, the energy of the input signal must continuously exceed the noise threshold value for the signal-debounce time. If the debounce times are kept small, then audible artifacts can result by rapid enabling and disabling the AGC function. At the same time, if the debounce time is kept too large, then the AGC may take time to respond to changes in levels of input signal swith respect to the noise threshold. Both noise and signal-debouncet ime can be disabled.

◆ **The AGC Output Information**

·**TheAGC noise-threshold flag** is a read-only flag indicating that the input signal has levels lower than the noise threshold, and thus is detected as noise (or silence). In such a condition, the AGC applies a gain of 0 dB.

·**Gain applied by AGC** is a read-only register setting which gives a real-time feed back to the system on the gain applied by the AGC to the recorded signal. This, a long with the target setting, can be used to determine the input signal level. In a steady-state situation TargetLevel (dB ) = GainAppliedbyAGC(dB) +Input SignalLevel(dB) When the  AGC noise threshold flag is set, then the status of gain applied by AGC is not valid.

·**The AGC saturation flag** is a read-only flag indicating that the ADC output signal has not reached its target level. However, the AGC is unable to increase the gain further because the required gain is higher than the maximum allowed PGA gain. Such a situation can happen when the input signal has low energy and the noise threshold is also set low. When the AGC noise threshold flag is set, the status of AGC saturation flag should be ignored.

·**The ADC saturation flag** is a read-only flag indicating an overflow condition in the ADC channel. On overflow, the signal is clipped and distortion results. This typically happens when the AGC target level is kept high and the energy in the input signal increases faster than the attack time.

◆ **The AGC signal level detect**
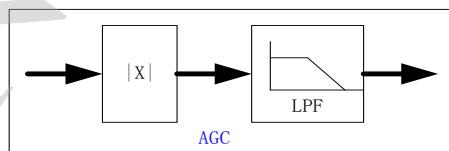


**Figure 37    AGC Signal level detect**

· **An AGC low-pass filter** is used to help determine the average level of the input signal. This average level is compared to the programmed detection levels in the AGC to provide the correct functionality. This low-pass filter is in the form of a first-order IIR filter. The transfer function of the filter implemented for signal level detection is given by

$$H(z) = \frac{\alpha}{1-(1-\alpha)z^{-1}}$$

Where: Coefficient $\alpha$ (3.24 format) is 26-bit 2s complement and will determine the time window over which average level to be made. The parameter is computed by.

$$\alpha = 1 - e^{-2.2Ts/ta}$$

Default time window is 108.8963 *Ts.

◆ **The AGC Characteristics**
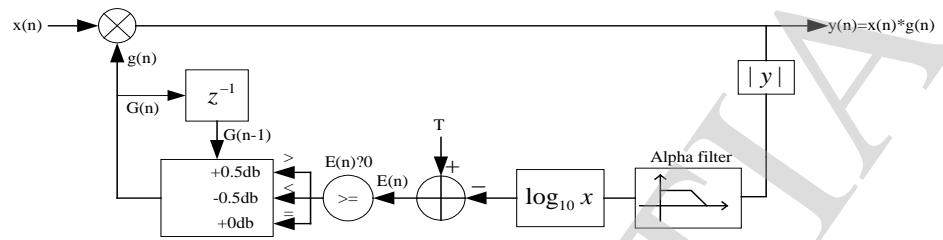


**Figure 38    AGC Module Characteristic**

# 11.15. Digital Audio Process for DAC

The DAP System Block Diagram For DAC.



DAP and System FuctionView
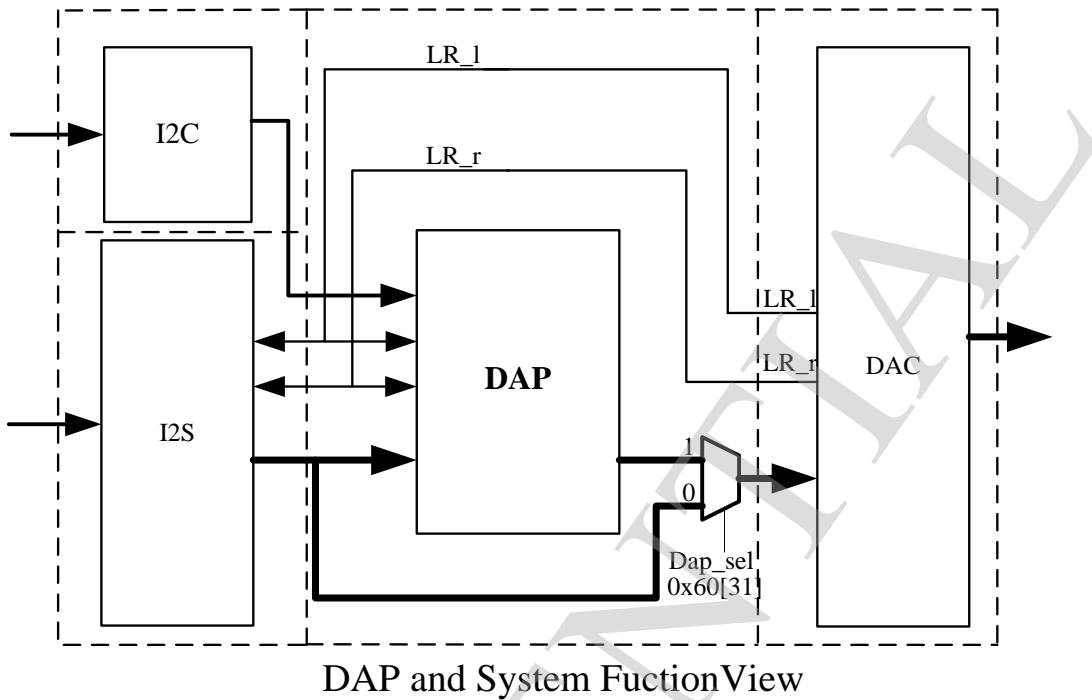
**Figure 39    DAC DAP System Block**

DAP for DAC Data Flow:
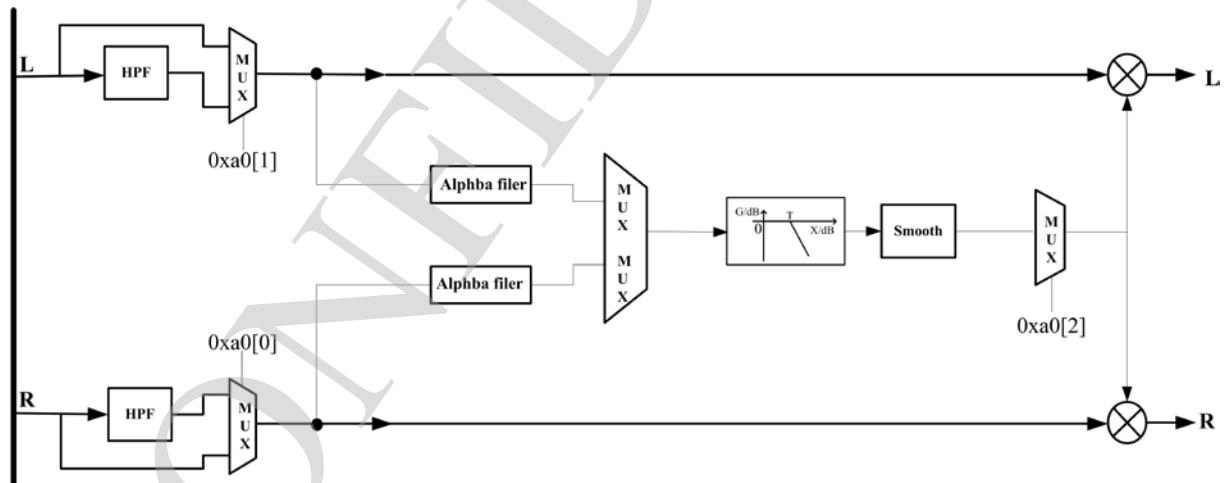


**Figure 40    DAC DAP Data Flow**

## 11.15.1. High Pass Filter

The DAP has individual channel high pass filter that can be enabled and disabled. The filter cutoff frequency is less than 1Hz.

$$H(z) = \frac{1 - z^{-1}}{1 - az^{-1}}$$

## 11.15.2. Dynamic Range Control

The dynamic range control(DRC) can be enabled in the digital playback path of AC100. It automatically adjusts the wide volume gain to flatten volume level.
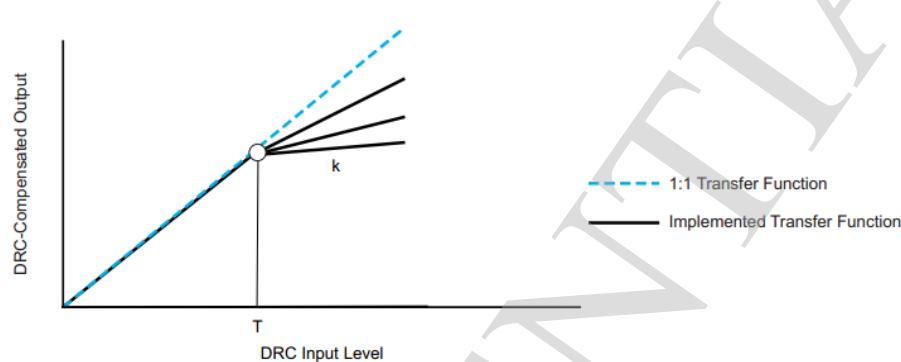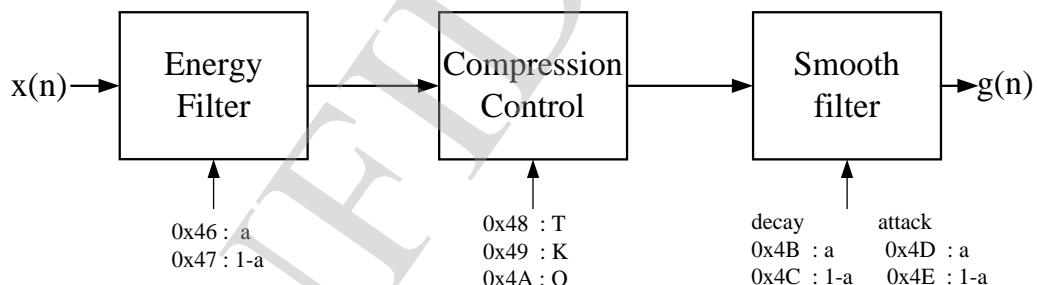


**Figure 41    DRC Response Characteristic**

The DRC supports the main feature below:



**Figure 42    DRC Block and Register Control**

- Adjustable threshold, offset, and compression levels
- Programmable energy coefficient, attack, and decay time constants
- Transparent compression: Compressors can attack fast enough to avoid apparent clipping before engaging, and decay times can be set slow enough to avoid pumping.

◆   **DRC parameter setting**

Numbers formatted as N.M numbers means that there are N bits to the left of the decimal point including the sign bit and M bits to the right of the decimal point. For example, Numbers formatted 3.24 means that there are 3 bits at the left of the decimal point and 24 bits at the right decimal point.

## ◆ Energy Filter

The Energy Filter is to estimate of the RMS value of the audio data stream into DRC, and has two parameters, which determine the time window over which RMS to be made. The parameter is computed by

$$\alpha = 1 - e^{-2.2Ts/ta}$$
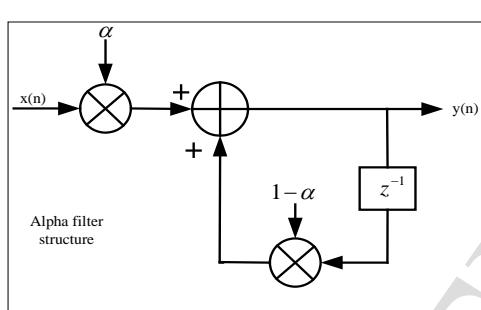


**Figure 43    Energy Filter Structure**

## ◆ Compression Control

This element has three parameters (T, K, O), which are all programmable, and the computation will be explained as below:

**T parameter** (Threshold Parameter Computation)

The threshold is the value that determines the signal to be compressed or not. When the signal's RMS is larger than the threshold, the signal will be compressed. The value of threshold input to the coefficient register is computed by

$$Tin = -\frac{T_{dB}}{6.0206}$$

There, $T_{dB}$ must less than zero, the positive value is illegal.

For example, it desired to set the T=-30dB, then $T_{in} = -\frac{-30}{6.0206} = 4.982$, and the 8.24 format of the Tin is

0x04FB_9ED0.

**K parameter** (Slope Parameter Computation )

The K is the slope within compression region. For example, a n:1 compression means that an output increase 1dB as RMS input increase n dB. The k input to the coefficient register is computed by

$$k = \frac{1}{n} - 1$$

There, n is from 1 to 50, and must be integer.

For example, for n=5, the $k = \frac{1}{5} - 1 = -0.8$, and the 3.24 format of the k is 0x733_3333

**O parameter** (Offset Parameter Computation )

The $O$ is the offset of the compression static curve. The offset input to the coefficient register is computed by $O_{in} = 10^{O/20}$

There, $O$ is -24dB to 24dB.

For example, it desired to set O=6dB, then $O_{in} = 10^{6/20} = 1.995$, and the 5.24 format of the $O_{in}$ is 0x1FE_C982.

◆ **Gain Smooth Filter**

The Gain Smooth Filter is to smooth the gain and control the ratio of gain increase and decrease. The decay time and attack is shown in Figure 5. The structure of the Gain Smooth filter is also the Alpha filter, so the rise time computation is the same as the Energy filter which is

$$\alpha = 1 - e^{-2.2Ts/ta}$$
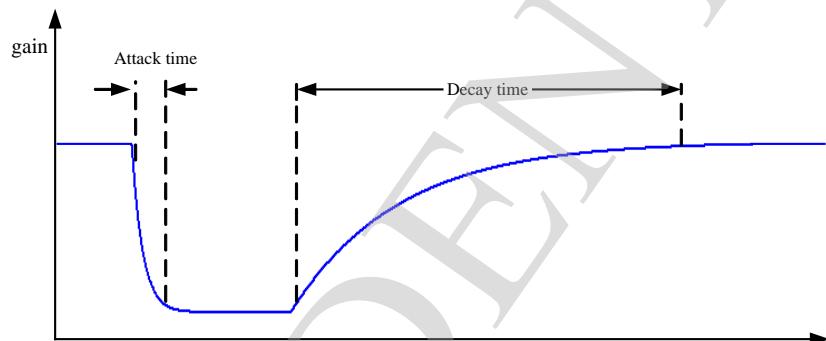


**Figure 44    Smooth Filter Characteristic**

# 11.16. RTC Module

There are a real time clock(RTC) module in AC100 for calendar usage.The RTC module provides second, minute, hour, weekday, day, month, and year information as well as alarm wakeup. The external 32.768kHz crystal oscillator is need to provide a low power, accurate reference.

The RTC fans out three 32.768 kHz outputs CKO1_RTC, CKO2_RTC, and CKO3_RTC derived from external oscillator, while the source also can be congigured as 4MHz frequency dividing output from ADDA oscillator. The outputs are seperately controlled by register CK32K_OUT_CTRLx(x=1,2,3). The first output CKO1_RTC is push-pull pin connected with AP, the CKO2_RTC and CKO3_RTC outputs are open-drain pins for other components such as baseband, or wifi module.

The general purpose registers e0h-efh are used for storing data, since the RTC domain is always power-on.

The block diagram is as below:
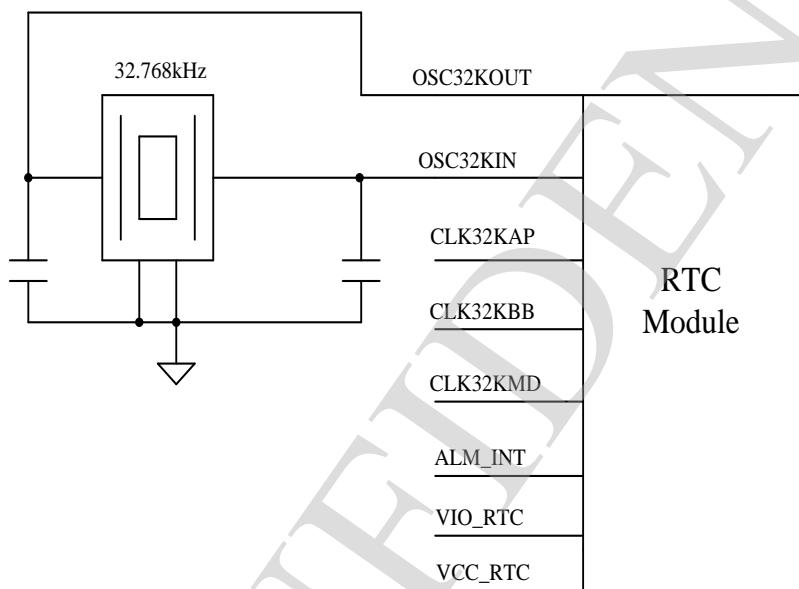
**Figure 45    RTC Block Dia**

# 12. Register List

| Register Name | Offset | Description |
|---|---|---|
| CHIP_AUDIO_RST | 00H | Chip Soft Reset |
| PLL_CTRL1 | 02H | PLL Configure Control 1 |
| PLL_CTRL2 | 03H | PLL Configure Control 2 |
| SYSCLK_CTRL | 04H | System Clocking Control |
| MOD_RST_CTRL | 05H | Module Clock Enable Control |
| ADDA_SR_CTRL | 06H | ADDA Sample Rate Configuration |
| I2S1LCK_CTRL | 10H | I2S1 BCLK/LRCK Control |
| I2S1_SDIN_CTRL | 11H | I2S1 SDIN Control |
| I2S1_SDOUT_CTRL | 12H | I2S1 SDOUT Control |
| I2S1_DIG_MIXER | 13H | I2S1 Digital Mixer Control |
| I2S1_VOL_CTRL1 | 14H | I2S1 Volume Control 1 |
| I2S1_VOL_CTRL2 | 15H | I2S1 Volume Control 2 |
| I2S1_VOL_CTRL3 | 16H | I2S1 Volume Control 3 |
| I2S1_VOL_CTRL4 | 17H | I2S1 Volume Control 4 |
| I2S1_MXR_GAIN | 18H | I2S1 Digital Mixer Gain Control |
| I2S2_CLK_CTRL | 20H | I2S2 BCLK/LRCK Control |
| I2S2_SDIN_CTRL | 21H | I2S2 SDIN Control |
| I2S2_SDOUT_CTRL | 22H | I2S2 SDOUT Control |
| I2S2_DIG_MIXER | 23H | I2S2 Digital Mixer Control |
| I2S2_VOL_CTRL1 | 24H | I2S2 Volume Control 1 |
| I2S2_VOL_CTRL2 | 26H | I2S2 Volume Control 2 |
| I2S2_MXR_GAIN | 28H | I2S2 Digital Mixer Gain Control |
| I2S3_CLK_CTRL | 30H | I2S3 BCLK/LRCK Control |
| I2S3_SDIN_CTRL | 31H | I2S3 SDIN Control |
| I2S3_SDOUT_CTRL | 32H | I2S3 SDOUT Control |
| I2S3_SGP_CTRL | 33H | I2S3 Signal Path Control |
| ADC_DIG_CTRL | 40H | ADC Digital Control |
| TBD | ... | ... |
| RTC_CTRL_REG | B0'h | RTC Control Register |
| RTC_RESET_REG | B1'h | RTC Reset Register |
| ALM_INT_ENA_REG | B2'h | Alarm Interrupt Enable Register |
| ALM_INT_STA_REG | B3'h | Alarm Interrupt Status Register |
| RTC_SEC_REG | B4'h | RTC Seconds Register |
| RTC_MIN_REG | B5'h | RTC Minutes Register |
| RTC_HOU_REG | B6'h | RTC Hours Register |
| RTC_WEE_REG | B7'h | RTC Weekdays Register |
| RTC_DAY_REG | B8'h | RTC Days Register |
| RTC_MON_REG | B9'h | RTC Months Register |
| RTC_YEA_REG | BA'h | RTC Years Register |
| ALM_SEC_REG | C3'h | Alarm Seconds Register |
| ALM_MIN_REG | C4'h | Alarm Minutes Register |

| ALM_HOU_REG | C5'h | Alarm Hours Register |
|---|---|---|
| ALM_WEE_REG | C6'h | Alarm Weekdays Register |
| ALM_DAY_REG | C7'h | Alarm Days Register |
| ALM_MON_REG | C8'h | Alarm Months Register |
| ALM_YEA_REG | C9'h | Alarm Years Register |
| | | |
| | | |
| RTC_GP_REGn | D0'h | RTC General Purpose Register n(n = 0,1,2……31) |

# Reg 00h_Chip Soft Reset Register

| Default: 0x0101 | | | Register Name: CHIP_AUDIO_RST |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:0 | R/W | 0x0101 | Writing to this register resets all register to their default state. Reading from this register will indicate device type and version. |

# Reg 01h_PLL Configure Control 1 Register

| Default: 0x0141 | | | Register Name: PLL_CTRL1 |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:14 | R/W | 0x0 | DPLL_DAC_BIAS<br>00：min<br>11：max |
| 13:8 | R/W | 0x1 | PLL_POSTDIV_M<br>PLL Post-Divider Factor M<br>Factor=0，M=64<br>Factor=1，M=1<br>...<br>Factor=63，M=63 |
| 7 | R/W | 0x0 | Reserved |
| 6 | R/W | 0x1 | Close_loop.<br>1: work as a PLL.<br>0: work as a free running VCO at a pre-fixed frequency. |
| 5:0 | R/W | 0x1 | INT<br>Integ[5:0], the loop bandwidth config.<br>0: works as free running mode.<br>1: small bandwidth, need more time to lock.<br>....<br>63: large bandwidth, need less time to lock, but may result in failing. |

# Reg 02h_PLL Configure Control 2 Register

| Default: 0x0000 | | | Register Name: PLL_CTRL2 |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15 | R/W | 0x0 | PLL_EN<br>PLL Enable<br>0: Disable<br>1: Enable<br>The PLL output FOUT= FIN*N/(M*(2K+1)), N=N_i+N_f; |
| 14 | R | 0x0 | PLL Locked status<br>0: Not locked or not enabled<br>1: Enabled and locked |
| 13:4 | R/W | 0x0 | PLL_PREDIV_NI<br>PLL Integer Part of Pre-Divider Factor N.<br>Factor=0，N_i=0 ;<br>Factor=1，N_i=1 ;<br>...<br>Factor=1023, N_i=1023 ; |
| 3 | / | / | / |
| 2:0 | R/W | 0x0 | PLL_POSTDIV_NF<br>PLL Fractional Part of Pre-Divider Factor N.<br>Factor=0，N_f=0*0.2 ;<br>Factor=1，N_f=1*0.2 ;<br>...<br>Factor=7, N_f=7*0.2 ; |

# Reg 03h_System Clocking Control Register

| Default: 0x0000 | | | Register Name: SYSCLK_CTRL |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15 | R/W | 0x0 | PLLCLK_ENA<br>PLLCLK Enable<br>0: Disable<br>1: Enable |
| 14 | R/W | 0x0 | Reserved |
| 13:12 | R/W | 0x0 | PLLCLK_SRC<br>PLL Clock Source Select<br>00: MCLK1<br>01: MCLK2<br>10: BCLK1<br>11: BCLK2 |
| 11 | R/W | 0x0 | I2S1CLK_ENA<br>I2S1CLK Enable<br>0: Disable<br>1: Enable |
| 10 | R/W | 0x0 | Reserved |

| 9:8 | R/W | 0x0 | I2S1CLK_SRC<br>I2S1CLK Source Select<br>00: MLCK1<br>01: MLCK2<br>1X: PLL |
|-----|-----|-----|-----|
| 7 | R/W | 0x0 | I2S2CLK_ENA<br>I2S2CLK Enable<br>0: Disable<br>1: Enable |
| 6 | R/W | 0x0 | Reserved |
| 5:4 | R/W | 0x0 | I2S2CLK_SRC<br>I2S2CLK Source Select<br>00: MLCK1<br>01: MLCK2<br>1X: PLL |
| 3 | R/W | 0x0 | SYSCLK_ENA<br>SYSCLK Enable<br>0: Disable<br>1: Enable |
| 2:1 | R/W | 0x0 | Reserved |
| 0 | R/W | 0x0 | SYSCLK_SRC<br>System Clock Source Select<br>0: I2S1CLK<br>1: I2S2CLK |

## Reg 04h_Module Clock Enable Control Register

| Default: 0x0000 | | | Register Name: MOD_CLK_ENA |
|-----|-----|-----|-----|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15:0 | R/W | 0x0 | Module clock enable control<br>0-Clock disable<br>1-Clock enable<br>BIT15-I2S1<br>BIT14-I2S2<br>BIT13-I2S3<br>BIT12-Reserved<br>BIT11-SRC1<br>BIT10-SRC2<br>BIT9-Reserved<br>BIT8-Reserved<br>BIT7-HPF & AGC<br>BIT6-HPF & DRC<br>BIT5-Reserved<br>BIT4-Reserved<br>BIT3-ADC Digital<br>BIT2-DAC Digital<br>BIT1-Reserved<br>BIT0-Reserved |

# Reg 05h_Module Reset Control Register

| Default: 0x0000 | | | Register Name: MOD_RST_CTRL |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:0 | R/W | 0x0 | Module reset control<br>0-Reset asserted<br>1-Reset de-asserted<br>BIT15-I2S1<br>BIT14-I2S2<br>BIT13-I2S3<br>BIT12-Reserved<br>BIT11-SRC1<br>BIT10-SRC2<br>BIT9-Reserved<br>BIT8-Reserved<br>BIT7-HPF & AGC<br>BIT6-HPF & DRC<br>BIT5-Reserved<br>BIT4-Reserved<br>BIT3-ADC Digital<br>BIT2-DAC Digital<br>BIT1-Reserved<br>BIT0-Reserved |

# Reg 06h_ADDA Sample Rate Configuration Register

| Default: 0x0000 | | | Register Name: I2S_SR_CTRL |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:12 | R/W | 0x0 | ADDA_FS_I2S1<br>ADDA Sample Rate synchronised with I2S1 clock zone<br>0000: 8KHz<br>0001: 11.025KHz<br>0010: 12KHz<br>0011: 16KHz<br>0100: 22.05KHz<br>0101: 24KHz<br>0110: 32KHz<br>0111: 44.1KHz<br>1000: 48KHz<br>1001: 96KHz<br>1010: 192KHz<br>Other: Reserved |
| 11:8 | R/W | 0x0 | ADDA_FS_I2S2<br>ADDA Sample Rate synchronised with I2S2 clock zone<br>0000: 8KHz<br>0001: 11.025KHz<br>0010: 12KHz |

| | | | |
|---|---|---|---|
| | | | 0011: 16KHz |
| | | | 0100: 22.05KHz |
| | | | 0101: 24KHz |
| | | | 0110: 32KHz |
| | | | 0111: 44.1KHz |
| | | | 1000: 48KHz |
| | | | 1001: 96KHz |
| | | | 1010: 192KHz |
| | | | Other: Reserved |
| 3 | R/W | 0x0 | SRC1_ENA<br>SRC1 Enable. SRC1 Performs sample rate conversion of digital audio input to the AC100.<br>0: Disable<br>1: Enable |
| 2 | R/W | 0x0 | SRC1_SRC<br>From which the input data will come.<br>0: I2S1 DAC Timeslot 0<br>1: I2S2 DAC |
| 1 | R/W | 0x0 | SRC2_ENA<br>SRC2 Enable. SRC2 Performs sample rate conversion of digital audio output from the AC100.<br>0: Disable<br>1: Enable |
| 0 | R/W | 0x0 | SRC2_SRC<br>To which the converted data will be output.<br>0: I2S1 ADC Timeslot 0<br>1: I2S2 ADC |

# Reg 10h_I2S1 BCLK/LRCK Control Register

| Default: 0x0000 | | | Register Name: I2S1LCK_CTRL |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15 | R/W | 0x0 | I2S1_MSTR_MOD<br>I2S1 Audio Interface mode select<br>0 = Master mode<br>1 = Slave mode |
| 14 | R/W | 0x0 | I2S1_BCLK_INV<br>I2S1 BCLK Polarity<br>0: Normal<br>1: Inverted |
| 13 | R/W | 0x0 | I2S1_LRCK_INV<br>I2S1 LRCK Polarity<br>0: Normal<br>1: Inverted |
| 12:9 | R/W | 0x0 | I2S1_BCLK_DIV<br>Select the I2S1CLK/BCLK1 ratio<br>0000: I2S1CLK/1<br>0001: I2S1CLK/2 |

| | | | |
|---|---|---|---|
| | | | 0010: I2S1CLK/4 |
| | | | 0011: I2S1CLK/6 |
| | | | 0100: I2S1CLK/8 |
| | | | 0101: I2S1CLK/12 |
| | | | 0110: I2S1CLK/16 |
| | | | 0111: I2S1CLK/24 |
| | | | 1000: I2S1CLK/32 |
| | | | 1001: I2S1CLK/48 |
| | | | 1010: I2S1CLK/64 |
| | | | 1011: I2S1CLK/96 |
| | | | 1100: I2S1CLK/128 |
| | | | 1101: I2S1CLK/192 |
| | | | 1110: Reserved |
| | | | 1111: Reserved |
| 8:6 | R/W | 0x0 | I2S1_LRCK_DIV<br>Select the BCLK1/LRCK ratio<br>000: 16<br>001: 32<br>010: 64<br>011: 128<br>100: 256<br>1xx: Reserved |
| 5:4 | R/W | 0x0 | I2S1_WORD_SIZ<br>I2S1 digital interface word size<br>00: 8bit<br>01: 16bit<br>10: 20bit<br>11: 24bit |
| 3:2 | R/W | 0x0 | I2S1_DATA_FMT<br>I2S digital interface data format<br>00: I2S mode<br>01: Left mode<br>10: Right mode<br>11: DSP mode |
| 1 | R/W | 0x0 | DSP_MONO_PCM<br>DSP Mono mode select<br>0: Stereo mode select<br>1: Mono mode select |
| 0 | R/W | 0x0 | I2S1_TDMM_ENA<br>I2S1 TDM Mode enable<br>0: Disable<br>1: Enable |

## Reg 11h_I2S1 SDOUT Control Register

| Default: 0x0000 | | | Register Name: I2S1_SDOUT_CTRL |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15 | R/W | 0x0 | I2S1_ADCL0_ENA |

| | | | I2S1 ADC Timeslot 0 left channel enable |
|---|---|---|---|
| | | | 0: Disable |
| | | | 1: Enable |
| 14 | R/W | 0x0 | I2S1_ADCR0_ENA |
| | | | I2S1 ADC Timeslot 0 right channel enable |
| | | | 0: Disable |
| | | | 1: Enable |
| 13 | R/W | 0x0 | I2S1_ADCL1_ENA |
| | | | I2S1 ADC Timeslot 1 left channel enable |
| | | | 0: Disable |
| | | | 1: Enable |
| 12 | R/W | 0x0 | I2S1_ADCR1_ENA |
| | | | I2S1 ADC Timeslot 1 right channel enable |
| | | | 0: Disable |
| | | | 1: Enable |
| 11:10 | R/W | 0x0 | I2S1_ADCL0_SRC |
| | | | I2S1 ADC Timeslot 0 left channel data source select |
| | | | 00: I2S1_ADCL0 |
| | | | 01: I2S1_ADCR0 |
| | | | 10: (I2S1_ADCL0+ I2S1_ADCR0) |
| | | | 11: (I2S1_ADCL0+ I2S1_ADCR0)/2 |
| 9:8 | R/W | 0x0 | I2S1_ADCR0_SRC |
| | | | I2S1 ADC Timeslot 0 right channel data source select |
| | | | 00: I2S1_ADCR0 |
| | | | 01: I2S1_ADCL0 |
| | | | 10: (I2S1_ADCL0+I2S1_ADCR0) |
| | | | 11: (I2S1_ADCL0+I2S1_ADCR0)/2 |
| 7:6 | R/W | 0x0 | I2S1_ADCL1_SRC |
| | | | I2S1 ADC Timeslot 1 left channel data source select |
| | | | 00: I2S1_ADCL1 |
| | | | 01: I2S1_ADCR1 |
| | | | 10: (I2S1_ADCL1+I2S1_ADCR1) |
| | | | 11: (I2S1_ADCL1+I2S1_ADCR1)/2 |
| 5:4 | R/W | 0x0 | I2S1_ADCR1_SRC |
| | | | I2S1 ADC Timeslot 1 right channel data source select |
| | | | 00: I2S1_ADCR1 |
| | | | 01: I2S1_ADC1L |
| | | | 10: (I2S1_ADCL1+I2S1_ADCR1) |
| | | | 11: (I2S1_ADCL1+I2S1_ADCR1)/2 |
| 3 | R/W | 0x0 | I2S1_ADCP_ENA |
| | | | I2S1 ADC Companding enable(8-bit mode only) |
| | | | 0: Disable |
| | | | 1: Enable |
| 2 | R/W | 0x0 | I2S1_ ADCP_SEL |
| | | | I2S1ADC Companding mode select |
| | | | 0: A-law |
| | | | 1: u-law |
| 1:0 | R/W | 0x0 | I2S1_SLOT_SIZ |

| | | | Select the slot size(only in TDM mode) |
| | | | 00: 8 |
| | | | 01: 16 |
| | | | 10: 32 |
| | | | 11: Reserved |

## Reg 12h_I2S1 SDIN Control Register

| Default: 0x0000 | | | Register Name: I2S1_SDIN_CTRL |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15 | R/W | 0x0 | I2S1_DACL0_ENA<br>I2S1 DAC Timeslot 0 left channel enable<br>0: Disable<br>1: Enable |
| 14 | R/W | 0x0 | I2S1_DACR0_ENA<br>I2S1 DAC Timeslot 0 right channel enable<br>0: Disable<br>1: Enable |
| 13 | R/W | 0x0 | I2S1_DACL1_ENA<br>I2S1 DAC Timeslot 1 left channel enable<br>0: Disable<br>1: Enable |
| 12 | R/W | 0x0 | I2S1_DACR1_ENA<br>I2S1 DAC Timeslot 1 right channel enable<br>0: Disable<br>1: Enable |
| 11:10 | R/W | 0x0 | I2S1_DACL0_SRC<br>I2S1 DAC Timeslot 0 left channel data source select<br>00: I2S1_DACL0<br>01: I2S1_DACR0<br>10: (I2S1_DACL0+I2S1_DACR0)<br>11: (I2S1_DACL0+I2S1_DACR0)/2 |
| 9:8 | R/W | 0x0 | I2S1_DACR0_SRC<br>I2S1 DAC Timeslot 0 right channel data source select<br>00: I2S1_DACR0<br>01: I2S1_DACL0<br>10: (I2S1_DACL0+I2S1_DACR0)<br>11: (I2S1_DACL0+I2S1_DACR0)/2 |
| 7:6 | R/W | 0x0 | I2S1_DACL1_SRC<br>I2S1 DAC Timeslot 1 left channel data source select<br>00: I2S1_DACL1<br>01: I2S1_DACR1<br>10: (I2S1_DACL1+I2S1_DACR1)<br>11: (I2S1_DACL1+I2S1_DACR1)/2 |
| 5:4 | R/W | 0x0 | I2S1_DACR1_SRC<br>I2S1 DAC Timeslot 1 right channel data source select<br>00: I2S1 DACR1<br>01: I2S1 DACL1 |

| | | | |
|---|---|---|---|
| | | | 10: (I2S1 DACL1+I2S1 DACR1) |
| | | | 11: (I2S1 DACL1+I2S1 DACR1)/2 |
| 3 | R/W | 0x0 | I2S1_DACP_ENA<br>I2S1 DAC Companding enable(8-bit mode only)<br>00: Disable<br>01: Enable |
| 2 | R/W | 0x0 | I2S1_ DACP_SEL<br>I2S1 DAC Companding mode select<br>0: A-law<br>1: u-law |
| 1 | R/W | 0x0 | Reserved |
| 0 | R/W | 0x0 | I2S1_LOOP_ENA<br>I2S1 loopback enable<br>0: No loopback<br>1: Loopback(SDOUT1 data output to SDOUT1 data input) |

# Reg 13h_I2S1 Digital Mixer Source Select Register

| Default: 0x0000 | | | Register Name: I2S1_MXR_SRC |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:12 | R/W | 0x0 | I2S1_ADCL0_MXL_SRC<br>I2S1 ADC Timeslot 0 left channel mixer source select<br>0: Disable    1: Enable<br>Bit15: I2S1_DA0L data<br>Bit14: I2S2_DACL data<br>Bit13: ADCL data<br>Bit12: I2S2_DACR data |
| 11:8 | R/W | 0x0 | I2S1_ADCR0_MXR_SRC<br>I2S1 ADC Timeslot 0 right channel mixer source select<br>0: Disable    1: Enable<br>Bit11: I2S1_DA0R data<br>Bit10: I2S2_DACR data<br>Bit9: ADCR data<br>Bit8: I2S2_DACL data |
| 7:6 | R/W | 0x0 | I2S1_ADCL1_MXR_SRC<br>I2S1 ADC Timeslot 1 left channel mixer source select<br>0: Disable    1: Enable<br>Bit7: I2S2_DACL data<br>Bit6: ADCL data |
| 5:4 | R/W | 0x0 | Reserved |
| 3:2 | R/W | 0x0 | I2S1_ADCR1_MXR_SRC<br>I2S1 ADC Timeslot 1 right channel mixer source select<br>0: Disable    1: Enable<br>Bit3: I2S2_DACR data<br>Bit2: ADCR data |
| 1:0 | R/W | 0x0 | Reserved |

# Reg 14h_I2S1 Volume Control 1 Register

| Default: 0xA0A0 | | | Register Name: I2S1_VOL_CTRL1 |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:8 | R/W | 0xA0 | I2S1_ADCL0_VOL<br>I2S1 ADC Timeslot 0 left channel volume<br>(-119.25dB To 71.25dB, 0.75dB/Step)<br>0x00: Mute<br>0x01: -119.25dB<br>………………<br>0x9F = -0.75dB<br>0xA0 = 0dB<br>0xA1 = 0.75dB<br>………………<br>0xFF = 71.25dB |
| 7:0 | R/W | 0xA0 | I2S1_ADCR0_VOL<br>I2S1 ADC Timeslot 0 right channel volume<br>(-119.25dB To 71.25dB, 0.75dB/Step)<br>0x00: Mute<br>0x01: -119.25dB<br>………………<br>0x9F = -0.75dB<br>0xA0 = 0dB<br>0xA1 = 0.75dB<br>………………<br>0xFF = 71.25dB |

# Reg 15h_I2S1 Volume Control 2 Register

| Default: 0xA0A0 | | | Register Name: I2S1_VOL_CTRL2 |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:8 | R/W | 0xA0 | I2S1_ADCL1_VOL<br>I2S1 ADC Timeslot 1 left channel volume<br>(-119.25dB To 71.25dB, 0.75dB/Step)<br>0x00: Mute<br>0x01: -119.25dB<br>………………<br>0x9F = -0.75dB<br>0xA0 = 0dB<br>0xA1 = 0.75dB<br>………………<br>0xFF = 71.25dB |
| 7:0 | R/W | 0xA0 | I2S1_ADCR1_VOL<br>I2S1 ADC Timeslot 1 right channel volume<br>(-119.25dB To 71.25dB, 0.75dB/Step)<br>0x00: Mute<br>0x01: -119.25dB |

| | | | |
|---|---|---|---|
| | | | ……………… |
| | | | 0x9F = -0.75dB |
| | | | 0xA0 = 0dB |
| | | | 0xA1 = 0.75dB |
| | | | ……………… |
| | | | 0xFF = 71.25dB |

## Reg 16h_I2S1 Volume Control 3 Register

| Default: 0xA0A0 | | | Register Name: I2S1_VOL_CTRL3 |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:8 | R/W | 0xA0 | I2S1_DACL0_VOL<br>I2S1 DAC Timeslot 0 left channel volume<br>(-119.25dB To 71.25dB, 0.75dB/Step)<br>0x00: Mute<br>0x01: -119.25dB<br>………………<br>0x9F = -0.75dB<br>0xA0 = 0dB<br>0xA1 = 0.75dB<br>………………<br>0xFF = 71.25dB |
| 7:0 | R/W | 0xA0 | I2S1_DACR0_VOL<br>I2S1 DAC Timeslot 0 right channel volume<br>(-119.25dB To 71.25dB, 0.75dB/Step)<br>0x00: Mute<br>0x01: -119.25dB<br>………………<br>0x9F = -0.75dB<br>0xA0 = 0dB<br>0xA1 = 0.75dB<br>………………<br>0xFF = 71.25dB |

## Reg 17h_I2S1 Volume Control 4 Register

| Default: 0xA0A0 | | | Register Name: I2S1_VOL_CTRL4 |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:8 | R/W | 0xA0 | I2S1_DACL1_VOL<br>I2S1 DAC Timeslot 1 left channel volume<br>(-119.25dB To 71.25dB, 0.75dB/Step)<br>0x00: Mute<br>0x01: -119.25dB<br>………………<br>0x9F = -0.75dB<br>0xA0 = 0dB<br>0xA1 = 0.75dB<br>……………… |

| | | | 0xFF = 71.25dB |
|---|---|---|---|
| 7:0 | R/W | 0xA0 | I2S1_DACR1_VOL<br>I2S1 DAC Timeslot 1 right channel volume<br>(-119.25dB To 71.25dB, 0.75dB/Step)<br>0x00: Mute<br>0x01: -119.25dB<br>………………<br>0x9F = -0.75dB<br>0xA0 = 0dB<br>0xA1 = 0.75dB<br>………………<br>0xFF = 71.25dB |

## Reg 18h_I2S1 Digital Mixer Gain Control Register

| Default: 0x0000 | | | Register Name: I2S1_MXR_GAIN |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:12 | R/W | 0x0 | I2S1_ADCL0_MXR_GAIN<br>I2S1 ADC Timeslot 0 left channel mixer gain control<br>0: 0dB    1: -6dB<br>Bit15: I2S1_DA0L data<br>Bit14: I2S2_DACL data<br>Bit13: ADCL data<br>Bit12: I2S2_DACR data |
| 11:8 | R/W | 0x0 | I2S1_ADCR0_MXR_GAIN<br>I2S1 ADC Timeslot 0 right channel mixer gain control<br>0: 0dB    1: -6dB<br>Bit11: I2S1_DA0R data<br>Bit10: I2S2_DACR data<br>Bit9: ADCR data<br>Bit8: I2S2_DACL data |
| 7:6 | R/W | 0x0 | I2S1_ADCL1_MXR_GAIN<br>I2S1 ADC Timeslot 1 left channel mixer gain control<br>0: 0dB    1: -6dB<br>Bit7: I2S2_DACL data<br>Bit6: ADCL data |
| 5:4 | R/W | 0x0 | Reserved |
| 3:2 | R/W | 0x0 | I2S1_ADCR1_MXR_GAIN<br>I2S1 ADC Timeslot 1 right channel mixer gain control<br>0: 0dB    1: -6dB<br>Bit3: I2S2_DACR data<br>Bit2: ADCR data |
| 1:0 | R/W | 0x0 | Reserved |

## Reg 20h_I2S2 BCLK/LRCK Control Register

| Default: 0x0000 | Register Name: I2S2_CLK_CTRL |
|---|---|

| Bit | Read/Write | Default | Description |
|---|---|---|---|
| 15 | R/W | 0x0 | I2S2_MSTR_MOD<br>I2S2 Audio Interface mode select<br>0 = Master mode<br>1 = Slave mode |
| 14 | R/W | 0x0 | I2S2_BCLK_INV<br>I2S2 BCLK Polarity<br>0: Normal<br>1: Inverted |
| 13 | R/W | 0x0 | I2S2_LRCK_INV<br>I2S2 LRCK Polarity<br>0: Normal<br>1: Inverted |
| 12:9 | R/W | 0x0 | I2S2_BCLK_DIV<br>Select the I2S2CLK/BCLK2 ratio<br>0000: I2S2CLK/1<br>0001: I2S2CLK/2<br>0010: I2S2CLK/4<br>0011: I2S2CLK/6<br>0100: I2S2CLK/8<br>0101: I2S2CLK/12<br>0110: I2S2CLK/16<br>0111: I2S2CLK/24<br>1000: I2S2CLK/32<br>1001: I2S2CLK/48<br>1010: I2S2CLK/64<br>1011: I2S2CLK/96<br>1100: I2S2CLK/128<br>1101: I2S2CLK/192<br>1110: Reserved<br>1111: Reserved |
| 8:6 | R/W | 0x0 | I2S2_LRCK_DIV<br>Select the BCLK2/LRCK2 ratio<br>000: 16<br>001: 32<br>010: 64<br>011: 128<br>100: 256<br>1xx: Reserved |
| 5:4 | R/W | 0x0 | I2S2_WORD_SIZ<br>I2S2 digital interface world length<br>00: 8bit<br>01: 16bit<br>10: 20bit<br>11: 24bit |
| 3:2 | R/W | 0x0 | I2S2_DATA_FMT<br>I2S digital interface data format<br>00: I2S mode |

| | | | 01: Left mode |
| | | | 10: Right mode |
| | | | 11: DSP mode |
| 1 | R/W | 0x0 | I2S2_MONO_PCM |
| | | | I2S2 Mono PCM mode select |
| | | | 0: Stereo mode select |
| | | | 1: Mono mode select |
| 0 | R/W | 0x0 | Reserved |

## Reg 21h_I2S2 SDOUT Control Register

| Default: 0x0000 | | | Register Name: I2S2_SDOUT_CTRL |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15 | R/W | 0x0 | I2S2_ADCL_EN |
| | | | I2S2 ADC left channel enable |
| | | | 0: Disable |
| | | | 1: Enable |
| 14 | R/W | 0x0 | I2S2_ADCR_EN |
| | | | I2S2 ADC right channel enable |
| | | | 0: Disable |
| | | | 1: Enable |
| 13:12 | R/W | 0x0 | Reserved |
| 11:10 | R/W | 0x0 | I2S2_ADCL_SRC |
| | | | I2S2 ADC left channel data source select |
| | | | 00: I2S2_ADCL |
| | | | 01: I2S2_ADCR |
| | | | 10: (I2S2_ADCL+I2S2_ADCR) |
| | | | 11: (I2S2_ADCL+I2S2_ADCR)/2 |
| 9:8 | R/W | 0x0 | I2S2_ADCR_SRC |
| | | | I2S2 ADC right channel data source select |
| | | | 00: I2S2_ADCR |
| | | | 01: I2S2_ADCL |
| | | | 10: (I2S2_ADCL+I2S2_ADCR) |
| | | | 11: (I2S2_ADCL+I2S2_ADCR)/2 |
| 7:4 | R/W | 0x0 | Reserved |
| 3 | R/W | 0x0 | I2S2_ADCP_ENA |
| | | | I2S2 ADC Companding enable(8-bit mode only) |
| | | | 00: Disable |
| | | | 01: Enable |
| 2 | R/W | 0x0 | I2S2_ADCP_SEL |
| | | | I2S2 ADC Companding mode select |
| | | | 0: A-law |
| | | | 1: u-law |
| 1:0 | / | / | / |

# Reg 22h_I2S2 SDIN Control Register

| Default: 0x0000 | | | Register Name: I2S2_SDIN_CTRL |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15 | R/W | 0x0 | I2S2_DACL_ENA<br>I2S2 DAC left channel enable<br>0: Disable<br>1: Enable |
| 14 | R/W | 0x0 | I2S2_DACR_ENA<br>I2S2 DAC right channel enable<br>0: Disable<br>1: Enable |
| 13:12 | R/W | 0x0 | Reserved |
| 11:10 | R/W | 0x0 | I2S2_DACL_SRC<br>I2S2 DAC left channel data source select<br>00: I2S2_DACL<br>01: I2S2_DACR<br>10: (I2S2_DACL+I2S2_DACR)<br>11: (I2S2_DACL+I2S2_DACR)/2 |
| 9:8 | R/W | 0x0 | I2S2_DACR_SRC<br>I2S2 DAC right channel data source select<br>00: I2S2_DACR<br>01: I2S2_DACL<br>10: (I2S2_DACL+I2S2_DACR)<br>11: (I2S2_DACL+I2S2_DACR)/2 |
| 7:4 | R/W | 0x0 | Reserved |
| 3 | R/W | 0x0 | I2S2_DACP_ENA<br>I2S2 DAC Companding enable(8-bit mode only)<br>00: Disable<br>01: Enable |
| 2 | R/W | 0x0 | I2S2_ DACP_SEL<br>I2S2 DAC Companding mode select<br>0: A-law<br>1: u-law |
| 1 | R/W | 0x0 | Reserved |
| 0 | R/W | 0x0 | I2S2_LOOP_EN<br>I2S2 loopback enable<br>0: No loopback<br>1: Loopback(SDOUT2 data output to SDOUT2 data input) |

# Reg 23h_I2S2 Digital Mixer Source Select Register

| Default: 0x0000 | | | Register Name: I2S2_MXR_SRC |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:12 | R/W | 0x0 | I2S2_ADCL_MXR_SRC<br>I2S2 ADC left channel mixer source select<br>0: Disable   1:Enable<br>Bit15: I2S1_DA0L data<br>Bit14: I2S1_DA1L data<br>Bit13: I2S2_DACR data<br>Bit12: ADCL data |
| 11:8 | R/W | 0x0 | I2S2_ADCR_MXR_SRC<br>I2S2 ADC right channel mixer source select<br>0: Disable   1:Enable<br>Bit11: I2S1_DA0R data<br>Bit10: I2S1_DA1R data<br>Bit9: I2S2_DACL data<br>Bit8: ADCR data |
| 7:0 | R/W | 0x0 | Reserved |

# Reg 24h_I2S2 Volume Control 1 Register

| Default: 0xA0A0 | | | Register Name: I2S2_VOL_CTRL1 |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:8 | R/W | 0xA0 | I2S2_ADCL_VOL<br>I2S2 ADC left channel volume<br>(-119.25dB To 71.25dB, 0.75dB/Step)<br>0x00: Mute<br>0x01: -119.25dB<br>………………<br>0x9F = -0.75dB<br>0xA0 = 0dB<br>0xA1 = 0.75dB<br>………………<br>0xFF = 71.25dB |
| 7:0 | R/W | 0xA0 | I2S2_ADCR_VOL<br>I2S2 ADC right channel volume<br>(-119.25dB To 71.25dB, 0.75dB/Step)<br>0x00: Mute<br>0x01: -119.25dB<br>………………<br>0x9F = -0.75dB<br>0xA0 = 0dB<br>0xA1 = 0.75dB<br>………………<br>0xFF = 71.25dB |

# Reg 26h_I2S2 Volume Control 2 Register

| Default: 0xA0A0 | | | Register Name: I2S2_VOL_CTRL2 |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:8 | R/W | 0xA0 | I2S2_DACL_VOL<br>I2S2 DAC left channel volume<br>(-119.25dB To 71.25dB, 0.75dB/Step)<br>0x00: Mute<br>0x01: -119.25dB<br>………………<br>0x9F = -0.75dB<br>0xA0 = 0dB<br>0xA1 = 0.75dB<br>………………<br>0xFF = 71.25dB |
| 7:0 | R/W | 0xA0 | I2S2_DACR_VOL<br>I2S2 DAC right channel volume<br>(-119.25dB To 71.25dB, 0.75dB/Step)<br>0x00: Mute<br>0x01: -119.25dB<br>………………<br>0x9F = -0.75dB<br>0xA0 = 0dB<br>0xA1 = 0.75dB<br>………………<br>0xFF = 71.25dB |

# Reg 28h_I2S2 Digital Mixer Gain Control Register

| Default: 0x0000 | | | Register Name: I2S2_MXR_GAIN |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:12 | R/W | 0x0 | I2S2_ADCL_MXR_GAIN<br>I2S2 ADC left channel mixer gain control<br>0: 0dB    1: -6dB<br>Bit15: I2S1_DA0L data<br>Bit14: I2S1_DA1L data<br>Bit13: I2S2_DACR data<br>Bit12: ADCL data |
| 11:8 | R/W | 0x0 | I2S2_ADCR_MXR_GAIN<br>I2S2 ADC right channel mixer gain control<br>0: 0dB    1: -6dB<br>Bit11: I2S1_DA0R data<br>Bit10: I2S1_DA1R data<br>Bit9: I2S2_DACL data<br>Bit8: ADCR data |
| 7:0 | R/W | 0x0 | Reserved |

# Reg 30h_I2S3 BCLK/LRCK Control Register

| Default: 0x0000 | | | Register Name: I2S3_CLK_CTRL |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15 | R/W | 0x0 | Reserved |
| 14 | R/W | 0x0 | I2S3_BCLK_INV<br>I2S3 BCLK Polarity<br>0: Normal<br>1: Inverted |
| 13 | R/W | 0x0 | I2S3_LRCK_INV<br>I2S3 LRCK Polarity<br>0: Normal<br>1: Inverted |
| 12:6 | R/W | 0x0 | Reserved |
| 5:4 | R/W | 0x0 | I2S3_WORD_SIZ<br>I2S3 digital interface world length<br>00: 8bit<br>01: 16bit<br>10: 20bit<br>11: 24bit |
| 3:2 | R/W | 0x0 | Reserved |
| 1:0 | R/W | 0x0 | I2S3_CLOC_SRC<br>I2S3 BCLK/LRCK source control<br>0: BCLK/LRCK Come from I2S1<br>1: BCLK/LRCK Come from I2S2<br>2: BCLK/LRCK is generated by I2S3, and the source clock is I2S1CLK<br>3: Reserved |

# Reg 31h_I2S3 SDOUT Control Register

| Default: 0x0000 | | | Register Name: I2S3_SDOUT_CTRL |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:4 | R/W | 0x0 | Reserved |
| 3 | R/W | 0x0 | I2S3_ADCP_ENA<br>I2S3 ADC Companding enable<br>00: Disable<br>01: Enable |
| 2 | R/W | 0x0 | I2S3_ ADCP_SEL<br>I2S3 ADC Companding mode select<br>0: A-law<br>1: u-law |
| 1:0 | R/W | 0x0 | Reserved |

# Reg 32h_I2S3 SDIN Control Register

| Default: 0x0000 | Register Name: I2S3_SDIN_CTRL |
|---|---|

| Bit | Read/Write | Default | Description |
|---|---|---|---|
| 15:4 | R/W | 0x0 | Reserved |
| 3 | R/W | 0x0 | I2S3_DACP_ENA<br>I2S3 DAC Companding enable(8-bit mode only)<br>00: Disable<br>01: Enable |
| 2 | R/W | 0x0 | I2S3_ DACP_SEL<br>I2S3 DAC Companding mode select<br>00: u-law<br>01: A-law |
| 1 | R/W | 0x0 | Reserved |
| 0 | R/W | 0x0 | I2S3_LOOP_ENA<br>I2S3 loopback enable<br>0: No loopback<br>1: Loopback(SDOUT3 data output to SDOUT3 data input) |

## Reg 33h_I2S3 Signal Path Control Register

| Default: 0x0000 | | | Register Name: I2S3_SGP_CTRL |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:12 | R/W | 0x0 | Reserved |
| 11:10 | R/W | 0x0 | I2S3_ADC_SRC<br>I2S3 PCM output source select<br>00: None<br>01: I2S2_ADCL<br>10: I2S2_ADCR<br>11: Reserved |
| 9:8 | R/W | 0x0 | I2S2_DAC_SRC<br>I2S2 DAC input source select<br>00: (I2S2_ADCL+ I2S2_ADCR)<br>01: Left input from I2S3_DAC; Right input from I2S2_ADCR<br>10: Left input from I2S2_ADCL; Right input from I2S3_DAC<br>11: Reserved |
| 7:0 | R/W | 0x0 | Reserved |

## Reg 40h_ADC Digital Control Register

| Default: 0x0000 | | | Register Name: ADC_DIG_CTRL |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15 | R/W | 0x0 | ENAD<br>ADC Digital part enable<br>0: Disable<br>1: Enable |
| 14 | R/W | 0x0 | ENDM<br>Digital microphone enable<br>0: Analog ADC mode<br>1: Digital microphone mode |

| 13 | R/W | 0x0 | ADFIR32<br>Enable 32-tap FIR filter<br>0: 64-tap<br>1: 32-tap |
|---|---|---|---|
| 12:4 | R/W | 0x0 | Reserved |
| 3:2 | R/W | 0x0 | ADOUT_DTS<br>ADC Delay Time For transmitting data after ENAD<br>00:5ms<br>01:10ms<br>10:20ms<br>11:30ms |
| 1 | R/W | 0x0 | ADOUT_DLY<br>ADC Delay Function enable for transmitting data after ENAD<br>0: Disable<br>1: Enable |
| 0 | R/W | 0x0 | Reserved |

## Reg 41h_ADC Volume Control Register

| Default: 0xA0A0 | | | Register Name: ADC_VOL_CTRL |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:8 | R/W | 0xA0 | ADC_VOL_L<br>ADC left channel volume<br>(-119.25dB To 71.25dB, 0.75dB/Step)<br>0x00: Mute<br>0x01: -119.25dB<br>………………<br>0x9F = -0.75dB<br>0xA0 = 0dB<br>0xA1 = 0.75dB<br>………………<br>0xFF = 71.25dB |
| 7:0 | R/W | 0xA0 | ADC_VOL_R<br>ADC left channel volume<br>(-119.25dB To 71.25dB, 0.75dB/Step)<br>0x00: Mute<br>0x01: -119.25dB<br>………………<br>0x9F = -0.75dB<br>0xA0 = 0dB<br>0xA1 = 0.75dB<br>………………<br>0xFF = 71.25dB |

## Reg 44h_HMIC Control 1 Register

| Default: 0x0000 | Register Name: HMIC_CTRL1 |
|---|---|

| Bit | Read/Write | Default | Description |
|---|---|---|---|
| 15:12 | R/W | 0x0 | HMIC_M <br> debounce when Key down or key up |
| 11:8 | R/W | 0x0 | HMIC_N <br> debounce when earphone plug in or pull out |
| 7 | R/W | 0x0 | HMIC_DATA_IRQ_MODE <br> Hmic Data Irq Mode Select <br> 0: Hmic data irq once after key down <br> 1: Hmic data irq from key down, util key up |
| 6:5 | R/W | 0x0 | HMIC_TH1_HYSTERESIS <br> Hmic Hysteresis Threshold1 <br> 00: no Hysteresis <br> 01: Pull Out when Data <= (Hmic_th2-1) <br> 10: Pull Out when Data <= (Hmic_th2-2) <br> 11: Pull Out when Data <= (Hmic_th2-3) |
| 4 | R/W | 0x0 | HMIC_PULLOUT_IRQ_EN <br> Hmic Earphone Pull out Irq Enable <br> 00: disable 11: enable |
| 3 | R/W | 0x0 | HMIC_PLUGIN_IRQ_EN <br> Hmic Earphone Plug in Irq Enable <br> 00: disable 11: enable |
| 2 | R/W | 0x0 | HMIC_KEYUP_IRQ_EN <br> Hmic Key Up Irq Enable <br> 00: disable 11: enable |
| 1 | R/W | 0x0 | HMIC_KEYDOWN_IRQ_EN <br> Hmic Key Down Irq Enable <br> 00: disable 11: enable |
| 0 | R/W | 0x0 | HMIC_DATA_IRQ_EN <br> Hmic Data Irq Enable <br> 0: disable 1: enable |

## Reg 45h_HMIC Control 2 Register

| Default: 0x0000 | | | Register Name: HMIC_CTRL2 |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:14 | R/W | 0x0 | HMIC_SAMPLE_SELECT <br> Down Sample Setting Select <br> 00: Down by 1, 128Hz <br> 01: Down by 2, 64Hz <br> 10: Down by 4, 32Hz <br> 11: Down by 8, 16Hz |
| 13 | R/W | 0x0 | HMIC_TH2_HYSTERESIS <br> Hmic Hysteresis Threshold2 <br> 0: no Hysteresis <br> 1: Key Up when Data <= (Hmic_th2-1) |
| 12:8 | R/W | 0x0 | HMIC_TH2 <br> Hmic_th2 for detecting Key down or Key up. |

| 7:6 | R/W | 0x0 | HMIC_SF<br>Hmic Smooth Filter setting<br>00: by pass<br>01: (x1+x2)/2<br>10: (x1+x2+x3+x4)/4<br>11: (x1+x2+x3+x4+ x5+x6+x7+x8)/8 |
|---|---|---|---|
| 5 | R/W | 0x0 | KEYUP_CLEAR<br>Key Up Irq Pending bit auto clear when Key Down Irq<br>0: don't clear    1: auto clear |
| 4:0 | R/W | 0x0 | HMIC_TH1<br>Hmic_th1[4:0], detecting eraphone plug in or pull out. |

## Reg 46h_HMIC Status Register

| Default: 0x0000 | | | Register Name: HMIC_STATUS |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15:13 | R/W | 0x0 | Reserved |
| 12:8 | R | 0x0 | HMIC_DATA<br>HMIC Average Data |
| 7:5 | R/W | 0x0 | Reserved |
| 4 | R/W | 0x0 | HMIC_PULLOUT_PENDING<br>Hmic Earphone Pull out Irq pending bit, write 1 to clear<br>0: No Pending Interrupt<br>1: Pull out Irq Pending Interrupt |
| 3 | R/W | 0x0 | HMIC_PLUGIN_PENDING<br>Hmic Earphone Plug in Irq pending bit, write 1 to clear<br>0: No Pending Interrupt<br>1: Plug in Irq Pending Interrupt |
| 2 | R/W | 0x0 | HMIC_KEYUP_PENDING<br>Hmic Key Up Irq pending bit, write 1 to clear<br>0: No Pending Interrupt<br>1: Key up Irq Pending Interrupt |
| 1 | R/W | 0x0 | HMIC_KEYDOWN_PENDING<br>Hmic Key Down Irq pending bit, write 1 to clear<br>0: No Pending Interrupt<br>1: Key down Irq Pending Interrupt |
| 0 | R/W | 0x0 | HMIC_DATA_PENDING<br>Hmic Data Irq pending bit, write 1 to clear<br>0: No Pending Interrupt<br>1: Data Irq Pending Interrupt |

## Reg 48h_DAC Digital Control Register

| Default: 0x0000 | | | Register Name: DAC_DIG_CTRL |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15 | R/W | 0x0 | ENDA.<br>DAC Digital Part Enable |

| | | | 0: Disabe |
| | | | 1: Enable |
| 14 | R/W | 0x0 | ENHPF |
| | | | HPF Function Enable |
| | | | 0: Enable |
| | | | 1: Disable |
| 13 | R/W | 0x0 | DAFIR32 |
| | | | Enable 32-tap FIR filter |
| | | | 0: 64-tap |
| | | | 1: 32-tap |
| 12 | R/W | 0x0 | Reserved |
| 11:8 | R/W | 0x0 | MODQU |
| | | | Internal DAC Quantization Levels |
| | | | Levels=[7*(21+MODQU[3:0])]/128 |
| | | | Default levels=7*21/128=1.15 |
| 7:0 | R/W | 0x0 | Reserved |

## Reg 49h_DAC Volume Control Register

| Default: 0xA0A0 | | | Register Name: DAC_VOL_CTRL |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:8 | R/W | 0xA0 | DAC_VOL_L |
| | | | DAC left channel volume |
| | | | (-119.25dB To 71.25dB, 0.75dB/Step) |
| | | | 0x00: Mute |
| | | | 0x01: -119.25dB |
| | | | ……………… |
| | | | 0x9F = -0.75dB |
| | | | 0xA0 = 0dB |
| | | | 0xA1 = 0.75dB |
| | | | ……………… |
| | | | 0xFF = 71.25dB |
| 7:0 | R/W | 0xA0 | DAC_VOL_R |
| | | | DAC right channel volume |
| | | | (-119.25dB To 71.25dB, 0.75dB/Step) |
| | | | 0x00: Mute |
| | | | 0x01: -119.25dB |
| | | | ……………… |
| | | | 0x9F = -0.75dB |
| | | | 0xA0 = 0dB |
| | | | 0xA1 = 0.75dB |
| | | | ……………… |
| | | | 0xFF = 71.25dB |

## Reg 4ch_DAC Digital Mixer Source Select Register

| Default: 0x0000 | | | Register Name: DAC_MXR_SRC |
|---|---|---|---|
| Bit | Read/Write | Default | Description |

| 15:12 | R/W | 0x0 | DACL_MXR_SRC<br>DAC left channel mixer source select<br>0: Disable    1:Enable<br>Bit15: I2S1_DA0L<br>Bit14: I2S1_DA1L<br>Bit13: I2S2_DACL<br>Bit12: ADCL |
| 11:8 | R/W | 0x0 | DACR_MXR_SRC<br>DAC right channel mixer source select<br>0: Disable    1:Enable<br>Bit11: I2S1_DA0R<br>Bit10: I2S1_DA1R<br>Bit9: I2S2_DACR<br>Bit8: ADCR |
| 7:0 | R/W | 0x0 | Reserved |

## Reg 4dh_DAC Digital Mixer Gain Control Register

| Default: 0x0000 | | | Register Name: DAC_MXR_GAIN |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15:12 | R/W | 0x0 | DACL_MXR_GAIN<br>DAC left channel mixer gain control<br>0: 0dB    1: -6dB<br>Bit15: I2S1_DA0L<br>Bit14: I2S1_DA1L<br>Bit13: I2S2_DACL<br>Bit12: ADCL |
| 11:8 | R/W | 0x0 | DACR_MXR_GAIN<br>DAC right channel mixer gain control<br>0: 0dB    1: -6dB<br>Bit11: I2S1_DA0R<br>Bit10: I2S1_DA1R<br>Bit9: I2S2_DACR<br>Bit8: ADCR |
| 7:0 | R/W | 0x0 | Reserved |

## Reg 50h_ADC Analog Control Register

| Default:0x3340 | | | Register Name: ADC_APC_CTRL |
|---|---|---|---|
| **Bit** | **R/W** | **Default** | **Description** |
| 15 | R/W | 0x0 | ADCREN<br>ADC Right channel Enable<br>0: Disable; 1: Enable |
| 14:12 | R/W | 0x3 | ADCRG<br>ADC Right channel input Gain control<br>From -4.5dB to 6dB, 1.5dB/step, default is 0dB |
| 11 | R/W | 0x0 | ADCLEN |

| | | | ADC Left channel Enable |
|---|---|---|---|
| | | | 0: Disable; 1: Enable |
| 10:8 | R/W | 0x3 | ADCLG |
| | | | ADC Left channel input Gain control |
| | | | From -4.5dB to 6dB, 1.5dB/step, default is 0dB |
| 7 | R/W | 0x0 | MBIASEN |
| | | | Master microphone BIAS Enable |
| | | | 0: Disable; 1: Enable |
| 6 | R/W | 0x1 | MMIC_BIAS_CHOPPER_EN |
| | | | Main MICrophone BIAS chopper Enable |
| | | | 0: Disable; 1: Enable |
| 5:4 | R/W | 0x0 | MMIC_BIAS_CHOPPER_CKS |
| | | | Main MICrophone BIAS chopper Clock select |
| | | | 00: 250k |
| | | | 01: 500k |
| | | | 10: 1Meg |
| | | | 11: 2Meg |
| 3 | / | / | / |
| 2 | R/W | 0x0 | HBIASMOD |
| | | | HBIAS&ADC working mode |
| | | | 0: HBIAS is enabled only when with load |
| | | | 1: HBIAS is enabled when HBIASEN write 1 |
| 1 | R/W | 0x0 | HBIASEN |
| | | | Headset microphone BIAS Enable |
| | | | 0: Disable; 1: Enable |
| 0 | R/W | 0x0 | HBIASADCEN |
| | | | Headset microphone BIAS Current sensor & ADC Enable |
| | | | 0: Disable; 1: Enable |

## Reg 51h_ADC Source Select Register

| Default:0x0000 | | | Register Name: ADC_SRC |
|---|---|---|---|
| **Bit** | **R/W** | **Default** | **Description** |
| 15:14 | / | / | / |
| 13:7 | R/W | 0x0 | RADC_MIXMUTE |
| | | | Right ADC Mixer Mute Control: |
| | | | 0: Mute; 1:On |
| | | | Bit 13: MIC1 Boost stage |
| | | | Bit 12: MIC2 Boost stage |
| | | | Bit 11: LINEINL-LINEINR |
| | | | Bit 10: LINEINR |
| | | | Bit 9: AUXINR |
| | | | Bit 8: Right output mixer |
| | | | Bit 7: Left output mixer |
| 6:0 | R/W | 0x0 | LADC_MIXMUTE |
| | | | Left ADC Mixer Mute Control: |
| | | | 0: Mute; 1:On |
| | | | Bit 6: MIC1 Boost stage |

| | | | Bit 5: MIC2 Boost stage |
|---|---|---|---|
| | | | Bit 4: LINEINL-LINEINR |
| | | | Bit 3: LINEINL |
| | | | Bit 2: AUXINL |
| | | | Bit 1: Left output mixer |
| | | | Bit 0: Right output mixer |

# Reg 52h_ADC Source Boost Control Register

| Default:0x4444 | | | Register Name: ADC_SRCBST_CTRL |
|---|---|---|---|
| Bit | R/W | Default | Description |
| 15 | R/W | 0x0 | MIC1AMPEN<br>MIC1 boost AMPlifier ENable<br>0: Disable; 1: Enable |
| 14:12 | R/W | 0x4 | MIC1BOOST<br>MIC1 boost amplifier Gain control<br>0dB when 000, and from 30dB to 48dB when 001 to 111 |
| 11 | R/W | 0x0 | MIC2AMPEN<br>MIC2 boost AMPlifier ENable<br>0: Disable; 1: Enable |
| 10:8 | R/W | 0x4 | MIC2BOOST<br>MIC2 boost amplifier Gain control<br>0dB when 000, and from 30dB to 48dB when 001 to 111 |
| 7 | R/W | 0x0 | MIC2SLT<br>MIC2 Source select<br>0: MIC2; 1: MIC3 |
| 6:4 | R/W | 0x4 | LINEIN_DIFF_PREG<br>LINEINL-LINEINR differential signal pre-amplifier gain control<br>-12dB to 9dB, 3dB/step, default is 0dB |
| 3 | / | / | / |
| 2:0 | R/W | 0x4 | AXI_PREG<br>AXI pre-amplifier gain control<br>-12dB to 9dB, 3dB/step, default is 0dB |

# Reg 53h_Output Mixer & DAC Analog Control Register

| Default:0x0f80 | | | Register Name: OMIXER_DACA_CTRL |
|---|---|---|---|
| Bit | R/W | Default | Description |
| 15 | R/W | 0x0 | DACAREN<br>Internal DAC Analog Right channel Enable<br>0:Disable<br>1:Enable |
| 14 | R/W | 0x0 | DACALEN<br>Internal DAC Analog Left channel Enable<br>0:Disable<br>1:Enable |
| 13 | R/W | 0x0 | RMIXEN |

| | | | Right Analog Output Mixer Enable<br>0:Disable<br>1:Enable |
|---|---|---|---|
| 12 | R/W | 0x0 | LMIXEN<br>Left Analog Output Mixer Enable<br>0:Disable<br>1:Enable |
| 11:9 | R/W | 0xf | HP_DCRM_EN<br>Headphone DC offset remove function enable<br>0:Disable<br>1:Enable<br>To remove the headphone buffer DC offset, this bit must be set 0xf before headphone PA enabled, and this bit must be set 0x0 before headphone PA disabled |
| 7:0 | R/W | 0x80 | Reserved |

## Reg 54h_Output Mixer Source Select Register

| Default:0x0000 | | | Register Name: OMIXER_SR |
|---|---|---|---|
| Bit | R/W | Default | Description |
| 15:14 | / | / | / |
| 13:7 | R/W | 0x0 | RMIXMUTE<br>Right Output Mixer Mute Control<br>0-Mute, 1-On<br>Bit 13: MIC1 Boost stage<br>Bit 12: MIC2 Boost stage<br>Bit 11: LINEINL-LINEINR<br>Bit 10: LINEINR<br>Bit 9: AUXINR<br>Bit 8: DACR<br>Bit 7: DACL |
| 6:0 | R/W | 0x0 | LMIXMUTE<br>Left Output Mixer Mute Control<br>0-Mute, 1-On<br>Bit 6: MIC1 Boost stage<br>Bit 5: MIC2 Boost stage<br>Bit 4: LINEINL-LINEINR<br>Bit 3: LINEINL<br>Bit 2: AUXINL<br>Bit 1: DACL<br>Bit 0: DACR |

## Reg 55h_Output Mixer Source Boost Register

| Default:0x56DB | | | Register Name: OMIXER_BST1_CTRL |
|---|---|---|---|
| Bit | R/W | Default | Description |
| 15:14 | R/W | 0x1 | HBIASSEL<br>HMICBIAS voltage level select |

| | | | 00: 1.88V |
|---|---|---|---|
| | | | 01: 2.09V |
| | | | 10: 2.33V |
| | | | 11: 2.50V |
| 13:12 | R/W | 0x1 | MBIASSEL<br>MMICBIAS voltage level select<br>00: 1.88V<br>01: 2.09V<br>10: 2.33V<br>11: 2.50V |
| 11:9 | R/W | 0x3 | AXG<br>AXin to L or R output mixer Gain control<br>From -4.5dB to 6dB, 1.5dB/step, default is 0dB |
| 8:6 | R/W | 0x3 | MIC1G<br>MIC1 to L or R output mixer Gain Control<br>From -4.5dB to 6dB, 1.5dB/step, default is 0dB |
| 5:3 | R/W | 0x3 | MIC2G<br>MIC2 to L or R output mixer Gain Control<br>From -4.5dB to 6dB, 1.5dB/step, default is 0dB |
| 2:0 | R/W | 0x3 | LINEING<br>LINEINL/R to L/R output mixer Gain Control<br>From -4.5dB to 6dB, 1.5dB/step, default is 0dB |

# Reg 56h_Headphone Output Control Register

| Default:0x0001 | | | Register Name: HPOUT_CTRL |
|---|---|---|---|
| Bit | R/W | Default | Description |
| 15 | R/W | 0x0 | RHPS<br>Right Headphone Power Amplifier (PA) Input Source Select<br>0: DACR<br>1: Right Analog Mixer |
| 14 | R/W | 0x0 | LHPS<br>Left Headphone Power Amplifier (PA) Input Source Select<br>0: DACL<br>1: Left Analog Mixer |
| 13 | R/W | 0x0 | RHPPA_MUTE<br>All input source to Right Headphone PA mute, including Right Output mixer and Internal DACR:<br>0:Mute, 1: On |
| 12 | R/W | 0x0 | LHPPA_MUTE<br>All input source to Left Headphone PA mute, including Left Output mixer and Internal DACL:<br>0:Mute, 1: On |
| 11 | R/W | 0x0 | HPPA_EN<br>Right & Left Headphone Power Amplifier Enable<br>0: Disable<br>1: Enable |
| 10 | / | / | / |

| 9:4 | R/W | 0x0 | HP_VOL<br>Headphone Volume Control, (HPVOL): Total 64 level, from 0dB to -62dB, 1dB/step, mute when 000000 |
|---|---|---|---|
| 3:2 | R/W | 0x0 | HPPA_DEL<br>Headphone delay time when start up<br>00: 4ms<br>01: 8ms<br>10: 16ms<br>11: 32ms |
| 1:0 | R/W | 0x1 | HPPA_IS<br>Headphone PA output stage current select<br>00 is minimum, 11 is maximum |

## Reg 57h_Earpiece Output Control Register

| Default:0x8200 | | | Register Name: ERPOUT_CTRL |
|---|---|---|---|
| Bit | R/W | Default | Description |
| 15 | R/W | 0x1 | Reserved |
| 14:12 | R/W | 0x0 | / |
| 12:11 | R/W | 0x0 | EAR_RAMP_TIME<br>Earpiece ramp time select<br>00: 256ms<br>01: 512ms<br>10: 640ms<br>11: 768ms |
| 10:9 | R/W | 0x1 | ESPA_OUT_CURRENT<br>Earpiece output stage current set<br>00 is minimum, 11is maximum |
| 8:7 | R/W | 0x0 | ESPSR<br>Earpiece input source select<br>00: DACR<br>01: DACL<br>10: Right Analog Mixer<br>11: Left Analog Mixer |
| 6 | R/W | 0x0 | ESPPA_MUTE<br>All input source to Earpiece PA mute, including Left Output mixer and Internal DACL:<br>0:Mute, 1: On |
| 5 | R/W | 0x0 | ESPPA_EN<br>Earpiece Power Amplifier Enable<br>0: Disable<br>1: Enable |
| 4:0 | R/W | 0x0 | ESP_VOL<br>Earpiece Volume Control, Total 31 level, from 0dB to -43.5dB, 1.5dB/step, mute when 00000 & 00001 |

# Reg 58h_Speaker Output Control Register

| Default:0x0880 | | | Register Name: SPKOUT_CTRL |
|---|---|---|---|
| Bit | R/W | Default | Description |
| 15:13 | R/W | 0x0 | Reserved |
| 12 | R/W | 0x0 | RSPKS<br>Right speaker input source select<br>0: MIXR<br>1: MIXL+MIXR |
| 11 | R/W | 0x1 | RSPKINVEN<br>Right speaker negative output enable<br>0: Disable; 1: Enable |
| 10 | / | / | / |
| 9 | R/W | 0x0 | RSPK_EN<br>Right Speaker Enable<br>0: Disable; 1: Enable |
| 8 | R/W | 0x0 | LSPKS<br>Left speaker input source select<br>0: MIXL<br>1: MIXL+MIXR |
| 7 | R/W | 0x1 | LSPKINVEN<br>Left speaker negative output enable<br>0: Disable; 1: Enable |
| 6 | / | / | / |
| 5 | R/W | 0x0 | LSPK_EN<br>Left Speaker Enable<br>0: Disable; 1: Enable |
| 4:0 | R/W | 0x0 | SPK_VOL<br>Right & Left speaker VOLume control<br>Total 31 level, from 0dB to -43.5dB, 1.5db/step, mute when 00000&00001 |

# Reg 59h_Lineout Control Register

| Default:0x8060 | | | Register Name: LOUT_CTRL |
|---|---|---|---|
| Bit | R/W | Default | Description |
| 15:8 | R/W | 0x80 | Reservd |
| 7:5 | R/W | 0x3 | LINEOUTG<br>Line out Gain Control<br>From -4.5dB to 6dB, 1.5dB/step, default is 0dB |
| 4 | R/W | 0x0 | LINEOUTEN<br>Line out Enable<br>0: disable 1: enable |
| 3 | R/W | 0x0 | LINEOUTS0<br>MIC1 Boost stage to Line out mute<br>0: Mute, 1: On |
| 2 | R/W | 0x0 | LINEOUTS1 |

| | | | MIC2 Boost stage to Line out mute<br>0: Mute, 1: On |
|---|---|---|---|
| 1 | R/W | 0x0 | LINEOUTS2<br>Right Output mixer to Line out mute<br>0: Mute, 1: On |
| 0 | R/W | 0x0 | LINEOUTS3<br>Left Output mixer to Line out mute<br>0: Mute, 1: On |

## Reg 80h_ADC DAP Left Status Register

| Default: 0x0000 | | | Register Name: AC_ADC_DAPLSTA |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:10 | R | 0x0 | Reserved |
| 9 | R | 0x0 | Left AGC saturation flag |
| 8 | R | 0x0 | Left AGC noise-threshold flag |
| 7:0 | R | 0x0 | Left Gain applied by AGC<br>(7.1 format 2s complement(-20dB – 40dB), 0.5B/ step)<br>0x50: 40dB<br>0x4F: 39.5dB<br>---------------<br>0x00: 00dB<br>0xFF: -0.5dB |

## Reg 81h_ADC DAP Right Status Register

| Default: 0x0000 | | | Register Name: AC_ADC_DAPRSTA |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 11:10 | R | 0x0 | Reserved |
| 9 | R | 0x0 | Right AGC saturation flag |
| 8 | R | 0x0 | Right AGC noise-threshold flag |
| 7:0 | R | 0x0 | Right Gain applied by AGC<br>(7.1 format 2s complement(-20dB – 40dB), 0.5dB /step)<br>0x50: 40dB<br>0x4F: 39.5dB<br>---------------<br>0x00: 00dB<br>0xFF: -0.5dB |

## Reg 82h_ADC DAP Left Channel Control Register

| Default: 0x0000 | | | Register Name: AC_ADC_DAPLCTRL |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15 | R/W | 0x0 | Reserved |
| 14 | R/W | 0x0 | Left AGC enable<br>0: disable    1: enable |
| 13 | R/W | 0x0 | Left HPF enable |

| Bit | Read/Write | Default | Description |
|---|---|---|---|
| | | | 0: disable    1: enable |
| 12 | R/W | 0x0 | Left Noise detect enable<br>0: disable    1: enable |
| 11:10 | R/W | 0x0 | Reserved |
| 9:8 | R/W | 0x0 | Left Hysteresis setting<br>00: 1dB<br>01: 2dB<br>10: 4dB<br>11: disable; |
| 7:4 | R/W | 0x0 | Left Noise debounce time<br>0000: disable<br>0001: 4/fs<br>0010: 8/fs<br>------------<br>1111: 16*4096/fs<br>$T=2^{(N+1)}/fs$, except N=0 |
| 3:0 | R/W | 0x0 | Left Signal debounce time<br>0000: disable<br>0001: 4/fs<br>0010: 8/fs<br>------------<br>1111: 16*4096/fs<br>$T=2^{(N+1)}/fs$, except N=0 |

## Reg 83h_ADC DAP Right Channel Control Register

| Default: 0x0000 | | | Register Name: AC_ADC_DAPRCTRL |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15 | R/W | 0x0 | Reserved |
| 14 | R/W | 0x0 | Right AGC enable<br>0: disable    1: enable |
| 13 | R/W | 0x0 | Right HPF enable<br>0: disable    1: enable |
| 12 | R/W | 0x0 | Right Noise detect enable<br>0: disable    1: enable |
| 11:10 | R/W | 0x0 | Reserved |
| 9: 8 | R/W | 0x0 | Right Hysteresis setting<br>00: 1dB<br>01: 2dB<br>10: 4dB<br>11: disable |
| 7: 4 | R/W | 0x0 | Right Noise debounce time<br>0000: disable<br>0001: 4/fs<br>0010: 8/fs<br>------------<br>1111: 16*4096/fs |

| | | | $T=2^{(N+1)}/fs$ ,except N=0 |
|---|---|---|---|
| 3: 0 | R/W | 0x0 | Right Signal debounce time<br>0000: disable<br>0001: 4/fs<br>0010: 8/fs<br>------------<br>1111: 16*4096/fs<br>$T=2^{(N+1)}/fs$, except N=0 |

## Reg 84h_ADC DAP Left Target Level Register

| Default: 0x2C28 | | | Register Name: AC_ADC_DAPLTL |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:14 | / | / | / |
| 13:8 | R/W | 0x2C<br>(-20dB) | Left channel target level setting(-1dB -- -30dB).(6.0format 2s complement) |
| 7:0 | R/W | 0x28<br>(20dB) | Left channel max gain setting(0-40dB).(7.1format 2s complement) |

## Reg 85h_ADC DAP Right Target Level Register

| Default: 0x2C28 | | | Register Name: AC_ADC_DAPRTL |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:14 | / | / | / |
| 13:8 | R/W | 0x2C(-20dB) | Right channel target level setting(-1dB -- -30dB).(6.0format 2s complement) |
| 7:0 | R/W | 0x28(20dB) | Right channel max gain setting (0-40dB). (7.1format 2s complement) |

## Reg 86h_ADC DAP Left High Average Coef Register

| Default: 0x0005 | | | Register Name: AC_ADC_DAPLHAC |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x0005 | Left channel output signal average level coefficient setting(the coefficient [reg86[10:0],reg87] is 3.24 format 2s complement) |

## Reg 87h_ADC DAP Left Low Average Coef Register

| Default: 0x1EB8 | | | Register Name: AC_ADC_DAPLLAC |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:0 | R/W | 0x1EB8 | Left channel output signal average level coefficient setting(the coefficient [reg86[10:0],reg87] is 3.24 format 2s complement) |

# Reg 88h_ADC DAP Right High Average Coef Register

| Default: 0x0005 | | | Register Name: AC_ADC_DAPRHAC |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x0005 | Right channel output signal average level coefficient setting(the coefficient [reg88[10:0],reg89] is 3.24 format 2s complement) |

# Reg 89h_ADC DAP Right Low Average Coef Register

| Default: 0x1EB8 | | | Register Name: AC_ADC_DAPRLAC |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15:0 | R/W | 0x1EB8 | Right channel output signal average level coefficient setting(the coefficient [reg88[10:0],reg89] is 3.24 format 2s complement) |

# Reg 8ah_ADC DAP Left Decay Time Register

| Default: 0x001F | | | Register Name: AC_ADC_DAPLDT |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15 | / | / | / |
| 14:0 | R/W | 0x001F (32x32fs) | Left decay time coefficient setting<br>0000: 1x32/fs<br>0001: 2x32/fs<br>------------------------<br>7FFF: $2^{15}$ x32/fs<br>T=(n+1)*32/fs<br>When the gain increases, the actual gain will increase 0.5dB at every decay time. |

# Reg 8bh_ADC DAP Left Attack Time Register

| Default: 0x0000 | | | Register Name: AC_ADC_DAPLAT |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15 | / | / | / |
| 14:0 | R/W | 0x0000 | Left attack time coefficient setting<br>0000: 1x32/fs<br>0001: 2x32/fs<br>------------------------<br>7FFF: $2^{15}$ x32/fs<br>T=(n+1)*32/fs<br>When the gain decreases, the actual gain will decrease 0.5dB at every attack time. |

## Reg 8ch_ADC DAP Right Decay Time Register

| Default: 0x001F | | | Register Name: AC_ADC_DAPRDT |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15 | / | / | / |
| 14:0 | R/W | 0x001F (32x32fs) | Right decay time coefficient setting<br>0000: 1x32/fs<br>0001: 2x32/fs<br>-----------------------<br>7FFF: $2^{15}$ x32/fs<br>T=(n+1)*32/fs<br>When the gain increases, the actual gain will increase 0.5dB at every decay time. |

## Reg 8dh_ADC DAP Right Attack Time Register

| Default: 0x0000 | | | Register Name: AC_ADC_DAPRAT |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15 | / | / | / |
| 14:0 | R/W | 0x0000 | Right attack time coefficient setting<br>0000: 1x32/fs<br>0001: 2x32/fs<br>-----------------------<br>7FFF: $2^{15}$ x32/fs<br>T=(n+1)*32/fs<br>When the gain decreases, the actual gain will decrease 0.5dB at every attack time. |

## Reg 8eh_ADC DAP Noise Threshold Register

| Default: 0x1E1E | | | Register Name:AC_ADC_DAPNTH |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15:13 | / | / | / |
| 12:8 | R/W | 0x1E (-90dB) | Left channel noise threshold setting.<br>0x00: -30dB<br>0x01: -32dB<br>0x02: -34dB<br>------------------------------------------<br>0x1D: -88dB<br>0x1E: -90dB<br>0x1F: -90dB(the same as 0x1E) |
| 7:5 | / | / | / |
| 4:0 | R/W | 0x1E(-90dB) | Right channel noise threshold setting(-90 -- -30dB).<br>0x00: -30dB<br>0x01: -32dB<br>0x02: -34dB<br>------------------------------------------ |

| | | | 0x1D: -88dB |
| | | | 0x1E: -90dB |
| | | | 0x1F: -90dB(the same as 0x1E |

## Reg 8fh_ADC DAP Left Input Signal High Average Coef Register

| Default: 0x0005 | | | Register Name: AC_ADC_DAPLHNAC |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x0005 | Left input signal average filter coefficient to check noise or not(the coefficient [reg8f[10:0],reg90] is 3.24 format 2s complement), always the same as the left output signal average filter's. |

## Reg 90h_ADC DAP Left Input Signal Low Average Coef Register

| Default: 0x1EB8 | | | Register Name: AC_ADC_DAPLLNAC |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:0 | R/W | 0x0005 | Left input signal average filter coefficient to check noise or not(the coefficient [reg8f[10:0],reg90] is 3.24 format 2s complement)  always the same as the left output signal average filter's |

## Reg 91h_ADC DAP Right Input Signal High Average Coef Register

| Default: 0x0005 | | | Register Name: AC_ADC_DAPRHNAC |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x0005 | Right input signal average filter coefficient to check noise or not(the coefficient [reg91[10:0],reg92] is 3.24 format 2s complement), always the same as the right output signal average filter's |

## Reg 92h_ADC DAP Right Input Signal Low Average Coef Register

| Default: 0x1EB8 | | | Register Name: AC_ADC_DAPRLNAC |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:0 | R/W | 0x1EB8 | Right input signal average filter coefficient to check noise or not(the coefficient [reg91[10:0],reg92] is 3.24 format 2s complement),  always the same as the right output signal average filter's |

## Reg 93h_ADC DAP High HPF Coef Register

| Default: 0x00FF | | | Register Name: AC_DAPHHPFC |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:11 | / | / | / |

| 10:0 | R/W | 0x00FF | HPF coefficient setting(the coefficient [reg93[10:0],reg14] is 3.24 format 2s complement) |
|------|-----|--------|------|

## Reg 94h_ADC DAP Low HPF Coef Register

| Default: 0xFAC1 | | | Register Name: AC_DAPLHPFC |
|------|------|------|------|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15:0 | R/W | 0xFAC1 | HPF coefficient setting(the coefficient [reg93[10:0],reg14] is 3.24 format 2s complement) |

## Reg 95h_ADC DAP Optimum Register

| Default: 0x0000 | | | Register Name: AC_DAPOPT |
|------|------|------|------|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15:11 | / | / | / |
| 10 | R/W | 0 | Left energy default value setting(include the input and output)<br>0: min<br>1: max |
| 9:8 | R/W | 00 | Left channel gain hystersis setting.<br>The different between target level and the signal level must larger than the hystersis when the gain change.<br>00: 0.4375db<br>01: 0.9375db<br>10: 1.9375db<br>11: 3db |
| 7:6 | / | / | / |
| 5 | R/W | 0 | The input signal average filter coefficient setting<br>0:   is the [reg8f[10:0], reg90] and [reg91[1:0], reg92];<br>1:   is the [reg86[10:0], reg87] and [reg88[1:0], reg89]; |
| 4 | R/W | 0 | AGC output when the channel in noise state<br>0: output is zero<br>1: output is the input data |
| 3 | / | / | / |
| 2 | R/W | 0 | Right energy default value setting(include the input and output)<br>0: min<br>1: max |
| 1:0 | R/W | 00 | Right channel gain hystersis setting.<br>The different between target level and the signal level must larger than the hystersis when the gain change.<br>00: 0.4375db<br>01: 0.9375db<br>10: 1.9375db<br>11: 3db |

# Reg a0h_DAC DAP Control Register

| Default: 0x0000 | | | Register Name: AC_DAC_DAPCTRL |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:3 | / | / | / |
| 2 | R/W | 0 | DRC enable control<br>0: disable    1: enable |
| 1 | R/W | 0 | Left channel HPF enable control<br>0: disable    1: enable |
| 0 | R/W | 0 | Right channel HPF enable control<br>0: disable    1: enable |

# Reg a1h_DAC DAP High HPF Coef Register

| Default: 0x00FF | | | Register Name: AC_DAC_DAPHHPFC |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:11 | / | / | / |
| 10:0 | R/W | 0xFF | HPF coefficient setting(the coefficient [reg a1[10:0], reg a2] is 3.24 format 2s complement) |

# Reg a2h_DAC DAP Low HPF Coef Register

| Default: 0xFAC1 | | | Register Name: AC_DAC_DAPLHPFC |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:0 | R/W | 0xFAC1 | HPF coefficient setting(the coefficient [reg a1[10:0], reg a2] is 3.24 format 2s complement) |

# Reg a3h_DAC DAP Left High Energy Average Coef Register

| Default: 0x0100 | | | Register Name: AC_DAC_DAPLHAVC |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x0100 | Left channel energy average filter coefficient setting(the coefficient [reg a3[10:0], reg a4] is 3.24 format 2s complement ) |

# Reg a4h_DAC DAP Left Low Energy Average Coef Register

| Default: 0x0000 | | | Register Name: AC_DAC_DAPLLAVC |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:0 | R/W | 0x0000 | Left channel energy average filter coefficient setting(the coefficient [rega3[10:0],rega4] is 3.24 format 2s complement) |

# Reg a5h_DAC DAP Right High Energy Average Coef Register

| Default: 0x0100 | | | Register Name: AC_DAC_DAPRHAVC |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x0100 | Right channel energy average filter coefficient setting(the coefficient [reg a5[10:0], reg a6] is 3.24 format 2s complement ) |

# Reg a6h_DAC DAP Right Low Energy Average Coef Register

| Default: 0x0000 | | | Register Name: AC_DAC_DAPRLAVC |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15:0 | R/W | 0x0000 | Right channel energy average filter coefficient setting(the coefficient [reg a5[10:0],reg a6] is 3.24 format 2s complement) |

# Reg a7h_DAC DAP High Gain Decay Time Coef Register

| Default: 0x0100 | | | Register Name: AC_DAC_DAPHGDEC |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x0100 | Gain smooth filter decay time coefficient setting(the coefficient [reg a7[10:0], reg a8] is 3.24 format 2s complement ) |

# Reg a8h_DAC DAP Low Gain Decay Time Coef Register

| Default: 0x0000 | | | Register Name: AC_DAC_DAPLGDEC |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15:0 | R/W | 0x0000 | Gain smooth filter decay time coefficient setting(the coefficient [reg a7[10:0], reg a8] is 3.24 format 2s complement ) |

# Reg a9h_DAC DAP High Gain Attack Time Coef Register

| Default: 0x0100 | | | Register Name: AC_DAC_DAPHGATC |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x0100 | Gain smooth filter attack time coefficient setting(the coefficient [reg a9[10:0], reg aa] is 3.24 format 2s complement ) |

# Reg aah_DAC DAP Low Gain Attack Time Coef Register

| Default: 0x0000 | | | Register Name: AC_DAC_DAPLGATC |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |

| 15:0 | R/W | 0x0000 | Gain smooth filter attack time coefficient setting(the coefficient [reg a9[10:0], reg aa] is 3.24 format 2s complement ) |
|------|-----|--------|------------------------------------------------------------------------------------------------------------------------|

## Reg abh_DAC DAP High Energy Threshold Register

| Default: 0x04FB | | | Register Name: AC_DAC_DAPHETHD |
|-----------------|-----------|---------|--------------------------------|
| Bit | Read/Write | Default | Description |
| 15:0 | R/W | 0x04FB | The DRC Energy compress threshold parameter T setting(the T = [reg ab, reg ac] is 8.24 format 2s complement ) |

## Reg ach_DAC DAP Low Energy Threshold Register

| Default: 0x9ED0 | | | Register Name: AC_DAC_DAPLETHD |
|-----------------|-----------|---------|--------------------------------|
| Bit | Read/Write | Default | Description |
| 15:0 | R/W | 0x9ED0 | The DRC Energy compress threshold parameter T setting(the T = [reg ab, reg ac] is 8.24 format 2s complement ) |

## Reg adh_DAC DAP High Gain K Parameter Register

| Default: 0x0780 | | | Register Name: AC_DAC_DAPHGKPA |
|-----------------|-----------|---------|--------------------------------|
| Bit | Read/Write | Default | Description |
| 15:11 | / | / | / |
| 10:0 | R/W | 0x0780 | The DRC gain curve slope k parameter setting(the K = [reg ad[10:0], reg ae] is 3.24 format 2s complement ) |

## Reg aeh_DAC DAP Low Gain K Parameter Register

| Default: 0x0000 | | | Register Name: AC_DAC_DAPLGKPA |
|-----------------|-----------|---------|--------------------------------|
| Bit | Read/Write | Default | Description |
| 15:0 | R/W | 0x0000 | The DRC gain curve slope k parameter setting(the K = [reg ad[10:0], reg ae] is 3.24 format 2s complement ) |

## Reg afh_DAC DAP High Gain Offset Parameter Register

| Default: 0x0100 | | | Register Name: AC_DAC_DAPHGOPA |
|-----------------|-----------|---------|--------------------------------|
| Bit | Read/Write | Default | Description |
| 15:13 | / | / | / |
| 12:0 | R/W | 0x0100 | The DRC gain curve offset O parameter setting(the O = [reg af[12:0], reg b0] is 5.24 format 2s complement ) |

## Reg b0h_DAC DAP Low Gain Offset Parameter Register

| Default: 0x0000 | | | Register Name: AC_DAC_DAPLGOPA |
|-----------------|-----------|---------|--------------------------------|
| Bit | Read/Write | Default | Description |

| | | | |
|---|---|---|---|
| 15:0 | R/W | 0x0000 | The DRC gain curve offset O parameter setting(the K = [reg af[12:0], regb0] is 5.24 format 2s complement ) |

# Reg b1h _DAC DAP Optimum Register

| Default: 0x0000 | | | Register Name: AC_DAC_DAPOPT |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15:6 | / | / | / |
| 5 | R/W | 0 | DRC gain defaut value setting<br>0: The default gain is 1<br>1: The default gain is 0 |
| 4:0 | R/W | 0x00 | The hysteresis of the gain smooth filter to use the decay time coefficient or the attack time coefficient.<br>When in the decay time state, if g(n-1)-g(n)>hysteresis, then the state will change to attack time state, and when in the attack time, if g(n)-g(n-1)>hysteresis, then the state will change to decay time state. Note the hysteresis of 0x00 and 0x04 is the same.<br>00000: $2^{-16}$<br>00001: $2^{-19}$<br>00010: $2^{-18}$<br>00011: $2^{-17}$<br>00100: $2^{-16}$<br>----------------<br>10011: $2^{-1}$<br>10100 ~11111: 1<br>hysteresis = $2^{n-20}$ ,except n=0x00, and n less 0x14. |

# Reg b4h_ADC DAP Enable Register

| Default: 0x0000 | | | Register Name: ADC_DAP_ENA |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15 | R/W | 0x0 | I2S1_ADCL0_AGC_ENA<br>I2S1 ADC timeslot 0 left channel AGC enable<br>0: Disable<br>1: Enable |
| 14 | R/W | 0x0 | I2S1_ADCR0_AGC_ENA<br>I2S1 ADC timeslot 0 right channel AGC enable<br>0: Disable<br>1: Enable |
| 13 | R/W | 0x0 | I2S1_ADCL1_AGC_ENA<br>I2S1 ADC timeslot 1 left channel AGC enable<br>0: Disable<br>1: Enable |
| 12 | R/W | 0x0 | I2S1_ADCR1_AGC_ENA<br>I2S1 ADC timeslot 1 right channel AGC enable<br>0: Disable |

| | | | 1: Enable |
|---|---|---|---|
| 11 | R/W | 0x0 | I2S2_ADCL_AGC_ENA<br>I2S2 ADC left channel AGC enable<br>0: Disable<br>1: Enable |
| 10 | R/W | 0x0 | I2S2_ADCR_AGC_ENA<br>I2S2 ADC right channel AGC enable<br>0: Disable<br>1: Enable |
| 9 | R/W | 0x0 | I2S2_DACL_AGC_ENA<br>I2S2 DAC left channel AGC enable<br>0: Disable<br>1: Enable |
| 8 | R/W | 0x0 | I2S2_DACR_AGC_ENA<br>I2S2 DAC right channel AGC enable<br>0: Disable<br>1: Enable |
| 7 | R/W | 0x0 | ADCL_AGC_ENA<br>ADC left channel AGC enable<br>0: Disable<br>1: Enable |
| 6 | R/W | 0x0 | ADCR_AGC_ENA<br>ADC right channel AGC enable<br>0: Disable<br>1: Enable |
| 5:0 | R/W | 0x0 | Reserved |

# Reg b5h_DAC DAP Enable Register

| Default: 0x0000 | | | Register Name: DAC_DAP_ENA |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15 | R/W | 0x0 | I2S1_DAC0_DRC_ENA<br>I2S1 DAC timeslot 0 DRC enable<br>0: Disable<br>1: Enable |
| 14 | R/W | 0x0 | Reserved |
| 13 | R/W | 0x0 | I2S1_DAC1_DRC_ENA<br>I2S1 DAC timeslot 1 DRC enable<br>0: Disable<br>1: Enable |
| 12 | R/W | 0x0 | Reserved |
| 11 | R/W | 0x0 | I2S2_DAC_DRC_ENA<br>I2S2 DAC DRC enable<br>0: Disable<br>1: Enable |
| 10:8 | R/W | 0x0 | Reserved |
| 7 | R/W | 0x0 | DAC_DRC_ENA |

| | | | DAC DRC enable<br>0: Disable<br>1: Enable |
|---|---|---|---|
| 6:0 | R/W | 0x0 | Reserved |

## Reg b8h_SRC1 Control 1 Register

| Default: 0x0000 | | | Register Name: SRC1_CTRL1 |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15 | R/W | 0x0 | SRC1_RATI_ENA<br>SRC1 Manual setting ratio enable<br>0-disable 1-enable |
| 14 | R | 0x0 | SRC1_LOCK_STS<br>SRC1 Ratio lock status<br>0-not locked 1-locked |
| 13 | R | 0x0 | SRC1_FIFO_OVR<br>SRC1 FIFO Overflow status<br>0-normal 1-overflowed |
| 12:10 | R | 0x0 | SRC1_FIFO_LEV_[8:6]<br>SRC1 FIFO Level high 3-bit |
| 9:0 | R/W | 0x0 | SRC1_RATI_SET_[25:16]<br>Manual setting ratio high 10-bit |

## Reg b9h_SRC1 Control 2 Register

| Default: 0x0000 | | | Register Name: SRC1_CTROL2 |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15:0 | R/W | 0x0 | SRC1_RATI_StET_[15:0]<br>Manual setting ratio low 16-bi |

## Reg bah_SRC1 Control 3 Register

| Default: 0x0040 | | | Register Name: SRC1_CTRL3 |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15:10 | R | 0x0 | SRC1_FIFO_LEV_[5:0]<br>SRC1 FIFO Level low 6-bit |
| 9:0 | R | 0x40 | SRC1_RATI_VAL_[25:16]<br>Calculated ratio high 10-bit |

## Reg bbh_SRC1 Control 4 Register

| Default: 0x0000 | | | Register Name: SRC1_CTRL4 |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15:0 | R | 0x0 | SRC1_RATI_VAL_[15:0]<br>Calculated ratio low 16-bit |

## Reg bch_SRC2 Control 1 Register

| Default: 0x0000 | | | Register Name: SRC2_CTRL1 |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15 | R/W | 0x0 | SRC2_RATI_ENA<br>SRC2 Manual setting ratio enable<br>0-disable 1-enable |
| 14 | R | 0x0 | SRC2_LOCK_STS<br>SRC2 Ratio lock status<br>0-not locked 1-locked |
| 13 | R | 0x0 | SRC2_FIFO_OVR<br>SRC2 FIFO Overflow status<br>0-normal 1-overflowed |
| 12:10 | R | 0x0 | SRC2_FIFO_LEV_[8:6]<br>SRC2 FIFO Level high 3-bit |
| 9:0 | R/W | 0x0 | SRC2_RATI_SET_[25:16]<br>Manual setting ratio high 10-bit |

## Reg bdh_SRC2 Control 2 Register

| Default: 0x0000 | | | Register Name: SRC2_CTRL2 |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15:0 | R/W | 0x0 | SRC2_RATI_SET_[15:0]<br>Manual setting ratio low 16-bit |

## Reg beh_SRC2 Control 3 Register

| Default: 0x0040 | | | Register Name: SRC2_CTRL3 |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15:10 | R | 0x0 | SRC2_FIFO_LEV_[5:0]<br>SRC2 FIFO Level low 6-bit |
| 9:0 | R | 0x0 | SRC2_RATI_VAL_[25:16]<br>Calculated ratio high 10-bit |

## Reg bfh_SRC2 Control 4 Register

| Default: 0x0000 | | | Register Name: SRC2_CTRL4 |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15:0 | R | 0x0 | SRC2_RATI_VAL_[15:0]<br>Calculated ratio low 16-bit |

## Reg c0h_RTC Analog Control Register

| Default: 0x003F | | | Register Name: CLK32KOUT_ACTRL |
|---|---|---|---|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15:8 | R/W | 0x00 | Reserved |

| 7 | R/W | 0x0 | CLK32AP_OD_CTR<br>CLK32KAP Output Pin Open Drain mode control<br>0: push-pull<br>1: reserved |
|---|---|---|---|
| 6:4 | R/W | 0x3 | VBG_TRM<br>VIO_RTC Voltage trimming<br>0: 1.08V    1:  1.12V<br>2: 1.16V    3:  1.2V<br>4: 1.24V    5:  1.28V<br>6: 1.32V    7:  1.36V |
| 3:2 | R/W | 0x3 | XTAL_G<br>xtal gain control<br>3: largest gain<br>0: smallest gain |
| 1 | R/W | 0x1 | XTAL_DEB<br>xtal fater startup config<br>0: slower startup<br>1: faster startup |
| 0 | R/W | 0x1 | XTAL_EN<br>xtal enable<br>0: xtal disable<br>1: xtal enable |

## Reg c1h_CK32K Output Control Register 1

| Default: 0x00e1 | | | Register Name: CK32K_OUT_CTRL1 |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:8 | R/W | 0x0 | Reserved |
| 7:5 | R/W | 0x3 | CK32KAP_PRE_DIV<br>Pre-division after 4MHz input from ADDA.<br>000: 1<br>001: 2<br>010: 4<br>011: 8<br>100: 16<br>101: 32<br>110: 64<br>111: 122(32KHz) |
| 4 | R/W | 0x0 | CK32KAP_MUX_SEL<br>CK32KAP Output source select control.<br>0: 32KHz from RTC<br>1: 4MHz from ADDA |
| 3:1 | R/W | 0x0 | CK32KAP_POST_DIV<br>Post-division after clock selection.<br>000: 1<br>001: 2<br>010: 4<br>011: 8 |

| | | | 100: 16 |
| | | | 101: 32 |
| | | | 110: 64 |
| | | | 111: 128 |
| 0 | R/W | 0x1 | CK32KAP_ENA |
| | | | CK32KAP Output enable control. |
| | | | 0: Disable output |
| | | | 1: Enable output |

## Reg c2h_CK32K Output Control Register 2

| Default: 0x0000 | | | Register Name: CK32K_OUT_CTRL2 |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:8 | R/W | 0x0 | Reserved |
| 7:5 | R/W | 0x0 | CK32KBB_PRE_DIV |
| | | | Pre-division after 4MHz input from ADDA. |
| | | | 000: 1 |
| | | | 001: 2 |
| | | | 010: 4 |
| | | | 011: 8 |
| | | | 100: 16 |
| | | | 101: 32 |
| | | | 110: 64 |
| | | | 111: 122(32KHz) |
| 4 | R/W | 0x0 | CK32KBB_MUX_SEL |
| | | | CK32KBB Output source select control. |
| | | | 0: 32KHz from RTC |
| | | | 1: 4MHz from ADDA |
| 3:1 | R/W | 0x0 | CK32KBB_POST_DIV |
| | | | Post-division after clock selection. |
| | | | 000: 1 |
| | | | 001: 2 |
| | | | 010: 4 |
| | | | 011: 8 |
| | | | 100: 16 |
| | | | 101: 32 |
| | | | 110: 64 |
| | | | 111: 128 |
| 0 | R/W | 0x0 | CK32KBB_ENA |
| | | | CK32KBB Output enable control. |
| | | | 0: Disable output |
| | | | 1: Enable output |

## Reg c3h_CK32K Output Control Register 3

| Default: 0x0000 | | | Register Name: CK32K_OUT_CTRL3 |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:8 | R/W | 0x0 | Reserved |

| Bit | Read/Write | Default | Description |
|---|---|---|---|
| 7:5 | R/W | 0x0 | CK32KMD_PRE_DIV<br>Pre-division after 4MHz input from ADDA.<br>000: 1<br>001: 2<br>010: 4<br>011: 8<br>100: 16<br>101: 32<br>110: 64<br>111: 122(32KHz) |
| 4 | R/W | 0x0 | CK32KMD_MUX_SEL<br>CK32KMD Output source select control.<br>0: 32KHz from RTC<br>1: 4MHz from ADDA |
| 3:1 | R/W | 0x0 | CK32KMD_POST_DIV<br>Post-division after clock selection.<br>000: 1<br>001: 2<br>010: 4<br>011: 8<br>100: 16<br>101: 32<br>110: 64<br>111: 128 |
| 0 | R/W | 0x0 | CK32KMD_ENA<br>CK32KMD Output enable control.<br>0: Disable output<br>1: Enable output |

## Reg c6h_RTC Reset Register

| Default: 0x0000 | | | Register Name: RTC_RST_REG |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:8 | WO | 0x0 | RTC_KEY_FIELD.<br>RTC key field should be written at value 0x53. Writing any other value in this field aborts the write operation. |
| 7:1 | / | / | / |
| 0 | R/W | 0x0 | RTC_RESET.<br>When this bit is set to 1, then all registers of time will be reset to default values.<br>0: No effect;<br>1: Reset relevant registers. |

## Reg c7h_RTC Control Register

| Default: 0x0000 | | | Register Name: RTC_CTRL_REG |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15 | R/W | 0x0 | RTC_SIM |

| | | | RTC simulation bit. |
|---|---|---|---|
| | | | When this bit is set '1', the relevant registers will rolling-over faster, such as second/minute/hour ext. |
| | | | 0: Normal mode, |
| | | | 1: Simulation mode. |
| 14:3 | / | / | / |
| 2 | R/W | 0x0 | Error mode<br>0 = Do not affect current Time/Week/Date<br>1 = Set the wrong segment to max value |
| 1 | R/W | 0x0 | RTC_STOP<br>RTC stop bit.<br>When this bit is set '1', the relevant registers will stop rolling-over, such as second/minute/hour ext.<br>0: No stop,<br>1: Stop rolling-over. |
| 0 | R/W | 0x0 | 12H_24H_MODE.<br>0: 12 hour mode.<br>1: 24 hour mode. |

## Reg c8h_RTC Seconds Register

| Default: 0x0000 | | | Register Name: RTC_SEC_REG |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:7 | / | / | / |
| 6:0 | R/W | 0x0 | RTC_SEC<br>These bits represent the current second value coded in BCD format.<br>The value should be from 0 to 59.<br>For example, if the [6:0] is '1011001', this represents the value 59. |

## Reg c9h_RTC Minutes Register

| Default: 0x0000 | | | Register Name: RTC_MIN_REG |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:7 | / | / | / |
| 6:0 | R/W | 0x0 | RTC_MIN<br>These bits represent the current minute value coded in BCD format.<br>The value should be from 0 to 59. |

## Reg cah_RTC Hours Register

| Default: 0x0001 | | | Register Name: RTC_HOU_REG |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:9 | / | / | / |
| 8 | R/W | 0x0 | AM_PM_SEL<br>AM/PM select.<br>0: AM,<br>1: PM. |

| 7:6 | / | / | / |
|------|------|------|------|
| 5:0 | R/W | 0x1 | RTC_HOU<br>These bits represent the current hour value coded in BCD format.<br>The value should be from 0 to 23. |

## Reg cbh_RTC Weekdays Register

| Default: 0x0000 | | | Register Name: RTC_WEE_REG |
|------|------|------|------|
| Bit | Read/Write | Default | Description |
| 15:3 | / | / | / |
| 2:0 | R/W | 0x0 | RTC_WEE<br>These bits represent the current weekday value coded in BCD format. The value should be from 0 to 6.<br>000: Sunday<br>001: Monday<br>010: Tuesday<br>011: Wednesday<br>100: Thursday<br>101: Friday<br>110: Saturday |

## Reg cch_RTC Days Register

| Default: 0x0001 | | | Register Name: RTC_DAY_REG |
|------|------|------|------|
| Bit | Read/Write | Default | Description |
| 15:6 | / | / | / |
| 5:0 | R/W | 0x1 | RTC_DAY<br>These bits represent the current day value coded in BCD format.<br>The value should be from 1 to 31. |

## Reg cdh_RTC Months Register

| Default: 0x0001 | | | Register Name: RTC_MON_REG |
|------|------|------|------|
| Bit | Read/Write | Default | Description |
| 15:5 | / | / | / |
| 4:0 | R/W | 0x1 | RTC_MON<br>These bits represent the current day value coded in BCD format.<br>The value should be from 1 to 12. |

## Reg ceh_RTC Years Register

| Default: 0x0000 | | | Register Name: RTC_YEA_REG |
|------|------|------|------|
| Bit | Read/Write | Default | Description |
| 15 | R/W | 0x0 | LEAP_YEAR<br>0: Not leap year<br>1: Leap year.<br>This bit will not set by hardware. It should be set or clear by |

| | | | software. |
|---|---|---|---|
| 14:8 | / | / | / |
| 7:0 | R/W | 0x0 | RTC_YEA<br>These bits represent the current day value coded in BCD format.<br>The max value is 99(0x10011001). |

## Reg cfh_RTC Update Trigger

| Default: 0x0000 | | | Register Name: RTC_UPD_TRIG |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15 | R/W | 0x0 | Time/Week/Date write trigger<br>0 = Nothing will happen.<br>1 = Writing a 1 to this bit will update the Time/Week/Date value.<br>This bit will always be 0 when being read. |
| 14:1 | R/W | 0x0 | Reserved |
| 0 | R/W | 0x0 | REG_C8H-REG_CEH Read control<br>0: Read the effective real time clock value<br>1: Read the value of REG_C8H-REG_CEH written by host |

## Reg d0h_Alarm Interrupt Enable Register

| Default: 0x0000 | | | Register Name: ALM_INT_ENA |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:1 | / | / | / |
| 0 | R/W | 0x0 | ALM_INT_ENA<br>Alarm interrupt enable.<br>0: Alarm interrupt disable<br>1: Alarm interrupt enable |

## Reg d1h_Alarm Interrupt Status Register

| Default: 0x0000 | | | Register Name: ALM_INT_STA_REG |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:1 | / | / | / |
| 0 | R/W | 0x0 | ALM_INT_STS<br>Alarm interrupt status. Set 1 to this bit will clear it.<br>0: Alarm interrupt is not pending;<br>1: Alarm interrupt is pending. |

## Reg d8h_Alarm Seconds Register

| Default: 0x0000 | | | Register Name: ALM_SEC_REG |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15 | R/W | 0x0 | ALM_SEC_ENA<br>Second alarm enable bit.<br>0: Disable second alarm;<br>1: Enable second alarm. |

| 14:7 | / | / | / |
|------|---|---|---|
| 6:0 | R/W | 0x0 | ALM_SEC_SET<br>These bits represent the current second value coded in BCD format.<br>The value should be from 0 to 59.<br>For example, if the [6:0] is '1011001', this represents the value 59. |

## Reg d9h_Alarm Minutes Register

| Default: 0x0000 | | | Register Name: ALM_MIN_REG |
|-----------------|---|---|----------------------------|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15 | R/W | 0x0 | ALM_MIN_ENA<br>Minute alarm enable bit.<br>0: Disable minute alarm;<br>1: Enable minute alarm. |
| 14:7 | / | / | / |
| 6:0 | R/W | 0x0 | ALM_MIN_SET<br>These bits represent the current minute value coded in BCD format.<br>The value should be from 0 to 59. |

## Reg dah_Alarm Hours Register

| Default: 0x0001 | | | Register Name: ALM_HOU_REG |
|-----------------|---|---|----------------------------|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15 | R/W | 0x0 | ALM_HOU_ENA<br>Hour alarm enable bit.<br>0: Disable hour alarm;<br>1: Enable hour alarm. |
| 14:9 | / | / | / |
| 8 | R/W | 0x0 | AM_PM_SEL<br>AM/PM select.<br>0: AM,<br>1: PM. |
| 7:6 | / | / | / |
| 5:0 | R/W | 0x1 | ALM_HOU_SET<br>These bits represent the current hour value coded in BCD format.<br>The value should be from 0 to 23. |

## Reg dbh_Alarm Weekdays Register

| Default: 0x0000 | | | Register Name: ALM_WEEK_REG |
|-----------------|---|---|-----------------------------|
| **Bit** | **Read/Write** | **Default** | **Description** |
| 15 | R/W | 0x0 | ALM_WEE_ENA<br>Week alarm enable bit.<br>0: Disable hour alarm;<br>1: Enable hour alarm. |
| 14:3 | / | / | / |
| 2:0 | R/W | 0x0 | ALM_WEE_SET |

These bits represent the current weekday value coded in BCD format. The value should be from 0 to 6.

000: Sunday

001: Monday

010: Tuesday

011: Wednesday

100: Thursday

101: Friday

110: Saturday

## Reg dch_Alarm Days Register

| Default: 0x0001 | | | Register Name: ALM_DAY_REG |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15 | R/W | 0x0 | ALM_DAY_ENA<br>Day alarm enable bit.<br>0: Disable day alarm;<br>1: Enable day alarm. |
| 14:6 | / | / | / |
| 5:0 | R/W | 0x1 | ALM_DAY_SET<br>These bits represent the current day value coded in BCD format. The value should be from 1 to 31. |

## Reg ddh_Alarm Months Register

| Default: 0x0001 | | | Register Name: ALM_MON_REG |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15 | R/W | 0x0 | ALM_MON_ENA<br>Month alarm enable bit.<br>0: Disable month alarm;<br>1: Enable month alarm. |
| 14:5 | / | / | / |
| 4:0 | R/W | 0x1 | ALM_MON_SET<br>These bits represent the current day value coded in BCD format. The value should be from 1 to 12. |

## Reg deh_Alarm Years Register

| Default: 0x0000 | | | Register Name: ALM_YEA_REG |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15 | R/W | 0x0 | ALM_YEA_ENA<br>Year alarm enable bit.<br>0: Disable year alarm;<br>1: Enable year alarm. |
| 14:5 | / | / | / |
| 7:0 | R/W | 0x0 | ALM_YEA_SET |

| | | | These bits represent the current day value coded in BCD format. |
|---|---|---|---|

## Reg dfh_Alarm Update Trigger

| Default: 0x0000 | | | Register Name: ALM_UPD_TRIG |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15 | R/W | 0x0 | Time/Week/Date write trigger<br>0 = Nothing will happen.<br>1 = Writing a 1 to this bit will update the alarm Time/Week/Date value. This bit will always be 0 when being read. |
| 14:1 | R/W | 0x0 | Reserved |
| 0 | R/W | 0x0 | REG_D8H-REG_DEH Read control<br>0: Read the effective alarm setting value<br>1: Read the value of REG_D8H-REG_DEH written by host |

## Reg e0h-efh RTC General Purpose Register n(n=0-15)

| Default: 0x0000 | | | Register Name: RTC_GP_REGn |
|---|---|---|---|
| Bit | Read/Write | Default | Description |
| 15:0 | R/W | 0x0 | RTC_GP_DATn<br>These bits art used to save data.(n = 0~15) |