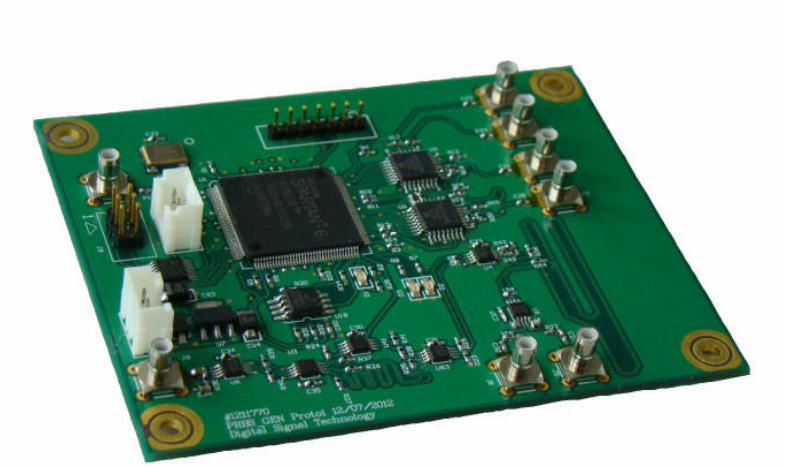
User’s Manual

PRBS/Pattern Generator

Part No. APG-3G



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Contents

1. General description

Independent 2 outputs are provided, which can be set different patterns.

2. Specification

2-1. Electrical specification

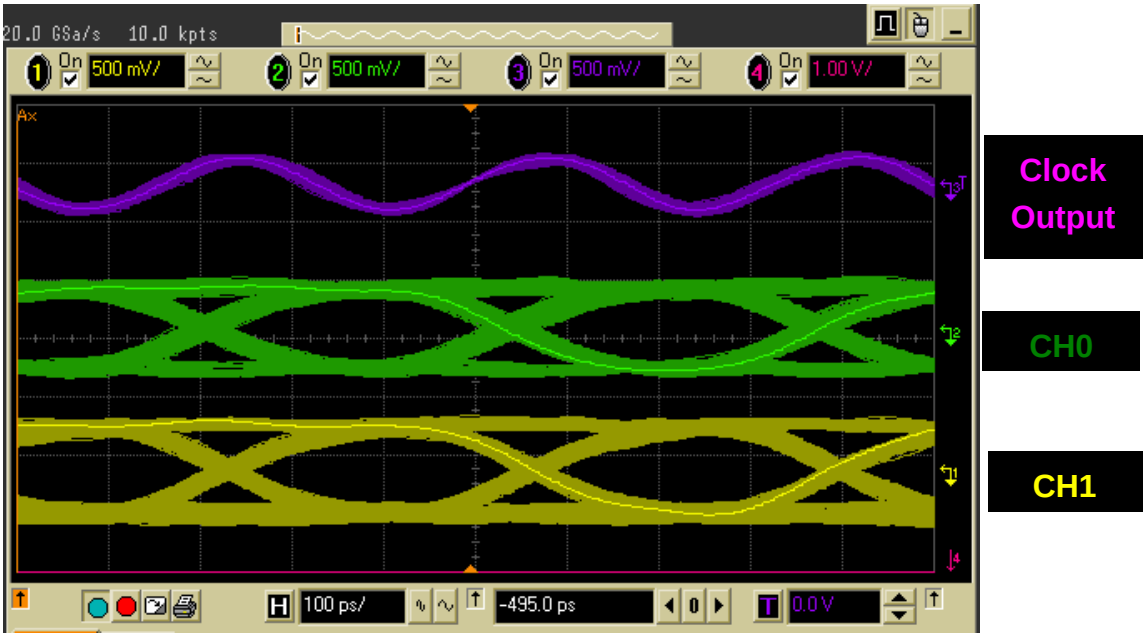
1) Input clock	SMB connector 50 ohm single end AC coupling
	Sine wave 30MHz~3000MHz −3dBm~3dBm
	Square wave 2KHz~3000MHz −3dBm~3dBm
	Shutdown/startup time is within 4nS. Duty ratio 50±10%
2) Trigger input	SMB connector 3.3V CMOS Pulled up internally at 10K ohm
	There is a jitter of +/−5nS up to pattern output start relative to trigger input.
3) Pattern output	SMB connector Differential PECL 2channels
	Individual channel patterns can be set. Skew between channels is within 20ps.
4) Clock output	SMB connector Differential PECL
	Skew between patterns is within 100ns.
5) Output bit length	1) External trigger mode
	Any bit length in a multiple of 32 of 32bit～256kbits per 1ch
	2) Continuous mode
	Any bit length in a multiple of an even number of 32bit～256kbits per 1ch
6) Bit trigger output mode	1) External trigger mode
	2) Continuous mode
8) Frequency counter	Frequency is counted by internal standard clock.
	Measurement accuracy is +/−50ppm.
	Measurement range is from 0.1MHz to 3040.0MHz.
7) LED on board	1) FPGA normal operation display
	2) Pattern outputting(also combining with alarm output)
	3) Frequency judgment of input RF clock
8) Control	Asynchronous serial communication 9600bps, 8 bit, 1 stop bit, non−parity
	Signal level 3.3VCMOS
9) Power requirements	3.3V single power +/−0.2V max. 1200mA
10)Outer dimensions	100mm x 80mm

2−2. Environmental condition

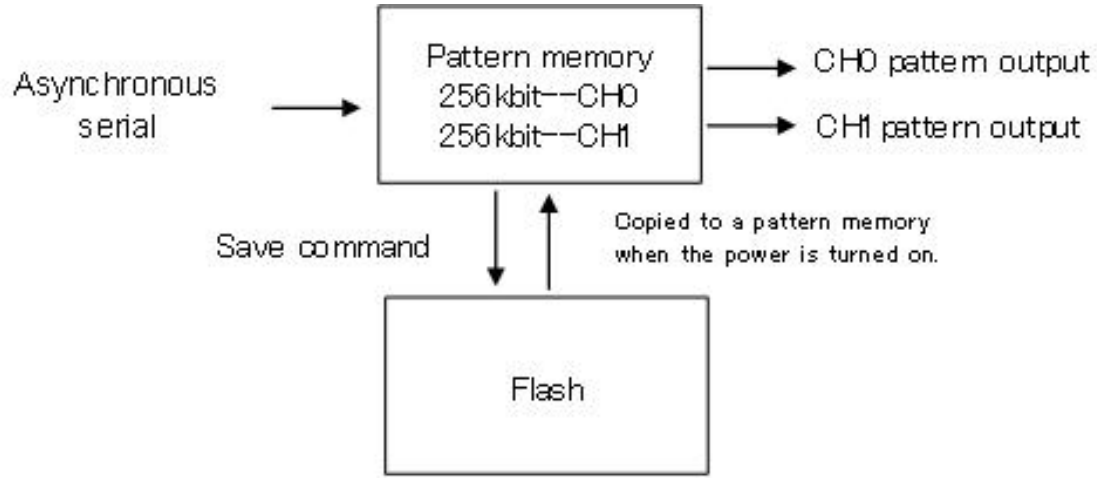
1) Operating temp. range	0~+60 degree C
2) Storage temp. range	−30~+70 degree C

2-3. Output wave example

3Gbps PCIExpress Compliance pattern



3. Memory configuration

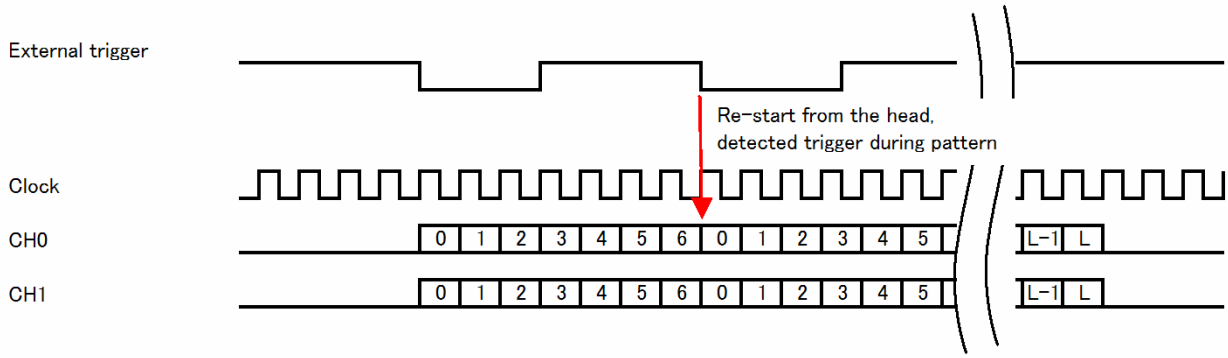


APG-3G has a pattern memory and a Flash memory. The pattern memory is volatile, and its data is lost when the power is turned OFF. The Flash memory is non-volatile, and its data is held even when the power is turned OFF. If any pattern is stored in the Flash memory, data in the Flash memory is copied to a pattern memory when the power is turned on. If no data is stored in the Flash memory, the pattern memory is cleared to “0” when the power is turned on. After storing data in a pattern memory in asynchronous serial, save it in the Flash memory with the SAVE command. Patterns of CH0 and CH1 are

output from the pattern memory. Refer to the description of the command for details of the above operation.

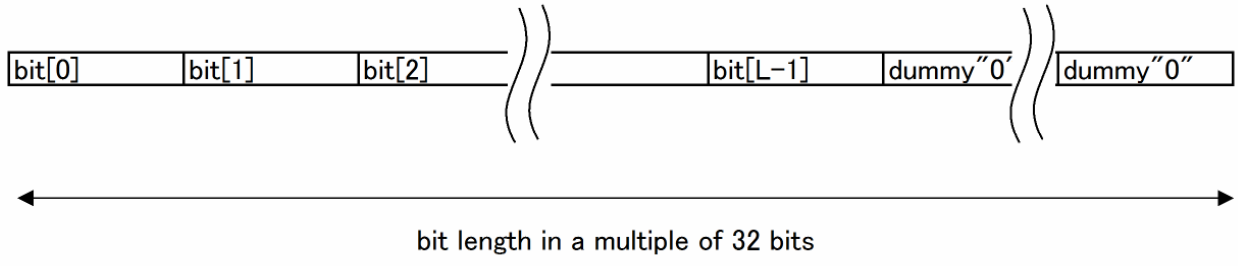
4. The explanation of pattern output mode

4-1. Description of external trigger mode

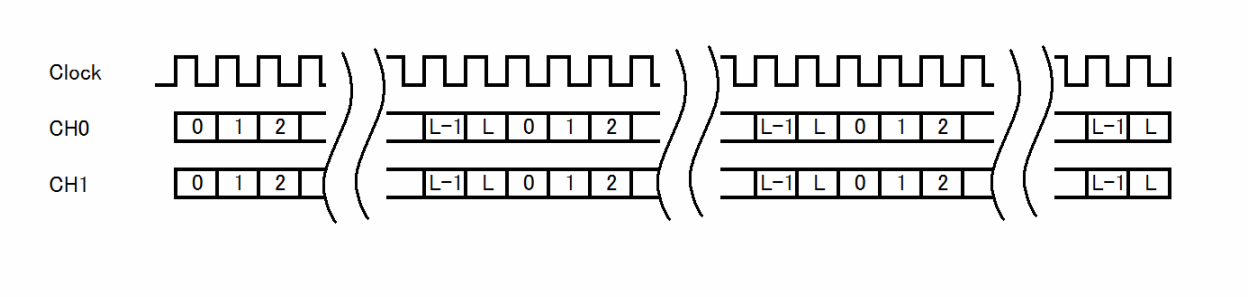


In this mode, the L level of the external trigger terminal is detected and data of a pattern memory is output only once. The bit pattern of a specified bit length is output from the head of the pattern memory. Refer to the description of the command for writing to the pattern memory and setting a bit length. If the trigger becomes the Low level before the bit pattern output is completed, pattern output is restarted at the time when the trigger becomes the Low level. The external trigger terminal is pulled up inside, and can be put to an external trigger only by connecting a push-on switch or the like. There is a jitter of ±5nS from a time when the external trigger is on to start of pattern output.

In the external trigger mode, only bit length in a multiple of 32 bits can be set. Add a dummy “0” behind the desired bit pattern and set a bit length in a multiple of 32.

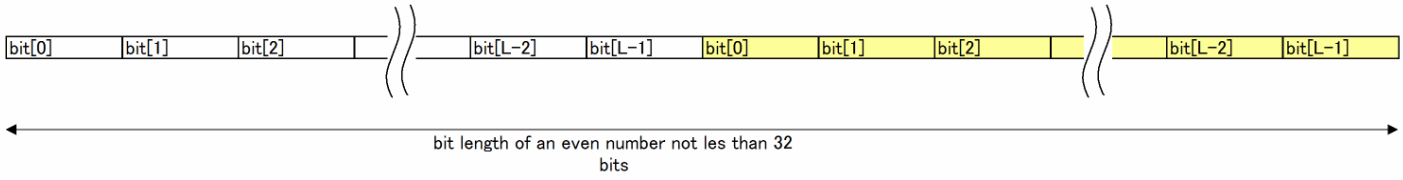


4-2.Description of continuous repetition mode

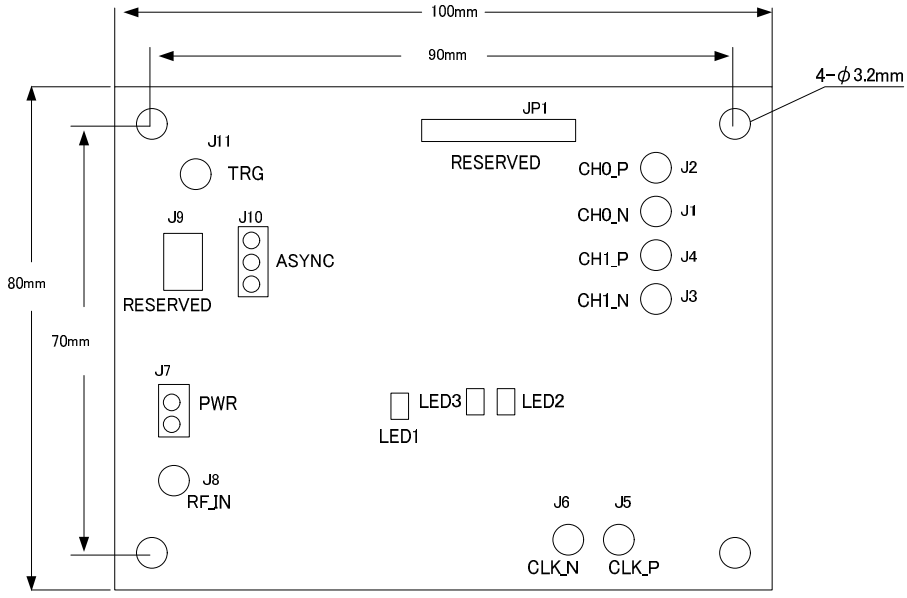


The set pattern is repeatedly output. A bit pattern is output from the head of the pattern memory, and the output returns to the head when the specified bit length is reached. Refer to the description of the command for setting the pattern memory and bit length.

In the continuous mode, a bit length of an odd number and a bit length not larger than 32 bits cannot be set. When setting a bit length of an odd number and not larger than 32 bits, couple some of the desired bit patterns to set a bit length of an even number not less than 32 bits.



5. Outer dimension



6. Connector

6-1. Connector names and description

Connector number	Name	Description
JP1	RESERVED	Not used. This connector must be opened
J1	CH0_P	PECL positive output(SMB) for CH0
J2	CH0_N	PECL negative output(SMB) for CH0
J3	CH1_P	PECL positive output(SMB) for CH0
J4	CH1_N	PECL positive output(SMB) for CH0
J5	CLK_P	PECL positive output(SMB) for Clock
J6	CLK_N	PECL positive output(SMB) for Clock
J7	PWR	Power supply terminal Part No. DF1BZ-2P-2.5DSA Manufacturer:Hirose
J8	RF_IN	Clock input(SMB)
J9	RESERVED	Not used. This connector must be opened.
J10	ASYNC	Asynchronous serial communication control Part No. DF1BZ-3P-2.5DSA Manufacturer:Hirose
J11	TRG	Input pin under external trigger mode

6-2.J7 Connecter pin assignment（Part No DF1BZ-2P-2.5DSA Manufacturer: Hirose）

Pin number.	Name	Description
1	+3.3V	Supply +3.3V
2	GND	GND

6-3.J10 Connecter pin assignment（Part No.DF1BZ-3P-2.5DSA Manufacturer: Hirose）

Pin number	Name	Description
1	GND	GND
2	RXD	Receiving port（Host → APG-3G）
3	TXD	Transmitting port(Host ← APG-3G）

7.Description of LEDs on board

LED1: Lights when FPGA is normally starting.

LED2: Lights in the continuous repetition mode and the external trigger mode.

This flashes when any error occurs in bit synchronization between 2 channels of pattern output.

LED3: Can be used for simple diagnosis of input clock quality as a result of frequency judgment for input clock.

This lights in the case of LowLimit < frequency of input clock < HighLimit.

Refer to the description of the command for setting LowLimit or HighLimit.

8. Control by asynchronous serial communication data

How to set from a PC serial port(RS-232C) is explained below.

8-1. Communication specification

Speed	9600bps
Data bits	8 bits
Stop bits	1 bit
Parity	None
Flow control	None
Logic Level	3.3V CMOS

8-2. RS-232C connection

The logic level of APG-3G serial communication is 3.3V CMOS, which cannot be directly connected to RS-232C level such as PC serial port. Level conversion between RS-232C and 3.3V CMOS is needed.

As an option, our level converter, LVC-232C is available for your convenience. Please refer to our Home Page;

http://dst.co.jp/en/manuals/lvc232c.pdf

8-3. Definition of command

A character string enclosed by “ ” means ASCII code, and “CR” and “LF” are control codes, meaning 0D (hex) and 0A (hex). "_" (underscore) means a space. If any invalid command is entered, “INVALID DATA,” “CR,” “LF” is returned. Characters to be entered shall be entered in uppercase. If a normal command is entered, “*” “CR,” “LF” is returned. In addition, the entered data is echoed back.

8-3-1. Command related to frequency counter

(1) FRQ-LO command

“FRQ-LO_dddd.d”CR LF

dddd.d: The LOW limit of the entered frequency shall be set in units of MHz. When the frequency becomes higher than the set LOW limit, LED2 lights off. Even if the frequency judgment function is not set, it does not relate to pattern output operation.

To set 2400.1MHz, enter the following data.

“FRQ-LO_2400.1” CR LF

(2) FRQ-HI command

“FRQ-HI _ddddd.d”CR LF

dddd.d: The HIGH limit of an input frequency shall be set in units of MHz. When the frequency becomes lower than the set HIGH limit, the LED2 lights off. Even if the frequency judgment function is not set, it does not relate to pattern output operation.

To set 2400.1MHz, enter the following data.

“FRQ-HI _2400.1” CR LF

8-3-2. Command related to pattern memory writing

(1) PS0 BRAM CSD command

This is a data transmission command set to the CH0 pattern memory.

When “PS0”CR LF is entered, the pattern memory acceptable status for a command CH0 is set in.

Further, transmit the PDATA command subsequently.

“BRAM_xxxx_xxxx”CR LF

“BRAM_xxxx_xxxx”CR LF

“BRAM_xxxx_xxxx”CR LF

“BRAM_xxxx_xxxx”CR LF

For xxxx, data shall be specified in hexadecimals of 4 digits + 4 digits. Data is stored sequentially from previously transmitted data in the pattern memory from the first one. In addition, data of hexadecimals of 4 digits + 4 digits is stored in a pattern memory with MSB first.

After completing transmission of the pattern, transmit “CSD”CR LF. Data transmission to the pattern memory is completed with “CSD”CR LF.

Even if the data has not reached 256kbit at the time transmission of data for a pattern memory is completed, transmission of the pattern can be interrupted by transmitting “CSD”CR LF. When no pattern data is stored in the Flash memory, the pattern memory is initialized to “0” when the power is turned on. When intentionally using “0” data, it is unnecessary to transmit data to the pattern memory.

For example, when setting a bit pattern as shown in the figure, enter as follows.

“PS0”CR LF

“BRAM_3EAA_AC15”CR LF

“BRAM_5500_0000”CR LF

“CSD”CR LF

(2) PS1 BRAM CSD command

This is a data transmission command set to the CH1 pattern memory. Similar to CH0, transmit

“PS1”CR LF

“BRAM_xxxx_xxxx”CR LF

“BRAM_xxxx_xxxx”CR LF

“BRAM_xxxx_xxxx”CR LF

“BRAM_xxxx_xxxx”CR LF

“CSD”CR LF

sequentially to set a command to CH1.

(3) CLEAR command

When “CLEAR”CR LF is entered, pattern memories of both of CH0 and CH1 are cleared to “0”.

(4) LENGTH command

When “LENGTH_xxxx_xxxx” CR LF is entered, a pattern length is set. For xxxx xxxx, specify a pattern length in 8 digit-hexadecimal. APG-3G has a memory of 256kbit, however, outputs patterns by bit number of head set in LENGTH. CH0 and CH1 cannot be individually set for the LENGTH command.

For example, when setting 40 bits, enter the following data.

“LENGTH_0000_0028” CR LF

(5) RD-P command

When “RD-P”CR LF is entered, data of a pattern memory is dumped. When interrupting dumping, enter “S”. As shown below, dumping is done from the first address of CH0 sequentially, and after ending dumping of CH0, subsequently dumping is done sequentially from the first address of CH1. Every 32 bits are dumped on one line.

“CH0 PATTERN MEMORY”CR LF

“xxxx_xxxx”CR LF

“xxxx_xxxx”CR LF

:

:

“CH1 PATTERN MEMORY”CR LF

“xxxx_xxxx”CR LF

“xxxx_xxxx”CR LF

:

:

8-3-3. Command related to the start and stop of pattern output

(1) CNT command

When “CNT”CR LF is entered, pattern output is started in the continuous repetition mode.

When pattern output is started in the continuous repetition mode, the LED2 lights. Bit synchronization between 2 channels may be lost due to exogenous noise or the like. When bit synchronization is lost, the LED2 flashes. In addition, whether synchronization between bits is lost or not can be confirmed with the START command. When synchronization between bits is lost, enter “CNT”CR LF again to eliminate bit synchronization loss.

(2) TRG command

When “TRG”CR LF is entered, pattern output is started in the external trigger mode. When an external trigger is set, the set pattern is output once.

When pattern output is started in the external trigger mode, the LED2 flashes. Bit synchronization between 2 channels may be lost due to exogenous noise or the like. When bit synchronization is lost, the LED2 flashes. In addition, whether synchronization between bits is lost or cannot be confirmed with the START command. When synchronization between bits is lost, enter “CNT”CR LF again to eliminate bit synchronization loss.

(3) STOP command

When “STOP”CR LF is entered, pattern output is stopped and the LED2 lights off.

8-3-4. Command related to the flash memory

(1) SAVE command

When “SAVE”CR is entered, information of the currently set pattern memory content, pattern length, HIGH/LOW limit of an input frequency, pattern burst stopping/repetition mode/external trigger mode is written in a flash memory.

When the power is turned on, these pieces of information are read out and set. When the SAVE command is executed in the repetition mode or the external trigger mode, the repetition mode/external trigger mode is set when the power is turned on next time. Unless correctly written, the following response returns.

“FLASH ERROR”CR LF

(2) ERASE command

When “ERASE”CR is entered, data stored in the flash memory is erased. Unless data in the flash memory is correctly erased, the following response returns.

“FLASH ERROR”CR LF

(3) RD-F command

When “RD-F”CR LF is entered, data in the FLASH memory is dumped. When interrupting dumping, enter “S”. As shown below, dumping is done from the first address of CH0 sequentially, and after ending dumping of CH0, subsequent dumping is done sequentially from the first address of CH1. Every 32 bits are dumped on one line.

“CH0 FLASH MEMORY”CR LF
“xxxx_xxxx”CR LF
“xxxx_xxxx”CR LF
:
:
“CH1 FLASH MEMORY”CR LF
“xxxx_xxxx”CR LF
“xxxx_xxxx”CR LF
:
:

8-3-5. Command related to setting parameters readout

(1) STAT command

When “STAT” CR LF is entered, a frequency of an input clock, frequency limit, set bit length, continuous repetition/external trigger/stopping, status of synchronization between channels are output sequentially.

The response is as follows.

“RF_IN=dddd.dMHz”CR LF
“FRQ_LO=dddd.dMHz”CR LF
“FRQ_HI=dddd.dMHz”CR LF
“LENGTH=0xXXXXXXXX”CR LF
“CNT”CR LF or “TRG”CR LF, or “STOP”CR LF
“Clock-Error”CR LF or no message

When “Clock-Error” is returned, there occurs a bit synchronization error between channels, therefore, send the CNT command and the TRG command again to eliminate synchronization loss between 2 channels.

8-3-6. Other command

(1)HELP command

When “HELP” CR LF is entered, a list and description of each command are output.

8-3-7. Precautions for input clock

APG-3G measures a frequency of the input clock at the time when the CNT command or the TRG command is entered, and adjusts hardware for data based on the measured frequency. When changing the frequency of the input clock in the process of the continuous repetition mode and the external trigger mode, send the CNT command and the TRG command again. In addition, when saving data in the CNT mode or TRG mode, connect the input clock before turning on the power because the TRG mode or CNT mode is set when turning on the power next time.

When a clock is entered from SG, bit synchronization between 2 channels may be lost due to transient phenomenon of SG when parameters (such as frequency, output level, output ON/OFF) of SG are changed. When there occurs any bit synchronization loss, the LED2 flashes, then send the CNT command and the TRG command to eliminate synchronization loss between 2 channels. Loss of bit synchronization can be confirmed even with the STAT command.

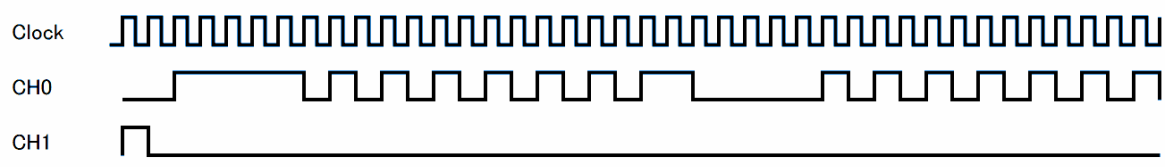
Bit synchronization between 2 channels may be also lost due to exogenous noise or the like. It is recommended to periodically monitor bit synchronization loss with the STAT command or by visual check of LED2.

8-3-8. Precautions when continuously setting data

When sending commands at high speeds, APG-3G may omit any data because it does not perform flow control. When processing of each command is completed, a prompt of “*” is returned, then send the next command after confirming reception of this prompt.

9. Command setting example

A command setting example is described as an example of a pattern to output a compliance pattern of PCIExpress in the continuous pattern output mode. As shown in the figure, a compliance pattern of 40 bits is output from CH0, and a pattern for trigger is output from CH1.



(1) Turn on the power and return the following message when initialization is normally completed.
“DST APG-3G Ver1.0A”CR LF

(2) Connect the input clock and confirm that the desired frequency is obtained with the STAT command.

“STAT”CR LF

(3) Set a frequency limit so that the frequency judgment function of the LED3 can be used. It is recommended to set a frequency limit with some allowance in consideration of variation in frequency of clock source used and measurement accuracy of frequency counter in this equipment, In addition, even if the frequency judgment function is not set, it does not relate to pattern output operation.

“FRQ-LO_dddd.d”CR LF
“FRQ- HI_dddd.d”CR LF

(3) Send data of 40 bits to a pattern memory of CH0.

“PS0”CR LF
“BRAM_3EAA_AC15”CR LF
“BRAM_5500_0000”CR LF
“CSD”CR LF

(4) Send data to a pattern memory of CH1. In CH1, only the first one bit is “1”, therefore, the BRAM command is used only once.

“PS1”CR LF
“BRAM_8000_0000”CR LF
“CSD”CR LF

(5) Set a pattern length.

“LENGTH_0000_0028”CR LF

(6) Start pattern output in the continuous repetition mode.

“CNT”CR LF

(7) Save in the flash memory.

“SAVE”CR LF

In the flash memory, information of pattern memory content, pattern length, continuous repetition/external trigger/stopping, and frequency limit are stored. Output of a compliance pattern of PCIExpress is started immediately when the power is turned on next time.

10. Factory default settings

Data is written in the Flash memory at the time of factory shipment so as to output the compliance pattern of PCIExpress described in 8. Command setting example. Data other than pattern data is written as follows.

FRQ_LO=0000.0MHz
FRQ_LHI=3000.0MHz
LENGTH=0x00000028
CNT mode

11. Shipping inspection

100% inspection shall be performed for the electrical specification in 2-1.

12. Warranty

If any defect is found due to the manufacturer's improper production or design within one year after delivery, repair or replacement shall be performed at the manufacturer's responsibility. Digital Signal Technology, Inc assumes no liability for damages that may occur as a result of handling by users even though the warranty period.

13. Accessories

For power supply	(J7 on PCB)2P connector cable	1 piece
For asynchronous serial communication	(J10 on PCB)3Pconnector cable	1 piece
Spacer/screw		4 sets

14. Others

14-1. This product, which employs a CMOS device, may be easily damaged by static electricity. DS Technology, Inc. assumed no liability for damages that may occur as the result of handling by users even through the above warranty period.

14-2. Do not supply over voltage power supply, or module may be damaged. DS Technology, Inc. assumes no liability for damages that may occur as the result of handling by users even though the above warranty period.