NEC

Application Note

78K0

8-Bit Single-Chip Microcontrollers

The Usage of POC and LVI

78K0/Kx2 Series

78K0/Fx2 Series

78K0/Lx2 Series

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NOTES FOR CMOS DEVICES

1. VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

2. HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

3. PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

4. STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

5. INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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Introduction

Target Readers

This application note is intended for users who understand the basic functions the 78K0/Fx2/Kx2/Lx2 family products and who will use those products to design application systems.

Purpose

The purpose of this application note is to help the user to understand the functionality and the benefit of the Power On Clear (POC) and the Low Voltage Detector (LVI). These features are implemented in all microcontrollers of the 78K0/Fx2/Kx2 and Lx2 – Subseries. The handling and usage shown in this document are for reference, only. The correct operation is not guaranteed if these samples are implemented as they are described here. The user has to adapt the usage and handling of both functions to the application specific needs.

Organization

This application note consists of the following main sections:

- Functionality of the POC
- Functionality of the LVI
- Software example how to use the LVI

How to Read this Application Note

It is assumed that the reader of this application note has a general knowledge in the fields of electrical engineering, logic circuits and microcontrollers.

- To gain a general understanding of functions:
→ Read this application note in the order of the **CONTENTS**. The mark “<R>” shows major revised points. The revised points can be easily searched by copying an “<R>” in the PDF file and specifying it in the “Find what:” field.

- To learn more about the 78K0/Fx2/Kx2/Lx2’s hardware functions:
→ See the user’s manual for each 78K0 product series .

Conventions

Data significance: Higher digits on the left and lower digits on the right
Active low representation: xxx (overscore over pin or signal name)
Note: Footnote for item marked with **Note** in the text
Caution: Information requiring particular attention
Remark: Supplementary information
Numeral representation: Binary.....xxxx or xxxxB
Decimal xxxx
Hexadecimal .....xxxxH

Table of Contents

List of Figures

CHAPTER 1 RELATED DEVICES

All devices listed below are incorporating the same Power On Clear (POC) and the same Low Voltage Detector (LVI) function.
Consequently, this application note can be used as a reference example for all devices from this list:

Device List::

78K0/KB2: μPD78F050x, μPD78F0503D
78K0/KC2: μPD78F051x, μPD78F0513D, μPD78F0515D
78K0/KD2: μPD78F052x, μPD78F0527D
78K0/KE2: μPD78F053x, μPD78F0537D
78K0/KF2: μPD78F054x, μPD78F0547D

78K0/FC2: μPD78F0881, μPD78F0882, μPD78F0883
78K0/FC2: μPD78F0884, μPD78F0885, μPD78F0886
78K0/FE2: μPD78F0887, μPD78F0888, μPD78F0889, μPD78F0890
78K0/FF2: μPD78F0891x, μPD78F08892, μPD78F0893

78K0/LE2: μPD78F036x, μPD78F0363D
78K0/LF2: μPD78F037x, μPD78F0376D
78K0/LF2: μPD78F038x, μPD78F0386D
78K0/LG2: μPD78F039x, μPD78F0397D

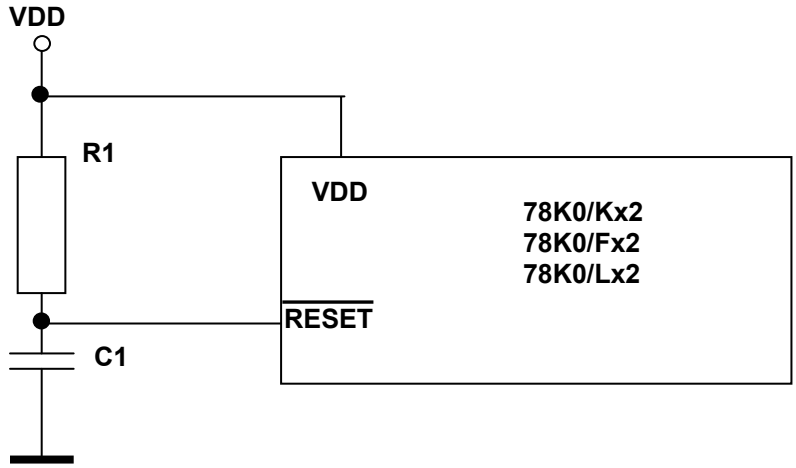
CHAPTER 2 OVERVIEW

2.1 Power On Clear (POC) – Functional Descripton

All devices in the products families listed before incorporate a Power On Clear (POC) function. This function generates a proper internal RESET signal while the supply voltage (VDD) for the microcontroller is switched on. This internal RESET signal generation will eliminate the need for a complex external RESET circuitry.
Although, a proper internal RESET signal will be generated by the POC function, an external pull-up resistor must be always connected to the RESET input pin of a microcontroller. Otherwise the microcontroller will not operate in the specified condition. The external RESET input has still the priority to generate an internal RESET signal if a low level is applied to the RESET input pin. Needless to say, the external RESET input has Schmitt-Trigger behaviour.

A typical example for an external pull-up resistor is given here:

Figure 2-1. Exmple for an external RESET circuit



Recommended values for R1 and C1:
R1 = 100K ... 10K, C1 = 1nF ... 10nF

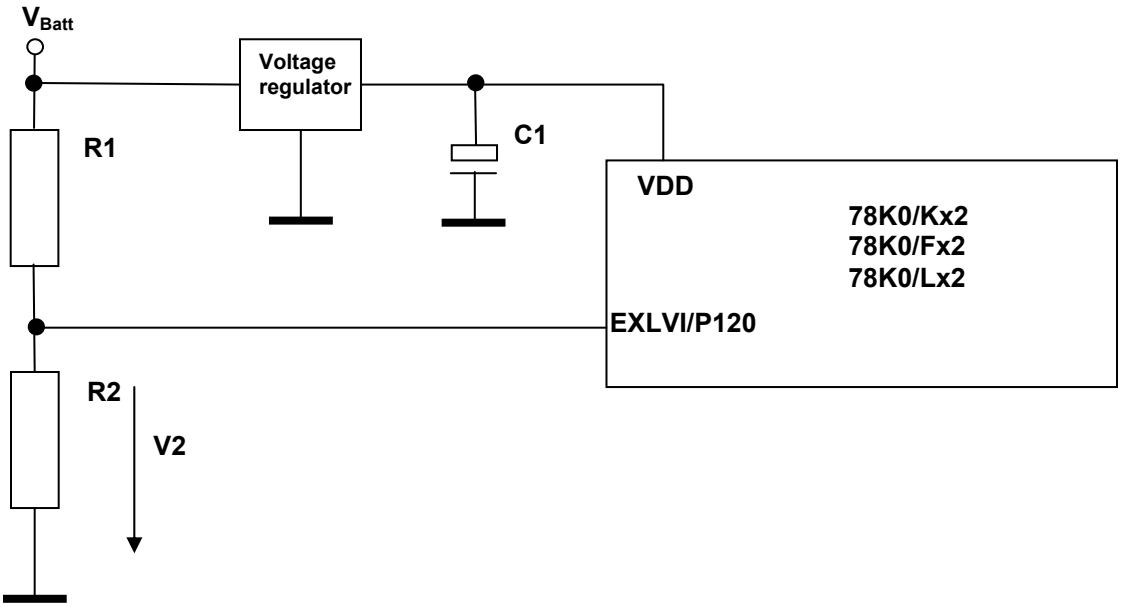
The purpose of capacitor C1 is to eliminate some spikes (maybe generated by EMI), which could cause some unexpected internal RESET's.

Depending on the supply voltage rise time (if the rise time is slow or fast), there are two configurations possible for the POC function. In order to adapt the correct Power On Reset function to each and every rise time of the VDD, an Option Byte must be set during the virgin flash programming. There are two possible examples given in Chapter 3.1

2.2 Low Voltage Detector (LVI) – Functional Descripton

All devices in the products families listed before incorporate a Low Voltage Detector (LVI), which allows the device to detect if the supply voltage falls below a certain threshold. When the supply voltage is crossing the dedicated (in advanced programmed) threshold voltage in falling direction either an internal interrupt (LVI Interrupt) or an internal RESET signal can be generated, automatically. Up to 16 different threshold voltage levels are possible to select (i.e. 4.24V down to 1.93V). For details, please refer to the corresponding device User's Manual.
Beside the programmable internal threshold voltages the devices also support an external input with a fixed threshold voltage [1.21V (typ)] The external LVI input (EXLVI/P120) can be used to detect a voltage fail prior to the power supply of the microcontroller (VDD) will disappear. Due to the fact, the power supply for the microcontroller (VDD) is usually buffered by an external capacitor (C1 > 10uF), the voltage will decrease more slow then V_{Batt}. The LVI interrupt will be generated when the input voltage (V2) to EXLVI is below 1.21V (i.e. V_{Batt} will fail). In this case, the microcontroller can still operate, because the microcontroller is buffered by the voltage supplied by the capacitor C1.
An example for possible application circuit is given here:

Figure 2-2. Example for an external LVI input circuit



Normal operation: $V2 = V_{Batt} \times R2 / (R1 + R2) > 1.31V$
LVI execution: $V2 = V_{Batt} \times R2 / (R1 + R2) < 1.11V$

The main intention of this application note is to give the user some basic ideas for the operation of the Low Voltage Detector (LVI).

The Low Voltage Detector (LVI) can also be used to confirm if the supply voltage for the microcontroller has reached a certain level. The confirmation for the correct voltage might be necessary to be executed before an external oscillator is switched on or before an A/D conversion is started or before an EEPROM emulation can be executed? A software example to confirm if the supply voltage has reached the specified level is given in the Chapter 3.2.

CHAPTER 3 OPERATION

3.1 Function of Power On Clear (POC)

The Power On Clear (POC) release voltage is fixed for all products to 1.59V (+/- 150mV). On the other hand, the real supply voltage range for a correct CPU operation is starting at 1.8V (VDD = 1.8V to 5.5V). Therefore, to make sure that the supply voltage will reach at least 1.8V or more, the rise time of the supply voltage must fulfil a certain requirement. In other words, the rise time of the supply voltage (VDD) must be at least 0.5V/ms or faster. In case, the supply voltage will rise up slower then 0.5V/ms, there is a possibility to keep the CPU in a kind of a wait mode until the supply voltage reaches a level of 2.7V.

The user can select by a corresponding setting of a flash Option Byte on which voltage level the CPU should start operation. In any case, the CPU will start operation using the internal 8MHz oscillator. The relevant option byte is located on a fixed ROM address at 0x0081. Please refer to the corresponding device User's Manual, Chapter "Option Byte"

Condition 1:
The supply voltage in the user application will rise up with 0.5V/ms or faster (i.e. 1V/ms, 2V/ms, …)
In this case, the option byte (called "POCMODE") can be set to → 00h
Address: 0x0081 = 0x00;
In this case, the CPU will start operation at > 1.8V, because there is in any case an internal wait time [approx. 3.2ms (typ)] where the internal voltage regulator (REGC) becomes stable after the RESET was released by the POC.

Condition 2:
The supply voltage in the user application will rise up with less then 0.5V/ms or slower (i.e. 0.4V/ms, 0.3V/ms, 0.2V/ms, …)
In this case, the option byte (called "POCMODE") must be set to → 01h
Address: 0x0081 = 0x01;
In this case, the CPU will not start operation before the supply voltage reaches 2.7V or more.
Remark:
After the CPU has started operation at 2.7V or more, the LVI can be used to program a threshold voltage even less then 2.7V (down to 1.93V) to enter a defined state (i.e LVI Interrupt generation or LVI RESET generation) in case the supply voltage false down.

3.1.1 Short Software Example to Setup the Option Byte.

Here is a software example how to define the Option Bytes for the Watchdog Timer and the POCMODE using the IAR Workbench:

```
/* ============================================================
** option byte definitions
** ============================================================
*/
#pragma constseg =OPTBYTE

__root const unsigned char optbyte [2] = {0x6E, 0x01};
//
//        WDT Window size = 100%
//        WDT State = Stopped
//        WDT Interval time = fosc/2**17
//        Internal low speed oscillator (240kHz) can be stopped by software
//
//        POCMODE = 0x01;   The CPU will be released at 2.7V
//        POCMODE = 0x00;   The POC will release the CPU at > 1.8V
//

#pragma constseg = default
```

3.2 Function of Low Voltage Detector (LVI)

The Low Voltage Detector (LVI) can either generate an internal interrupt or it can alternatively generate an internal RESET signal. The user can select between two sources which one should trigger the LVI function:

- An internal programmable threshold voltage selected by the LVIS – Register
- An external threshold voltage selected by the EXLVI/P120 input. In this case, the threshold voltage is fixed to 1.21V (+/- 100mV)

3.2.1 LVIM register

The selection between interrupt or internal RESET generation is performed by the LVIMD flag of the LVIM register. If LVIMD=0 the interrupt generation is selected, if LVIMD=1 internal RESET generation is selected.

Further flags of the LVIM register are:
LVION = 0 → disable LVI operation
LVION = 1 → enable LVI operation
LVISEL = 0 → detects level of VDD
LVISEL = 1 → detects level of EXLVI input [1.21V (typ)]
LVIF = 0 → Will indicate the supply voltage VDD (or the input voltage to EXLVI) > detection voltage
LVIF = 1 → Will indicate the supply voltage VDD (or the input voltage to EXLVI) < detection voltage

3.2.2 LVIS register

The specific threshold voltage can be selected by the LVI - Register. The minimum threshold voltage is 1.93V and the maximum threshold voltage is 4.24V. In between these levels there are 14 other threshold voltage levels selectable. For more details please refer to the corresponding User's Manual.

Caution:
Any write access to the LVIS - or LVIM - Register must be done when the Low Voltage Detection function is disabled by **(LVION = 0)**

CHAPTER 4 SOFTWARE FUNCTIONS

4.1 Software Example for the Low Voltage Detector (LVI)

The enclosed software example shows a possible solution to confirm by the LVI function that the power supply of the microcontroller has reached its specified voltage range before the external oscillator (i.e. 20MHz) is switched on by the user.

4.2 Description – Software Example

The below given software example will execute the following steps:

- Check for the RESET source, was it a RESET by the LVI or was it any other RESET source?
- Initialize the LVIS and the LVIM register in case of any other RESET
- Start up the external oscillator (i.e. 20MHz) when VDD > 4.0V
- Wait for the external oscillator to become stable
- Switch peripheral and CPU clock to the external oscillator clock
- Switch of the internal high-speed oscillator (8MHz) to save some current

4.3 LVI Software Example – Source Code

General Conditions:

1. After any kind of RESET release
2. The Option Byte for the POC mode selection (0x0081) is 0x00 or 0x01
   (POCMODE = 0 // After Power On Reset, the CPU operation will be released when VDD > 1.8V)
   (POCMODE = 1 // After Power On Reset, the CPU operation will be released when VDD > 2.7V)

```
void LVI_ExtClock_Init (void)
            // Here the CPU will operate with the internal High Speed oscillator (8MHz)

{
   LVIMK  = 1;              // Disable the LVI Interrupt
   if(LVION == 0)           // Check if LVION = 1? If yes, it was a RESET caused by the LVI.
                            // In this case, the LVIM and LVIS register initialization must be skipped!!
   {
        LVISEL = 0;         // Detect the level of the supply voltage (VDD)
        LVIS   = 0x00;      // Select a detection voltage of VDD > 4.24V
        LVION  = 1;         // Enable the voltage detection function
   }

  TMHMD1 = 0x70;            // f_RL --> 240kHz internal Low-speed oscillator
  CMP01  = 0x05;            // set period for > 10us to wait for LVI operation stabilization (refer to UM)

  TMIFH1 = 0;               // Clear TMIFH1 request flag
  TMHE1  = 1;               // Enable Timer operation


  While (TMIFH1 !=1 );      // Wait for > 10us to secure that the LVI is working correct
  {
        __no_operation();
  }



  TMHE1  = 0;               // Stop Timer
  TMIFH1 = 0;               // Clear the Timer Request flag
```

```
  while (LVIF == 1);        // Wait for VDD to become 4.24V, or more
  {                         // For VDD < 4.24V the Low-voltage detection flag (LVIF) is “1”
       __no_operation();
  }

  LVIIF  = 0;               // Clear the LVI Interrupt request flag


// Now, we will start the external 20MHz resonator


  AMPH   = 1;               // For fx >  10MHz ---> AMPH = 1
                            // For fx <= 10MHz ---> AMPH = 0
  EXCLK  = 0;               // Don't use external active clock
  OSCSEL = 1;               // Enable external Resonator (crystal or ceramic) at X1, X2
  MOC = 0x00;               // Allow external clock to operate

  while (OSTC < 0x1F)       // Wait for main clock to become stable (3.27ms @ 20MHz)
  {
  __no_operation();
  }

  OSTS = 0x05;              // Select an oscillator stabilization
                            // time after a STOP mode release



  XSEL = 1;                 // Switch the peripheral clock to external clock
  MCM0 = 1;                 // Switch CPU clock to external clock



  while (MCS != 1)
  {
  __no_operation();         // Wait for the real switch from internal
                           // clock (8MHz) to the external system clock
  }
```

```
  PCC   = 0x00;            // Use high speed clock (direct clock) for the CPU clock
                           // For VDD > 4V the CPU can use fXH as CPU clock (here 20MHz)


  RCM = 0x01;              // Now, the internal high-speed Osc. (8MHz) could be
                           // stopped to reduce the total current consumption

     //  End of  “LVI_ExtClock_Init”
}
```

CHAPTER 5 VALID SPECIFICATION

Item	Date published	Document No.	Document Title
1	Jul 2007 or later	U17328E	78K0/KB2 User's Manual
2	Feb 2007 or later	U17336E	78K0/KC2 User's Manual
3	May 2006 or later	U17312E	78K0/KD2 User's Manual
4	May 2006 or later	U17260E	78K0/KE2 User's Manual
5	May 2006 or later	U17397E	78K0/KF2 User's Manual
6	Mar 2007 or later	U17555E	78K0/FC2 User's Manual
7	Mar 2007 or later	U17554E	78K0/FE2 User's Manual
8	Mar 2007 or later	U17553E	78K0/FF2 User's Manual
9	Jul 2006 or later	U17734E	78K0/LE2 User's Manual
10	Aug 2006 or later	U17504E	78K0/LF2 User's Manual
11	Sep 2006 or later	U17473E	78K0/LG2 User's Manual

CHAPTER 6 REVISON HISTORY

Item	Date published	Document No.	Comment
1	Jul 2007	U18876EE1V0AN00	1st Release