NEX-ISA
ISA Bus Support Users Manual

Including these Software Support packages:
ISA

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1.0 OVERVIEW

1.1 General Information

The NEX-ISA adapter has been designed to provide quick and easy connections to interface a 102- or 136-channel TLA600/700, a 92A96, or a 92C96 acquisition module to an ISA backplane. (The ISA designation refers to the Industry Standard Architecture specification, which is the equivalent of the IBM PC XT/AT bus.) In addition, the method of connection permits the use of other acquisition cards, pattern generation cards or other measurement devices such as oscilloscopes.

The included software will permit the acquisition of ISA bus cycles, and will display the data in easy-to-read symbolic form rather than raw hexadecimal or binary data.

Please note that this manual uses some terms generically. For instance, references to a 92A96 acquisition card apply to a 92C96 acquisition card; references to the DAS9200 apply equally to the TLA500; and references to the TLA600/700 apply to a TLA704, 711, 714, 715, 720 or 721 chassis with one or more 7*3/4 acquisition cards.

Appendix D is a silk-screen print of the NEX-ISA Adapter board. Referring to this drawing while reading the manual is suggested.

This manual assumes that the user is familiar with the ISA Bus specification and the Tektronix TLA600/700, DAS9200, or TLA500 Logic Analyzer. Also, in the case of the TLA600/700, it is expected that the user is familiar with Windows O.S.

For information on using a Prism 32GPX/GPD module with this support, or if 5¼" DAS floppies are needed, please contact Nexus Technology. See Appendix F for contact information.

2.0 SOFTWARE INSTALLATION

One 3½" diskette has been included with the NEX-ISA Bus Adapter. It is for use with the TLA600/700 series. Diskettes for the DAS9200 or TLA500 are available upon request. Please see Appendix E for contact information.

2.1 TLA600/700

The ISA support software is loaded in the same method as other Win95 programs. Place the NEX-ISA Install disk in the floppy drive of the TLA600/700. Select **Control Panel** and run **Add/Remove Programs**, choose **Install**, **Next**, then **Finish**. Add/Remove will then run SETUP.EXE on the floppy and install the support in its proper place on the hard disk.

To load a support into the TLA600/700, first select the desired Logic Analyzer card in the Setup screen, select Load Support Package from the File pull-down, then choose ISA and click on **Okay**. Note that for either support the Logic Analyzer card must be at least 102-channels in width.

2.2 DAS9200

The included diskette should be loaded onto the DAS9200 using the Install Application function. This function is available from the Disk Services menu of the DAS. For more information, refer to the Tektronix DAS9200 or TLA500 System User's Manual.

Load the desired support from within the 92A96 Config menu by choosing "ISA Support" and pressing <RETURN>. The channel grouping, clocking and symbols will then be loaded.

3.0 CONFIGURING the NEX-ISA BUS ADAPTER

3.1 General Information

There are two jumper areas on the NEX-ISA adapter board - JP1 and JP2. When using the NEX-ISA adapter in an 8-bit (XT) slot, shorting blocks must be placed across these two jumpers for proper data acquisition by the logic analyzer. When using the adapter in a 16-bit (AT) slot, the shorting blocks must be removed. If they are left on when using the NEX-ISA board in an AT slot, improper operation of the target system may result.

4.0 CONNECTING to the NEX-ISA ADAPTER

4.1 General

Although taller than a standard XT or AT module, the NEX-ISA adapter is designed to plug directly into any full-size ISA backplane slot. The board length and connector spacing conforms to ISA specifications.

4.2 TLA600/700

When using NEX-ISA support with a TLA600/700 containing a 7*3/4 acquisition module, the necessary acquisition data sections are A0-A3, D0-D3, and C0-C3. These grouped channels (8 podlets to a group) should be connected to the locations denoted for the A96. Follow the silk-screened information on the board that shows the proper relationship between the signal and

reference inputs. When properly connected, the sides of the podlets that have writing on them should be visible.

Connect the four clock leads to their specified locations at J12 (the only connector with 4 locations). Again, follow the silk-screened information to properly connect the clock input and its ground. Table 1 shows the wiring and Channel Grouping for the TLA600/700 when used with the NEX-ISA adapter.

4.3 92A96

When using a 92A96 or 92C96, connect the grouped pods to their appropriate locations by following the silk-screen information printed on the adapter board. The 92A/C96 pods are labeled A0-A3, D0-D3, and C0-C3. Each pod has its proper location denoted on the silk-screen of the adapter board. When attaching the pods, follow the silk-screen information on the board showing the ground and signal pin locations. When properly connected, the colored sides of the podlets should be visible.

Connect the four clock leads (one per A96 cable) to their specified locations at J12 (the only connector with 4 locations). Again, follow the silk-screened information to properly connect the clock input and its ground. Table 1 shows the wiring and Channel Grouping for the 92A96 when used with the NEX-ISA adapter.

Group Name	Signal Name	ISA Pin #	TLA700 / 92A96 input
Address (Hex)	LA23	C2	A3:7
	LA22	C3	A3:6
	LA21	C4	A3:5
	LA20	C5	A3:4
	SA19	A12	A3:3
	SA18	A13	A3:2
	SA17	A14	A3:1
	SA16	A15	A3:0
	SA15	A16	A2:7
	SA14	A17	A2:6
	SA13	A18	A2:5
	SA12	A19	A2:4
	SA11	A20	A2:3
	SA10	A21	A2:2
	SA9	A22	A2:1
	SA8	A23	A2:0
	SA7	A24	A1:7
	SA6	A25	A1:6
	SA5	A26	A1:5
	SA4	A27	A1:4
	SA3	A28	A1:3
	SA2	A29	A1:2
	SA1	A30	A1:1
	SA0	A31	A1:0
Misc (Off)	RESET	B2	C3:0
	AEN	A11	C1:5
	BALE	B28	C1:2
	SBHE	C1	C1:1
	CLK	B20	C3:3
DMA_Req (Off)	DRQ7	D15	D0:6
	DRQ6	D13	D0:5
	DRQ5	D11	D0:4
	DRQ3	B16	D0:3
	DRQ2	B6	D0:2
	DRQ1	B18	D0:1
	DRQ0	D09	D0:0
DMA_Ack (Off)	-DAK7	D14	D1:6
	-DAK6	D12	D1:5
	-DAK5	D10	D1:4
	-DAK3	B15	D1:3
	-DAK2	B26	D1:2
	-DAK1	B17	D1:1
	-DAK0	D8	D1:0
MiscAddr	LA19	C6	C2:7
	LA18	C7	C2:6
	LA17	C8	C2:5
Clock:0	ISAWR	*	- - - - -
Clock:1	CLK=	B20	- - - - -
Clock:2	ISAWR=	*	- - - - -
Clock:3	CLK==	B20	- - - - -

Group Name	Signal Name	ISA Pin #	TLA700 / 92A96 input
Data (Hex)	SD15	C18	D3:7
	SD14	C17	D3:6
	SD13	C16	D3:5
	SD12	C15	D3:4
	SD11	C14	D3:3
	SD10	C13	D3:2
	SD9	C12	D3:1
	SD8	C11	D3:0
	SD7	A2	D2:7
	SD6	A3	D2:6
	SD5	A4	D2:5
	SD4	A5	D2:4
	SD3	A6	D2:3
	SD2	A7	D2:2
	SD1	A8	D2:1
	SD0	A9	D2:0
CycType (Sym)	-IOW	B13	C0:3
	-IOR	B14	C0:2
	-SMEMW	B11	C0:5
	-SMEMR	B12	C0:4
	-MEMW	C10	C0:1
	-MEMR	C9	C0:0
BusCtrl (Sym)	T/C	B27	C1:0
	-IOCHK	A1	C1:6
	-REFRSH	B19	C3:1
	-MASTER	D17	C1:7
	-0WS	B8	C1:4
	IORDY	A10	C1:3
	-MEM16	D1	C0:7
	-IO16	D2	C0:6
Intrpts (Off)	IRQ15	D6	C2:2
	IRQ14	D7	C2:1
	IRQ12	D5	C2:0
	IRQ11	D4	A0:7
	IRQ10	D3	A0:6
	IRQ9	B4	A0:5
	IRQ7	B21	A0:4
	IRQ6	B22	A0:3
	IRQ5	B23	A0:2
	IRQ4	B24	A0:1
	IRQ3	B25	A0:0
Unused (Off)	- - - - -	- - -	C3:7
	- - - - -	- - -	C3:6
	- - - - -	- - -	C3:5
	- - - - -	- - -	C3:4
	- - - - -	- - -	C2:4
	- - - - -	- - -	C2:3
	- - - - -	- - -	D1:7
	- - - - -	- - -	D0:7

Table 1- ISA TLA600/700/92A96 Wiring

* Derived signal

5.0 CLOCK SELECTION

5.1 General Information

There are two clocking options available when using the NEX-ISA support package. Each is explained in detail below.

When using a TLA600/700, the clocking mode is selected by moving to the System window, clicking on Setup for the appropriate LA card, then clicking on **More** (a button to the right of the Clocking field). Choose the desired mode in the Clocking Select field.

When using a DAS9200 or TLA500, the clocking selection is made in the Clock menu.

5.2 Clocking Options - Explanation

Cycle Acquisition Only - This is the default clocking selection. In this mode every bus transaction is acquired. All Wait states are ignored. This clocking selection offers the best use of your acquisition memory by ignoring all Wait states, and also provides more easily understood data. For this acquisition mode to work properly, the ISA signals -MEMR, -MEMW, -IOR, -IOW, -SMEMR, -SMEMW, and CLK must be present.

Every CLK Edge - In this mode, data will be acquired on every edge of the ISA CLK signal. This clocking mode shows *all* bus cycles, including Wait states. Since no clocking qualification is done only the CLK signal is required.

6.0 VIEWING DATA

6.1 Viewing State Data on the TLA600/700

After making an initial acquisition, the TLA600/700 will display the data in the Listing (State) format. Address and Data information is displayed in hexadecimal format; Cycle Type (CycType) and Bus Control (BusCtrl) data is displayed using symbols; Miscellaneous, DMA Request and Acknowledge, Interrupts, and MiscAddr data groups default to OFF.

The use of Symbol Tables when displaying state data enables the user to quickly determine what type of bus cycle was acquired. When using NEX-ISA, a symbol table (ISA_Cyc, Table 2) has been provided to show the type of bus cycle that occurred on the ISA bus. This symbol table quickly shows whether the acquisition was a memory or I/O operation, a read or a write, etc.

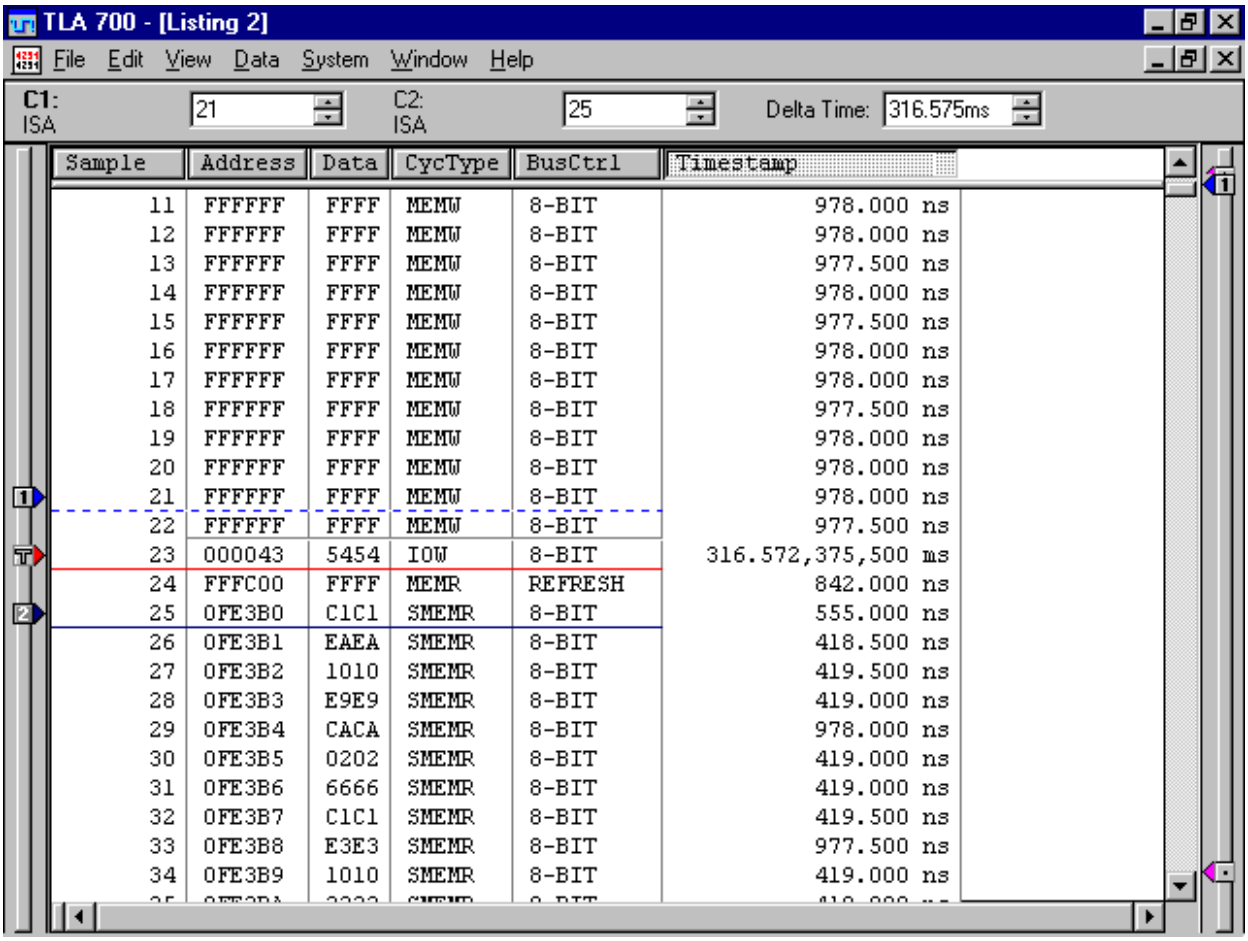
A second symbol table (ISA_BusCtrl, Table 3) shows whether the bus transaction was a Refresh cycle, or an 8- or 16-bit operation.

It is important to note that changing the group, channel, or wiring of the CycType or BusCtrl groups can result in incorrect symbol information being displayed.

Pattern	TLA700 / 92A96 Symbol
0xxxxx	IOW
x0xxxx	IOR
xx0xxx	SMEMW
xxx0xx	SMEMR
xxxx0x	MEMW
xxxxx0	MEMR

Table 2- ISA_Cyc Cycle Type Symbol Table

Signals, from left to right: -IOW, -IOR, -SMEMW, -SMEMR, -MEMW, -MEMR



Sample	Address	Data	CycType	BusCtrl	Timestamp
11	FFFFFF	FFFF	MEMW	8-BIT	978.000 ns
12	FFFFFF	FFFF	MEMW	8-BIT	978.000 ns
13	FFFFFF	FFFF	MEMW	8-BIT	977.500 ns
14	FFFFFF	FFFF	MEMW	8-BIT	978.000 ns
15	FFFFFF	FFFF	MEMW	8-BIT	977.500 ns
16	FFFFFF	FFFF	MEMW	8-BIT	978.000 ns
17	FFFFFF	FFFF	MEMW	8-BIT	978.000 ns
18	FFFFFF	FFFF	MEMW	8-BIT	977.500 ns
19	FFFFFF	FFFF	MEMW	8-BIT	978.000 ns
20	FFFFFF	FFFF	MEMW	8-BIT	978.000 ns
21	FFFFFF	FFFF	MEMW	8-BIT	978.000 ns
22	FFFFFF	FFFF	MEMW	8-BIT	977.500 ns
23	000043	5454	IOW	8-BIT	316.572,375,500 ms
24	FFFC00	FFFF	MEMR	REFRESH	842.000 ns
25	0FE3B0	C1C1	SMEMR	8-BIT	555.000 ns
26	0FE3B1	EAEA	SMEMR	8-BIT	418.500 ns
27	0FE3B2	1010	SMEMR	8-BIT	419.500 ns
28	0FE3B3	E9E9	SMEMR	8-BIT	419.000 ns
29	0FE3B4	CACA	SMEMR	8-BIT	978.000 ns
30	0FE3B5	0202	SMEMR	8-BIT	419.000 ns
31	0FE3B6	6666	SMEMR	8-BIT	419.000 ns
32	0FE3B7	C1C1	SMEMR	8-BIT	419.500 ns
33	0FE3B8	E3E3	SMEMR	8-BIT	977.500 ns
34	0FE3B9	1010	SMEMR	8-BIT	419.000 ns

Figure 1- ISA State Display on TLA600/700

Pattern	TLA700 / 92A96 Symbol
xx0xxxx x	REFRESH
xx1xxx0 x	MEM16
xx1xxxx 0	IO16
xx1xxx1 1	8-BIT

Table 3- ISA_Bus Bus Control Symbol Table

Signals, from left to right: T/C, -IOCHK, -REFRSH, -MASTER, -0WS, IORDY, -MEM16, -IO16

6.2 Viewing Timing Data on the TLA600/700

By default, the TLA600/700 will display an acquisition in the Listing (State) mode. However, the same data can be displayed in Timing form by adding a Waveform Display window. This is done by clicking on the **Window** pull-down, selecting **New Data Window**, clicking on **Waveform Window Type**, then choosing the Data Source. Two choices are presented: ISA and ISA-MagniVu. The first (ISA) will show the exact same data (same acquisition mode) as that shown in the Listing window, except in Timing format. The second selection, ISA-MagniVu, will show all of the channels in 2GHz MagniVu mode, so that edge relationships can be examined at the module's trigger point. With either selection, all channels can be viewed by scrolling down the window. Refer to the TLA600/700 System User's Manual for additional information on formatting the Waveform display.

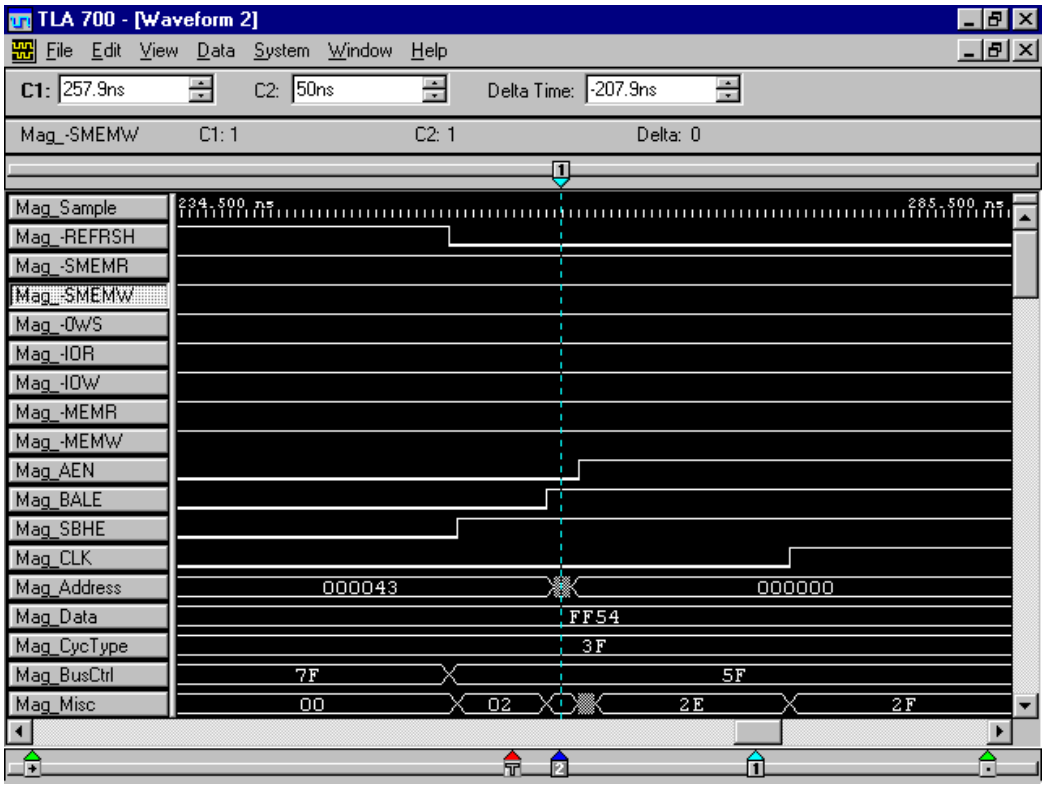


Figure 2- ISA MagniVu Display on TLA600/700

6.3 Viewing State Data on the DAS9200/TLA500

After an acquisition is made the DAS9200 Logic Analyzer will display the data in State Display mode (as a default only). Address and Data information is displayed in hexadecimal format; Cycle Type (CycType) and Bus Control (BusCtrl) data is displayed using symbols; Miscellaneous, DMA Request and Acknowledge, Interrupts, and MiscAddr data groups default to OFF.

The use of Symbol Tables when displaying state data enables the user to quickly determine what type of bus cycle was acquired. When using NEX-ISA, a symbol table (ISA_Cyc, Table 2) has been provided to show the type of bus cycle that occurred on the ISA bus. This symbol table quickly shows whether the acquisition was a memory or I/O operation, a read or a write, etc.

A second symbol table (ISA_BusCtrl, Table 3) shows whether the bus transaction was a Refresh cycle, or an 8- or 16-bit operation.

It is important to note that changing the group, channel, or wiring of the CycType or BusCtrl groups can result in incorrect symbol information being displayed.

6.4 Viewing Timing Data on the DAS9200/TLA500

It may be useful to display acquired information using the Timing Diagram display of the DAS9200. (Note that, unlike some other logic analyzers, with the DAS9200 there is no need to re-acquire ISA data when changing from one display mode to another. The same data can be viewed in either format.) This method of data display can be particularly useful when an asynchronous acquisition has been made (using the DAS9200 internal acquisition clock) to determine the relationships between signal edges.

Refer to the appropriate Tektronix DAS 92A96 Module User's Manual for more detailed information on formatting the display of the acquired data.

APPENDIX A - Necessary Signals for Clocking

Because of the number of control signals defines in the ISA specification, additional circuitry had to be provided to ensure proper clocking of data. A 74S30 8-input NAND gate is used to gate -IOW, -IOR, -SMEMW, -SMEMR, -MEMW, and -MEMR to provide a logic high output (ISAWR) whenever any one of these inputs goes low. This generated signal is what is used to acquire information when in the “Cycle Acquisition Only” mode.

When acquiring data in “Acquire Every CLK Edge” mode, the only signal necessary for clocking is CLK.

APPENDIX B - Considerations

B.1 ISA Loading

It must be noted that the NEX-ISA Bus Adapter does not provide any buffering of the ISA backplane signals. This was a conscious design decision that was made by balancing the tradeoffs of possible backplane loading versus signal acquisition accuracy. By not introducing signal buffers it is possible, using the NEX-SIA adapter, to see the exact timing relationships and signal waveforms from the backplane. It is also much easier to connect pattern generators to the backplane since buffer direction is not a concern. It is believed that the signal loading of the TLA600/700 or 92A96 acquisition cards is low enough so that ISA signal degradation will not occur.

The NEX-ISA Adapter Board was designed so that the run lengths for critical signals (and those with the highest activity levels, such as the address / data bus) are as short as possible. This should help greatly in retaining signal integrity.

B.2 "Patch" Areas

If signal loading or reflection does become a concern, the capability exists to add series resistors to any ISA signal. Patch areas have been provided next to each TLA600/700/A96 connector, consisting of two rows of plated through holes. These areas (outlined on the silk-screen and labeled as Nxx) are suitable for individual resistors or resistor networks. To add a series resistor, simply cut the trace of the desired signal on the component side of the board, and solder the resistor between the two feed-throughs.

B.3 Pattern Generation

Because there is no buffer circuitry on the NEX-ISA Adapter, it is well suited for use with the 92S16 and 92S32 Pattern Generator modules available for the DAS9200. By connecting pattern generator probes to the A96 signal connectors on the Adapter, desired bus activity can be simulated. This can be particularly effective when trying to debug interrupt or DMA conflicts.

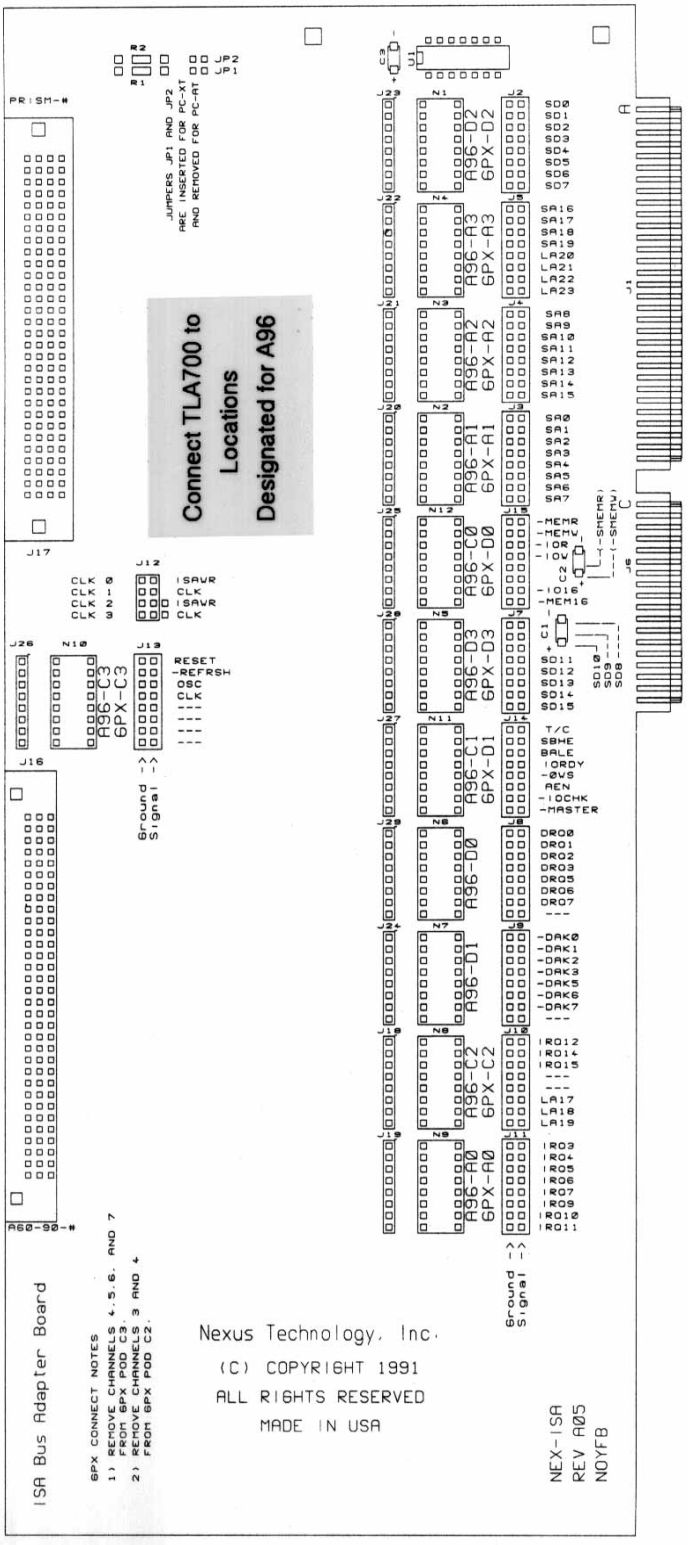
It should be noted that, because of the pin spacing of the A96 connectors, it is not recommended that the Tektronix P6464 or P6465 pattern generator probes be used without providing adequate cooling for their podlets. These probes use active podlets that can get very warm in use. A better choice would be the P6463 pods which are passive and do not have such cooling requirements.

APPENDIX C - ISA Bus Pinout

Pin #	Side B - Solder Side	Side A - Component Side
1	Ground	-IOCHK
2	RESET	SD7
3	+5V	SD6
4	IRQ9	SD5
5	-5V	SD4
6	DRQ2	SD3
7	-12V	SD2
8	-0WS	SD1
9	+12V	SD0
10	Ground	IORDY
11	-SMEMW	AEN
12	-SMEMR	SA19
13	-IOW	SA18
14	-IOR	SA17
15	-DAK3	SA16
16	DRQ3	SA15
17	-DAK1	SA14
18	DRQ1	SA13
19	REFRSH	SA12
20	CLK	SA11
21	IRQ7	SA10
22	IRQ6	SA9
23	IRQ5	SA8
24	IRQ4	SA7
25	IRQ3	SA6
26	-DAK2	SA5
27	T/C	SA4
28	BALE	SA3
29	+5V	SA2
30	OSC	SA1
31	Ground	SA0

Pin #	Side D - Solder Side	Side C - Component Side
1	-MEM16	SBHE
2	-IO16	LA23
3	IRQ10	LA22
4	IRQ11	LA21
5	IRQ12	LA20
6	IRQ15	LA19
7	IRQ14	LA18
8	-DAK0	LA17
9	DRQ0	-MEMR
10	-DAK5	-MEMW
11	DRQ5	SD8
12	-DAK6	SD9
13	DRQ6	SD10
14	-DAK7	SD11
15	DRQ7	SD12
16	+5V	SD13
17	-MASTER	SD14
18	Ground	SD15

APPENDIX D - NEX-ISA Silk Screen



APPENDIX E - Support

About Nexus Technology, Inc.

Established in 1991, Nexus Technology, Inc. is dedicated to developing, marketing, and supporting Bus Analysis applications for Tektronix Logic Analyzers.

We can be reached at:

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Support Contact Information

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General Information	**support@nexustechnology.com**
Quote Requests	**quotes@nexustechnology.com**

We will try to respond within one business day.

If Problems Are Found

Document the problem and e-mail the information to us. If at all possible please forward a Saved System Setup (with acquired data) that shows the problem. Do not send a text listing alone as that does not contain enough data for analysis. To prevent corruption during the mailing process it is strongly suggested that the Setup be zipped before transmission.

APPENDIX F - References

Tektronix TLA600/700 System User's Manual

Tektronix TLA600/700 Logic Analyzer User's Manual

Tektronix DAS9200 / TLA500 System User's Manual

Tektronix 92A96 / 92C96 Module User's Manual

"AT Bus Design" by Edward Solari
Published by Annabooks, San Diego, CA

"Intel ISA Bus Specification and Application Notes"
Rev. 3.00, January 30, 1990

"Personal Computer Bus Standard"
IEEE document P996
Draft D2.02, 13 July 1990