PSDB_SRAM™

SRAM Daughter Board

Data Book

January 2008

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USA
1600 Wyatt Drive Suite 1
Santa Clara,
CA 95054, USA

Tel: 1 - 408 - 969 - 0389
Fax: 1 - 866 - 615 - 6810

sales_usa@GiDEL.com

Worldwide
2 Ha'ilan Street, P.O. Box 281
Or Akiva,
Israel 30600

Tel: +972 - 4610 - 2500
Fax:+972 - 4610 - 2501

sales_eu@GiDEL.com

Web: **www.GiDEL.com**
info@GiDEL.com

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Introduction

GiDEL PROCStar II™ and ***PROCSpark II***™ are high performance reconfigurable boards. In addition to the on-board FPGA devices that may perform complex calculations and run the algorithms, various devices may be added to the PROC boards to increase calculation performance. Connectors located on the component side of the PROC boards enable mounting of upto 4 Gidel daughterboards. These daughterboards, designated **PSDB,** may be used for system adaptation and to add logic.

GiDEL PSDB_SRAM™ is a daughterboard designed to provide high-speed and low-latency NoBL SRAM for data storage. This daughterboard is extremely useful when user's design requires very fast and extensive random accesses to memory, as in case of real-time image processing.

There are two types of PSDBs: **PSDB1** and **PSDB2**.

- **PSDB1** (PSDB of type 1) are mainly intended to enable interfacing with the PROC motherboards.
- **PSDB2** (PSDB of type 2) may be used to provide several functions:
  - ✓ Adding unique features, such as DSPs, to the motherboard.
  - ✓ Adding massive and fast connections to the FPGAs.
  - ✓ Providing additional memory storages to the PROC boards.

GiDEL ***PSDB_SRAM*** is a type 2 daughterboard(**PSDB2**). All PSDB2s use two connectors to mount onto the PROC motherboard. These connectors are located on the component side of the motherboard to the left and to the right of each FPGA device.

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PSDB_SRAM Key Features

PSDB_SRAM provides SRAM memory extension to the PROC boards. It is designed to support unlimited true back-to-back Read/Write operations with no wait states. The on-board SRAM device is equipped with the advanced (NoBL) logic required to enable Read/Write operations on consecutive clock cycles. This feature dramatically improves the throughput of data in systems that require frequent Write/Read transitions. In addition, the on-board SRAM chip has an on-chip burst counter that enables the user to supply a single address and conduct up to four Reads/Writes without reasserting the address inputs.

PSDB_SRAM provides the following features:

- ✓ 200 MHz SRAM speed.
- ✓ 512Kx36 SRAM bits.
- ✓ NoBL architecture.
- ✓ Linear / Interleaved burst access ability
- ✓ Automatic detection by hardware / software

PSDB_SRAM Locations

PROCStar II and ***PROCSpark II*** motherboards have a number of connectors that allow different installation options for ***PSDB_SRAM*** daughterboards. The following figure shows installation options for ***PSDB_SRAM*** when using a ***PROCStar II*** motherboard.

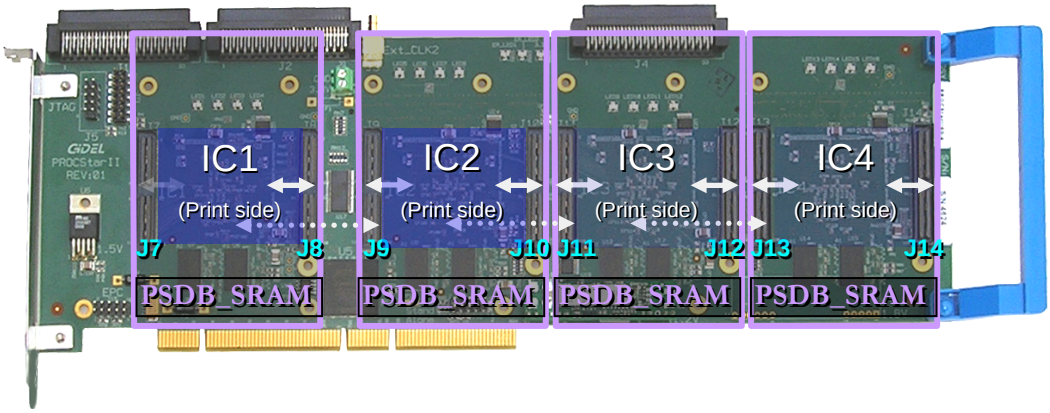

Figure 1: ***PSDB_SRAM*** **locations on** ***PROCStar II***

Since ***PSDB_SRAM*** is a type 2 daughter board (**PSDB2**), it uses two connectors, located to the left and right of the FPGA, to connect to the PROC motherboard. Placing ***PSDB_SRAM***, for example, on J7 and J8 of a ***PROCStar II*** motherboard (location1) connects that daughterboard to IC1 (see Figure 1).

When a ***PROCStar II*** motherboard is used, ***PSDB_SRAM*** daughterboards can be installed on any of the ***four*** available locations, provided there is an FPGA installed on that location. On a ***PROCStarII 60-2*** motherboard, for example, one can install ***PSDB_SRAM*** on locations 1 and 2 only.

Notes

1. The FPGA devices and connectors are located on opposite sides of GiDEL PROC boards. Therefore connecting a daughter board will not limit the FPGAs' cooling.
2. It is possible to connect several daughterboards of different types to a PROC motherboard.

PSDB_SRAM Signals

The ***GiDEL PROCWizard***™ can generate a top-level design for each FPGA located on a ***PROCStar II*** board. For FPGAs that are connected to ***PSDB_SRAM***, ***PROCWizard*** automatically generates the signals, which connect the top-level to the daughterboard. In addition, it generates board constrains needed to connect these signals to the daughterboard physically. The following table describes the generated signals and their functions.

Symbol	Function	Direction
sram_a	SRAM address bus	Output
sram_dqa	SRAM data bus A	In/Out
sram_dqb	SRAM data bus B	In/Out
sram_dqc	SRAM data bus C	In/Out
sram_dqd	SRAM data bus D	In/Out
sram_ce	SRAM chip enable bus	Output
sram_dqpa	SRAM data bus A parity bit	In/Out
sram_dqpb	SRAM data bus B parity bit	In/Out
sram_dqpc	SRAM data bus C parity bit	In/Out
sram_dqpd	SRAM data bus D parity bit	In/Out
sram_bwa	SRAM data bus A write select	Output
sram_bwb	SRAM data bus B write select	Output
sram_bwc	SRAM data bus C write select	Output
sram_bwd	SRAM data bus D write select	Output
sram_adv	SRAM advance	Output
sram_we	SRAM write enable	Output
sram_cen	SRAM clock enable	Output
sram_oe	SRAM output enable	Output
sram_zz	SRAM sleep	Output
sram_mode	SRAM mode	Output
sram_clk	SRAM clock	Output

Table 1 : PSDB_SRAM I/Os

For more information on automatic generation using ***GiDEL PROCWizard***, please refer to ***GiDEL PROCWizard User's Manual***, chapter 5.

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PSDB_SRAM Connectivity

The following simplified schematic diagrams provide information on connectivity between the SRAM Chip and the left PSDB connector.

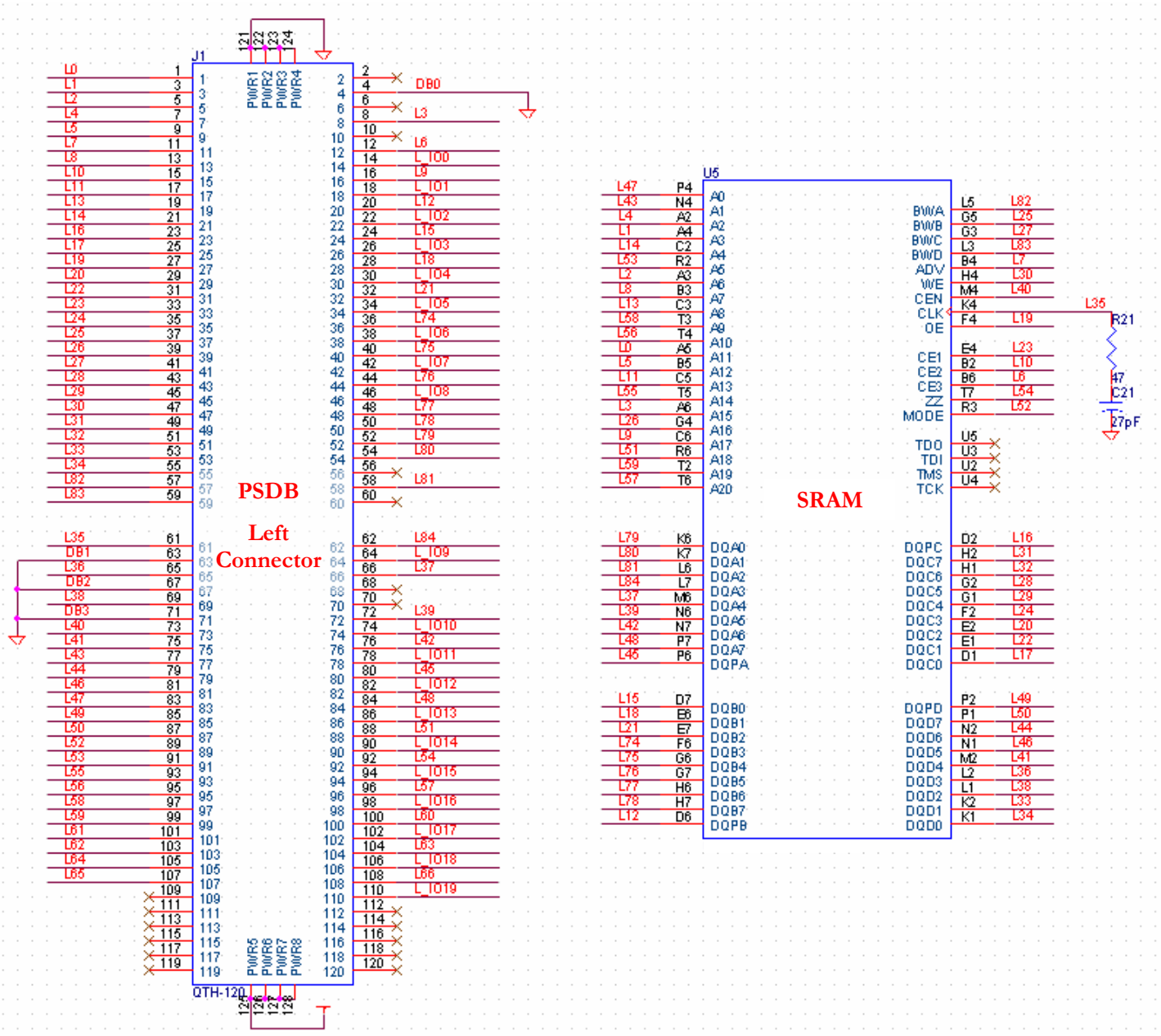

Figure 2: PSDB Left Connector and SRAM Schematics

The following table lists the pin names, as show in Figure 2, and their respective trace delay.

Pin name	Trace delay (ps)
A0	78.6
A1	84.2
A2	58.1
A3	75.9
A4	54.4
A5	58.3
A6	64.3
A7	65.7
A8	63.6
A9	66.5
A10	83.1
A11	86.9
A12	84.1
A13	81.2
A14	89.6
A15	47.7
A16	72.5
A17	55.4
A18	53.5
A19	63.5
A20	52.4
DQA0	51.5
DQA1	57.4
DQA2	49.2
DQA3	61.2
DQA4	52
DQA5	46.3
DQA6	54.5
DQA7	57.3
DQPA	47.4
BWA	85.9
DQB0	57.9
DQB1	50.7
DQB2	59.4
DQB3	46
DQB4	47.7

Pin name	Trace delay (ps)
DQB5	55.3
DQB6	44.8
DQB7	54.9
DQPB	56.8
BWB	83.5
DQC0	45.8
DQC1	46.9
DQC2	55.6
DQC3	55.1
DQC4	43.9
DQC5	61.7
DQC6	43.9
DQC7	54.3
DQPC	56.4
BWC	66.6
DQD0	48.2
DQD1	54.7
DQD2	50.6
DQD3	57.4
DQD4	64.5
DQD5	52.5
DQD6	62.2
DQD7	53.5
DQPD	61.4
BWD	64.7
MODE	67.6
OE	85.4
WE	74.2
ZZ	55
ADV	74.2
CE1	72.1
CE2	55
CE3	49.1
CEN	73.7
CLK	73.1

Table 2: Pin Trace Delay

PSDB_SRAM Mechanical Specifications

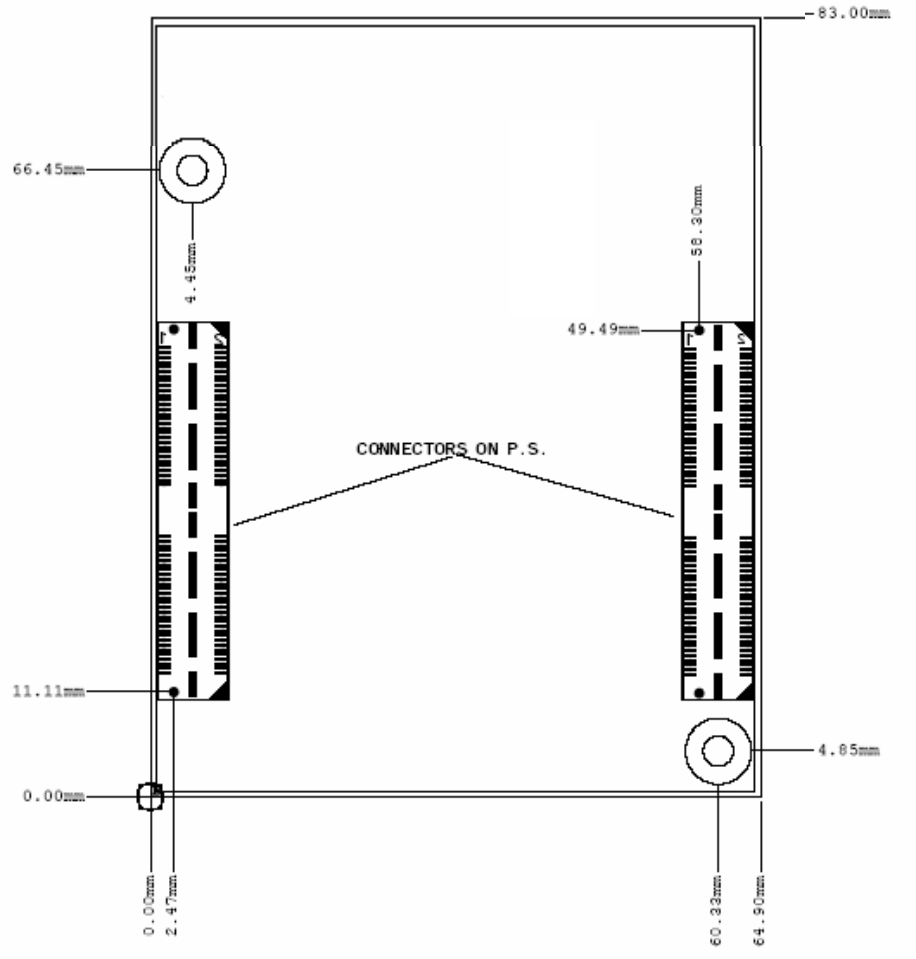

Figure 3 : *PSDB_SRAM* mechanical dimensions (top view).

PSDB_SRAM Power Consumption

The following table describes the ***PSDB_SRAM*** power consumption**.**

	Min	**Typical**	**Max**
Idd (3.3V)	110 mA	350 mA	500 mA

Table 3 : PSDB_SRAM Power Consumption

Revision History

Date	Description
February 2008	SRAM speed update
January 2008	Addition of Pin Trace Delay Table
December 2007	Addition of PSDB Connectivity Schematics
February 2005	Initial Document

Distributed by:

MaxxVision GmbH
Sigmaringer Str. 121
70567 Stuttgart
Tel.: +49 711 997 996 3
Fax: +49 711 997 996 50
www.maxxvision.com
info@maxxvision.com