AT91SAM9G10 Microcontroller Schematic Check List

1. Introduction

This application note is a schematic review check list for systems embedding the Atmel® ARM® Thumb®-based AT91SAM9G10 microcontroller.

It gives requirements concerning the different pin connections that must be considered before starting any new board design and describes the minimum hardware resources required to quickly develop an application with the AT91SAM9G10. It does not consider PCB layout constraints.

It also gives advice regarding low-power design constraints to minimize power consumption.

This application note is not intended to be exhaustive. Its objective is to cover as many configurations of use as possible.

The Check List table has a column reserved for reviewing designers to verify the line item has been checked.

AT91 ARM Thumb-based Microcontrollers

Application Note

6493A–ATARM–31-Jul-09

2. Associated Documentation

Before going further into this application note, it is strongly recommended to check the latest documents for the AT91SAM9G10 Microcontroller on Atmel's Web site.

Table 2-1 gives the associated documentation needed to support full understanding of this application note.

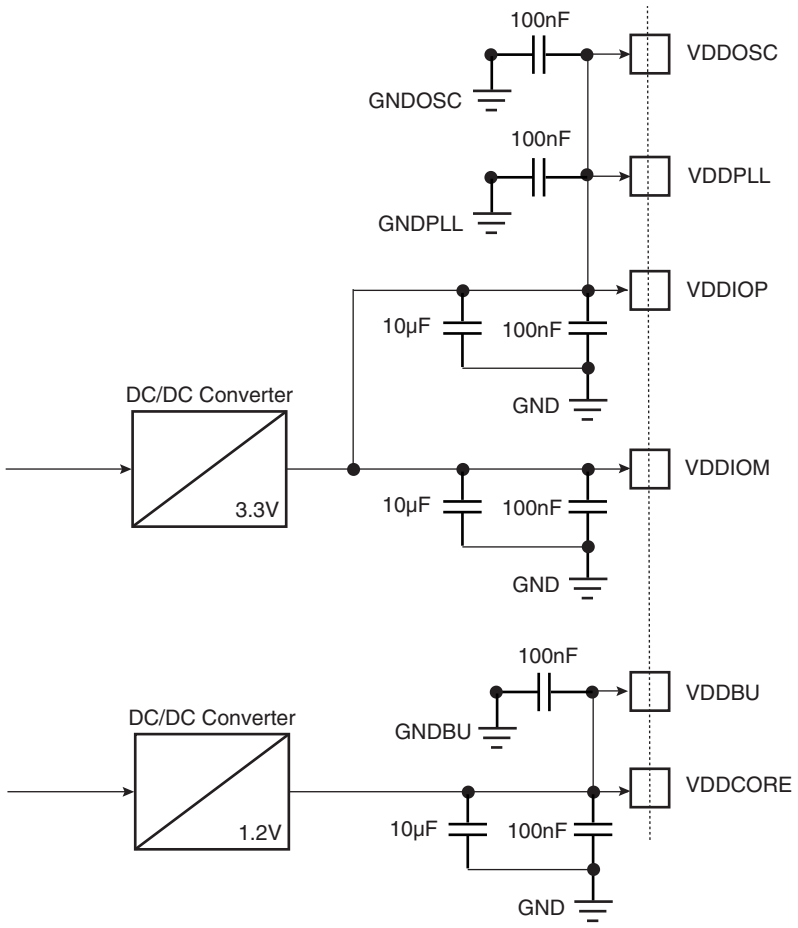
Table 2-1. Associated Documentation

Information	Document Title
User Manual Electrical/Mechanical Characteristics Ordering Information Errata	AT91 ARM Thumb-based Microcontrollers AT91SAM9G10 Preliminary Datasheet
Internal architecture of processor ARM/Thumb instruction sets Embedded in-circuit-emulator	ARM9EJ-S™ Technical Reference Manual ARM926EJ-S™ Technical Reference Manual
Evaluation Kit User Guide	AT91SAM9G10-EKES User Guide
Using SDRAM on AT91SAM9 Microcontrollers	Using SDRAM on AT91SAM9 Microcontrollers Application Note
NAND Flash Support in AT91SAM9 Microcontrollers	NAND Flash Support in AT91SAM9 Microcontrollers Application Note

3. Schematic Check List

CAUTION: The AT91SAM9 board design must comply with the power-up and power-down sequence guidelines provided in the datasheet to guarantee reliable operation of the device.

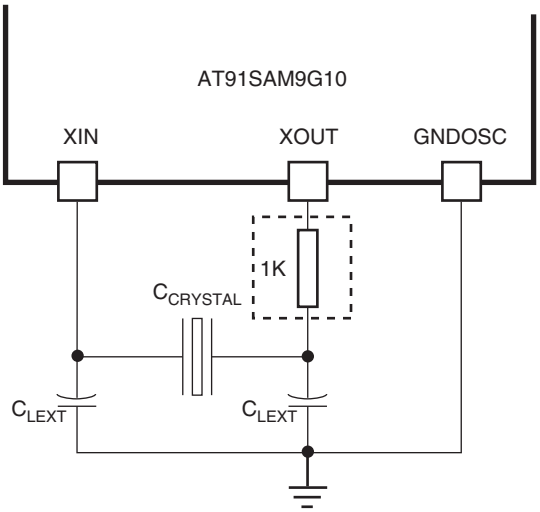
1.2V and 3.3V Dual Power Supply Schematic Example[1]

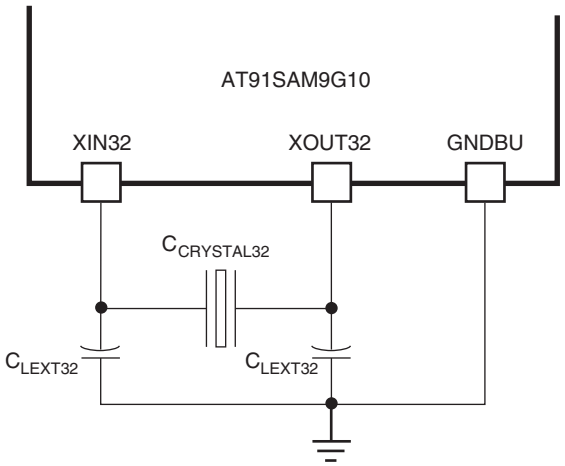
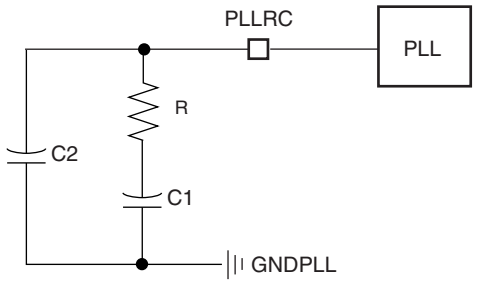


Power Supply on VDDIOP: 3.3V - Power Supply on VDDIOM: 3.3V

[1] These values are given only as a typical example

☑	Signal Name	Recommended Pin Connection	Description
	VDDCORE	1.08V to 1.32V Decoupling/Filtering capacitors (100 nF and 10µF)[1][2]	Powers the device. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDBU	1.08V to 1.32V Decoupling capacitor (100 nF)[1][2]	Powers the Slow Clock oscillator and a part of the System Controller.
	VDDIOM[3]	1.65 to 1.95V or 3.0V to 3.6V Decoupling/Filtering capacitors (100 nF and 10µF)[1][2]	Powers External Bus Interface I/O lines. Dual voltage range supported. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDIOP[3]	2.7V to 3.6V Decoupling/Filtering capacitors (100 nF and 10µF)[1][2]	Powers Peripheral I/O lines and USB transceivers. Decoupling/Filtering capacitors must be added to improve startup stability and reduce source voltage drop.
	VDDOSC	3.0V to 3.6V Decoupling capacitor (100 nF)[1][2]	Powers the Main Oscillator.
	VDDPLL	3.0V to 3.6V Decoupling capacitor (100 nF)[1][2]	Powers the PLL cells.
	GND	Ground	GND pins are common to VDDCORE, VDDIOM and VDDIOP pins. GND pins should be connected as shortly as possible to the system ground plane.
	GNDBU	Backup Ground	GNDBU pin is provided for VDDBU pin. GNDBU pin should be connected as shortly as possible to the system ground plane.
	GNDPLL	PLL Ground	GNDPLL pin is provided for VDDPLL pin. GNDPLL pin should be connected as shortly as possible to the system ground plane.
	GNDOSC	Oscillator Ground	GNDOSC pin is provided for VDDOSC pin. GNDOSC pin should be connected as shortly as possible to the system ground plane.

☑	Signal Name	Recommended Pin Connection	Description
Clock, Oscillator and PLL			
	XIN XOUT Main Oscillator in Normal Mode	Crystals between 3 and 20 MHz Capacitors on XIN and XOUT (crystal load capacitance dependent) 1 kOhm resistor on XOUT only required for crystals with frequencies lower than 8 MHz.	Crystal load capacitance to check ($C_{CRYSTAL}$).  Example: for an 18.432 MHz crystal with a load capacitance of $C_{CRYSTAL}$= 12.5 pF, external capacitors are required: C_{LEXT} = 16.2 pF. Refer to the electrical specifications of the AT91SAM9G10 datasheet.
	XIN XOUT Main Oscillator in Bypass Mode	XIN: external clock source XOUT: can be left unconnected	3.3V square wave signal (VDDPLL) External clock source up to 50 MHz Duty Cycle: 40 to 60% Refer to the electrical specifications of the AT91SAM9G10 datasheet.

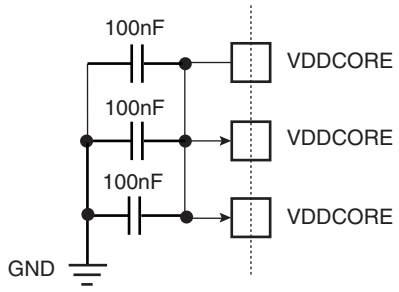
☑	Signal Name	Recommended Pin Connection	Description
	XIN32 XOUT32 Slow Clock Oscillator	32.768 kHz Crystal Capacitors on XIN32 and XOUT32 (crystal load capacitance dependent)	Crystal load capacitance to check ($C_{CRYSTAL32}$).  Example: for a 32.768 kHz crystal with a load capacitance of $C_{CRYSTAL32}$= 12.5 pF, external capacitors are required: C_{LEXT32} = 18 pF. Refer to the electrical specifications of the AT91SAM9G10 datasheet.
	PLLRCA PLLRCB	Second-order filter Can be left unconnected if PLL not used.	See the Excel spreadsheet contained in "ATMEL_PLL_LFT_Filter_CALCULATOR_AT91_xxx.zip" (available from Software Files on the Atmel Web site) allowing calculation of the best R-C1-C2 component values for the PLL Loop Back Filter.  R, C1 and C2 must be placed as close as possible to the pins.

☑	Signal Name	Recommended Pin Connection	Description
ICE and JTAG[4]			
	TCK	Pull-up (100 kOhm)[1]	This pin is a Schmitt trigger input. No internal pull-up resistor.
	TMS	Pull-up (100 kOhm)[1]	This pin is a Schmitt trigger input. No internal pull-up resistor.
	TDI	Pull-up (100 kOhm)[1]	This pin is a Schmitt trigger input. No internal pull-up resistor.
	TDO	Floating	Output driven at up to V_{VDDIOP}
	RTCK	Floating	Output driven at up to V_{VDDIOP}
	NTRST	Please refer to the I/O line considerations and the errata sections of the AT91SAM9G10 datasheet.	Internal pull-up resistor to V_{VDDIOP} (15 kOhm).
	JTAGSEL	**In harsh environments,[5] It is strongly recommended to tie this pin to GNDBU if not used or to add an external low-value resistor (such as 1 kOhm).**	Internal pull-down resistor to GNDBU (15 kOhm). Must be tied to V_{VDDBU} to enter JTAG Boundary Scan.
Reset/Test			
	NRST	Application dependent. Can be connected to a push button for hardware reset.	NRST is configured as an open drain output at power up. NRST is controlled by the Reset Controller (RSTC). An internal pull-up resistor to V_{VDDIOP} (100 kOhm) is available for User Reset and External Reset control.
	TST	**In harsh environments,[5] It is strongly recommended to tie this pin to GNDBU if not used or to add an external low-value resistor (such as 1 kOhm)**	Internal pull-down resistor to GNDBU (15 kOhm).
	BMS (PB3)	Application dependent.	Internal pull-up resistor to V_{VDDIOP} (100 kOhm). Must be tied to V_{VDDIOP} to boot from Embedded ROM. Must be tied to GND to boot from external memory (EBI Chip Select 0).
Shutdown/Wakeup Logic			
	SHDN	Application dependent. Do not tie over V_{VDDBU}. A typical application connects the pin SHDN to the shutdown input of the DC/DC Converter providing the main power supplies.	This pin is a push-pull output. SHDN pin is driven low to GNDBU by the Shutdown Controller (SHDWC).
	WKUP	0V to V_{VDDBU}.	This pin is an input-only. WKUP behavior can be configured through the Shutdown Controller (SHDWC).

☑	Signal Name	Recommended Pin Connection	Description
		PIO	
	PAx PBx PCx	Application dependent.	All PIOs are pulled-up inputs (100 kOhms) at reset except those which are multiplexed with the Address Bus signals that require to be enabled as peripherals. Refer to the column “Reset State” of the PIO Controller multiplexing tables in the product datasheet. Schmitt Trigger on All Inputs To reduce power consumption if not used, the concerned PIO can be configured as an output, driven at ‘0’ with internal pull-up disabled.
		EBI	
	D0-D31	Application dependent.	Data Bus (D0 to D31) Data bus lines are pulled-up inputs to V_{VDDIOM} at reset. Note: D16 to D31 are multiplexed with the PIOC controller.
	A0-A22 (A23-A25)	Application dependent.	Address Bus (A0 to A25) All address lines are driven to ‘0’ at reset. Note: A23 (PA30), A24 (PA31) and A25 (PC3) are enabled by default at reset through the PIO controllers.
SMC - SDRAM Controller - CompactFlash® Support - NAND Flash Support			
See “External Bus Interface (EBI) Hardware Interface” on page 11.			

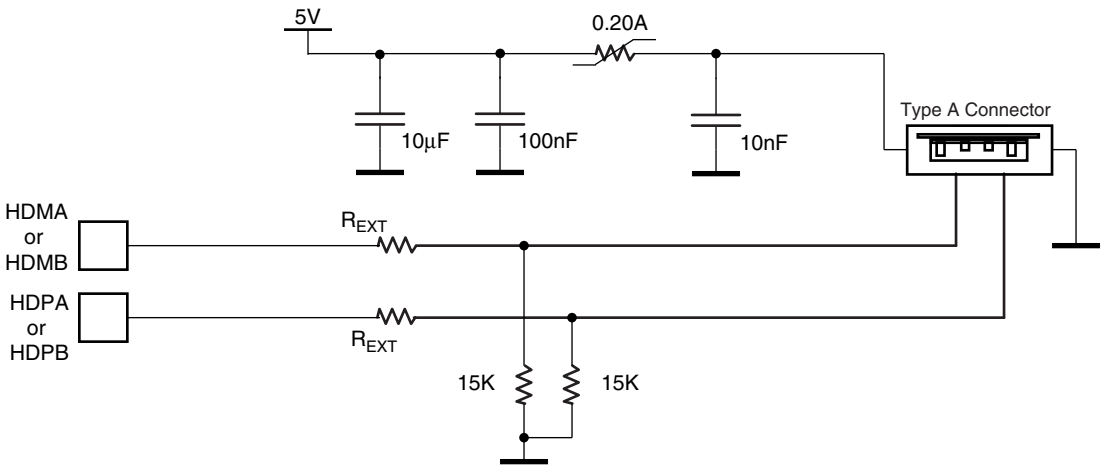
☑	Signal Name	Recommended Pin Connection	Description
USB Host (UHP)			
	HDPA HDPB	Application dependent.[6] Typically, 15 kOhm resistor to GND.	No internal pull-down resistors. To reduce power consumption, if USB Host is not used, connect HDPA/HDPB to GND.
	HDMA HDMB	Application dependent.[6] Typically, 15 kOhm resistor to GND.	No internal pull-down resistors. To reduce power consumption, if USB Host is not used, connect HDMA/HDMB to GND.
USB Device (UDP)			
	DDP	Application dependent.[7]	Integrated programmable pull-up resistor (USB_PUCR) No internal pull-down resistor. To reduce power consumption, if USB Device is not used, connect DDM to GND.
	DDM	Application dependent.[7]	No internal pull-down resistor. To reduce power consumption, if USB Device is not used, connect DDM to GND.

Notes:
1. These values are given only as a typical example.
2. Decoupling capacitors must be connected as close as possible to the microcontroller and on each concerned pin.



3. The double power supplies VDDIOM and VDDIOP power the device differently when interfacing with memories or with peripherals.
4. It is recommended to establish accessibility to a JTAG connector for debug in any case.
5. In a well-shielded environment subject to low magnetic and electric field interference, the pin may be left unconnected. In noisy environments, a connection to ground is recommended.

6. Example of USB Host connection:
   A termination serial resistor (R_{EXT}) must be connected to HDPA/HDPB and HDMA/HDMB. A recommended resistor value is defined in the electrical specifications of the AT91SAM9G10 datasheet.



7. Example of USB Device connection:
   As there is an embedded pull-up, no external circuitry is necessary to enable and disable the 1.5 kOhm pull-up.
   To prevent over consumption when the host is disconnected, an external pull-down can be added to DDP and DDM.
   A termination serial resistor (R_{EXT}) must be connected to DDP and DDM. A recommended resistor value is defined in the electrical specifications of the AT91SAM9G10 datasheet.

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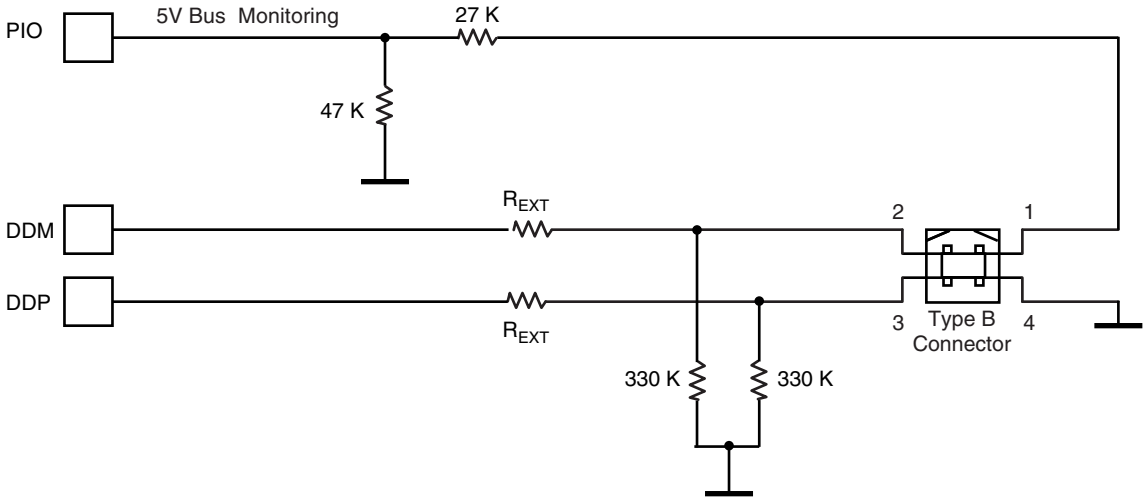

4. External Bus Interface (EBI) Hardware Interface

Table 4-1 and Table 4-2 detail the connections to be applied between the EBI pins and the external devices for each Memory Controller.

Table 4-1. EBI Pins and External Static Devices Connections

Pins	Pins of the Interfaced Device					
	8-bit Static Device	2 x 8-bit Static Devices	16-bit Static Device	4 x 8-bit Static Devices	2 x 16-bit Static Devices	32-bit Static Device
Controller	**SMC**					
D0 - D7	D0 - D7	D0 - D7	D0 - D7	D0 - D7	D0 - D7	D0 - D7
D8 - D15	–	D8 - D15	D8 - D15	D8 - D15	D8 - 15	D8 - 15
D16 - D23	–	–	–	D16 - D23	D16 - D23	D16 - D23
D24 - D31	–	–	–	D24 - D31	D24 - D31	D24 - D31
A0/NBS0	A0	–	NLB	–	NLB(3)	BE0(5)
A1/NWR2/NBS2	A1	A0	A0	WE(2)	NLB(4)	BE2(5)
A2 - A25	A[2:25]	A[1:24]	A[1:24]	A[0:23]	A[0:23]	A[0:23]
NCS0	CS	CS	CS	CS	CS	CS
NCS1/SDCS	CS	CS	CS	CS	CS	CS
NCS2	CS	CS	CS	CS	CS	CS
NCS3/NANDCS	CS	CS	CS	CS	CS	CS
NCS4/CFCS0	CS	CS	CS	CS	CS	CS
NCS5/CFCS1	CS	CS	CS	CS	CS	CS
NCS6/NAND0E	CS	CS	CS	CS	CS	CS
NCS7/NANDWE	CS	CS	CS	CS	CS	CS
NRD/CFOE	OE	OE	OE	OE	OE	OE
NWR0/NWE	WE	WE(1)	WE	WE(2)	WE	WE
NWR1/NBS1	–	WE(1)	NUB	WE(2)	NUB(3)	BE1(5)
NWR3/NBS3	–	–	–	WE(2)	NUB(4)	BE3(5)

Notes:
1. NWR0 enables lower byte writes. NWR1 enables upper byte writes.
2. NWRx enables corresponding byte x writes (x = 0, 1, 2 or 3).
3. NBS0 and NBS1 enable respectively lower and upper bytes of the lower 16-bit word.
4. NBS2 and NBS3 enable respectively lower and upper bytes of the upper 16-bit word.
5. BEx: Byte x Enable (x = 0,1,2 or 3)

Table 4-2. EBI Pins and External Devices Connections

Pins	Pins of the Interfaced Device			
	SDRAM[3]	Compact Flash	Compact Flash True IDE Mode	NAND Flash[4]
Controller	**SDRAMC**	**SMC**		
D0 - D7	D0 - D7	D0 - D7	D0 - D7	I/O0-I/O7
D8 - D15	D8 - D15	D8 - 15	D8 - 15	I/O8-I/O15[5]
D16 - D31	D16 - D31	–	–	–
A0/NBS0	DQM0	A0	A0	–
A1/NWR2/NBS2	DQM2	A1	A1	–
A2 - A10	A[0:8]	A[2:10]	A[2:10]	–
A11	A9	–	–	–
SDA10	A10	–	–	–
A12	–	–	–	–
A13 - A14	A[11:12]	–	–	–
A15	–	–	–	–
A16/BA0	BA0	–	–	–
A17/BA1	BA1	–	–	–
A18 - A20	–	–	–	–
A21	–	–	–	CLE
A22	–	REG	REG	ALE
A23 - A24	–	–	–	–
A25	–	CFRNW[1]	CFRNW[1]	–
NCS0	–	–	–	–
NCS1/SDCS	CS	–	–	–
NCS2	–	–	–	–
NCS3/NANDCS	–	–	–	CE[6]
NCS4/CFCS0	–	CFCS0[1]	CFCS0[1]	–
NCS5/CFCS1	–	CFCS1[1]	CFCS1[1]	–
NCS6/NANDOE	–	–	–	RE
NCS7/NANDWE	–	–	–	WE
NRD/CFOE	–	OE	–	–
NWR0/NWE/CFWE	–	WE	WE	–
NWR1/NBS1/CFIOR	DQM1	IOR	IOR	–
NWR3/NBS3/CFIOW	DQM3	IOW	IOW	–
CFCE1	–	CE1	CS0	–
CFCE2	–	CE2	CS1	–
SDCK	CLK	–	–	–

Table 4-2. EBI Pins and External Devices Connections (Continued)

Pins	Pins of the Interfaced Device			
	SDRAM[3]	Compact Flash	Compact Flash True IDE Mode	NAND Flash[4]
Controller	**SDRAMC**	**SMC**		
SDCKE	CKE	–	–	–
RAS	RAS	–	–	–
CAS	CAS	–	–	–
SDWE	WE	–	–	–
NWAIT	–	WAIT	WAIT	–
Pxx[2]	–	CD1 or CD2	CD1 or CD2	–
Pxx[2]	–	–	–	CE[6]
Pxx[2]	–	–	–	RDY

Notes:
1. Not directly connected to the CompactFlash slot. Permits the control of the bidirectional buffer between the EBI data bus and the CompactFlash slot.
2. Any PIO line.
3. For SDRAM connection examples, see Using SDRAM on AT91SAM9 Microcontrollers application note.
4. For NAND Flash connection examples, see NAND Flash Support in AT91SAM Microcontrollers application note.
5. I/O8 - I/O15 bits used only for 16-bit NAND Flash.
6. CE connection depends on the Nand Flash.
   For standard NAND Flash devices, it must be connected to any free PIO line.
   For “CE don’t care” NAND Flash devices, it can be either connected to NCS3/NANDCS or to any free PIO line.

5. AT91SAM Boot Program Hardware Constraints

See the AT91SAM Boot Program section of the AT91SAM9G10 datasheet for more details on the boot program.

5.1 AT91SAM Boot Program Supported Crystals (MHz)

The Main Oscillator is not bypassed by the Boot ROM. Thus, It is possible to use the crystals shown in Table 5.1 but not external clocks.

Table 5-1. Supported Crystals (MHz)

3.0	3.2768	3.6864	3.84	4.0
4.433619	4.608	4.9152	5.0	5.24288
6.0	6.144	6.4	6.5536	7.159090
7.3728	7.864320	8.0	9.8304	10.0
11.05920	12.0	12.288	13.56	14.31818
14.7456	16.0	17.734470	18.432	20.0

5.2 SAM-BA® Boot

The SAM-BA Boot Assistant supports serial communication via the DBGU or the USB Device Port.

Table 5-2. Pins Driven during SAM-BA Boot Program Execution

Peripheral	Pin	PIO Line
DBGU	DRXD	PA9
DBGU	DTXD	PA10

5.3 Serial and DataFlash® Boot

The Serial and DataFlash Boot programs search for a valid application in either a SPI Serial Flash or a DataFlash memory.

The memory must be connected to NPCS0 of the SPI0.

The DataFlash and Serial Flash downloaded code size must be smaller than 12 kbytes.

Table 5-3. Pins Driven during DataFlash Boot Program Execution

Peripheral	Pin	PIO Line
SPI0	MOSI	PA1
SPI0	MISO	PA0
SPI0	SPCK	PA2
SPI0	NPCS0	PA3

5.4 NAND Flash Boot

The NAND Flash Boot program searches for a valid application in an SLC 8-bit or 16-bit NAND Flash memory.

The NandFlash downloaded code size must be smaller than 12 kbytes.

Table 5-4. Pins Driven during NAND Flash Boot Program Execution

Peripheral	Pin	PIO Line
PIOC	NAND CS	PC14
PIOC	NAND OE	PC0
PIOC	NAND WE	PC1
Address Bus	NAND CLE	A21
Address Bus	NAND ALE	A22

5.5 EEPROM Boot

The EEPROM Boot program searches for a valid application in the EEPROM memory connected to the TWI.

The EEPROM downloaded code size must be smaller than 12 kbytes.

Table 5-5. Pins driven during EEPROM Boot Program Execution

Peripheral	Pin	PIO Line
TWI	TWCK	PA8
TWI	TWD	PA7

5.6 SD Card Boot

The SD Card Boot program searches for a valid application in a standard SD Card memory (High Capacity SDCards (SDHC) are not supported by the SDCard Boot).

The SDCard downloaded code size must be smaller than 12 kbytes.

Table 5-6. Pins Driven during SD Card Boot Program Execution

Peripheral	Pin	PIO Line
MCI0	MCCK	PA2
MCI0	MCCDA	PA1
MCI0	MCDA0	PA0
MCI0	MCDA1	PA4
MCI0	MCDA2	PA5
MCI0	MCDA3	PA6

Revision History

Doc. Rev	Comments	Change Request Ref.
6493A	First issue	

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