MIP405T

USERS MANUAL

MPL Industrial PC with IBM PowerPC™ Processor

The MIP405T is a highly integrated industrial single board computer in PC/104 form factor. Build around the PPC405 IBM PowerPC™ Processor it is well suited for applications requiring small size, high performance and Low Power. The MIP405T can be used in a standard operating environment without the necessity of a fan.

All major components required to build a industrial PC system are implemented on a single PC/104 sized board. It features one E-IDE, one 10/100Base TX Ethernet, two serial ports, and a real time clock. The 16-bit PC/104 (ISA) and the PC/104+ (PCI) interface offers easy and flexible expansion capabilities.

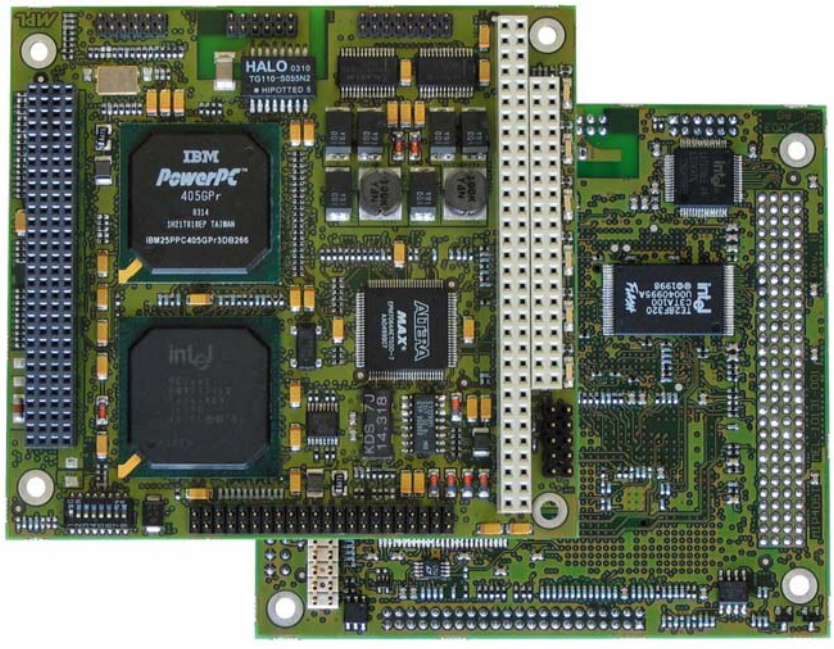
Integration of the MIP405T into a system is facilitated by the fact of offering standard a connector E-IDE (44 pin header). The serial interfaces as can be accessed through 2mm pin headers. Particular precaution has been taken to the EMC so that an entire system can fulfill the CE and FCC requirements.

The SDRAM is soldered on board.

All these features make the MIP405T to the ideal solution for any low-cost embedded control application where a flexible industrial PC is needed.

Features

- Low Power IBM PPC405 Processor
- Processor clock up to 400 MHz
- Up to 128MByte SDRAM on board.
- Integrated 10/100 Mbit/s Ethernet Controller
- PC/104 and PC/104 Plus interface
- One EIDE HDD ports
- Two RS232 ports
- Low power consumption



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1. Introduction

1.1 About this manual

This manual assists the installation and initialization procedure by providing all hardware related information necessary to handle and configure the MIP405T.
For all bootloader related information please refer to the PPCBoot for the MIP405T User Manual (MEH-10082-002) supplied by MPL AG or your local MIP405T supplier. The PPCBoot for MIP405T User Manual is also available on the internet under "http://www.mpl.ch" in PDF format.
The manual is written for technical personnel responsible for integrating the MIP405T into their system.

1.2 Safety precautions and handling

For personal safety and safe operation of the MIP405T, follow all safety procedures described here and in other sections of the manual.

- Power must be removed from the system before installing (or removing) the MIP405T to prevent the possibility of personal injury (electrical shock) and/or damage to the product.
- Handle the product carefully, i.e., dropping or mishandling the MIP405T can cause damage to assemblies and .
- Do not expose the equipment to moisture.

WARNING

There are no user-serviceable components on the MIP405T

1.3 Electrostatic discharge (ESD) protection

Various electrical components within the product are sensitive to static and electrostatic discharge (ESD). Even a non-sensible static discharge can be sufficient to destroy or degrade a component's operation!

1.4 Equipment safety

Great care is taken by MPL that all its products are thoroughly and rigorously tested before leaving the factory to ensure that they are fully operational and conform to specification. However, no matter how reliable a product, there is always the remote possibility that a defect may occur. The occurrence of a defect on this device may, under certain conditions, cause a defect to occur in adjoining and/or connected equipment. It is the user's responsibility to ensure that adequate protection for such equipment is incorporated when installing this device. MPL accepts no responsibility whatsoever for such kind of defects, however caused.

2. General information and specifications

This chapter provides a general overview over the MIP405T and its features. It outlines the electrical and physical specifications of the product, its power requirements and a list of related publications.

2.1 Specifications

Electrical

Processor:
- IBM PPC405GPr PowerPC™ 32Bit RISC Processor
- Separate, configurable, two-way set-associative instruction (16 kByte) and data (16 kByte) cache units
- Technology: IBM CMOS SA-27E, 0.18 Micron Process Technology
- Clock frequency up to 400 MHz
- Very low power consumption

Bootloader ROM:
- Up to 8MB Flash EEPROM
- 512kB PPCBoot (open source) boot loader
- Easy boot loader update

Memory:
- Up to 128MByte soldered SDRAM on board

RTC:
- backed with external battery
- Year 2000 compliant

PC/104 /Plus interface:
- ISA bridge Intel 82371EB (Southbridge)
- 16 Bit PC/104 interface
- 32 Bit PC/104 Plus interface

Serial ports:
- 1 RS232 port with full modem handshake
- 1 selectable port RS232 / TTL
- RS232 transfer rates up to 230 kBaud
- TTL transfer rates up to 1.15 MBaud
- Available on 16pin 2mm header

E-IDE port:
- Up to 2 drives
- Available on 44 pin header, 2 mm pitch, for 2,5” Notebook hard disk.
- PIO Mode 4 and Bus Master IDE, transfers up to 14 Mbytes/s
- Ultra DMA/33 mode, synchronous DMA mode transfers up to 33 Mbytes/s
- Activity indicator on board

Ethernet:
- PPC405 integrated 10/100 MBit/s Ethernet Controller
- IEEE802.3 10BASE-T and 100BASE-TX compatible
- IEEE 802.3u Autonegotiation Support
- IEEE 802.3x 100BASE-TX Flow Control support
- Activity indicators for link detection/network traffic and 100 Mbit/s operation on board

Indicators:
- Power LED (green)
- Reset / Power Fail LED (red)
- Error LED (red)
- HDD activity LED (green)
- LAN LED (green)
- 1 user programmable LED (green)

PHYSICAL/POWER

Form factor:
PC/104, with connectors in defined I/O connectors overhang regions
Length: 95.89 mm (3.775 inches)
Width: 90.17 mm (3.550 inches)
Height: 8.5 mm (0.335 inch) (excluding PC/104 bus connectors)

Weight:
ca. 80g

Power supply:
Over PC/104 bus interface or through separate 10-pin 2,54mm header connector.

Input Power requirement:
+5V: +5VDC ± 5%

Power consumption:
t.b.d.

ENVIRONMENT

Temperature range:
-40°C to +85°C (-40°F to +185°F)

Relative humidity:
10% ... 90% non condensing

2.2 Dimensions

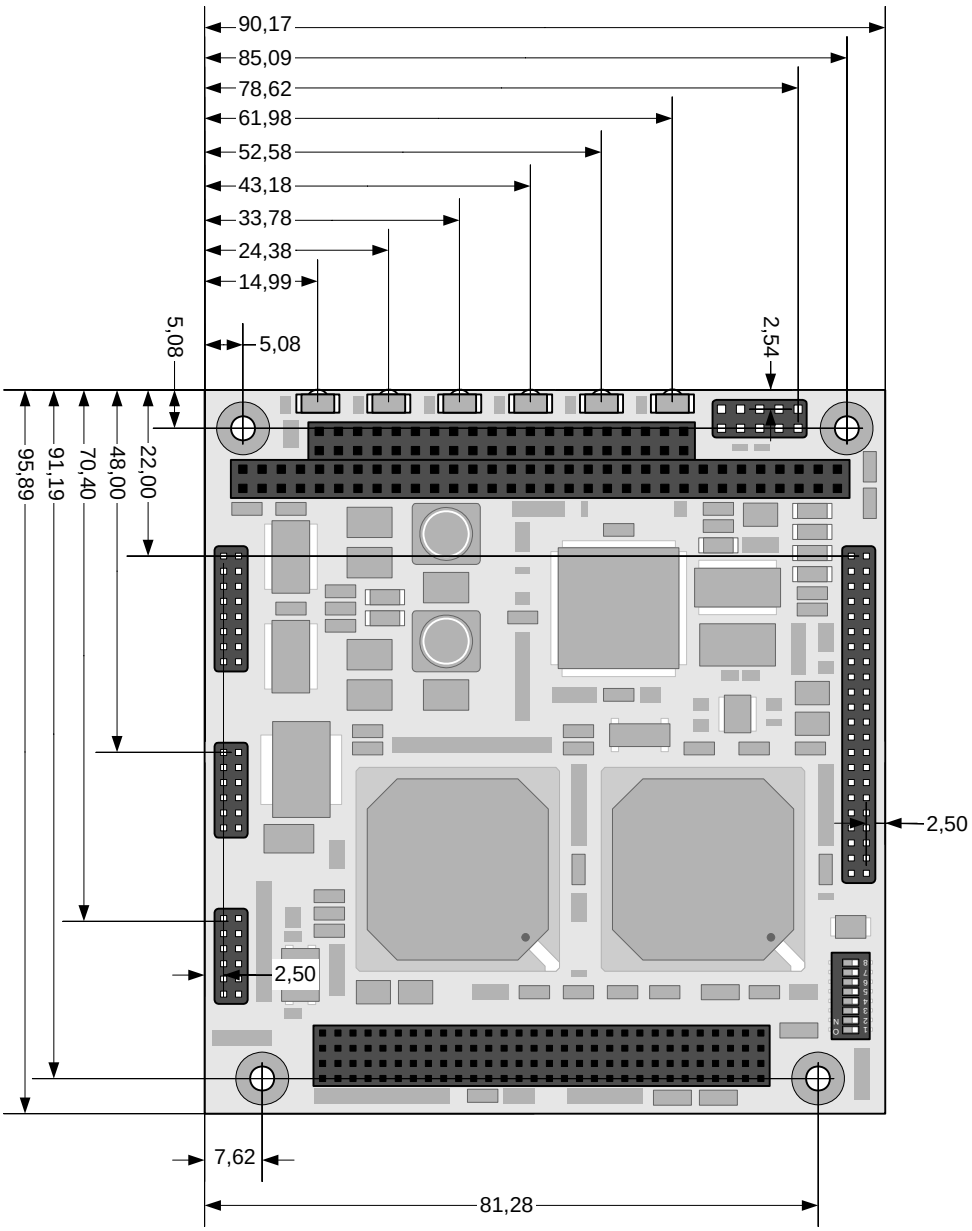


Figure 2.2.1 Dimensions MIP405T

3. Preparation for use

3.1 Parts location

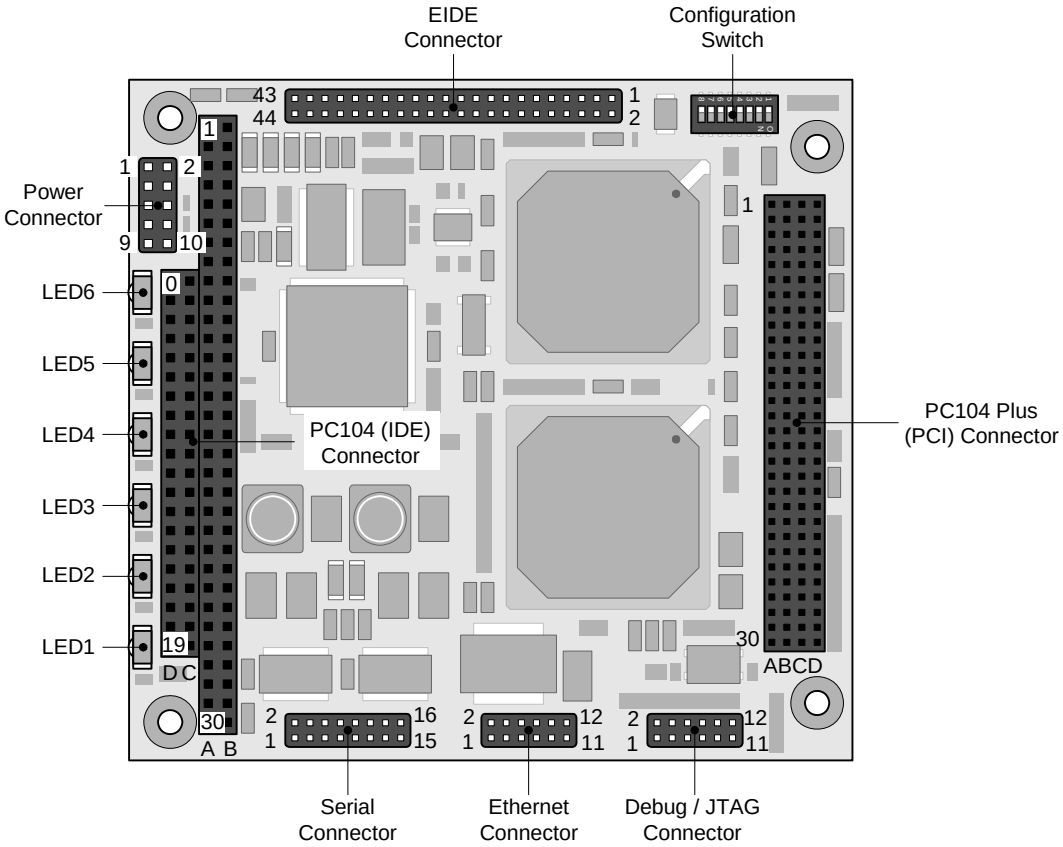


Figure 3.1.1 Parts location

3.2 Switch settings

Default switch settings are bold. Please note, that modifications of the switches during operation have no effect. The changes become valid after the next reset.

3.2.1 Configuration Switch

PPC405 PLL Settings						
S1	**S2**	**S3**	**CPU**	**PLB**	**OPB**	**PPC405 processor**
OFF	OFF	OFF	132 MHz	66 MHz	16.5 MHz	GPr-266/333/400, GP-200/266
OFF	OFF	ON	165 MHz	66 MHz	16.5 MHz	GPr-266/333/400
OFF	ON	OFF	198 MHz	99 MHz	24.75 MHz	GPr-266/333/400, GP-200/266
OFF	ON	ON	247.5 MHz	99 MHz	24.75 MHz	GPr-266/333/400
ON	OFF	OFF	264 MHz	132 MHz	33 MHz	GPr-266/333/400, GP-266
ON	OFF	ON	297 MHz	99 MHz	24.75 MHz	GPr-333/400
ON	ON	OFF	330 MHz	132 MHz	33 MHz	GPr-333/400
ON	ON	ON	396 MHz	132 MHz	33 MHz	GPr-400
S4			**Serial Port 1 Interface Mode**			
ON			TTL			
OFF			RS232			
S5			**EEPROM write protection**			
ON			Write protected			
OFF			Unprotected			
S6			**FLASH write protection**			
ON			Write protected			
OFF			Unprotected			
S7			**User Configuration 1**			
ON			User defined			
OFF			User defined			
S8			**User Configuration 2**			
ON			User defined			
OFF			User defined			

Table 3.2.1Configuration Switch

3.3 LED Indicators

Ref	Color	Function	Description
LED6	Green	USER	Lit if ULED bit is set in extension register *COM_Mode* (please refer to 4.3.5)
LED5	Green	LAN	Lit when LAN activity is detected
LED4	Green	IDE	Lit when IDE activity is detected
LED3	Red	EXEPTION	Lit when PPC405 has detected an Error (Sys_Error)
LED2	Red	RESET	Lit when PPC405 is in Reset state
LED1	Green	POWER	Lit when 5V power is Ok

Table 3.3.1 Indicators

3.4 Connectors

3.4.1 Serial port connector

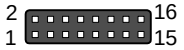
Number	Signal	Description	Pinout
1	RXD1 (TTL)	Receive Data, Port 1 (TTL)	
2	TXD1 (TTL)	Transmit Data, Port 1 (TTL)	
3	RXD1	Receive Data, Port 1	
4	TXD1	Transmit Data, Port 1	
5	RTS1/DTR1	Request to Send or Data Terminal Ready, Port 1	
6	CTS1/DSR1	Clear to Send or Data Set Ready, Port 1	
7	DCD0	Carrier Detect, Port 0	
8	DSR0	Data Set Ready, Port 0	
9	RXD0	Receive Data, Port 0	
10	RTS0	Request to Send, Port 0	
11	TXD0	Transmit Data, Port 0	
12	CTS0	Clear to Send, Port 0	
13	DTR0	Data Terminal Ready, Port 0	
14	RI0	Ring Indicator, Port 0	
15	GND	Ground	
16	GND	Ground	

Table 3.4.1 Serial Port Connector

3.4.2 Debug/JTAG connector

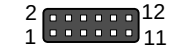
Number	Signal	Description	Pinout
1	VCC5	5V power supply	
2	GND	Ground	
3	CPU_TDO	CPU JTAG Data Out	
4	CPU_TDI	CPU JTAG Data In	
5	CPU_TRST#	CPU JTAG Reset	
6	CPU_TCK	CPU JTAG Clock	
7	CPU_TMS	CPU JTAG Mode Select	
8	CPU_HALT#	CPU Halt	
9	PLD_TDI	PLD JTAG Data In	
10	PLD_TDO	PLD JTAG Data Out	
11	PLD_TMS	PLD JTAG Mode Select	
12	PLD_TCK	PLD JTAG Clock	

Table 3.4.2 Debug/JTAG connector

3.4.3 Ethernet Connector

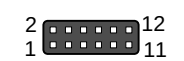
Number	Signal	Description	Pinout
1	TX+	Transmit Data +	
2	TX-	Transmit Data -	
3	RX+	Receive Data +	
4	TERM1	Common Mode Termination 1	
5			
6	RX-	Receive Data -	
7	TERM2	Common Mode Termination 2	
8			
9	NC		
10	NC		
11	EARTH	Shield	
12	EARTH	Shield	

Table 3.4.3 10/100Base TX Header

3.4.4 Power Connector

This connector is needed if no power via PC104 bus is provided. No other inputs than this and the power inputs on PC104 bus must be used to power the board.

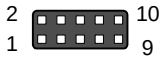
Pin number	Signal	Description	Pinout
1	GND	Ground	
2	V_{IN}	Input voltage	
3	GND	Ground	
4	V_{IN}	Input voltage	
5	SRESET#	System Reset Input (active low)	
6	V_{RTC}	RTC Backup Voltage	
7	V_{IN}	Input voltage	
8	GND	Ground	
9	V_{IN}	Input voltage	
10	GND	Ground	

Table 3.4.4 Power connector

Input Voltage : $+5V_{DC}$ (+-5%)
RTC Backup Voltage: $+2.5V_{DC}$ ... $+4.5V_{DC}$
Contact Current: max. 3A

WARNING
Be aware of the input voltage polarization !
Wrong polarization of the input voltage can cause serious damage to the MIP405T and attached peripherals!

3.4.4.1 Mounting an external Reset Switch

On the SRESET# input on the External Power Connector exists the possibility to mount an external Reset Switch for system reset, see Figure . The SRESET# input is active low and can be connected directly to an open drain output (internal 10kΩ pull up resistor to 3.3V).

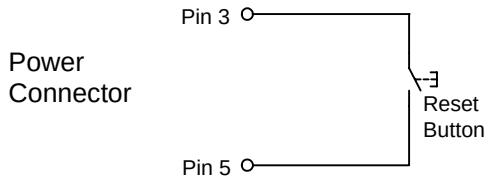


Figure 3.4.4.1 Mounting an External Reset Switch

WARNING
Do not apply other voltages than Vin- or tristate to the SRESET# input!
Exceeding these limits can cause serious damage to the MIP405T!

3.4.5 PC104 interface pin numbers

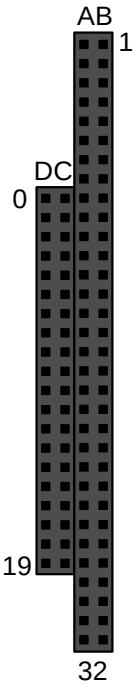
Number	Row A	Row B	Row C	Row D	Pinout
0	--	--	GND	GND	
1	/IOCHCK	GND	/SBHE	/MEMCS16	
2	SD7	RSTDRV	LA23	/IOCS16	
3	SD6	+5V	LA22	IRQ10	
4	SD5	IRQ9	LA21	IRQ11	
5	SD4	(-5V)[1]	LA20	IRQ12	
6	SD3	DRQ2	LA19	IRQ15	
7	SD2	(-12V)[1]	LA18	IRQ14	
8	SD1	/ENDXFR	LA17	/DACK0	
9	SD0	(+12V)[1]	/MEMR	DRQ0	
10	IOCHRDY	NC	/MEMW	/DACK5	
11	AEN	/SMEMW	SD8	DRQ5	
12	SA19	/SMEMR	SD9	/DACK6	
13	SA18	/IOW	SD10	DRQ6	
14	SA17	/IOR	SD11	/DACK7	
15	SA16	/DACK3	SD12	DRQ7	
16	SA15	DRQ3	SD13	+5V	
17	SA14	/DACK1	SD14	(/MASTER)[1]	
18	SA13	DRQ1	SD15	GND	
19	SA12	/REFRESH	NC	GND	
20	SA11	SYSCLK	--	--	
21	SA10	IRQ7	--	--	
22	SA9	IRQ6	--	--	
23	SA8	IRQ5	--	--	
24	SA7	IRQ4	--	--	
25	SA6	IRQ3	--	--	
26	SA5	/DACK2	--	--	
27	SA4	TC	--	--	
28	SA3	BALE	--	--	
29	SA2	+5V	--	--	
30	SA1	OSC	--	--	
31	SA0	GND	--	--	
32	GND	GND	--	--	

Table 3.4.5 PC/104 connector

Notes:

[1] *Signal not available. (-5V, +12V and -12V are not connected and /MASTER is pulled-down to GND)*

3.4.6 PC104+ Interface pin numbers

Number	Row A	Row B	Row C	Row D	Pinout
1	GND	NC	+5V	AD0	
2	+5V	AD2	AD1	+5V	
3	AD5	GND	AD4	AD3	
4	C/BE0	AD7	GND	AD6	
5	GND	AD9	AD8	GND	
6	AD11	+5V	AD10	(M66EN)[1]	
7	AD14	AD13	GND	AD12	
8	(+3.3V)[2]	C/BE1	AD15	(+3.3V)[2]	
9	SERR	GND	(SBO)[1]	PAR	
10	GND	PERR	(+3.3V)[2]	(SDONE)[1]	
11	STOP	(+3.3V)[2]	(LOCK)[1]	GND	
12	(+3.3V)[2]	TRDY	GND	DEVSEL	
13	FRAME	GND	IRDY	(+3.3V)[2]	
14	GND	AD16	(+3.3V)[2]	C/BE2	
15	AD18	(+3.3V)[2]	AD17	GND	
16	AD21	AD20	GND	AD19	
17	(+3.3V)[2]	AD23	AD22	(+3.3V)[2]	
18	IDSEL0	GND	IDSEL1	IDSEL2	
19	AD24	C/BE3	+5V	IDSEL3	
20	GND	AD26	AD25	GND	
21	AD29	+5V	AD28	AD27	
22	+5V	AD30	GND	AD31	
23	REQ0	GND	REQ1	+5V	
24	GND	REQ2	+5V	GNT0	
25	GNT1	+5V	GNT2	GND	
26	+5V	CLK0	GND	CLK1	
27	CLK2	+5V	CLK3	GND	
28	GND	INTD	+5V	RST	
29	(+12V)[1]	INTA	INTB	INTC	
30	(-12V)[1]	NC	NC	GND	

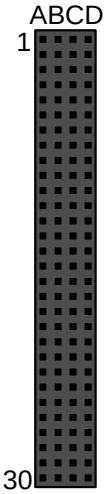


Table 3.4.6 PC/104 Plus connector

Notes:

[1] *Signal not available. (SBO, SDONE and LOCK are pull-up to 5V, M66EN is connected to GND and +12V and -12V are not connected).*

[2] *3.3V power pins are not connected.*

3.4.7 E-IDE connector

Pin	Signal	Description	Pin	Signal	Description
1	/RESET	Reset	2	GND	Ground
3	D7	Data bit 7	4	D8	Data bit 8
5	D6	Data bit 6	6	D9	Data bit 9
7	D5	Data bit 5	8	D10	Data bit 10
9	D4	Data bit 4	10	D11	Data bit 11
11	D3	Data bit 3	12	D12	Data bit 12
13	D2	Data bit 2	14	D13	Data bit 13
15	D1	Data bit 1	16	D14	Data bit 14
17	D0	Data bit 0	18	D15	Data bit 15
19	GND	Ground	20	KEY	Key / not connected
21	DRQ	DMA request	22	GND	Ground
23	IOW	I/O write strobe	24	GND	Ground
25	IOR	I/O read strobe	26	GND	Ground
27	IORDY	I/O ready	28	HDBALE	Spindle sync / cable select
29	DACK	DMA acknowledge	30	GND	Ground
31	IRQ	Interrupt request	32	IOCS16	I/O chipselect16
33	A1	Address 1	34	NC	Not connected
35	A0	Address 0	36	A2	Address 2
37	CS0	Chipselect 0	38	CS1	Chipselect 1
39	ACTLED	Activity LED	40	GND	Ground
41	VCC	+5V	42	VCC	+5V
43	GND	Ground	44	GND	Ground

Table 3.4.7 EIDE connectors

4. Operation

4.1 Block diagram

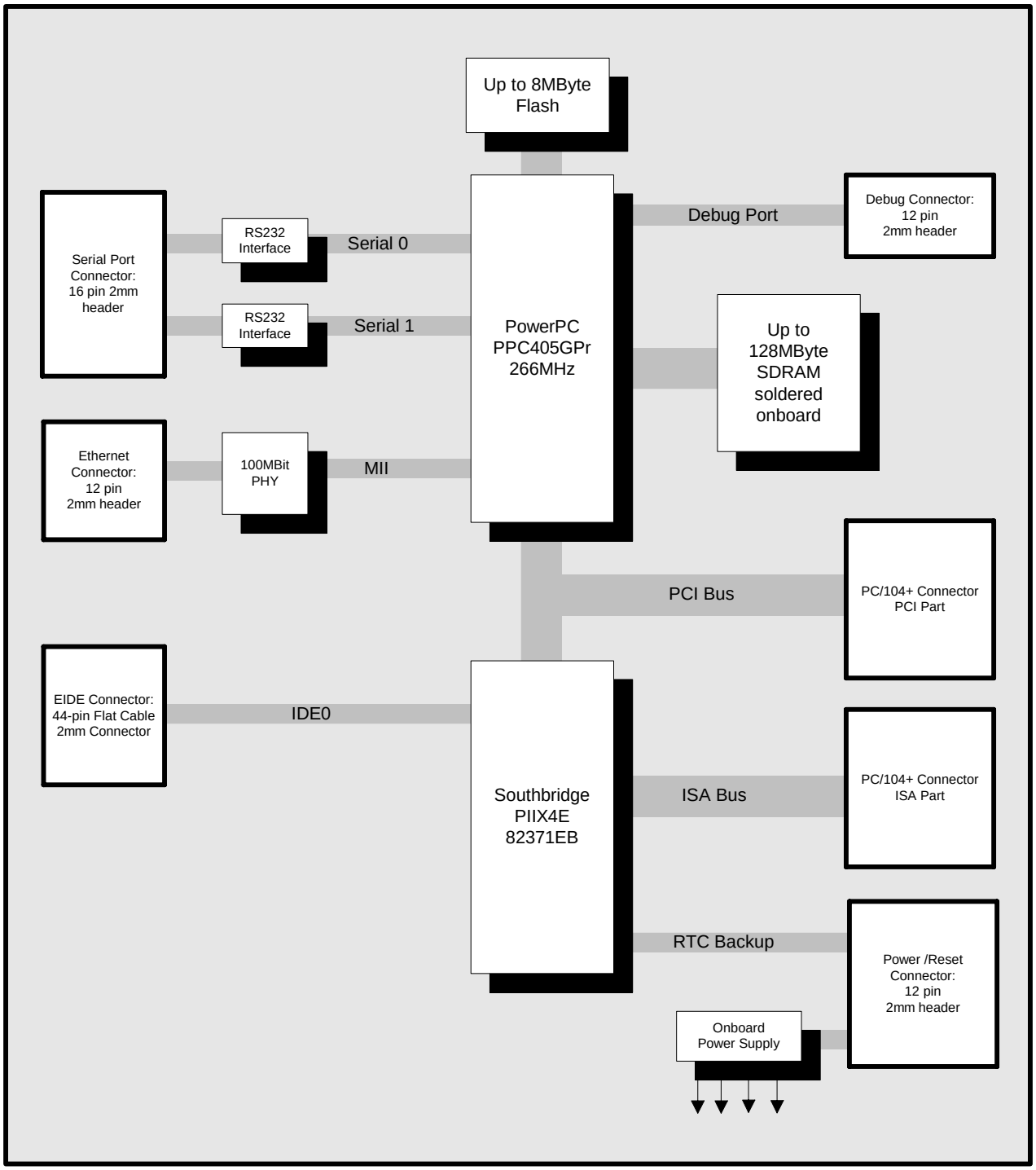


Figure 4.1 MIP405T Block Diagram

4.2 Interrupts

4.2.1 CPU Interrupts

The PPC405 provides 7 Interrupts. They are distributed as follows:

CPU IRQ	IRQ Source	Source
0	INTR# (PIIX4E Interrupt Controller)	EPLD
1	Not used	EPLD
2	SMI# , INIT# and NMI#	EPLD
3	PCI_INTA#	PCI Bus
4	PCI_INTB#	PCI Bus
5	PCI_INTC#	PCI Bus
6	PCI_INTD#	PCI Bus

Table 4.2.1 CPU Interrupts

Note:

- *The 3 Interrupts from the EPLD are routed as follows:*
  - *INTR# is the inverted INTR Signal form the PIIX4E Interrupt Controller*
  - *NMI# is the inverted NMI Signal from the PIIX4E*
  - *SMI# is the PIIX4E SMI# Signal*

4.2.2 ISA Interrupts

The ISA Interrupts are routed as follows:

IRQs	Device	Remarks
IRQ0	Timer	PIIX4E Internal, not available
IRQ1	Free	
IRQ2	2nd IRQ Controller	PIIX4E Internal, not available
IRQ3	Free	
IRQ4	Free	
IRQ5	Free	
IRQ6	Free	
IRQ7	Free	
IRQ8	RTC	PIIX4E Internal, not available
IRQ9	Free	
IRQ10	Free	
IRQ11	Free	
IRQ12	Free	
IRQ13	Free	
IRQ14	Primary IDE	Not Maskable
IRQ15	Secondary IDE	Not Maskable

Table 4.2.2 ISA Interrupts

4.3 Extension registers

The PLD is located at the CS7# on the peripheral local bus. The bit notations are in big Endian Format (That is D0 MSB, D7 LSB)

Offset	Name	Type	Function
5	EXT_REG	Read only	Config Register
4	COM_MODE	Read/Write	Communication Mode Register
3	IRQ_REG	Read only	IRQ Register
2	BOARD_REV	Read only	Board Revision and populated Configuration
1	PLD_VERS	Read only	Versions Number of the PLDs
0	PLD_PART	Read only	Part Number of the PLDs

Table 4.3 Extensions Registers

4.3.1 PLD Partnumber Register

PLD_PART					PLD_CS# + 0x00		Read Only	
	D0	D1	D2	D3	D4	D5	D6	D7
Read	MIPID	PLD Part Number						
Default	1	0	0	0	0	0	0	0

Table 4.3.1 PLD Partnumber register

MIPID: MIP405 product identification bit. 0=MIP405, 1=MIP405T
PLD Part Number: is the Part Index of the PLD.

4.3.2 PLD Version Register

PLD_VERS					PLD_CS# + 0x01		Read Only	
	D0	D1	D2	D3	D4	D5	D6	D7
Read	PLD Version Number							
Default	0	0	0	0	0	0	0	0

Table 4.3.2 PLD Version Register

PLD Version Number is the Version Number of the PLD.

4.3.3 Board Revision and Config Register

BOARD_REV					PLD_CS# + 0x02		Read Only	
	D0	D1	D2	D3	D4	D5	D6	D7
Read	PCB0	PCB1	PCB2	PCB3	CFG0	CFG1	CFG2	CFG3
Default	0	0	0	0	X	X	X	X

Table 4.3.3 Board Revision and Config Register

PCBx: Binary decoded PCB Revision. Add an ASCII ‘A’ to this number to get the PCB Revision. Currently PCB3..0 = 0 => ‘A’.

CFGx: Config Inputs. Used to distinguish different population or other Options.:

CFG0..3	Option
0001	MIP405T-1 (GPr-266 MHz, 64MByte SDRAM, 4 Mbyte FLASH

4.3.4 IRQ Register

IRQ_REG					PLD_CS# + 0x03		Read Only	
	D0	D1	D2	D3	D4	D5	D6	D7
Read	INTR#	Reserved	Reserved	SMI#	INIT#	NMI#	Reserved	Reserved
Default	1	0	0	1	1	1	1	1

Table 4.3.4 IRQ Register

INTR#: Interrupt from PIIX4E. (Low Active) Will be forwarded to the PPC405 on INT0#
SMI#: System Management Interrupt from PIIX4E. (Low Active) Will be forwarded to the PPC405 on INT2#
INIT#: Init Output from PIIX4E. (Low Active) Will be forwarded to the PPC405 on INT2#
NMI#: Non maskable Interrupt from PIIX4E. (Low Active) Will be forwarded to the PPC405 on INT2#

4.3.5 Communication Mode Register

COM_MODE					PLD_CS# + 0x04		Read / Write	
	D0	D1	D2	D3	D4	D5	D6	D7
Read	Reserved	S0	S1	S2	Reserved	ULED	Reserved	IDERST
Write	Reserved	S0	S1	S2	Reserved	ULED	Reserved	IDERST
Default	0	0	0	0	0	0	0	0

Table 4.3.5 Communication Mode Register

SER1ALT: Alternate SER1 Hardware Handshake. If set, the SER1 uses DTR, DSR Handshaking instead of CTS, RTS. If this Bit is set, clear the Bit DCS, and set the bit RDS in the Register CHCR0 of the PPC405.
S[2..0]: Binary encoded value for the UARTSERCLK clock input of the PPC405.

S2	S1	S0	Clock nom.	Clock eff.	Error ppm
0	0	0	7.3728 MHz	7.3977 MHz	3381
0	0	1	11.0592 MHz	11.064 MHz	438
0	1	0	12 MHz	12.002 MHz	167
0	1	1	18.432 MHz	18.435 MHz	144
1	0	0	22.1184 MHz	22.114 MHz	215
1	0	1	24 MHz	23.996 MHz	158
1	1	0	36.864 MHz	36.869 MHz	144
1	1	1	40 MHz	39.992 MHz	196

ULED: If set, the User LED is switched on.

4.3.6 Configuration Switch Register

DIP Switch					PLD_CS# + 0x05		Read Only	
	D0	D1	D2	D3	D4	D5	D6	D7
Read	S1-1	S1-2	S1-3	S1-4	S1-5	S1-6	S1-7	S1-8

Table 4.3.6 Configuration Switch Register

5. Support information

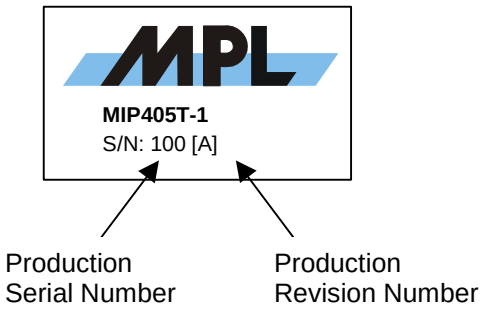
5.1 MPL AG

In case of questions contact MPL AG or your local distributor.

MPL AG homepage: www.mpl.ch
Email address: support@mpl.ch

5.2 Production serial and revision number

To get the actual production revision number of your device, please see the label on the bottom of the MIP405T Board.



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Copyright and revision history

This manual reflects Revision A of the MIP405T.

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Our local distributor: