Addendum

DSP56309UMAD/D
Rev. 1, 11/2002

DSP56309 User's Manual Addendum

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CONTENTS

1 Introduction

This document provides updated information for revision 0 of the *DSP56309 User's Manual (DSP56309UM/D)*. The updates include the following:

- Modified signal definitions
- New Operating Mode Register (OMR) layout and bit definitions
- Updated SCI Receive Register (SRX) description
- Updated OMR and Timer Registers (TLR, TCPR, TCR) programming sheets

2 Modified Signal Definitions

Area to Change	Change Description
Table 2-1, p. 2-3	• Change Ground (GND) to Ground (GND)[5]. • Add Note 5 as follows: **5**. The number of Ground signals listed are for the 144-pin TQFP package. For the 196-ball MAP-BGA package, there are 66 GND connections.
Figure 2-1, p. 2-4	• Change $\overline{\text{HA10}}$ to HA10 • Change $\overline{\text{HRW}}$ to HRW • Change $\overline{\text{AA0}}$–$\overline{\text{AA3}}$ to AA0–AA3 • Change $\overline{\text{TMS}}$ to TMS • Change **Grounds:** to **Grounds[4]:** • At the bottom of the figure, add the following note: **4**. The GND signals are listed for the 144-pin TQFP package. For the 196-ball MAP-BGA package, all grounds except GND_P and GND_{P1} are connected together and referenced as GND. There are 64 GND connections.
Table 2-3, p. 2-7	• Change the note at the end of the table to the following: **Note:** The subsystem GND signals (GND_Q, GND_A, GND_D, GND_C, GND_H, and GND_S) are listed for the 144-pin TQFP package. For the 196-ball MAP-BGA package, all grounds except GND_P and GND_{P1} are connected together inside the package and referenced as GND.
Table 2-8, pp. 2-11 to 2-12	• Change $\overline{\text{BR}}$ signal **State During Reset, Stop, or Wait** to: Reset: Output (deasserted) State during Stop/Wait depends on BRH bit setting: • BRH = 0: Output, deasserted • BRH = 1: Maintains last state (that is, if asserted, remains asserted) • Change $\overline{\text{BB}}$ signal **State During Reset, Stop, or Wait** to Ignored input

Modified Signal Definitions

Area to Change	Change Description
Table 2-11, pp. 2-17 to 2-21	• Change the title of the third column to **State During Reset**[1,2]. • Add the following notes to the end of the table: **Notes:** **1.** In the Stop state, the signal maintains the last state as follows: • If the last state is input, the signal is an ignored input. • If the last state is output, these lines are tri-stated. **2.** The Wait processing state does not affect the signal state. • Change **State During Reset or Stop** for all signals to Ignored input. • Change the signal description for PB14 to: **Port B14**—When the HI08 is configured as GPIO through the HPCR, this signal is individually programmed through the HDDR.
Table 2-12, pp. 2-22 to 2-25	• Change the title for the third column to **State During Reset**[1,2]. • Change **State During Reset** for all signals to Ignored input. • Add notes that state: **Notes:** **1.** In the Stop state, the signal maintains the last state as follows: • If the last state is input, the signal is an ignored input. • If the last state is output, these lines are tri-stated. **2.** The Wait processing state does not affect the signal state. • For all signals, delete the middle paragraph in the signal description. ESSI0 does not support keeper circuits. • For all signals, change PCR0 to PCRC and PRR0 to PRRC.
Table 2-13, pp. 2-26 to 2-28	• Change the title for the third column to **State During Reset**[1,2]. • Change **State During Reset** for all signals to Ignored input. • Add notes that state: **Notes:** **1.** In the Stop state, the signal maintains the last state as follows: • If the last state is input, the signal is an ignored input. • If the last state is output, these lines are tri-stated. **2.** The Wait processing state does not affect the signal state. • For all signals, delete the middle paragraph in the signal description. ESSI1 does not support keeper circuits. • For all signals, change PCR1 to PCRD and PRR1 to PRRD.
Table 2-14, pp. 2-29 to 2-30	• Change the title for the third column to **State During Reset**[1,2]. • Change **State During Reset** for all signals to Ignored input. • Add notes that state: **Notes:** **1.** In the Stop state, the signal maintains the last state as follows: • If the last state is input, the signal is an ignored input. • If the last state is output, these lines are tri-stated. **2.** The Wait processing state does not affect the signal state. • For all signals, delete the middle paragraph in the signal description. The SCI does not support keeper circuits. • For all signals, change PCR to PCRE and PRR to PRRE.
Table 2-15, p. 2-31	• Change the title for the third column to **State During Reset**[1,2]. • Change **State During Reset** for all signals to Ignored input. • Add notes that state: **Notes:** **1.** In the Stop state, the signal maintains the last state as follows: • If the last state is input, the signal is an ignored input. • If the last state is output, these lines are tri-stated. **2.** The Wait processing state does not affect the signal state. • For all signals, delete the middle paragraph in the signal description. The triple timer module does not support keeper circuits.

3 Operating Mode Register (OMR) Layout and Definition

Area to Change	Change Description
Figure 4-3, p. 4-17	Replace with the following:

Stack Control/Status (SCS)								Extended Operating Mode (EOM)								Chip Operating Mode (COM)							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			SEN	WRP	EOV	EUN	XYS	ATE	APD	ABE	BRT	TAS	BE	CDP[1–0]		MS	SD		EBD	MD	MC	MB	MA
Reset:																							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	*	*	*	*

* After reset, these bits reflect the corresponding value of the mode input (that is, MODD, MODC, MODB, or MODA, respectively).

SEN—Stack Extension Enable
WRP—Extended Stack Wrap Flag
EOV—Extended Stack Overflow Flag
EUN—Extended Stack Underflow Flag
XYS—Stack Extension Space Select

ATE—Address Tracing Enable
APD—Address Priority Disable
ABE—Asynch. Bus Arbitration Enable
BRT—Bus Release Timing
TAS—TA Synchronize Select
BE—Burst Mode Enable
CDP1—Core-DMA Priority 1
CDP0—Core-DMA Priority 0

MS—Memory Switch Mode
SD—Stop Delay
EBD—External Bus Disable
MD—Operating Mode D
MC—Operating Mode C
MB—Operating Mode B
MA—Operating Mode A

Reserved bit. Read as zero; write to zero for future compatibility

Figure 4-3. Operating Mode Register (OMR)

4 SCI Receive Register (SRX) Description

Area to Change	Change Description
Section 8.6.4.1, p. 8-20	Change the beginning of the fourth paragraph from “In Synchronous mode” to “In Asynchronous mode”.

5 Updated Programming Sheets

Use the following examples to replace **Figure D-2** and **Figure D-21** in the *DSP56309 User’s Manual*.

Application:_____ Date:_____

_____ Programmer:_____

Sheet 2 of 5

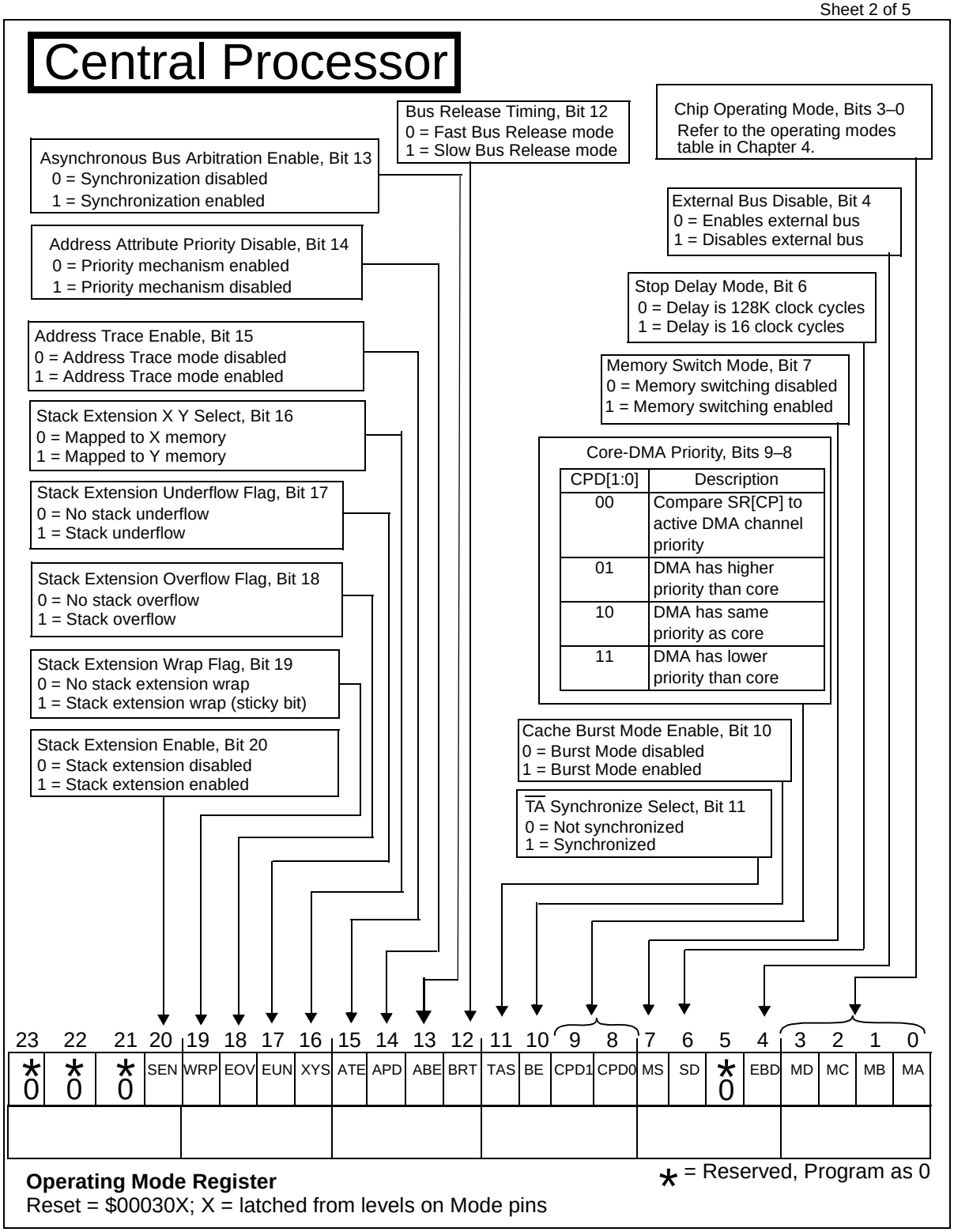

Figure D-2. Operating Mode Register (OMR)

Application:_____ Date:_____

_____ Programmer:_____

Sheet 3 of 3

Timers

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Timer Reload Value																							

Timer Load Register
Reset = $xxxxxx, value indeterminate after reset

TLR0—X:$FFFF8E Write Only
TLR1—X:$FFFF8A Write Only
TLR2—X:$FFFF86 Write Only

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value Compared to Counter Value																							

Timer Compare Register
Reset = $xxxxxx, value indeterminate after reset

TCPR0—X:$FFFF8D Read/Write
TCPR1—X:$FFFF89 Read/Write
TCPR2—X:$FFFF85 Read/Write

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Timer Count Value																							

Timer Count Register
Reset = $000000

TCR0—X:$FFFF8C Read Only
TCR1—X:$FFFF88 Read Only
TCR2—X:$FFFF84 Read Only

Figure D-21. Timer Load, Compare, Count Registers (TLR, TCPR, TCR)

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