ZNEO™ Z16F Series Flash Microcontroller Contest Kit

User Manual

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Safeguards

The following precautions must be observed when working with the devices described in this document.

Caution: Always use a grounding strap to prevent damage resulting from electrostatic discharge (ESD).

Revision History

The following table lists all revisions of this document, reasons for revision, and affected page numbers.

Date	Revision Level	Description	Page #
August 2006	01	Original Issue.	

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Introduction

The ZNEO Z16F Series Flash microcontrollers are based on ZiLOG's advanced ZNEO 16-bit CPU core. The ZNEO Z16F Series MCU family of devices sets a new standard of performance and efficiency with a 24-bit address bus and 16-bit data bus. This contest kit board supports the ZNEO™ microcontroller.

The ZNEO™ Contest Kit allows users to become familiar with the hardware and software tools available with this product. This kit consists of the 128KB version of the ZNEO™ Development board that supports and presents the features of the ZNEO™. The software development tool kit allows users to begin writing application software and contains all supporting documents.

This manual acquaints users with the technical details of the ZNEO™ Contest Kit.

System/Software Requirements

IBM PC (or compatible computer) with the following recommended configurations:

Supported Host System Configuration

- Windows XP Professional, Windows 2000 SP4, Windows 98SE
- PentiumIII/500MHz processor or higher
- 128MB RAM or more
- 100MB hard disk space or more (includes application and documentation)
- Super VGA video adapter
- CD-ROM for installation
- USB high-speed poort (when using USB Smart Cable)

- RS-232 communication port with hardware flow control
- Internet browser (Internet Explorer or Netscape)

Installation

This section provides instructions for setting up your ZNEO Contest Kit.

Configuring the 9VDC Universal Power Supply

The universal power supply kit features several different plug adapters in one box and the power supply itself in another. The power supply ships with a slide-out plate that must be removed to insert the location-specific plug adapter.

1. Remove the slide-out plate.
2. Select the AC plug adapter appropriate for your locale and insert it into the slot that remains after removing the slide-out plate.
3. Slide the new plug adapter into the slot until it snaps into place.

For convenience, you can leave the adapter slot cover in place and plug in a standard computer equipment AC power cord (purchased separately) between the AC cord receptacle on the end of the power supply and an electrical outlet.

Setting Up the Contest Kit Board

Setting up the ZNEO contest kit board involves setting its jumpers and using the USB Smart Cable to connect the board to a high-speed or full-speed USB port on your ZiLOG Developer Studio II (ZDS II) host system.

Caution: Always use a grounding strap to prevent damage resulting from electrostatic discharge (ESD).

1. For initial setup, make sure jumper J10, DIS IRDA, is OUT. See Table 7, "Configuration Headers and Jumpers" on page 29, for detailed jumper descriptions.
2. Your development kit is preprogrammed with code for demonstration purposes and is a simple way to verify that the board is working properly.

   To run the preprogrammed Demo software, connect power and press reset switch SW4. The 7x5 LED matrixes D1 through D4 will display " WEL".

   Connect the contest kit board console port to a development PC serial port (57600 8-N-1) and use the Hyperterminal application to do more testing.

   Press reset switch SW4. The hyperterminal will display the following text:

   ```
   T       Read Current Temperature
   W       Write DS1722
   R       Read DS1722
   [ESC]   EXIT

   DS1722>
   ```

   Enter "T" to read current temperature. The 7x5 LED matrixes D1 to D4 will scroll/display the current room temperature.
3. After running the Demo software, disconnect power from the development board.
4. Install the included USB Smart Cable. If you have previously installed a USB Smart Cable as part of another ZiLOG Development Kit, the drivers are already present on your system. Plug the USB Smart Cable supplied with your ZNEO development kit into an available USB port. The USB Smart Cable drivers will automatically install.

If you have never installed the USB Smart Cable on your system, do so as described below for the appropriate operating system.

Consult the readme.txt file included with your ZNEO installation for additional information.

Caution: Do not connect the power supply to the development board before connecting a USB Smart Cable to both the host PC and development board.

Installing the USB Smart Cable with Windows XP

1. Connect the USB Smart Cable to the host PC for the first time.

   The Found New Hardware Wizard should activate automatically.

2. In the Wizard, select **Install from a list or specific location (Advanced);** then click **Next**.

Note: If the Windows Logo testing dialog appears, select **Continue Anyway**.

3. Select **Search for the best driver in these locations** and **Include this location in search.**
4. Browse to the driver directory, one of the following:

```
<ZiLOG Developer Studio II Installation Directory>
\device drivers\USB
```

```
<ZiLOG Developer Studio II Installation CD>
\Device Drivers\USB
```

5. Click **Next**, and then click **Next** again after the appropriate driver is found.
6. Click **Finish** to complete the installation.

Installing the USB Smart Cable with Windows 2000

1. Connect the USB Smart Cable to the host PC for the first time.

The Found New Hardware Wizard should activate automatically.

2. In the Wizard, click **Next**.
3. Select **Search for a suitable driver for my device (Recommended);** then click **Next.**
4. Select **Specify a location**; then click **Next.**
5. Browse to the driver directory, one of the following:

```
<ZiLOG Developer Studio II Installation Directory>
device drivers\USB
```

```
<ZiLOG Developer Studio II Installation CD>
\Device Drivers\USB
```

6. Click **OK**, and then click **Next** after the appropriate driver is found.
7. Click **Finish** to complete the installation.

Installing the USB Smart Cable with Windows 98SE

1. Connect the USB Smart Cable to the host PC for the first time.

   The Found New Hardware Wizard should activate automatically.

2. In the Wizard, click **Next**.
3. Select **Search for the best driver for your device (Recommended);** then click **Next**
4. Select **Specify a location**; then browse to the driver directory, one of the following:

```
<ZiLOG Developer Studio II Installation Directory>
device drivers\USB
```

```
<ZiLOG Developer Studio II Installation CD>
\Device Drivers\USB
```

5. Click **Next**, and then click **Next** again after the appropriate driver is found.
6. Click **Finish** to complete the installation.

Connecting the USB Smart Cable to the Target Board

Attach one end of the six-conductor ribbon cable (included) to the USB Smart Cable six-pin DBG connector (P4). Attach the free end of the ribbon cable to the DBG connector on the target board. Ensure that pin 1 on the ribbon cable (indicated by the dark stripe) is aligned with pin 1 on the target connector (see the board labeling at connector P4 to determine pin 1).

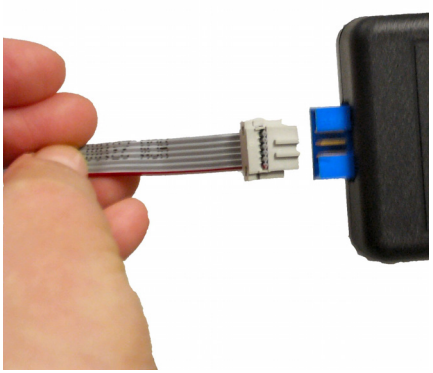


Figure 1. Connecting the Six-Conductor Ribbon Cable to the USB Smart Cable

Applying Power to the Contest Kit Board

1. After installing the USB Smart Cable, connect the power supply to the contest kit board at connector P3, then to an electrical outlet.
2. The Green 3.3VDC LED D6 illuminates, indicating that power is being supplied to the board.

Installing the ZDSII–ZNEO™ Series Software

Perform the following steps to install the software tools:

1. Insert the ZDS II CD into your computer's CD-ROM drive. DemoShield launches automatically. If it does not automatically launch, go to the root of the CD-ROM and double-click the file `launch.exe`.
2. *DemoShield* provides several installation choices. Select "Install ZiLOG Developer Studio" to install now. You can install other software and accompanying documentation later.
3. Follow the instructions on the screen to complete the installation.

Getting Started Using ZDS II

To begin developing code for the ZNEO Contest Kit, download the application sample code from http://www.zilog.com/library. Click the link for the ZNEO Contest Kit Sample Code, Version 1.0.0 and save it to your hard disk when prompted.

After downloading, double-click the `Install_ZNEO_Contest_Kit_Sample_Code_Library_1.0.0.exe` file to install the sample code.

Navigate to `C:\Program Files\ZiLOG\Applications_Library\ZNEO Contest Kit Sample Code Library 1.0.0\Peripheral_Sample_Code\source` to view the samples provided.

Perform the following procedure to open and use the `ZNEO_Contest_Kit_SampleCode.zdsproj` sample project. This project is designed to compile and download into ZNEO internal Flash memory.

1. Connect the contest kit board console port to a serial port on the development PC. Start the Hyperterminal application (57600 8-N-1).
2. Connect and apply power to the contest kit board as described in "Setting Up the Contest Kit Board" on pages 3 through 7 Connect the console port to the .

Caution: Do not apply power to the development board unless the USB Smart Cable is connected both to the host PC and to the development board's DBG port P4.

3. Run the ZiLOG Developer Studio II software. By default, the ZiLOG Developer Studio II program is located in the Start menu under:

   `Programs → ZiLOG ZDSII ZNEO <version_number> → ZDSII ZNEO <version_number>`

4. Select Open Project from the File menu. The Open Project dialog box appears.
5. Browse to the `source` folder for the `ZNEO_Contest_Kit_SampleCode.zdsproj` file, located by default in:

   ```
   C:\Program Files\ZiLOG\Applications_Library
   \ZNEO Contest Kit Sample Code Library 1.0.0
   \Peripheral_Sample_Code\source
   ```

6. Select the `ZNEO_Contest_Kit_SampleCode.zdsproj` file and click Open. The initial ZiLOG Developer Studio II program screen opens (see Figure 2 on page 10).

   If you want to view the project source files, double-click the Project Files folder on left side of the IDE interface. Double-click an individual file to open that file in the ZDS II file editor.

Note: The following figures are for reference only. Your results may very slightly due to configuration differences or later software revisions.

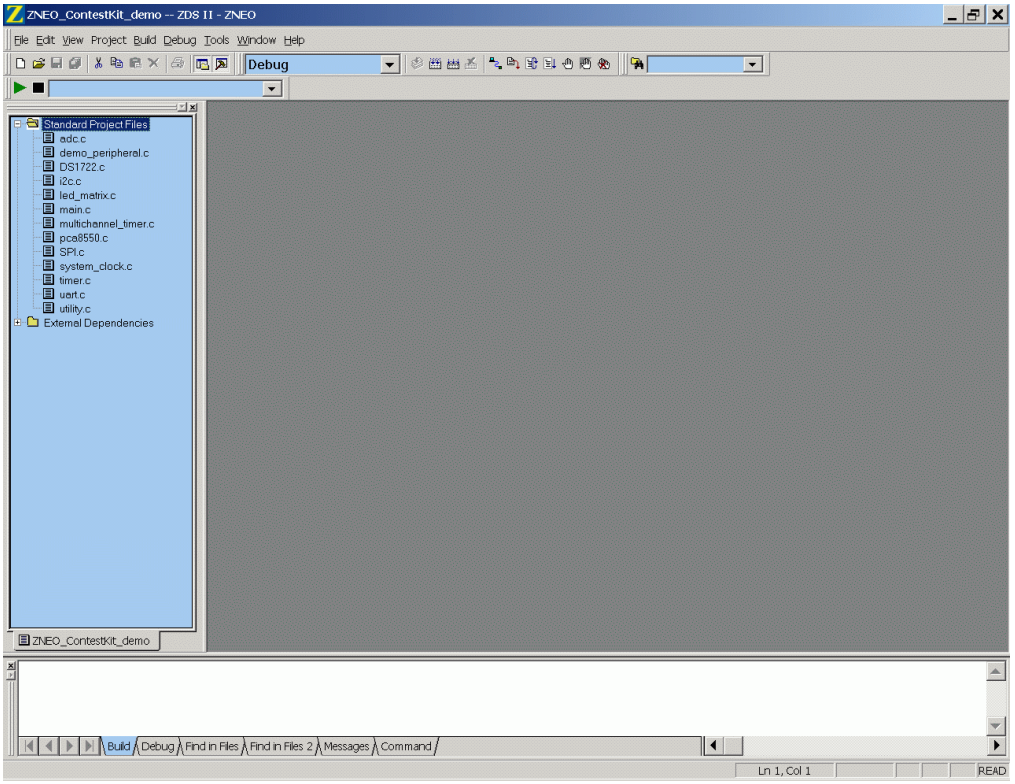


Figure 2. ZiLOG Developer Studio II Opening Screen

7. Click the Rebuild All icon to build the project. Wait for the build to complete as indicated by the "Build Completed" confirmation in the status window at the bottom of the screen. See Figure 3.

Rebuild All Icon

8. You will see an IDE message about programming option bits. Click the Yes button to continue.

Reset Icon

9. Click the Reset icon to connect and download the code to the development board.
10. Click Go to start the program. The screen changes as illustrated in Figure 4 on page 13.


Go Icon

The hyperterminal (57600 8-N-1) will show the following messages:

```
***** ZNEO Contest Kit Sample Code Demo Help *****

A       ADC
I       I2C
S       ESPI
U       UART
M       Multichannel Timer
T       Timer
L       LED
H       Help
Select any one of the above options to view the
corresponding peripheral demo.


ZNEO>>
```

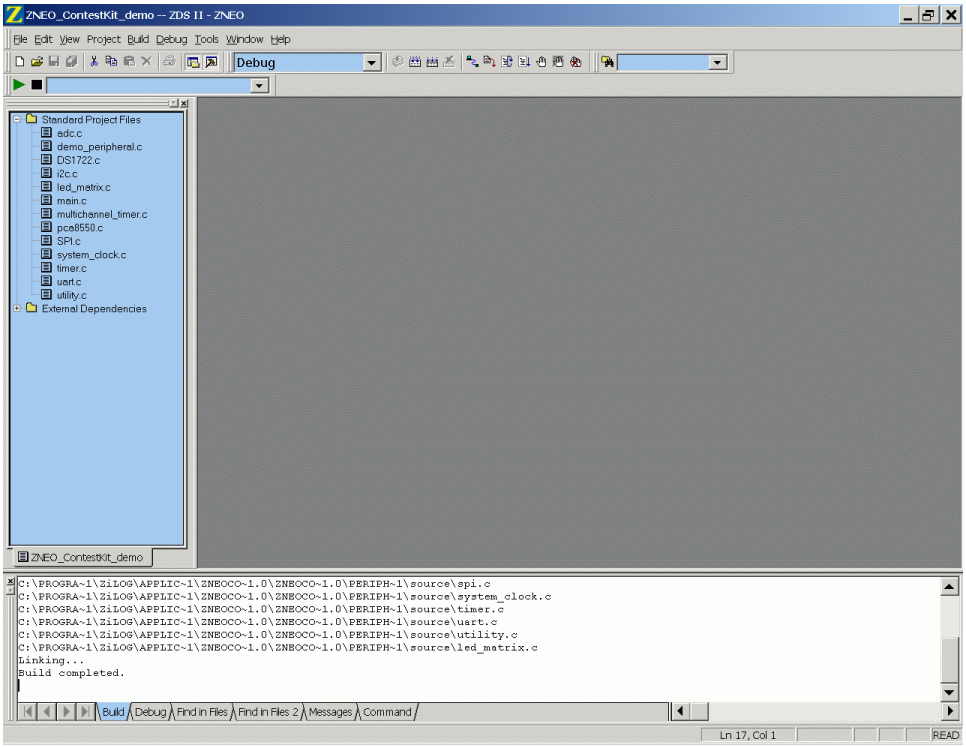


Figure 3. ZiLOG Developer Studio II Build Completed Screen

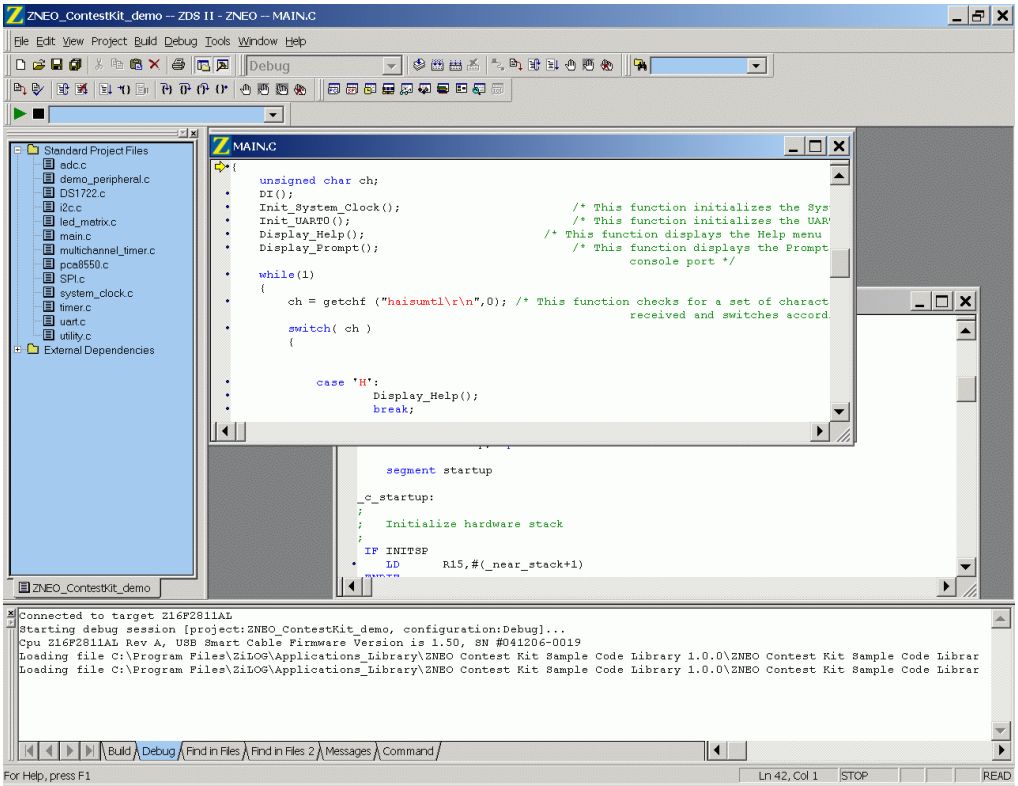


Figure 4. ZiLOG Developer Studio II Screen After Pressing GO

For more information about using ZiLOG Developer Studio II and building projects for your ZNEO® development kit, refer to the *ZiLOG Developer Studio II–ZNEO™ Series User Manual (UM0171)*.

Troubleshooting Tips

If you experience trouble running the demo program with the ZNEO development board, check the following before contacting ZiLOG Technical Support for assistance:

- Verify that you are using ZDS II version 4.10.0 or later.
- Make sure you are using the unmodified sample project code as described in “Getting Started Using ZDS II” on page 8.
- Verify that you have properly connected the USB Smart Cable to the host PC and the development board as described in “Setting Up the Contest Kit Board” on page 3. Ensure that pin 1 of the cable is properly aligned with DBG connector pin 1 of the development board.
- Apply power to the development board. The green 3.3VDC LED- should be on. If it is not illuminated, verify that power is properly connected to the board as described in "Configuring the 9VDC Universal Power Supply" on page 3.
- In ZDS II, select the Project > Settings menu item. In the Debugger tab of the Project Settings window, look in the Target section and verify that either the Z16F2800100ZCOG or Z8F2811AL checkbox is checked. Verify that the drop-down menu in the Debug Tool section is set to USBSmartCable.

  Click the Setup button in the Debug Tool box and verify that the serial number for the USB Smart Cable interface is present. If the serial number is missing, reinstall the USB Smart Cable driver software.
- In ZDS II, click the Rebuild All  button. Verify that the project rebuilds with no errors.
- Verify that the development board is not currently running any code -- no LEDs should be blinking.

- In ZDS II, click the IDE Reset  button. ZDS II will connect to the development board and download code to it.

If you perform these steps and cannot get the demo code to run, contact ZiLOG Technical Support at www.ZiLOG.com.

ZNEO™ Contest Kit Board

Introduction

ZNEO™ Contest Kit Board (128KB version) is an evaluation and prototyping board for the ZNEO™ Z16F Series of microcontrollers. The board provides customers with a tool to evaluate features of ZNEO™ family, and to start developing an application before building the hardware.

Features

- ZNEO™ MCU
- LED array with four 7 x 5 LED matrices
- Serial Communications Devices
  - I^2C configuration IC for Expansion Module
  - SPI Interface with temperature sensor
- IrDA transceiver
- Power and communication interfaces
  - 9VDC power supply
  - Two RS-232 connectors
  - One RS-485 connector with two ports
- Expansion Module interface
- Embedded modem socket with U.S. phone line interface (modem is not included in the kit)
- Three pushbuttons

Block Diagram

The board consists of six major blocks:

1. ZNEO™ MCU
2. Serial communication devices (SPI and I^2C)
3. Power and communication interfaces
4. LED array
5. Expansion Module interfaces
6. IrDA transceiver
7. ZiLOG Debug Interface (DBG)

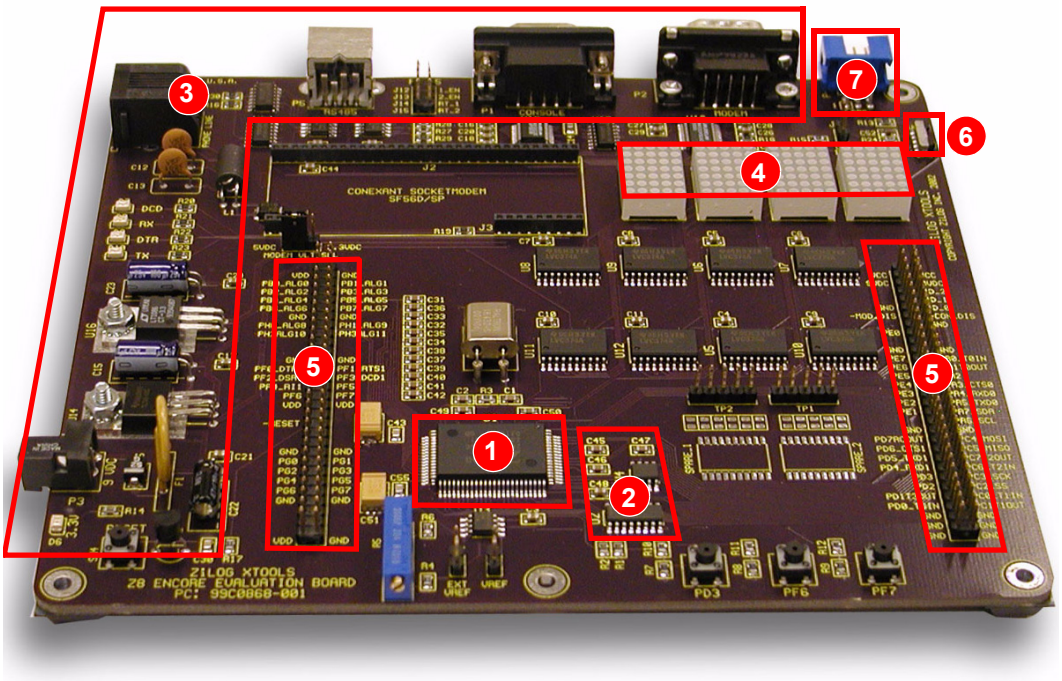


Figure 10. Major ZNEO™ Contest Kit Board Blocks

Figure 11 illustrates the ZNEO™ Contest Kit Board block diagram.

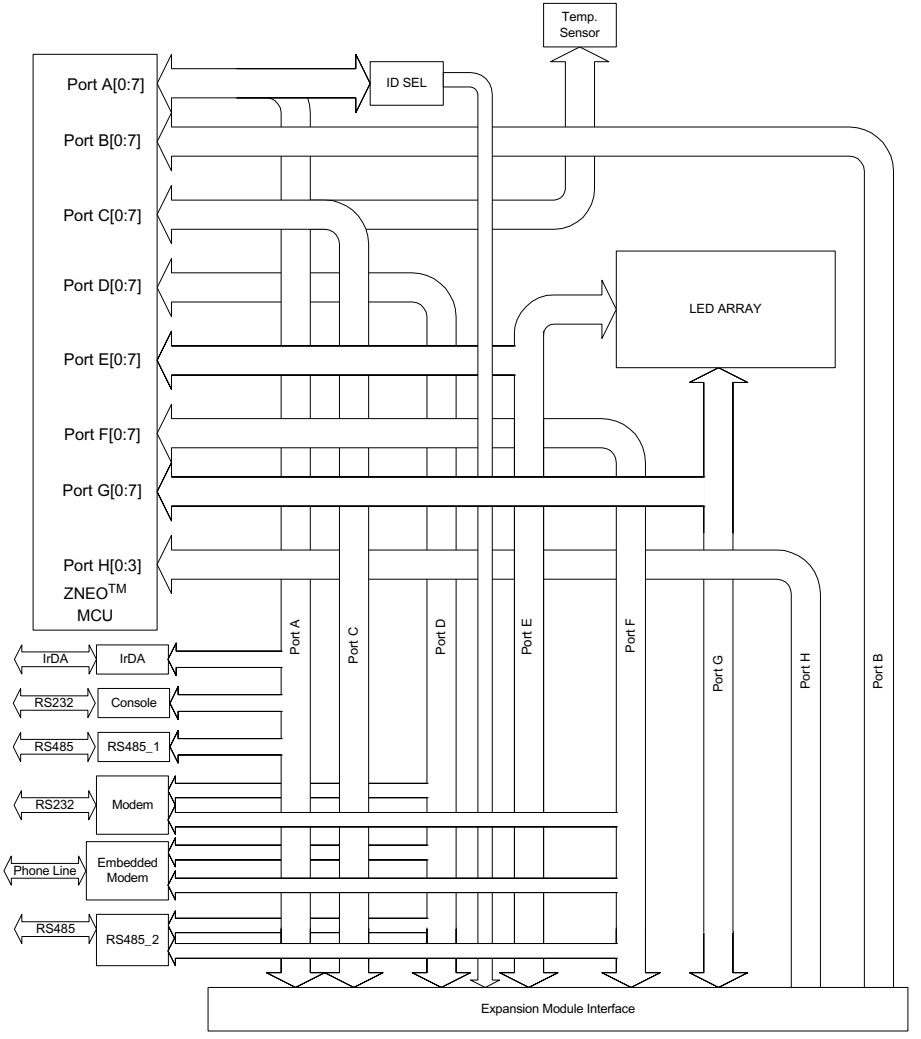


Figure 11. ZNEO™ Contest Kit Board Block Diagram

MCU

The ZNEO Z16F Series Flash microcontrollers are based on ZiLOG's advanced ZNEO 16-bit CPU core. The ZNEO Z16F Series MCU family of devices sets a new standard of performance and efficiency with a 24-bit address bus and 16-bit data bus.

The ZNEO Z16F Series External Interface allows seamless connection to external memory and peripherals. A 24-bit address bus and selectable 8-bit or 16-bit data bus allows parallel access up to 16MB.

The Contest Kit Board contains circuitry to support and presents all the features of the ZNEO™. The main features of the ZNeo™ are:

- 20MHz ZiLOG ZNeo CPU Core
- 32-128KB internal Flash program memory with 16-bit access and in-circuit programming capability
- Up to 4KB internal RAM with 16-bit access
- External Interface allows seamless connection to external data memory and peripherals with:
  - 6 chip selects with programmable Wait states
  - 24-bit address bus supports up to 16MB
  - Selectable 8-bit or 16-bit data bus widths
  - Programmable Chip Select signal polarity
  - ISA-compatible mode
- Up to twelve channels 10-bit analog-to-digital converter (ADC)
- Operational Amplifier
- Analog Comparator
- 4-channel DMA controller supports internal or external DMA requests
- Two full-duplex 9-bit UARTS with support for LIN and IrDA

- Internal Precision Oscillator
- I2C master-slave controller
- Enhanced Serial Peripheral Interface (ESPI) controller
- 12-bit PWM module with three complementary pairs or six independent PWM outputs with dead-band generation and fault trip input
- Three standard 16-bit timers with capture, compare, and PWM capability
- Watch-Dog Timer (WDT) with internal RC oscillator
- Up to 76 I/O pins
- Up to 24 interrupts with programmable priority
- Single-pin on-chip debugger
- Power-On Reset (POR)
- Voltage Brown-Out Protection (VBO)
- 2.7–3.6V operating voltage with 5V-tolerant inputs
- 0°C to +70°C standard temperature, -40°C to +105°C extended temperature, and -40°C to +125°C automotive operating ranges

For further information on the ZNEO™ family of devices, consult the product specification, P/N PS0220.

LED Array

The LED array display user information. There are four 7x5 LED matrixes. To light up an LED dot the appropriate Anode bit must be 1, and the correlated Cathode must be 0. All Anodes are addressed by Port G, and Cathodes are addressed by Port E. Every LED Matrix is addressed by separate pair of registers. Each of the register pairs is addressed by a bit of Port E or Port G. Tables 1 through 4 describe how to address each Anode and Cathode of D1 through D4.

Table 1. LED Anode Assignments

Function \ Port G Bit #	6	5	4	3	2	1	0
Anode Row 0							X
Anode Row 1						X	
Anode Row 2					X		
Anode Row 3				X			
Anode Row 4			X				
Anode Row 5		X					
Anode Row 6	X						
Note: Row 0 = Topmost Row							

Table 2. LED Cathode/Modem/Trigger

Function \ Port E Bit #	4	3	2	1	0
Cathode Column 0					X
Cathode Column 1				X	
Cathode Column 2			X		
Cathode Column 3		X			
Cathode Column 4	X				
Note: Column 0 = Leftmost Column					

Table 3. LED Addressing

Function \ Port, Bit #	PE[5]	PE[6]	PE[7]	PG[7]
D3	X			
D4		X		
D1			X	
D2				X

Serial Communications Devices

I²C Interface

The ZNeo™ is compatible with I²C protocol (in this case the PCA8550). The I²C controller consists of two bidirectional bus lines, a serial data (SDA) line and a serial clock (SCL) line.

The I²C Controller operates in Master mode to transmit and receive data.

Having a PCA8550 on board enables configuration of the Expansion Module. The PCA8550 is a 4-bit multiplexer that selects four bits of data either from a non-volatile register or from the input pins. In this case four input pins are left unconnected and only a non-volatile register is selected as a source of data. Only three bits are used. Currently this chip is not used by the software provided with the board, so a user is free to use it to their advantage. The configuration register (Table 4) is available at the address 0x9C for Write operation and 0x9D for Read operation on the PCA8550 device. Please refer to the PCA8550 Product Specification (www.semiconductors.philips.com) for more details on programming this device.

Table 4. I²C Address for Configuration Register on the PCA8550 (U2)

Device \ Bit #	7	6	5	4	3	2	1	0
Value	1	0	0	1	1	1	0	R/W

SPI Interface

The serial peripheral interface (SPI) allows the ZNeo™ to exchange data between other peripheral devices such as EEPROMs, A/D converters and ISDN devices. The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface.

To work with SPI interface for temperature/sensor types of applications, DS1722 Digital Thermometer was incorporated into the board. The serial mode is SPI. Refer to the DS1722 Product Specification for more details on programming the device.

IrDA Transceiver

The ZNeo™ contains two fully-functional, high-performance UARTs with Infrared Encoder/Decoders (Endec). The Infrared Endec is integrated with an on-chip UART to allow easy communication between the ZNeo™ and IrDA transceivers. Infrared communication provides secure, reliable, low-cost, point-to-point communication between PCs, PDAs, cell phones, printers and other infrared enabled devices.

Power and Communication Interfaces

- A 9VDC power supply powers the board
- Two RS-232 DB9 connectors and an RS-485 connector with two ports
- A ZiLOG IrDA transceiver is integrated onto the ZNEO™ contest kit board

USB Smart Cable

The ZNEO™ USB Smart Cable enables communication with the Host computer.

Expansion Module Interface

The Expansion Module Interface allows addition of any plug-in modules. The Expansion Module Interface brings out the signals from the ZNEO™ device for debug and testing.

Two 60-pin male headers, J6 and J8, implement the Expansion Module Interface. Tables 5 and 6 list the signals and their direction, where applicable.

Table 5. Header J6

Pin #	Signal Name	Function	Direction	Comments
1		VCC		
2		VCC		
3		9VDC		
4		9VDC		
5	SCL	I^2C Clock	OUT	
6	ID2	contest Kit Board ID	OUT	
7	SDA	I^2C Data	IN/OUT	
8	ID1	contest Kit Board ID	OUT	
9		GND		
10	ID0	contest Kit Board ID	OUT	
11	-MOD_DIS	Modem Disable	OUT	If a shunt is installed the Modem Function on the contest kit board is disabled
12	-CON_DIS	Console Disable	OUT	If a shunt is installed the Console Function on the contest kit board is disabled
13	-MWAIT		IN	Reserved (see note)
14	GND			
15	PE0	Port E, Bit 0	IN/OUT	
16				
17	-CS3			Reserved (see note)
18				
19	GND			

Note: Do not use pins marked Reserved when designing Expansion Modules.
All of the signals are driven directly by the MCU.

Table 5. Header J6 (Continued)

Pin #	Signal Name	Function	Direction	Comments
20	GND			
21	PE7	Port E, bit 7	IN/OUT	
22	PA0	Port A, bit 0	IN/OUT	T0IN
23	PE6	Port E, bit 6	IN/OUT	
24	PA1	Port A, bit1	IN/OUT	T0OUT
25	PE5	Port E, bit 5	IN/OUT	
26	PA2	Port A, bit 2	IN/OUT	
27	PE4	Port E, bit 4	IN/OUT	
28	PA3	Port A, bit 3	IN/OUT	CTS0
29	PE3	Port E, bit 3	IN/OUT	
30	PA4	Port A, bit 4	IN/OUT	RXD0
31	PE2	Port E, bit 2	IN/OUT	
32	PA5	Port A, bit 5	IN/OUT	TXD0
33	PE1	Port E, bit 1	IN/OUT	
34	PA7	Port A, bit 7	IN/OUT	SDA
35	RESERVED			
36	PA6	Port A, bit 6	IN/OUT	SCL
37		GND		
38		GND		
39	PD7	Port D, bit 7	IN/OUT	RCOUT
40	PC4	Port C, bit 4	IN/OUT	MOSI
41	PD6	Port D, bit 6	IN/OUT	CTS1
42	PC3	Port C, bit 3	IN/OUT	MISO
43	PD5	Port D, bit 5	IN/OUT	TXD1
44	PC7	Port C, bit 7	IN/OUT	T2OUT
45	PD4	Port D, bit 4	IN/OUT	RXD1

Note: Do not use pins marked Reserved when designing Expansion Modules.
All of the signals are driven directly by the MCU.

Table 5. Header J6 (Continued)

Pin #	Signal Name	Function	Direction	Comments
46	PC6	Port C, bit 6	IN/OUT	T2IN
47	PD3	Port D, bit 3	IN/OUT	
48	PC3	Port C, bit 3	IN/OUT	SCK
49	PD2	Port D, bit 2	IN/OUT	
50	PC2	Port C, bit 2	IN/OUT	SS
51	PD1	Port D, bit 1	IN/OUT	T3OUT
52	PC0	Port C, bit 0	IN/OUT	T1IN
53	PD0	Port D, bit 0	IN/OUT	T3IN
54	PC1	Port C, bit 1	IN/OUT	T1OUT
55		GND		
56		GND		
57		GND		
58		GND		
59		GND		
60		GND		

Note: Do not use pins marked Reserved when designing Expansion Modules.
All of the signals are driven directly by the MCU.

Table 6. Header J8

Pin #	Signal Name	Function	Direction	Comments
1		VDD		
2		GND		
3	PB0	Port B, bit 0	IN	ALG0 Analog input
4	PB1	Port B, bit 1	IN	ALG1 Analog input
5	PB2	Port B, bit 2	IN	ALG2 Analog input

Note: Do not use pins marked Reserved when designing Expansion Modules.
All of the signals are driven directly by the MCU.

Table 6. Header J8 (Continued)

Pin #	Signal Name	Function	Direction	Comments
6	PB3	Port B, bit 3	IN	ALG3 Analog input
7	PB4	Port B, bit 4	IN	ALG4 Analog input
8	PB5	Port B, bit 5	IN	ALG5 Analog input
9	PB6	Port B, bit 6	IN	ALG6 Analog input
10	PB7	Port B, bit 7	IN	ALG7 Analog input
11		GND		
12		GND		
13	PH0	Port H, bit 0	IN	ALG8 Analog input
14	PH1	Port H, bit 1	IN	ALG9 Analog input
15	PH2	Port H, bit 2	IN	ALG10 Analog input
16	PH3	Port H, bit 3	IN	ALG11 Analog input
17				Reserved (see note)
18				Reserved (see note)
19				Reserved (see note)
20				Reserved (see note)
21		GND		
22		GND		
23	PF0	Port F, bit 0	IN/OUT	DTR1
24	PF1	Port F, bit 1	IN/OUT	RTS1
25	PF2	Port F, bit 2	IN/OUT	DSR1
26	PF3	Port F, bit 3	IN/OUT	DCD1
27	PF4	Port F, bit 4	IN/OUT	RI1
28	PF5	Port F, bit 5	IN/OUT	
29	PF6	Port F, bit 6	IN/OUT	
30	PF7	Port F, bit 7	IN/OUT	
31		VDD		

Note: Do not use pins marked Reserved when designing Expansion Modules. All of the signals are driven directly by the MCU.

Table 6. Header J8 (Continued)

Pin #	Signal Name	Function	Direction	Comments
32		VDD		
33	-RD	Read		Reserved (see note)
34	-WR	Write		Reserved (see note)
35	-RESET	Pushbutton reset	OUT	
36	INSTRD			Reserved (see note)
37	-BUSACK			Reserved (see note)
38	-BUSREQ			Reserved (see note)
39	-NMI			Reserved (see note)
40	PHI			Reserved (see note)
41		GND		
42		GND		
43	PG0	Port G, bit 0	IN/OUT	
44	PG1	Port G, bit 1	IN/OUT	
45	PG2	Port G, bit 2	IN/OUT	
46	PG3	Port G, bit 3	IN/OUT	
47	PG4	Port G, bit 4	IN/OUT	
48	PG5	Port G, bit 5	IN/OUT	
49	PG6	Port G, bit 6	IN/OUT	
50	PG7	Port G, bit 7	IN/OUT	
51		GND		
52		GND		
53	-CS0			Reserved (see note)
54	-CS1			Reserved (see note)
55	-CS2			Reserved (see note)
56	-CSx			Reserved (see note)

Note: Do not use pins marked Reserved when designing Expansion Modules. All of the signals are driven directly by the MCU.

Table 6. Header J8 (Continued)

Pin #	Signal Name	Function	Direction	Comments
57	-MEMRQ			Reserved (see note)
58	-IORQ			Reserved (see note)
59		VDD		
60		GND		
Note: Do not use pins marked Reserved when designing Expansion Modules. All of the signals are driven directly by the MCU.				

Configuration Headers/Jumpers

Configuration headers/jumpers help to configure the board. Table 7 provides the function of each header, and related headers, registers or devices.

Note: The default settings for all jumpers is OUT.

Table 7. Configuration Headers and Jumpers

Header	Function	Related Headers, Registers or Devices
J1	RJ11	
J2	Modem connector	Header 32
J3	Modem connector	Header 9
J4	Modem connector	Header 2
J6.12 (-CON_DIS), J6.14 (GND)	Console Enable/Disable	J2
J6.11 (-MOD_DIS), J6.9 (GND)	Modem Enable/Disable	
J7	External Vref	Internal Vref Control
J8	Expansion Module Header	
J9	Vref test point	R5
J10	IrDA Enable/Disable	J6.12 (-CON_DIS), J6.14, (GND)

Table 7. Configuration Headers and Jumpers

Header	Function	Related Headers, Registers or Devices
J11	SocketModem Power (3VDC/5VDC)	
J12	RS-485_1_EN	
J13	RS-485_2_EN	
J14	RT_1	
J15	RT_2	

Tables 8 through 13 provide jumper information concerning the shunt status, functions and devices affected of selected jumpers.

Table 8. J6.9–J6.11 -Modem Enable/Disable

Shunt Status	Function	Device Affected
IN	Modem connector (P2) is disabled	UART1 cannot communicate through P2. Ports D and F can be assigned to functions other than UART1.
OUT	Modem connector (P2) is enabled	If the embedded SocketModem is not in the socket, UART1 communicates through P2.

Table 9. J6.12–J6.14 -Console Enable/Disable

Shunt Status	Function	Device Affected
IN	Console connector (P1) is disabled	If J6.12–14 is IN and J10 is IN, Port A (3-5) is assigned to IrDA; if J10 is OUT Port A (3-5) is assigned to UART0.
OUT	Console connector (P1) is enabled	None

Table 10. J7 External Vref

Shunt Status	Function	Device or Register Affected
IN	External Vref is used for ADC	Internal Vref is disabled.
OUT	Internal Vref is used for ADC	Internal Vref is enabled.

Table 11. J9 Vref

	Function	Device or Register Affected
J9-1	Test point to external Vref	Vref
J9-2	GND	None

Table 12. J10 IrDA Enable/Disable

Shunt Status	Function	Device Affected
IN	IrDA enabled	Only the IrDA interface is operational.
OUT	IrDA disabled	UART0 communicates through RS-232. If J6 12-14 is IN Port A (3-5) can be assigned to other funtions (console connector P1 is disabled. If J6 12-14 is OUT console connector P1 is enabled (Port A (3-5) is assigned to UART0).

Note: If the IrDA board is installed the Console port is disabled.

Table 13. J11 SocketModem Power (3VDC/5VDC)

Shunt Position	Function	Device Affected
IN (pins 1-2)	5.0VDC is provided to power SocketModem	SocketModem
OUT (pins 2-3)	3.3VDC is provided to power SocketModem	SocketModem

Table 14. J12–RS-485_1_Enable First Interface

Shunt Position	Function	Device Affected
IN	RS-485 disabled	none
OUT	Enables RS-485 first interface	Console and IrDA

Table 15. J13–RS-485_1_Enable Second Interface

Shunt Position	Function	Device Affected
IN	RS-485 disabled	none
OUT	Enables RS-485 second interface	SocketModem

Table 16. J14–RT_1,Termination Resistors Enable, RS-485 First Interface

Shunt Position	Function	Device Affected
IN	First RS-485 interface termination resistors disabled	none
OUT	Enables first RS-485 interface termination resistors	none

Table 17. J15–RT_2,Termination Resistors Enable, RS-485 Second Interface

Shunt Position	Function	Device Affected
IN	Second RS-485 interface termination resistors disabled	none
OUT	Enables second RS-485 interface termination resistors	none

Embedded Modem

Figure 12 identifies the embedded modem location.

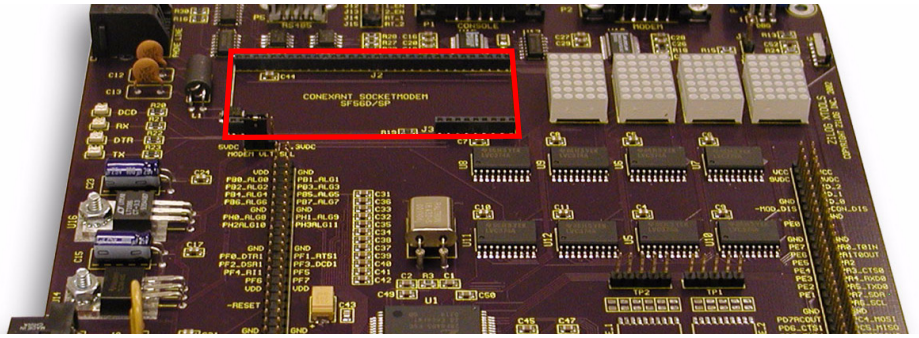


Figure 12. Embedded Modem Placement

The contest kit board provides for an embedded modem, the SF56D/SP SocketModem. The SocketModem is not part of the kit. Table 18 lists ordering information for the modem. The interface communicates with the modem serially. LEDs D7-D10 provide information about the status of the modem's interface lines. The phone line connection is for the U.S. only. To connect to a modem outside of the U.S., modifications must be made to the board. The necessary data is found in the SocketModem Data Sheet on www.zilog.com.

Table 18. SocketModem Ordering Information

Sales Order Number	Part Number	Configuration
SC56H1	SC43-E310-001	V.90/56 kbps, serial interface, +5V operation
SC56H1_L	SC43-E320-001	V.90/56 kbps, serial interface, +3.3V operation
SC336H1	SC34-E310-001	V.34/33.6 kbps, serial interface, +5V operation
SC336H1_L	SC34-E310-001	V.34/33.6 kbps, serial interface, +5V operation
SC144H1	SC14-E310-001	V.32/14.4 kbps, serial interface, +5V operation
SC144H1_L	SC14-E310-001	V.32/14.4 kbps, serial interface, +5V operation

Pushbuttons

The ZNEO™ contest kit board contains three user-configurable pushbuttons (see Figure 13).

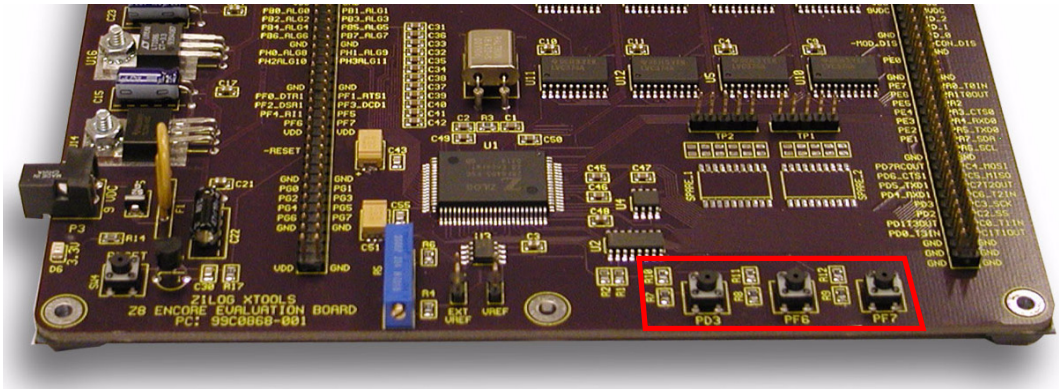
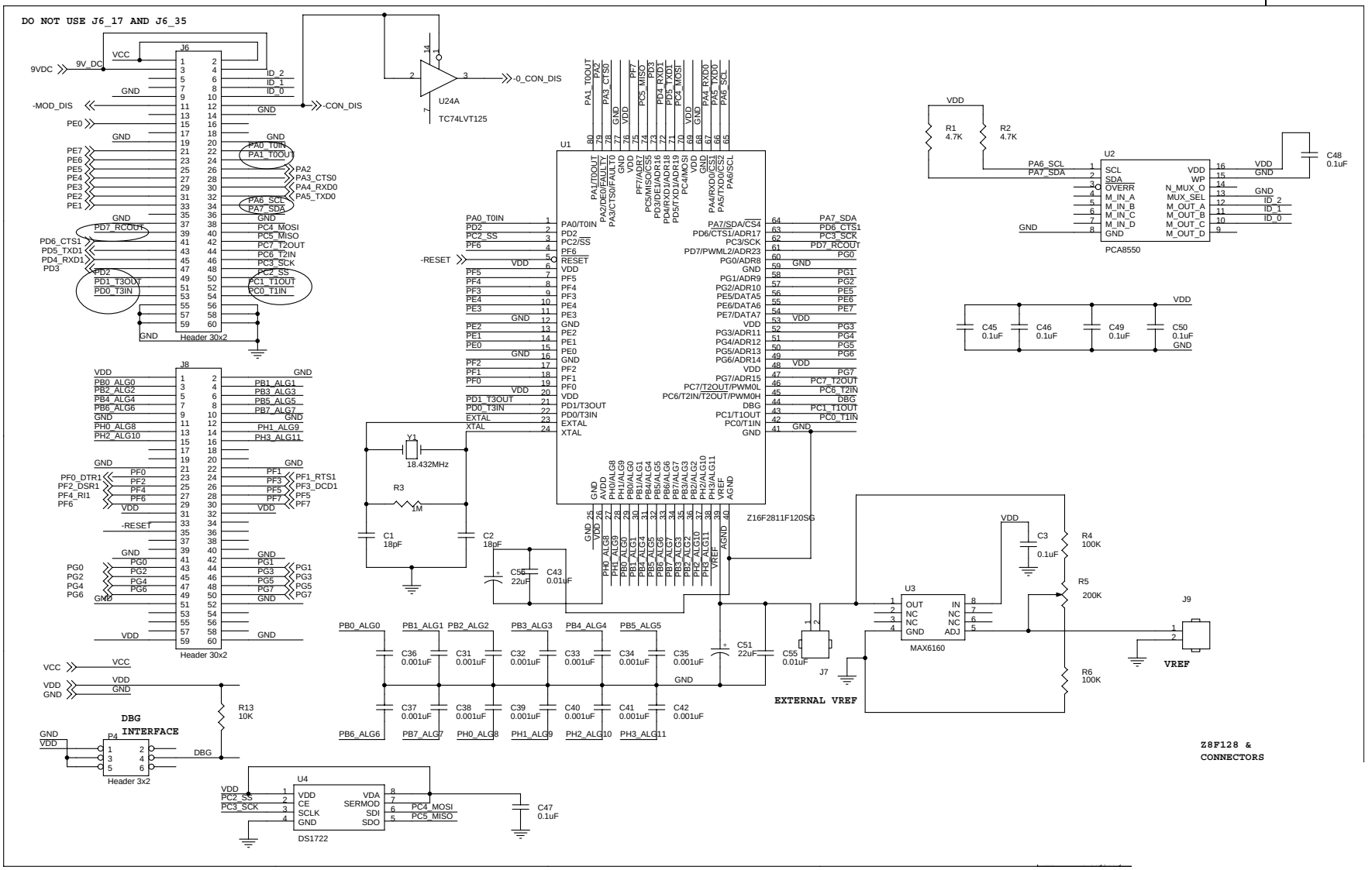


Figure 13. User-Configurable Pushbuttons

Schematics

This section includes schematics for the ZNEO™ Contest Kit Board.



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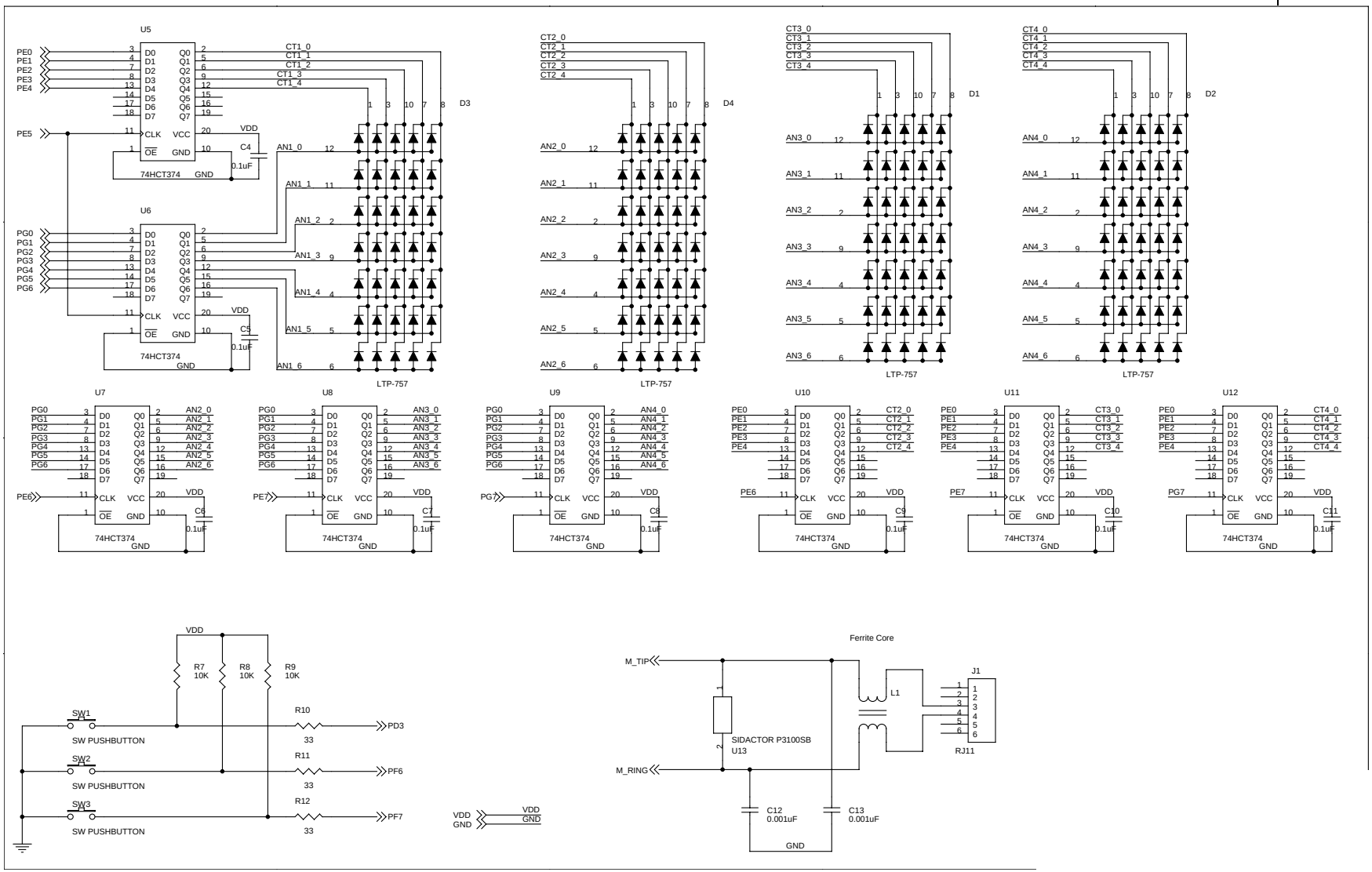

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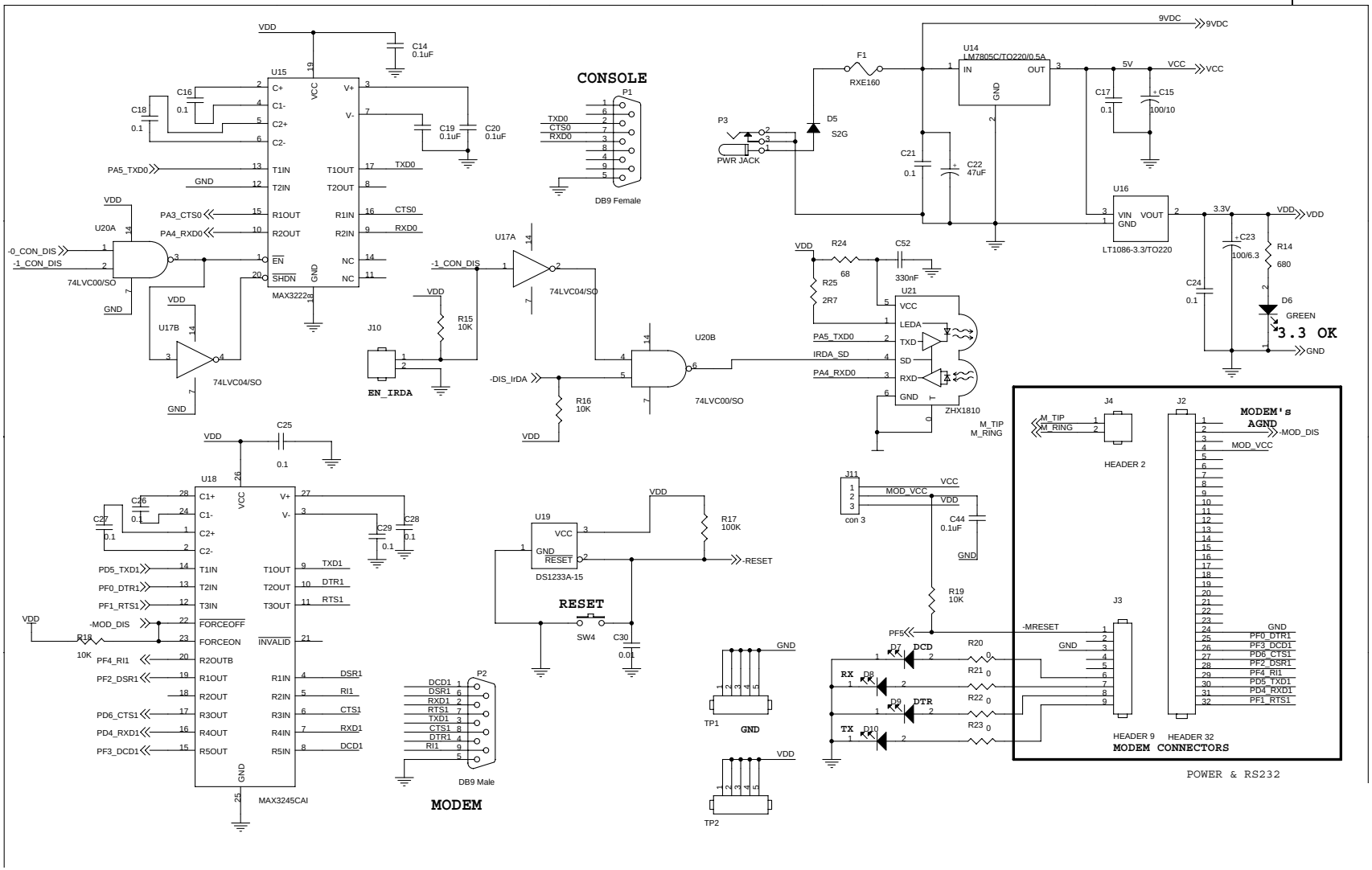

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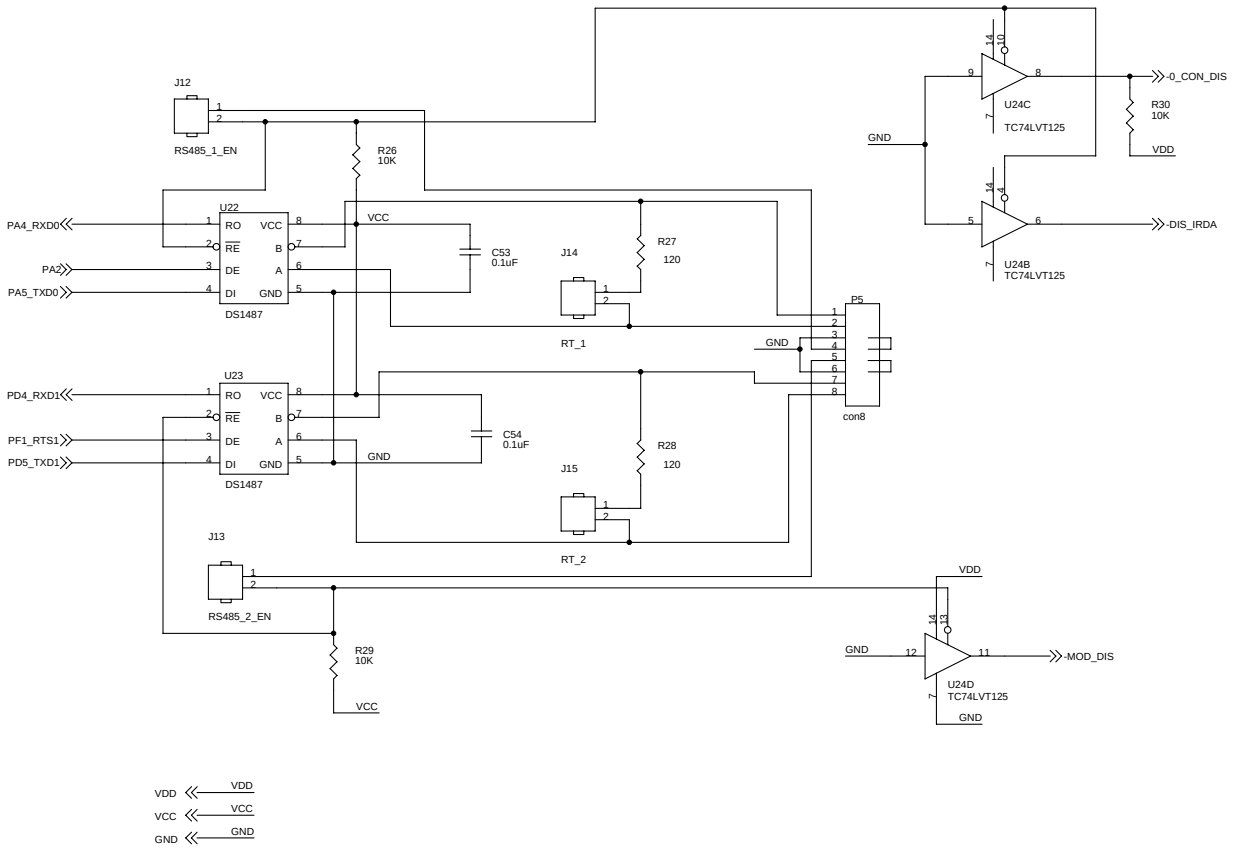

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