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NADC2530
8-CHANNEL 13 BIT
VME NUCLEAR ADC

USER MANUAL

PCB Issue 3
FPGA Version 2530V307

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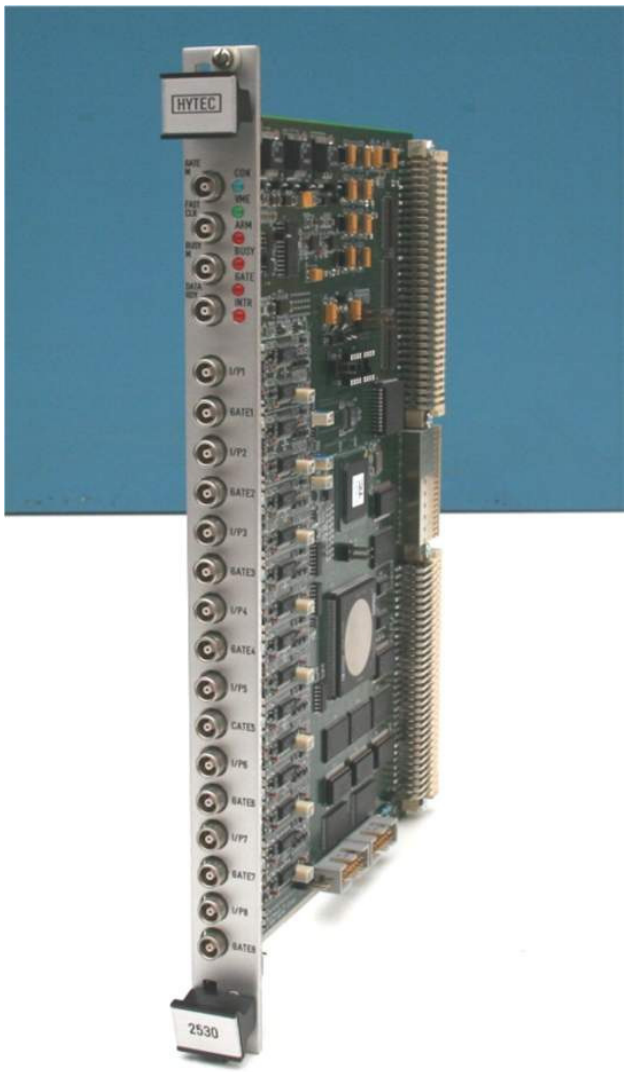
1. Description

The Hytec ADC2530 is a VME module that provides 8 channels of peak-sensing voltage digitisation with the following characteristics:-

- 8 pulse inputs
- Single sampling ADC and 8-input multiplexer
- 13 bits resolution (8000 channels)
- Sliding-scale correction of differential non-linearity
- +/-2% differential non-linearity
- +/- 0.025% linear non-linearity
- 0V - 8.191V input range (positive or negative-going, jumper selectable)
- 1k / 50R input impedance jumper selectable
- On-board dual-port SRAM
- Code format straight binary
- List or histogram modes
- Event counter for list mode
- Self-triggering or Gated modes
- 3us conversion and readout time per input
- Front panel Gate, Fast clear, Data ready, Busy NIM/ECL signals
- Two DAC settings for common Lower Level and Upper Level discrimination.
- Front panel Lemo 00 co-axial connectors
- Front panel LED status indication



1.1 Power Requirements

+5V @ 300mA
+12V @ 200mA (quiescent)
-12V @ 200mA (quiescent)

1.2 Operating Temperature Range

0 to +45 deg Celsius ambient.

1.3 Mechanical

6U single width VME module with access to P1 and P2 connectors.

1.4 Front Panel Indicators

'VME'	LED (green) illuminates for a minimum of 100msecs whenever the module is accessed via the VME bus.
'ARM'	LED (red) indicates that the module is Armed and is acquiring data.
'BUSY'	LED (red) indicates that an input pulse has been accepted and is being converted.
'GATE'	LED (red) illuminated when the module is in Gate mode.
'INTR'	LED (red) indicates that the conditions for interrupt have occurred (***does not indicate a VME interrupt on to the backplane***).
'CONFIG'	LED (blue) indicates that the module is powered and configured.

1.5 Signal Specifications

1.5.1 Pulse Inputs 1-8

Connector type:	Lemo 00 socket isolated from panel. Centre pin-Signal, Outer-AGND.
Signal:	Pulse with rounded top
Span:	0 to 8.191V (1mV per channel). Polarity jumper selectable
Rise time:	100ns – 20us for accurate peak detection.
Input impedance	1K/50R jumper selectable.
ADC resolution:	13 bits (8000 channels with sliding-scale correction).
Diff. non-linearity:	+/-2% (over 99% of range).
Int. non-linearity:	+/-0.025% (over 99% of range).
Offset error:	+/-1LSB.
Gain Error:	+/-1LSB
Gain Drift:	+/-20ppm per deg C
Offset Drift:	+/-2ppm per deg C
ADC conversion :	3uS per input.
Dead time:	1us-20us depending on mode and input usage
Gate period:	20ns-20us

1.5.2 Gate Input (Gates 1-8 and Master Gate)

Connector type: Lemo 00 socket
Signal: NIM/ECL
Causes conversion when the peak of the input pulse is coincident with Gate. Master Gate applies to all inputs in List mode. Individual gates allow conversions on coincident channels in Histogram mode and List mode.

1.5.3 Fast Clear Input

Connector type: Lemo 00 socket
Signal: NIM/ECL
Clears all peak detectors to zero within 50ns

1.5.4 Busy Output

Connector type: Lemo 00 socket
Signal: NIM/ECL
Output signal generated when a pulse is accepted and remains true until all circuits are free to accept a new input

1.5.5 Data Ready Output

Connector type: Lemo 00 socket
Signal: NIM/ECL
Asserted when any Half-full or Full flag is set and can be cleared by writing to Full or Half-Full flags in Fullness register. Or it can be set by a number of events.

2. Technical Note for the ADC2530

2.1 What is the 2530?

This is a VME64 module which accepts up to eight voltage pulsed signals. It measures their peak heights and either counts the number of occurrences at certain peak heights for each input channel (histogram mode) or stores the conversions sequentially in its memory (list mode).

2.2 What are the pulses that it measures?

The input signals are 'rounded top' or Gaussian-shaped pulses. These are derived from radiation detectors such as scintillation (e.g. sodium iodide) or solid-state detectors (e.g. Ge-Li). They are in the form of charge pulses which are normally amplified and converted to voltages by front-end pre-amplifiers and amplifiers. The pulses are shaped to produce rise and fall times of different values. Shaping produces a well defined pulse which is relatively free from noise. Usually the rising edge is fast (50-200ns for solid-state and 200ns-1us for scintillation) with a slow falling edge which decays away exponentially and can be of the order of microseconds or tens of microseconds in the case of scintillation detectors.

2.3 How is the pulse measured?

When the input pulse starts to rise, at some point it exceeds a programmed voltage which determines the lower level discriminator setting. This is set to be above the noise threshold. When this voltage is exceeded the discriminator output opens a linear gate. This gates the pulse to a capacitor which charges up to the peak voltage. This stored voltage is compared with the input pulse and when it exceeds the amplitude of the input pulse, because the input tails away, the linear gate is closed and the peak voltage is held on the capacitor. The voltage stored on the capacitor is then buffered and switched to an ADC for conversion to a binary value.

2.4 Why is good integral and differential non-linearity important?

The measured voltage is proportional to the energy of the detected particle. The spectrum of energies present needs to be measured and it is important that there is a linear relationship between the different energies. This is defined by the integral linearity of the ADC.
The ADC converts the input voltages to 8K different values. The input voltage is a continuous variable and many voltages may have the same converted value. This range is termed a 'bin' and the width of the bin is determined by the differential non-linearity of the ADC. A pulse derived from a radiation detector will be subject to statistical variation and its value may be spread across several bins. Therefore, if a number of pulses derived from the same energy are converted and the conversions with the same values (i.e. falling within the same bin) are counted then the spectrum of the counts will be, ideally, Gaussian. If the bins vary greatly in width then the spectral shape will be distorted.

2.5 What is sliding-scale correction?

Most ADCs have a figure for differential non-linearity of 1/2LSB to 2LSBs. This represents a figure of 50-200%. In order to minimise the differential non-linearity a sliding-scale correction may be applied. This is done by adding a small varying waveform to the signal and then subtracting its digital value from the resultant conversion. Therefore the input voltage is varied across several bins so that with time the variation in bin width is averaged out. If the variation is 64 bins the differential non-linearity will be reduced from 50% to 50/64% or less than 1%. Other errors are involved – the DAC producing the varying summing voltage will also be non-linear. This may be reduced by increasing the resolution of the ADC and dividing down both the analogue output and the digital subtracted value. In practice 1-2% DNL is considered good.

Sliding scale over 64 bins = 6bits = 0- 0x3F of ADC.

Volts/bit of ADC = $2.5/2^{13}$ = 305.176uV

Thus 6bits = 0x3F x 305.176uV = 19.226mV

In the 8.191V range the shaker will move by 19.226mV x (8.191/2.5) = 62.992mV

The shaker injects a negative voltage as this allows a peak pulse at a max voltage of 8.191V to be digitised with out the shaker causing over ranging.
However if a peak pulse of less that approx 63mV then the shaker will take the voltage negative which will cause errors.

2.6 Why use a histogram mode?

When a radioisotope is detected it will produce pulses of different amplitudes depending on the escape energies of the detected particles. The isotope may be identified by a spectrum of energies and its mass can be calculated by the rate of emissions. Therefore it is necessary to count the pulses with similar amplitudes (related to energy) to form a spectrum of counts (frequency) vs bin number (energy). This provides an energy spectrum in which the radiation can be identified from the energy peaks and the activity by the integrated counts divided by the time to acquire them. This time must be the actual count time and should take into account the dead time of the ADC (live time = real time – dead time). Therefore, the time for which the ADC cannot accept a new pulse (dead time) must be indicated (Busy).
The individual gates associated with each input are used for coincidence gating. When the input pulse is in coincidence with its gate it is converted and the data recorded. If it is not in coincidence the pulse is rejected and a fast clear initiated to discharge the hold capacitor and reset the linear gate. In this case the event counter will not be incremented.

2.7 What is List mode?

List (or Gate) Mode uses the Master Gate or individual gates inputs on the front panel to initiate conversions. Any inputs that have a pulse present in coincidence with the gate/s are converted. The conversions are listed to memory with formatting words to provide header, number of channels converted, a 48bit time stamp, highest conversion value, pulse pileup and channel number, end-of-block and event count. Each gate pulse is counted in order to provide the event count.

When individual or master gate events coincide then the event counter will only be incremented once.

In the case of an event occurring in List mode with ZE set and where none of the inputs makes the LLT/HLT. Then the event counter is incremented and a header which includes the number channels held in the list (with ZE set this is always 1000=8 chans), a 48bit time stamp a trailer with event count and in between 8 longwords of channel data with a zero conversion value and a channel tag for each of the 8 channels will be logged in memory.

In the case of an event occurring in List mode with ZE not set and where none of the inputs makes the LLT/HLT. Then the event counter is incremented and a header which includes the number channels held in the list (with ZE not set this will be 000=0 chan) a 48bit time stamp and a trailer with event count will be logged in memory.

When the gate is open in List mode a record is made of the number of pulses per channel (pulse pileup) and the largest signal that occurred during the gate is logged.
The four bit pulse pileup data per channel has been put in the top 4 bits of the same word as the channel number.

3. Operating Modes

3.1 Self Triggering

A pulse received on any input if it is within the lower and upper level discriminator settings will cause the peak value detected to be digitised.

3.2 List Zero Enable

A pulse received on any input if it is within the LLD and ULD settings and coincident with the Gate pulse will cause the peak value detected to be digitised. If the Zero Enable bit is set in the CSR, those channels which do not convert will record a zero conversion.

3.3 Histogram Memory

Eight memory banks accumulate a spectrum of sample frequency vs channel number (conversion value) for each input. The spectra are each 8Kx32 bits. When any channel overflows acquisition on that input is halted until the Full flag is cleared.

3.4 List Memory

The conversions are listed to memory with formatting words to provide header, number of channels converted, conversion value and channel number, end-of-block and event count.

3.5 Interrupt Settings

The VME interrupt level generated by the unit is set using 3 bits in the CSR (IP2 – IP0) see table below.

VME Interrupt Priority Level	IP2	IP1	IP0
None	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

The interrupt is set if a Half Full or Full flag status bit and its corresponding mask bit are set. Or when the number of events is greater than the value set in the Number of Events to Data Ready Flag register when in List Mode.
The front panel INTR light is taken from the IS bit in the CSR and does not indicate that a VME interrupt has been asserted. It only shows only that the conditions for an interrupt to be generated have occurred.
A VME interrupt will only be generated when IS='1', IE='1' and the interrupt priority bits IP0 to IP2 in the CSR are set greater than zero.

3.5.1 Hist Mode Interrupt

Hist Mode STOP on FULL and Interrupt
Half full flags channel 1 to 8 on bits 8 to 15
Full flag channel 1 to 8 on bits 0 to 7
The unit will stop i.e. ARM automatically cleared when full flag set for a channel and the corresponding Interrupt Mask Flag set.
If Interrupt mask not set then unit will set full flag for channel and wrap around on bin count.

3.5.2 List Mode Interrupts

Interrupts in List Mode can be generated on the Full/Half Full flags or when a set number of events has occurred as set in the Number of Events to Data Ready register.
In List Mode the half full flag is bit 8 and the Full flag is bit 0 in the Fullness register.
To generate an interrupt on half full need to set bit 8 in the Interrupt mask register and to generate an interrupt on full need to set bit 0 in interrupt mask reg. For both these need to have 'IT' (bit12 CSR) set to '0'.
The Full flag is set in List Mode when there is insufficient room in the memory for a full sized event to be stored. The acquisition will also be stopped (i.e. ARM automatically cleared) to prevent the memory wrapping round on its self.
When 'IT' (bit12 CSR) set to '1' an interrupt is generated when the number of events is greater than the value set in the Number of Events to Data Ready Flag register.

3.6 Timestamp

The Timestamp comprises of a 48bit counter running at 32MHz (onboard system clock) this gives approx 2443.36hours.
The time stamp starts running as soon as the FPGA has configured. It can be zeroed by writing to a bit in the CSR, or it can be zeroed from the font panel Fast Clear input when the unit is not ARMed.
The contents of the Timestamp counter are latched when either the Master Gate or any of the individual channel gates are asserted in List mode.
The counter will be latched on the first gate to go if multiple gates are asserted.

4. Use of the VME data bus and Memory Access

4.1 Base Address

The module uses A16/D32/D16/ A16D8(EO) is read only (Even and Odd byte) or A24/D32/D16/ A24D8(EO) is read only for accesses to the module Configuration Registers.
The base address of the configuration registers is determined either by the geographical addressing lines GA0 to GA4 or by PCB jumpers J15 to J19.
To use geographical addressing lines set J15 to J19 all to 1 and 2 to use PCB jumpers to select base address set J15 to J19 to positions 2 and 3 as required (all address lines pulled up use jumper to pull down).

Address	Offset	Range	Assignment	Size
I/O Base+	0x0000	0x0000 0x0001	Manufacturer's ID	2 Bytes
I/O Base+	0x0002	0x0002 0x0003	Device Type	2 Bytes
I/O Base+	0x0004	0x0004 0x001F	Module specific configuration registers	28 Bytes
I/O Base+	0x0020	0x0020 0x003F	Not Mapped Reserved for future use	32 Bytes
I/O Base+	0x0040	0x0040 0x0041	Module serial number	2 Bytes
I/O Base+	0x0042	0x0042 0x00BF	Data in Non volatile memory	126 Bytes

NADC2530 A16 and A24 address Map

4.1.1 Short Addressing (A16 AM29h and 2Dh)

The A16 base address is determined either by PCB jumper settings J15=A11 to J19=A15 or by geographical addressing lines GA0 =A11 to GA4=A15.

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
J19 GA4	J18 GA3	J17 GA2	J16 GA1	J15 GA0	X	X	X	X	X	X	X	X	X	X	x

Address modifiers
Configuration Registers:
AM29 Short (A16) non-privilege
AM2D Short (A16) supervisory

4.1.2 Standard Addressing (A24 AM39h and 3Dh)

The A24 base address is determined either by PCB jumper settings J15=A19 to J19=A23 or by geographical addressing lines GA0 =A19 to GA4=A23.
Address modifiers
Configuration Registers:
AM39 Standard (A24) non-privilege
AM3D Standard (A24) supervisory

4.1.3 Carrier board Configuration ROM (A24 AM2Fh)

The module provides CR/CSR Support as specified in the VME64x specification. See **appendix B** for the contents of the configuration ROM.
Address modifiers
AM2F Configuration ROM/Control & Status Registers.

4.2 Memory Access

The unit's base address is stored as an offset in the Memory Offset register.
The module uses address lines A21 to A31.
The unit also supports 32 bit VME block transfer mode BLT and 64 bit MBLT for memory access.
Memory data may be written and read using A32/D64/D32/D16 (EO).
Words and bytes are accessed via D15-D00. A1 addresses the low order word of a longword, A0 the high order word (big endian), thus A0 accesses the first conversion, A1 the second, and so on.

4.3 Extended Addressing Address Modifiers

Memory: AM 09 or 0D (extended non-privileged. or supervisory)
BTL: AM 0B or 0F (extended non-privileged. or supervisory)
MBTL: AM 08 or 0C (extended non-privileged or supervisory)

4.3.1 Memory Data (List Mode)

Memory top = Base + 512K x 32 bit words

D31 D16	D15 D00
List mode data MS	List mode data LS

Memory base = Value in Memory Offset Register.

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	
					0	1	0	UID7	UID6	UID5	UID4	UID3	UID2	UID1	UID0	Header User ID

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	
				CT3	CT2	CT1	CT0									Nos of valid chans

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	
					1	0	1	TS47	TS46	TS45	TD44	TS43	TS42	TS41	TS40	Timestamp Header and Top Byte

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	
TS39	TS38	TS37	TS36	TS35	TS34	TS33	TS32	TS31	TS30	TS29	TS28	TS27	TS26	TS25	TS24	Timestamp Top Word

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	
					1	1	0	TS23	TS22	TS21	TS20	TS19	TS18	TS17	TS16	Timestamp Header Bottom Byte

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	
TS15	TS14	TS13	TS12	TS11	TS10	TS9	TS8	TS7	TS6	TS5	TS4	TS3	TS2	TS1	TS0	Timestamp Bottom Word

D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	
PP3	PP2	PP1	PP0		0	0	0						CH2	CH1	CH0	Channel Number Nos pulse per event

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	
			AD12	AD 11	AD 10	AD 09	AD 08	AD 07	AD 06	AD 05	AD 04	AD 03	AD 02	AD 01	AD 00	ADC Data

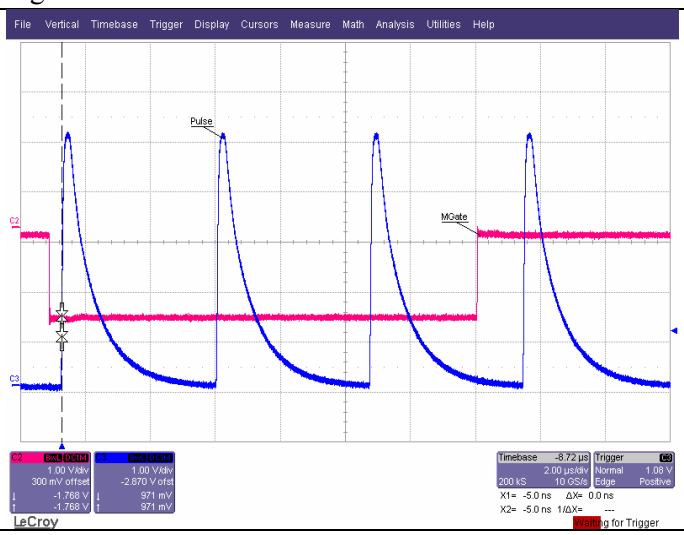
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	
					1	0	0	EC23	EC22	EC21	EC20	EC19	EC18	EC17	EC16	End of Block and Top byte of Event Cnt

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00	
EC15	EC14	EC13	EC12	EC 11	EC 10	EC 09	EC 08	EC 07	EC 06	EC 05	EC 04	EC 03	EC 02	EC 01	EC 00	Event Count bottom two bytes

CT0-CT3 denote the number of valid channels in the event 0000=none and 1000=8.
CH0-CH2 denote the channel number 000=chan1 and 111=chan8.
PP0 – PP3 denotes the number of pulses received by a channel for a single event.
ADxx denotes ADC conversion data bit
EC0-EC23 denote the event count
Bits 24-26 in each 32 bit word denote header/value/end of block
If ‘ZE’ set number of valid channels will always be set to 8 and those channels which do not convert will have there channel numbers recorded and zero as there conversion data.

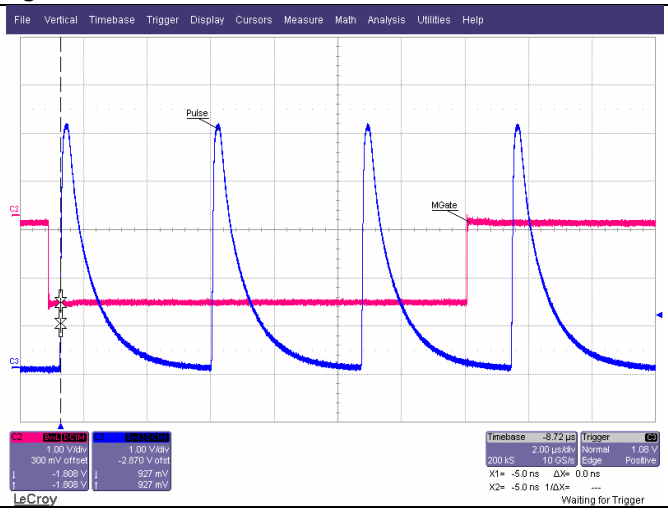
List Mode gate left open HE=0 GE=1 **ZE=0** User ID = 0xAA Input to channel I/P3
In this case 3 pulses digitised and the largest recorded

List Mode Data
0x02AA0100
0x05002444
0x065197D1
0x300212B7
0x04000001



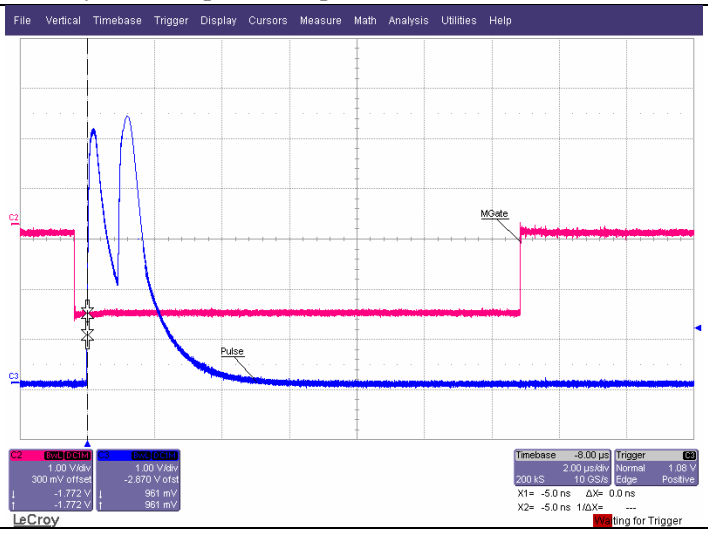
List Mode gate left open HE=0 GE=1 **ZE=1** User ID = 0xAA Input to channel I/P3
In this case 3 pulses digitised and the largest recorded

List Mode Data
0x02AA0800
0x050026DD
0x0611F169
0x00000000
0x00010000
0x300212B5
0x00030000
0x00040000
0x00050000
0x00060000
0x00070000
0x04000001



List Mode gate left open HE=0 GE=1 ZE=0 User ID = 0xAA Input to channel I/P3
In this case where a double pulse occurs only the first peak is captured.

List Mode Data
0x02AA0100
0x05004289
0x0698B7D6
0x100212BC
0x04000001



4.3.2 Memory Data (Histogram mode)

Spectra for each input are stored in memory in **Histogram mode** as shown:-
Memory top = Base + 64K 32 bit words

D31 D16 D15 D00		
Spectrum 8	8K channels x 32 (Counts the number of times a conversion value occurs for input 8)	0xFFFF 0xE000
Spectrum 7	8K channels x 32 (Counts the number of times a conversion value occurs for input 7)	0xDFFF 0xC000
Spectrum 6	8K channels x 32 (Counts the number of times a conversion value occurs for input 6)	0xBFFF 0xA000
Spectrum 5	8K channels x 32 (Counts the number of times a conversion value occurs for input 5)	0x9FFF 0x8000
Spectrum 4	8K channels x 32 (Counts the number of times a conversion value occurs for input 4)	0x7FFF 0x6000
Spectrum 3	8K channels x 32 (Counts the number of times a conversion value occurs for input 3)	0x5FFF 0x4000
Spectrum 2	8K channels x 32 (Counts the number of times a conversion value occurs for input 2)	0x3FFF 0x2000
Spectrum 1	8K channels x 32 (Counts the number of times a conversion value occurs for input 1)	0x1FFF 0x0000

Memory base = Value in Memory Offset Register.

4.3.3 Memory Data (Histogram Mode)

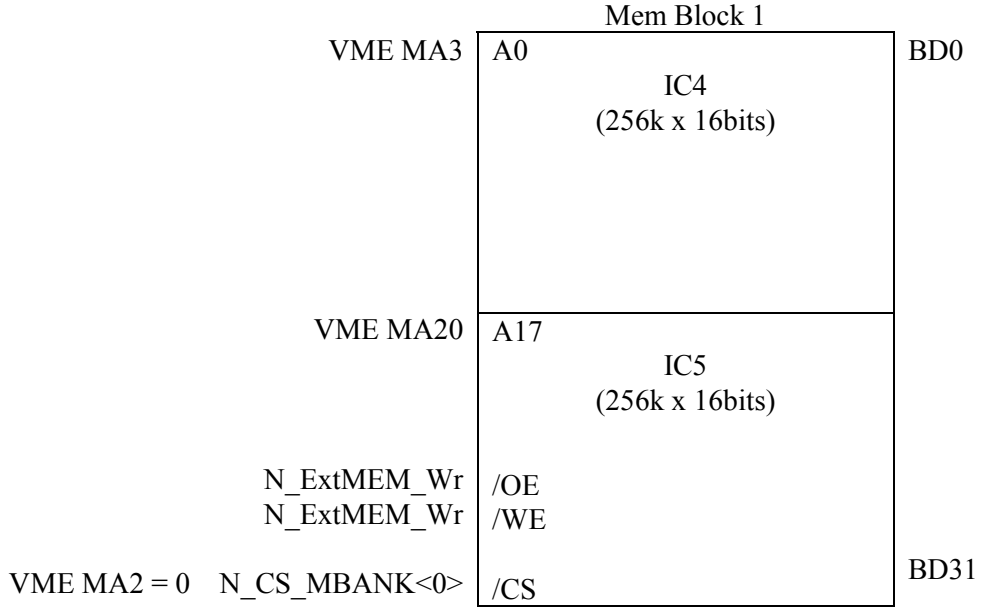
D31	D30	D29	D28	D27	D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16
S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16

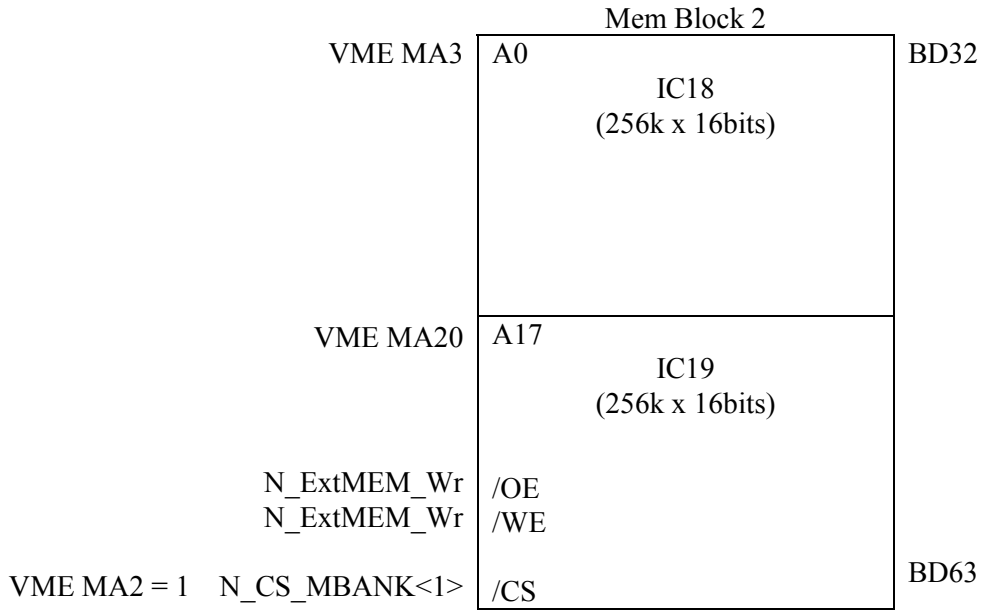
D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0

S0-31 denotes ADC conversion sampling frequency data. An overflow will set Full.

4.4 PCB MEMORY and DATA PATH

Total memory = 512K x 32 bits (0x00000 – 0x7FFFF)
Total memory = 256K x 64 bits (0x00000 – 0x3FFFF)





Mem Block 2		Mem Block 1		Address
Chan(7)222	**Hist FFF**	**Chan(7) 423**	**Hist FFE**	3FFFF
Chan(7)777	**Hist FFD**	**Chan(7) 555**	**Hist FFC**	3FFFC
Chan(0) 000	**Hist 3**	**Chan(0) 000**	**Hist 2**	0002
Chan(0) 000	**Hist 1**	**Chan(0) 000**	**Hist 0**	0000
ADC_MA(0)=1		ADC_MA(0)=0		
BD63			BD0	

5. Firmware Registers

5.1 Manufactures Device ID (Read)

Address: Base + 00 Value = 0x1F7F

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	1	1	1	1	1	0	1	1	1	1	1	1	1

5.2 Device Type (Read)

Address: Base + 02 Value= 0x09E2 (2530dec)

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	1	0	0	1	1	1	1	0	0	0	1	0

5.3 Control & Status Register (CSR)

Control (Write) Address: Base + 04
Note NU = Not Used.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
HE	GE	ZE	IT	IP2	IP1	IP0	ARM	I.E	CLTS	ACM	FFCLR	SC	iDR	SS	Rst

Status (Read) Address: Base + 04
Note NU = Not Used.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
HE	GE	ZE	IT	IP2	IP1	IP0	ARM	I.E	IS	ACM	NU	SC	oDR	SS	Bsy

HE Enables histogram mode
GE Enables Gate mode
ZE Enables zero conversion – an input registers 0 if not in coincidence with Gate.
IT This sets the Interrupt source IT='0' interrupt from Full and Half full flags.
IT='1' interrupt when the event count is greater than the value in the Number Events to Data Ready Flag register.
IP0-2 Sets interrupt priority level.
ARM Start acquisition according to mode (Automatically cleared on memory full in List Mode).
IE Interrupt Enable - An IRQ is generated if IS is set and interrupts are enabled.
The IRQ number is determined by IP0-2. This bit is cleared during interrupt cycle ROAK.
IS **Read only** Interrupt status set by any mask enabled fullness flag or by number of events.
CLTS **Write only** This clears the Timestamp counter when ARM is not asserted.
ACM Automatic Memory clear FP Busy set during clear ACM auto cleared when completed
FFCLR **Write only** This forces a fast clear on all channels (FFCLR bit auto cleared after approx 100ns)
SC Set calibration ON (see Calibration Register)
oDR Data Ready set by any mask enabled fullness flag or by a set number of events.
iDR iDR='0' Data Ready set when any of the channel flags are set.
iDR='1' Data Ready set when a programmed number of events occurs.
SS Sliding scale set to '0'= enabled and set to'1'= disabled.
Busy Set when an input pulse/pulses have been accepted and are being converted. This remains true until all inputs are free to accept new input.
Rst Clears status register to zero.

GE	HE	MODE
0	0	Test mode convert no gate not put into memory
0	1	Histogram mode
1	0	Gate mode using front panel Master Gate data put in to memory in list mode
1	1	Histogram were individual gates on front panel are used

5.4 Memory Offset (Read/Write)

Address: Base + 06

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
A31	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	X	X	X	X	X

The memory offset sets the memory base address in pages of 128Kwords. D00 and D01 are ignored.

5.5 List Mode Memory Address Counter LS (Read/Write)

Address: Base + 08

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

In this version of the firmware removing ARM in List mode does not clear memory address counter.

5.6 List Mode Memory Address Counter MS (Read/Write)

Address: Base + 0A

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
X	X	X	X	X	X	X	X	X	X	X	X	X	C18	C17	C16

5.7 Interrupt Vector (Read/Write. Automatically read by an IACK operation)

Address: Read = Base + 0C, Write = Base + 0C

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
V15	V14	V13	V12	V11	V10	V09	V08	V07	V06	V05	V04	V03	V02	V01	V00

The interrupt vector register can be overwritten and read. The vector is generated during an IACK cycle when the module has interrupted. This allows D08(EO) writes as well as reads.

5.8 Calibration And Test Register (Read/Write)

Address: Base + 0E

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
DEAC	X	X	X	X	X	X	DISC	X	X	X	X	MEN	M2	M1	M0

Select which channel to calibrate when SC set in CSR. This opens the channel gate and sets the MUX switch on PCB to allow voltage at the channel input to be measured.
M0 to M2 selects channel (000 = chan 1 to 111 = chan 8) and MEN enables the MUX switch.
The ADC will convert and update the Conversion Register as fast as it can i.e. as soon as one sample read a next is started.
When DISC Disable compensation '0' then compensation applied.
When Disable Auto Fast Clear (DEAC) set a fast clear pulse will not be issued this is for test only.

5.9 Fullness Flag Register (Read/Write)

Address: Base + 10

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
HF8	HF7	HF6	HF5	HF4	HF3	HF2	HF1	F8	F7	F6	F5	F4	F3	F2	F1

The Half full and Full flags for each channel 1-8. In spectrum mode Full denotes sample overflow.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
NU	NU	NU	NU	NU	NU	NU	HF	NU	NU	NU	NU	NU	NU	NU	F

The Half full and Full flags in LIST mode.
The Full flag is set in List Mode when there is insufficient room in the memory for a full sized event to be stored i.e. number of free longwords in memory < 10. The acquisition will also be stopped (i.e. ARM automatically cleared) to prevent the memory wrapping round on its self.

5.10 Interrupt Mask/Number Events to Data Ready Flag Register (Read/Write)

Address: Base + 12

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
M16	M15	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1

The interrupt mask bits mask on each respective flag and enable them to generate interrupt when iDR='0'.
When set to Number of Events to Data Ready flag by iDR='1' then in List Mode the Data Ready flag in the CSR and the front panel output 'DATA RDY' will be set when the number of events is greater than the value set in the Number of Events to Data Ready Flag register.

5.11 Lower Level Discriminator Value (Read/Write)

Address: Base + 14

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	LD11	LD10	LD9	LD8	LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0	0	0

The value written to this register will set the common lower level discriminator value from 0V to 0.8191V full-scale.
Pulses rising above this level will have their peak values held and converted. Pulses below this level will be ignored or recorded as zero according to the control setting.

LLD DAC Value = (((Vreq/3.2764)/(0.25/4095))<<2) &0x3ffc;

DAC 12 bits first 2 bit must be zero and last 2 bits must be zero these are control bits.

5.12 Upper Level Discriminator Value (Read/Write)

Address: Base + 16

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	UD11	UD10	UD9	UD8	UD7	UD6	UD5	UD4	UD3	UD2	UD1	UD0	0	0

The value written to this register will set the common upper level discriminator value as 8.191V full-scale.
Pulses above the Lower Level and below this level will be converted. Pulses rising above this level will be ignored or recorded as zero according to the control setting

ULD DAC Value = (((Vreq/3.2764)-2)/(0.5/4095))<<2) &0x3ffc;

DAC 12 bits first 2 bit must be zero and last 2 bits must be zero these are control bits.

5.13 Event Counter LS (Read/Write)

Address: Base + 18

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0

5.14 Event Counter MS (Read/Write)

Address: Base + 1A

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
								EC23	EC22	EC21	EC20	EC19	EC18	EC17	EC16

5.15 Conversion (Read) Address: Base + 1C

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

ADC 16bit raw value this holds last channel conversion. Used for calibration were one channel calibrated at a time.

OR

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
MA2	MA1	MA0	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0

ADC 13bit raw with mux switch settings to select a channel. Could be like this on final version !!!!

5.16 Sliding Scale Test register (Read/Write) Address: Base + 1E

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	SS11	SS10	SS9	SS8	SS7	SS6	SS5	SS4	SS3	SS2	SS1	SS0	0	0

DAC 12 bits first 2 bit must be zero and last 2 bits must be zero these are control bits.
This register is used for testing of the Sliding Scale function.

5.17 User ID register (Read/Write) Address: Base + 20

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
0	0	0	0	0	0	0	0	UID7	UID6	UID5	UID4	UID3	UID2	UID1	UID0

The user can enter an 8bit ID which will be appended to the Header D16 – D23 in List mode.

6. VME System Reset

6.1 A VME system reset will clear the following registers:

- CSR CB
- Memory Offset Register
- IP Interrupt Select register

7. Sliding Scale Correction

If ARM = ‘1’ and SS = ‘0’ then sliding scale counters for each channel will increment.
If ARM = ‘0’ or SS = ‘1’ then sliding scale counters are cleared to zero.

The sliding scale value of each channel is loaded every time the channel flag is set.

8. FPGA OPERATION

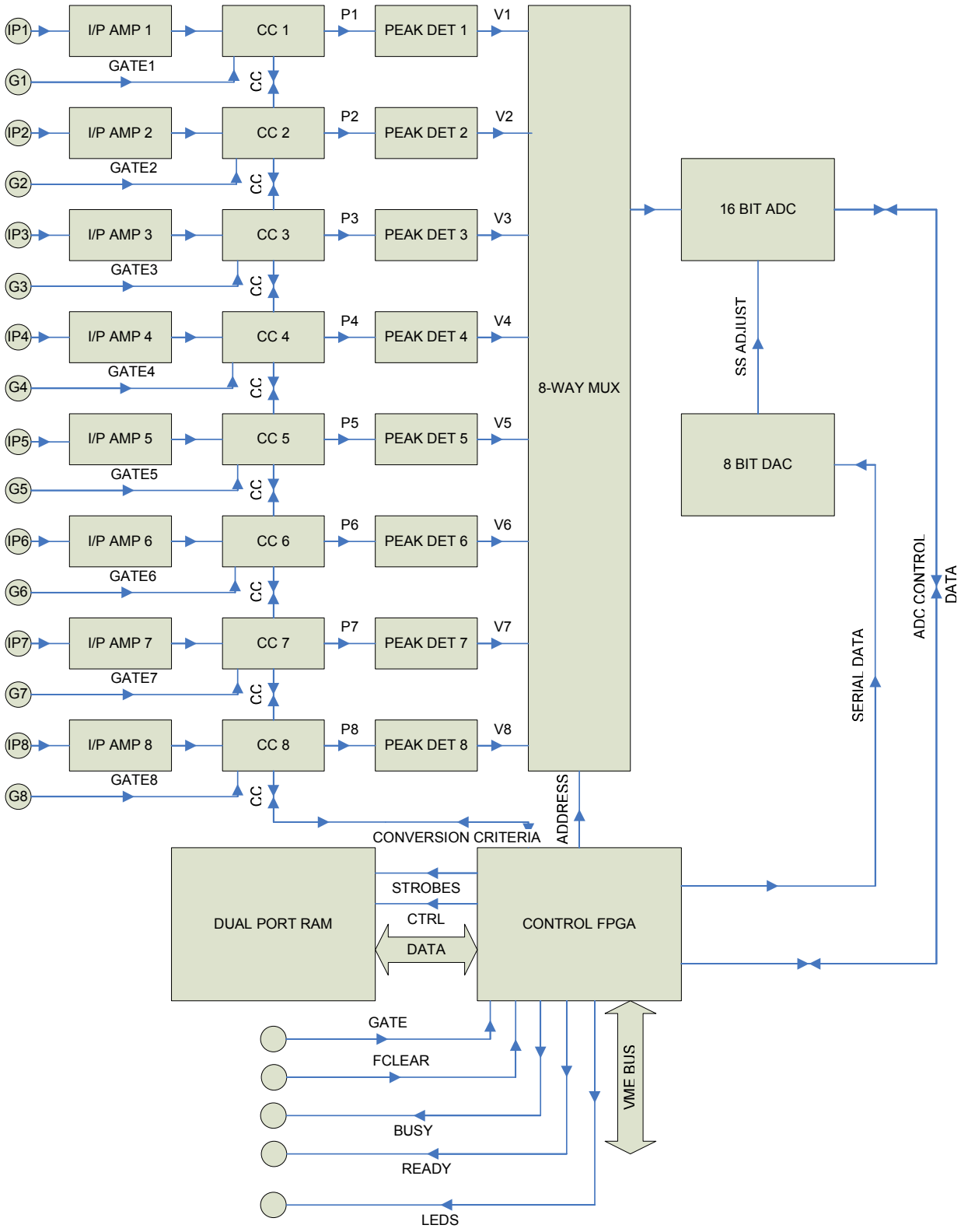
The controlling firmware is implemented in a Field Programmable Gate Array (FPGA). The code has been written in VHDL and consist of a number of state machines and discrete logic.

Lower level detector (LLD) asserted on rising pulse the module waits for Peak Detect (PKDET) to go low. If this does not go low within a defined time (125ns) the system times out and a fast clear is invoked and the reading aborted.
If PKDET set Low then unit waits for PKDET High. If at this point ARM=0 or if LLD = 0 (gate open on a glitch) or if ULD = 1 (to small or to fast a pulse) then again fast clear set and reading aborted.

9. Data Format

Data format 0x0000 = 0V, 0x0001=1mV, 0x1FFF = +8.191V.

10. NADC2530 BLOCK DIAGRAM



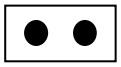
2530 8-CHANNEL VME NUCLEAR ADC
BLOCK DIAGRAM

APPENDIX A Configuration ROM

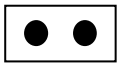
Address Offset	Value	Definition
0x03	C1	Check Sum
0x07	00	Length of ID ROM MSB
0x0B	02	Length of ID ROM
0x0F	00	Length of ID ROM LSB
Configuration ROM data access width		
0x13	0x83	Use D16 or D8
CSR data access width		
0x17	0x83	Use D16 or D8
CSR space Specification ID		
0x1B	0x02	VME64x-1997
Identify a Valid CR		
0x1F	0x43	'C'
0x23	0x52	'R'
Manufacturer's ID		
0x27	0x00	
0x2B	0x1F	
0x2F	0x7F	
Board ID		
0x33	0x4E	hex ANSI =N (Nuclear)
0x37	0x41	hex ANSI =A (ADC)
0x3B	0x09	0x9E2 = 2530dec
0x3F	0xE2	
Revision ID		
0x43	0x03	PCB issue
0x47	0x03	Xilinx version (same as PCB issue)
0x4B	0x00	Xilinx revision nos
0x4F	0x01	Xilinx revision nos
ASCII string null terminated or 0x000000		
0x53	0x00	
0x57	0x00	
0x5B	0x00	
Reserved for future use		
0x5F to 0x7B		
Program ID code		
0x7F	0x01	No program, ID ROM only
Interrupt capabilities		
0xF7	0xFE	Denotes support for Int levels 7 - 1
Start of VME64X Defined CR		
0x83, 0x87, 0x8B	0x001004	Offset to BEG_USER_CR
0x8F, 0x93, 0x97	0x001103	Offset to END_USER_CR
Board Serial Number		
0xCB, 0xCF, 0xD3	0x001000	Offset to BEG_SN
0xD7, 0xDB, 0xDF	0x001003	Offset to END_SN
Data Access Width		
0x103	0x84	Accepts D32, D16 or D08(EO) cycles
AM code mask		
0x123 .. 0x13F	0x2200A2000000BB00	AM codes 3D,39,2F,2D,29, 0F,0D,0C,0B,09,08

APPENDIX B PCB Jumper and Link Settings

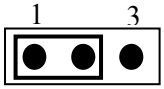
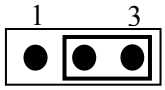
MGATE

Jumper	Jumper setting	**MGATE INPUT** (Lemo 00 socket) Causes conversion of input pulses coincident with Gate. Master Gate applies to all inputs in List mode.
J8		For ECL input put jumper IN And if MGATE input is not driven
		For NIM input jumper OUT
J7		No termination jumper OUT
		Jumper IN puts 51ohm termination on MGATE input. And if MGATE input is not driven

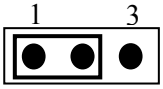
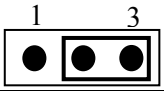
FAST CLEAR

Jumper	Jumper setting	**FAST CLR INPUT** (Lemo 00 socket) Clears all peak detectors to zero within 50ns
J10		For ECL input put jumper IN And if Fast Clear input is not driven
		For NIM input jumper OUT
J9		No termination jumper OUT
		Jumper IN puts 51ohm termination on Fast Clear input. And if Fast Clear input is not driven

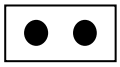
MBUSY

Jumper	Jumper setting	**MBUSY OUTPUT** (Lemo 00 socket) Output signal (NIM/ECL) generated when a pulse is accepted and remains true until all circuits are free to accept a new input
J11		For ECL output put jumper across 1 and 2 (J12 must be OUT).
		For NIM output put jumper across 2 and 3 (J12 must be IN)
J12		For ECL jumper OUT no termination.
		For NIM put jumper IN. This puts 51ohm termination on MBUSY output.

DATA RDY

Jumper	Jumper setting	**DATA RDY OUTPUT** (Lemo 00 socket) Asserted when any Half-full or Full flag is set and can be cleared by writing to Full or Half-Full flags in Fullness register. Or it can be set by a number of events.
J13		For ECL output put jumper across 1 and 2 (J12 must be OUT)
		For NIM output put jumper across 2 and 3 (J12 must be IN)
J14		For ECL jumper OUT no termination.
		For NIM put jumper IN. This puts 51ohm termination on DATA RDY output.

GATE (Chan) Individual Channel Input

Jumper	Jumper setting	**GATE (Chan Nos) INPUT** (Lemo 00 socket) Individual channel Gates allow conversions on coincident channels in Histogram mode and List mode.
J6 Chans 1 to 8		For ECL input put jumper IN And if GATE X input is not driven
		For NIM input jumper OUT
J5 Chans 1 to 8		No termination jumper OUT
		Jumper IN puts 51ohm termination on GATE X input. And if GATE X input is not driven

Channel Input Terminations
J1 (Chans 1-8) When made 56R is connected across the respective input.

Channel Input Inverted/non-inv
J2 and J3 (Chans 1-8)
J2= 2:3 J3= 1:2 Inverted
J2= 1:2 J3= 2:3 Non Inverted

Channel Input Range
J4 (Chans 1-8)
0 to 8.0V place link in J4 1:2
0 to 2.0V place link in J4 2:3 *(not yet tested)*

FPGA Boot
J20 Master Made when Master FPGA (IC22 and IC23) SPROM installed.
J24 Must be IN Factory set (bottom ejector handle over ride).

Grounds
LK1 GND to AGND When made connects Analogue Ground to Digital Ground.
NOTE Do not remove this link as component damage may result .

Pre-charge voltage pins
LK2 Fit for VME creates with out Pre-charge voltage pins.

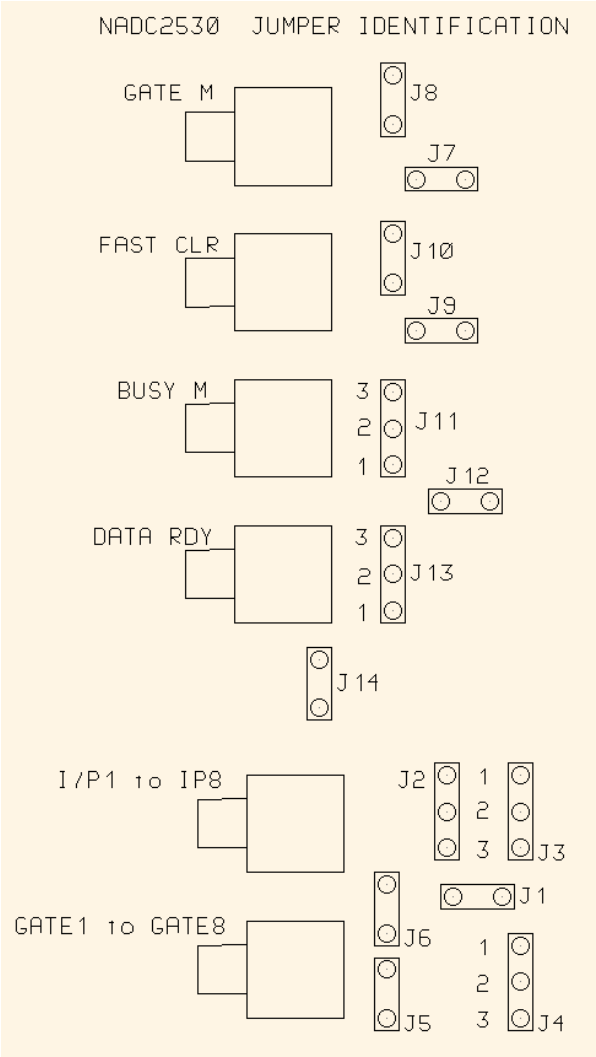
Set Base Address
J15 – J19 Base address

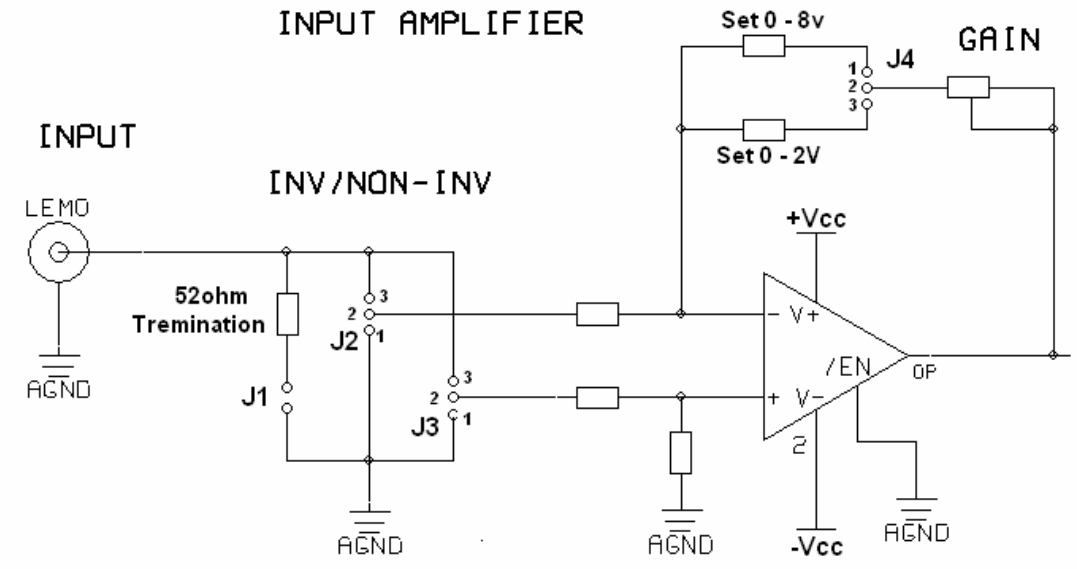
To use VME64 geographical addressing lines all jumpers should be inserted in to position 1:2.

To use the user set base address removing all Base address jumpers from positions 1:2 and insert the required jumpers in to positions 2:3.
With no jumpers in position 2:3 for J19 to J15 the address is 0x0000 A16 or 0x000000 A24.
With one jumpers in position 2:3 for J15 the address is 0x0800 A16 or 0x080000 A24.
With all jumpers in position 2:3 for J19 to J15 the address is 0xF800 A16 or 0xF80000 A24.

Base Addrs (Hex)		J19 2:3 A15	J18 2:3 A14	J17 2:3 A13	J16 2:3 A12	J15 2:3 A11
A16	A24					
0000	000000	OUT	OUT	OUT	OUT	OUT
0800	080000	OUT	OUT	OUT	OUT	IN
1000	100000	OUT	OUT	OUT	IN	OUT
1800	180000	OUT	OUT	OUT	IN	IN
:	:	:	:	:	:	:
E000	E00000	IN	IN	IN	OUT	OUT
E800	E80000	IN	IN	IN	OUT	IN
F000	F00000	IN	IN	IN	IN	OUT
F800	F80000	IN	IN	IN	IN	IN

APPENDIX C Jumper Identification





APPENDIX D Digital Signals

NIM (Nuclear Instrument Module)

Terminated Signals

The characteristic impedance for terminated signals is 50 ohms as set out in the table below.

	Logic '0'	Logic '1'
Outputs into 50 ohms	-2 to +2 mA	-14 to -18 mA
Inputs	-4 to +20 mA	-12 to -36 mA

ECL (Emitter-coupled logic)

ECL running on negative supply V_{HIGH} = -1.00V V_{LOW} = -1.80V

APPENDIX E Modification to Allow Operation on Non VME64 Backplanes

This modification is required if there is no 3.3V supplied via the back plane. i.e. a non VME 64 backplane.

The diagram below shows the wire modification to connect the on board 3.3V to the fuse F3. The bottom of the wire is attached to the underside of the +3V3 test pin. The top end of the wire is attached to the fuse F3 top holder.
To check the mod there should be continuity between +3V3 test pin and the pos of capacitor C9.

The fuse F3 must be removed.

When the module is powered up the BLUE led on the front panel of the NADC2530 should come ON and then go OFF in under a couple of seconds to indicate that the power supplies and the FPGA are up and running.