USER MANUAL

Accessory 34A

Opto 32-Bit Input/ 32-Bit Output Board

3Ax-602350-xUxx

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21314 Lassen Street Chatsworth, CA 91311 // Tel. (818) 998-2095 Fax. (818) 998-7807 // www.deltatau.com

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Delta Tau Data Systems, Inc. Technical Support
Phone: (818) 717-5656
Fax: (818) 998-7807
Email: support@deltatau.com
Website: http://www.deltatau.com

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INTRODUCTION

PMAC's Accessory 34A(ACC-34A) is a general-purpose discrete input/output (I/O) board. ACC-34A provides 32 lines of optically isolated inputs and 32 lines of optically isolated outputs. Port A contains the 32 input lines (AI0 to AI31). Port B contains the 32 output lines (BO0 to BO31). The actual I/O Reads and Writes are carried out using a special form of M-variables, which will be described later. ACC-34A is one of a series of I/O accessories for PMAC that uses the JTHW connector. Others are:

ACC-34	The Opto 64-bit Input/Output board
ACC-34B	The 64-bit Standard Opto I/O Interface board
ACC-18	The Thumbwheel Multiplexer board
ACC-8D Option 7	The Resolver to Digital Converter board
ACC-8D Option 8	The Absolute Encoder Interface board

All of the above accessories use the JTHW multiplex address scheme, and several of them may be daisy-chained to a single PMAC. For enhanced noise reduction and long distance installation, Accessories 35A and 35B provide differential buffer capabilities for the JTHW signals. The use of the long distance buffer pair (ACC-35A and ACC-35B) is recommended whenever the required cable length between PMAC and ACC-34x is over 3 meters (10 feet).

Up to 32 ACC-34As may be connected to a single PMAC, which gives a possible 1024 input and 1024 output lines *in addition* to those available on the PMAC board and on the parallel I/O expansion board(s) (ACC-14). Accessory 34 communicates to PMAC via its JTHW connector through the supplied flat cable.

ACC-34A output drivers are organized in a set of four 8-bit groups. Each group (each byte) may be ordered with either current sourcing drivers (default) or with current sinking drivers. The default configuration of this accessory board uses UDN2981 current sourcing drivers for the four 8-bit output groups. With this configuration, the current drawn from each output line should be limited to 100 mA at voltage levels between 12 and 24 volts. Custom orders (ordered as ACC-34A Option 1) are available for current sinking applications. In current sinking configurations, one ULN2803 driver is used for each 8-bit output group. Each open collector output line can sink up to 100 mA when pulled up to a voltage level between 12 to 24 volts (external pull-up resistors are not supplied). When this accessory is ordered with its Option 1, the mixing of current sourcing and sinking drivers is possible (in 8-bit groups).

ACC-34A input buffers are also organized in a set of four 8-bit groups. Each group (each byte) uses one ULN2802 driver as the input buffer. Both current sourcing and sinking inputs are accommodated by the appropriate setting of the pertinent jumpers and diode groups as explained later in this Manual. The default setting is for current sourcing configurations on all inputs.

ACC-34A also supports a local watchdog timer feature independent of PMAC's. The operation of this feature is explained at the end of this manual (see also the enclosed schematic).

CONNECTORS

Refer to the layout diagram of ACC-34A for the location of the connectors on the board. A pin definition listing for each connector begins on page 28 of this Manual.

J1 (JTHW)

This 26-pin Header provides the link between PMAC's JTHW (J3) and ACC-34A. Using the supplied flat cable, PMAC's J3 should be connected to J1. Through this connector, PMAC sets the outputs and reads the inputs. The power for the processor side of the opto-isolation circuitry is provided from the PMAC board through this connector. For the connection of multiple ACC-34As to a single PMAC, a daisy-chain cable is required (consult Delta Tau for a Special Order on the daisy-chain cable). A daisy-chain cable is also required if one or more Thumbwheel Multiplexer boards (ACC-18) or R-to-D boards (ACC-8D Opt. 7) are used in conjunction with one or more ACC-34As.

TB1

This 10-pin Terminal Block is used for the connection to the first set of eight input lines (AI0 to AI7). A separate power supply for the pull-up/down resistors of AI0 to AI7 should be brought in through this connector (15 to 24V, 70 mA).

TB2

This 10-pin Terminal Block is used for the connection to the second set of eight input lines (AI8 to AI15). In addition, a separate power supply for the pull-up/down resistors of AI8 to AI15 should be brought in through this connector (15 to 24V, 70 mA).

TB3

This 10-pin Terminal Block is used for the connection to the third set of eight input lines (AI16 to AI23). A separate power supply for the pull-up/down resistors of AI16 to AI23 should be brought in through this connector (15 to 24V, 70 mA).

TB4

This 10-pin Terminal Block is used for the connection to the fourth set of eight input lines (AI24 to AI31). A separate power supply for the pull-up/down resistors of AI24 to AI31 should be brought in through this connector (15 to 24V, 70 mA).

TB5

This 10-pin Terminal Block is used for the connection to the first set of eight output lines (BO0 to BO7). A separate power supply for BO0 to BO7 should be brought in through this connector. In the sourcing configuration, this supply will be used to drive the loads on the eight lines (up to 800 mA maximum at 24V). In the sinking configuration, the current requirement from this power supply is minimal (approx. 70 mA).

TB6

This 10-pin Terminal Block is used for the connection to the second set of eight output lines (BO8 to BO15). A separate power supply for BO8 to BO15 should be brought in through this connector. In the sourcing configuration, this supply will be used to drive the loads on all eight lines (up to 800 mA maximum at 24V). In the sinking configuration, the current requirement from this power supply is minimal (approx. 70 mA).

TB7

This 10-pin Terminal Block is used for the connection to the third set of eight output lines (BO16 to BO23). A separate power supply for BO16 to BO23 should be brought in through this connector. In the sourcing configuration, this supply will be used to drive the loads on all the eight lines (up to 800 mA maximum at 24V). In the sinking configuration, the current requirement from this power supply is minimal (approx. 70 mA).

TB8

This 10-pin Terminal Block is used for the connection to the fourth set of eight output lines (BO24 to BO31). A separate power supply for BO24 to BO31 should be brought in through this connector. In the sourcing configuration, this supply will be used to drive the loads on all eight lines (up to 800 mA maximum at 24V). In the sinking configuration, the current requirement from this power supply is minimal (approx. 70 mA).

TB9

This is a 2-pin terminal block used to bring in the power supply (12-24V) for logic circuits on the I/O side of the opto-isolation circuitry. For proper operation of the board, this power supply must be brought in through TB9.

MULTIPLEX ADDRESS MAP

Each ACC-34 occupies eight bytes of address space on the PMAC's JTHW multiplex memory space. This memory space is 8-bits wide, which provides the ability to daisy chain 32 (256/8) ACC-34XS together (or a combination of ACC-34XS, ACC-18s and ACC-8D OPT7s). The 5-bit DIP switch, SW1, determines the address of each ACC-34X board on the allocated memory space. Port A occupies the base address (i.e. bytes 0, 8, 16 etc.) and Port B occupies the base address plus 4 (i.e. bytes 4, 12, 20 etc.). The following table shows how SW1 should be set for one or more ACC-34X boards connected to the same PMAC.

SW1 DIP Switch Setting

Board #	Byte (Port A & Port B)	5	4	3	2	1
#1	0 & 4	ON	ON	ON	ON	ON
#2	8 & 12	ON	ON	ON	ON	OFF
#3	16 & 20	ON	ON	ON	OFF	ON
#4	24 & 28	ON	ON	ON	OFF	OFF
#5	32 & 36	ON	ON	OFF	ON	ON
#6	40 & 44	ON	ON	OFF	ON	OFF
#7	48 & 52	ON	ON	OFF	OFF	ON
#8	56 & 60	ON	ON	OFF	OFF	OFF
#9	64 &68	ON	OFF	ON	ON	ON
#10	72 & 76	ON	OFF	ON	ON	OFF
#11	80 & 84	ON	OFF	ON	OFF	ON
#12	88 &92	ON	OFF	ON	OFF	OFF
#13	96 & 100	ON	OFF	OFF	ON	ON
#14	104 & 108	ON	OFF	OFF	ON	OFF
#15	112 & 116	ON	OFF	OFF	OFF	ON
#16	120 & 124	ON	OFF	OFF	OFF	OFF
#17	128 & 132	OFF	ON	ON	ON	ON
#18	136 & 140	OFF	ON	ON	ON	OFF
#19	144 & 148	OFF	ON	ON	OFF	ON
#20	152 & 156	OFF	ON	ON	OFF	OFF
#21	160 & 164	OFF	ON	OFF	ON	ON
#22	168 & 172	OFF	ON	OFF	ON	OFF
#23	176 & 180	OFF	ON	OFF	OFF	ON
#24	184 &188	OFF	ON	OFF	OFF	OFF
#25	192 & 196	OFF	OFF	ON	ON	ON
#26	200 & 204	OFF	OFF	ON	ON	OFF
#27	208 & 212	OFF	OFF	ON	OFF	ON
#28	216 & 220	OFF	OFF	ON	OFF	OFF
#29	124 & 228	OFF	OFF	OFF	ON	ON
#30	232 & 236	OFF	OFF	OFF	ON	OFF
#31	240 & 244	OFF	OFF	OFF	OFF	ON
#32	248 & 252	OFF	OFF	OFF	OFF	OFF

This table shows the daisy-chain board address relationship with respect to the 5-bit (SW1) DIP position setting.
Note: ON=CLOSED, OFF=OPEN. To turn "off" a switch, push down on the "open" side. To turn "on" a switch, push down on the "numbered" side.

INPUT AND OUTPUT PORTS

Port A is always configured as an input port, and the output lines are driven by writing to port B. The input and the output lines can be read or written to using TWS type M-variables. Once the correct M-variable definition assignment is done, one may use these M-variables in the usual ways (e.g. motion programs, PLC programs, etc.). Efficient programming techniques for TWS M-variable processing are discussed below.

Jumpers E1 through E8 and E17 through E21 together with the diode packs DP1 to DP4 determine the sinking/sourcing characteristics of the input port (see below). For sourcing a high level on, an input line is read as binary 1 (positive logic). For sinking a high level on, an input line is read as binary 0 (negative logic).

Jumpers E9 through E16 together with drivers U17 through U20 determine the sinking/sourcing characteristic of the output port (see below). For a sourcing setup, writing a binary 1 generates a high level on the corresponding output line (positive logic). For a sinking setup, writing a binary 1 turns on the corresponding open collector transistor output, and this in turn switches on the output (negative logic).

M-VARIABLE ASSIGNMENTS

There is a special format 32-bit wide M-variable for reading the data from, and writing the data to an ACC-34 card: TWS.

Note:

This special M-variable definition is implemented in PMAC's firmware with a version number equal to or higher than 1.13. In version 1.14D, the TWS format was modified in its address designation field to prevent unintentional reads from an output port or unintentional writes to an input port. If your PROM version is between 1.13 to 1.14C, you may request a free PROM update to version 1.14D or above.

```
M{constant}->TWS:{m-plex}      ;Serial Thumbwheel Multiplexer M-
                               ;Variable Definition
```

This command causes PMAC to define the specified M-variable or range of M-variables to point to a 32-bit word of input or output serially multiplexed on the "thumbwheel" port on an Accessory 34x board.

Note:

The individual bits of the "thumbwheel" port on an Accessory 34x board can not be directly assigned to an M-variable. Only 32-bit words (ports) of input or output can be accessed.

The address on the multiplex port specified here must match the address set by the DIP switch on the ACC-34x board. The ACC-34x manual contains a table listing all of the possibilities.

The entire word must either be all input or all output. On power-up/reset, all ACC-34x words are software-configured as inputs (if the hardware is configured for outputs, all outputs will be OFF -- pulled up to the supply voltage). Any subsequent write operation to an I/O word on the port with one of these M-variables automatically makes the entire word an output word with individual bits ON or OFF, as determined by the value written to the word.

Any subsequent read operation of a word that has been set up for output configures, or tries to configure, the entire word into an input word, which turns any hardware outputs OFF. Therefore, it is important that the following rules be observed when working with these M-variables:

Never use this M-variable form to write to a word that is set up for inputs.
Never use this M-variable form to read from a word that is set up for outputs

The best procedure for using TWS M-variables in a program is as follows: The input word (TWS M-variable) should be copied into its image variable at the beginning of a sequence of operations. The operations can then be done on the image variable without requiring PMAC to actually read or write to the I/O port for each operation. The output word is first "assembled" into its image variable, and then copied to the actual output word once at the end of a sequence of operations. This procedure will allow the most efficient and flexible use of TWS M-variables.

Note

This type of variable can only be used in background tasks (PLCs and PLCCs 1-31). They cannot be used in foreground tasks (motion programs and PLC and PLCC 0).

For an input port, **{m-plex}** is a legal byte number (from column 2 of Table 1) plus 1. Any attempt to write to a TWS type M-variable defined with bit zero of its address set to 1, is automatically prevented by PMAC's firmware. For an **output** port, **{m-plex}** is a legal byte number (from column 2 of Table 1) **plus**

2. An attempt to read a TWS type M-variable defined with bit one of its address set to 1, returns zero, and the actual read is prevented by PMAC's firmware.

Note

Individual bits cannot be directly assigned to an M-variable of this type. Rather, banks of 32 bits (ports) can be assigned to M-variables.

Example: To address Port A (bits 0 to 31) of board #1 as an input using M100, use the following definition:

Board #	Byte (Port A & Port B)	5	4	3	2	1
#1	0 & 4	ON	ON	ON	ON	ON

```
M100->TWS:1  ; Port A (AIO 0-31) of an ACC-34 with SW1 switches all ON
             ; assigned for read only (1=0+1)
```

Similarly, to address Port B of the same board #1 as an output using M101, use the following definition:

```
M101->TWS:6  ; Port B (BIO 0-31) of an ACC-34 with SW1 switches all ON
             ; assigned for write only (4+2=6)
```

To address Port A of board #6 as an input using M300, use the following definition:

Board #	Byte(Port A & Port B)	5	4	3	2	1
#6	40 & 44	ON	ON	OFF	ON	OFF

```
M300->TWS:41  ; Port A (AIO 0-31) of an ACC-34 with SW1 switches
              ; assigned for read only (41=40+1)
```

Note

A 32-bit Read or a 32-bit Write to an individual port takes approximately 64 microseconds of time in the PMAC's background time slot. As a result, excessive and unnecessary references to TWS type M-variables is not recommended (see below for efficient ACC-34x I/O processing).

Note

TWS type M-variable definition addresses which point to the base address directly (e.g. **M300->TWS:40**) are still valid (i.e. they do not generate error). However, their use is very strongly discouraged. This is because both reads and writes are enabled when the least significant and the next least significant addresses bits are both zero (e.g. hexadecimal 40 = 01000000 in binary). In this situation, any accidental read of an output port (say via the Executive programs watch window) will cause all the output transistors to be turned off (outputs pulled to the supply voltage)! Alternatively, writing to an input port will automatically reconfigure it to an output port! It is therefore safer and more predictable when bits 0 & 1 of the M-variable definition are intentionally used to disable either the read function or the write function.

PROCESSING ACC-34X INPUTS & OUTPUTS

Because the PMAC interface to the Accessory 34 family of I/O boards (ACC-34x) is by full, 32-bit words transmitted serially (even when access to only a single bit is desired), the user must consider carefully how the interface is done and how frequently. Care must also be taken to work efficiently with the data so that PMAC is not bogged down with slow serial reads and writes, and time-consuming logic to assemble and disassemble I/O words.

The recommended strategy is to keep "images" of each input or output word in PMAC's internal memory, or in the dual-ported RAM. The input words are copied into their image words, and the output words are copied from their image words. Most program operations deal with these image words; this way, slow transfer to or from an ACC-34x board is performed less frequently. During the act of copying, bit inversion can also be performed with the exclusive-or function.

WHEN TO ACCESS ACC-34X

The actual reads and writes for an ACC-34x board can only be done in a background PLC program (PLC 1-31) or through on-line commands, which are executed between PLC programs. Motion programs and PLC 0 cannot directly access this I/O (they can work only with the image words). Reading an input word from an ACC-34x is simply a question of using the TWS-form M-variable for that word on the right side of an equation. Usually, this operation simply copies the input word into its internal image variable. Similarly, writing an output word to an ACC-34x involves using the M-variable for that word on the left side of an equation, typically just copying it from its internal image word.

Most users will treat ACC-34x I/O the same way that a traditional PLC treats its I/O; all of the inputs are read at the beginning of a PLC software scan, and all of the outputs are written to at the end of the scan. In between, all the processing of the variables is done while working with the internal image words. It is possible to make the write operation to the output word conditional on a change in the image word for the output from the previous scan, but the time involved in making the decision and storing each scan's value is about the same as the actual writing to the output.

ACC-34X SETUP

For the purpose of ACC-34x setup, the following example will demonstrate how to utilize 32 inputs and 32 outputs of an ACC-34x. Let us first define three variables that will be used during the ACC-34x I/O procedure.

Actual Word Variable	Variable which is read or written to by ACC-34x & PMAC
Image Word Variable	Variable assigned set equal to (Image) actual word variable
Image Bit Variable	Single bit of image word variable

Image Word Variables

It is best to use fixed-point M-variables as the internal image variables for the I/O words. When this is done, a single M-variable representing the entire I/O word can be used for the copying operation. Then separate M-variables can be used to access individual bits or segments of the image word. Use of these smaller M-variables allows PMAC's efficient firmware to do the masking and logic necessary to pick out portions of the I/O word, rather than slower user program code.

PMAC Location of Image Words

Where should these internal image variables reside in PMAC's memory?

Open Memory Standard PMAC:

For a standard PMAC with no DPRAM on board, the image word will be in an otherwise unused double register in PMAC's own memory. There are several places to find unused registers. There are 16 open registers that are set to zero automatically on power-up at PMAC addresses $0770 to $077F. There are 16 more open registers, whose values are held when power is off at PMAC addresses $07F0 to $07FF. It is possible to use the registers of otherwise unused P and Q-variables for this purpose.

These registers should be accessed with fixed-point M-variables, not floating-point P or Q-variables. A double fixed-point register in PMAC's internal memory is defined by the D format of M-variable (e.g. M61->D:$07F0). This is a 48-bit register (only the low 32 bits will be used). The low 24 bits of the I/O will be in the Y-memory, and the high 8 bits of the I/O will be in the low 8 bits of X-memory.

DPRAM Standard PMAC:

If the system has dual-ported RAM, it is probably best to use a 32-bit register in DPRAM. This way, the host computer always has immediate access to the I/O. In fact, it is possible to use PMAC just as a pass-through between the host computer and the ACC-34x boards, letting the host computer do all the processing. A 32-bit fixed-point register in DPRAM is defined by the DP format of M-variable (e.g. M60-> DP:$DF00). This type of variable occupies the low 16 bits (bits 0 to 15) of PMAC Y-memory, and the low 16 bits of PMAC X-memory at the same address, with the less significant bits in Y-memory. It appears to the host computer as two 16-bit registers at consecutive even addresses, with the less significant bits at the lower address.

Turbo PMAC Location of Image Words

Open Memory Turbo PMAC

For a Turbo PMAC with no DPRAM on board, the image word will be in an unused double register in Turbo PMAC's own memory. There are several places to find unused registers. There are 16 open registers that are automatically set to zero on power-up at Turbo PMAC addresses $0010F0 to $0010FF. Also, it is possible to use the registers of otherwise unused P and Q-variables for this purpose.

These registers should be accessed with fixed-point M-variables, not floating-point P or Q-variables. A double fixed-point register in PMAC's internal memory is defined by the D format of M-variable (e.g. M80->D:$0010F0). This is a 48-bit register (only the low 32 bits will be used). The low 24 bits of the I/O will be in the Y-memory, and the high 8 bits of the I/O will be in the low 8 bits of X-memory.

When working with the ACC-34x I/O with this method of using fixed-point image variables, the only software overhead is the actual copying between image and I/O. Including program interpretation time, this amounts to about 100 microseconds per 32-bit word. Aside from this, working with the I/O through the image words is at least as fast as direct (parallel) PMAC I/O. There is a potential latency of a full PLC scan on the actual I/O, which must be respected. Many systems will have a few critical I/O points that cannot tolerate this latency; these typically use PMAC's JOPTO port or ACC-14 I/O for these time-critical points, then use ACC-34x for I/O that do not need to be so fast.

DPRAM Standard Turbo PMAC

If the system has dual-ported RAM (Option 2 is required), it is probably best to use a 32-bit register in DPRAM. This way, the host computer always has immediate access to the I/O. In fact, it is possible to use PMAC just as a pass-through between the host computer and the ACC-34x boards, letting the host computer do all the processing. A 32-bit fixed-point register in DPRAM is defined by the DP format of M-variable (e.g. M80-> DP:$060000). This type of variable occupies the low 16 bits (bits 0 to 15) of PMAC Y-memory, and the low 16 bits of PMAC X-memory at the same address, with the less significant bits in Y-memory. It appears to the host computer as two 16-bit registers at consecutive even addresses, with the less significant bits at the lower address.

Preventing Conflicts in Output Image Words

Care must be taken if tasks of different priority levels are trying to write to the same output image word, or if both the host computer and PMAC are trying to write to the same DPRAM output image word. If the proper techniques are not used, occasional output changes will not be executed, and because of the intermittent nature of the problem, it will be very difficult to diagnose. If the application has two priority levels or two computers that write to the same ACC-34x output word, separate partial image words must be used. These words combined as the output word is sent.

Note

There is no conflict in having different tasks or different processors read from the same input word.

Remember that a computer cannot actually write to less than a word of memory at a time, even if it only wants to change one bit. In PMAC the word length is 24 bits; for the DPRAM, it is 16 bits. If a computer wants to change less than a full word, it must read the full word, modify the bits it wants with "mask words", then write back the full word.

There are two priority levels in PMAC that can write to these image words: the foreground level, which includes all of the motion programs and PLC 0; and the background level, which includes PLCs 1-31 and on-line commands. The problem can occur when a higher priority task interrupts a lower priority task that is in the middle of changing the image word with a read-modify-write operation. When the lower priority task resumes, it will undo the changes made by the higher priority task. Similarly, if the image word is in the DPRAM, and one side starts its read-modify-write cycle on the word but does not finish it before the other side starts its own cycle, the side that starts later can undo the changes made by the side that starts first.

Note

Two tasks at the same priority level cannot interrupt each other; one will always finish an operation before the other starts. Therefore, there is no need to worry about two motion programs writing to the same image word; or a motion program and PLC 0; because these tasks are at the same priority level. Similarly, there is no need to worry about two background PLC programs writing to the same image word, or a background PLC and on-line commands.)

To prevent this possible conflict, the different priority levels or different processors must use different image words, even if they each represent only a part of the same total output word. These partial words are then combined in the act of writing to the actual output word.

The simplest way to split an image word is to use the natural X-memory vs. Y-memory split in PMAC's memory. If you are using a double word in PMAC's internal memory, you can reserve the 24 bits in Y-memory for one priority level, and the 8 bits in X-memory for the other. If you are using the DPRAM, you can reserve the 16 bits in Y-memory for one processor or priority level, and the 16 bits in X-memory for another. If you do this, no special techniques need to be used. On PMAC, simply write to the partial words with a X or Y format M-variable; PMAC will automatically do the read-modify-write cycle without touching the other part of the word. On the host computer, access the DPRAM register with the short (16-bit) integer format, not the long.

However, if you cannot arrange your split in this fashion, you must create separate "overlapping" image words and explicitly combine them.

Example: Take a system where the low 12 bits will be written to by background PLCs and the high 20 bits will be written to by motion programs. Create two separate image words: one for each priority level, and the actual output word:

PMAC	Turbo PMAC	Comments
M101->D:$0770	M81->D:$0010F0	; Image word for PLC programs (background)
M102->D:$0771	M82->D:$0010F1	; Image word for motion programs (foreground)
M103->TWS:6	M83->TWS:6	; ACC-34x output word; write-only

We also define single-bit M-variables to parts of these same internal addresses: at Y:$0770 ($0010F0 for Turbo), bits 0 to 11 for the PLCs; then at Y:$0771($0010F1 for Turbo), bits 12 to 23, and X:$0771($0010F1 for Turbo), bits 0 to 7 for the motion programs. At the end of a PLC scan, to create the actual output word on an ACC-34x from the image words, we would use the program statement:

```
M103 = (M101 & $00000FFF) | (M102 & $FFFFF000)
```

The bit-by-bit AND (&) operations make sure no falsely set bits in unused portions of the image words get into the output word. They are not strictly necessary if the unused bits can be guaranteed to be zero. The bit-by-bit OR (|) operation combines the word. The assignment of the resulting value to M103 causes it to be written to the ACC-34x.

If you want to be able to write to the same bit of an output image word with two different priority levels or processors, one of the tasks must do so indirectly by writing into a holding register. The other task must take this holding register and transfer the bit value into the image word. This task must decide what to do in case of any conflict (i.e. one task wants to clear the bit, and the other wants to set it).

The following example illustrates the method of working with ACC-34x I/O. It describes the procedure for memory allocation, for the inputs, and for the outputs (Image Word Variables) that will work with either Dual Ported RAM or PMAC memory locations

Example: This example shows the image variables both in DPRAM and several places in internal memory. In a real application, a single location range would probably be chosen.

Set-up and Definitions: ; Actual ACC-34 I/O Words

```
M1000->TWS:1      ; First side of first ACC-34x board; an input here
                  ; Location is at port address 0; added 1 for read only

M1002->TWS:6      ; Second side of first ACC-34x board; an output here
                  ; Location is at port address 4 added 2 for write only

M1004->TWS:9      ; First side of second ACC-34x board; an input here
                  ; Location is at port address 8; added 1 for read only

M1006->TWS:14     ; Second side of second ACC-34x board; an output here
                  ; Location is at port address 12; added 2 for write
                  ; only
```

Image Words

PMAC	Turbo PMAC	Comments
M1001->DP:$D800	M1001->DP:$060800	; 32-bit fixed-point DPRAM register
M1003->D:$0770	M1003->D:$0010F0	; 48-bit fixed-point register, set to zero on ; power-up
M1005->D:$07F0	* Power-down hold registers are not available in Turbo PMAC M1005->D:$0061F0	; PMAC: 48-bit fixed-point register, value held ; through power-down ; Turbo PMAC: use this register for P-variable, ; treated as 48-bit fixed point value
M1007->D:$13FF	M1007->D:$0063FF	; Register for P1023, treated as 48-bit ; fixed-point value
* User Buffer Storage Space is same for the battery backed Turbo PMAC.		

Individual Pieces of Image Words

For PMAC Memory Locations

Port A Setup: Read Only		
PMAC	**Turbo PMAC**	**Comments**
M1000->TWS:1	M1000->TWS:1	Port A (AIO 0-31)
M1001->D:$770	M1003->D:$0010F0	Image word for PLC's
M800->Y:$770,0	M800->Y:$0010F0,0	Bit0 (LSB)
M801->Y:$770,1	M801->Y:$0010F0,1	Bit1
M802->Y:$770,2	M802->Y:$0010F0,2	Bit2
M822->Y:$770,22	M822->Y:$0010F0,22	Bit22
M823->Y:$770,23	M823->Y:$0010F0,23	Bit23
M824->X:$770,0	M824->X:$0010F0,0	Bit24
M825->X:$770,1	M825->X:$0010F0,1	Bit25
M830->X:$770,6	M830->X:$0010F0,6	Bit30
M831->X:$770,7	M831->X:$0010F0,7	Bit31 (MSB)
Port B Setup: Write Only		
PMAC	Turbo PMAC	Comments
M1002->TWS:6	M1002->TWS:6	Port B (BIO 0-31)
M1003->D:$771	M1003->D:$0010F1	Image word for PLC's
M900->Y:$771,0	M900->Y:$0010F1,0	Bit0 (LSB)
M901->Y:$771,1	M901->Y:$0010F1,1	Bit1
902->Y:$771,2	M902->Y:$0010F1,2	Bit2

922->Y:$771,22	M922->Y:$0010F1,22	Bit22
923->Y:$771,23	M923->Y:$0010F1,23	Bit23
924->X:$771,0	M924->X:$0010F1,0	Bit24
925->X:$771,1	M925->X:$0010F1,1	Bit25
M930->X:$771,6	M930->X:$0010F1,6	Bit30
M931->X:$771,7	M931->X:$0010F1,7	Bit31 (MSB)

For PMAC Dual Ported RAM Locations

Port A Setup: Read Only		
PMAC	**Turbo PMAC**	**Comments**
M1000->TWS:1	M1000->TWS:1	Port A (AIO 0-31)
M1001->DP:$D800	M1001->DP:$060800	Image word for PLC's
M800->Y:$D800,0	M800->Y:$060800,0	Bit0 (LSB)
M801->Y:$D800,1	M801->Y:$060800,1	Bit1
M802->Y:$D800,2	M802->Y:$060800,2	Bit2
M814->Y:$D800,14	M814->Y:$060800,14	Bit14
M815->Y:$D800,15	M815->Y:$060800,15	Bit15
M816->X:$D800,0	M816->X:$060800,0	Bit16
M817->X:$D800,1	M817->X:$060800,1	Bit17
M830->X:$D800,14	M830->X:$060800,14	Bit30
M831->X:$D800,15	M831->X:$060800,15	Bit31 (MSB)
Port B Setup: Write Only		
PMAC	**Turbo PMAC**	**Comments**
M1002->TWS:6	M1002->TWS:6	Port B (BIO 0-31)
M1003->DP:$D801	M1003->DP:$060801	Image word for PLC's
M900->Y:$D801,0	M900->Y:$060801,0	Bit0 (LSB)
M901->Y:$D801,1	M901->Y:$060801,1	Bit1
M902->Y:$D801,2	M902->Y:$060801,2	Bit2
M914->Y:$D801,14	M914->Y:$060801,14	Bit14
M915->Y:$D801,15	M915->Y:$060801,15	Bit15
M916->X:$D801,0	M916->X:$060801,0	Bit16
M917->X:$D801,1	M917->X:$060801,1	Bit17
M930->X:$D801,14	M930->X:$060801,14	Bit30
M931->X:$D801,15	M931->X:$060801,15	Bit31 (MSB)

Programs:

```
; "Reset" PLC program that only runs once on power-up or reset

OPEN PLC 1 CLEAR
M1003=0            ; Clear output image word to make sure all outputs off
M1007=0            ; Ditto
...
DISABLE PLC 1      ; To make sure this only runs once on power-up/reset
CLOSE

                   ;PLC program to copy the inputs into image words at
          beginning of each scan
OPEN PLC 2 CLEAR
M1001=M1000              ; Copy first input word into its image register
M1005=M1004^$FFFFFFFF    ; Copy second input word into its image register,
                                                        ; inverting
...
```

```
CLOSE

                    ; PLC program that works with individual bits of image
                   words
OPEN PLC 3 CLEAR
IF (M100=1 AND M101=0 AND P43>50)
    M301=1
ELSE
    M301=0
ENDIF
...
CLOSE

                       ;  PLC program that copies image words to outputs at end
                   of scan
OPEN PLC 31 CLEAR
M1002=M1003             ; Copy first output image word to ACC-34x
M1004=M1005^$FFFFFFFF   ; Copy second output image word to ACC-34x, inverting
```

USING ACC-34 WITH MACRO STATION

Two ACC-34's could be used at each MACRO Station in the ring. The MACRO Station has eight variables used for this purpose: MI90, MI91, MI92, MI93, MI94, MI95, MI96, and MI97. Each ACC-34 Port has two variables associated with it. The first variable is the multiplexer port address, and the second is the actual input or output word. To read or write to these variables, special MACRO Station read and write commands (buffered and on-line) can be used to read and write to and from the Ultralite or Turbo Ultralite.

Port Address	Actual Word	Type
MI90	MI91	Input – Read Only
MI92	MI93	Output – Write Only
MI94	MI95	Input – Read Only
MI96	MI97	Output – Write Only

These variables are implemented on MACRO Station firmware versions V1.111 and newer.

Example: The user wants two ACC-34AAs connected to the multiplexer port on the MACRO station for 128-bits of I/O. The SW1 settings for the boards in this example are shown below.

Board #	Byte (Port A & Port B)	5	4	3	2	1
#1	0 & 4	ON	ON	ON	ON	ON
#2	8 & 12	ON	ON	ON	ON	OFF

Based on the switch settings, the port address settings would be:

```
MSn,   MI90=1          ; Port A Board 1
MSn,   MI92=6          ; Port B Board 1
MSn,   MI94=9          ; Port A Board 2
MSn,   MI96=14         ; Port B Board 2
```

The user could then read and write from and to the MACRO station using the following definitions and commands:

PMAC Ultralite	Turbo PMAC Ultralite	Comments
M1000->D:$07F0	M1000->D:$0061F0	; input image word for ; Ultralite ; board 1
M1001->D:$07F1	M1001->D:$0061F1	; output image word for ; Ultralite board 1
M1002->D:$07F2	M1002->D:$0061F2	; input image word for ; Ultralite board 2
M1003->D:$07F3	M1003->D:$0061F3	; output image word for ; Ultralite board 2

The following commands could be used as either on-line commands for testing, or they could be used in your PLC or motion program as buffer commands:

```
MSRn, MI91, M1000       ; Reads the value of MSn, MI91 to M1000
MSWn, MI93, M1001       ; Writes the value of M1001 to MSn, MI93
MSRn, MI95, M1002       ; Reads the value of MSn, MI95 to M1002
MSRn, MI97, M1003       ; Reads the value of M1003 to MSn, MI97
```

MS{anynode},MI90: Multiplexer Port #1 Read Address

Range: $00 - $FF
Units: MACRO Station Multiplexer Port Addresses
Default: $00

MI90 specifies the address on the MACRO Station's JTHW multiplexer port of a 32-bit input port on an ACC-34 family I/O board. If MI90 is set greater than 0, the 32 input values will be copied periodically into Station variable MI91. MI90 must match the multiplexer port address of the ACC-34 board from which the inputs are to be read, as set by the SW1 DIP switch bank on the board. For the regular input port, the value of MI90 should be set 1 greater than the base address of the board set by the DIP switch bank. For the ACC-34C's optional second 32-bit input port, the value of MI94 should be set 3 greater than the base address.

MS{anynode},MI91: Multiplexer Port #1 Read Value

Range: $00000000 - $FFFFFFFF
Units: Individual bits

MI91 contains the 32-bit value read from the input port of the ACC-34 whose multiplexer port address is specified by MI90. Each bit represents one input from the port. Bit n of MI91 represents Input n on the port.

MS{anynode},MI92: Multiplexer Port #1 Write Address

Range: $00 - $FF
Units: MACRO Station Multiplexer Port Addresses
Default: $00

MI92 specifies the address on the MACRO Station's JTHW multiplexer port of a 32-bit output port on an ACC-34 family I/O board. If MI92 is set greater than 0, the 32 output values will be copied periodically from Station variable MI93. MI92 must match the multiplexer port address of the ACC-34 board from which the inputs are to be read, as set by the SW1 DIP switch bank on the board. The value of MI92 should be set 6 greater than the base address of the board set by the DIP switch bank.

MS{anynode},MI93: Multiplexer Port #1 Write Value

Range: $00000000 - $FFFFFFFF
Units: Individual bits

MI93 contains the 32-bit value written to the output port of the ACC-34 whose multiplexer port address is specified by MI92. Each bit represents one output on the port. Bit n of MI93 represents Output n on the port.

MS{anynode},MI94: Multiplexer Port #2 Read Address

Range: $00 - $FF
Units: MACRO Station Multiplexer Port Addresses
Default: $00

MI94 specifies the address on the MACRO Station's JTHW multiplexer port of a 32-bit input port on an ACC-34 family I/O board. If MI94 is set greater than 0, the 32 input values will be copied periodically into Station variable MI95. MI94 must match the multiplexer port address of the ACC-34 board from which the inputs are to be read, as set by the SW1 DIP switch bank on the board. For the regular input port, the value of MI94 should be set 1 greater than the base address of the board set by the DIP switch bank. For the ACC-34C's optional second 32-bit input port, the value of MI94 should be set 3 greater than the base address.

MS{anynode},MI95: Multiplexer Port #2 Read Value

Range: $00000000 - $FFFFFFFF
Units: Individual bits

MI95 contains the 32-bit value read from the input port of the ACC-34 whose multiplexer port address is specified by MI94. Each bit represents one input from the port. Bit n of MI95 represents Input n on the port.

MS{anynode},MI96: Multiplexer Port #2 Write Address

Range: $00 - $FF
Units: MACRO Station Multiplexer Port Addresses
Default: $00

MI96 specifies the address on the MACRO Station's JTHW multiplexer port of a 32-bit output port on an ACC-34 family I/O board. If MI96 is set greater than 0, the 32 output values will be copied periodically from Station variable MI97. MI96 must match the multiplexer port address of the ACC-34 board from which the inputs are to be read, as set by the SW1 DIP switch bank on the board. The value of MI96 should be set 6 greater than the base address of the board set by the DIP switch bank.

MS{anynode},MI97: Multiplexer Port #1 Write Value

Range: $00000000 - $FFFFFFFF
Units: Individual bits

MI97 contains the 32-bit value written to the output port of the ACC-34 whose multiplexer port address is specified by MI96. Each bit represents one output on the port. Bit n of MI97 represents Output n on the port.

POWER SUPPLY AND OPTO-ISOLATION CONSIDERATIONS

The power for the PMAC processor side of the opto-isolation circuitry is brought in directly from J1 (JTHW). The power for the external side of the opto-isolation circuitry should be from a separate supply brought in through TB9. This can be any level from 12 V to 24 V. The current requirements for the power brought in through TB9 is approximately 0.4 A at 24 volts or 0.8 A at 12 V.

For TB1 to TB4 inputs the power supply for the 3.3 Kς pull-up resistors can range from 15 to 24 volts. At 24 volts the current requirement is approximately 70 mA.

For TB5 to TB7 outputs in the sourcing configuration the supply voltage may range from 12 to 24V. The maximum current requirement should be limited to 100 mA per output line, which translates to 800 mA per terminal block. For sinking configurations, the supply voltage may range between 12 and 24 V (the maximum current is limited to that which flows through the nine 3.3 Kς pull-up resistors (approx. 70 mA).

ACC-34A and Its Option 1 (Custom Order)

The default configuration of ACC-34A populates the board with UDN2981 for output sourcing drivers. All jumpers and diode packs are set up for sourcing configuration on all inputs and outputs. We recommend the use of the Accessory 34 (not 34A) for an all-sinking configuration. If it is desired to mix sourcing and sinking I/Os, then ACC-34A should be order with its option 1. To order ACC-34A Option 1, the enclosed order form must be filled up and sent to the factory. Customizing (mixing sourcing and sinking I/O lines) may be accomplished in groups of eight input lines and eight output lines. The following tables indicate jumper, diode pack and chip modifications required for each group.

Output Configuration

Output Group[1]	Sourcing[2]			Sinking		
	Output driver	**Jumpers**	**Diode Pack**	**Output driver**	**Jumpers**	**Diode Pack**
O1 (TB5) BO0-7	U17 is UDN2981	E9 pin 2 to 3 E10 pin 2 to 3	DP5 Reversed[3]	U17 is ULN2803	E9 pin 2 to1 E10 pin 2 to 1	DP5
O2 (TB6) BO8-15	U18 is UDN2981	E11 pin 2 to 3 E12 pin 2 to 3	DP6 Reversed[3]	U18 is ULN2803	E11 pin 2 to 1 E12 pin 2 to 1	DP6
O3 (TB7) BO16-23	U19 is UDN2981	E13 pin 2 to 3 E14 pin 2 to 3	DP7 Reversed 3	U19 is ULN2803	E13 pin 2 to1 E14 pin 2 to 1	DP7
O4 (TB8) BO24-31	U20 is UDN2981	E15 pin 2 to 3 E16 pin 2 to 3	DP8 Reversed[3]	U20 is ULN2803	E15 pin 2 to 1 E16 pin 2 to 1	DP8

1 The 32-bit outputs are made up of 4 groups. Each output group consists of 8 bits that correspond to lines driven through TB5 to TB8.

2 Default configuration is for *all* sourcing outputs. Order ACC-34A with Opt. 1 if one or more sinking groups of outputs are needed. This requires sending a custom order form to factory.

3 "Reversed" diode pack means pin #1 of the corresponding LED pack must be positioned on pin #11 of socket. This is required for sourcing configuration and is installed by factory for the default setup of ACC-34A.

Input Configuration

Input Group[1]	Sourcing[2]		Sinking	
	Jumpers	**Diode Pack**	**Jumpers**	**Diode Pack**
I1 (TB1) AI0-7	E1 pin 2 to 3 E2 pin 2 to 3	DP1 Reversed[3]	E1 pin 2 to 1 E2 pin 2 to 1	DP1
I2 (TB2) AI8-15	E3 pin 2 to 3 E4 pin 2 to 3	DP2 Reversed[3]	E3 pin 2 to 1 E4 pin 2 to 1	DP2
I3 (TB3) AI16-23	E5 pin 2 to 3 E6 pin 2 to 3	DP3 Reversed[3]	E5 pin 2 to 1 E6 pin 2 to 1	DP3
I4 (TB4) AI24 -31	E7 pin 2 to 3 E8 pin 2 to 3	DP4 Reversed[3]	E7 pin 2 to 1 E8 pin 2 to 1	DP4

[1] The 32-bit inputs are made up of 4 groups. Each input group consists of 8 bits that correspond to lines driven through TB1 to TB4.

[2] The default configuration is for *all* sourcing inputs. Order ACC-34A with Opt. 1 if one or more sinking groups of outputs are needed. This requires sending a custom order form to factory.

[3] "Reversed" diode pack means pin #1 of the corresponding LED pack must be positioned on pin #11 of socket. This is required for sourcing configuration and is installed by factory for the default setup of ACC-34A.

In addition to the above jumpers, E17 to E21 must be set correctly according to the type of input required. This is shown in the table below.

Input Polarity Jumpers Setup

Input Type Group (Sinking or Sourcing)				Jumper Setup				
I1 (AI0-7)	**I2 (AI8- 15)**	**I3 (AI16-23)**	**I4 (AI24-31)**	**E17**	**E18**	**E19**	**E20**	**E21**
Source*	Source*	Source*	Source*	2 to 3*	2 to 1*	2 to 1*	2 to 1*	2 to 3*
Source	Source	Source	Sink	2 to 3	2 to 1	2 to 1	2 to 3	2 to 1
Source	Source	Sink	Source	2 to 3	2 to 1	2 to 3	2 to 3	2 to 3
Source	Source	Sink	Sink	2 to 3	2 to 1	2 to 3	2 to 1	2 to 1
Source	Sink	Source	Source	2 to 3	2 to 3	2 to 3	2 to 1	2 to 3
Source	Sink	Source	Sink	2 to 3	2 to 3	2 to 3	2 to 3	2 to 1
Source	Sink	Sink	Source	2 to 3	2 to 3	2 to 1	2 to 3	2 to 3
Source	Sink	Sink	Sink	2 to 3	2 to 3	2 to 1	2 to 1	2 to 1
Sink	Source	Source	Source	2 to 1	2 to 3	2 to 1	2 to 1	2 to 3
Sink	Source	Source	Sink	2 to 1	2 to 3	2 to 1	2 to 3	2 to 1
Sink	Source	Sink	Source	2 to 1	2 to 3	2 to 3	2 to 3	2 to 3
Sink	Source	Sink	Sink	2 to 1	2 to 3	2 to 3	2 to 1	2 to 1
Sink	Sink	Source	Source	2 to 1	2 to 1	2 to 3	2 to 1	2 to 3
Sink	Sink	Source	Sink	2 to 1	2 to 1	2 to 3	2 to 3	2 to 1
Sink	Sink	Sink	Source	2 to 1	2 to 1	2 to 1	2 to 3	2 to 3
Sink	Sink	Sink	Sink	2 to 1	2 to 1	2 to 1	2 to 1	2 to 1

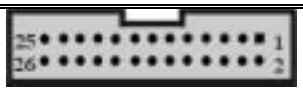
* This is the default factory setup. Any other combination is designated as Option 1 (Custom order). Also see the enclosed Option 1 order form.

Watch Dog Timer (Role of Jumper E22)

ACC-34A has a local watchdog timer which is enabled unless the jumper E22 is removed (In the default factory setup, this jumper is installed). A 1.5 second period watchdog timer circuitry is enabled on ACC-34A when jumper E22 is installed. When the timer is enabled if PMAC (either through a PLC program or a motion program) does not reads from or writes to the ACC-34A board at least once per 1.5 seconds, the watchdog timer trips. When this occurs, the output transistors are turned OFF (no current is driven on any of the 32 outputs). A subsequent read or write always re-initializes the board.

CONNECTOR PINOUTS

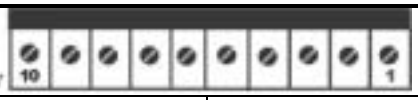
J1 (26-Pin Header)

Top View 

Pin #	Symbol	Function	Description	Notes
1	GND	Common	PMAC Common	
2	GND	Common	PMAC Common	
3	DAT0	Output	Data Bit 0	
4	SEL0	Input	Address Line 0	
5	DAT1	Output	Data Bit 1	Not connected
6	SEL 1	Input	Address Line 1	
7	DAT2	Output	Data Bit 2	Not connected
8	SEL2	Input	Address Line 2	
9	DAT3	Output	Data Bit 3	Not connected
10	SEL3	Input	Address Line 3	
11	DAT4	Output	Data Bit 4	Not connected
12	SEL 4	Input	Address Line 4	
13	DAT5	Output	Data Bit 5	Not connected
14	SEL5	Input	Address Line 5	
15	DAT6	Output	Data Bit 5	Not connected
16	SEL6	Input	Address Line 6	
17	DAT7	Output	Data Bit 6	Not connected
18	SEL7	Input	Data Bit 7	
19	N.C.			Not connected
20	GND	Common	PMAC Common	
21	N.C.			Not connected
22	GND	Common	PMAC Common	
23	N.C.			Not connected
24	GND	Common	PMAC Common	
25	+5V	Input	+5V DC Supply	
26	N.C.			Not connected

This header should be connected to PMAC's J3 (JTHW) via the supplied 26-pin flat cable.

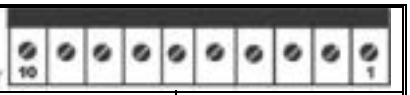
TB1 (10-pin Terminal Block)

Top View 

Pin #	Symbol	Function	Description	Notes
1	AI0	Input	Port A Bit 0	
2	AI1	Input	Port A Bit 1	
3	AI2	Input	Port A Bit 2	
4	AI3	Input	Port A Bit 3	
5	AI4	Input	Port A Bit 4	
6	AI5	Input	Port A Bit 5	
7	AI6	Input	Port A Bit 6	
8	AI7	Input	Port A Bit 7	
9	AGND	I/O Common	Return Signal	
10	AV+1	I/O Supply	15 to 24 Volts	*

* Used only for the ten 3.3kç pull-up/down resistors and LEDs (15 to 24V,70MA).

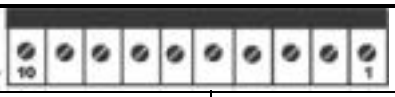
TB2 (10-pin Terminal Block)

Top View 

Pin #	Symbol	Function	Description	Notes
1	AI8	Input	Port A Bit 8	
2	AI9	Input	Port A Bit 9	
3	AI10	Input	Port A Bit 10	
4	AI11	Input	Port A Bit 11	
5	AI12	Input	Port A Bit 12	
6	AI13	Input	Port A Bit 13	
7	AI14	Input	Port A Bit 14	
8	AI15	Input	Port A Bit 15	
9	AGND	I/O Common	Return Signal	
10	AV+2	I/O Supply	15 to 24 Volts	*

* Used only for the ten 3.3kς pull-up/down resistors and LEDs (15 to 24V, 70 mA).

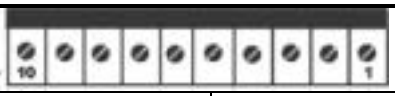
TB3 (10-Pin Terminal Block)

Top View 

Pin #	Symbol	Function	Description	Notes
1	AI16	Input	Port A Bit 16	
2	AI17	Input	Port A Bit 17	
3	AI18	Input	Port A Bit 18	
4	AI19	Input	Port A Bit 19	
5	AI20	Input	Port A Bit 20	
6	AI21	Input	Port A Bit 21	
7	AI22	Input	Port A Bit 22	
8	AI23	Input	Port A Bit 23	
9	AGND	I/O Common	Return Signal	
10	AV+3	I/O Supply	15 to 24 Volts	*

* Used only for the ten 3.3kς pull-up/down resistors and LEDs (15 to 24V, 70 mA).

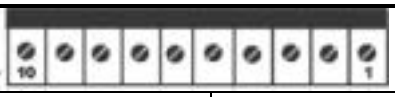
TB4 (10-Pin Terminal Block)

Top View 

Pin #	Symbol	Function	Description	Notes
1	AI24	Input	Port A Bit 24	
2	AI25	Input	Port A Bit 25	
3	AI26	Input	Port A Bit 26	
4	AI27	Input	Port A Bit 27	
5	AI28	Input	Port A Bit 28	
6	AI29	Input	Port A Bit 29	
7	AI30	Input	Port A Bit 30	
8	AI31	Input	Port A Bit 31	
9	AGND	I/O Common	Return Signal	
10	AV+4	I/O Supply	15 to 24 Volts	

* Used only for the ten 3.3kς pull-up/down resistors and LEDs (15 to 24V, 70 mA)

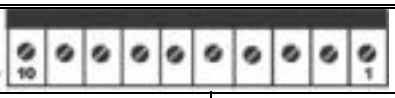
TB5 (10-Pin Terminal Block)

Top View 

Pin #	Symbol	Function	Description	Notes
1	BO0	Output	Port B Bit 0	
2	BO1	Output	Port B Bit 1	
3	BO2	Output	Port B Bit 2	
4	BO3	Output	Port B Bit 3	
5	BO4	Output	Port B Bit 4	
6	BO5	Output	Port B Bit 5	
7	BO6	Output	Port B Bit 6	
8	BO7	Output	Port B Bit 7	
9	AGND	I/O Common	Return Signal	
10	AV+5	I/O Supply	12 to 24 Volts	*

* In the sourcing configuration, this supply will be used to drive the loads on all eight lines (up to 800 mA maximum at 24V). In the sinking configuration, the current requirement from this power supply is minimal (approx. 70 mA).

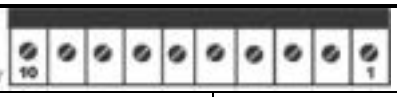
TB6 (10-Pin Terminal Block)

Top View 

Pin #	Symbol	Function	Description	Notes
1	BO8	Output	Port B Bit 8	
2	BO9	Output	Port B Bit 9	
3	BO10	Output	Port B Bit 10	
4	BO11	Output	Port B Bit 11	
5	BO12	Output	Port B Bit 12	
6	BO13	Output	Port B Bit 13	
7	BO14	Output	Port B Bit 14	
8	BO15	Output	Port B Bit 15	
9	AGND	I/O Common	Return Signal	
10	AV+6	I/O Supply	12 to 24 Volts	*

* In the sourcing configuration, this supply will be used to drive the loads on all eight lines (up to 800 mA maximum at 24V). In the sinking configuration, the current requirement from this power supply is minimal (approx. 70 mA).

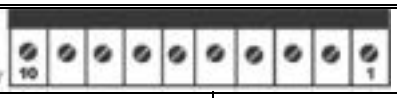
TB7 (10-Pin Terminal Block)



Pin #	Symbol	Function	Description	Notes
1	BO16	Output	Port B Bit 16	
2	BO17	Output	Port B Bit 17	
3	BO18	Output	Port B Bit 18	
4	BO19	Output	Port B Bit 19	
5	BO20	Output	Port B Bit 20	
6	BO21	Output	Port B Bit 21	
7	BO22	Output	Port B Bit 22	
8	BO23	Output	Port B Bit 23	
9	AGND	I/O Common	Return Signal	
10	AV+7	I/O Supply	12 to 24 Volts	*

* In the sourcing configuration this supply will be used to drive the loads on all eight lines (up to 800 mA maximum at 24V). In the sinking configuration, the current requirement from this power supply is minimal (approx. 70 mA).

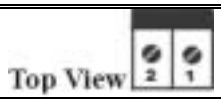
TB8 (10-Pin Terminal Block)



Pin #	Symbol	Function	Description	Notes
1	BO24	Output	Port B Bit 24	
2	BO25	Output	Port B Bit 25	
3	BO26	Output	Port B Bit 26	
4	BO27	Output	Port B Bit 27	
5	BO28	Output	Port B Bit 28	
6	BO29	Output	Port B Bit 29	
7	BO30	Output	Port B Bit 30	
8	BIO31	Output	Port B Bit 31	
9	AGND	I/O Common	Return Signal	
10	AV+8	I/O Supply	5 to 24 Volts	*

* In the sourcing configuration, this supply will be used to drive the loads on all eight lines (up to 800 mA maximum at 24V). In the sinking configuration, the current requirement from this power supply is minimal (approx. 70 mA).

TB9 (2-Pin Terminal Block)



Pin #	Symbol	Function	Description	Notes
1	AGND	Common	External Supply Ground	
2	A+24V	Power Supply	External Supply for Opto-Isolators	12V to 24 V Unregulated

TB9 is a 2-pin terminal block used to bring in the power supply (12-24V) for the I/O side of the opto-isolation circuitry. For proper operation of the board, this power supply must be brought in through TB9.

PMAC ACC-34A OPTION 1 (CUSTOM ORDER) FORM

This form must be completed for mixing sourcing and sinking I/Os on the Opto 32 bit Input/ 32 bit Output board (ACC-34A):

Please check one entry in each row:

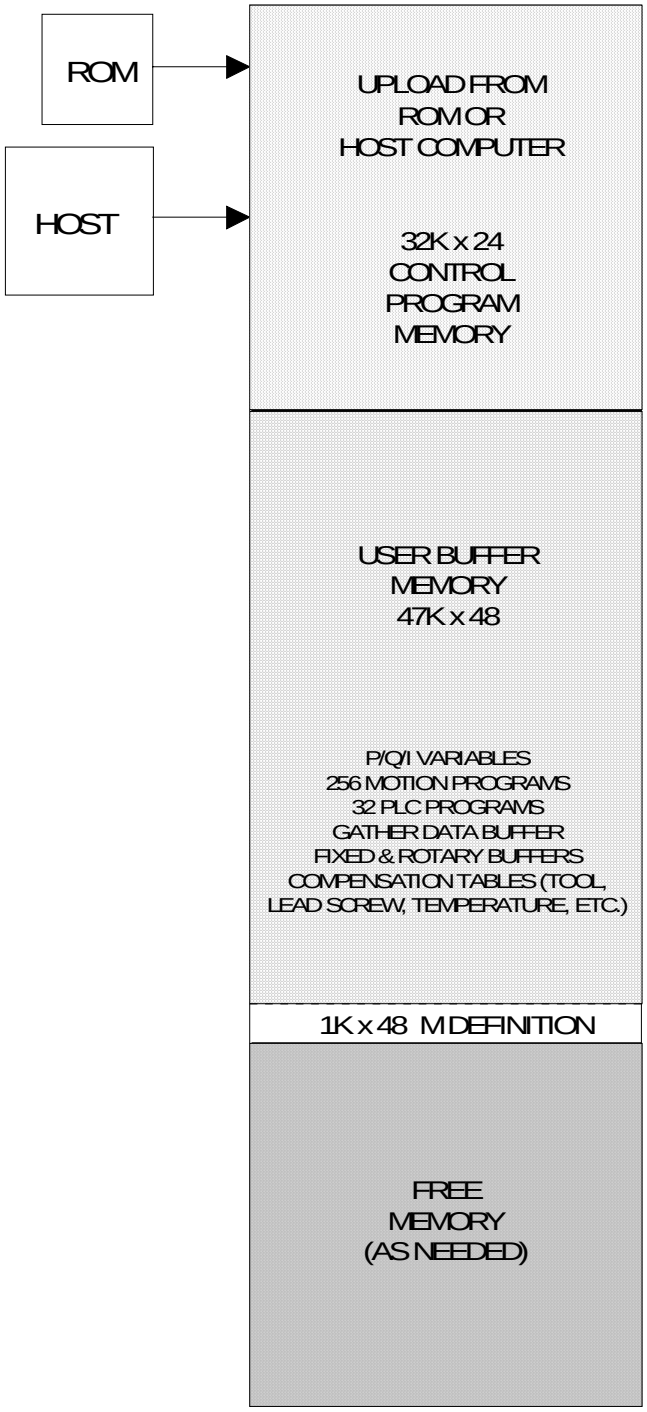
Input/Output Terminals	**Check Appropriate Row for *Sourcing* Configuration**	**Check Appropriate Row for *Sinking* Configuration**
I1 (TB1) AI0-7		
I2 (TB2) AI8-15		
I3 (TB3) AI16-23		
I4 (TB4) AI24-31		
O1 (TB5) BO0-7		
O2 (TB6) BO8-15		
O3 (TB7) BO16-23		
O4 (TB8) BO24-31		

Example: Suppose it is desired to have O1 sinking O2, O3 and O4 sourcing and I2 sinking with I1 ,I3 and I4 sourcing. For this example the above table should be filled as shown below:

Input/Output Terminals	**Check Appropriate Row for Sourcing Configuration**	**Check Appropriate Row for Sinking Configuration**
I1 (TB1) AI0-7	√	
I2 (TB2) AI8-15		√
I3 (TB3) AI16-23	√	
I4 (TB4) AI24-31	√	
O1 (TB5) BO0-7		√
O2 (TB6) BO8-15	√	
O3 (TB7) BO16-23	√	
O4 (TB8) BO24-31	√	

DIAGRAMS

PMAC Memory



ROM = 128K x 8

EAROM = 2K x 8
Stores I Parameters only

RAM = 128K X 24
Battery Backed
Program, X & Y Memory

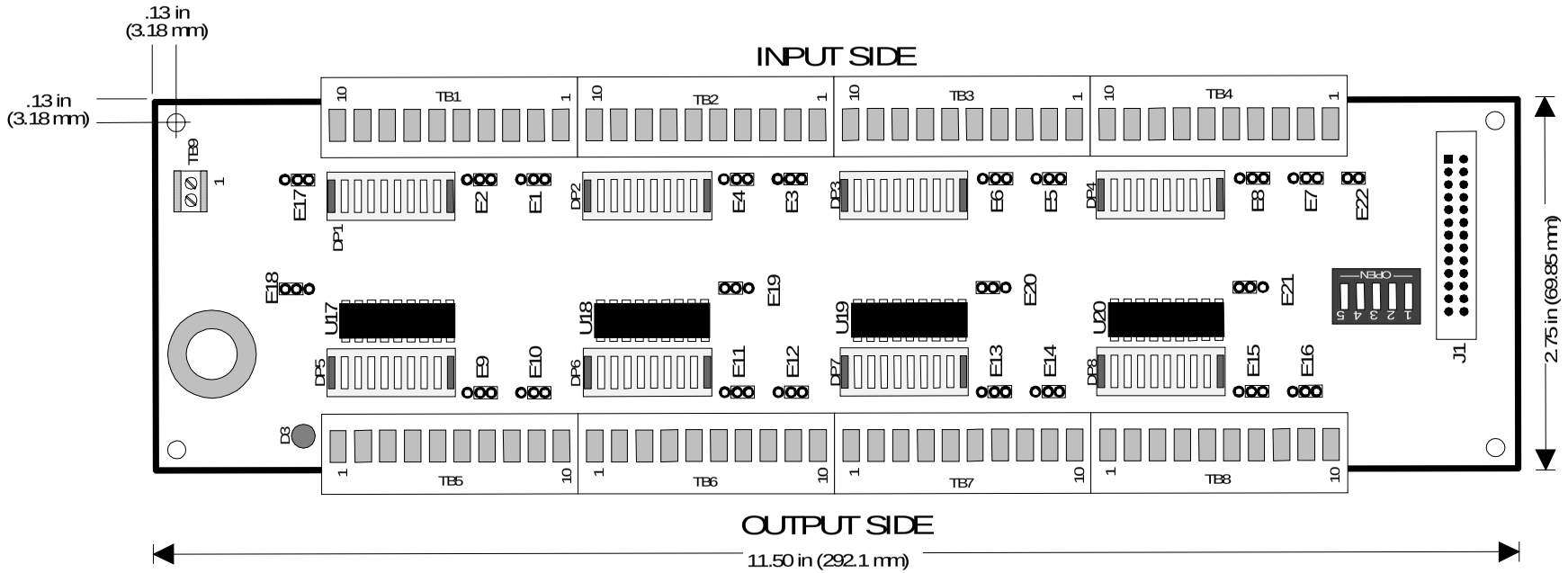
RAM:
NORMAL: 65 nsecs
1 WAIT STATE/20 MHz

MEDIUM: 45 nsecs
0 WAIT STATE/20 MHz

FAST: 25 nsecs
0 WAIT STATE/30 MHz

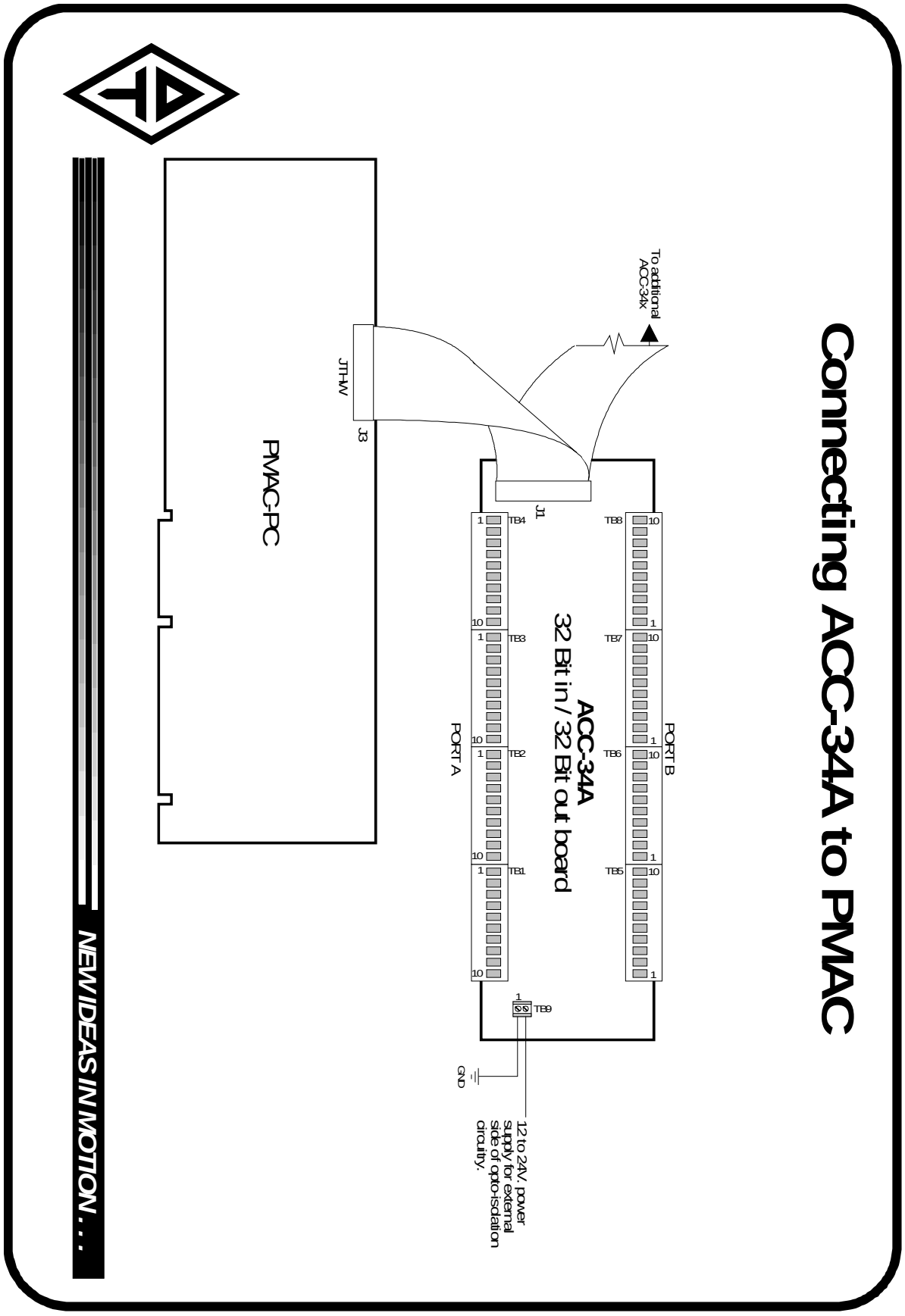
End of RAM is definable by user

ACC-34A
(32-Bit input / 32-Bit output opto board)



- Note: Shaded LED's are *always* lit when power is supplied to pin #10 of the respective terminal block. Other LED's connected to individual I/O pins.

U17-20 - UDN2981 for sourcing outputs
U17-20 - ULN2803 for sinking outputs


Connecting ACC-34A to PMAC
To additional ACC-34x
JTH-4V
J3
PMAC-PC
J1
ACC-34A
32 Bit in / 32 Bit out board
PORT A
PORT B
TB4
TB3
TB2
TB1
TB8
TB7
TB6
TB5
TB9
GND
12 to 24V. power supply for external side of opto-isolation circuitry.
NEW IDEAS IN MOTION . . .