# IP-OptoAD16

## Opto-Isolated 16-bit
## A/D Conversion
## IndustryPack®

## User's Manual


Manual Revision: 2 7/27/99 Hardware Revision: A

**IP-OptoAD16**

**Opto-Isolated 16-bit A/D Conversion IndustryPack®**

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# Product Description

The IP-OptoAD16 is an IndustryPack® compatible module providing a galvanically isolated 16 channel multiplexed 16 bit ADC with on board DC/DC converter.

Data acquisition and conversion time is mode dependent: up to 12 ms without channel / gain change and up to 14.5 µs with channel / gain change.

The 16 input channels of the multiplexer can be configured by software to operate either in single ended mode or in differential mode with eight inputs. The multiplexer of the ADC circuit is over voltage protected up to 70 $V_{p-p.}$ A programmable gain amplifier allows gains of 1, 2, 5, 10 (IP-OptoAD16-BPV-1/UPV-1) or 1, 2, 4, 8 (IP-OptoAD16-BPV-2/UPV-2). The full scale input range is ±10V for the IP-OptoAD16-BPV-1/BPV-2 and 0V to 10V for the IP-OptoAD16-UPV-1/UPV-2 (for a gain of 1). Each IP-OptoAD16 is calibrated at the factory. Calibration information is stored in the Identification PROM unique to each IP.

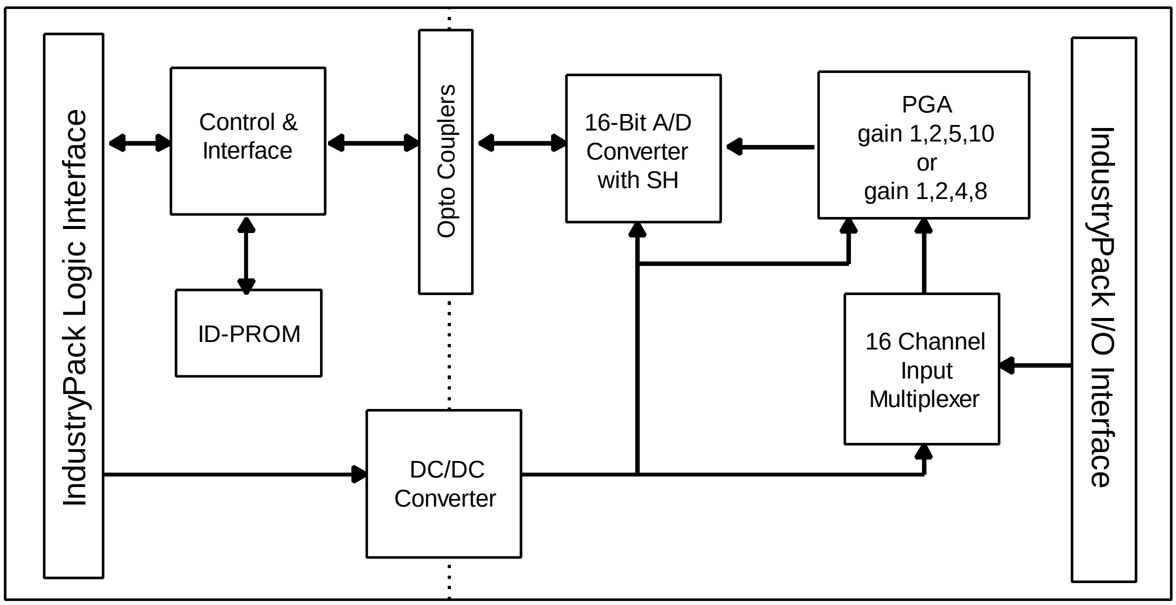



**Figure 1 IP-OptoAD16 Block Diagram**

# Functional Description

## Analog Input

The IP-OptoAD16 provides 16 single ended or 8 differential multiplexed analog inputs for. The desired input and the mode (single ended or differential) is selected by programming the input multiplexer.

A software programmable gain amplifier with gain settings of 1, 2, 5 and 10 for the IP-OptoAD16-BPV-1/UPV-1 and 1, 2, 4 and 8 for the IP-OptoAD16-BPV-2/UPV-2 allows a direct connection of a wide range of sensors and instrumentation. The maximum analog input voltage range is ±10V at a gain of 1 for IP-OptoAD16-BPV-1/BPV-2. For the IP-OptoAD16-UPV-1/UPV-2 the maximum analog input voltage range is 0V to 10V at a gain of 1.

The ADC is a 16 bit ADS7809 with a maximum sample and conversion time of 10µs.

In multiplexed analog input systems a settling time must expire before the data can be converted after the change of the input channel. This settling time is depended on the programmed gain. At the most analog input solutions it is the responsibility of the user to observe the settling time. The IP_OptoAD16 module has an Automatic Settling Time Control mode. If this mode is enabled, a write to the ADC Control Register, which is necessary to select a new input channel by the multiplexer, initiates a data conversion automatically after the settling time has expired.

The absolute accuracy of the module is increased by using the possibility to correct the data by software with factory calibration factors, which are stored in the individual ID PROM of the module.

## Data Correction

There are two errors which affect the DC accuracy of the ADC. The first is the zero error (offset). This is the data value when converting with the input connected with its own ground in single ended mode, or with shorted inputs in differential mode. This error is corrected by subtracting the known error from all readings.

The second error is the gain error. Gain error is the difference between the ideal gain and the actual gain of the programmable gain amplifier and the ADC. It is corrected by multiplying the data value by a correction factor.

The data correction values are obtained during factory calibration and are stored in the modules individual version of the ID PROM. The ADC has a pair of offset and gain correction values for each of the programmable gains.

The correction values are stored in the ID PROM as two's complement 16-Bit wide values in the range -32768 to 32767. For higher accuracy they are scaled to 1/4 LSB.

### ADC Correction Formula

The basic formula for correcting any ADC reading for the **IP-OptoAD16-BPV-1/BPV-2** ( input voltage range +/- 10V ) is :

$$\textbf{Value} = \textbf{Reading} * ( 1 - \textbf{Gain}_{corr} \;/\; 131072 ) - \textbf{Offset}_{corr} \div 4$$

The basic formula for correcting any ADC reading for the **IP-OptoAD16-UPV-1/UPV-2** ( input voltage range 0V to 10V ) is:

$$\textbf{Value} = \textbf{Reading} * ( 1 - \textbf{Gain}_{corr} \;/\; 262144 ) - \textbf{Offset}_{corr} \div 4$$

Value is the corrected result, Reading is the data read from the ADC, $Gain_{corr}$ and $Offset_{corr}$ are the correction factors from the ID PROM.

$Gain_{corr}$ and $Offset_{corr}$ correction factors are stored in each for the possible gain settings.

**Note**: Floating point arithmetics or scaled integer arithmetics is necessary to avoid rounding error while computing above formula.

# ID PROM Contents

## ID PROM Contents IP-OptoAD16

| ADDRESS | FUNCTION | |
|---|---|---|
| $01 | ASCII 'I' | $49 |
| $03 | ASCII 'P' | $50 |
| $05 | ASCII 'A' | $41 |
| $07 | ASCII 'C' | $43 |
| $09 | Manufacturer ID | $B3 |
| $0B | Model Number | $22 |
| $0D | Revision | $10 |
| $0F | RESERVED | $00 |
| $11 | Driver-ID low-byte | $00 |
| $13 | Driver-ID high-byte | $00 |
| $15 | number of bytes used | $1D |
| $17 | C R C | $ variable |
| | | |
| $ 19 | Version -xx | $ see Figure 3 |
| | | |
| $ 1B | Offset Error at Gain = 1 low byte | |
| $ 1D | Offset Error at Gain = 1 high byte | |
| $ 1F | Offset Error at Gain = 2 low byte | |
| $ 21 | Offset Error at Gain = 2 high byte | |
| $ 23 | Offset Error at Gain = 4 / 5 low byte | |
| $ 25 | Offset Error at Gain = 4 / 5 high byte | |
| $ 27 | Offset Error at Gain = 8 / 10 low byte | |
| $ 29 | Offset Error at Gain = 8 / 10 high byte | board |
| $ 2B | Gain Error at Gain = 1 low byte | dependent |
| $ 2D | Gain Error at Gain = 1 high byte | |
| $ 2F | Gain Error at Gain = 2 low byte | |
| $ 31 | Gain Error at Gain = 2 high byte | |
| $ 33 | Gain Error at Gain = 4 / 5 low byte | |
| $ 35 | Gain Error at Gain = 4 / 5 high byte | |
| $ 37 | Gain Error at Gain = 8 / 10 low byte | |
| $ 39 | Gain Error at Gain = 8 / 10 high byte | |
| | | |
| $ 3B | Not used | $ 00 |
| ..... | | ...... |
| $ 3F | | $ 00 |

**Figure 2 ID PROM Contents IP-OptoAD16**

# ID Prom Contents IP-OptoAD16 Model dependent

| IP-OptoAD16 | Version $19 |
|---|---|
| BPV –1 | $0A |
| BPV –2 | $0B |
| UPV –1 | $14 |
| UPV –2 | $15 |

**Figure 3 ID PROM Contents Model Dependent**

# IP Addressing

The IP-OptoAD16 is controlled by a set of registers, which are directly accessible in the IO address space of the IP.

| ADDRESS | NAME | FUNCTION | SIZE | ACCESS |
|---|---|---|---|---|
| $ 00 | CONTREG | ADC Control Register | word | R/W |
| $ 02 | DATAREG | ADC Data Register | word | R/W |
| $ 05 | STATREG | ADC Status Register | byte | R |
| $ 07 | CONVERT | ADC Convert Start Register | byte | W |
| $ 09 | INTVEC | Interrupt Vector Register | byte | R/W |
| $ 0B | IDWRENA | ID-PROM write enable | byte | W |

**Note**: IDWRENA is for factory use only, do **not** write to this register.

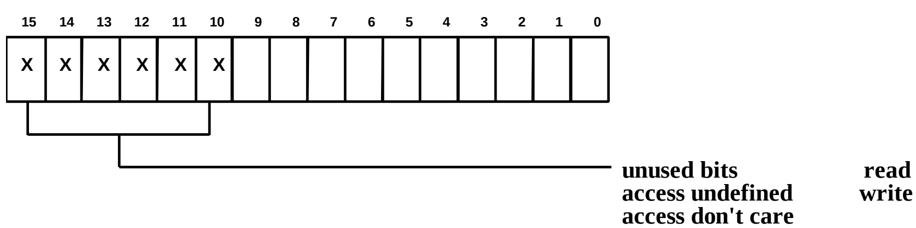
## ADC Register Set

The ADC of the IP-OptoAD16 is controlled by a set of 4 registers. All registers are cleared by IP_RESET.

ADC Control Register
ADC Data Register
ADC Status Register
ADC Convert Start Register

### ADC Control Register Address $00

The ADC Control Register CONTREG is used to select an input channel, the gain and the mode for the next data conversion. This is done by writing the corresponding bit pattern into bit 0 to bit 9.




#### ADC Channel Selection

Bit 0 to bit 3 of the ADC Control Register CONTREG are used to select an input channel for the  data conversion.

Bit 4 of the ADC Control Register CONTREG is used to control if the module operates in differential or in single ended mode. If this bit is set to '1' differential mode is selected.

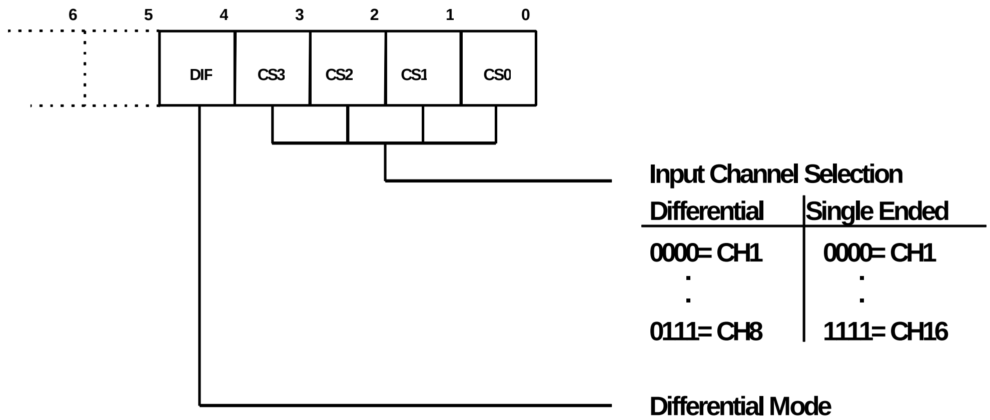
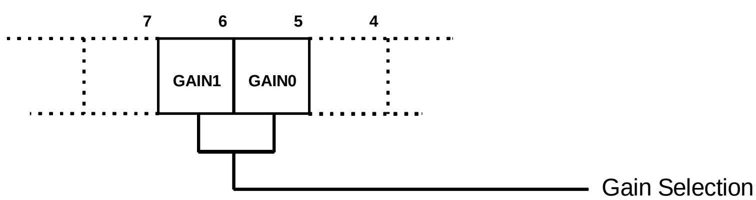



**Figure 4 CONTREG Input Channel Selection and Mode**

**Note**: In differential mode only channels 1 to 8 may be selected. In this mode channels 9 to 16 are used as - input for channels 1 to 8.

## ADC Gain Selection

Bit 5 and bit 6 of the ADC Control Register CONTREG are used to program the gain of the input amplifier.




| IP-OptoAD16-BPV-1/UPV-1 | IP-OptoAD16-BPV-2/UPV-2 |
|---|---|
| 00 = G1 | 00 = G1 |
| 01 = G2 | 01 = G2 |
| 10 = G5 | 10 = G4 |
| 11 = G10 | 11 = G8 |

**Figure 5 CONTREG Input Gain Selection**

## ADC Automatic Settling Time Control

If bit 7 of the ADC Control Register CONTREG is set to '1', the Automatic Mode for the settling time is enabled. In this mode a data conversion is initiated by writing to the ADC Control Register CONTREG, but however is automatically delayed by hardware until the gain depended settling time has expired. If bit 7 of the ADC Control Register CONTREG is set to '0', the Normal Mode for the settling time is enabled. In this mode a data conversion is initiated by writing to the ADC Convert Start Register CONVERT after selecting the desired channel and gain by writing to the ADC Control Register CONTREG.


**Figure 6 CONTREG Automatic Settling Time Control**

**Note**: The settling time for all IP-OptoAD16 Modules is 10µs for all gains.

### ADC Pipeline Mode Control

If bit 8 is set to '1' the pipeline mode is selected. In pipeline mode the result from the conversion (N-1) is shifted into the ADC Data Register DATAREG during the conversion N.

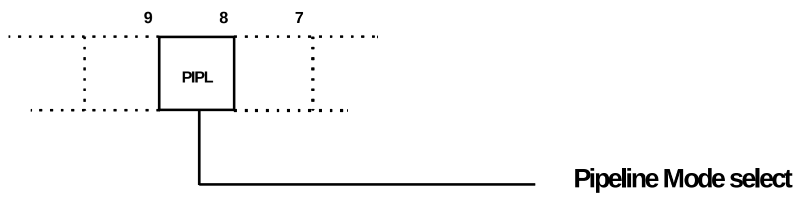



**Figure 7 CONTREG Pipeline Mode Control**

### ADC Interrupt Enable

Bit 8 of the ADC Control Register CONTREG is used to enable interrupt generation of the module. If this bit is set to '1' interrupts are always initiated, whenever the settling time is over ( on IP_INTREQ1 ) and data conversion has been completed ( on IP_INTREQ0 ). If the module is in the automatic mode ( bit7 set to '1' ) only one interrupt at the end of data conversion ( on IP_INTREQ0 ) is being generated.

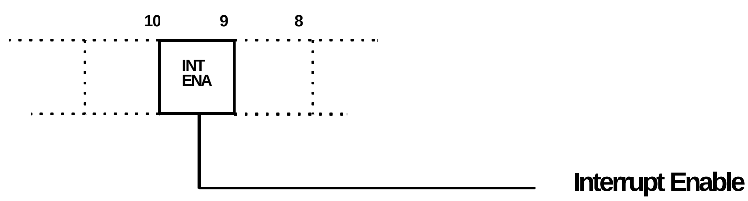



**Figure 8 CONTREG Interrupt Enable**

## ADC Data Register Address $02

The ADC Data Register DATAREG contains the converted data value. The 16 bit ADC value allows direct processing of the data as a 16 bit two's complement integer value for the IP-OptoAD16-BPV-1/BPV-2 and 16 bit straight binary for IP-OptoAD16-UPV-1/UPV-2.

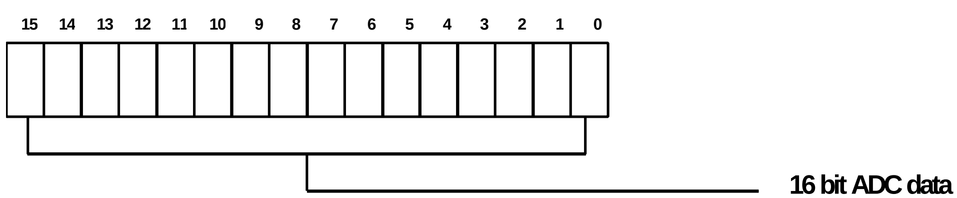



**Figure 9 ADC Data Register**

| DESCRIPTION | DIGITAL OUTPUT | |
|---|---|---|
| | binary two's complement<br>TIP501-10/11 | straight binary<br>TIP501-20/21 |
| + Full Scale (FS - 1LSB) | $7FFF | $FFFF |
| Midscale | $0000 | $8000 |
| One LSB Below Midscale | $FFFF | $7FFF |
| - Full Scale | $8000 | $0000 |

**Figure 10 Data Register Description**

**Note**: The contents of ADC Data Register DATAREG is not valid as long as the ADC Busy Flag is read as '1'.

## ADC Status Register Address $05

Bit 0 and bit 1 of the ADC Status Register STATREG reflect the status of the ADC converter. As long as bit 0 is read as '1', the settling time did not expire after writing to the ADC Control Register CONTREG. Bit 1 indicates the busy status of the ADC converter itself ( '1' = ADC busy ). If Automatic Mode is active bit 1 indicates a '1' during the settling time and the conversion time.

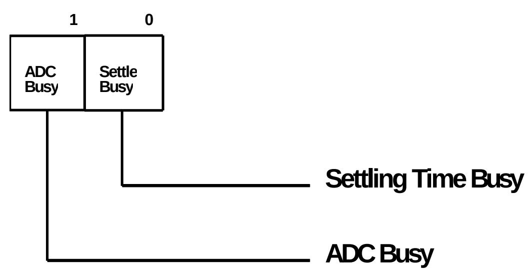



**Figure 11 ADC Status Register**

**Note**: Bit 2 - 7 of the ADC Status Register are undefined.

## ADC Convert Start Register Address $07

If the IP-OptoAD16 is configured in Normal Mode writing any value into the ADC Convert Register CONVERT starts a data conversion immediately.

**Note**: In normal mode it is in the responsibility of the user to observe the settling time busy flag and the ADC busy flag of the ADC Status Register. Writes to the ADC Convert Start Register CONVERT during ADC busy = '1' are ignored.

## Interrupt Vector Register Address $09

The Interrupt Vector Register INTVEC is a byte wide read/write register. The Interrupt Vector Register is shared between both interrupt sources, but both, the settling time ready and the ADC data ready will create an individual interrupt. A read cycle to the INTVEC Register acknowledges and clears the interrupt.

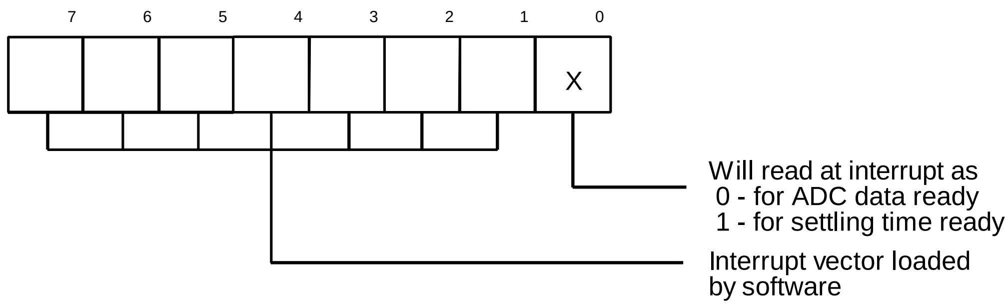



**Figure 12 INTVEC Interrupt Vector Register**

For an interrupt from settling time ready bit 0 of the interrupt vector will read as '1'. For an interrupt from the ADC data ready bit 0 will read as '0'. If the vector register is for example loaded with '$60', settling time ready interrupt vector will be read as '$61' and ADC data ready interrupt vector will be read as '$60'. In I/O space D0 of the interrupt vector register is always read as '0'.

**Note**: The interrupt settling time ready is created by the falling edge of settling time busy status and uses the INTREQ1, the interrupt ADC ready is created by the falling edge of ADC busy status and uses the INTREQ0 interrupt line of the IP bus.

## ID Write Enable Register Address $0B

This register is for factory use only. Do not write to this register. If bit 0 is set '1' a write access to the ID-PROM is enabled.

# Operating Modes

The IP-OptoAD16 supports four operating modes which are selected with bit 7 ( Normal / Automatic Mode ) and bit 8 ( Pipeline / no Pipeline Mode ) of the ADC Control Register CONTREG.

## Mode Overview

- Normal Mode / No Pipeline Mode
- Automatic Mode / No Pipeline Mode
- Normal Mode / Pipeline Mode
- Automatic Mode / Pipeline Mode

| | CONTREG Bit 7 = 1<br>Automatic Mode | CONTREG Bit 7 = 0<br>Normal Mode |
|---|---|---|
| CONTREG Bit 8 = 1<br>Pipline Mode | After the settling time has expired conversion N is started and the result of conversion N-1 is shifted into the ADC Data Register. | A write access to the CONVERT register starts conversion N and shifts the result of conversion N-1 into the ADC Data Register. |
| CONTREG Bit 8 = 0<br>No Pipline Mode | After the settling time has expired conversion N is started and the result of conversion N is shifted into the ADC Data Register. | A write access to the CONVERT register starts conversion N and shifts the result of conversion N into the ADC Data Register. |

**Figure 13 Operating Modes**

**Note**: In Normal Mode the user should observe the settling time by the settle busy flag in the ADC Status Register.

## Automatic Mode

The Automatic Mode is enabled by setting bit 7 of the ADC Control Register CONTREG to '1'. A write access to the ADC Control Register CONTREG with bit 7 set to '1' start a conversion for the programmed channel and gain after the settling time has expired. In Pipeline Mode ( bit 8 of the ADC Control Register CONTREG set to '1' ) the result of the previous conversion is shifted into the ADC Data Register DATAREG during the actual conversion. If the Pipeline Mode is switched off the result of the actual conversion is shifted into the ADC Data Register DATAREG.

# State Diagram Automatic Mode

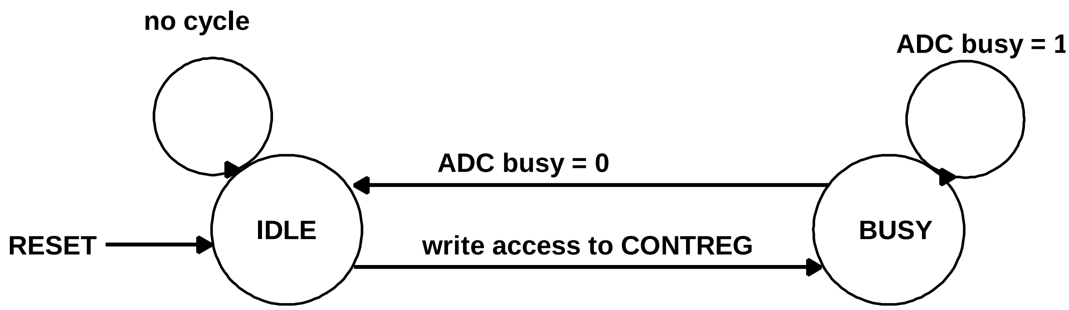
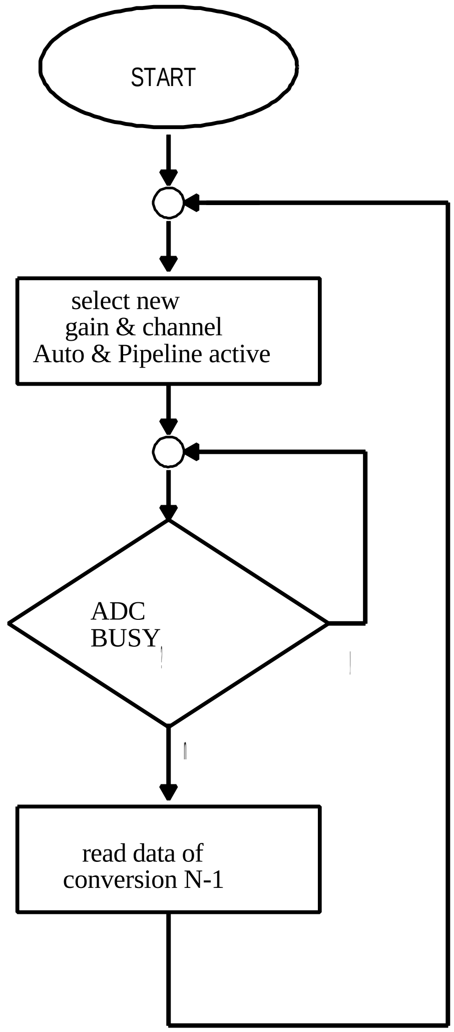



**Figure 14 State Diagram Automatic Mode**

In Automatic Mode the ADC busy flag is active during the whole cycle of channel/gain select, settling time and data conversion. When the ADC busy flag becomes inactive ( = '0' ) the conversion result is accessible in the ADC Data Register DATAREG and an interrupt will be generated if interrupts are enabled.

# Automatic Mode with Data Pipeline

If Automatic Mode with Pipeline is selected during conversion N the result of conversion N-1 is shifted into the ADC Data Register DATAREG. The acquisition and conversion time in this mode is 22µs.




Write access to the ADC Control Register starts automatically the conversion N after the settling time has expired and shifts the result of conversion N-1 into the ADC Data Register.

Bit1 of the ADC Status Register indicates ADC busy during the whole cycle.

Read data of the conversion N-1 from ADC Data Register

**Figure 15 Flowchart Automatic Mode with Data Pipeline**

## Automatic Mode without Data Pipeline

If Automatic Mode without Pipeline is selected the result of the actual conversion is shifted into the ADC Data Register DATAREG. The acquisition and conversion time in this mode is 32ms.

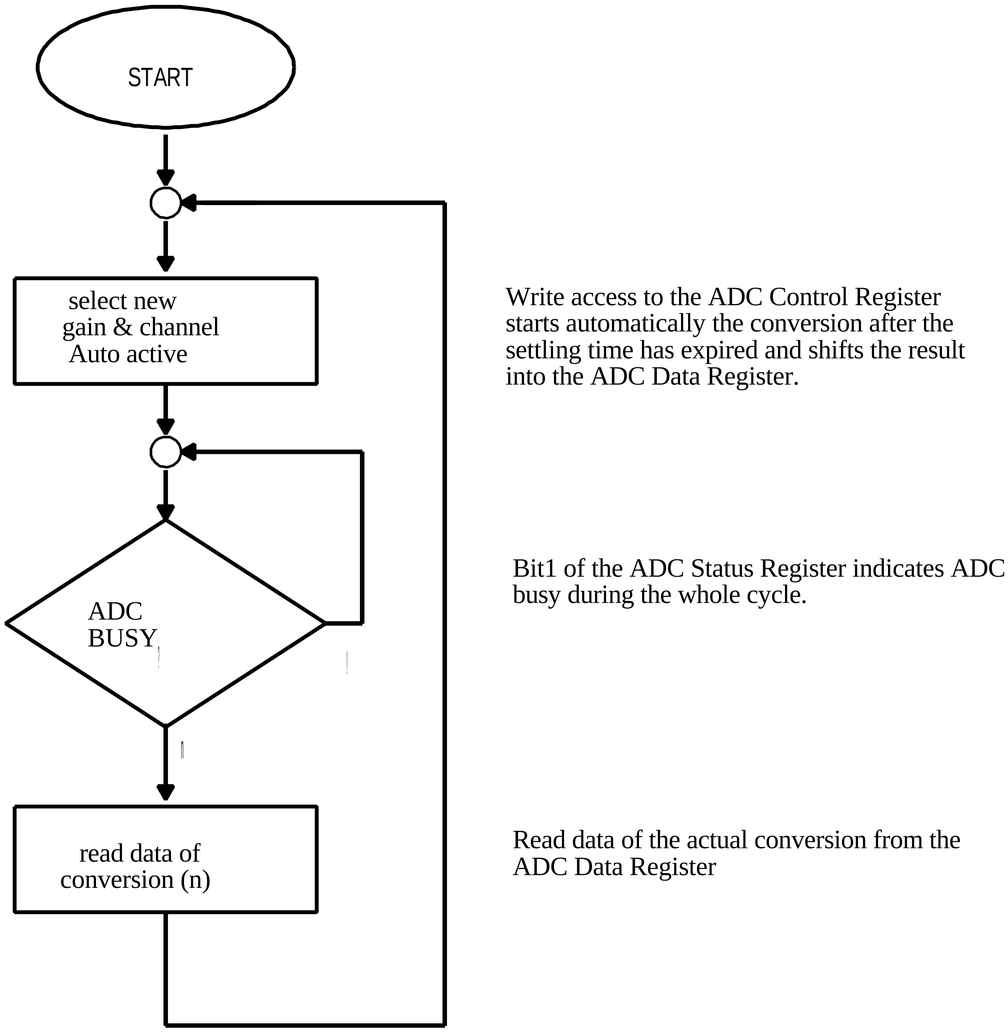



**Figure 16 Flowchart Automatic Mode without Data Pipeline**

# Normal Mode

The Normal Mode is enabled by setting bit 7 of the ADC Control Register CONTREG to `0`. A write access to the ADC Control Register CONTREG with bit 7 set to '0' ( Normal Mode enabled ) selects a new channel and gain for the next conversion. As long as the settling time expires bit 0 of the ADC Status Register STATREG ( settle busy flag ) reads as `1`. After the settling time has expired a conversion can be started by writing to the ADC Convert Start Register CONVERT. To achieve higher conversion rates it is possible to select a new channel and gain for the next conversion after the previous conversion has been started. In this mode the settling time for the new channel and the conversion time of the actual channel proceed simultaneously. As long as bit 1 of the ADC Status Register STATREG ( ADC busy flag ) reads as `1` conversion is in progress. Reading bit 1 of the ADC Status Register as `0`indicates that the conversion result is accessible in the ADC Data Register DATAREG.

If interrupts are enabled two interrupts will be generated: the first interrupt at the end of the settling time, the second interrupt at the end of conversion.

## State Diagram Normal Mode

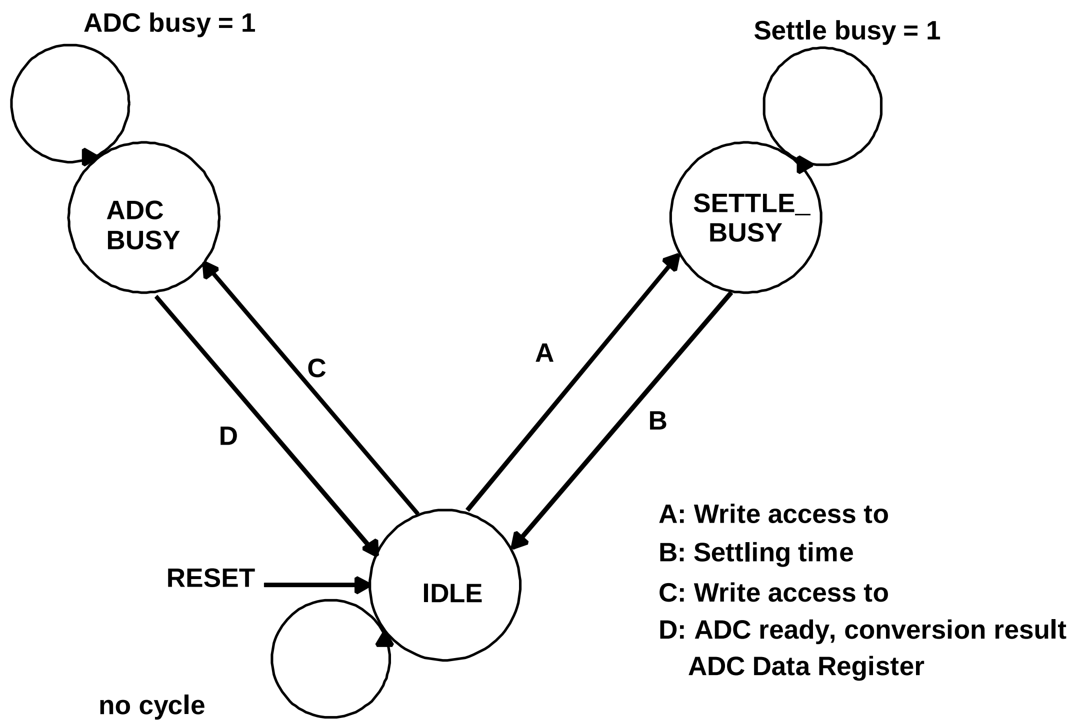



**Figure 17 State Diagram Normal Mode**

## Normal Mode with Data Pipeline

If Normal Mode with Pipeline is selected during conversion N the result of conversion N-1 is shifted into the ADC Data Register DATAREG. In this mode it is possible that the settling time and conversion time simultaneous proceed. The acquisition and conversion time in this mode is 12ms with no change of channel / gain and 14.5ms with change of channel / gain.

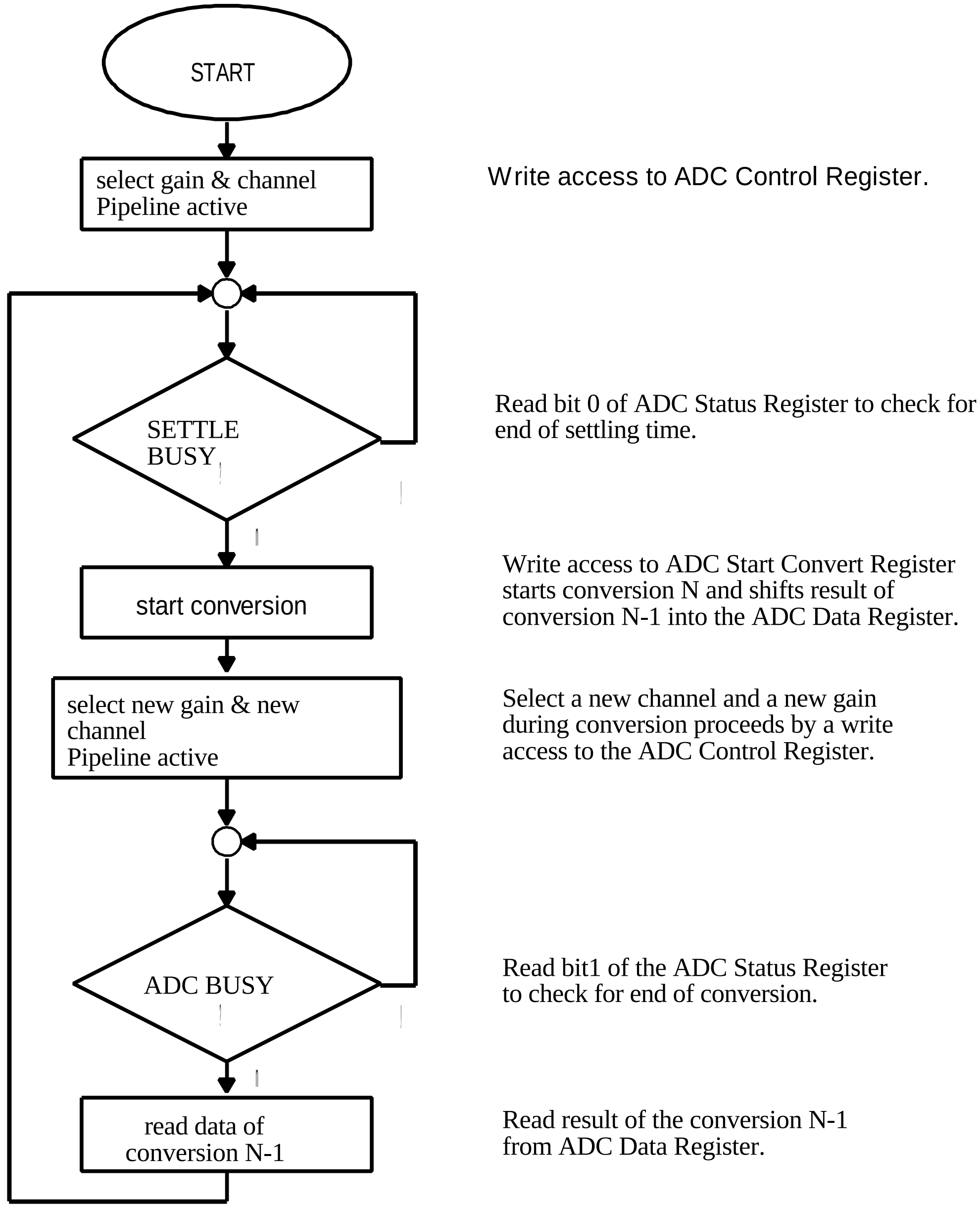



**Figure 18 Flowchart Normal Mode with Data Pipeline**

**Note**: For conversions without channel and gain change it is not necessary to observe the settle busy flag of the ADC Status Register.

## Normal Mode without Data Pipeline

If Normal Mode without Pipeline is selected the result of the actual conversion is shifted into the ADC Data Register DATAREG. In this mode it is possible that the settling time and conversion time simultaneous proceed. The acquisition and conversion time in this mode is 22µs.

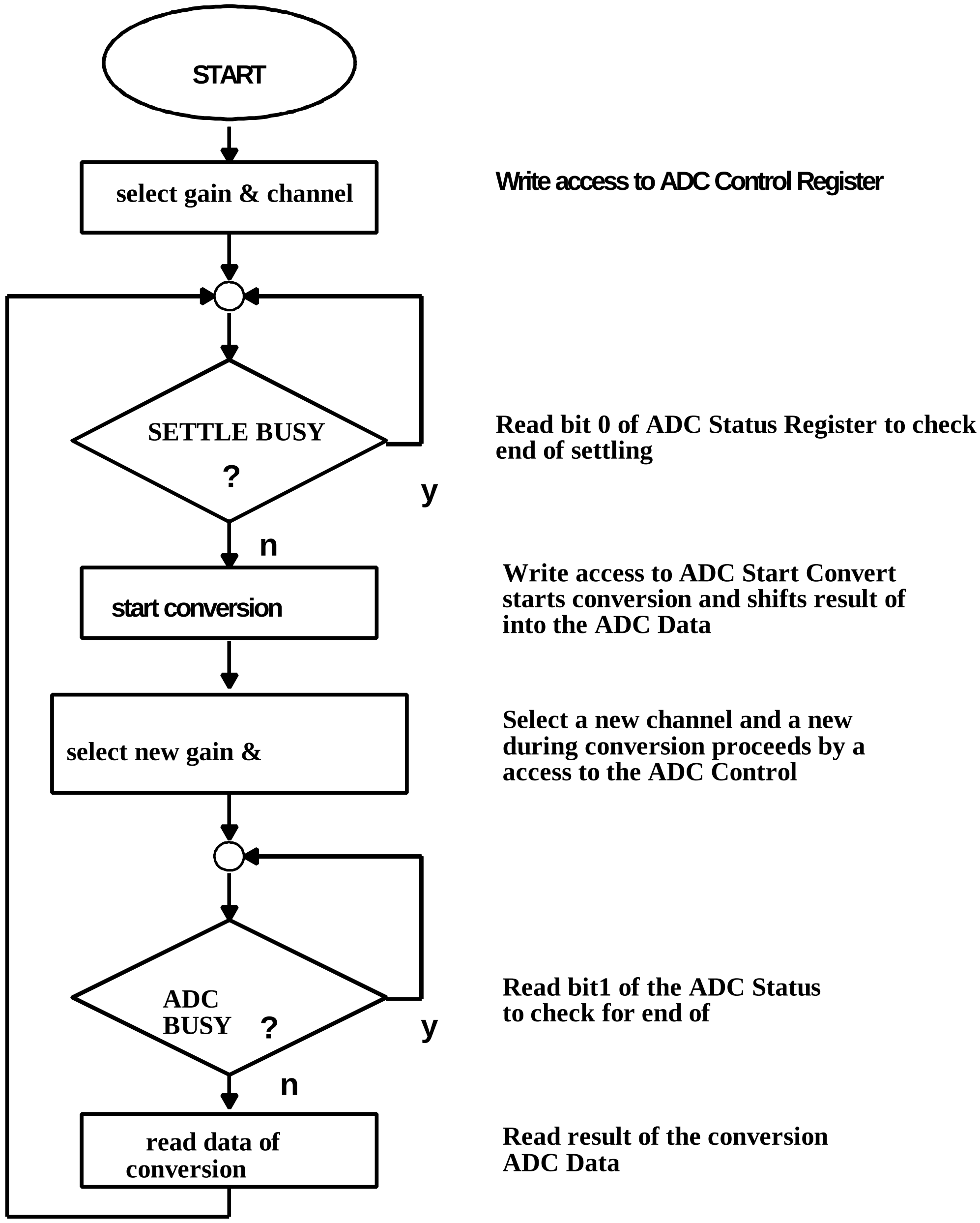



**Figure 19 Flowchart Normal Mode without Data Pipeline**

**Note**: For conversions without channel and gain change it is not necessary to observe the settle busy flag of the ADC Status Register.

# IP I/O connector

## Analog Input Connections

| | Mode | |
|---|---|---|
| Pin Number | Single Ended | Differential |
| 01 | ADC Input 1 | ADC Input 1 + |
| 02 | ADC Input 9 | ADC Input 1 - |
| 03 | AGND | AGND |
| 04 | ADC Input 10 | ADC Input 2 - |
| 05 | ADC Input 2 | ADC Input 2 + |
| 06 | AGND | AGND |
| 07 | ADC Input 3 | ADC Input 3 + |
| 08 | ADC Input 11 | ADC Input 3 - |
| 09 | AGND | AGND |
| 10 | ADC Input 12 | ADC Input 4 - |
| 11 | ADC Input 4 | ADC Input 4 + |
| 12 | AGND | AGND |
| 13 | ADC Input 5 | ADC Input 5 + |
| 14 | ADC Input 13 | ADC Input 5 - |
| 15 | AGND | AGND |
| 16 | ADC Input 14 | ADC Input 6 - |
| 17 | ADC Input 6 | ADC Input 6 + |
| 18 | AGND | AGND |
| 19 | ADC Input 7 | ADC Input 7 + |
| 20 | ADC Input 15 | ADC Input 7 - |
| 21 | AGND | AGND |
| 22 | ADC Input 16 | ADC Input 8 - |
| 23 | ADC Input 8 | ADC Input 8 + |
| 24 | AGND | AGND |

**Figure 20 IP-OptoAD16 Analog Input Connections**

# Power Input Connections

| Pin Number | Function |
|---|---|
| 44 | AGND |
| 45 | -15V |
| 46 | AGND |
| 47 | +15V |
| 48 | AGND |
| 49 | +5V |
| 50 | AGND |

**Figure 21 IP-OptoAD16 Power Input Connections**

**Note**: The power input connections are reserved for special versions of the IP-OptoAD16 without on board DC/DC converter.

# Specifications

| | |
|---|---|
| Logic Interface | IndustryPack Logic Interface |
| Size | single wide IP |
| I/O Interface | 50-conductor flat cable |
| Analog Inputs | 16 single ended channels or<br>8 differential channels |
| Input Isolation | All channels are galvanically isolated from<br>the IP Interface. DC/DC converter on board. |
| Input Gain Amplifier | Programmable for gain 1, 2, 5, 10 (IP-OptoAD16-BPV-1/UPV-2)<br>Programmable for gain 1, 2, 4, 8 (IP-OptoAD16-BPV-2/UPV-2) |
| Input Voltage Range | IP-OptoAD16-BPV-1: IP-OptoAD16-UPV-1:<br>±10V, 0V to 10V (gain = 1)<br>±5V , 0V to 5V (gain = 2)<br>±2V , 0V to 2V (gain = 5)<br>±1V , 0V to 1V (gain = 10)<br><br>IP-OptoAD16-BPV-2: IP-OptoAD16-UPV-2:<br>±10V, 0V to 10V (gain = 1)<br>±5V, 0V to 5V (gain = 2)<br>±2.5V, 0V to 2.5V (gain = 4)<br>±1.25V, 0V to 1.25V (gain = 8) |
| Input Over Voltage | Input over voltage protection up to 70V p-p |
| Input ADC | 16 bit ADC; data acquisition and conversion time up to 12ms without channel / gain change and up to 14.5ms with channel / gain change (mode dependent). |
| Calibration Data | Calibration data for gain and offset correction in ID PROM |
| Accuracy | ± 4LSB, after calibration for all IP-OptoAD16 Modules. |
| Linearity | ± 4LSB for all IP-OptoAD16 Modules |
| No Missing Code | Minimum 15 LSB |
| Wait States | IDSEL 1 wait state<br>IOSEL 0 wait state<br>INTSEL 0 wait state |
| Power Requirements | typ. 310 mA @ 5V |
| Temperature Range | Specification -25°C to 85°C<br>Operating -40°C to 85°C<br>Storage -45°C to 125°C<br>Humidity5 - 95% non-condensing |

# Warranty and Repair

SBS GreenSpring warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, SBS GreenSpring's sole responsibility shall be to repair, or at SBS GreenSpring's sole option to replace, the defective product. The product must be returned by the original customer, insured, and shipped prepaid to SBS GreenSpring. All replaced products become the sole property of SBS GreenSpring.

SBS GreenSpring's warranty of and liability for defective products is limited to that set forth herein. SBS GreenSpring disclaims and excludes all other product warranties and product liability, expressed or implied, including but not limited to any implied warranties of merchantability or fitness for a particular purpose or use, liability for negligence in manufacture or shipment of product, liability for injury to persons or property, or for any incidental or consequential damages.

SBS GreenSpring's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of SBS GreenSpring.

## Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. SBS GreenSpring will not be responsible for damages due to improper packaging of returned items. For service on SBS GreenSpring products not purchased directly from SBSGreenSpring, contact your reseller. Products returned to SBS GreenSpring for repair by other than the original customer will be treated as out-of-warranty.

## Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

### For Service Contact:

Customer Service Department
SBS GreenSpring Modular I/O
181 Constitution Drive
Menlo Park, CA 94025
(415) 327-1200
FAX: (415) 327-3808
email: support@greenspring.com