VETROC: VXS-based Electron Trigger and Readout Card for Hall A Compton

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I INTRODUCTION

This is a specification for a custom trigger and readout board, namely "VETROC", for the Compton Polarimeter DAQ in Hall A. Here we state the application and the requirements. We would like to have a prototype board in 1 year and the final solution in 3 years.

The details of the technical solution will be worked out by Ben Raydo and the JLab Electronics Group. For example, two of the solutions we've discussed informally are : 1) Make a PCB to serialize discriminated signals and ship these optically to a VXS SSP, which sends this information to a CTP; and 2) Make a PCB that is a VXS board that takes in electrical discriminated inputs and sends this information to CTP. Depending on the discriminator outputs a board may or may not be needed to convert those, too, so they can be sent over cable to the VXS crate.

For background information about the plans for the upgrade of the Compton DAQ see http://hallaweb.jlab.org/equipment/daq/compton_coda3.pdf

II APPLICATION

The Hall A Compton polarimeter uses a circularly polarized laser to scatter light from the JLab polarized electron beam; the polarimeter measures the

helicity-dependent asymmetry in both the scattered photons and the electrons. The asymmetry determines the electron beam polarization. One may measure the asymmetry in the photons, the electrons, or in a coincidence; the methods have different systematic errors. The goal is to achieve an error $\leq 1\%$ necessary for several future high-precision physics experiments. For the photons we plan to use the JLab FADC250. For the electrons, we plan to use the board we are specifying here. We should keep in mind that the VETROC is part of a larger DAQ, as this impacts the design.

More information about the Hall A Compton polarimeter may be found online at http://hallaweb.jlab.org/compton

In the existing setup, the electron detector is a 4-plane silicon microstrip detector with 192 strips per plane for a total of 768 channels. The signals from this strips are amplified and discriminated with electronics located near the detector. This results in LVDS signals that are sent along 15m of cable to the trigger electronics. The existing trigger electronics is called the "etroc" [1]. VETROC will be replacing the etroc for the following reasons: (i) to achieve a higher performance (see rates in table 3); (ii) to accommodate possible future designs of this detector (more channels, perhaps up to 1000), and (iii) to provide for local engineering support for the Compton electronics.

III ANTICIPATED DATA

Figure 1 shows a typical event in the Compton electron detector. The track leaves a trail of hits. A "hit" is defined as logical level "true" on a strip generated by the amplifier/discriminator board; a hit occurs if the strip's signal was above a threshold. Often there may be only one hit per plane, but there could be more hits in a plane depending on the energy sharing between the strips. In addition, there will also be background hits and noise, as illustrated in fig 1.

The VETROC has the following jobs:

1. Decide if the hits form a good track and then generate an event trigger.

2. Read out the strips pertaining to the track at a high rate, up to 1 MHz

IV DEFINITION OF TRIGGERS AND PRESCALING

The following triggers are required. Some of this is negotiable if it proves to be too difficult to engineer. Each trigger should be prescalable by a prescale factor of up to 2^{24}. This should be programmable via a 24-bit register corresponding to that trigger.

First, let us define "strip matching". In the triggers defined below, when we say a plane M is matched to plane P, we mean the following: for a given settable time window width a strip N on plane M "matches" with a strip on plane $P \neq M$ if plane P contains a hit on any of the strips $N + X - T, N + X - T + 1, N + X + T + 2, ...N + X + T$ in the time window where X and T are programmable registers that are $\leq N_{\max}$ and where $N_{\max}$ is the maximum number of strips on the plane (presently $N_{\max} = 192$). If $N_{\max}$ is an inconvenient limit for X and T in the implementation, then it would be acceptable to have a bound such as abs$(X) \leq 20$ and $T \leq 20$. Note, X is a programmable offset that is different for each plane (it's the X alignment). And T is global to the detector; it defines the tolerance of the match. If the planes are all well-aligned, then we'll set $X = 0$. A typical tolerance will be $T = 2$.

The purpose of parameters X and T in this strip-matching algorithm is to accommodate possible small misalignments, track angles, inefficiencies, and energy sharing between strips.

Here are the triggers we want:

1. **Trigger 1**: A hit in any plane. (A "hit' is defined at the start of section III). No strip matching is required.
2. **Trigger 2**: A matching hit in any pair of planes. Strips are "matched" as defined above.
3. **Trigger 3**: A matching hit in 3 out of 4 planes.
4. **Trigger 4**: A matching hit in all 4 planes
5. **Trigger 5: Coincidence with Photons** VETROC should form a coincidence trigger between trigger N (selected from N=1-4 defined above) and an externally provided photon trigger within a time window C with a user-settable delay D for one of the signals, as further specified below.

Here is an example of a trigger 2: In this example, we set $X = 0$ and $T = 2$, which are typical values if the strip alignment is good. A hit in strip N in

plane 2 matching a hit on any of the strips $N-2, N-1, N, N+1, N+2$ in plane 3 would make a trigger 2. And plane 3 can also match plane 2 : a hit in strip N in plane 3 matching a strip $N-2, N-1, N, N+1, N+2$ in plane 2 would make a trigger 2. Indeed, a match between *any* two planes will make a trigger 2.

Regarding the Coincidence with Photons (trigger 5): It is assumed that the FADC-based photon DAQ system can produce a trigger signifying a photon from the Compton process. The VETROC device should support a coincidence trigger between this externally provided photon trigger and a selected electron trigger. The programmable features of this coincidence trigger: The user can select which electron trigger to use in coincidence (trigger 1 - 4), and the coincidence time window C is programmable within the range $0.05 < C < 50$ μsec in $\sim 2^{10}$ steps of $0.05\,\mu$sec. Furthermore, we need to be able to adjust the timing delay D of one of the two signals involved in the coincidence trigger, with $0.05 < D < 50$ μsec in $\sim 2^{10}$ steps of $0.05\,\mu$sec.

The unprescaled triggers should be available as outputs of the board. This way we can use them to trigger other devices, to check on a scope, etc.

V READOUT AND NOISE SUPPRESSION

The most straightforward way seems to be solution 2 listed in the introduction, which is pretty similar to the FADC design but for the VETROC we only record logic levels for the strips. Having a VXS board is also a potential cost saver since it would allow to have a complete setup in one crate and if scaling up is needed it could be done using several CTPs and a GTP. Depending on the number of channels needed and since timing resolution is pretty coarse, one could downsample the data up to 96 nsec slices, though it seemed that 24 nsec slices was a good number for the 768 channels of the current detector. A logic mask could be set to turn off transfer of data of some particular channels in case they are noisy. This mask could be applied either on the VXS board or at the CTP level, whichever is the easiest to implement.

The CTP will generate the trigger for the electron with the logic previously defined and the photon, thus creating the single electron, single photon and electron photon coincidences.

The VETROC board should have same pipeline memory depth as the FADC of 8 μs and the trigger should generate a trigger in less than 8 μs so that it can be operated deadtime-less without any data loss.

Some channels (strips) might be noisy, so the VETROC should have a pro-

grammable feature to control individual channels. A channel can be in one of three states, as defined below. This is programmable at setup time, i.e. before an experimental run.

Channel States:

1. **Turned on**: The channel is allowed to participate in trigger formation and is read out when hit. This is the normal, desirable state.
2. **Trigger off**: Is ignored by the trigger but is read out if there is a hit.
3. **Turned off**: Is ignored by the trigger and is never read out.

VI ADDITIONAL LOGIC INPUT

A few additional logic levels needs to be recorded to record the laser state and polarization for example. Those could be logic connectors on the front panel or we could use a complete connector similar to the electron detector inputs.

VII HELICITY RECORDING AND ONBOARD SCALERS

The analysis of the polarization is done by computing a beam asymmetry from the difference of electrons or photons scattered depending of the direction of the helicity of the beam. The helicity is a logic signal (1 or 0) provided by the polarized source which lasts for typically 1 msec. Note the typical flip rate is 1 kHz and the maximum is 2 kHz. Since the asymmetries measured can be very small a common way to reduce any effect of electronics pick-up from the helicity signal is to delay the reporting of this signal to the experiment by a certain number of helicity windows, typically by 8 patterns (a pattern is either a pair, quartet, or octet of helicity windows). In order to record this signal, we propose that the VETROC module has a memory of up to 256 windows (32 octets). Ideally we want to record the 3 logic levels in this way: the Helicity, T-Settle and Pair Sync. The state of those memories will be recorded in the data stream together with the Electron detector hits allowing to access easily the helicity of the events.

On the VETROC board, there should be a number of scaler registers (these have also been called "accumulators"), which are integrated over the time of a helicity signal ("helicity gating") and sorted by helicity. They must be integrated over the time of valid helicity, which is defined as the logical AND of

the helicity pulse and T-settle. These integrated scaler values will be read out at the rate of helicity flipping (∼1 kHz), and must be flagged by the helicity to which they belong. At a minimum, we want to have the five triggers (without prescaling), defined above, counted in scalers. In addition, if it's not too expensive, we would like to add scalers on each strip for each helicity. The scalers would enable quick checks and high-statistics running if we are limited by data transfer. The scalers are incremented separately for each helicity state and can be transferred in a separate type of event at the end of the helicity window. Given that the event-mode readout will produce $\sim$ 20 Gb/hour, we may envision a "production-mode" of running as follows: the event-mode triggers are heavily prescaled (so we record a small diagnostic sample of them), and we rely mainly on the helicity-gated scalers for results. This will work if the system is thoroughly debugged and the backgrounds are low, etc.

VIII DESIRED BUT NOT REQUIRED FEATURES

The following features are desired if they are not too difficult or expensive. They are not required.

- The option to provide an externally-formed trigger 5 (or could be a new trigger 6) from coincidences formed in external electronics.
- For each strip, it is desirable to have an programmable deadtime, defined as an amount of time after a hit that the strip cannot produce another pulse. We would like to study the rates as a function of this deadtime. This deadtime could be programmable as a register with a value D that varies from $0 < D < 10\mu$sec in 2^{10} steps.
- The time tag (250 MHz clock) should have an output so we can look at it or use it elsewhere.

A Proposed Data Structures

This section discusses a workable data structure. We are flexible on what we can accept, as long as it provides a good solution.

The old ETROC trigger [1] provided a fixed data size of 32 words of 32 bits, sending the state of all the bits. One way to reduce the data to be transferred would be to transfer a list of channels hit for each plane. In the current design there are 24 bytes for each planes.

Definitions:

- *Time tag* = A 1 MHz clock sent to every module for synchronization.
- *Pattern IO* = Logic input for the laser states and other information. We mention the need for I/O in section VI.
- *Logic hit pattern* = A pattern of strips, with the same layout as one plane, which shows a hit where the trigger definition was satisfied.

A note about the "logic hit pattern". For the existing ETROC, only one trigger was defined at any given time. Since for the new VETROC we'd have multiple triggers, if we want to preserve the feature of the logic hit pattern we'd need to specify for which trigger it is displayed. The usefulness of the logic hit pattern was that it allowed rapid debugging of the trigger, because one could make an event display together with the hits in the planes. The Logic hit pattern could be enabled only for debugging purpose since it can result in a lot of hits. During production, we'd probably want to turn off the logic hit pattern, to reduce the size of the readout.

Two Types of Data Structures for VETROC

For the VETROC board, we want to have the option of having two data formats. Again, this is a suggestion which follows from experience with the old "etroc" board. The board would run with one or the other format selectable at the start of a run. The formats are called the "fixed size data" format and the "variable size data format". The former would be good for debugging with complete information, while the latter would typically have less data to read out and could be used for production running if the circumstances are favorable. We want to have the flexibility of switching between fixed or variable data size depending on the trigger rates and background conditions.

Fixed Size Data Structure

Here we specify the fixed-size data structure for each trigger. Assuming a 64 bit data structure now we want the data structure in table 1 Note that this has 16 words, each 64 bits.

Variable Size Data Structure

Here we specify the variable-size data structure for each trigger. This feature would allow to reduce the data transferred when the signal is clean and only a few hits are recorded by plane. Assuming each strip number is encoded on 1 byte, the event size is reduced as long as there are less than 24 hits per plane. The proposed event structure is shown in table 2. Note, we assume a 64 bit data structure here. This would give 8 64-bit words if there is less than 7 hits

TABLE 1. Fixed Data Structure

Data	Structure
Time tag, trigger pattern, and pattern IO register	64 bit
Logic hit pattern	3 x 64 bit
Plane A hit pattern	3 x 64 bit
Plane B hit pattern	3 x 64 bit
Plane C hit pattern	3 x 64 bit
Plane D hit pattern	3 x 64 bit

TABLE 2. Variable Data Structure

Variable Size Data	Structure
Time tag and Pattern IO	48 bit + 16 bit
Trigger Pattern and Helicity	2 * 64 bit
Logic hit pattern	Plane 4 bit, hits 4 bit,4 bit per strip hit
Plane A hit pattern	Plane 4 bit, hits 4 bit,4 bit per strip hit
Plane B hit pattern	Plane 4 bit, hits 4 bit,4 bit per strip hit
Plane C hit pattern	Plane 4 bit, hits 4 bit,4 bit per strip hit
Plane D hit pattern	Plane 4 bit, hits 4 bit,4 bit per strip hit

per plane.

IX COMPATIBILITY WITH PREVIOUS DETECTOR

We should make the VETROC electronics compatible with the existing amplifier/discriminator boards. If those boards are ever replaced, then the new boards would need to be compatible with VETROC.

The current detector is using 3M 50 pins connectors, each of them carrying 48 channels of detectors. The connectors of the module should be as high density as possible within a reasonable price. We would need to convert the 50 pins ribbon cable to the higher density connector. This might be accomplished with an external conversion box. Ideally, if it's easy to do, we should be able to send out a copy of those 50 pins signal to be input in the old ETROC for cross checks at the beginning.

Table 3 shows additional specifications for the VETROC board.

REFERENCES

1. ETROC User Manual, Laboratoire de Physique Corpusculaire, Jan 2012.

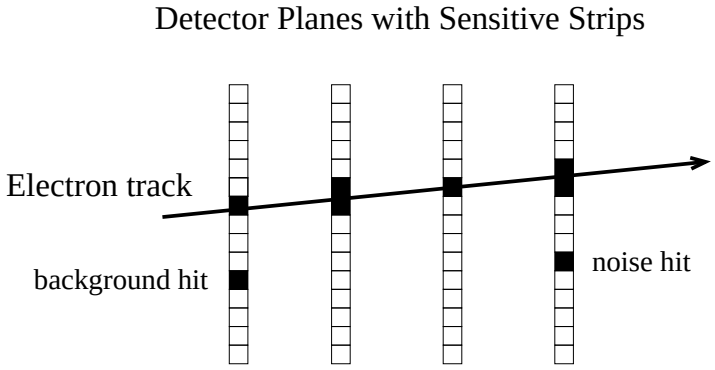

FIGURE 1. Illustration of a typical event from the Compton electron detector. Four planes of sensitive strips are shown. For clarity, only 15 strips per plane are shown, while the actual detector will have more (table 3). The electrons passing through will leave hits *if* the strip was efficient. There may also be background hits, e.g. from synchrotron radiation, and noise hits, as illustrated.

TABLE 3. Specifications for the VETROC

Quantity	Specification
Input Signal Type	LVDS
Signal Interface	50-connector (25-pair) ribbon cable
Pulse Width of Signals	1 to 2 μsec
Time Resolution	1 nsec desired; 100 nsec adequate
Typ / Max Rates for whole detector	100 kHz/ 1 MHz
Electronic Deadtime	$\leq$ 20 nsec
Readout Deadtime	zero below 300 kHz
Distance to Detector	15 meters
Number of Detector Planes	4
Max Channels per plane	256