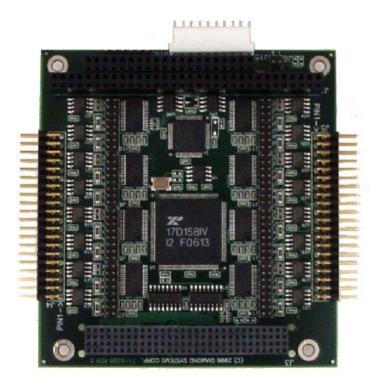


DIAMOND SYSTEMS CORPORATION

Emerald-MM-8Plus

PC/104-Plus 8-Port Multi-Protocol Serial Port Module

User Manual v1.04



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Introduction

Emerald-MM-8Plus is a PC/104-*Plus* module with four or eight serial ports connected through the PCI bus. Each port supports RS-232, RS-422, RS-485 and 5V TTL interfaces using jumper configuration. The board also has eight digital I/O lines and a 16-bit counter/timer.

Emerald-MM-8Plus is connector compatible with the Emerald-MM-8P, Emerald-MM-8M, and Emerald-MM-8232 boards. It is compatible with all CPUs with PC/104-*Plus* connectors. The board is intended to be compatible with any CPU with a PC/104-*Plus* expansion socket and operates with both 3.3V and 5V PCI I/O voltage buses.

Description and Features

Two I/O headers are provided, with four serial ports on each header. The board operates on +5V only, eliminating the need for a +12V supply that is often required for serial port operation.

Emerald-MM-8Plus is based on the Exar XR17D158IV Octal UART. This device contains eight identical sets of registers, one set for each port. The registers are compatible with the standard PC serial port. Each port contains a 64-byte FIFO.

The Emerald-MM-8Plus has the following features.

- I/O connectors compatible with Emerald-MM-8P (two connectors, 40 pins, four ports per connector).
- Eight serial ports based on Exar XR17D158IV Octal UART with 64-byte FIFOs.
- RS-232, RS-422, RS-485, and TTL interfaces supported: RS-232/422/485 jumper selectable; TTL available as
 a custom assembly configuration.
- Baud rates to 921.6Kbps in RS-232 or TTL mode, 1.8432Mbps in RS-422/RS-485 modes.
- Jumper-selected protocol and line termination.
- EEPROM storage of configuration data for instant availability on power-up.
- I/O lines are short circuit protected.
- Eight digital I/O lines with 5V logic.
- LED connected to digital I/O line 0.
- Programmable counter/timer with selectable clock source.
- Dual 40-pin I/O headers, 4 ports per header.
- +5V only operation.
- Extended temperature (-40 to +85°C) operation.
- PC/104-Plus form factor.
- Stackthrough PC/104 and PC/104-Plus connectors installed.

Refer to the Exar XR17D158IV datasheet, listed in the Additional Information section of this document, for detailed information about using the UART, DIO and EEPROM functionality with the PC/104-*Plus* bus.

Block Diagram

Figure 1 shows the Emerald-MM-8Plus functional blocks.

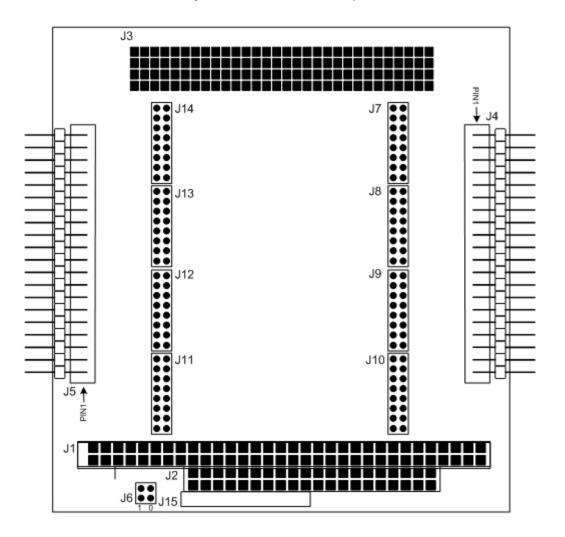
Protocol Selection **PCI Slot ID** Jumpers Protocol Selection PLD PCI/104 (PCI) Connector (8X) J4 RS232/ 8X Serial Ports RS422/RS485 J5 Transceivers Octal UART 8 DIO 8 DIO + Counter/Timer J15 PCI/104 (ISA) Connector 14.7456 MHz Config **EEPROM** Crystal

Figure 1: EMM-8Plus Functional Block Diagram

Board Description

Figure 2 shows the Emerald-MM-8Plus board connectors and jumpers.

Figure 2: EMM-8Plus Board Layout



Connector Summary

The following tables list the Emerald-MM-8Plus board connectors.

| Connector | Description | Manufacturer Part No. |
|-----------|-------------------------------|-----------------------|
| J1 | PC/104, ISA bus A,B | EPT 962-60323-12 |
| J2 | PC/104, ISA bus C,D | EPT 962-60203-12 |
| J3 | PC/104-Plus PCI bus connector | - |
| J4 | Serial ports 1-4 | |
| J5 | Serial ports 5-8 | |
| J15 | Digital I/O and counter/timer | |

Jumper Summary

The following table lists the Emerald-MM-8Plus jumpers.

| Jumper | Description |
|---------|---|
| J6 | PCI bus slot selection. |
| J7-J10 | Serial port configuration (Serial ports 1-4, respectively). |
| J11-J14 | Serial port configuration (Serial ports 5-8, respectively). |

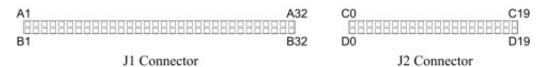
Connectors

This section describes the connectors on the Emerald-MM-8Plus board.

PC/104 ISA Bus

Connectors J1 and J2 carry the ISA bus signal. Figure 3 shows the PC/104 A and B pin layout for J1, and the C and D pin layout for J2. These signals are not used to communicate with the CPU but are pass to other cards on the PC/104 stack.

Figure 3: PC/104 ISA Bus Connectors - J1, J2



| J1 Connector Pinout | | | | | |
|---------------------|-----|-----|----------|--|--|
| IOCHCHK- | A1 | B1 | GND | | |
| SD7 | A2 | B2 | RESETDRV | | |
| SD6 | A3 | В3 | +5V | | |
| SD5 | A4 | B4 | IRQ9 | | |
| SD4 | A5 | B5 | -5V | | |
| SD3 | A6 | B6 | DRQ2 | | |
| SD2 | A7 | B7 | -12V | | |
| SD1 | A8 | B8 | ENDXFR- | | |
| SD0 | A9 | B9 | +12V | | |
| IOCHRDY | A10 | B10 | keyed | | |
| AEN | A11 | B11 | SMEMW- | | |
| SA19 | A12 | B12 | SMEMR- | | |
| SA18 | A13 | B13 | IOW- | | |
| SA17 | A14 | B14 | IOR- | | |
| SA16 | A15 | B15 | DACK3- | | |
| SA5 | A16 | B16 | DRQ3 | | |
| SA14 | A17 | B17 | DACK1- | | |
| SA13 | A18 | B18 | DRQ1 | | |
| SA12 | A19 | B19 | REFRESH- | | |
| SA11 | A20 | B20 | SYSCLK | | |
| SA10 | A21 | B21 | IRQ7 | | |
| SA9 | A22 | B22 | IRQ6 | | |
| SA8 | A23 | B23 | IRQ5 | | |
| SA7 | A24 | B24 | IRQ4 | | |
| SA6 | A25 | B25 | IRQ3 | | |
| SA5 | A26 | B26 | DACK2- | | |
| SA4 | A27 | B27 | TC | | |
| SA3 | A28 | B28 | BALE | | |
| SA2 | A29 | B29 | +5V | | |
| SA1 | A30 | B30 | OSC | | |
| SA0 | A31 | B31 | GND | | |
| GND | A32 | B32 | GND | | |

| J2 Connector Pinout | | | | | | |
|---------------------|-----|-----|---------|--|--|--|
| | | | | | | |
| GND | C0 | D0 | GND | | | |
| SBHE- | C1 | D1 | MEMCS16 | | | |
| LA23 | C2 | D2 | IOCS16- | | | |
| LA22 | C3 | D3 | IRQ10 | | | |
| LA21 | C4 | D4 | IRQ11 | | | |
| LA20 | C5 | D5 | IRQ12 | | | |
| LA19 | C6 | D6 | IRQ15 | | | |
| LA18 | C7 | D7 | IRQ14 | | | |
| LA17 | C8 | D8 | DACK0- | | | |
| MEMR- | C9 | D9 | DRQ0 | | | |
| MEMW- | C10 | D10 | DACK5- | | | |
| SD8 | C11 | D11 | DRQ5 | | | |
| SD9 | C12 | D12 | DACK6- | | | |
| SD10 | C13 | D13 | DRQ6 | | | |
| SD11 | C14 | D14 | DACK7- | | | |
| SD12 | C15 | D15 | DRQ7 | | | |
| SD13 | C16 | D16 | +5 | | | |
| SD14 | C17 | D17 | MASTER- | | | |
| SD15 | C18 | D18 | GND | | | |
| keyed | C19 | D19 | GND | | | |
| | | | | | | |

PC/104-Plus PCI Bus

The PC/104-*Plus* bus is essentially identical to the PCI Bus except for the physical design. A single pin and socket connector is specified for the bus signals. A 120-pin header, J3, arranged as four 30-pin rows incorporates a full 32-bit, 33MHz PCI Bus. The additional pins on the PC/104-*Plus* connectors are used as ground or key pins. The female sockets on the top of the board enable stacking another PC/104-*Plus* board on top of the Emerald-MM-8Plus board. The EMM8-PLUS cannot be configured as a PCI bus master.

In the connector J3 pinout table, below, the top corresponds to the left edge of the connector when the board is viewed from the primary side (the side with the female end of the PC/104-*Plus* connector), and the board is oriented so that the PC/104 connectors are along the bottom edge of the board and the PC/104-*Plus* connector is in the top of the Emerald-MM-8Plus board.

Figure 4: PC/104-Plus PCI Connector - J3



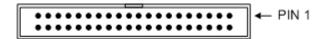
| | А | В | С | D |
|----|--------------|----------|----------|--------------|
| 1 | GND/5.0V KEY | Reserved | +5V | AD00 |
| 2 | VI/O | AD02 | AD01 | +5V |
| 3 | AD05 | GND | AD04 | AD03 |
| 4 | C/BE0* | AD07 | GND | AD06 |
| 5 | GND | AD09 | AD08 | GND |
| 6 | AD11 | VI/O | AD10 | M66EN |
| 7 | AD14 | AD13 | GND | AD12 |
| 8 | +3.3V | C/BE1* | AD15 | +3.3V |
| 9 | SERR* | GND | Reserved | PAR |
| 10 | GND | PERR* | +3.3V | Reserved |
| 11 | STOP* | +3.3V | LOCK* | GND |
| 12 | +3.3V | TRDY* | GND | DESEL* |
| 13 | FRAME* | GND | IRDY* | +3.3V |
| 14 | GND | AD16 | +3.3V | C/BE2* |
| 15 | AD18 | +3.3V | AD17 | GND |
| 16 | AD21 | AD20 | GND | AD19 |
| 17 | +3.3V | AD23 | AD22 | +3.3V |
| 18 | IDSEL0 | GND | IDSEL1 | IDSEL2 |
| 19 | AD24 | C/BE3* | VI/O | IDSEL3 |
| 20 | GND | AD26 | AD25 | GND |
| 21 | AD29 | +5V | AD28 | AD27 |
| 22 | +5V | AD30 | GND | AD31 |
| 23 | REQ0* | GND | REQ1* | VI/O |
| 24 | GND | REQ2* | +5V | GNT0* |
| 25 | GNT1* | VI/O | GNT2* | GND |
| 26 | +5V | CLK0 | GND | CLK1 |
| 27 | CLK2 | +5V | CLK3 | GND |
| 28 | GND | INTD* | +5V | RST* |
| 29 | +12V | INTA* | INTB* | INTC* |
| 30 | -12V | ~REQ3 | ~GNT3 | GND/3.3V KEY |

On the Emerald-MM-8Plus, the octal UART is connected to the PCI bus and is powered by 5V with its PCI interface powered by the PCI bus VIO, which can be 3.3V or 5V. For this reason, the connector is not keyed (to prevent certain types of cards from being inserted).

I/O Header Connectors

Emerald-MM-8Plus provides two identical 40-pin headers labeled J4 and J5 for the serial ports. Four ports are contained on each header.

Figure 5: I/O Header Connectors - J4, J5



Connector, J4, is for ports 1-4 and is located along the right side of the board.

| J4 Port No. | Pin Assignment |
|-------------|----------------|
| PORT1 | Pins 1 - 10 |
| PORT2 | Pins 11 - 20 |
| PORT3 | Pins 21 - 30 |
| PORT4 | Pins 31 - 40 |

Connector, J5, is for ports 5-8 and is located along the left side of the board.

| J5 Port No. | Pin Assignment |
|-------------|----------------|
| PORT5 | Pins 1 - 10 |
| PORT6 | Pins 11 - 20 |
| PORT7 | Pins 21 - 30 |
| PORT8 | Pins 31 - 40 |

Pin numbers are marked on the board to assist with connector orientation.

Cable Assembly Number C-DB9M-4 connects this header to four DE-9 Male connectors, for direct connection to RS-232-C signaling. The following tables list the signals for the appropriate mode of operation, as well as the DE-9 pin numbers to which these signals are wired.

| J5 | | | | |
|--------|------|----|----|------|
| Port1: | DCD1 | 1 | 2 | DSR1 |
| | RXD1 | 3 | 4 | RTS1 |
| | TXD1 | 5 | 6 | CTS1 |
| | DTR1 | 7 | 8 | RI1 |
| | GND | 9 | 10 | DIO0 |
| Port2: | DCD2 | 11 | 12 | DSR2 |
| | RXD2 | 13 | 14 | RTS2 |
| | TXD2 | 15 | 16 | CTS2 |
| | DTR2 | 17 | 18 | RI2 |
| | GND | 19 | 20 | DIO1 |
| Port3: | DCD3 | 21 | 22 | DSR3 |
| | RXD3 | 23 | 24 | RTS3 |
| | TXD3 | 25 | 26 | CTS3 |
| | DTR3 | 27 | 28 | RI3 |
| | GND | 29 | 30 | DIO2 |
| Port4: | DCD4 | 31 | 32 | DSR4 |
| | RXD4 | 33 | 34 | RTS4 |
| | TXD4 | 35 | 36 | CTS4 |
| | DTR4 | 37 | 38 | RI4 |
| | GND | 39 | 40 | DIO3 |

| J4 | | | | |
|--------|------|----|----|------|
| Port5: | DCD5 | 1 | 2 | DSR5 |
| | RXD5 | 3 | 4 | RTS5 |
| | TXD5 | 5 | 6 | CTS5 |
| | DTR5 | 7 | 8 | RI5 |
| | GND | 9 | 10 | DIO4 |
| Port6: | DCD6 | 11 | 12 | DSR6 |
| | RXD6 | 13 | 14 | RTS6 |
| | TXD6 | 15 | 16 | CTS6 |
| | DTR6 | 17 | 18 | RI6 |
| | GND | 19 | 20 | DIO5 |
| Port7: | DCD7 | 21 | 22 | DSR7 |
| | RXD7 | 23 | 24 | RTS7 |
| | TXD7 | 25 | 26 | CTS7 |
| | DTR7 | 27 | 28 | RI7 |
| | GND | 29 | 30 | DIO6 |
| Port8: | DCD8 | 31 | 32 | DSR8 |
| | RXD8 | 33 | 34 | RTS8 |
| | TXD8 | 35 | 36 | CTS8 |
| | DTR8 | 37 | 38 | RI8 |
| | GND | 39 | 40 | DI07 |

| Signal | Definition | DE-9 Pin | Direction |
|--------|---------------------|----------|---------------|
| DCDn | Data Carrier Detect | pin 1 | Input |
| DSRn | Data Set Ready | pin 6 | Input |
| RXDn | Receive Data | pin 2 | Input |
| RTSn | Request to Send | pin 7 | Output |
| TXDn | Transmit Data | pin 3 | Output |
| CTSn | Clear to Send | pin 8 | Input |
| DTRn | Data Terminal Ready | pin 4 | Output |
| RIn | Ring Indicator | pin 9 | Input |
| GND | Ground | pin 5 | Signal Ground |
| DIOn | Digital I/O | - | - |

| | J | 5 | | | | | 14 | |
|-----------|----|----|-----------|------|-----------|------|----|-----------|
| Port1: NC | 1 | 2 | NC | | Port5: No | 1 | 2 | NC |
| TXD/RXD+1 | 3 | 4 | TXD/RXD-1 | | TXD/RXD+ | 5 3 | 4 | TXD/RXD-5 |
| NC | 5 | 6 | NC | | N | 5 | 6 | NC |
| NC | 7 | 8 | NC | | N | 7 | 8 | NC |
| GND | 9 | 10 | DIO0 | | GNI | 9 | 10 | DIO4 |
| Port2: NC | 11 | 12 | NC | _ | Port6: N | 11 | 12 | NC |
| TXD/RXD+2 | 13 | 14 | TXD/RXD-2 | RXD6 | TXD/RXD+ | 3 13 | 14 | TXD/RXD-6 |
| NC | 15 | 16 | NC | | N | 15 | 16 | NC |
| NC | 17 | 18 | NC | | N | 17 | 18 | NC |
| GND | 19 | 20 | DIO1 | | GNI | 19 | 20 | DIO5 |
| Port3: NC | 21 | 22 | NC | _ | Port7: No | 21 | 22 | NC |
| TXD/RXD+3 | 23 | 24 | TXD/RXD-3 | | TXD/RXD+ | 7 23 | 24 | TXD/RXD-7 |
| NC | 25 | 26 | NC | | N | 25 | 26 | NC |
| NC | 27 | 28 | NC | | N | 27 | 28 | NC |
| GND | 29 | 30 | DIO2 | _ | GNI | 29 | 30 | DIO6 |
| Port4: NC | 31 | 32 | NC | _ | Port8: No | 31 | 32 | NC |
| TXD/RXD+4 | 33 | 34 | TXD/RXD-4 | | TXD/RXD+ | 33 | 34 | TXD/RXD-8 |
| NC | 35 | 36 | NC | | N | 35 | 36 | NC |
| NC | 37 | 38 | NC | | N | 37 | 38 | NC |
| GND | 39 | 40 | DIO3 | | GNI | 39 | 40 | DIO7 |

| Signal | Definition | DE-9 Pin | Direction |
|-----------|--------------------------------------|----------|----------------|
| TXD/RXD+n | Differential Transceiver Data (HIGH) | pin 2 | bi-directional |
| TXD/RXD-n | Differential Transceiver Data (LOW) | pin 7 | bi-directional |
| GND | Ground | pin 5 | Signal Ground |
| NC | (not connected) | - | - |
| DIOn | Digital I/O | - | - |

| | J | 5 | |
|-----------|----|----|-------|
| Port1: NC | 1 | 2 | NC |
| TXD+1 | 3 | 4 | TXD-1 |
| NC | 5 | 6 | RXD-1 |
| RXD+1 | 7 | 8 | NC |
| GND | 9 | 10 | DIO0 |
| Port2: NC | 11 | 12 | NC |
| TXD+2 | 13 | 14 | TXD-2 |
| NC | 15 | 16 | RXD-2 |
| RXD+2 | 17 | 18 | NC |
| GND | 19 | 20 | DIO1 |
| Port3: NC | 21 | 22 | NC |
| TXD+3 | 23 | 24 | TXD-3 |
| NC | 25 | 26 | RXD-3 |
| RXD+3 | 27 | 28 | NC |
| GND | 29 | 30 | DIO2 |
| Port4: NC | 31 | 32 | NC |
| TXD+4 | 33 | 34 | TXD-4 |
| NC | 35 | 36 | RXD-4 |
| RXD+4 | 37 | 38 | NC |
| GND | 39 | 40 | DIO3 |

| | J | 4 | |
|-----------|----|----|-------|
| Port5: NC | 1 | 2 | NC |
| TXD+5 | 3 | 4 | TXD-5 |
| NC | 5 | 6 | RXD-5 |
| RXD+5 | 7 | 8 | NC |
| GND | 9 | 10 | DIO4 |
| Port6: NC | 11 | 12 | NC |
| TXD+6 | 13 | 14 | TXD-6 |
| NC | 15 | 16 | RXD-6 |
| RXD+6 | 17 | 18 | NC |
| GND | 19 | 20 | DIO5 |
| Port7: NC | 21 | 22 | NC |
| TXD+7 | 23 | 24 | TXD-7 |
| NC | 25 | 26 | RXD-7 |
| RXD+7 | 27 | 28 | NC |
| GND | 29 | 30 | DIO6 |
| Port8: NC | 31 | 32 | NC |
| TXD+8 | 33 | 34 | TXD-8 |
| NC | 35 | 36 | RXD-8 |
| RXD+8 | 37 | 38 | NC |
| GND | 39 | 40 | DIO7 |

| Signal | Definition | DE-9 Pin | Direction |
|-------------|----------------------------|-------------|---------------|
| TXD+n/TXD-n | Differential transmit data | pin 2/pin 7 | Output* |
| RXD+n/RXD-n | Differential receive data | pin 4/pin 8 | Input* |
| GND | Ground | pin 5 | Signal Ground |
| NC | (not connected) | - | - |
| DIOn | Digital I/O | - | - |

(* Separate lines)

Digital I/O and Counter/timer Connector

Connector J15 is a 1x10, single-row, right-angle connector that provides the following digital I/O and counter/timer signals.

| 1 | DIO7 |
|----|---------------------------------|
| 2 | DIO5 |
| 3 | DIO3 |
| 4 | DIO1 |
| 5 | Counter/timer In |
| 2 | DIO 6 |
| 4 | DIO 4 |
| 6 | DIO 2 |
| 8 | DIO 0/Counter/timer Out/LED Out |
| 10 | GND |

| Signal | Definition |
|-------------------|--|
| DIO 0-7 | Digital I/O; programmable direction |
| Counter/timer In | Counter/timer input |
| Counter/timer Out | Counter/timer output |
| LED Out | User-defined LED, typically for board status |
| GND | Ground |

The DIO/Counter connector J15 provides access to 8 UART DIO lines. These same lines are available on the port connectors J4 and J5. Users should be aware that the DIO on the serial port connectors and J15 are the same line

Board Configuration

The board provides jumper blocks to configure the following functions.

- Serial port protocol RS-232/422/485/TTL: 2 positions for each port.
- RS-422/485 RX and TX termination: 4 positions for each port.
- RS-485 echo yes/no per port: 1 position for each port.
- PCI slot ID: 2 positions for slot 0-3 selection.

For hardwired configuration, locations are provided on the PCB for 0-ohm resistors to be installed to replace each valid jumper position.

Serial Protocol Selection

Jumper blocks J7 through J14 are used to select the protocol for each serial port, as shown in the table below. Each jumper block configures one port, and each port may have its protocol set independently of the other ports.

| Jumper | Port |
|--------|------|
| J7 | 1 |
| Ј8 | 2 |
| Ј9 | 3 |
| J10 | 4 |
| J11 | 5 |
| J12 | 6 |
| J13 | 7 |
| J14 | 8 |

In RS-422 or RS-485 networks, termination resistors are normally installed at the endpoints of the cables to minimize reflections on the lines. Emerald-MM-8Plus provides 150Ω resistors for this purpose. To enable resistor termination for a port, install jumpers in the locations T and R of that port's corresponding configuration jumper block as shown, below.

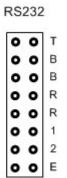
Note: Termination is only needed, and should only be used, at the cable endpoints. Enabling these termination resistors at each end of the cable results in an effective impedance of 60Ω . Installing termination resistors at additional points in the network may cause overloading and failure of the line drivers due to the lower impedance caused by multiple resistors in parallel.

In RS-422 or RS-485 networks, biasing resistors are normally installed at the endpoints of the cables to force a known inactive state on the lines to reduce noise and eliminate line float by pulling the Data+ line to ± 5 V and the Data- line to ground. Emerald-MM-8Plus provides ± 4.7 K Ω resistors for this purpose. To enable resistor termination for a port, install jumpers in the locations ± 8.7 of that port's corresponding configuration jumper block as shown above. For RS422 networks the RX termination always has biasing resistors connected when used and the TX termination has the biasing resistor connections optional when used.

Note: Biasing is only needed, and should only be used, at one of the cable endpoints. Installing biasing resistors at additional points in the network may cause overloading and failure of the line drivers due to the lower impedance caused by multiple resistors in parallel.

Figure 6 shows the J7 through J14 jumper settings to select the RS-232 protocol. (No pins are jumpered).

Figure 6: RS-232 Protocol Selection



RS-422 Selection

Figure 7 shows the J7 through J14 jumper settings to select the RS-422 protocol options.

Figure 7: RS-422 Protocol Selection Options

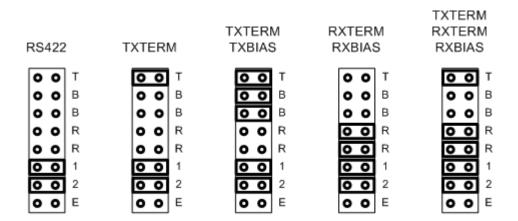


Figure 8 shows the J7 through J14 jumper settings to select the RS-485 protocol options.

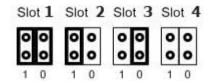
Figure 8: RS-485 Protocol Selection Options

| NOECH | 10 | | CHO RM | NOEC TERI BIAS | М | ECH(| | ECH TER BIA | MS |
|-------|-----|---|------------|----------------------|------------|------|---|-------------------|------------|
| 0 0 |] т | ि | ৹⊤ | 0 | 5 ⊤ | 0 0 | Ţ | 0 | ন ⊤ |
| 0 0 | В | 0 | o B | 0 | В | 0 0 | В | 0 | о в |
| 0 0 | В | 0 | o B | 0 | В | 0 0 | В | 0 | о в |
| 0 0 | R | 0 | 0 R | 0 0 | R | 0 0 | R | 0 | o R |
| 0 0 | R | 0 | o R | 0 0 | R | 0 0 | R | 0 | o R |
| 0 0 | 1 | 0 | 0 1 | 0 0 | 1 | 0 0 | 1 | 0 | ୭ ୀ |
| 0 0 | 2 | 0 | 0 2 | 0 0 | 2 | 0 0 | 2 | 0 | 0 2 |
| 0 0 | E | 0 | O E | 0 0 | E | 0 0 | E | 0 | ○ E |

PCI Slot ID Selection

Jumper block J6 sets the PCI slot ID using two jumpers, as shown in Figure 9. Take care in selecting the correct PCI slot to avoid resource conflicts in the software driver.

Figure 9: PCI Slot ID Selection Jumper



I/O Map

The Emerald-MM-8Plus contains eight registers for controlling board functions and 18 registers for configuring the serial I/O ports.

Emerald-MM-8Plus Registers

The following table describes the basic Emerald-MM-8Plus registers.

| Base+ | Write | Read |
|-------|---------------------------------|---------------------------------|
| 0 | Address pointer/enable register | Address pointer/enable register |
| 1 | Address/IRQ no. Data | Address registers readback |
| 2 | Digital I/O direction register | Interrupt status register |
| 3 | Digital output register | Digital input/readback register |
| 4 | EEPROM read/write + address | EEPROM busy status |
| 5 | EEPROM data (write operation) | EEPROM data (read operation) |
| 6 | Reload command | N/A |
| 7 | N/A | N/A |

Port Configuration Registers

Emerald-MM-8Plus contains 18 additional registers for configuring various serial port parameters. These registers are accessed through the address pointer register at Base+0, described above. The register map is shown in the following table.

| Register No. | Function |
|--------------|---------------------------------|
| 0 | Port 0 address |
| 1 | Port 1 address |
| 2 | Port 2 address |
| 3 | Port 3 address |
| 4 | Port 4 address |
| 5 | Port 5 address |
| 6 | Port 6 address |
| 7 | Port 7 address |
| 8 | Port 0 IRQ no. |
| 9 | Port 1 IRQ no. |
| 10 | Port 2 IRQ no. |
| 11 | Port 3 IRQ no. |
| 12 | Port 4 IRQ no. |
| 13 | Port 5 IRQ no. |
| 14 | Port 6 IRQ no. |
| 15 | Port 7 IRQ no. |
| 16 | Port 0-3 protocol configuration |
| 17 | Port 4-7 protocol configuration |

Writing Data to a Register

To write data to a register, first write the number of that register (0-17) to the board's address pointer/enable register at Base address+0. Then write the data to the board's data register at Base address+1.

Setting a Port Address

To program an address for a port, write the upper seven bits of the 10-bit I/O address into bits 6-0 of the address register for that port. The value written to the address register is, therefore, the desired I/O address divided by 8. All I/O addresses should be on 8-byte boundaries between 0x100 and 0x3F8. Addresses below 0x100 are reserved for CPU functions. A value of 0x00 for a port address disables that port.

IRQ Selection

To select an interrupt level for a port, write the desired interrupt level to the port interrupt level register. Valid interrupt levels are 2, 3, 4, 5, 6, 7, 10, 11, 12 and 15. Writing any other value to the interrupt level register including 0x00 causes the port not to generate interrupts.

Enabling a Port

Bit seven of Base+0 is the port enable bit and must be set, after manual loading of port addresses and interrupts, to enable serial port operation. On power-up or reset, all ports are automatically reloaded with the EEPROM values and are then enabled.

Configuring Port Protocol

To configure the serial protocol for a port the pair of bits assigned to that port must be configured as shown, below.

Register No. 16

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|--------|--------|--------|--------|--------|--------|--------|--------|
| Name: | Port 3 | Port 3 | Port 2 | Port 2 | Port 1 | Port 1 | Port 0 | Port 0 |
| | CFG1 | CFG0 | CFG1 | CFG0 | CFG1 | CFG0 | CFG1 | CFG0 |

Register No. 17

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|-------|--------|--------|--------|--------|--------|--------|--------|--------|--|
| Name: | Port 7 | Port 7 | Port 6 | Port 6 | Port 5 | Port 5 | Port 4 | Port 4 | |
| | CFG1 | CFG0 | CFG1 | CFG0 | CFG1 | CFG0 | CFG1 | CFG0 | |

| CFG0 | CFG1 | Protocol |
|------|------|---------------------|
| 0 | 0 | RS-232 |
| 1 | 0 | RS-422 |
| 0 | 1 | RS-485 with echo |
| 1 | 1 | RS-485 without echo |

I/O Register Descriptions

This section describes the basic Emerald-MM-8Plus register details.

Address Pointer/Enable Register

This register selects the address or IRQ register to be programmed and also enables the serial ports. The value written to this register can be read back for diagnostic purposes.

After writing the address to the register, the appropriate data are then written to the data register at base+1.

Base+0 (Read/Write)

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|--------|---|---|---|-------|---|---|---|
| Name: | ENABLE | - | - | - | A3-A0 | | | |

ENABLE Enables chip selects for the 8 serial ports: 1 = enable, 0 = disable.

On power-up or reset, all ports are automatically programmed from the EEPROM and enabled.

When manually programming the address and IRQ registers, this bit must be set after programming is complete to enable the serial ports.

A3-A0 Address of internal configuration register:

0-7, Address registers for ports 0-7, respectively.

8-15, Interrupt level register for ports 0-7, respectively.

Address/IRQ Protocol Data Register

This register is used to write data to the register selected using the address/enable register described, above. The data are written to this register after the address is selected.

Note: Writing to the serial port address and IRQ registers does not cause a write-through to the corresponding EEPROM registers. You must explicitly write the data to the EEPROM to store these settings for future use when the board is reset or the power is cycled.

I/O Address example:

For a desired I/O address of 0x140 (0 1 0 1 0 0 0 0 0 0), only the upper 7 bits are used. The least significant three bits are always 0, resulting in all addresses occurring on 8-byte boundaries.

The value of the required bits is, therefore, 0 1 0 1 0 0 0 (0x28).

An easy way to generate these bits is to divide the I/O address by eight, or right-shift three places.

Base+1 (Write)

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|---|---|---|---|-------|---|---|---|
| Name: | = | | | | D6-D0 | | | |

D6-D0 Register data.

For address registers, D6–0 contains the upper 7 bits of the 10-bit base address of the serial port. Valid port base addresses are 0x100 to 0x3F8.

For interrupt level registers, Only D3–0 are used. Valid values are 2, 3, 4, 5, 6, 7, 10, 11, 12 and 15. Any other value prevent interrupts from operating on the selected port.

Readback Address Register

This register provides a means to read back the current address settings for Ports 1–8 as a diagnostic tool to verify that the board is present and responding. Using this technique, all eight address registers can be read back. However, the IRQ registers cannot be read back. All 18 register values can be read back from the EEPROM.

Base+1 (Read)

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|---|---|---|---|-------|---|---|---|
| Name: | - | | | | D6-D0 | | | |

D6-D0 Current address settings for Ports 1–8.

Digital I/O Direction Register

This register determines the direction of each of the eight digital I/O lines. The direction of each bit can be programmed individually. This register is cleared to zero (0) on reset or power-up. (All bits in input mode).

Base+2 (Write)

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|------|------|------|------|------|------|------|------|
| Name: | DIR7 | DIR6 | DIR5 | DIR4 | DIR3 | DIR2 | DIR1 | DIR0 |

DIR7-0 Direction: 0 = input, 1 = output.

Interrupt Status Register

The interrupt status register indicates the status of each port interrupt request line. The register operates regardless of whether or not interrupt sharing is enabled (see below). If two or more ports share the same interrupt level, the status register continues to indicate the correct status of each port interrupt request line. If different ports share different interrupt levels, the status register also continues to operate properly.

Base+2 (Read)

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|------|------|------|------|------|------|------|------|
| Name: | INT7 | INT6 | INT5 | INT4 | INT3 | INT2 | INT1 | INT0 |

INT7-0 Interrupt request status: 0 = No interrupt request pending, 1 = Interrupt request is pending.

Digital I/O Output Register

This register programs the digital output lines on the I/O headers. Any line set to output mode using the configuration register at base+2 is set to the value specified in this register. Any I/O line in input mode is unaffected.

The digital output register is cleared to zero (0) on power up or system reset.

Base+3 (Write)

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|---|---|---|--------|--------|---|---|---|
| Name: | | | | DOUT7- | -DOUT0 | | | |

DOUT7-0 Set digital output line to value specified.

Digital Input Register

This register returns the state of the eight digital I/O lines on the I/O headers. Any line in output mode is read back. Any line in input mode is read as the state of the pin on the I/O header.

Input pins that are not driven externally float and have an undefined readback value. The value may change on successive read operations, which is normal behavior for a floating input pin.

Base+3 (Read)

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|------|------|------|------|------|------|------|------|
| Name: | DIO7 | DIO6 | DIO5 | DIO4 | DIO3 | DIO2 | DIO1 | DIO0 |

DIO7-0 Logic state of I/O line 7-0.

EEPROM Command and Address Register

This register is used to initiate an EEPROM read or write operation. First, the data is written to base+5, followed by writing the address and read/write bit of this register to initiate the operation. After initiating the operation, the application program should monitor the BUSY bit by reading this address to detect when the operation is complete.

Base+4 (Write)

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-----|------|------|------|------|------|------|------|
| Name: | R/W | EEA6 | EEA5 | EEA4 | EEA3 | EEA2 | EEA1 | EEA0 |

R/W Command bit:: 1 = write operation, 0 = read operation.

EEA6-0 EEPROM address. Only the lowest 64 bytes of the 256-byte EEPROM are accessible. The lowest 16

bytes contain configuration information for the board. The remaining bytes are available for user

applications.

EEPROM Busy Status Register

The BUSY bit indicates whether or not the EEPROM is currently performing a read, write, or reload operation. The application program must monitor this bit before performing another operation. Performing a new operation without waiting for the previous operation to finish causes the new operation to be ignored.

Base+4 (Read)

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|------|---|---|---|---|---|---|---|
| Name: | BUSY | | | | - | | | |

BUSY EEPROM Busy status: 1 = busy, 0 = idle.

EEPROM Data Register

When writing to the EEPROM, the data is first written to this register before the address and write bit are written to register base+4.

When reading from the EEPROM, the address to read from is first written to base+4. Then, the application program must monitor the BUSY bit in base+4 to detect when the operation is complete. When it is the BUSY bit is zero (0), the program may read the EEPROM data from this register.

Base+5 (Read/Write)

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|---|-----------|---|---|---|---|---|---|
| Name: | | EED7-EED0 | | | | | | |

EED7-0 EEPROM data.

Configuration Register Reload Command Register

This register is used to cause a reload of the contents of the EEPROM into the board configuration registers. This can be done at any time. For example, you may use this operation to recall known good settings in the case when invalid data has been loaded into the registers.

Base+6 (Write)

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|--------|---|---|---|---|---|---|---|
| Name: | RELOAD | | | | = | | | |

RELOAD Set to 1 to force a reload of the eight address and eight interrupt level settings, from the EEPROM into the board. The BUSY bit (base+4, bit 7) goes high and remains high until the reload is complete.

Digital I/O and Counter/Timer

The XR17D158 UART offers 8 built-in digital I/O lines and a programmable counter/timer. The 8 DIO lines and the counter/timer signals are brought out to an 8-pin connector on the lower edge of the board.

The DIO and counter/timer signals are 3.3V nominal logic signals and have ESD protection.

The 8 DIO lines are also available on the 8 extra pins on the two serial I/O connectors to provide compatibility with EMM-8P. The user must be made aware of the limitation that only one source can be used for input, either the serial port connector or the dedicated DIO connector.

The counter/timer's output is multiplexed under software control to DIO 0. The counter/timer's input is programmable for either an internal clock or an external signal. The external signal is available on a pin on the digital I/O connector.

DIO 0 has an LED connected to it for use in displaying board activity or health status.

Specifications

Serial Ports

- No. of serial ports: 8
- Protocols: RS-232, RS-422, RS-485
- Maximum baud rate: 921.6Kbps (RS-232), 1.832Mbps (RS-422/RS-485)
- Communications parameters: 5, 6, 7, or 8 data bits; even, odd, or no parity
- Short circuit protection: All outputs protected against continuous short circuit

RS-232 mode

Input impedance: 3KΩ min
 Input voltage swing: ±30V max
 Display type: ±5V min, ±7V typical

RS-422/RS-485 modes

- Differential input threshold: -0.2V min, +0.2V max
- Input impedance: 12KΩ min
- Input current: +1.0mA max $(V_{IN} = 12V)$ -0.8mA max (VIN = -7V)
- Differential output voltage: 2.0V min (RL = 50Ω)
- High/low states differential output voltage symmetries: 0.2V max

Digital I/O

- No. of I/O lines: 8 in, 8 out
- Input voltage: Low: -0.3V min, 0.8V max High: 2.0V min, 5.3V max
- Output voltage: Low: 0.0V min, 0.4V max (IOL = 6mA max)

High: 3.7V min, 5.0V max (IOH = -4mA max)

General

- Dimensions: 3.55" x 3.775" LxW (PC/104 standard)
- Power supply: +5VDC $\pm 10\%$
- Current consumption: 160mA typical, all outputs unloaded
- Operating temperature: -40° to +85° C
- Operating humidity: 5% to 95% non-condensing
- PC/104 bus: 8-bit and 16-bit bus headers are installed and used (16-bit header is used for interrupt levels only)
- I/O header: 2 40-position (2x20) .025" square pin header on .1" centers;

Headers mate with standard ribbon cable (IDC) connectors

Additional Information

Additional information can be found at the following websites.

- 1. Diamond Systems Corporation (http://www.diamondsystems.com/)
- 2. Datasheet, XR17D158 Universal (3.3V and 5V) PCI Bus Octal UART, Exar Corporation, August 2005. (.pdf)