NEC

User's Manual

IMAPCAR-USB2

Development Board

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NEC Electronics Corporation
1753, Shimonumabe, Nakahara-ku,
Kawasaki, Kanagawa 211-8668, Japan
Tel: 044 4355111
http://www.necel.com/

[America]

NEC Electronics America, Inc.
2880 Scott Blvd.
Santa Clara, CA 95050-2554,
U.S.A.
Tel: 408 5886000
http://www.am.necel.com/

[Europe]

NEC Electronics (Europe) GmbH
Arcadiastrasse 10
40472 Düsseldorf, Germany
Tel: 0211 65030
http://www.eu.necel.com/

United Kingdom Branch
Cygnus House, Sunrise Parkway
Linford Wood, Milton Keynes
MK14 6NP, U.K.
Tel: 01908 691133

Succursale Française
9, rue Paul Dautier, B.P. 52
78142 Velizy-Villacoublay Cédex
France
Tel: 01 30675800

Tyskland Filial
Täby Centrum
Entrance S (7th floor)
18322 Täby, Sweden
Tel: 08 6387200

Filiale Italiana
Via Fabio Filzi, 25/A
20124 Milano, Italy
Tel: 02 667541

Branch The Netherlands
Steijgerweg 6
5616 HS Eindhoven,
The Netherlands
Tel: 040 2654010

[Asia & Oceania]

NEC Electronics (China) Co., Ltd
7th Floor, Quantum Plaza, No. 27
ZhiChunLu Haidian District,
Beijing 100083, P.R.China
Tel: 010 82351155
http://www.cn.necel.com/

NEC Electronics Shanghai Ltd.
Room 2511-2512, Bank of China
Tower,
200 Yincheng Road Central,
Pudong New Area,
Shanghai 200120, P.R. China
Tel: 021 58885400
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NEC Electronics Hong Kong Ltd.
12/F., Cityplaza 4,
12 Taikoo Wan Road, Hong Kong
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Singapore 307684
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Preface

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Chapter 1 Introduction

1.1 System Requirements

Host PC A PC supporting Windows XP or Windows 2000 is required for an appropriate IMAPCAR development tool suite. A Pentium III 500 MHz (at least), 128 MB of RAM, 256-colour display (1024 × 768), CD-ROM drive and 100 Mbytes of free hard disk space are required to install IMAPCAR development suite (compiler and debugger package).

Host Interface A standard USB2 connection is required.

1.2 Package Contents

Please verify that you have received all parts listed in the package contents list attached to IMAPCAR-USB2 package. If any part is missing or seems to be damaged, please contact the dealer from whom you purchased your IMAPCAR-USB2 Development Board.

Note Updates to this User Manual, additional documentation and/or utilities for IMAPCAR-USB2 Development Board, if available, may be downloaded from NEC Electronics' web page(s): *www.eu.necel.com*

1.3 Ordering Information

Part Number: IMAPCAR-USB2

1.4 Related Documents

- IMAPCAR Datasheet
- IMAPCAR User’s manual
- IMAPCAR Architecture

- 1DC quick guide
- 1DC source debugger
- 1DC language
- 1DC programming tips
- 1DC library
- 1DC image processing library

- IOFCONV Object file converter

1.5 Abbreviations

There are some abbreviations used in this document, which may require additional information to be understood correctly.

Altera	FPGA vendor
GND	Ground
I/F	Interface
NC	not connected
PC	Personal Computer
PCB	Printed Circuit Board
SIMD	Single Instruction stream Multiple Data stream
CS	Chip Select

Chapter 2 Board Features

The IMAPCAR USB board aims at becoming the development and embeddable solution for IMAPCAR technology. Its main interests are the following one:

- IMAPCAR's control is available trough a computer, via the USB2 interface
- V850/PHO3 mother board can control IMAPCAR and make the link to any car network (CAN, Flexray, LIN,…)
- The video input and output boards are exchangeable and fully customizable

This manual is intended to user's, who want to understand the functions of IMAPCAR-USB2 development board. This manual presents the HW User's Manual.

2.1 Features

The development board has an IMAPCAR chip soldered; processor speed is configurable via DIP-Switch. The prototype chip is directly connected to at least 4 Mbytes of SSRAM, built up with SSRAM devices when using a total bus width of 64-bits. The SSRAM supports up to 100 MHz SSRAM clock.

A short summary of the board features is given below:

- IMAPCAR chip
- CPLD: ALTERA type (Stratix EPM570)
- USB2 connection for development on IMAPCAR
- 8 General purposes IOs from IMAPCAR
- Extension connectors for Video input and output
- Extension connector for External parallel interface (V850 or else)
- Board size: 160mm x 100mm

The MCU flash does only contain software to handle communication between IMAPCAR and the USB2 interface. The board has no function already implemented; the user has to program it.

The SDBIMAP development environment can be used on the host PC to control the IMAPCAR by USB2 connection.

2.2 Board Usage Examples

In the figure below neither a camera nor a display is connected to IMAPCAR-USB2 board. Image input/output & input/output parameters are entered through the USB bus interface.

The PC is connected to the board through the USB interface and is used to program the program/data/image memory of IMAPCAR device.

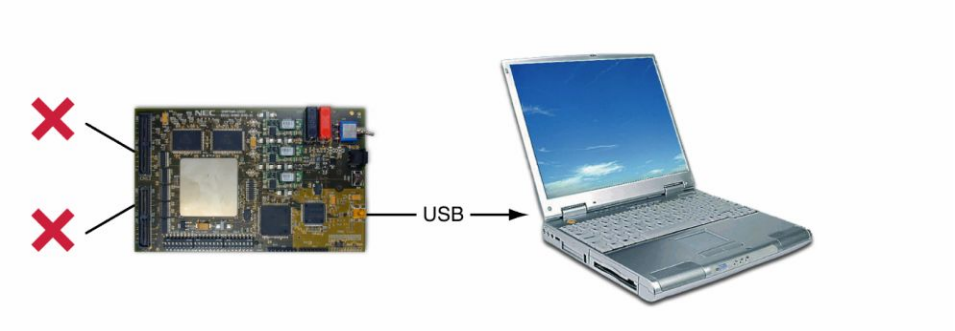

Figure 2-1 Development with PC using the USB interface

In figure 2-2, the video inputs & outputs can be tested in offline mode using the USB connection to the PC. Up to three 8-bits synchronized video flows can be entered in the IMAPCAR device. A display can be as well connected.

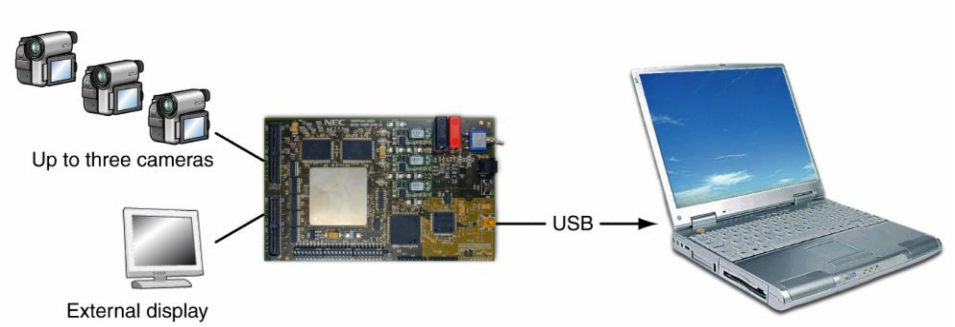

Figure 2-2 Office tests with PC controlling IMAPCAR through the USB interface

The figure 2-3 shows the new feature from the IMAPCAR-USB2 that enables embedded tests while being controlled by a 32 bits micro-controller; this can be the V850/PHO3 starter kit.

The video input/output configuration remains the same as the above use case (for example two front stereo cameras & an external display).

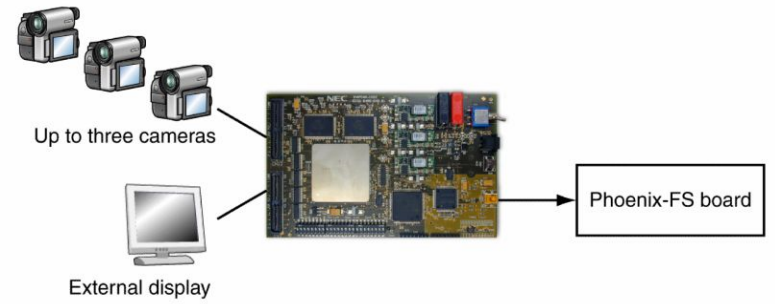

Figure 2-3 Embedded system with microcontroller

Chapter 3 Functional Description

The main part of the IMACPAR-USB2 development board is the NEC IMACPAR chip. Its programming and debug can be done by the USB interface in debug mode or via a supervisor microcontroller in demonstrator mode.

To use this development board, some additional tools are recommended which are not parts of this package:

- SDBIMAP software installed on a PC with USB2 interface
- V850/PHO3 Autosar starter kit board
- V850 mini-cube for debug and programming of the V850/PHO3 device

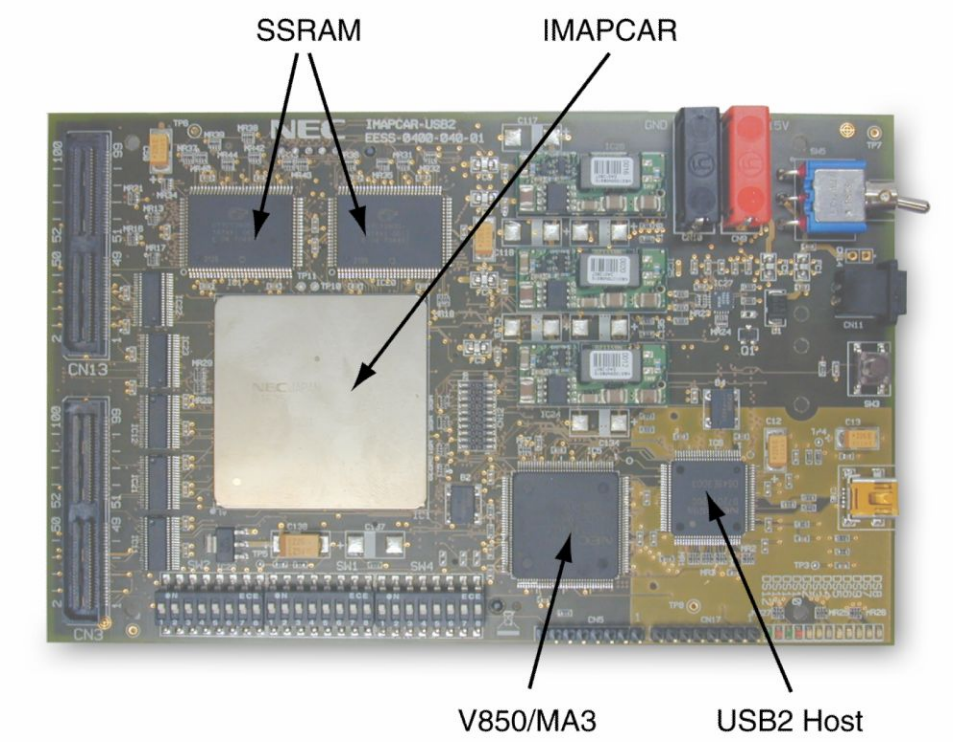

Figure 3-1 Development board (top view)

3.1 Block Diagram

The IMAPCAR-USB2 board contains an IMAPCAR device which is the heart of the system. To work correctly, this device needs external SSRAM memories provided on the board.

The control of the board can be performed in two different ways:

- A PC via the USB interface (V850/MA3 based)
- An external host controller (e.g. V850/PHO3 Autosar starter kit board).

This control I/F is driven by the host interface multiplexer and it depends on the DIP-SWITCH SW2 configuration. The role of the CPLD is only signal adaptation and configuration handling, intelligence is embedded on it.

The video input and output interfaces are provided to the IMAPCAR via a buffer protection. These buffers can be validated or invalidated by jumper configuration.

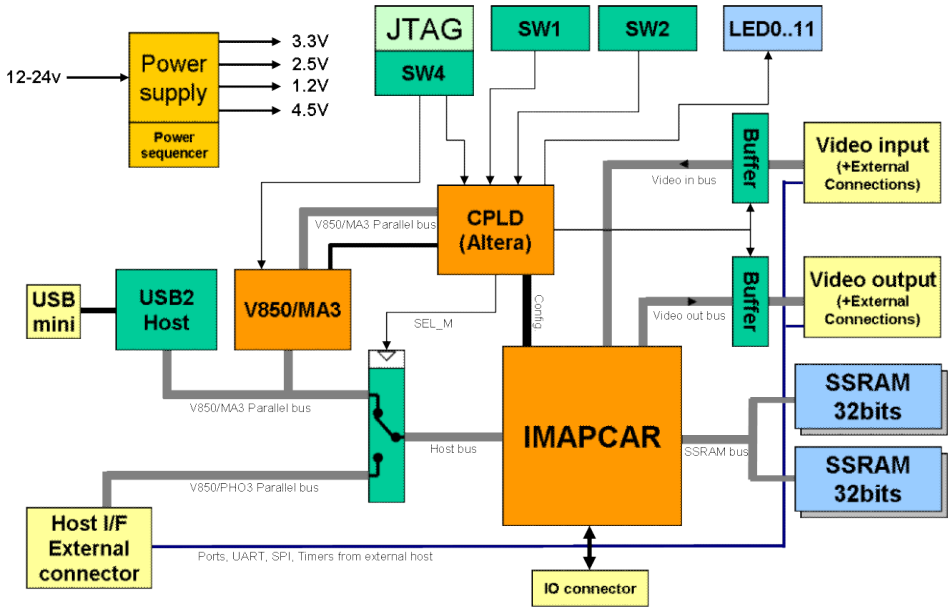

Figure 3-2 Simplified block diagram

3.2 External Interfaces

The external interfaces are described in the figure 2-3. The power supply is done either by the power banana (CN9, CN10) or by the power plug (CN11). The mini-USB connector (CN6) is used to control the IMAPCAR-USB2 when in development tool mode; this is replaced by the external host interface in demonstrator mode (CN1, CN2). Video inputs and outputs are directly provided via SMD connectors (CN3, CN13) to connect with custom interfaces boards. Two 2.54mm connectors are provided to provide an easy access to some IMAPCAR internal signals.

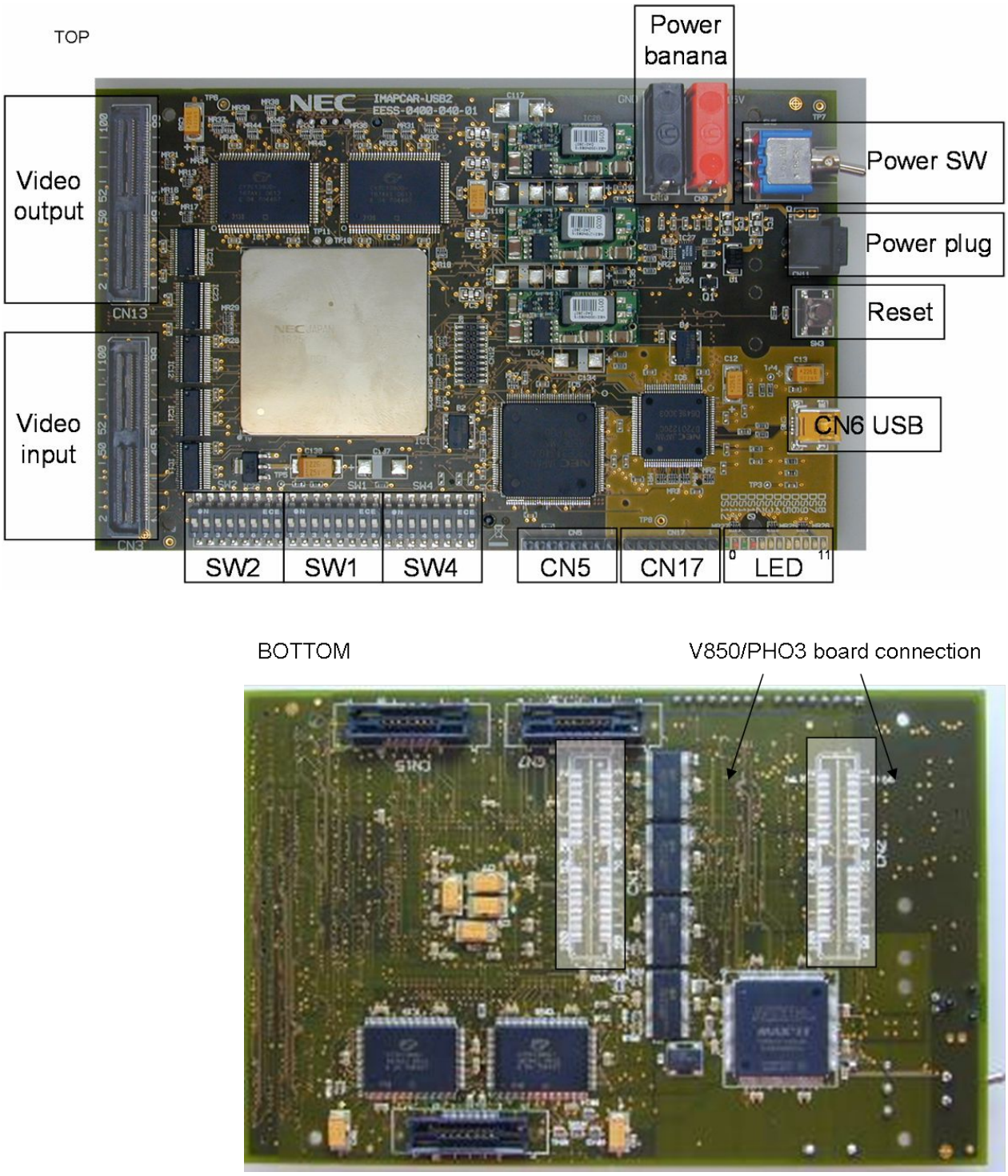

Figure 3-4 External interfaces

(1) USB2 debug interface

- CN6 mini-USB connector

(2) Video Interfaces

- CN13 Video output interface
- CN3 Video input interface

(3) Power

- CN9, CN10 Standard Plugs for Lab Power Supply (12-24V)
- CN11 Standard Plug for 15V/1A plug in Power Supply

(4) External Host I/F

- CN1, CN2 V850/PHO3 external connection

(5) Others

- CN12 CPLD / MA3 programming interface (JTAG) / (for internal use only)

3.3 Default Memory Map

The IMAPCAR prototype chip contains 256 Kbytes of internal RAM memory map and additional 256KB dedicated to access to the internal registers.

The physical address is 0x0078 0000 to 0x007F FFFF when the host I/F is in 8MB mode (SSRAMSEL register = 0x00)
It becomes 0x03F8 0000 to 0x03FF FFFF when in 64MB mode (SSRAMSEL register = 0x03).

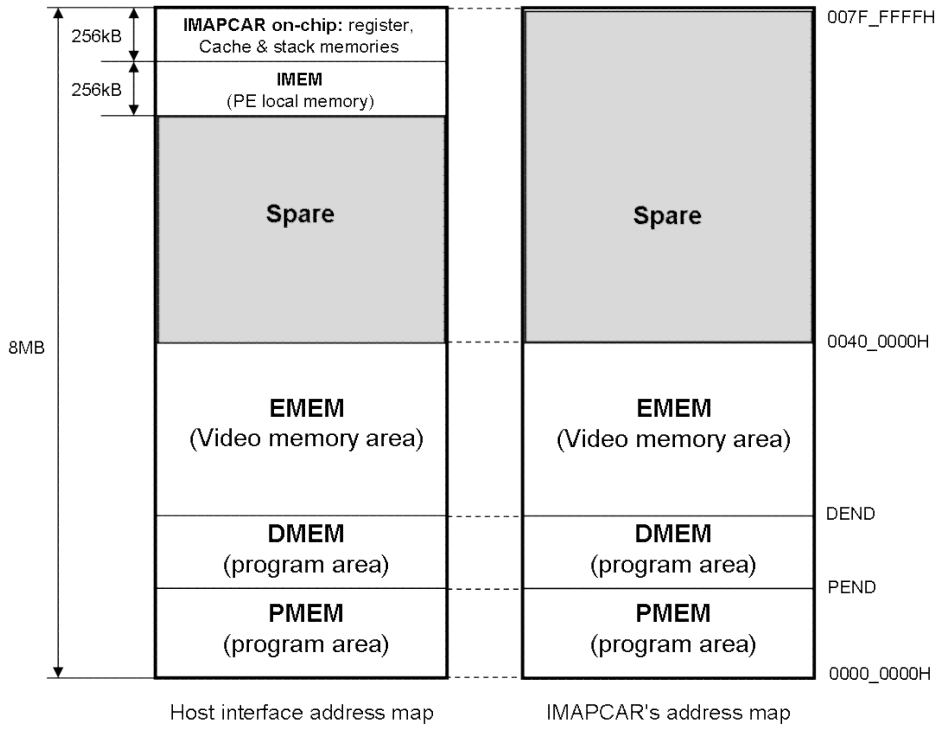

Figure 3-5 IMAPCAR-USB2 Development Board / Default Memory Map

Remark Figure 3-4 shows the default memory map at start-up. The SSRAMSEL register is at 0x00 by default.

Chapter 4 Detailed Functional Description

4.1 Power Supply Connectors

There are two connector types provided on the development board to connect a power supply. You can either use the “classic” laboratory style connectors CN9 and CN10 or the texas style connector CN14. CN14 is used by the power supply that is delivered together with the board. The board consumes typically 300 mA at 15V (does not include any externally connected boards or debugger). Feeding the board with lower voltages increases (!) the supply current due to the switched power supply circuits.

The power switch SW5 is switched off at the left side, and on at the right side (front view).

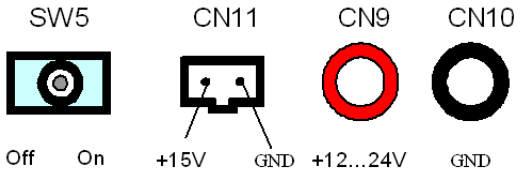

Figure 4-1 Power supply connectors (front view)

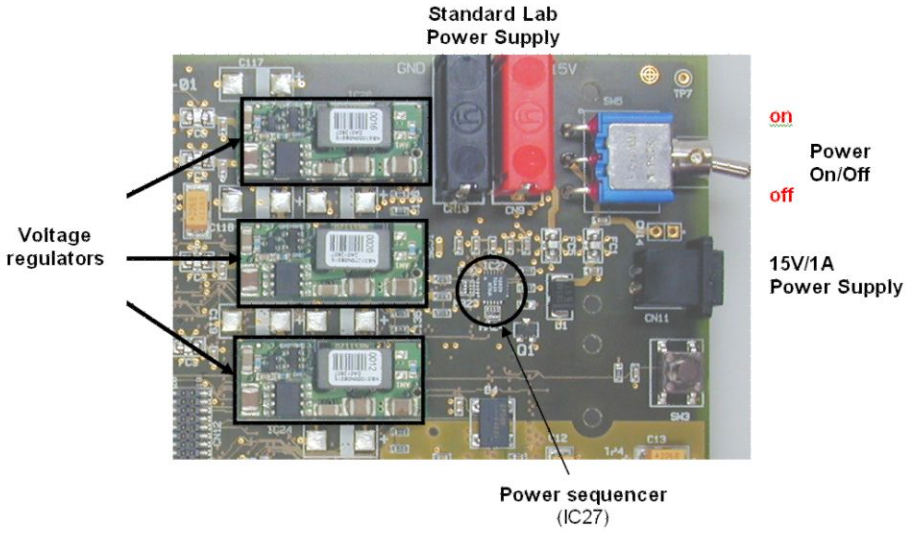

Figure 4-2 Power supply connectors location

4.2 Clock Setting

Figure 4-3 shows the clock distribution on the IMAPCAR-USB2 board. There exist three clock generator on-board: a 8MHz oscillator for the V850/MA3 controller; a 30MHz for the USB interface chip and a 20MHz oscillator for the IMAPCAR. The CPLD receives the 8MHz clock as well but it is not used.

The IMAPCAR contains a PLL that can multiply the clock frequency by a factor of 3, 4, 5 or 6 to reach the maximum frequency of 100 MHz. This clock is then used for the SSRAM access. The video input and output are restricted to 30MHz and the host interface to 20MHz maximum. The remaining signals are lower frequency.

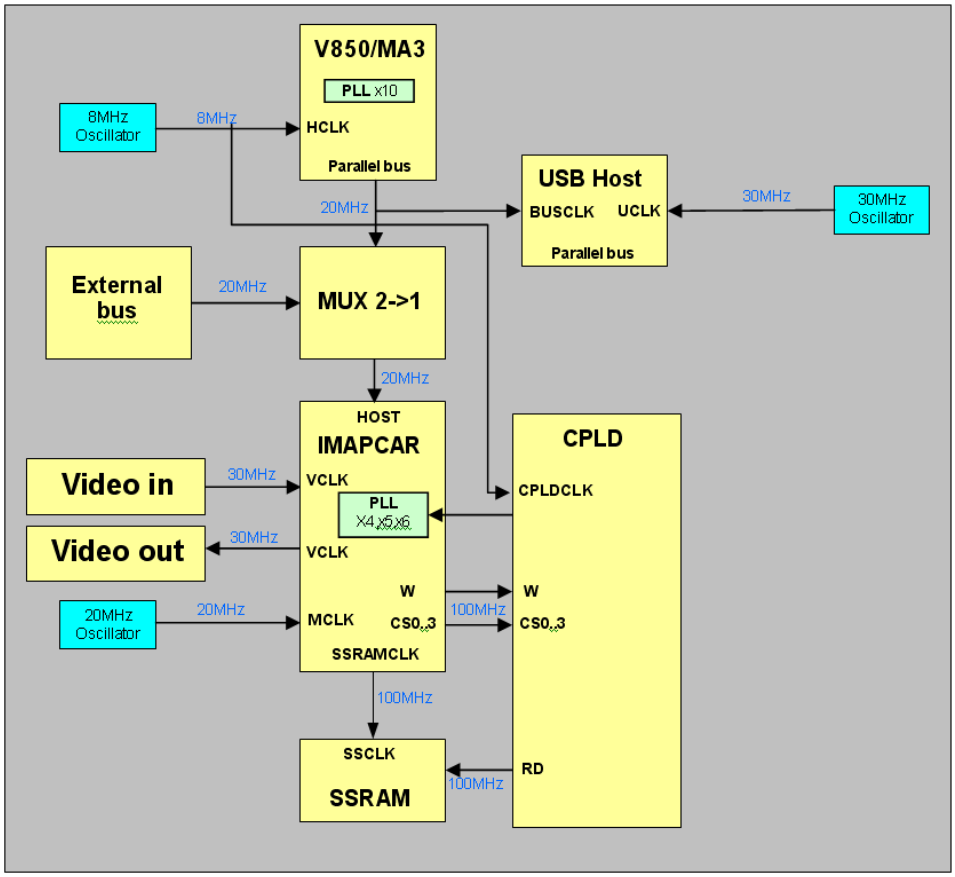

Figure 4-3 Clock structure

The clock allocation on the IMAPCAR-USB2 development board is shown in Table 4-1.

Table 4-1 Clock allocation

Clock	Range	Function
MCLK	20 MHz	IMAPCAR main clock
HCLK	8 MHz	Host V850/MA3 main clock
UCLK	30 MHz	USB host main clock
VCLK	≤ 30 MHz	Video input/output clock
SSRAMCLK	≤ 100MHz	SSRAM clock provided by IMAPCAR
Parallel bus clock	≤ 20MHz	IMAPCAR control bus interface

Figure 4-4 shows the location of HEX and DIL Switches responsible for the clock setting.

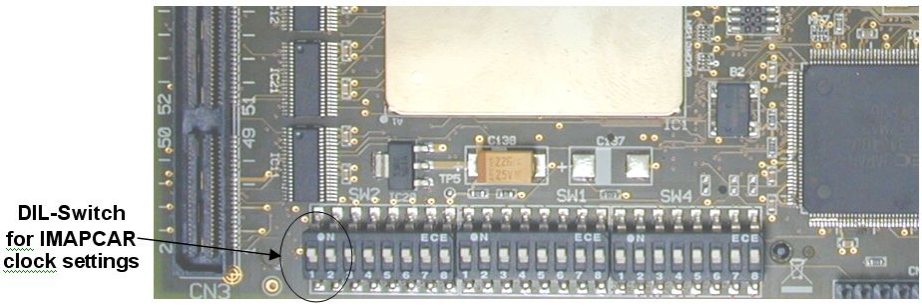

Figure 4-4 Clock settings location

DIP-Switch (SW2) 1-2 are used to select the running frequency of the IMAPCAR (IC1), which corresponds to SCLK that controls the SSRAMs.

This can be set to the following different values:

Table 4-2 IMAPCAR PLL settings (IC1) / Output frequencies

SW2-1	SW2-2	IMAPCAR frequency
OFF	OFF	60 MHz
ON	OFF	80 MHz
OFF	ON	100 MHz
ON	ON	Prohibited

The default setting is shaded in grey colour.

4.3 Reset Structure

The IMAPCAR-USB2 development board has one main button (SW3) to initiate a system reset. Moreover, during power-on, a system reset is automatically initiated.

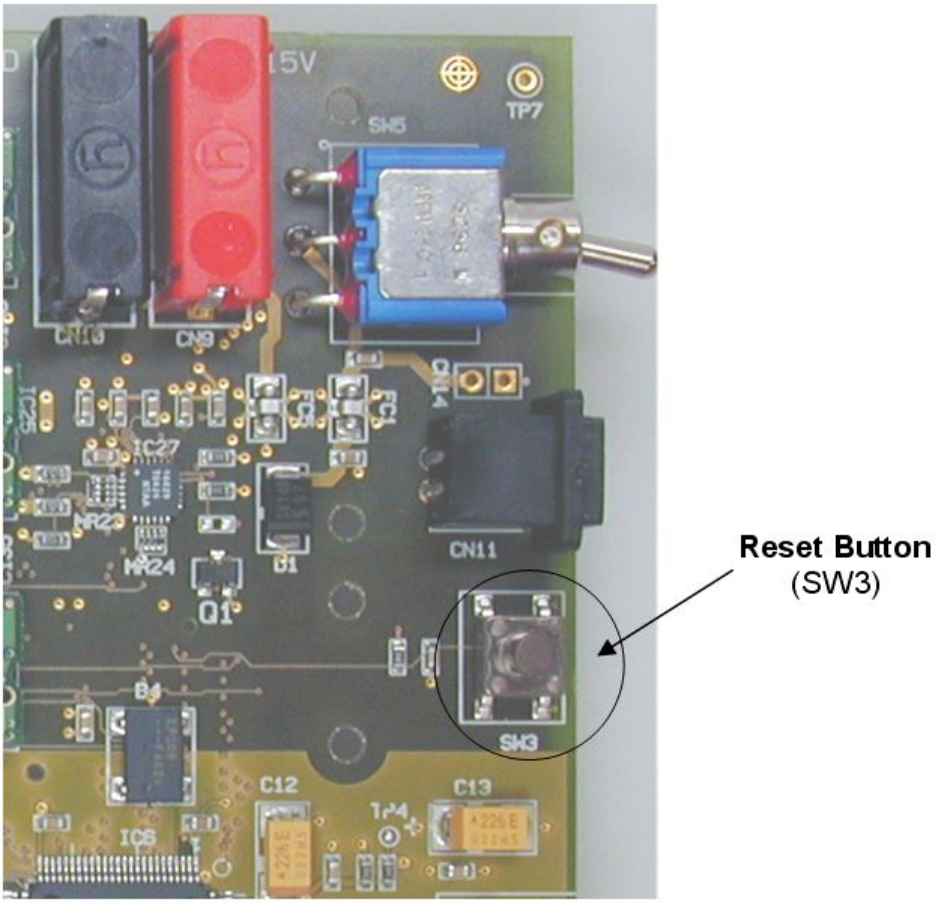

Figure 4-5 Reset button location

The main reset logic is implemented in the Power sequencer (IC27) and CPLD (IC7). The possible reset sources of the IMAPCAR-USB2 development board are as follow:

- The Sys_RESET signal is the main reset of the development board
- The Ext_RESET signal to initiate a system reset controlled by an external signal

Figure 4-6 shows the reset structure of the IMAPCAR2 development board.

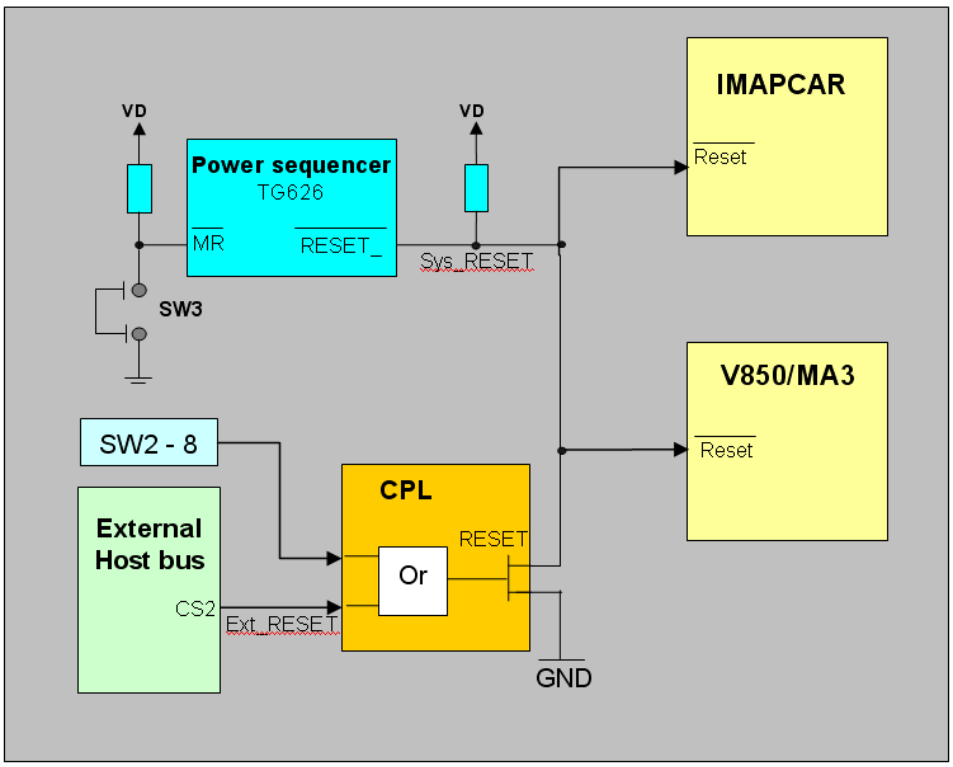

Figure 4-6 Reset structure

- Sys_RESET signal:
  The IMAPCAR-USB2 development board has a main reset called Sys_RESET. This reset signal is used as system reset for the whole IMAPCAR-USB2 development board. This reset is activated by the following conditions
  - power-on
  - manual push button SW3
- Ext_RESET signal:
  The IMAPCAR-USB2 development board can be reseted from an external board, it provides a reset input called **Ext_RESET**. This reset allows generating a system reset for the IMAPCAR device. This reset is activated by the following condition:
  - By external reset request from external host I/F connector (PIN CS2)

Both reset signals (Sys_RESET, Ext_RESET) are low level active.

4.4 SSRAM Memory

The MAPCAR-USB2 board comprises 4 SSRAM that provide a 64bits memory access at the core speed. These SSRAM always work in pair and only two of them can be running at the same time.

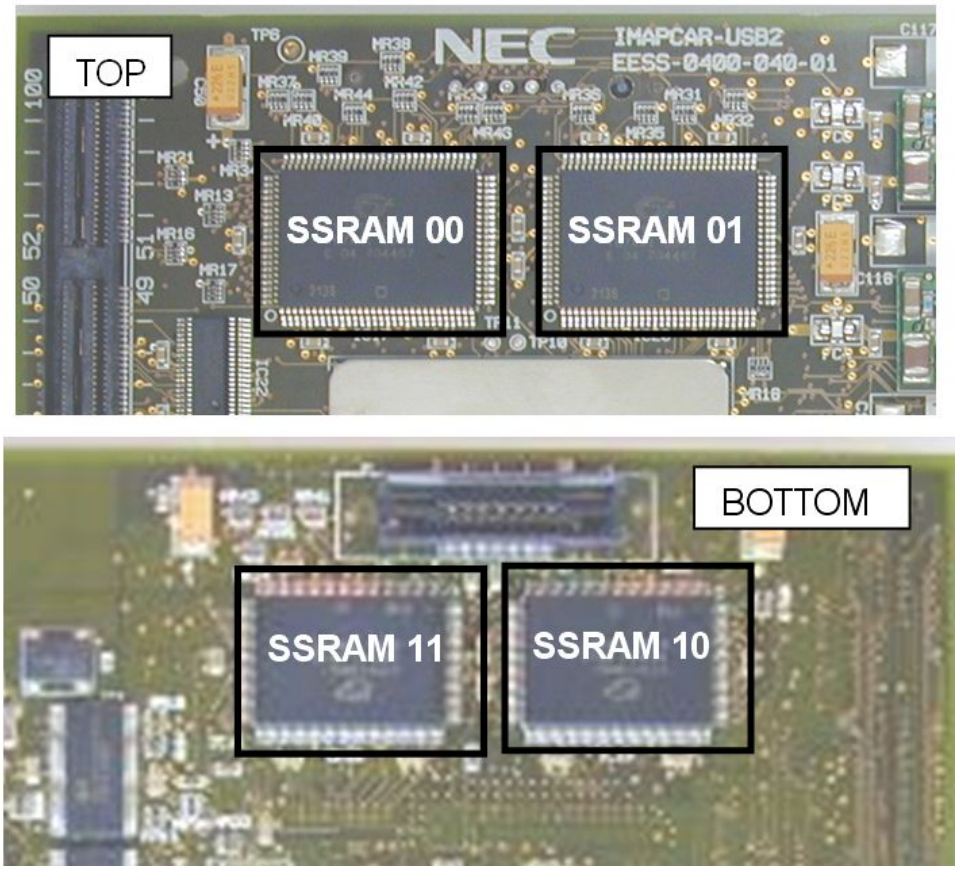

Figure 4-7 SSRAM memory location

The amount of memory on-board depends on the selected memory:

- CYC1360 x4 4MB of SSRAM available (8MB Host address space)
- CYC1380 x4 8MB of SSRAM available (16MB Host address space)
- CYC1440 x4 16MB of SSRAM available (32MB Host address space)
- CYC1480 x4 32MB of SSRAM available (64MB Host address space)

Please check the memories on-board to know your configuration.

4.5 CPLD Functions

The IMAPCAR-USB2 development board comprises a CPLD for board configuration. This CPLD comprises the following features:

- IMAPCAR configuration
- Host I/F selection
- SSRAM signal adaptation
- Video input, output & synchronization buffer validation
- LED display

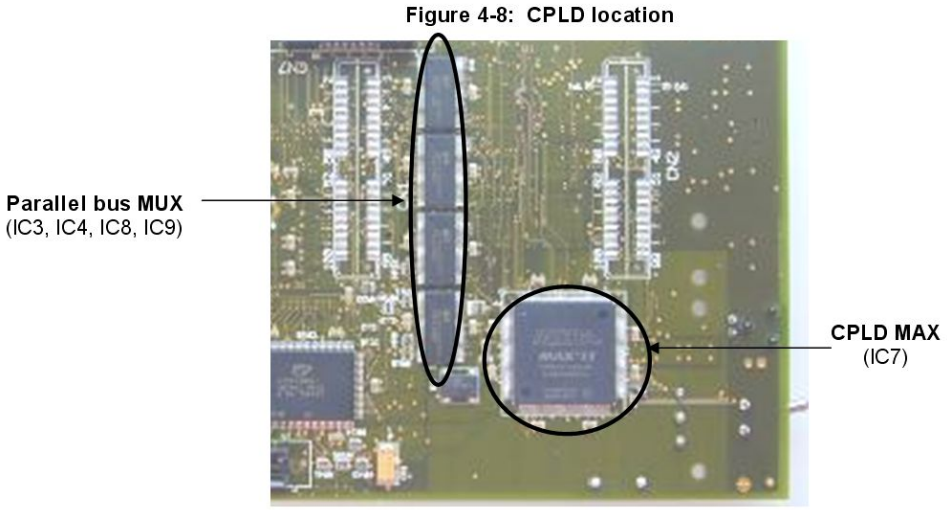

Figure 4-8 CPLD location

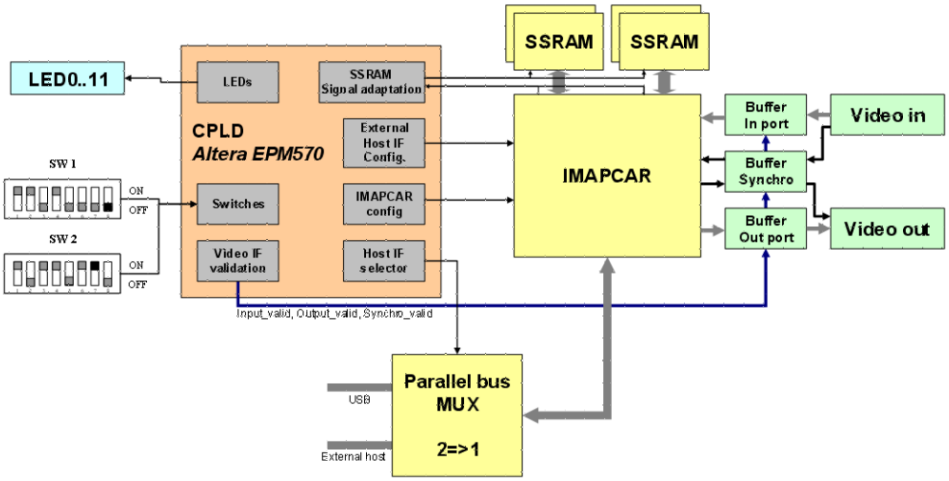

Figure 4-9 CPLD block diagram

4.6 Interfaces and Connectors

4.6.1 External Host Interface

The external host interface was designed to work with the V850/PHO3 AUTOSAR STARTER KIT BOARD. The referenced signals come directly from these boards. Nevertheless, the pinning is provided in this document to enable a different Host microcontroller board to control the IMAPCAR.

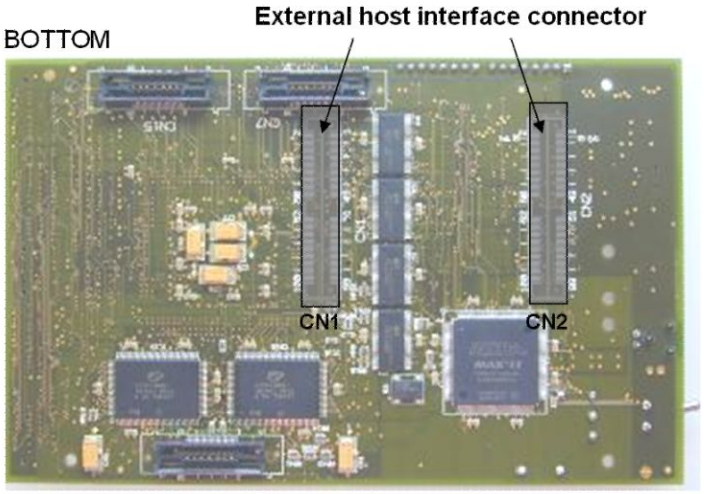

Figure 4-10 External host interface connector (CN1 and CN2)

4.6.1.1 Host Interface Signal List

Table 4-3 External host interface signal list

Signal name	Signal type	Function
A_P1...25	Input	Address bus
D_P0...31	bidirectional	Data bus
PCS_P0...5	Input	Chip select
PCD_P0...3	Input	Byte enable
PCT_P4	Input	Write signal
PCT_P5	Input	Read signal
PCM_P0	output	Wait signal

Caution The chip select 2 from the host interface can be used to control the IMAPCAR chip or to reset the IMAPCAR-USB2 board. This depends on SW2 configuration.

4.6.1.2 Connectors Pinning (CN1 and CN2)

Table 4-4 SMD connector (CN1) external host interface

Index on CN1	Signal name	Index on CN1	Signal name
2	NC	1	NC
4	NC	3	NC
6	A_P2	5	A_P1
8	A_P4	7	A_P3
10	A_P6	9	A_P5
12	A_P8	11	A_P7
14	A_P10	13	A_P9
16	A_P12	15	A_P11
18	A_P14	17	A_P13
20	A_P16	19	A_P15
22	A_P18	21	A_P17
24	A_P20	23	A_P19

Index on CN1	Signal name	Index on CN1	Signal name
26	D_P0	25	A_P21
28	D_P2	27	D_P1
30	D_P4	29	D_P3
32	D_P6	31	D_P5
34	D_P8	33	D_P7
36	D_P10	35	D_P9
38	D_P12	37	D_P11
40	D_P14	39	D_P13
42	D_P16	41	D_P15
44	D_P18	43	D_P17
46	D_P19	45	PCT5
48	D_P20	47	NC
50	D_P21	49	NC
52	D_P22	51	NC
54	D_P23	53	NC
56	D_P24	55	NC
58	D_P25	57	NC
60	D_P26	59	NC
62	D_P27	61	NC
64	NC	63	NC
66	D_P28	65	NC
68	D_P30	67	D_P29
70	PCM_P0	69	D_P31
72	NC	71	NC
74	PCT_P4	73	NC
76	PCD_P2	75	NC
78	PCD_P4	77	PCD_P3
80	PCS_P0	79	PCD_P5
82	NC	81	PCS_P2
84	PCS_P4	83	PCS_P3
86	NC	85	NC
88	NC	87	NC
90	NC	89	NC
92	NC	91	NC
94	NC	93	NC
96	NC	95	NC
98	NC	97	NC
100	NC	99	NC
		101	GND

Table 4-5 SMD connector (CN2) external host interface

Index on CN2	Signal name	Index on CN2	Signal name
2	Reserved	1	Reserved

Index on CN2	Signal name	Index on CN2	Signal name
4	Reserved	3	Reserved
6	Reserved	5	Reserved
8	Reserved	7	Reserved
10	Reserved	9	Reserved
12	Reserved	11	Reserved
14	Reserved	13	Reserved
16	NC	15	Reserved
18	NC	17	NC
20	NC	19	NC
22	NC	21	NC
24	NC	23	NC
26	NC	25	NC
28	NC	27	NC
30	NC	29	NC
32	NC	31	NC
34	NC	33	NC
36	NC	35	NC
38	NC	37	NC
40	NC	39	NC
42	NC	41	NC
44	NC	43	NC
46	NC	45	NC
48	NC	47	NC
50	NC	49	NC
52	P8_P0	51	A_P22
54	P8_P1	53	A_P23
56	P8_P2	55	A_P24
58	P8_P3	57	A_P25
60	P8_P4	59	NC
62	P8_P5	61	NC
64	P8_P6	63	P11_P0
66	P9_P0	65	P11_P1
68	P9_P1	67	P11_P2
70	P9_P2	69	P11_P3
72	P9_P3	71	P11_P4
74	P9_P4	73	P11_P5
76	P9_P5	75	P1_P0
78	P9_P6	77	P1_P1
80	P4_P0	79	P1_P2
82	P4_P1	81	P1_P3
84	P4_P2	83	P1_P4
86	P4_P3	85	P1_P5
88	P4_P4	87	P1_P6

Index on CN2	Signal name	Index on CN2	Signal name
90	P4_P5	89	P1_P7
92	P3_P0	91	P2_P0
94	P3_P1	93	P2_P1
96	P3_P2	95	P2_P2
98	P3_P3	97	P2_P3
100	P2_P5	99	P2_P4
		101	GND

4.6.1.3 "V850/PHO3 AUTOSAR Starter Kit" Port Functions

When using the V850/PHO3 Autosar starter kit to control the IMAPCAR-USB2 board, the ports that are connected to the Host interface connector have advanced features as described in the table below.

Table 4-6 V850/PHO3 starter kit ports functions

Port	PIN count	Functional description
P1	8	Timers TAA0 to TAA3 channels
P2	6	Timers TAA4 to TAA7 channels
P3	4	UARTC0 & UARTC1
P4	6	CSIB0 & CSIB1
P7	4	Address extension bits A22..A25 (used for the parallel interface)
P8	7	CSIE0, CAN2 & CAN3
P9	7	CSIE1 (with 4CS)
P11	6	Timers TMS0 & TMS1 input channels

4.6.2 Video Input and Output Connectors

The video output and input are available on SMD connectors CN3 and CN13 respectively for the video input and output signals.

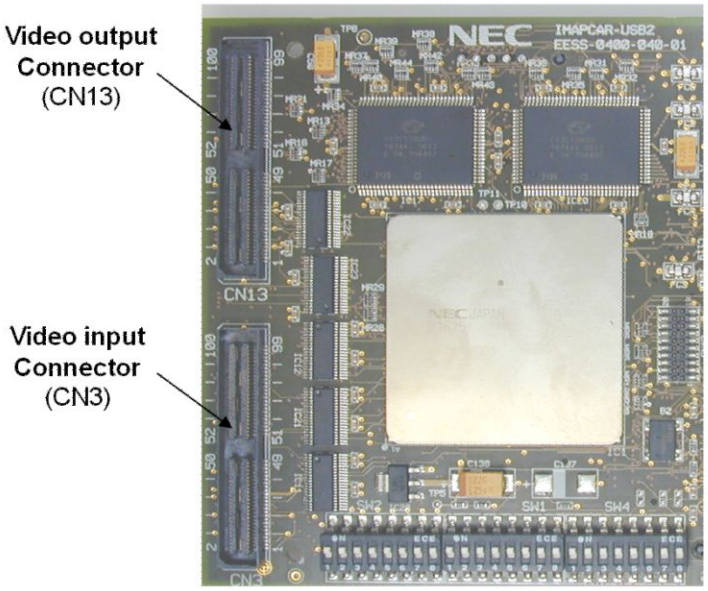

Figure 4-11 Video connectors (CN3 and CN13)

4.6.2.1 Interrupt Signals

The interrupt signals INT0…5 are dedicated to the video interface. For an easier usage, the IMAPCAR has an auto-interrupt generator integrated. This will generate all video interrupt signals from the ODDEVEN, HSYNC and VSYNC signals. Moreover, three general purpose interrupts are provided via three pins VINTAB6...8 and one is coming from the host interface access.

Table 4-7 Interrupt signal specification

Signal name	With auto-interrupt generator	Without auto-interrupt generator
VINT_AB0	ODDEVEN (odd/even field signal)	Video processing interrupt signal
VINT_AB1	HSYNC (Horizontal synchronization)	Video processing interrupt signal
VINT_AB2	VSYNC (Vertical synchronization)	Video processing interrupt signal
VINT_AB3	Use prohibited	Video processing interrupt signal
VINT_AB4	Use prohibited	Video processing interrupt signal
VINT_AB5	Use prohibited	Video processing interrupt signal
VINT_AB6	General purpose interrupt signal	
VINT_AB7	General purpose interrupt signal	
VINT_AB8	General purpose interrupt signal	

4.6.2.2 Video Interface Singal List

The video input and output boards contain the video signals and share the synchronization and clock signals. The acknowledge output pins are available on the connectors but most often they are used only for test purposes.

In addition, some signals from the host interface connector are provided to the two boards. These nets can be used either for the communication between the boards and the microcontrollers or for inter-boards communication.

Table 4-8 Video input interface signals list (CN3)

Signal name	Signal type	Function
SRI_AB0...23	Input	Parallel pixel representation for video input to IMAPCAR
SCLK_AB	Input	Pixel clock
VINT_AB0...7	Input	Interrupt signals.
VACK_AB0...5	Output	Acknowledge of video interrupts
P1_P0...7	Bidirectional	Port 1 provided by V850/PHO3 starter kit board
P2_P0...5	Bidirectional	Port 2 provided by V850/PHO3 starter kit board
P3_P0...3	Bidirectional	Port 3 provided by V850/PHO3 starter kit board
P4_P0...5	Bidirectional	Port 4 provided by V850/PHO3 starter kit board
P8_P0...6	Bidirectional	Port 8 provided by V850/PHO3 starter kit board
P9_P0...6	Bidirectional	Port 9 provided by V850/PHO3 starter kit board
P11_P0...5	Bidirectional	Port 11 provided by V850/PHO3 starter kit board

Table 4-9 Video output interface signals list (CN13)

Signal name	Signal type	Function
SRO_AB0...23	Output	Parallel pixel representation for video input to IMAPCAR
SCLK_AB	Output	Pixel clock
VINT_AB0...7	Output	Interrupt signals. With auto-interrupt generator: - VINT_AB0 : Field - VINT_AB1 : VSYNC - VINT_AB2 : HSYNC
VACK_AB0...5	Output	Acknowledge of video interrupts
P1_P0...7	Bidirectional	Port 1 provided by V850/PHO3 starter kit board
P2_P0...5	Bidirectional	Port 2 provided by V850/PHO3 starter kit board
P3_P0...3	Bidirectional	Port 3 provided by V850/PHO3 starter kit board
P4_P0...5	Bidirectional	Port 4 provided by V850/PHO3 starter kit board
P8_P0...6	Bidirectional	Port 8 provided by V850/PHO3 starter kit board
P9_P0...6	Bidirectional	Port 9 provided by V850/PHO3 starter kit board
P11_P0...5	Bidirectional	Port 11 provided by V850/PHO3 starter kit board

4.6.2.3 Video Input Connector Signal Pinning (CN3)

Table 4-10 SMD Connector (CN3) video input connector

Index on CN3	Signal name	Index on CN3	Signal name
1	SRI_AB0	2	SRI_AB1
3	SRI_AB2	4	SRI_AB3
5	SRI_AB4	6	SRI_AB5
7	SRI_AB6	8	SRI_AB7
9	VDD2.5	10	VDD3.3
11	SRI_AB8	12	SRI_AB9
13	SRI_AB10	14	SRI_AB11
15	SRI_AB12	16	SRI_AB13
17	SRI_AB14	18	SRI_AB15
19	VDD2.5	20	VDD3.3

Index on CN3	Signal name	Index on CN3	Signal name
21	SRI_AB16	22	SRI_AB17
23	SRI_AB18	24	SRI_AB19
25	SRI_AB20	26	SRI_AB21
27	SRI_AB22	28	SRI_AB23
29	VDD1.2	30	VDD5
31	VDD1.2	32	SCLK_AB
33	NC	34	VDD5
35	VINT_AB0	36	VINT_AB1
37	VINT_AB2	38	VINT_AB3
39	VINT_AB4	40	VINT_AB5
41	VINT_AB6	42	VINT_AB7
43	VINT_AB8	44	VDD5
45	VACK_AB0	46	VACK_AB1
47	VACK_AB2	48	VACK_AB3
49	VACK_AB4	50	VACK_AB5
51	P8_P0	52	GND
53	P8_P1	54	GND
55	P8_P2	56	GND
57	P8_P3	58	GND
59	P8_P4	60	GND
61	P8_P5	62	GND
63	P8_P6	64	P11_P0
65	P9_P0	66	P11_P1
67	P9_P1	68	P11_P2
69	P9_P2	70	P11_P3
71	P9_P3	72	P11_P4
73	P9_P4	74	P11_P5
75	P9_P5	76	P1_P0
77	P9_P6	78	P1_P1
79	P4_P0	80	P1_P2
81	P4_P1	82	P1_P3
83	P4_P2	84	P1_P4
85	P4_P3	86	P1_P5
87	P4_P4	88	P1_P6
89	P4_P5	90	P1_P7
91	P3_P0	92	P2_P0
93	P3_P1	94	P2_P1
95	P3_P2	96	P2_P2
97	P3_P3	98	P2_P3
99	P2_P5	100	P2_P4
101	GND		

4.6.2.4 Video Output Connector Signal Pinning (CN13)

Table 4-11 SMD Connector (CN13) video output connector

Index on CN3	Signal name	Index on CN3	Signal name
1	SRO_AB0	2	SRO_AB1
3	SRO_AB2	4	SRO_AB3
5	SRO_AB4	6	SRO_AB5
7	SRO_AB6	8	SRO_AB7
9	VDD2.5	10	VDD3.3
11	SRO_AB8	12	SRO_AB9
13	SRO_AB10	14	SRO_AB11
15	SRO_AB12	16	SRO_AB13
17	SRO_AB14	18	SRO_AB15
19	VDD2.5	20	VDD3.3
21	SRO_AB16	22	SRO_AB17
23	SRO_AB18	24	SRO_AB19
25	SRO_AB20	26	SRO_AB21
27	SRO_AB22	28	SRO_AB23
29	VDD1.2	30	VDD5
31	VDD1.2	32	SCLK_AB
33	NC	34	VDD5
35	VINT_AB0	36	VINT_AB1
37	VINT_AB2	38	VINT_AB3
39	VINT_AB4	40	VINT_AB5
41	VINT_AB6	42	VINT_AB7
43	VINT_AB8	44	VDD5
45	VACK_AB0	46	VACK_AB1
47	VACK_AB2	48	VACK_AB3
49	VACK_AB4	50	VACK_AB5
51	P8_P0	52	GND
53	P8_P1	54	GND
55	P8_P2	56	GND
57	P8_P3	58	GND
59	P8_P4	60	GND
61	P8_P5	62	GND
63	P8_P6	64	P11_P0
65	P9_P0	66	P11_P1
67	P9_P1	68	P11_P2
69	P9_P2	70	P11_P3
71	P9_P3	72	P11_P4
73	P9_P4	74	P11_P5
75	P9_P5	76	P1_P0
77	P9_P6	78	P1_P1
79	P4_P0	80	P1_P2
81	P4_P1	82	P1_P3

Index on CN3	Signal name	Index on CN3	Signal name
83	P4_P2	84	P1_P4
85	P4_P3	86	P1_P5
87	P4_P4	88	P1_P6
89	P4_P5	90	P1_P7
91	P3_P0	92	P2_P0
93	P3_P1	94	P2_P1
95	P3_P2	96	P2_P2
97	P3_P3	98	P2_P3
99	P2_P5	100	P2_P4
101	GND		

4.6.3 Test Connector

For test purposes, a connector is provided where some signals can be taken. This chapter describes the list of functions available.

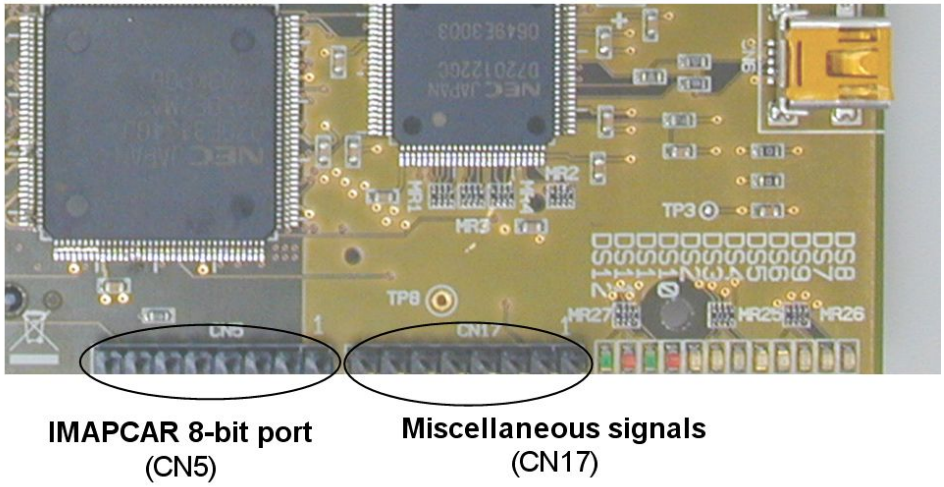

Figure 4-12 Test connectors

Pin n°	8	7	6	5	4	3	2	1
Function	IMAPCAR port 7	IMAPCAR port 6	IMAPCAR port 5	IMAPCAR port 4	IMAPCAR port 3	IMAPCAR port 2	IMAPCAR port 1	IMAPCAR port 0

Figure 4-13 IMAPCAR 8-bit port (CN5)

Pin n°	8	7	6	5	4	3	2	1
Function	GND	3.3V	2.5V	1.2V	N.C.	ERROUT	BREAK	SCLKVLD

Figure 4-14 Miscellaneous signals (CN17)

4.6.4 USB2 Interface

The µPD720122 provides the USB2 PHY core and the BUS Interface Unit. The control of the USB2 is done in the external microcontroller V850/MA3. Its role is to make the gateway between the USB2 communication and the IMAPCAR.

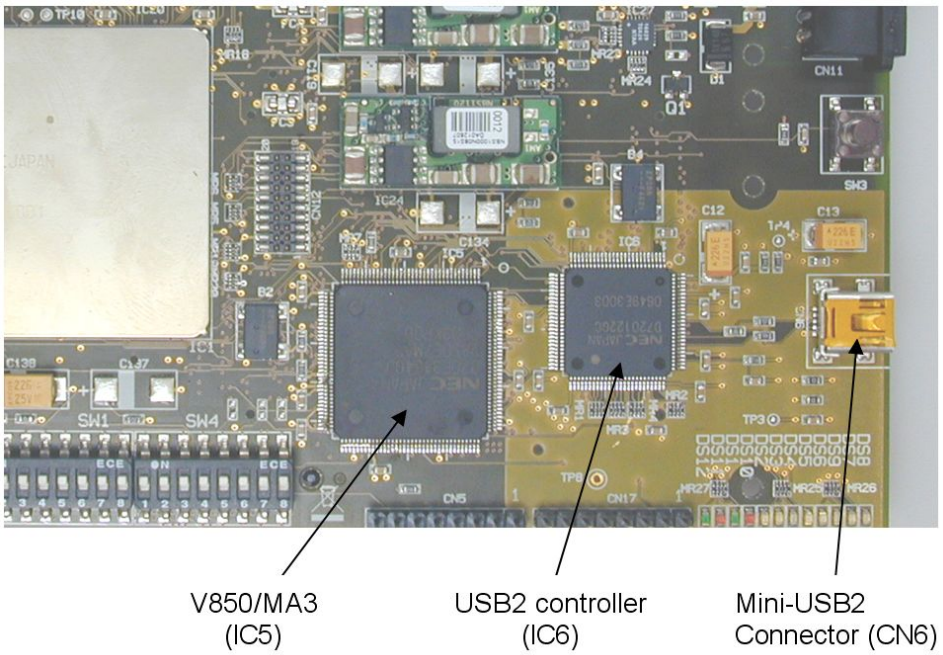

Figure 4-15 USB2 function location

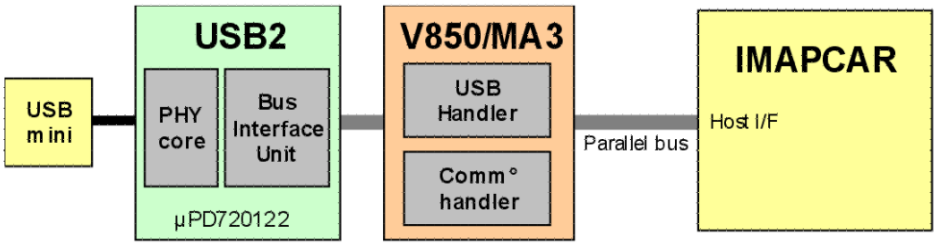

Figure 4-16 USB2 interface block diagram

4.7 IMAPCAR Configuration

The IMAPCAR chip is controlled by several DIL-Switches through the CPLD. These DIL-Switches are shown in Figure 4-17. The DIL-Switch setting to ON will apply low signal level and setting to OFF will apply high signal level to the corresponding signal. This is valid for all DIL-Switches mentioned in this chapter.

The signals that are mentioned in this chapter have to be set before the reset signal becomes inactive.

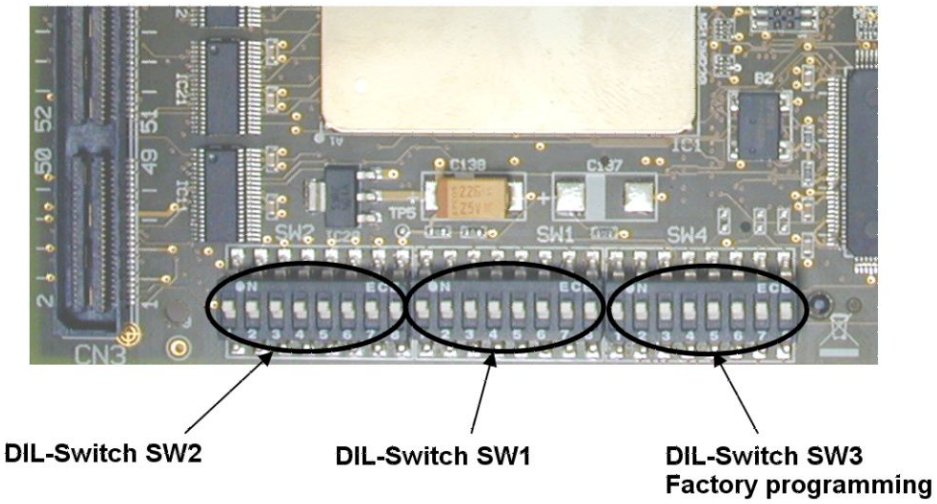

Figure 4-17 IMAPCAR-USB2 switches location

4.7.1 Video Validation and Host Interface Configuration (SW1)

The operation mode of the IMAPCAR-USB2 prototype chip is determined by DIL-Switch SW1.

Figure 4-18 DIL-switch for mode setting (SW1)

Note The default setting is shaded in grey colour.

4.7.1.1 Video Interface Validation Switches

Table 4-12 Video interface validation switches

SW1-1	Video input validation
OFF	Video input discarded
ON	Video input processed

SW1-2	Video output validation
OFF	Video output discarded
ON	Video output processed

4.7.1.2 External Host Interface Configuration

Table 4-13 External host interface configuration

SW1-3	External host interface endian
OFF	Big endian
ON	Little endian

SW1-4	External host interface bus width setting
OFF	16-bits
ON	32-bits

SW1-4	External host interface wait active select
OFF	Active low
ON	Active high

SW1-6	SW1-7	External host interface wait inactive timing settings
OFF	OFF	WAIT_B goes inactive at read data output
ON	OFF	WAIT_B goes inactive one clock cycle after read data output
OFF	ON	WAIT_B goes inactive two clock cycle after read data output
ON	ON	WAIT_B goes inactive three clock cycle after read data output

4.7.2 IMAPCAR PLL Setting and Board Behaviour (SW2)

The control of endianness, debug purpose and start-up memory map of the System-on-Chip Lite+ prototype chip is controlled by DIL-Switch SW2.

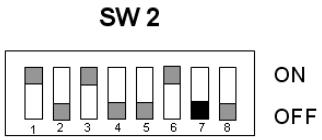

Figure 4-19 DIL-switch for control settings (SW2)

Note The default settings are shaded in grey colour.

4.7.2.1 IMAPCAR PLL Setting

Table 4-14 SMD Connector (CN13) video output connector

SW2-1	SW2-2	IMAPCAR PLL multiplier settings
OFF	OFF	X3 : 60MHz IMAPCAR operation
ON	OFF	X4 : 80MHz IMAPCAR operation
OFF	ON	X5 : 100 MHz IMAPCAR operation

SW2-1	SW2-2	IMAPCAR PLL multiplier settings
ON	ON	X6 : Prohibited setting

4.7.2.2 External Host Interface Configuration

Table 4-15 SMD Connector (CN13) video output connector

SW2-3	Chip select linked to IMAPCAR
OFF	IMAPCAR is mapped to the CS2 area
ON	IMAPCAR is mapped to the CS3 area

SW2-4	Host interface specific configuration
OFF	MA3 configuration
ON	Custom host interface configuration

SW2-5	SW2-6	Host interface master selection
OFF	OFF	Prohibited
ON	OFF	External host interface
OFF	ON	USB interface
ON	ON	Prohibited

4.7.2.3 External Reset Validation

Table 4-16 External reset configuration

SW2-8	Host interface specific configuration
OFF	The CS2 pin is used as external reset source
ON	No external reset is available

The default settings are shaded in grey colour.

4.8 Control of Status LEDs

Two LEDs show the status of the IMAPCAR-USB2 system controlled by the CPLD and DIL-Switch SW2 as mentioned in chapter 4.4.2.

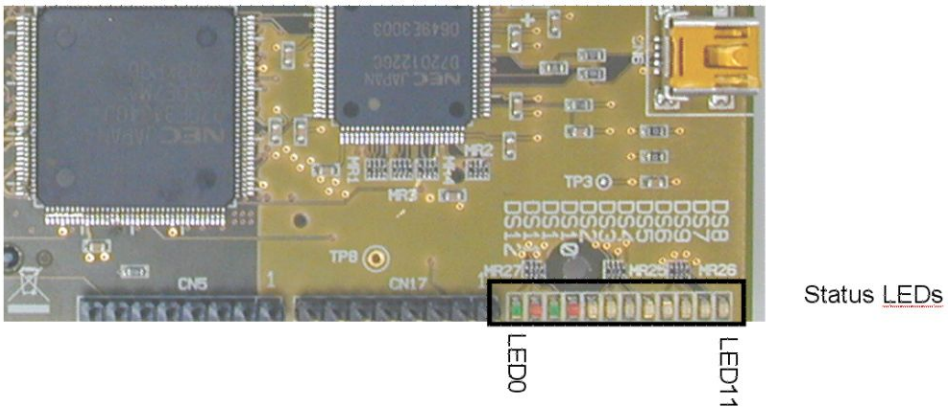

Figure 4-20 Status LEDs IMAPCAR-USB2 board

LED signification:

- LED0 (Green) On: USB interface selected / Off: USB interface not selected
- LED1 (Red) Flashing: USB access attempt / Non-flashing: No USB access attempt
- LED2 (Green) On: External host interface selected / Off: External host interface not selected
- LED3 (Red) Flashing: External host transferring / Non-flashing: External host not transferring
- LED4 (Orange) On: Video input validated / Off: Video input inhibited
- LED5 (Orange) On: Video output validated / Off: Video output inhibited
- LED6(Orange) On: IMAPCAR is in Break mode / Off: IMAPCAR is in run mode
- LED7(Orange) On: Video capture is working / Off: Video capture is idle
- LED8(Orange) On: Non-active chip select idle / Off: Non-active chip select request
- LED9 (Orange) Flashing: SSRAM 00-01 accessed ongoing / idle: No SSRAM 00-01 access
- LED10 (Orange) Flashing: SSRAM 00-01 accessed ongoing / idle: No SSRAM 00-01 access
- LED11(Orange) Spare (always off)

Chapter 5 Video Adapter Board Description

The video interfaces are fully customizable. The boards provided in the package are a passive board and a FPGA based board for custom logic implementation that could be used for LVDS interfacing.

5.1 LVDS Board

This board aims at prototyping different video controllers in FPGA. This FPGA is provided blank. The user has to program it.

5.1.1 Functional Description

The board embeds an Altera Stratix2 family type device which is referenced EP2S15. Three differential lines are provided via the firewire type connectors, signals like LVDS can be then connected to the FPGA. This device family implements direct LVDS serializer and de-serializer.

Moreover, LED and switches are provided to create a simple man-machine interface. In addition the video signals and the control board ports are directly connected from the connector to the FPGA.

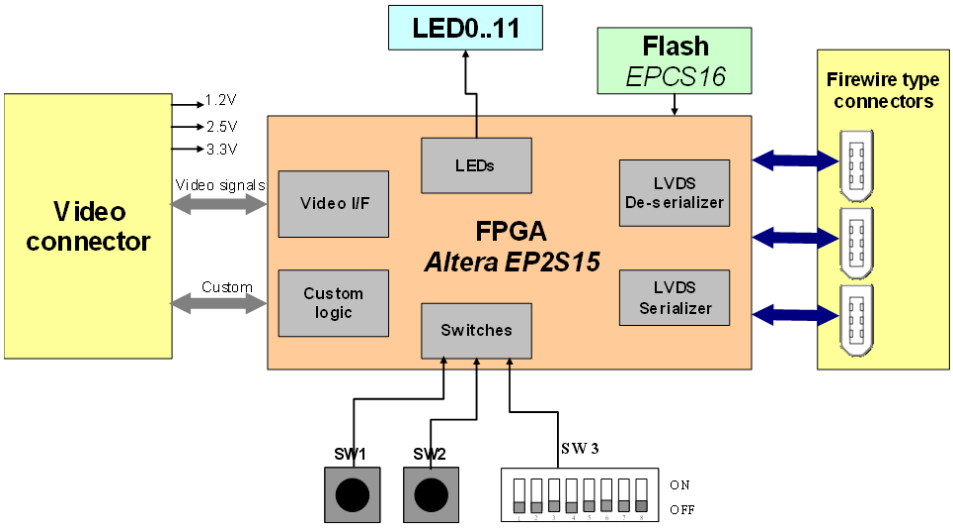

Figure 5-1 LVDS board block diagram

For a fast start, an empty project is available for this FPGA with PIN assignment already performed. You might ask for it to your local support team if needed.

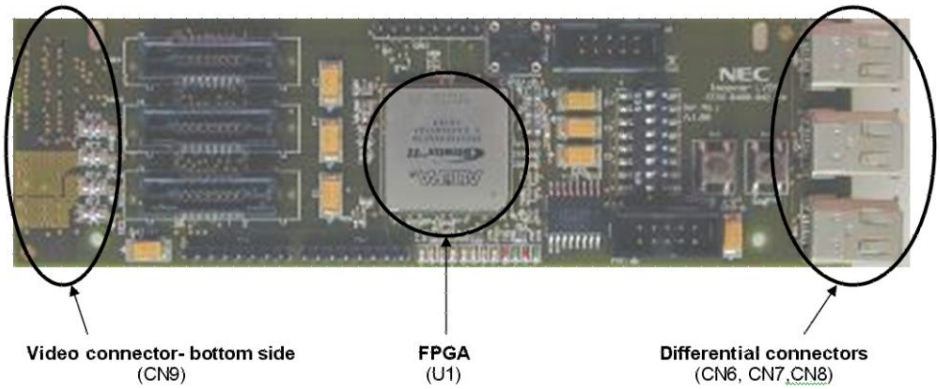

Figure 5-2 LVDS board view

5.1.2 FPGA Signal List

Table 5-1 FPGA pinning (U1)

PIN name	Signal name	PIN name	Signal name
BUTTON[0]	PIN_F6	SERIAL1[1]	PIN_K2
BUTTON[1]	PIN_C5	SERIAL1[2]	PIN_K3
CLK_UNUSED[1]	PIN_N19	SERIAL2[0]	PIN_H1
CLK_UNUSED[2]	PIN_N20	SERIAL2[1]	PIN_H2
CLK_UNUSED[3]	PIN_N4	SERIAL2[2]	PIN_H3
CLK_UNUSED[4]	PIN_M2	SERIAL3[0]	PIN_G1
CLK_UNUSED[5]	PIN_M3	SERIAL3[1]	PIN_G2
CLKIN	PIN_N3	SERIAL3[2]	PIN_G3
LED[0]	PIN_C1	SRI_AB[0]	PIN_A13
LED[1]	PIN_C2	SRI_AB[1]	PIN_B13
LED[2]	PIN_D1	SRI_AB[2]	PIN_C13
LED[3]	PIN_D2	SRI_AB[3]	PIN_D13
LED[4]	PIN_E1	SRI_AB[4]	PIN_C14
LED[5]	PIN_E2	SRI_AB[5]	PIN_D14
LED[8]	PIN_F1	SRI_AB[6]	PIN_A15
LED[9]	PIN_F2	SRI_AB[7]	PIN_B15
LED[10]	PIN_F4	SRI_AB[8]	PIN_C15
LED[11]	PIN_F5	SRI_AB[9]	PIN_D15
LVDS_RX[1]	PIN_Y1	SRI_AB[10]	PIN_A16
LVDS_RX[2]	PIN_V1	SRI_AB[11]	PIN_B16
LVDS_RX[3]	PIN_T1	SRI_AB[12]	PIN_C16
LVDS_TX[1]	PIN_W3	SRI_AB[13]	PIN_A17
LVDS_TX[2]	PIN_U4	SRI_AB[14]	PIN_B17
LVDS_TX[3]	PIN_R5	SRI_AB[15]	PIN_C17
P1_P[0]	PIN_Y18	SRI_AB[16]	PIN_A18
P1_P[1]	PIN_AA18	SRI_AB[17]	PIN_B18
P1_P[2]	PIN_AB18	SRI_AB[18]	PIN_C18
P1_P[3]	PIN_Y17	SRI_AB[19]	PIN_D18

PIN name	Signal name	PIN name	Signal name
P1_P[4]	PIN_AA17	SRI_AB[20]	PIN_A19
P1_P[5]	PIN_AB17	SRI_AB[21]	PIN_B19
P1_P[6]	PIN_AA16	SRI_AB[22]	PIN_E18
P1_P[7]	PIN_AB16	SRI_AB[23]	PIN_E19
P2_P[0]	PIN_Y14	SWITCH[0]	PIN_A8
P2_P[1]	PIN_AA13	SWITCH[1]	PIN_B8
P2_P[2]	PIN_AB13	SWITCH[2]	PIN_C8
P2_P[3]	PIN_Y13	SWITCH[3]	PIN_A7
P2_P[4]	PIN_Y12	SWITCH[4]	PIN_B7
P2_P[5]	PIN_AA12	SWITCH[5]	PIN_C7
P3_P[0]	PIN_Y16	SWITCH[6]	PIN_A6
P3_P[1]	PIN_Y15	SWITCH[7]	PIN_B6
P3_P[2]	PIN_AA15	TESTPORT[0]	PIN_B12
P3_P[3]	PIN_AB15	TESTPORT[1]	PIN_C12
P4_P[0]	PIN_W20	TESTPORT[2]	PIN_B11
P4_P[1]	PIN_W21	TESTPORT[3]	PIN_C11
P4_P[2]	PIN_W22	TESTPORT[4]	PIN_A10
P4_P[3]	PIN_V18	TESTPORT[5]	PIN_B10
P4_P[4]	PIN_Y21	TESTPORT[6]	PIN_C10
P4_P[5]	PIN_Y22	TESTPORT[7]	PIN_B9
P8_P[0]	PIN_K22	TP[0]	PIN_Y10
P8_P[1]	PIN_J20	TP[1]	PIN_AA10
P8_P[2]	PIN_J21	TP[2]	PIN_AB10
P8_P[3]	PIN_K20	TP[3]	PIN_Y9
P8_P[4]	PIN_K21	TP[4]	PIN_AA9
P8_P[5]	PIN_L20	TP[5]	PIN_Y8
P8_P[6]	PIN_L21	TP[6]	PIN_AA8
P9_P[0]	PIN_P19	TP[7]	PIN_AB8
P9_P[1]	PIN_P20	VACK_AB[0]	PIN_G20
P9_P[2]	PIN_P21	VACK_AB[1]	PIN_G21
P9_P[3]	PIN_R21	VACK_AB[2]	PIN_G22
P9_P[4]	PIN_R22	VACK_AB[3]	PIN_H20
P9_P[5]	PIN_T21	VACK_AB[4]	PIN_H21
P9_P[6]	PIN_T22	VACK_AB[5]	PIN_H22
P11_P[0]	PIN_U20	VINT_AB[0]	PIN_C21
P11_P[1]	PIN_U21	VINT_AB[1]	PIN_C22
P11_P[2]	PIN_U22	VINT_AB[2]	PIN_D21
P11_P[3]	PIN_V19	VINT_AB[3]	PIN_D22
P11_P[4]	PIN_V21	VINT_AB[4]	PIN_E20
P11_P[5]	PIN_V22	VINT_AB[5]	PIN_E22
RESETZ	PIN_AB5	VINT_AB[6]	PIN_E21
SCLK_AB	PIN_M21	VINT_AB[7]	PIN_F21
SERIAL1[0]	PIN_K1	VINT_AB[8]	PIN_F22

5.2 Passive Board

This board intends at being used for test and prototyping. This can be plugged to a camera module for example as well as being used in combination with a TFT screen display.

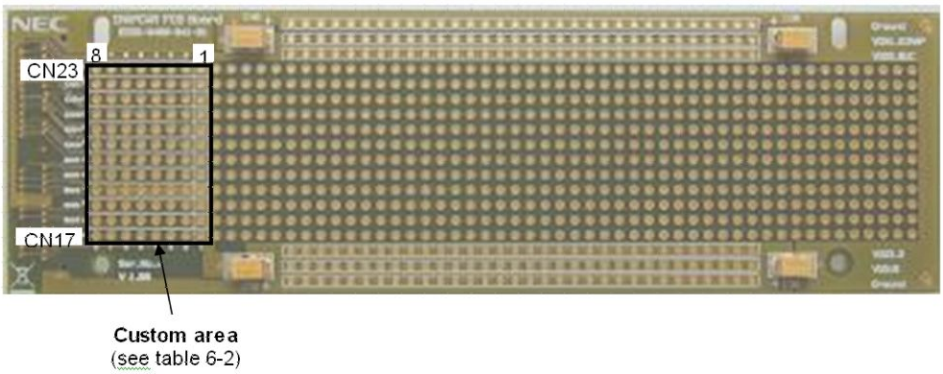

Figure 5-3 Passive board

Connector	8	7	6	5	4	3	2	1
CN23	P3_P1	P3_P0	P2_P5	P2_P4	P2_P3	P2_P2	P2_P1	P2_P0
CN21	P4_P5	P4_P4	P4_P3	P4_P2	P4_P1	P4_P0	P3_P3	P3_P2
CN24	P1_P7	P1_P6	P1_P5	P1_P4	P1_P3	P1_P2	P1_P1	P1_P0
CN19	P8P0	P9_P6	P9_P5	P9_P4	P9_P3	P9_P2	P9_P1	P9_P0
CN14	NC	NC	P11_P5	P11_P4	P11_P3	P11_P2	P11_P1	P11_P0
CN13	NC	NC	P8_P6	P8_P5	P8_P4	P8_P3	P8_P2	P8_P1
CN16	NC	VACK_AB5	VACK_AB4	VACK_AB3	VACK_AB2	VACK_AB1	VACK_AB0	VINT_AB8
CN22	VINT_AB7	VINT_AB6	VINT_AB5	VINT_AB4	VINT_AB3	VINT_AB2	VINT_AB1	VINT_AB0
CN18	GND	GND	GND	GND	SCLK_AB	GND	GND	GND
CN20	SR_AB23	SR_AB22	SR_AB21	SR_AB20	SR_AB19	SR_AB18	SR_AB17	SR_AB16
CN15	SR_AB15	SR_AB14	SR_AB13	SR_AB12	SR_AB11	SR_AB10	SR_AB9	SR_AB8
CN17	SR_AB7	SR_AB6	SR_AB5	SR_AB4	SR_AB3	SR_AB2	SR_AB1	SR_AB0

Chapter 6 Board Operation

This chapter explains practical usage of the IMAPCAR-USB2 development board.

6.1 Development Tool Mode

The IMAPCAR-USB2 board can be used in development tool mode controlled by a PC, with or without video input/output boards connected to it.

In the example figure 6-1, an analog video input and an analog video output board are connected to it. For more details on the video interface, please refer to the chapter 4.5.2 Video input and output connector.

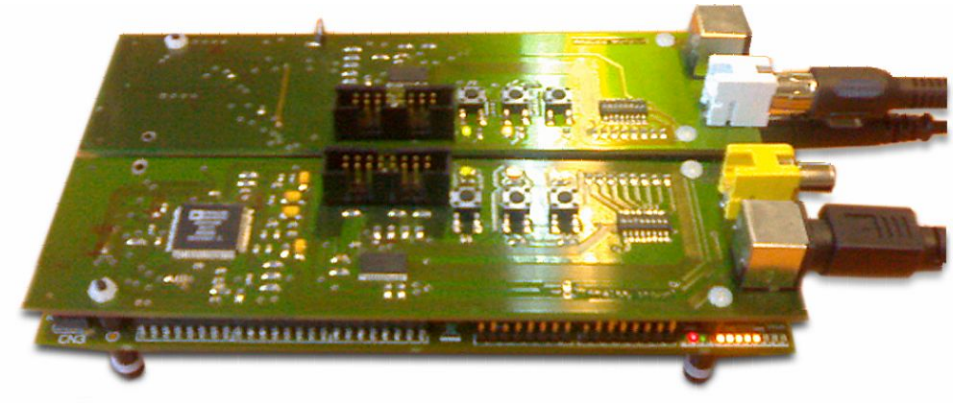

Figure 6-1 IMAPCAR-USB2 in development tool mode

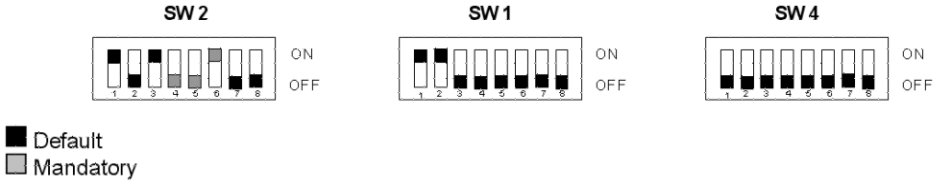

Figure 6-2 Default jumper configuration for development tool mode

Getting started

This chapter gives a “step-by-step” description, how to start with the development board.

- Check if all DIP switches are in their default position (USB position)
- Connect the IMAPCAR-USB2 development board with the USB cable to a host PC with the SDBIMAP software installed.
- Connect the power supply to the board.
- Power-on the board.
- Start the SDBIMAP SW.

Now the board is ready to be controlled by the development tools environment. If used in video mode, the LED9 (orange) should be flashing and possibly the LED10 as well.

6.2 Demonstrator Mode

The IMAPCAR-USB2 board can be used in demonstrator mode while being controlled by an external supervisor microcontroller.

In the example 6-2, the video input and output boards provided in the example bellow are the analog input and output boards.

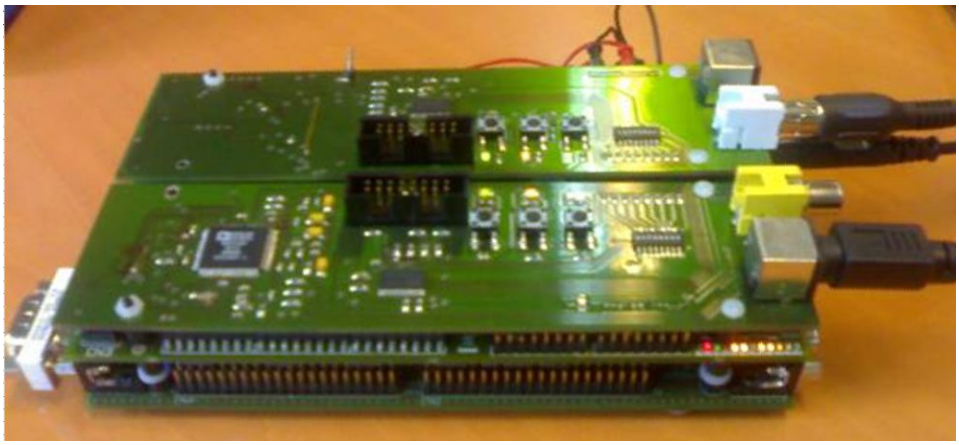

Figure 6-3 IMAPCAR-USB2 in demonstrator mode

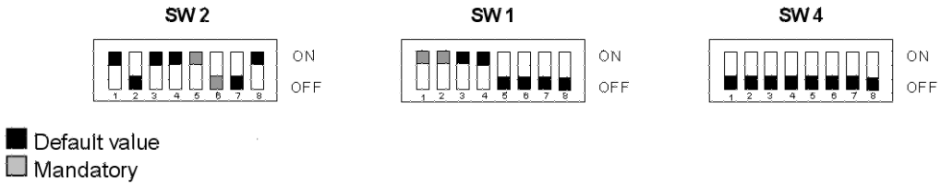

Figure 6-4 Default jumper configuration for demonstrator mode

Getting started

This chapter gives a “step-by-step” description, how to start up the demonstrator kit.

- Check if all DIP switches are in their default position (External host interface position)
- Connect the IMAPCAR-USB2 development board to the supervisor microcontroller board
- Connect the power supply to both boards.
- Power-on the IMAPCAR-USB2 board and wait a few seconds.
- Power-on the supervisor microcontroller board.

The board should be running. To make sure the video flow is well capture, the LED9 (orange) should be flashing and possibly the LED10.