Aeroflex Colorado Springs
RadHard Eclipse FPGA
Frequently Asked Questions

(NOTE - FAQs WILL BE UPDATED ON A REGULAR BASIS)

Introduction:

QuickLogic has licensed their metal-to-metal Vialink™ technology to Aeroflex Colorado Springs (Aeroflex). The agreement calls for Aeroflex to have access to QuickLogic's Embedded Standard Product (ESP) and FPGA technology.

Questions and Answers:

Question 1)

What kind of products will Aeroflex design with the QuickLogic technology?

Answer 1)

We will offer non-volatile 0.25µm Radiation Hardened (RadHard) Eclipse FPGA suitable for all space missions. The first device offered is the UT6325. Aeroflex plans to provide many new programmable products with the QuickLogic technology.

Question 2)

What is the procurement vehicle for these products? Will DSCC SMD numbers be assigned?

Answer 2)

Yes, the SMD number has been assigned – 5962-04229 – and the device will be qualified as QML Q and QML V.

Question 3)

How will these products be packaged for space applications?

Answer 3)

RadHard Eclipse FPGA Packages		QuickLogic FPGA (Prototyping Option)
CQFP208	PQFP208	PQFP208
CQFP288	PBGA280	PBGA280
CCGA/CLGA484	PBGA484	PBGA484

We are offering PCB footprints with lead-forming guidelines for the 208-CQFP/208-PQFP and 288-CQFP. We are also offering socket adapters for 280 BPGA and 484 PBGA to match the socket for a plastic package to the corresponding ceramic footprint (i.e. 280 PBGA/288 CQFP, 484 PBGA/484 CLGA).

Question 4)

What type of radiation goals do you have for these products?

Answer 4)

Radiation Target for Aeroflex RadHard Eclipse FPGA	
Total Ionizing Dose	100/300 krad (Si)
Single Event Latch-up (SEL)	> 120 MeV-cm^2/mg
Single Event Upsets (SEU)	< 10^{-8} Errors/Bit-Day.

Question 5)

What orbits will the products be targeted for?

Answer 5)

Low, middle, high earth and deep space orbits. (All space missions)

Question 6)

What reliability goals do you have for the new products?

Answer 6)

We plan to demonstrate less than 10 FITS.

Question 7)

What voltages will be available?

Answer 7)

For the RadHard Eclipse products, they will use 2.5volt core and 3.3volt I/Os.

Question 8)

Since the VCC and VCCIO are different power supplies (i.e. I/O at 3.3V), is there any sequence to providing power to the device.

Answer 8)

There is no functional failures on UT6325 regardless of power sequence and no in-rush current effects identified regardless of power sequencing (highest Vccio current observed = 280mA)

Aeroflex recommendations for powering-up UT6325

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1) Starting point for Power-up (Vcc-offset) should be less than 300 mV.
2) The power supply should ramp up/down monotonically.
3) The ramp up time should be more than 1 us and less than 200 ms.
4) Minimize time when supplies are at mid-range.

For QuickLogic QL6325 Prototypes:
If (Vccio-Vcc) <500mV, you do not have to worry about current spikes or forward biasing the internal diodes.
1) Vccio and Vcc ramp up to 2.5V simultaneously, then Vccio continues to 3.3V. (Vccio-Vcc) always equals zero. This is an ideal case where current consumption is normal and no power diodes are forward biased. No reliability issues.
2) Vccio ramps to 3.3V, then 500us later Vcc ramps up to 2.5V. In this case Vccio-Vcc=3.3V for 500us. Since the diode is reversed biased, no current is sinked to Vcc. However, when Vcc ramps up to 2.5V, there is a high probability that you will have a current spike of about 100~300mA. This is not a problem if the power supply used can handle the additional short-term current requirement. No reliability issues, but can cause power-up problems if the power supply can not support the greater current requirement. No permanent damage.
3) Vcc ramps to 2.5V, then 500us later Vccio ramps to 3.3V. In this case, Vccio-Vcc= ~2.5V for 500us. Since the power diodes are forward biased you will see an additional current load on the power supply. Having the diode on for long periods of time can cause a reliability problem as it can wear out the diode and subsequently damage the internal transistors. Having the diodes turned on for a few microseconds every time you power-up should not cause any reliability issues.
4) Vccio and Vcc both ramp up in less than 400us. The length of the power up sequence is for initialization of the RAM blocks. If the device is powered-up too fast, then the RAM blocks may not function correctly (i.e. false data).

Question 9)

Can the RadHard Eclipse be run with a negative voltage supply, i.e., Vcc attached to ground and Vss attached to –2.5V?

Answer 9)

Yes, since you maintain the same 2.5V potential difference from power to ground. Remember that all data inputs must now respect this new voltage bias.

Question 10)

Is the I/O buffer 5 volt tolerant?

Answer 10**)**
No. We could accept 5V inputs if the current is limited to prevent overdriving the ESD diodes. We, however, can not drive 5V out. The 5V Tolerance Application Note is available at
http://ams.aeroflex.com/ProductFiles/AppNotes/FPGA5VToleranceApNote3-06.pdf.

Question 11)

What I/O buffer capabilities are available?

Answer 11)

The I/O is 3.3V tolerant. They may interface to PCI, LVTTL, and LVCMOS3 signals**.** With the addition of an external resistor, they may also interface to LVDS and LVPECL signals. Both the input and output portions of the bi-directional I/O are registered. The I/O buffer cell also contains a pull-down resistor which may be used.

Question 12)

How many RAM cells are available on the UT6325 and how can they be configured to support EDAC for error detection and correction?

Answer 12)

The UT6325 FPGA contains 24 dual-ported RAM cells which may be cascaded to increase address depth or word width. In order to make best use of these base cells, the designer should use the RAM Compiler (the RAM/ROM/FIFO wizard) included in the QuickWorks® design tool suite, which support both devices. This will compile a RAM netlist of various depth and width to meet a specific need. As examples, if the application requires a 256x16 bit RAM with a 6 bit EDAC code, the user would input a 256 depth and 22-bit width requirement into the compiler. The Wizard would then create a Verilog/ VHDL netlist constructing this RAM configuration out of 3 separate 256x9 RAM cells. The user would then instantiate this Verilog/VHDL block into the rest of their design.

Question 13)

What is the worst case skew over military conditions that would be expected for a global or array clock distribution network?

Answer 13)

Worst case skew will not exceed 550ps for either array or global clock distribution networks.

Question 14)

Are there a maximum number of loads which may be placed on an array or global clock network?

Answer 14)

No. Each array or global distribution network is sufficiently buffered to be able to drive all flip-flop loads present in the FPGA.

Question 15)
Is the interface of the QuickLogic FPGA identical to the Aeroflex RadHard Eclipse FPGA interface in terms of driver capability etc?

Answer 15)
Yes, the I/O interface and drive is the same. The dedicated pins (dedicated clock, clock and IOCTRL) are 2.5V, LVCMOS3, compliant.

Question 16)
How do you terminate the unused I/Os?

Answer 16)
All unused I/O (bidirectional buffers) are automatically tied to ground by SpDE. The grounding structure is 200ohm resistor in series with an N-channel transistor. The gate is controlled through ViaLink™ programming. When activated, this structure has a nominal pull down current of about 75uA with the VCCIO = 3.3V.

Question 17)

Are there absolute maximum input rise and/or fall times?

Answer 17)

Our specs do not state a maximum rise and fall time for input signals that guarantees the stated prop delays in the datasheet. To say that T_{prop} is unaffected by input rise/fall times is accurate when the rise/fall times are somewhat reasonable and well behaved. If input rise fall times are extremely fast (<5ns) one may encounter issues with overshoot, ringing and reflections. Similarly, if input rise/fall are extremely slow (> 100ns), one may experience long signal delays caused by the slowness of the input signal in reaching the input switch point for the given device. If the rise/fall times are between 6ns and 15ns, the user should be able to safely use the published T_{prop} values.

Question 18)

How can you use a falling edge clock?

Answer 18)

The falling edge clocks can't be put on the clock network directly since the flip flops in the QuickLogic/Aeroflex devices are positive edge triggered. For the negative edge clocks, the user needs to invert the signal and then put it on the clock network. One can do this by (inverter then GCLKBUFF_25UM) or (CLKPAD_25UM -> inverter -> GCLKBUFF_25UM). The latter one will reduce the skew.

Question 19)

How do I assign a High Drive/IO Control network to a net?

Answer 19)

The user has to manually instantiate High Drive Pad in their design. The instantiation of the High Drive Pad is explained on page 52 of the QuickWorks User Manual.

Question 20)

What is the advantage and process to implement a PCI interface in a UT6325 FPGA?

Answer 20)

We plan to offer the UT5732 which is on the base part of UT6325 and includes a PCI Interface. The UT5732 combines the guaranteed performance of an embedded PCI controller stitched together with a flexible FPGA fabric on a single piece of silicon. With this approach, Aeroflex assists the customers in rapidly getting their products to market. By eliminating the need for the customers to deal with the PCI interface, UT5732 allows them to focus on adding value and differentiation to their PCI-based design. We have an agreement with QL to use the same core as the one QuickLogic provides to their customers. The device will be available by September, 2005.

Question 21)

What are the design goals and tools?

Answer 21)

The development software tools and programming hardware will have 100% compatibility between QuickLogic's products and Aeroflex's RadHard products. Customers may use QuickLogic's QuickWorks® design software for development and System General QL9600 Device Programmers and Adapters for programming. Customers can download the software at http://www.quicklogic.com/home.asp?PageID=326&sMenuID=210. It is QuickWorks 9.7 and click on "download now" button.

Question 22)

Are the Eclipse libraries available in a .db format for use with Synopsys FPGA Compiler?

Answer 22)

Yes.

Question 23)

Is soft IP available to the customer?

Answer 23)

Yes, customers can use QuickLogic existing IP such as UART, SDRAM controllers, PCI Core as well as Aeroflex 8051 Microcontroller IP.

Question 24)

What is the pricing for the design tools available in the QuickWorks® tool suite?

Answer 24)

QuickLogic offers an “ala carte” pricing program for design tools. Please contact your Aeroflex Regional Sales Manager or call 800-645-8862 for pricing information.

Question 25)

How do you upgrade the Lite version of Aldec license to the full version and what will be the pricing?

Answer 25)

If you ordered the QS-VERILOG (VHDL) or QS-ALD-SimVH software packages you will receive the Lite version of Active-HDL. The full version of Active-HDL requires an upgrade (AQE-VHDL-T). When ordering the full version, be sure to include C-AQE-LITE, which is a discount for customers who have already purchased the Lite version. You can contact Aldec directly to receive this upgraded license.

Aldec would like to provide QuickLogic the opportunity to upgrade all customers that have purchased a QuickLogic Lite Edition (TBL) to the QuickLogic Edition (TBL) based on the following upgrade pricing and credits. This Upgrade Option is valid until December 31, 2005.

Note: All expiration dates of the (TBL) will remain the same. (i.e., if a customer purchased QE-Lite from QuickLogic and the original expiration date of their (TBL) is June 30, 2005 and the customer purchases the full (TBL) upgrade to QuickLogic Edition their license expiration date will still remain June 30, 2005. The customer does not receive more time; they only receive a product without limitations.

Credit for QuickLogic Lite = <$600.00> (Customer must already have a valid license of QuickLogic Lite Edition and only one credit can be applied per upgrade license). Please refer to the part numbers below. North American (Time Based QuickLogic Edition Pricing), Part Number Price (All Pricing in US Dollars):
AQE-VHDL-T $2,197.25
AQE-VLOG-T $2,197.25
C-AQE-LITE <$600.00>

Question 26)
Will the QuickLogic development software support Aeroflex RadHard FPGA devices?

Answer 26)
The user will be able to target Aeroflex RadHard FPGA devices in the QuickLogic development software.

Question 27)

Will Aeroflex continue their current standard and semi-custom product offerings?

Answer 27)

Absolutely!

Question 28)

What is the pricing?

Answer 28)

Please contact your Aeroflex Regional Sales Manager or call 800-645-8862 for pricing information.

Question 29)

Who do we contact at Aeroflex about these new products?

Answer 29)

Please call:

Ron Lake, Principal Applications Engineer FPGA Products
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800-645-8862 is our toll free number