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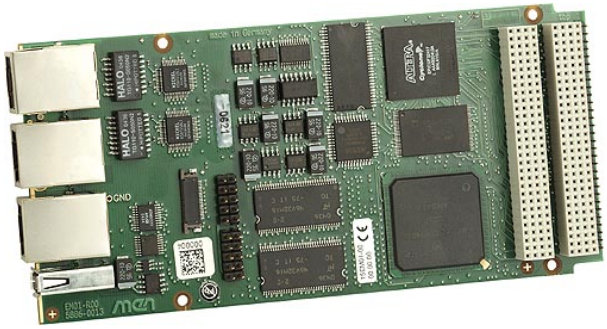
EM1 - Embedded System Module with MPC5200



- **Embedded System Module with:**
- **MPC5200 / 384 MHz**
- **FPGA 12,000 LEs (approx.144,000 gates)**
- **Up to 256 MB on-board DDR SDRAM**
- **Up to 8 MB boot Flash, NAND Flash**
- **2 MB SRAM, 16 MB additional SDRAM**
- **Fast Ethernet, COM, USB 1.1 (front)**
- **Dual CAN controller**
- **MENMON™ BIOS for PowerPC® cards**
- **COMs, graphics, IDE etc. optional via FPGA**
- **Stackable with PCI-104**

The EM1 can be supplied as a stand-alone module, with an application-specific carrier card and/or with additionally plugged PCI-104 modules.
The EM1 is controlled by the MPC5200 PowerPC® processor which was specially developed for automotive applications and which operates at up to 400 MHz and 700 MIPS. The complete ESM™ module in standard form has an operational temperature of -40 to +85°C. The CPU consumes less than 1 W at 384 MHz. The EM1 is equipped with up to 256 MB soldered SDRAM and up to 1 GB NAND Flash as well as with 16 MB additional SDRAM, up to 8 MB boot Flash and 2 MB battery-backed SRAM.
The EM1 provides one Fast Ethernet interface (second interface prepared through FPGA), one serial line and USB 1.1 at its front panel. As an alternative to RJ45, D-Sub connectors guarantee reliable functions also in harsh environments. Two CAN controllers with V2.0A/B CAN protocol are included in the MPC5200. The physical CAN interfaces are accessible via SA-Adapters™.
Further UARTs and other additional I/O functions can be realized in the on-board FPGA and accessed via a carrier board. The functionality of the FPGA is dynamically loaded by the application software.
The EM1 comes with MENMON™ support. This firmware/BIOS can be used for bootstrapping operating systems (from disk, Flash or network), for hardware testing, or for debugging applications without running any operating system.
The EM1 is designed to operate under harsh environmental conditions including -40 to +85°C operation temperature, shock, vibration, humidity. It focuses on applications in transportation (railways), automotive and avionics.
For a first evaluation of the functions of the EM1 it is strongly recommended to use the EK6 ESM™ starter kit. The kit consists of the standard CPU module, an FPGA loaded with additional I/O functions, the carrier card with I/O connectors, an external PSU, VGA and RJ45 to D-Sub cables, and an adapter for mounting a PCI-104 module.
ESM™ modules are complete computers which consist of the hardware (CPU, chip set, memory, I/O) which is not fixed to any application-specific function, and an FPGA programmed in VHDL code for user-defined I/O. ESM™ modules are based on PCI. They have two system connectors: J1 has a fixed signal assignment, while J2 is variable depending on the final application-specific configuration of the ESM™ and the carrier board. J2 also feeds the I/O signals of the functions programmed in the FPGA to the carrier card.

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Technical Data

CPU
- PowerPC®
  - MPC5200
  - Up to 400MHz

Memory
- 2x16KB L1 data and instruction cache integrated in MPC5200
- Up to 256MB SDRAM system memory
  - Soldered
  - DDR
  - 64MHz memory bus frequency
- Up to 1GB soldered NAND Flash (and more), FPGA-controlled
- 16MB additional SDRAM, FPGA-controlled, e.g. for video data and NAND Flash firmware
- Up to 8MB boot Flash
- 2MB battery-backed SRAM, or: 128KB non-volatile FRAM
- Serial EEPROM 8kbits for factory settings

Mass Storage
- Parallel IDE (PATA)
  - One port for hard-disk drives
  - Available via I/O connector
  - FPGA-controlled
- Up to 1GB soldered ATA NAND Flash (and more), FPGA-controlled

Graphics
- Available via I/O connector
- FPGA-controlled

I/O
- USB
  - One USB 1.1 port
  - Series A connector at front panel
  - OHCI implementation
  - Data rates up to 12Mbits/s
- Ethernet
  - One 10/100Base-T Ethernet channel
  - Second Ethernet channel can be implemented through update of FPGA
  - Two RJ45 or one D-Sub connector at front panel
- One RS232 UART (COM1)
  - RJ45 or D-Sub connector at front panel
  - Data rates up to 115.2kbits/s
  - 512-byte transmit/receive buffer
  - Handshake lines: CTS, RTS
- CAN bus
  - Two CAN bus channels
  - 2.0 A/B CAN protocol
  - Data rates up to 1 Mbit/s
  - Connection via on-board connectors
  - External transceivers using SA-Adapters™
- Further I/O depending on FPGA configuration

Front Connections
- One USB 1.1 (Series A)
- Two Ethernet (RJ45 or D-Sub)
- One RS232 UART COM1(RJ45 or D-Sub)

FPGA
- Standard factory FPGA configuration:
  - Main bus interface
  - 16Z070_IDEDISK - IDE controller for NAND Flash
  - 16Z043_SDRAM - Additional SDRAM controller (16MB; 1MB used for graphics)
  - 16Z023_IDENHS - IDE controller (PIO mode 0; non-hot-swap)
  - 16Z044_DISP - Display controller (800 x 600, 60Hz/70Hz, 6-bit RGB)
  - 16Z031_SPI - SPI touch panel controller
  - 16Z025_UART - UART controller (controls COM10..COM13)
  - 16Z034_GPIO - GPIO controller (6 lines)
- The FPGA offers the possibility to add customized I/O functionality. See FPGA.

PCI Interface
- 32-bit, 32-MHz PCI interface at PCI-104 connector J1
- Compliant with PCI Specification 2.2
- Support of 4 external masters

Miscellaneous
- Real-time clock
- Power supervision and watchdog

Electrical Specifications
- Supply voltage/power consumption:
  - +5V (-2%/+5%), 10mA max., only for USB
  - +3.3V (-2%/+5%), 1A typ.
- MTBF: 232,000h @ 40°C (derived from MIL-HDBK-217F)

Mechanical Specifications
- Dimensions: conforming to ESM™ specification (PCB: 149mm x 71mm), Type I-S
- Weight: 90g (w/o heat sink)

Environmental Specifications
- Temperature range (operation):
  - -40..+85°C
  - Airspeed: min. 2 m/s
- Temperature range (storage): -40..+85°C
- Relative humidity (operation): max. 95% non-condensing
- Relative humidity (storage): max. 95% non-condensing
- Altitude: -300m to + 3,000m
- Shock: 15g/11ms
- Bump: 10g/16ms
- Vibration (sinusoidal): 2g/10..150Hz
- Conformal coating on request

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Technical Data

Safety
- PCB manufactured with a flammability rating of 94V-0 by UL recognized manufacturers

EMC
- Tested according to EN 55022 (radio disturbance), IEC1000-4-2 (ESD) and IEC1000-4-4 (burst)

BIOS
- MENMON™

Software Support
- VxWorks®
- Linux (ELinOS)
- QNX®
- PikeOS (partitionable RTOS) certified platform
- CANopen firmware (Vector Informatik)
- CAN support: MEN Driver Interface System (MDIS™ for Windows®, Linux, VxWorks®, QNX®, OS-9®)
- For more information on supported operating system versions and drivers see Software.

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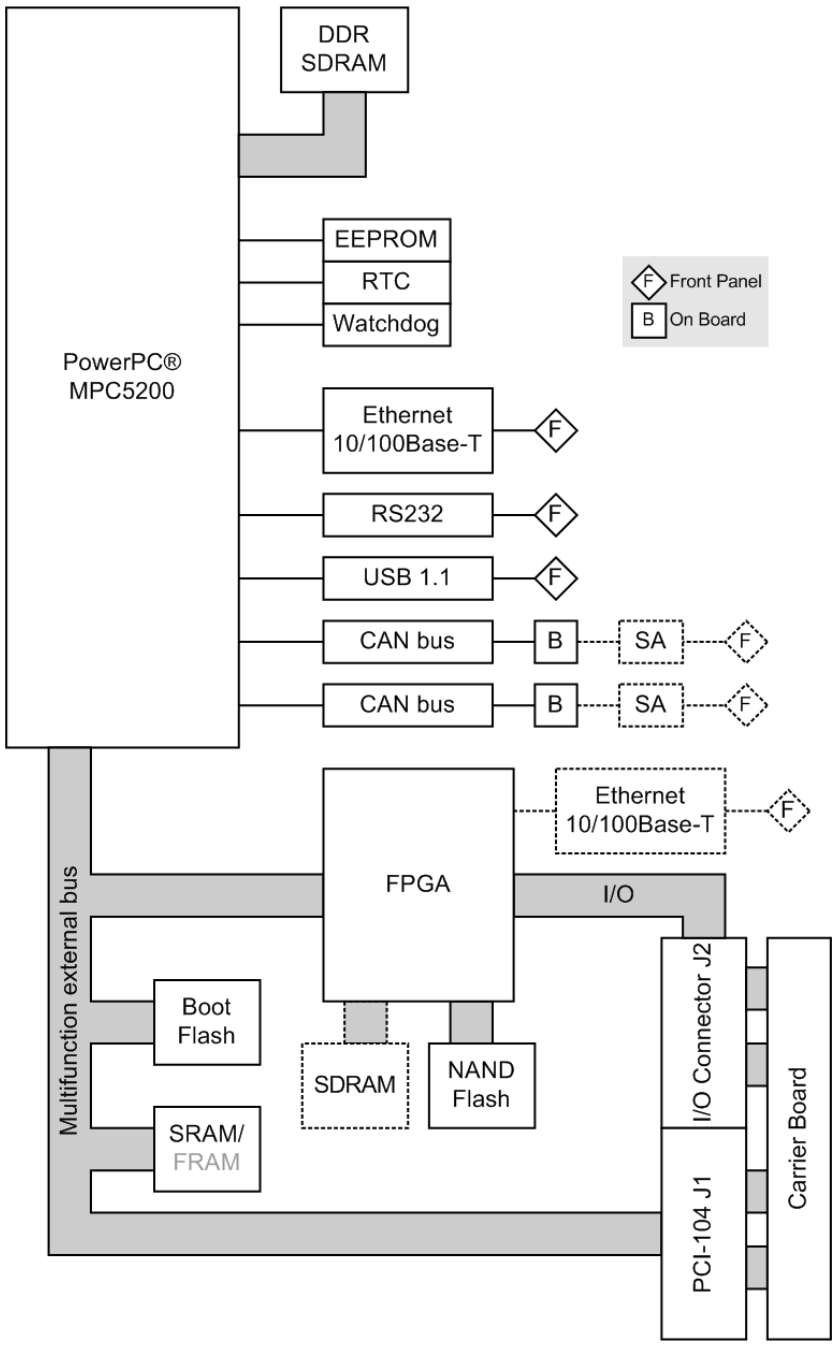
Diagram



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Configuration & Options

Standard Configurations

Article No.	CPU Type	FPGA	System RAM	NAND Flash	Boot Flash	Additional SDRAM	SRAM	Misc.
15EM01-00	MPC5200, 384MHz	12,000 LE	128 MB	128 MB	2 MB	16 MB	2 MB	Front I/O
15EM01N00	MPC5200B, 384MHz	18,752 LE	256 MB	1 GB	2 MB	16 MB	2 MB	Front I/O
15EM01A00	MPC5200B, 384MHz	18,752 LE	256 MB	128 MB	2 MB	16 MB	2 MB	Rear I/O
15EM01A01	MPC5200B, 384MHz	18,752 LE	256 MB	128 MB	2 MB	16 MB	2 MB	Rear I/O, 5V only

Options

CPU

- MPC5200, 384 MHz

Memory

- System RAM
  - 128 MB or 256 MB
- NAND Flash
  - 0 MB up to maximum available
- Boot Flash
  - 2 MB, 4 MB or 8 MB
- Additional SDRAM
  - 0 MB or 16 MB
- SRAM
  - 0 MB or 2 MB
- 128KB non-volatile FRAM instead of SRAM

I/O

- Front connections
  - D-Sub connectors for Ethernet and COM/USB
- Second Ethernet channel at front through FPGA

Mechanical

- PCI and I/O connectors can also be placed for face-to-face assembly (ESM™ Type N)

Please note that some of these options may only be available for large volumes. Please ask our sales staff for more information.

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FPGA

FPGA Capabilities

- FPGA Altera® Cyclone™ EP1C12
  - 12,060 logic elements
  - 239,616 total RAM bits
- Connection
  - Available pin count: 77 pins
  - Functions available e.g. via I/O connector

Flexible Configuration

- This MEN board offers the possibility to add customized I/O functionality in FPGA.
- It depends on the board type, pin counts and number of logic elements which IP cores make sense and/or can be implemented. Please contact MEN for information on feasibility.
- Depending on the hardware platform, SA-Adapters™ can be used to realize the physical lines.

MEN IP Cores

- MEN has a large number of standard IP cores to choose from.
- Examples:
  - IDE (e.g. PIO mode 0, UDMA mode 5)
  - UARTs
  - CAN bus
  - Display control
  - Fast Ethernet (10/100Base-T)
  - ...
- For IP cores developed by MEN please refer to our IP core overview.
  - IP Core compare chart (PDF)
- MEN also offers development of new (customized) IP cores.

Third-Party IP Cores

- Third-party IP cores can also be used in combination with MEN IP cores.
- Examples:
  - www.altera.com
  - www.opencores.org

FPGA Design Environment

- Altera® offers free download of Quartus® II Web Edition
  - Complete environment for FPGA and CPLD design
  - Includes schematic- and text-based design entry
  - Integrated VHDL and Verilog HDL synthesis and support for third-party synthesis software
  - SOPC Builder system generation software
  - Place-and-route, verification, and programming
- Altera® Quartus® II Web Edition FPGA design tool

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Ordering Information

Related Hardware

08EK06-00	ESM™ evaluation kit for EM1: Mini ATX carrier board, EM1 with PowerPC® MPC5200 / 384MHz, 128MB DDR SDRAM, 128MB NAND Flash, 2MB SRAM, 16MB graphics memory, 2 MB boot Flash, 1 Fast Ethernet, 1 UART, 1 USB 1.1, graphics, IDE, RJ45 to D-Sub cable,VGA cable, external PSU and adapter for mounting of one PCI-104 module, 0..+60°C, discontinued as of June 28, 2007
15EM01A00	MPC5200B/384MHz, FPGA 18,752 logic elements, 256MB SDRAM, 128MB NAND Flash, 2MB SRAM, 16MB graphics memory, 2MB boot Flash, -40..+85°C with qualified components
15EM01A01	MPC5200B/384MHz, FPGA 18,752 logic elements, 256MB SDRAM, 128MB NAND Flash, 2MB SRAM, 16MB graphics memory, 2MB boot Flash, single 5V supply, -40..+85°C with qualified components
15EM01N00	MPC5200B/384MHz, FPGA 18,752 logic elements, 256 MB SDRAM, 1 GB NAND Flash, 2 MB SRAM, 16 MB graphics memory, 2 MB boot Flash, front: 2 Fast Ethernet (RJ45), 1 UART (RJ45), 1 USB, -40..+85°C with qualified components (also for ESM™ evaluation kit EK6N)

Miscellaneous

05F006-00	RS232 interface cable RJ45 to 9-pin D-Sub (1 COM to 1 COM), 2m

Software: OS independent

13Z015-06	MDIS4™/2004 driver (MEN) for 16Z029_CAN (MSCAN/Layer2)
13Z016-06	MDIS4™/2004 driver (MEN) for 16Z029_CAN (CANopen master)
13Z017-06	MDIS4™/2004 low-level driver sources (MEN) for 16Z034_GPIO and 16Z037_GPIO

Software: Linux

13Z025-90	Linux native driver (MEN) for 16Z025_UART, 16Z057_UART and 16Z125_UART
13Z044-90	Linux native driver (MEN) for 16Z044_DISP (frame buffer)

Software: Windows

13Z044-70	Windows® native driver (MEN) for 16Z044_DISP (frame buffer)

Software: VxWorks

10EM01-60	VxWorks® BSP (MEN) for EM1, EM1A, EM1N, EK6, EK6N, F12N and F12
13Z025-60	VxWorks® native driver (MEN) for 16Z025_UART, 16Z057_UART and 16Z125_UART

Software: QNX

10EM01-40	QNX® BSP (MEN) for EM1, EM1A, EM1N, EK6, EK6N, F12N and F12
13Z025-40	QNX® native driver (MEN) for 16Z025_UART and 16Z125_UART
13Z044-40	QNX® native driver (MEN) for 16Z044_DISP (frame buffer)

Software: Firmware/BIOS

14EM01-00	MENMON™ (Firmware) for EM1, EM1A, EM1N, F12 and F12N (object code)

Documentation

20EM00-00	ESM™ Specification
20EM01-00	EM1 User Manual
20EM01-ER	EM1 Errata
21APPN009	Application Note: 16Z025_UART and 16Z125_UART under Linux
21MENM-00	MENMON™ 2nd Edition User Manual
22Z025-ER	16Z025_UART Errata

For the most up-to-date ordering information and direct links to other data sheets and downloads, see the EM1 online data sheet under » www.men.de.

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