FuturePlus Systems Corporation

FS4435 DP State Analysis Preprocessor

User Manual

For use with Tektronix Logic Analyzers

Revision – 1.2

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Introduction

How to Use This Manual

This manual is organized to help you quickly find the information you need.

- **Analyzing the DP Bus** chapter introduces you to the FS4435 and lists the minimum equipment required and accessories supplied for DP bus analysis.
- The **State Analysis** chapter explains how to configure the FS4435 to perform state analysis on your bus.
- The **General Information** chapter provides information on the operating characteristics, and cable header pinout for the FS4435 probe.

Definitions

The following terms are used to describe aspects of the DP bus:

- Channel - One differential signal (2 wires).
- Link - One direction of a DP link. The FS4435 handles 1 DP and 1 Aux link.

Analyzing the DP Bus

This chapter introduces you to the FuturePlus Systems FS4435 preprocessor and lists the minimum equipment required for analysis.

The FS4435 is a DP State Analysis preprocessor. The preprocessor can connect to the target by either a half-size midbus probe, or flying leads. The “sideband” signals, such as AUX and HPD connect to the probe using separate cables. The preprocessor itself is controlled by the Probe Manager software, which runs under Windows and communicates with the preprocessor via a USB cable.

The FS4435 “snoops” a link without significantly degrading its signal integrity. The high speed serial signal is deserialized and processed for packet identification by the FS4435 before being sent to the logic analyzer connections. Additionally, the preprocessor provides trigger and filtering functions. The dis-assembler software running on the logic analyzer provides information regarding the transactions within the captured traffic.

Accessories Supplied

The FS4435 product consists of the following accessories:

- The FS4435 preprocessor, power supply and cable, Protocol Disassemblers (FS1163 and Aux Port for DP), FS44xx Probe Manager application and USB drivers on a CD. A USB cable is provided for connecting the FS4435 preprocessor to the Windows based machine that the Probe Manager is loaded on.
- This User Manual and Quick Start sheet.

Minimum Equipment Required

The minimum equipment required for analysis of a DP consists of the following equipment:

- Tektronix TLA analysis frame with the TLA7AA4 modules. One is required for each DP and AUX link.
- 4 FS1055 cables for connection of the Preprocessor to the TLA
- A DP target bus. It is **STRONGLY recommended** that the user review and apply the probing guidelines described in the application note “DisplayPort Probing” when planning for use of the preprocessor on any target system.

Probing System Overview

The architecture of the FS4435 preprocessor and the design of the DP link to be probed should both be thoroughly understood before attempting to use the probe.

The following is a general outline of the steps to be taken when probing a new link. Read the following pages for more specific information.

The FS4435 preprocessor requires the understanding and correct set-up of 4 different systems before a trace should be taken.

1. Probe Manager software. This software is identified as FS44xx Probe Mgrr.exe and is on the CD that comes with the FS4435. Additionally, there is a folder within this CD that contains all the necessary USB drivers that your Windows system requires. When Windows searches for the USB drivers to load during the first connection of the FS4435, Windows **MUST be directed to load the drivers from this CD** in the system or the proper USB drivers will not load. In some cases it may necessary to temporarily disconnect the Windows system from the local network to insure that Windows does not automatically default to getting the drivers from the Internet. If the correct USB drivers are not loaded the user will see a Windows error ("Unable to load DLL") as soon as the "Run" button is used.

NOTE: The Microsoft .NET Framework must be on the system for the Probe Manager application to load properly.

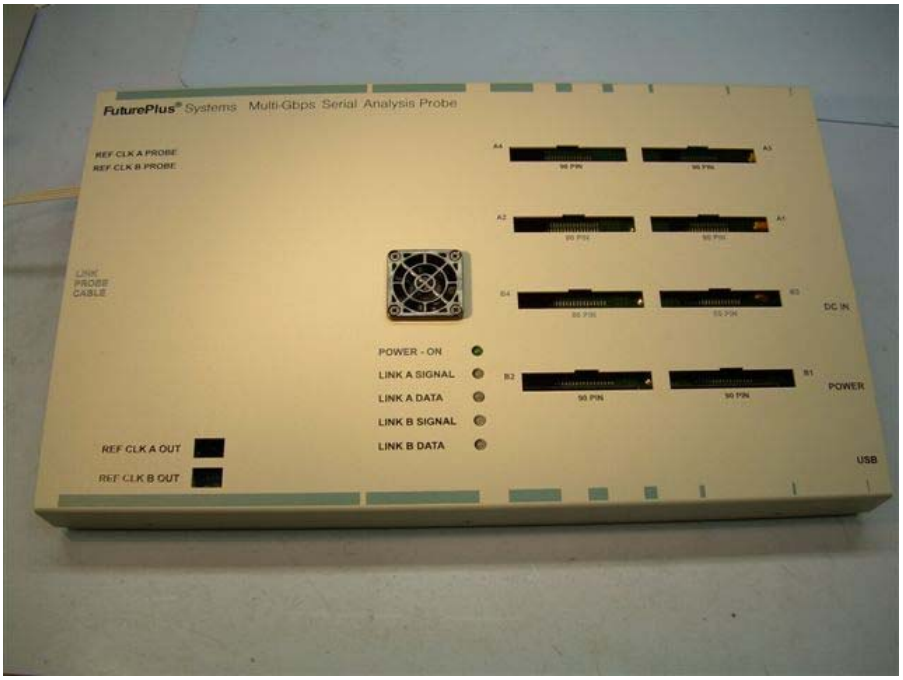
2. FS4435 probe. This preprocessor requires its own DC power supply which is provided. Additionally, this preprocessor is completely initialized, set-up and controlled by the Probe Manager software that resides on a Windows based system (either stand alone PC or TLA logic analyzer). All communication to the FS4435 preprocessor is by means of the USB port on the PC (or logic analyzer). Improper or incomplete installation of either the correct USB driver or the Probe Manager software will prevent operation of the FS4435.
3. Tektronix Logic Analyzer. The TLA Disassembler files for the TLA7xxx analyzer (FS1163) are on a CD. Install these files as required and follow the instructions for logic analyzer module (card) interconnections and logic analyzer connections to the FS4435 probe.
4. Target platform. There are two probing options, mid-bus probe or flying lead. There are also a variety of link implementations besides widths. There are protocol attributes such as lane inversion, data scrambling, and lane reversal, which need to be defined in the Probe Manager in order for the preprocessor to capture data properly.

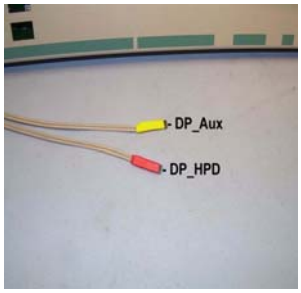
It is strongly recommended that the user methodically proceed in the following manner when setting up the probe. There is more detail on each step in this manual.

1. Load the Probe Manager software and (FS1163) on the PC and/or logic analyzer. Leave the CD in the system for access to the USB drivers.
2. Configure (merge) the logic analyzer modules as required, and run the Tektronix Logic analyzer's internal diagnostics. If the analyzer passes, then make the appropriate target probe connections to the FS4435 preprocessor and from the preprocessor to the TLA (FS1055 cables).
3. Connect the appropriate probing cable(s) to the target system, power up the probe. This may result in a Windows dialog searching for the "*FTDI FTD2XX*" USB drivers; direct it to the Probe Manager CD. Check the Windows Device Manager to make sure that it loaded properly.
4. Open up the Probe Manager application and select the appropriate settings for the probe cable being used and the target link. Check that the expected Pad assignments for the probed link show green after the Run button has been pressed. For the first capture turn off all the filters.
5. If the FS4435 preprocessor LEDs are all Green and the first trace file captured on the logic analyzer has no error messages then it is a good indication that all initial settings are correct.
6. A link showing Signal LED green and Data LED orange constantly, needs settings for link width, lane reverse or lane inversion adjusted in the Probe Config window.
7. A link showing Signal LED orange or red may have a problem with the reference clock settings or connection. More information on link signal status can be seen in the Log File window.

Depending on the DP target system Reference Clock and data lane signal characteristics, such as jitter tolerance, jitter spectrum and/or signal characteristics at the probing location the user may always see some level of orange DATA LED activity and see the corresponding errors recorded on the TLA and in the Probe Error Log. Please remember that the FS4435 cannot operate with spread spectrum clocking on the link.

Front Panel





The connections and features of the FS4435 preprocessor include:

- DC input for provided external AC to DC power supply (please note that the use of any other power supply voids the warranty on the FS4435), On/Off switch and USB connections to the Windows PC/TLA7xxx where the Probe Manager software will be loaded.
- Link Probe cable connection for 1 of the probing cables (mid-bus or FL)
- Logic Analyzer 90 pin pod connections. A1 – A4 are connections for A Link Processor, and B1 – B4 are for B Link Processor.
- Cables for connection to AUX and HPD.
- Loss of Lock LEDs under the cover of the preprocessor. Link A lane 0:3 are on the top and Link B lane 0:3 are below them. Red indicates Loss of Lock, which will prevent preprocessor operation. Dark indicates proper operation
- LED indication of preprocessor power on and Link status. For each link there is a pair of LEDs which have the following states:

Link A or B Signal LED color	Meaning	Link A or B Data LED color	Meaning
Green	Link OK	Green	Data clocking Into Analyzer
Dark	Loss of Signal	Dark	No Data clocking into Analyzer
Orange	Data Invalid (8b10b error)	Orange	Any Error: 8b10b, Align, Framing, Idle
Red	Receiver Fault or Int	Red	Preprocessor Clock Error

FS4435 Probing Cables

The FS4435 can be configured with different probing cables dependent on what the user requires:

FS1032	½ size midbus footprint probe cable for x1 to x4
FS1036	Flying lead probing cable for x1 to x4
FS1040	DisplayPort Interposer

The DisplayPort Probing application note provides specific information on the successful application of midbus probing and also details general requirements for the Reference Clock signal and other aspects of the link to be probed. The FS4435 manual assumes that the user is familiar with this information and has applied it.

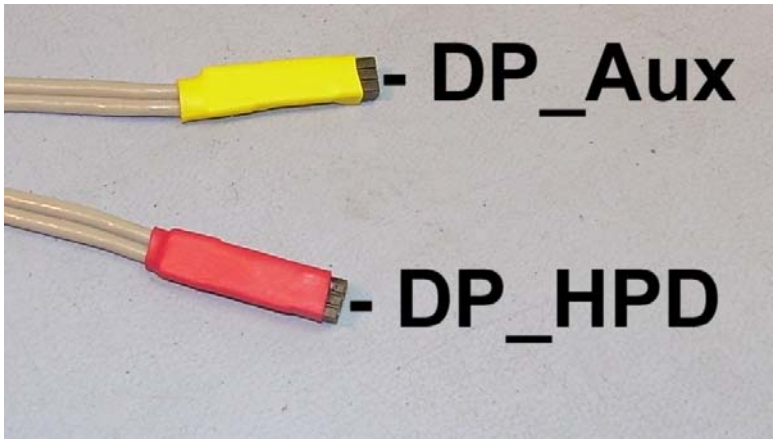
The cable should be attached to the FS4435 and carefully secured with the 2 captive fasteners on the cable. The probing end should be attached to the target by screwing into the retention module (midbus probe) Use of the flying lead probe requires careful installation and mechanical support of special flex circuit tips

The “sideband” signals for DP need to be connected to the FS4435 preprocessor separately from the data link probing cables. There are uniquely identified and labeled cables for doing this. **These must be properly oriented for polarity.**

The DP AUX channel requires a high speed differential connection using a Samtec .050 header where pins 1 and 3 are AUXp and AUXn. The HP_INT signal has its own cable that also connects to a .050 header, pin 1 is the signal and pin 2 is the ground connection.

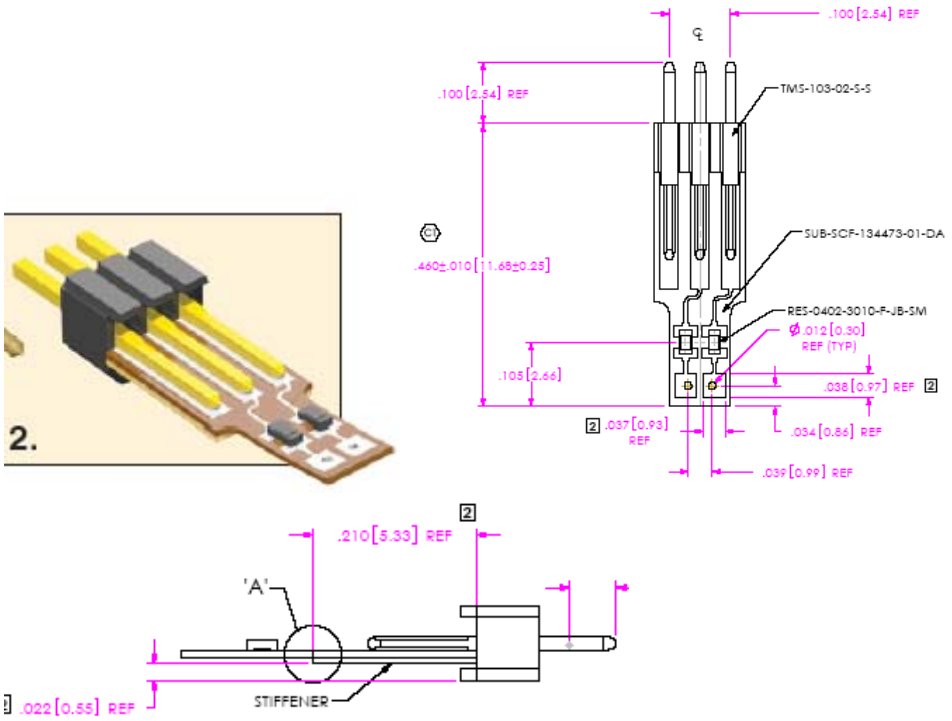
NOTE: These signals cannot see voltages higher than 4 VDC or there is a risk of damaging the preprocessor.

“sideband” cables



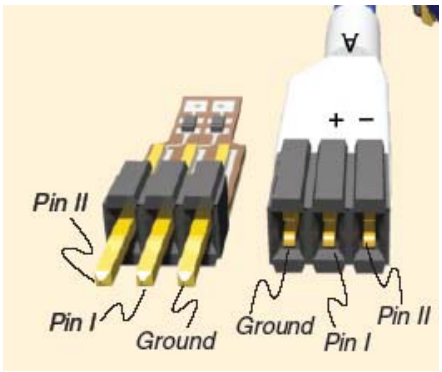
Flying Lead Probing (FS1036 cable assembly)

The FS1036 flying lead cable assembly allows the FS4435 preprocessor to connect to components on the target board by means of directly soldering a flex pcb to a component or feature on the target pcb, then connecting the header on the flying lead cable to the other end of the flex pcb.



A few general guidelines about the use of the flying lead cable

1. There is an instruction booklet with the FS1036 cable that provides detail on how to solder the flex pcb to your board. Refer to this document.
2. Polarity matters. Makes sure you know how the + and – sides of the signal are connected. Adjustment to polarity can be made in the Probe manager.



FS1036 Flying Lead flex tips only.

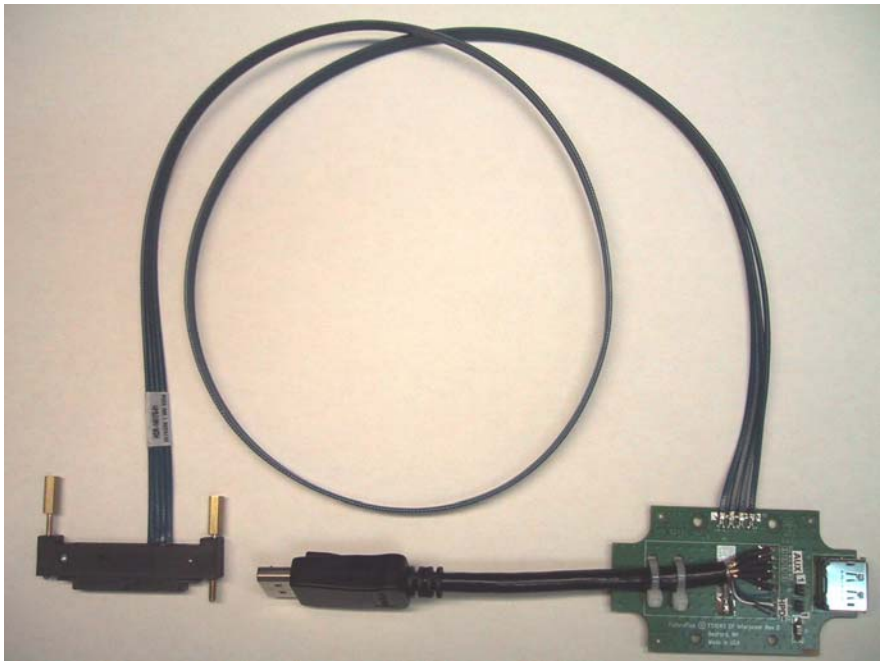
Not the “sideband signals”

The FS1036 flying lead cable has 8 pairs of channel connectors which are labeled A-G for up to 4 channels of a link and B-H which can be used for another link.

Make the appropriate cable and channel selections in the Probe Manager before taking any measurements.

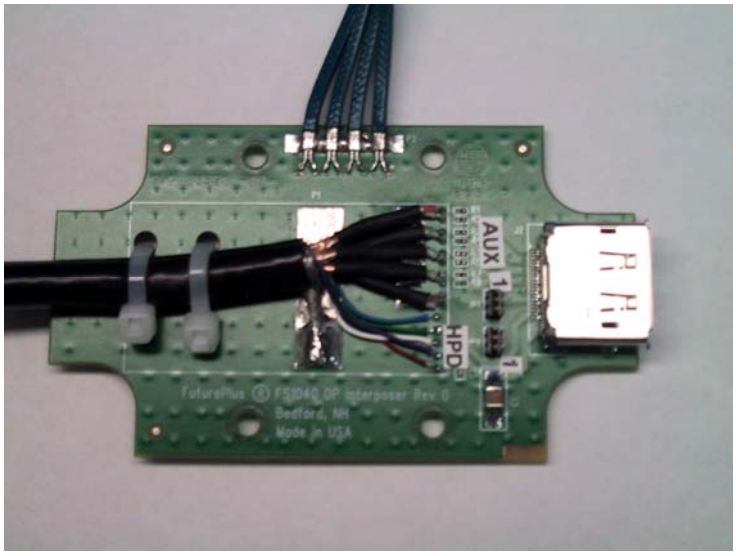
FS1040 DP interposer

The FS1040 DisplayPort interposer is designed to plug between the motherboard and the DisplayPort cable from the monitor. The FS1040 then provides the high-speed serial signals to the preprocessor, as well as, the Aux channel and HPD signal connections. The cable provides a complete “pass-thru” of all 20 signals specified for the DP cable in section 4.2 of the v1.1a specification. There is no reordering of the lane bits. The interposer has been qualified at 2.7GBps.



The FS1040 is connected to the FS443x probe in the same manner as the other probe cable. It can be selected on the Probe Manager Config page.

Aux and HPD signals can be attached to the 3 pin headers on the FS1040. Polarity of the connection is important so match the pin 1 labels on the sideband cables to the labeled pins on the FS1040.



Installing your Software for the First Time

The following outlines the software installation procedure when using the preprocessor for the first time. Please do not attach the preprocessor to the analyzer or computer that will be controlling the preprocessor until told to do so.

1. Place the software CD that came with the product into the logic analyzer or computer that you will be installing the software on. In the case of a machine that does not have a CD drive, the machine will either have to be put on a network and the files loaded remotely or the CD files can be transferred from a USB drive.

2. Navigate to the installation CD using Windows explorer and click on the following files. Follow the instructions on the screen to install.*

   - FS1163/AUX.exe Protocol Dis-assembler

   - FS44xx Probe Mgr.exe

3. Once all the above files have been installed, connect the FS4435 to the analyzer/computer via the USB port. Power on the FS4435 probe.

4. The found new hardware wizard should appear the first time the preprocessor is attached and powered up. Select “No, not this time” when it asks if the computer can go to Windows update to search for the software. Then select Next.

5. On the next screen select the Advanced option (not the Recommended) to select from a specific list or location. Select Next.

6. Select the CD-ROM drive to load the driver from; you do not have to select a specific directory. Select Next.

7. There may be a warning that comes up about Windows XP compatibility, ignore this warning and continue with installation.

8. Click Finish to complete the installation.

Once all the previous steps have completed all necessary software as well as USB drivers will be installed. This procedure only needs to be done on initial install. You may now go to the desktop and click on the Probe manager icon to start the probe manager.

*If you are installing on a PC to only control the FS4435 then you can omit the installation of the FS1163/AUX.exe, but you must follow the rest of the steps.

For instructions on loading system files please refer to the section on loading system files later in this manual.

Connecting the Tektronix logic analyzer to the FS4435

The FuturePlus Systems FS1055 cable is designed to attach to the 90 pin connectors on the FS4435 and to the TLA7AA connector on the other end. Each FS1055 connects 2 FS4435 90 pin pods (17 channels each) to 1 TLA module input (34 channels)

The table below explains how to connect TLA7AA4 card to the FS4435.

Logic Analyzer	FS4435	Comment
DP		
Master #1 A3, A2	A1	Clock
D3, D2	A2	(270 Mhz at 2.7Gbs)
Master #1 A1, A0,	A3	(160 MHz at 1.62Gbs)
D1, D0	A4	
AUX		
Master #2 A3, A2	B1	Clock
D3, D2	B2	
A1, A0	B3	
D1, D0	B4	
10b Link A and B		
Master C3, C2	A1	Clock
C1, C0	A2	
A1, A0	A3	
D1, D0	A4	
Master A3, A2	B1	
D3, D2	B2	
E3, E2	B3	
E1, E0	B4	

Based on the probing needs install the appropriate modules into the Tektronix logic analyzer and remove any adapter cables that may be attached to the module cables. When probing a single direction of a x1, x2 or x4 link, the FS4435 drives 4 pods of signals (2 FS1055 cables) to the logic analyzer.

It is important before you load a system file you initiate a self test on all your modules installed in your logic analyzer to insure all modules are working properly.

Loading System files

From the system window of the TLA application, select a logic analyzer module. After selecting the module in the System window, either right click the mouse and select “Load Support Package or go the File->Load Support Package. After clicking “Load Support Package” a list of installed support packages will appear. Select the support package that matches the desired analysis requirements. The dis-assembler will load along with the system file. If you are analyzing more than 1 link, simply choose another analyzer module from the system window and select “Load Support Package” to load the second module.

The analyzers supported by the FS4435 system files are theTLA7AA4 cards

DP – x1, x2, x4 DP link analysis. Requires 2 FS1055 cables and 68 logic analysis channels.

AUX – AUX analysis. Requires 2 FS1055 cables and 68 logic analysis channels.

Offline Analysis

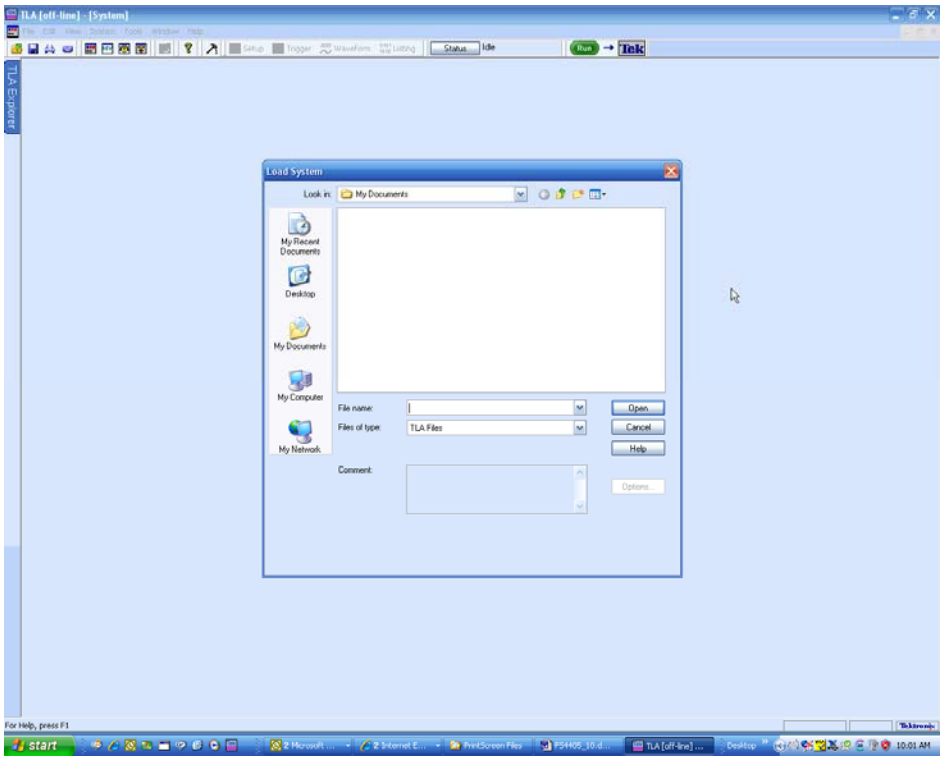
Data that is saved as a *.tla file, can be imported into the TLA7xxx environment for analysis. You can do offline analysis on a PC if you have the TLA7xxx operating system installed on the PC, if you need this software please contact Tektronix.

Offline analysis allows a user to be able to analyze a trace offline at a PC so it frees up the analyzer for another person to use the analyzer to capture data.

In order to view decoded data offline, after installing the TLA7xxx environment on a PC, you must install the FuturePlus software. Please follow the installation instructions for "Setting up TLA7xxx analyzer". Once the FuturePlus software has been installed follow these steps to import the data and view it.

From the desktop, double click on the Tektronix TLA icon. When the application comes up there will be a series of questions, answer the first question asking which startup option to use, select Continue Offline. On the analyzer type question, select Cancel. When the application comes all the way up you should have a blank screen with a menu bar and tool bar at the top.

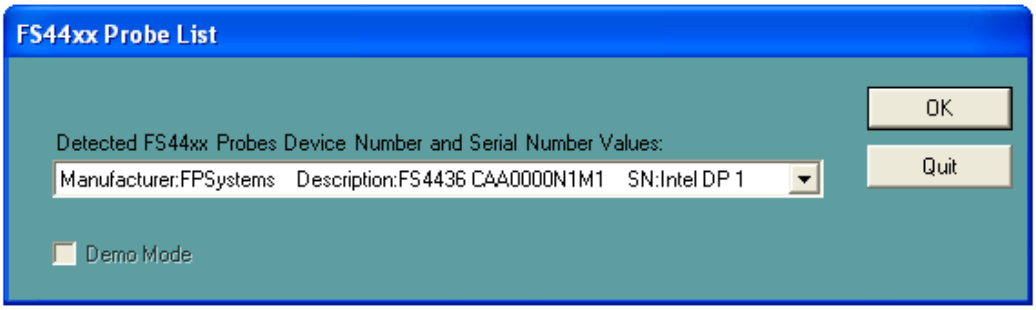
Open the .tla file using the File, Load System menu selection and browse to the desired .tla file.



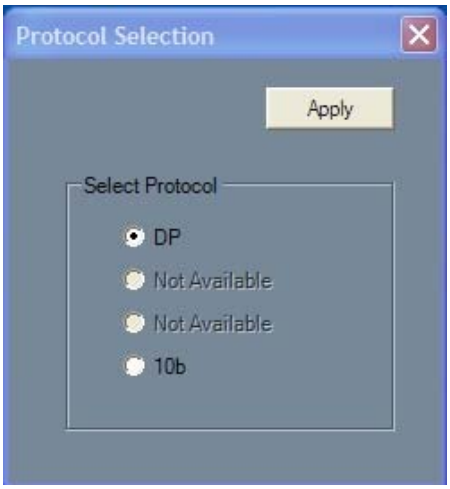
Probe Manager Application

The Probe Manager software can be found as the FS44xx Probe Mgr.exe file on the CD provided in the Documentation package. Insert the CD into the computer that will be used to control the FS4435 probe. This computer must have a USB connection. Using Windows File Manager, select the FS44xx Probe Mgr.exe file and double-click it, which initiates the installation software on the computer and places an icon on the desktop. Follow the directions that follow including agreeing to the license terms, once the software installation is complete click on finish. To start the program manager simply double click its desktop icon.

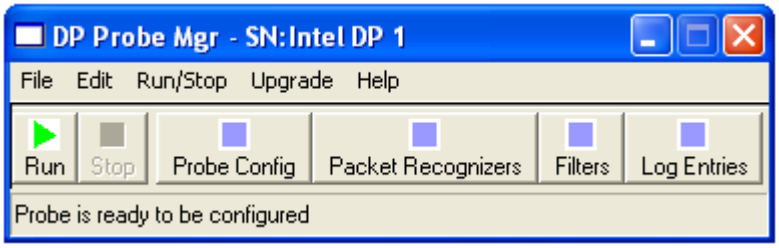
The Probe Manager application detects all FS44xx probes that are connected to the USB bus and allows the user to select which preprocessor will be controlled by the current instance of the Probe Manager application from the initial screen as seen below.



The initial screen is followed by the Protocol Selection screen, in which the user selects a protocol to configure the FS4435 Preprocessor. The FS4435 has choices for DP and raw 10b decode.



Once the protocol has been selected, the application displays the Main dialog as seen below:



The user configures and controls the preprocessor from the main form. The form is composed of a menu bar, a tool bar and a status message bar. The menu bar provides options that allow the user to configure and run the probe. The tool bar provides options to configure the preprocessor and the status bar displays the probes current status and/or any errors that may have been encountered. Error messages displayed in the status bar are also logged in the Log Form if logging is enabled.

The menu bar contains the following options:

File

- Open Config File – Displays an open file dialog in which the user may navigate to and open the file contains a previous session's saved probed settings.
- Save As - Displays a save file dialog in which the user may specify where a preprocessor settings system file may be saved.
- Exit – Shut down the application.

Edit

- Modify Title String – Allows the user to specify the title string that appears in all sub-dialog's title bar. This is helpful when running multiple probes.

Run/Stop

- Run Probe Mgr – Running the preprocessor with the current settings. This is an alternative to clicking the tool bar Run button.
- Stop Probe Mgr - Stop the probe. This is an alternative to clicking the tool bar Stop button

Upgrade

- FPGA – Upgrade one of 2 protocol specific FPAG configurations.

Help

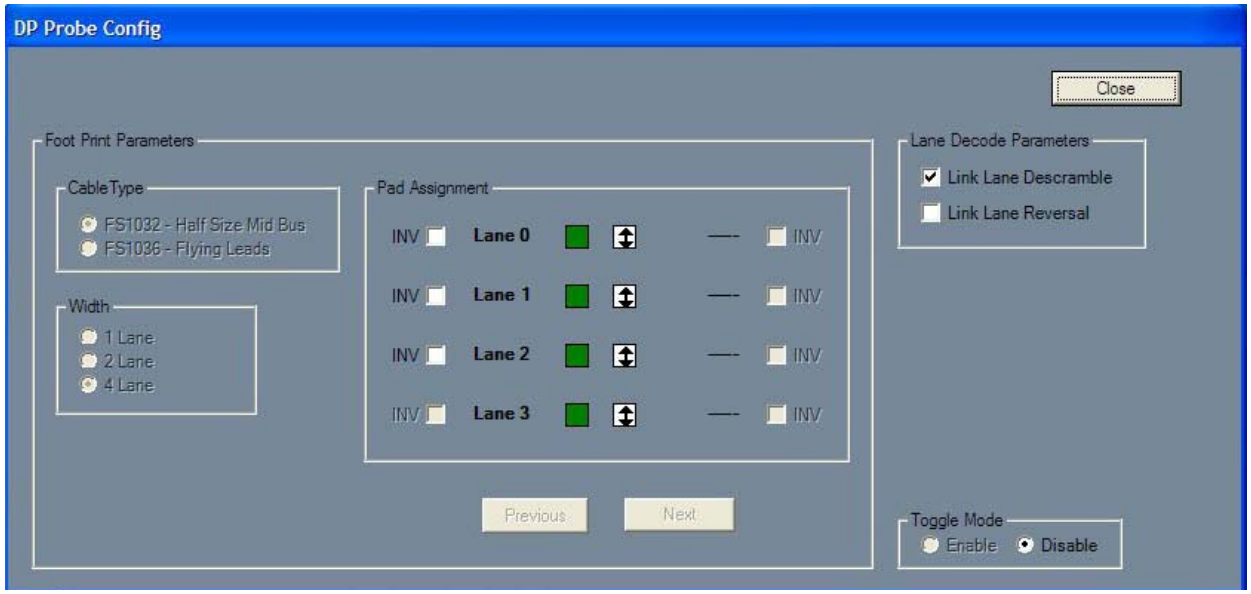
- About – Display version numbers for the Probe Manager application and FPGA configuration.

Preprocessor Configuration

The application displays up to five sub-dialogs. These are used to configure the FS4435 probe.

The four sub-forms are:

- Probe Configuration – Covers the type of cable used and basic aspects of the link being probed.
- Filters – Allows the user to specify the types of packets to be filtered
- Pixel Recognizers – Allows the user to trigger on a particular pixel value.
- Log Entries – Run time preprocessor status.



DP Probe Config X1 X2 X4 Dialog

Note: there is no Config required for Aux or HPD signals

The functions provided on these forms include:

- Selection of the Probing Cable type, Link width, and pad arrangement (referring to the arrangement of lanes on the mid-bus probe pads; see the “PCI Express Probing Design Guide for the FS440X” for more specific information).
- The Pad Assignment graphic shows the assignment of logical lanes as a result of user selections, and also represents the physical layout of mid-bus pads. The FS4435 processes channels from the left column in link-processor A and from the right column in link-processor B.
- Next or Previous buttons scroll through the various types of currently supported pad assignments.
- Lane Inversion can be selected on an individual channel basis by clicking the INV button associated with each lane.
- While the preprocessor is stopped, signal activity indicators are provided on each channel. Signal presence is indicated by an up-down arrow symbol and a lack of signal presence is indicated by a flat horizontal line symbol.
- Selection of Lane Reversal on each link.
- Selection of Data Descrambling on each link.
- Hot Plug Cable – If the HPD cable from the probe is not connected to the target, uncheck this box .
- Selection of Toggle mode. When activated, the preprocessor output signals to the logic analyzer pods and the link status LEDs are toggled.

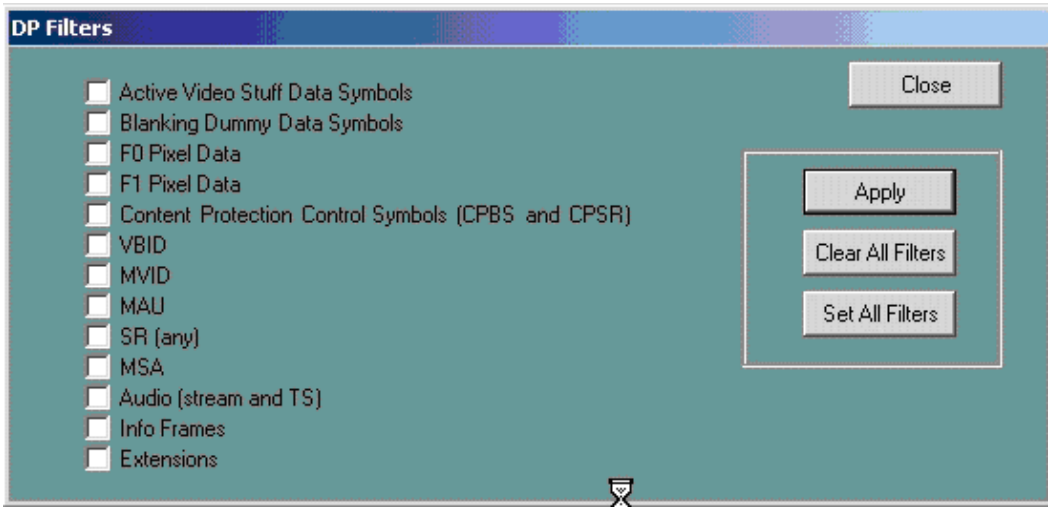
Dynamic Lane width tracking

The FS4435 can maintain lock and processing on a DP link as it changes lane width under certain conditions.

FuturePlus Systems recommends that you stop the preprocessor, reconfigure the lane width, and then restart the preprocessor. This will set-up the serdes properly for that new lane width and all the LEDs and Error Log should operate properly at that new lane width.

Filtering

The Filter dialogue page provides the user with a comprehensive suite of predefined filter functions to apply to either Link. These filters are state based, which means that the event has to occur on all active lanes for it to be filtered. Control Symbols cannot be filtered as they are needed for Protocol Decode.



DP Filters Dialog

Filter types include all types of states. Many of the filters will operate on several types of states, e.g. “Content Protection Control Symbols” will filter all control symbols associated with any Content Protection sequence of states.

Filters can be enabled to filter out entire secondary data packets. There are currently no capabilities to filter portions of any secondary data packets.

Filtering is done in real time by the FS4435 hardware. It must be stopped to change Filter settings

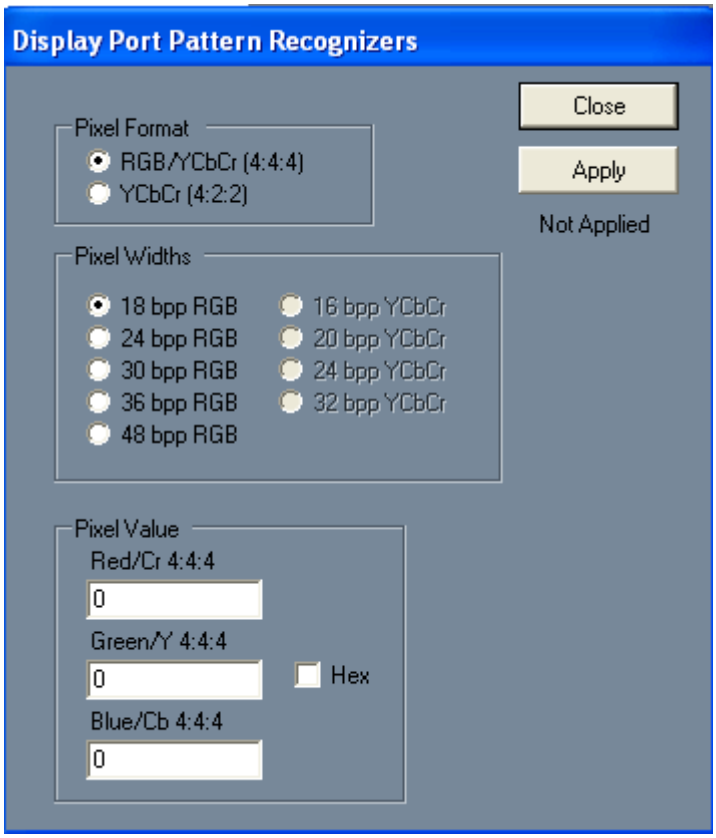
Filtering out unwanted traffic such as dummy data symbols can extend the storage capabilities of the logic analyzer. Filtering out irrelevant bus traffic can help users focus on specific packets of interest.

To filter out any particular traffic type, click on the appropriate box so a √ appears and click apply. You must restart the preprocessor by pressing the green run button so the new values will be written to the preprocessor hardware.

DP has only one link and thus there are no controls to specify filters for link A or B.

The status of the probe, and the link under test, can be seen in this tab page.

Pixel Recognition



The Pixel Recognition function allows the user to trigger on any pixel value. It's set-up involves the following controls:

Pixel Format – Either RGB/YCbCr 4:4:4 format or YCbCr 4:2:2 format

Pixel Width – Select the correct total bits per pixel format from the choices listed.

The target system's pixel format can be found in the MSA packet of the DP listing.

Pixel Value – Enter the decimal (or Hex) value of each color component of the pixel to be triggered on. Leaving a field blank will define a "don't care" for that value.

Click on the "Apply" button after the values are set to set the Pixel Recognizer to flag the defined value. The Group name Pixel_Recognizer can then be used in the Trigger statement. This signal will pulse high on the state that contains this pixel value.

Advanced Pixel Triggering

The Pixel Recognizer function of the FS4435 can be combined with the triggering functionality of the logic analyzer to find a specific pixel value at a specific pixel location.

The user is required to know the following information in order to set up these triggers;

- Number of lanes
- Format of the pixel (RGB, YCbCr, bits per pixel)
- Horizontal line # that will contain the pixel
- Pixel color value

This function uses multiple levels of triggering:
Note: For this trigger to work, filters must be set so Stuffed Data symbols during the active video segment are filtered out

Conditional Storage using Group Storage=1
Level 1 - locate the start of the active video frame (Vertical Blanking BE)
Level 2 and 3 - locate the start of the defined horizontal line (Horizontal Blanking BE) using counter 1
Level 4 – Find the logic analyzer state within the desired video line that the desired pixel is located on. If no trigger then go to Level 1

Trigger Level 1 – The start of a video frame can be defined as the Vertical Blanking End and can be set in the trigger using the Event code “Vertical Blanking BE”. However some systems can generate multiple Vertical BEs before any Horizontal video, so a trigger function may need to include F0 or F1 pixel information to determine the start of the desired video frame.

Trigger Level 2 and 3 – The horizontal line number for the desired pixel has to be defined by the user. This line can be counted up to by using the Event Code “Horizontal Blanking BE”. Note that for a pixel at line 10 the counter would be set to 9 (counter 1= line number -1)

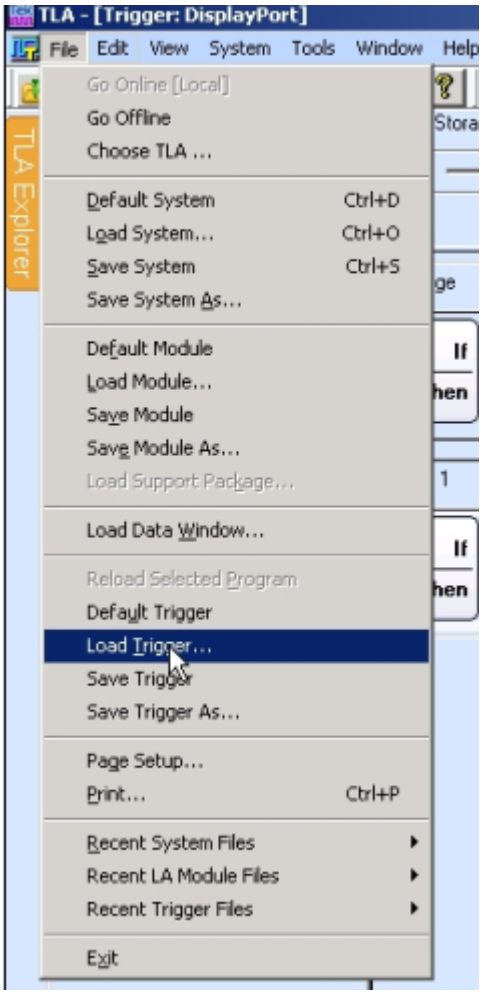
Trigger Level 4 – Once the desired line is found we use the index number of the pixel (pixel index numbers start at 0) to find what state to test the pixel recognizer against. The value of Counter 2 is as follows:

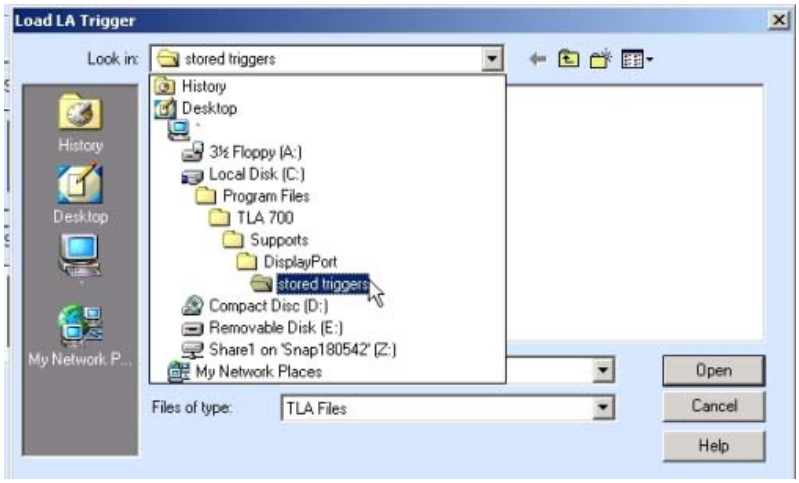
Counter 2 = ((Pixel Index number/Link Width)* (Bits per pixel/8))-1

If the desired pixel color at the specified location is not part of this frame the trigger will go back to State 1 and look for this location/color combination in the next frame.

The logic analyzer triggering combined with the pixel recognizer will get the trigger to the exact pixel if it is a x1 configuration. Based on the number of lanes and the format of the pixel it will at worst get it to the correct state where the user will visually have to determine which out of 4 pixels matches the recognizer.

There are several saved Triggers for this advanced Pixel triggering. These can be loaded from the File menu

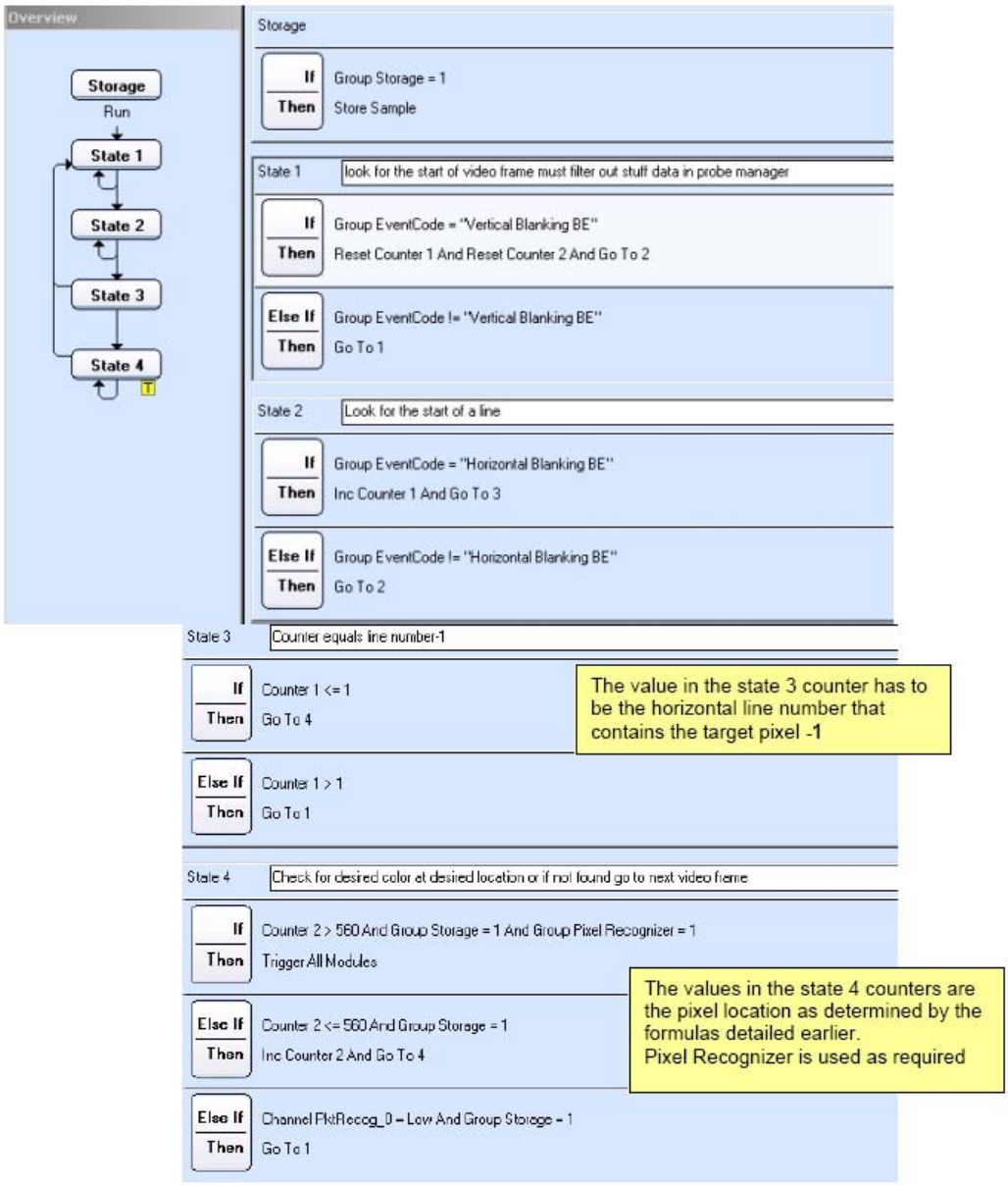




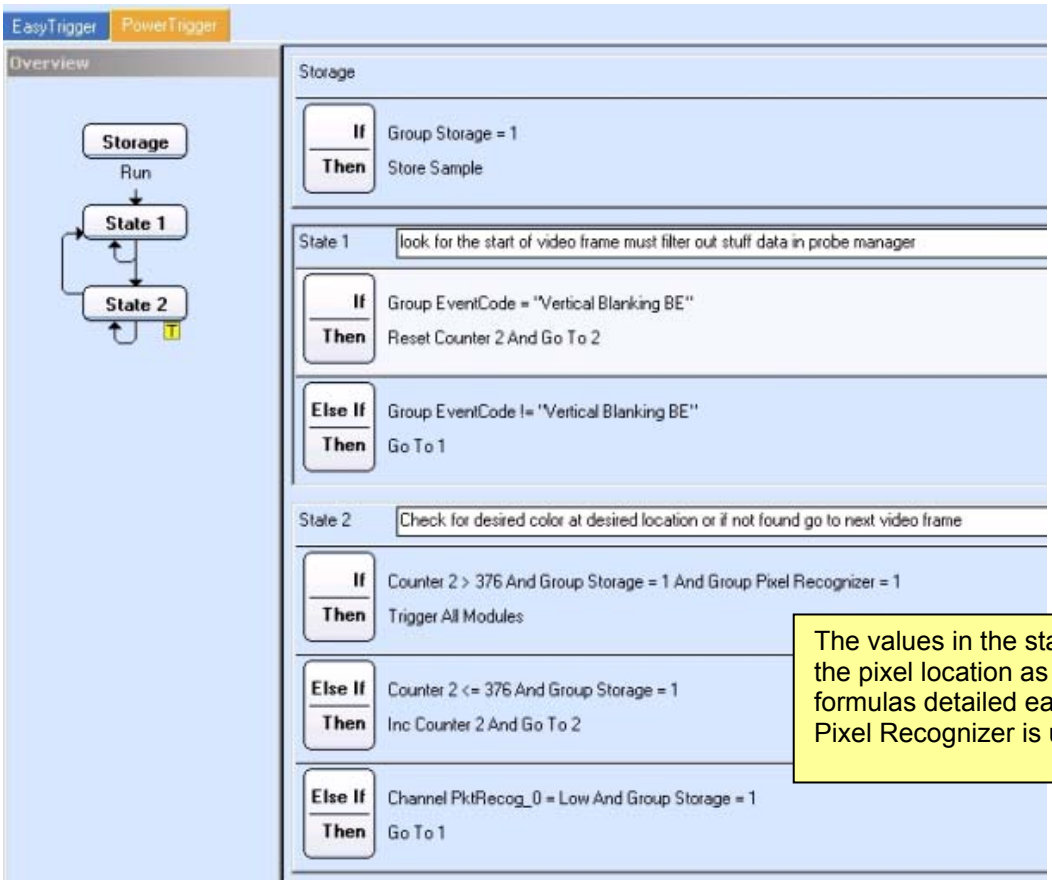
The first Trigger is designed to allow the user to trigger on a particular pixel value in a horizontal line that is not the first line of the Frame.

Note that these Triggers require that *Active Video Stuff Data Symbols* are being filtered.

The Trigger is shown below with some detail on those settings which will need adjustment based on the user's needs.


Overview
Storage
Run
State 1
State 2
State 3
State 4
T
Storage
If
Then
Group Storage = 1
Store Sample
State 1
look for the start of video frame must filter out stuff data in probe manager
If
Then
Group EventCode = "Vertical Blanking BE"
Reset Counter 1 And Reset Counter 2 And Go To 2
Else If
Then
Group EventCode != "Vertical Blanking BE"
Go To 1
State 2
Look for the start of a line
If
Then
Group EventCode = "Horizontal Blanking BE"
Inc Counter 1 And Go To 3
Else If
Then
Group EventCode != "Horizontal Blanking BE"
Go To 2
State 3
Counter equals line number-1
If
Then
Counter 1 <= 1
Go To 4
Else If
Then
Counter 1 > 1
Go To 1
The value in the state 3 counter has to be the horizontal line number that contains the target pixel -1
State 4
Check for desired color at desired location or if not found go to next video frame
If
Then
Counter 2 > 560 And Group Storage = 1 And Group Pixel Recognizer = 1
Trigger All Modules
Else If
Then
Counter 2 <= 560 And Group Storage = 1
Inc Counter 2 And Go To 4
Else If
Then
Channel PktRecog_0 = Low And Group Storage = 1
Go To 1
The values in the state 4 counters are the pixel location as determined by the formulas detailed earlier.
Pixel Recognizer is used as required

This is the simple pixel Trigger for use when the desired pixel value is on Line 1 ONLY



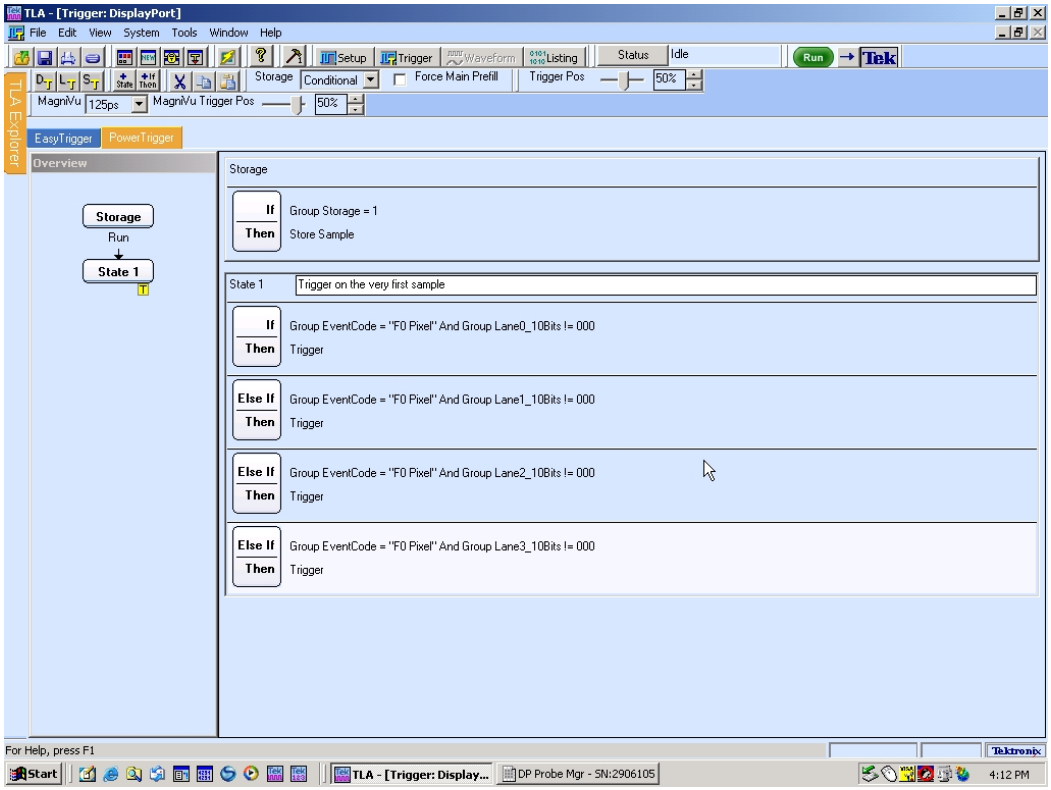
The values in the state 2 counters are the pixel location as determined by the formulas detailed earlier.
Pixel Recognizer is used as required

How to Trigger on a Bad Pixel

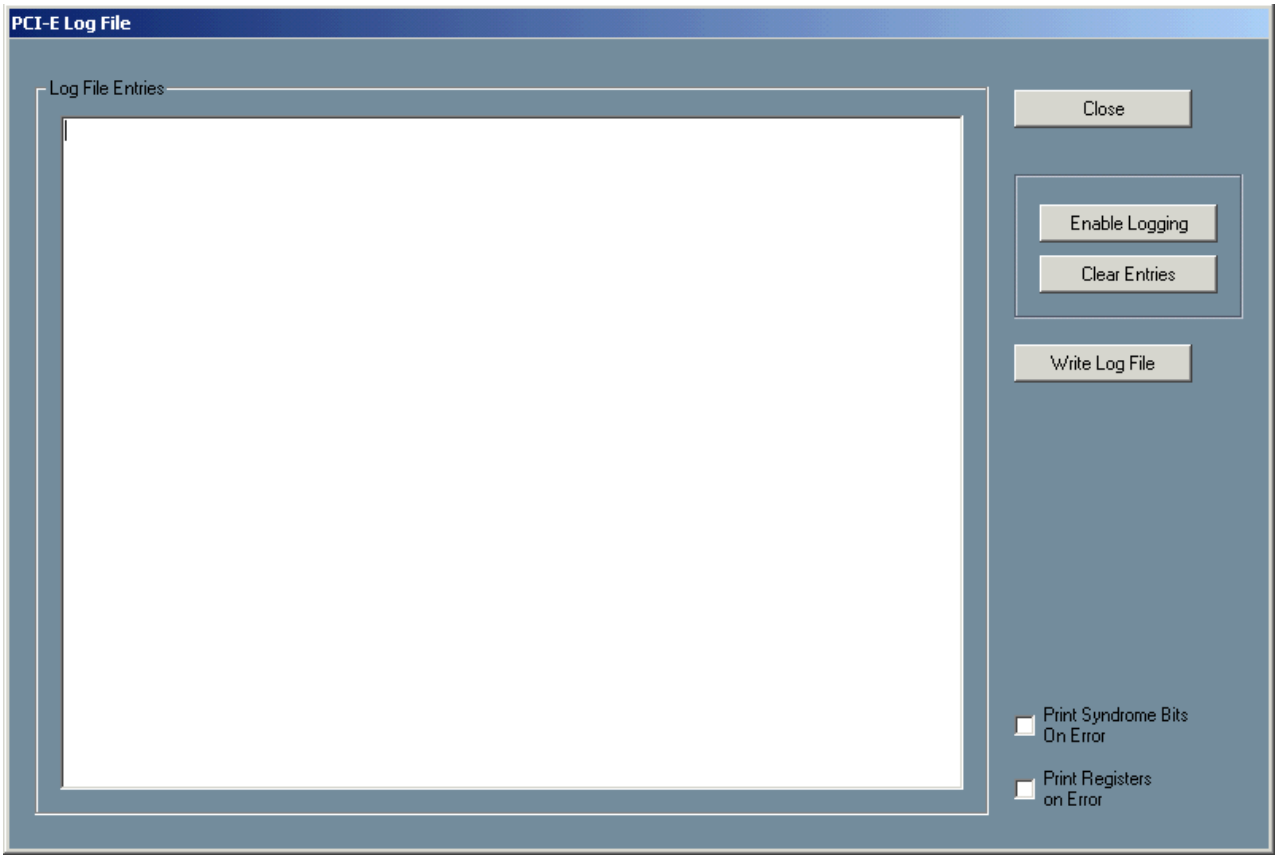
A simple way to find a bad pixel in a screen is to have the source drive the screen to all one color, for example black (RGB 0,0,0). Program the Logic Analyzer to look for **not black** on any of the active lanes.

Note: When using the Pixel Recognizer as part of the triggers it is recommended that ***Active Video Stuffing Data Symbols*** be filtered out using the Filtering menu.

Below is an example trigger that shows how this can be accomplished.



Log File



Log File

Once started, logging continues even if the preprocessor is stopped and started, or if the log window is closed and re-opened. The log file will not repeat an error that repeats itself constantly.

Once a preprocessor has been stopped, the log entries can be written to a file of the user's choice by clicking the Write Log File button.

State Analysis

This chapter explains how to use the FS4435 to perform state analysis.

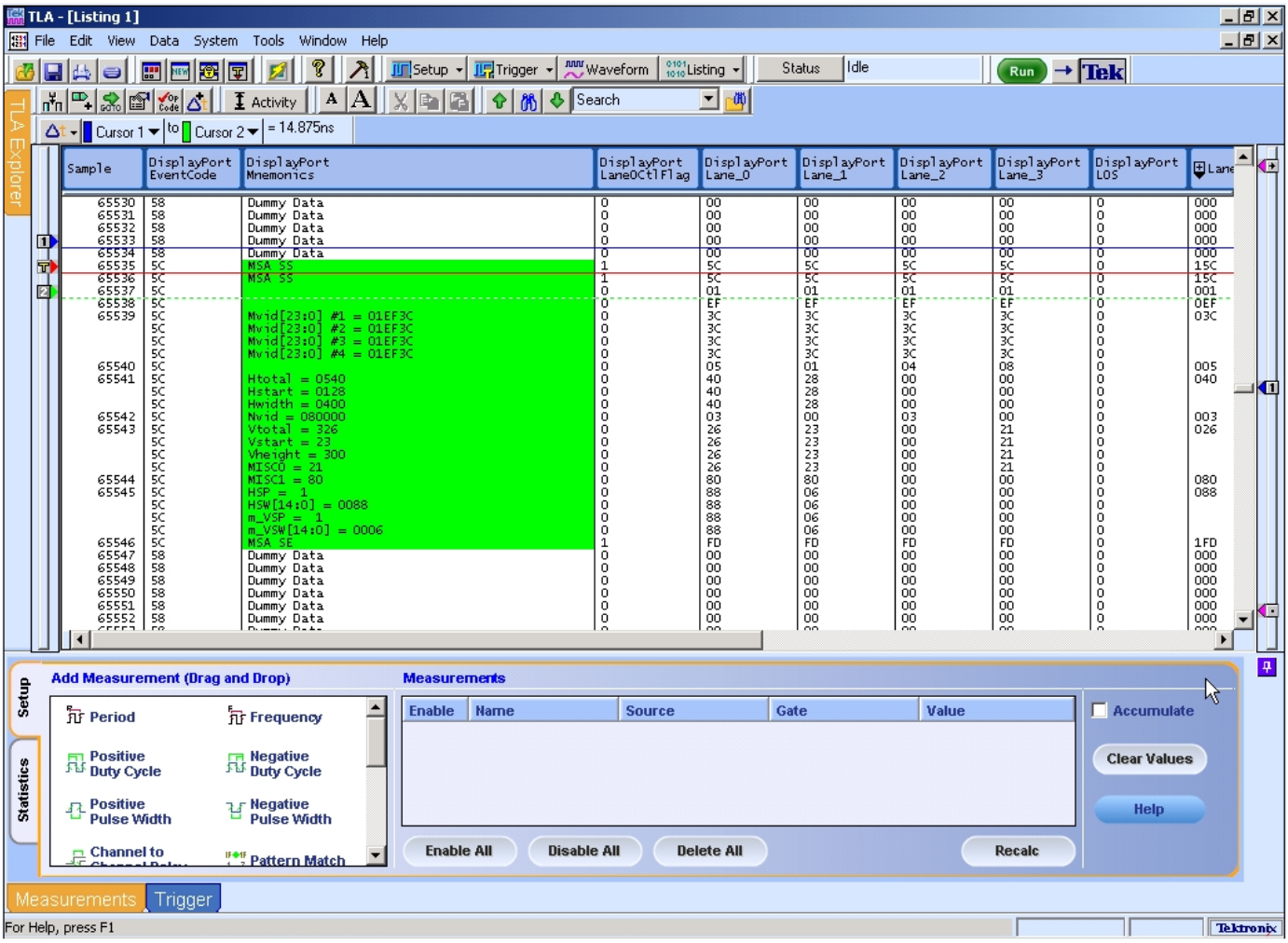
From the system window of the TLA application, select a logic analyzer module. After selecting the module in the System window, either right click the mouse and select “Load Support Package or go the File->Load Support Package. After clicking “Load Support Package” a list of installed support packages will appear. Select the support package that matches the desired analysis requirements. The dis-assembler will load along with the system file. If you are analyzing more than 1 link, simply choose another analyzer module from the system window and select “Load Support Package” to load the second module.

A list of Support Packages are as follows:

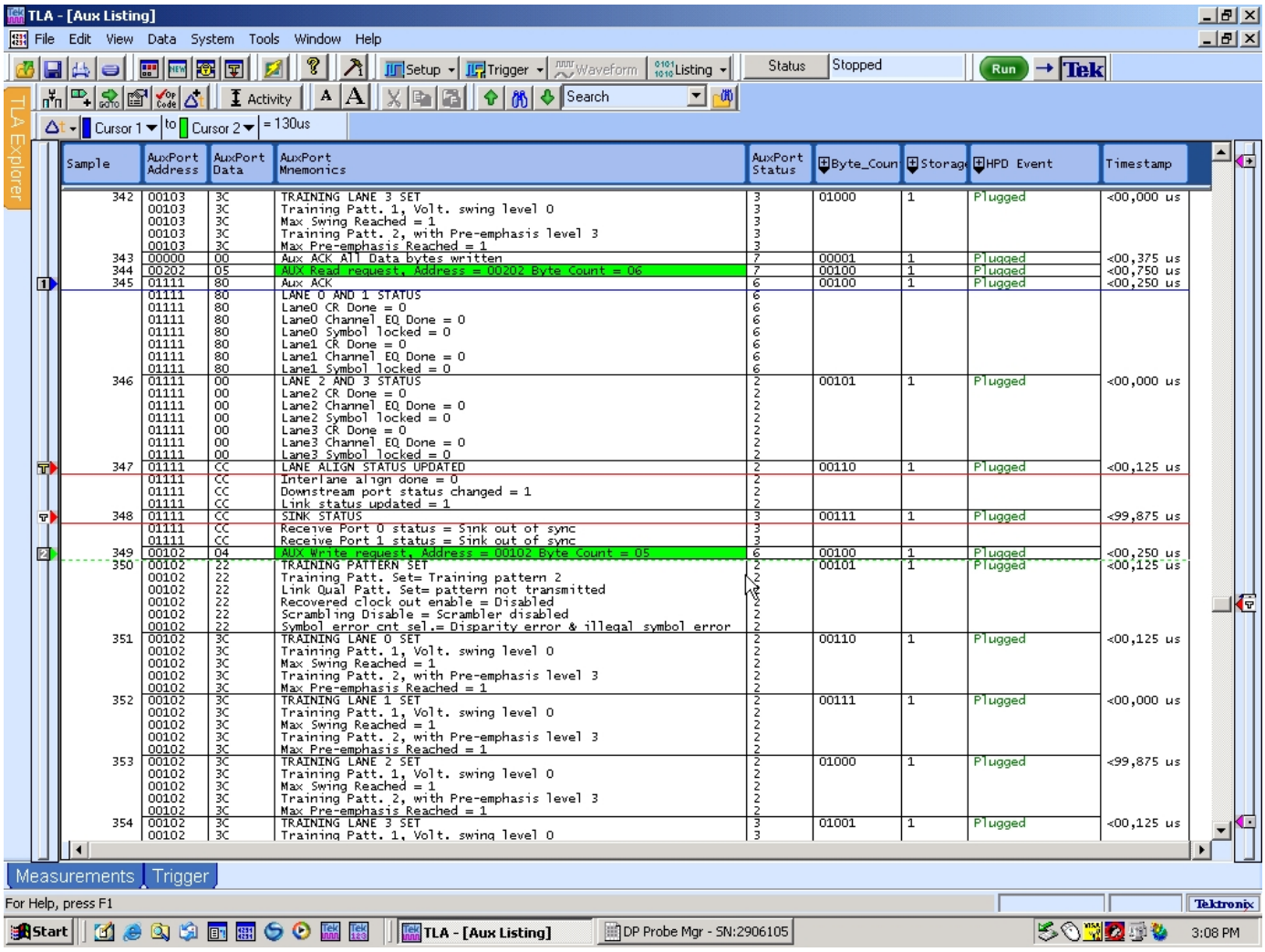
FS1163: DisplayPort

AuxPort: DisplayPort Auxiliary Port

The following is an example listing screen showing the protocol decode provided by the Disassembler for DisplayPort



The following is an example listing screen showing the protocol decode provided by the Disassembler for AuxPort.



Symbol files

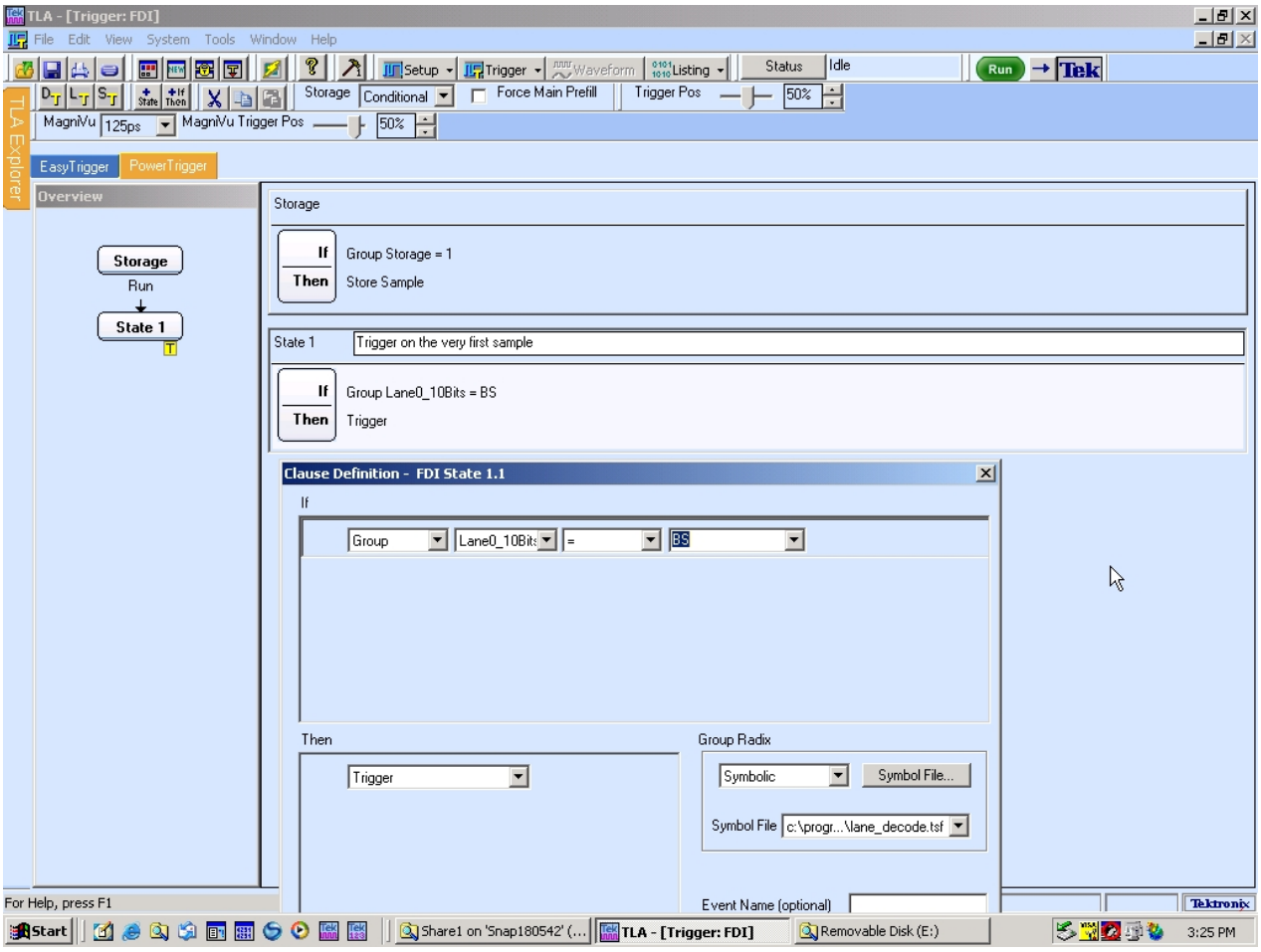
The Support package includes symbol files for the following:

- DP lane data
- Event Codes
- AUX channel Commands
- 10b decode

These are separate files that can be loaded to provide more information in the lister or for use in defining triggers.

Triggering

The system files allows logic analyzer based trigger set-ups that utilize the pre defined symbols described earlier.



- Remember to always use conditional storage. This is because the preprocessor clock is free running and the Storage bit is used to qualify what is sent to the logic analyzer modules. There is a separate storage bit for HPD, HPD_Valid.
- The Event Code field makes it easy to trigger on particular packet types.

To capture specific traffic use the channel signals that can assist in identifying the activity that you want to capture. For example, to capture training use the channel TRAIN, which goes high during training activity. Turning off descrambling when looking at training will properly display the K characters.

Acquiring Data

First, insure that the FS4435 is attached to its external power supply and powered on, which would be indicated by a green Power On LED. Open up the Probe Manager software and insure the appropriate selections are made and applied, finally make sure that the preprocessor is connected via the appropriate cable(s) to the target system.

Once connected, with the link active, open up the Probe Config window and select cable type, lane width, and other options. Verify that lane activity indicators show activity at the correct lanes. Run the preprocessor and observe the LEDs.

If a link's Signal LED is green but its Data LED is orange then there may be a need to select different options for lane width, lane reverse or lane inversion in the Probe Config window.

The FS4435 should show a green Signal LED of any Link being probed, as well as a green or dark data LED.

Configure the analyzer trigger menu to acquire data. Select RUN and, as soon as the trigger condition is met, the logic analyzer will begin to acquire data. The analyzer will continue to acquire data and will display the data when the analyzer memory is full; the trigger specification is TRUE or when you select STOP.

Main Link status is communicated by a pair of LEDs as follows:

Signal LED State	**Meaning**
Dark	LOS (no signal on an active lane)
Red	RX Fault: Lost Signal, Lost Synch on Data, FIFO over run or under run. See Log for more information.
Orange	Invalid Symbol or Disparity Error
Green	OK

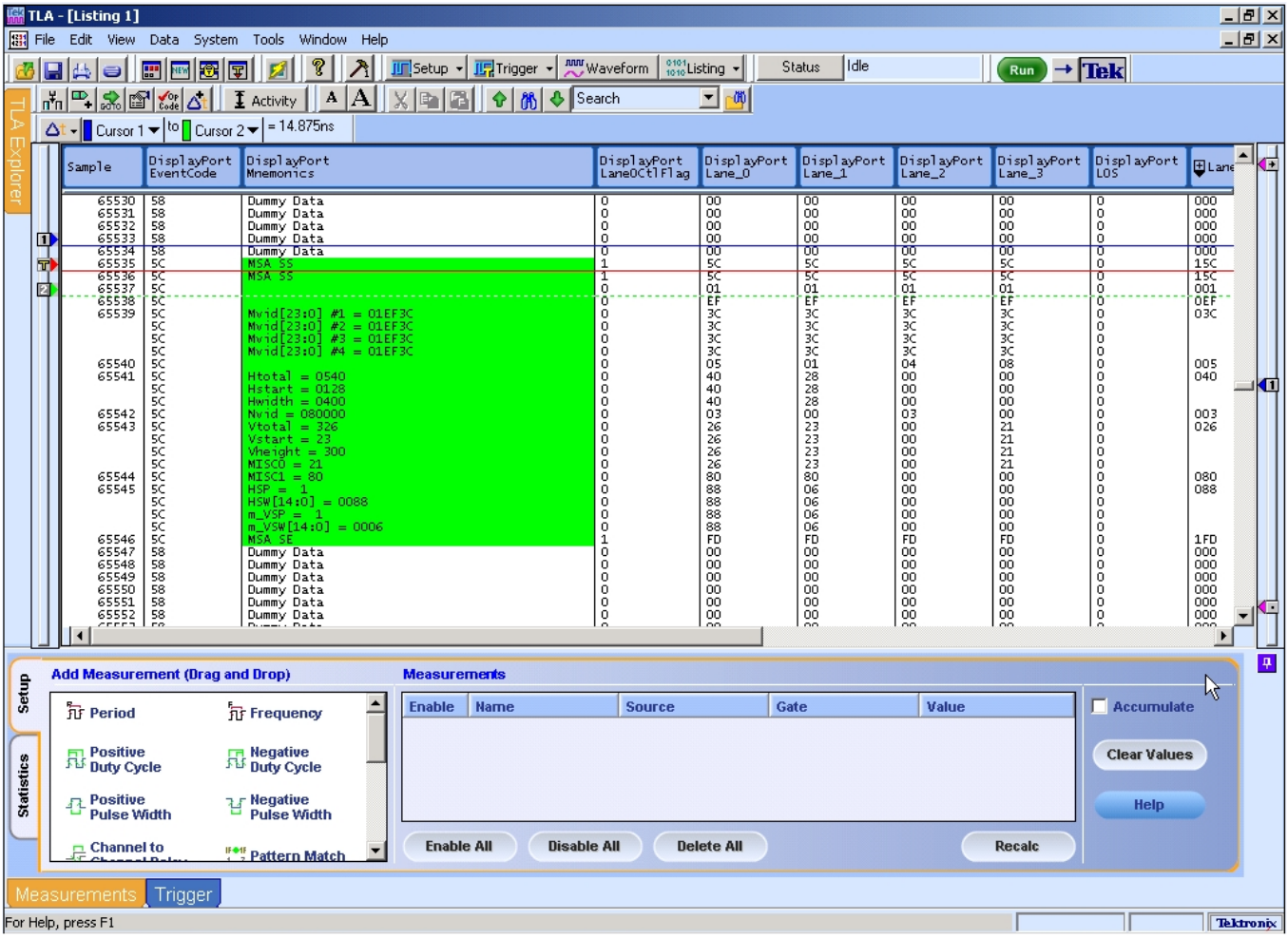
Data LED State	**Meaning**
Red	FPGA Lost lock on clock(s). Preprocessor needs to stop and run again.
Orange	Any Error: Invalid Symbol or Disparity Error, Align, Framing, Idle.
Green	OK, Data clocking into analyzer.
Dark	No Data (due to filtering or not running)

All transient events, such as a single bit error or a packet clocked into the analyzer, are stretched to short visible pulses on the LEDs.

There are no LED's to show the status of the AUXPORT.

The Protocol Disassembler

Captured DP data is as shown in the following figure. The figure below displays the Main Link protocol decode.



The FS4435 Disassemblers will perform the following functions:

- Decode all DP or AUX, protocol data
- Color code the transaction type. The colors used by the software are as follows:
  - Main Stream Attributes: Green
  - Secondary Data Packets: Blue
  - All other states: White
  - AuxPort: Source initiated: Green

In order for the FS4435 Main Link DP Disassembler to decode the pixel data they must be set to the proper Pixel Width which is found in the Properties tab of it's column heading.

DP Groups

Besides de-serializing the data stream for the logic analyzer, the FS4435 generates a number of identification and control bits that are used by the Protocol Disassembler and logic analyzer. These are also available to the user and are described below. These are the same for any DP link. AUX port is defined separately.

Field	Bits	Definition	Pod	Bits
Storage Flag	1	1= Store this state 0 = Discard	A4 (B4)	16
Data Error	1	1= This state includes an error		15
TRAIN	1	A Training or IDLE sequence has been detected		14
Packet Recognizer	3	1= Packet recognized (pulsed for one clock cycle during packet)		13:11
Event Code	8	Describes what type of packet, signal event or error event. Code is held for duration of packet (Transfer unit?) except that signal and error events can over-write any state except the start state. When start and end coincide, the event code for the starting packet is displayed.		10:3
Sideband signals	3	Spares when in DisplayPort mode.		2:0
Spare	2	Spare	A3 (B3)	16:15
Data Present [3,2,1,0]	4	1= Corresponding lane data byte is present. 0= Data not valid. This might be used to indicate that this lane has been dropped.		14:11
LOS [3,2,1,0]	4	1= Corresponding lane Loss of Signal 0= Signal detect Logically named, reflects lane reverse status(?)		10:7
Lane 0 Symbol Invalid	1	0= Valid 8b decode 1= Incorrect disparity **or** code violation.		6
Lane 0 Control Flag	1	1=K character (control) 0= D character (data)		5
Lane 0 8b Data	8	Decoded 8b value		4:0
			A2 (B2)	16:14
Lane 1 Symbol Invalid	1	0= Valid 8b decode 1= Incorrect disparity **or** code violation.		13
Lane 1 Control Flag	1	1=K character (control) 0= D character (data)		12
Lane 1 8b Data	8	Decoded 8b value		11:4
Lane 2 Symbol Invalid	1	0= Valid 8b decode 1= Incorrect disparity **or** code violation.		3
Lane 2 Control Flag	1	1=K character (control) 0= D character (data)		2
Lane 2 8b Data	8	Decoded 8b value		1:0
			A1 (B1)	15:10
Lane 3 Symbol Invalid	1	0= Valid 8b decode 1= Incorrect disparity **or** code violation.		9
Lane 3 Control Flag	1	1=K character (control) 0= D character (data)		8
Lane 3 8b Data	8	Decoded 8b value		7:0

Clock is on A1 bit 16 and B1 bit 16.

Event Code symbol definitions

Event Code Symbol	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
							Err bits	Err bits
	Video	Field						
F0 Pixel	1	0	0	0	1	x	0	0
F0 Filler (including FS/FE)	1	0	0	1	0	x	0	Mismatch
BS	1	x	0	1	1	x	0	Mismatch
SR	1	x	1	0	0	x	0	Mismatch
Content Protection BS	1	x	1	0	1	x	0	Mismatch
Content Protection SR	1	x	1	1	0	x	0	Mismatch
F1 Pixel	1	1	0	0	1	x	0	0
F1 Filler (including FS/FE)	1	1	0	1	0	x	0	Mismatch
	Blanking	Horizontal						
Horizontal Blanking BE	0	0	0	0	0	1	Missed SR	Mismatch
Horizontal Blanking VBID	0	0	0	0	1	0	0	Mismatch
Horizontal Blanking MVID	0	0	0	0	1	1	V_err	Mismatch
Horizontal Blanking MAUD	0	0	0	1	0	0	A_err	Mismatch
SR	0	x	0	1	0	1	0	Mismatch
Horizontal Blanking Dummy	0	0	0	1	1	0	0	0
Horizontal Blanking Audio Stream	0	0	1	0	0	0	0	0
Horizontal Blanking Audio TS	0	0	1	0	0	1	0	0
Horizontal Blanking Reserved	0	0	1	0	1	0	0	0
Horizontal Blanking Extension	0	0	1	0	1	1	0	0
Horizontal Blanking Info Frame	0	0	1	1	0	0	0	0
	Blanking	Vertical						
Vertical Blanking BE	0	1	0	0	0	1	Missed SR	Mismatch
Vertical Blanking VBID	0	1	0	0	1	0	0	Mismatch
Vertical Blanking MVID	0	1	0	0	1	1	V_err	Mismatch
Vertical Blanking MAUD	0	1	0	1	0	0	A_err	Mismatch
SR	0	x	0	1	0	1	0	Mismatch
Vertical Blanking Dummy	0	1	0	1	1	0	0	0
Vertical Blanking MSA	0	1	0	1	1	1	0	0
Vertical Blanking Audio Stream	0	1	1	0	0	0	0	0
Vertical Blanking Audio TS	0	1	1	0	0	1	0	0
Vertical Blanking Reserved	0	1	1	0	1	0	0	0
Vertical Blanking Extension	0	1	1	0	1	1	0	0
Vertical Blanking Info Frame	0	1	1	1	0	0	0	0

Event Code Errors:

These signals are asserted for 1 state and are defined as the following:

Mismatch - The mismatch bit is set when there when the KChar or configuration fields of the active lanes don't match. Checks are made on all KChars and the VBID, MVID and MAUD fields.

V_err (MVID Check) - The V_err bit is set when the no_video bit is set in the VBID and the MVID field is not 0.

A_err (MAUD Check) - The A_err bit is set when the audio_mute bit is set in the VBID and the MVAUD field is not 0.

Missed SR - There is a BE counter on each of the four lanes. If 512 BEs are received without receiving an SR on any lane the Missed SR error is asserted.

AUX Group

Aux Port is a half-duplex, bi-directional channel between DisplayPort transmitter (source) and DisplayPort receiver (sink). It consists of 1 differential pair transporting self-clocked data. The AUX CH supports a bandwidth of **1Mbps.** The DisplayPort Source Device is the master (also referred to as AUX CH requester) that initiates an AUX CH transaction. DisplayPort Sink Device is the slave (also referred to as the replier) is the device that responds to the transaction.

Aux channel has its own clock (67KHz) so that it can be clocked into separate modules in the LA on a separate clock domain. It also has its own dis-assembler that has to be loaded separately.

<table>
<tr><th>Field</th><th>Bits</th><th>Definition</th><th>Probe</th><th>Channel</th></tr>
<tr><td>Command</td><td>4</td><td>Command Field</td><td>B1</td><td>3:0</td></tr>
<tr><td>ADDR[11:0]</td><td>12</td><td>Address Field</td><td>B1</td><td>15:4</td></tr>
<tr><td>ADDR[19:12]</td><td>8</td><td>Address Field</td><td>B2</td><td>7:0</td></tr>
<tr><td>Aux CLK</td><td>1</td><td></td><td>B1</td><td>16</td></tr>
<tr><td>DATA[7:0]</td><td>8</td><td>Data field</td><td>B2</td><td>15:8</td></tr>
<tr><td>SYNC</td><td>1</td><td>Sync Bit
First part of the transfer, CMD, ADDR and DATA are all updated, if SYNC is 0 then only DATA is updated.</td><td>B3</td><td>0</td></tr>
<tr><td>STOP
Spare
Spare
Request</td><td>1
1
1
1</td><td>Stop, last byte of the transfer.

High when transaction is request</td><td>B3
B3
B3
B3</td><td>1
2
3
4</td></tr>
<tr><td>Response</td><td>1</td><td>High when transaction is response</td><td>B3</td><td>5</td></tr>
<tr><td>Timeout</td><td>1</td><td>Response Timer timeout period 300us</td><td>B3</td><td>6</td></tr>
<tr><td>HPD event</td><td>2</td><td>
<table>
<tr><th>Bit 1</th><th>Bit0</th><th>Meaning</th></tr>
<tr><td>0</td><td>0</td><td>Unplugged HPD=Low (level)</td></tr>
<tr><td>0</td><td>1</td><td>HPD pulsed low .25ms to 1.25ms Interrupt event (event signaled on rising edge of HPD)</td></tr>
<tr><td>1</td><td>0</td><td>HPD pulsed low > 1.75ms unplug repluged (event signaled on rising edge of HPD)</td></tr>
<tr><td>1</td><td>1</td><td>Plugged In HPD=High (level)</td></tr>
</table>
</td><td>B3</td><td>8:7</td></tr>
<tr><td>Storage</td><td>1</td><td>Indicates Valid states</td><td>B3</td><td>15</td></tr>
<tr><td>Byte Count</td><td>5</td><td>Number of valid bytes received inclusive of current state</td><td>B4</td><td>10:6</td></tr>
</table>

The Storage bit should be used as a qualifier for storing AUX data.

The rate at which Storage is pulsed depends on the packet type. AUX transfers begin with a four bit CMD, a 20 bit address and 8 bits of data. Some packet types contain additional data which will be presented 8 bits at a time. For the additional bytes the Storage bit will be pulsed as each byte is ready, the Command and ADDR Fields will be unchanged.

10 b decode Groups

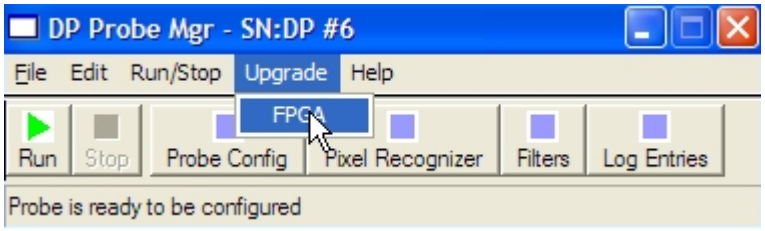
A 10b decode mode is provided in the FS4435. This mode has to be loaded using the Probe Manger at start-up. It requires different connections from the Tek modules and provides the following labels for the user.

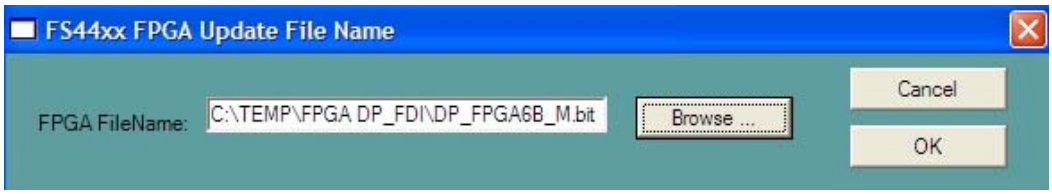
Pre-defined Label	Bits	Definition/Usage	Logic Analyzer Probes
Align Flag	1	1= Alignment of multi-lane link detected	A4[4]
Any Invalid Error Flag	1	1= This state includes an 8b10b code error (either disparity error or decode error in any active lane)	A4[3]
LOS [3,2,1,0]	4	1= Corresponding lane Loss of Signal 0= Signal detect on lane (x2 x4 mode only)	A4[2:0] A3[16]
Any LOS	1	1= Loss of Signal detected in any active lane 0= Signal detected in all active lanes	A3[15]
Lane 0 Disparity Error	1	1= Lane 0 data has incorrect 8b10b disparity	A3[14]
Lane 0 Invalid Decode Error	1	1= Lane 0 data is not a valid 8b10b code	A3[13]
Lane0	10	Physical Lane 0 Data, 10-bit encoded	A3[12:3]
Lane 1 Disparity Error	1	1= Lane 1 data has incorrect 8b10b disparity	A3[2]
Lane 1 Invalid Decode Error	1	1= Lane 1 data is not a valid 8b10b code	A3[1]
Lane1	10	Physical Lane 1 Data, 10-bit encoded	A3[0] A2[16:8]
Lane 2 Disparity Error	1	1= Lane 2 data has incorrect 8b10b disparity	A2[7]
Lane 2 Invalid Decode Error	1	1= Lane 2 data is not a valid 8b10b code	A2[6]
Lane2	10	Physical Lane 2 Data, 10-bit encoded	A2[5:0] A1[15:12]
Lane 3 Disparity Error	1	1= Lane 3 data has incorrect 8b10b disparity	A1[11]
Lane 3 Invalid Decode Error	1	1= Lane 3 data is not a valid 8b10b code	A1[10]
Lane3	10	Physical Lane 3 Data, 10-bit encoded	A1[9:0]

Clock is inputted to CK3

FPGA Upgrade

The FS4435 Probe Manager has the ability to reprogram any of the2 firmware program locations in the probe.
If a FS4435 probe firmware upgrade is required a new file will be provided by FuturePlus Systems. Copy the file on the hard drive of the PC that hosts the FS4435 Probe Manager. Click on the “Upgrade” button on the Probe Manager and then browse to the location where the firmware upgrade was stored.





When the upgrade process is complete the Probe Manager will remind the user to reboot the FS4435 probe and the Probe Manager software.

General Information

This chapter provides additional reference information including the characteristics and signal connections for the FS4435 probe.

Characteristics

The following operating characteristics are not specifications, but are typical operating characteristics for the FS4435 probe.

Standards Supported

If the product is used in a manner not specified by manufacturer, then the protection provided by the equipment may become impaired.

DisplayPort version 1.1a

Power Requirements

100-240VAC, 2 amps.

Logic Analyzer Required

Tektronix TLA7AA4 modules installed in a TLA71x or TLA70xx frame.

Number of Probes Used

The State Adapter Probe interface uses 4 FS1055 cables of 90 pin type.

Environmental Temperature

Non operating: -40 to +75 degrees C (-40 to +167 degrees F)

Operating: 20 to 30 degrees C (68 – 86 degrees F)

Altitude

Operating: 4,6000m (15,000 ft)

Non operating: 15,3000m (50,000 ft)

Humidity

Up to 80% relative humidity. Avoid sudden, extreme temperature changes which would cause condensation on the FS4435 module.

Testing and Troubleshooting Servicing

There are no automatic performance tests or adjustments for the FS4435 module. If a failure is suspected in the FS4435 module contact the factory or your FuturePlus Systems authorized distributor.

The repair strategy for the FS4435 is module replacement. However, if parts of the FS4435 module are damaged or lost contact the factory for a list of replacement parts.