ACE-B8700 Board

PCI I/O Board with discrete I/O, battery backup SRAM, Timer, Power-off intrusion Event Logger and Protect-U

User Manual

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Revision

Version	Date	Author	Description
1.0	2010/03/01	Kenny Lee	Initial release

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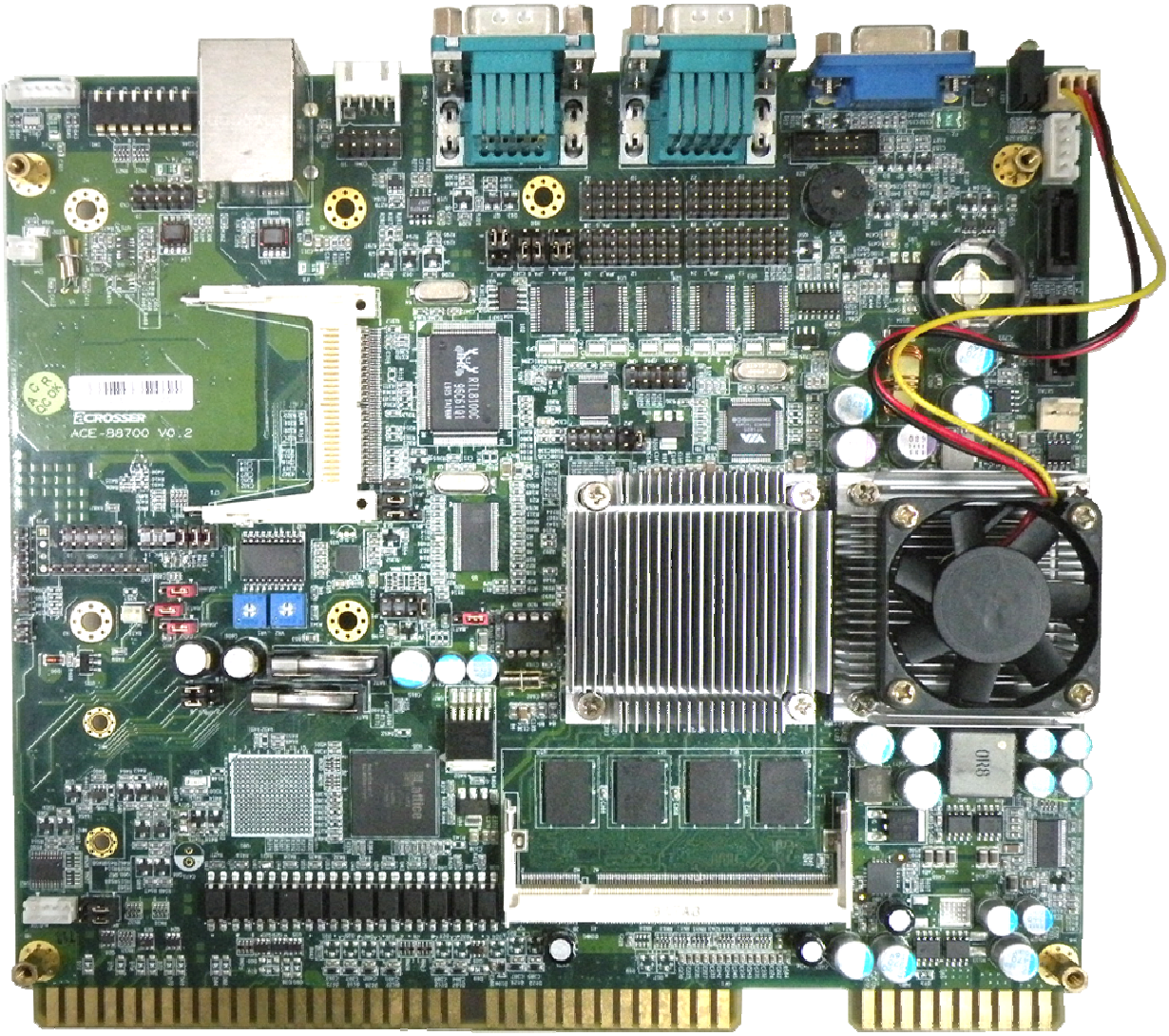
1 INTRODUCTION

Welcome to the ACE-B8700 Computer. The ACE-B8700 is an All-in-One gaming board integrated a VIA VX800 industrial computer with Acrosser's gaming controller. This gaming controller features digital input, digital output, SRAM, timer, intrusion logger, secured real time clock and security ID. Together with the software development kit (SDK), ACE-B8700 is very easy to control devices in a gaming machine. Please refer to following specification for detail functions.



1.1 Specifications

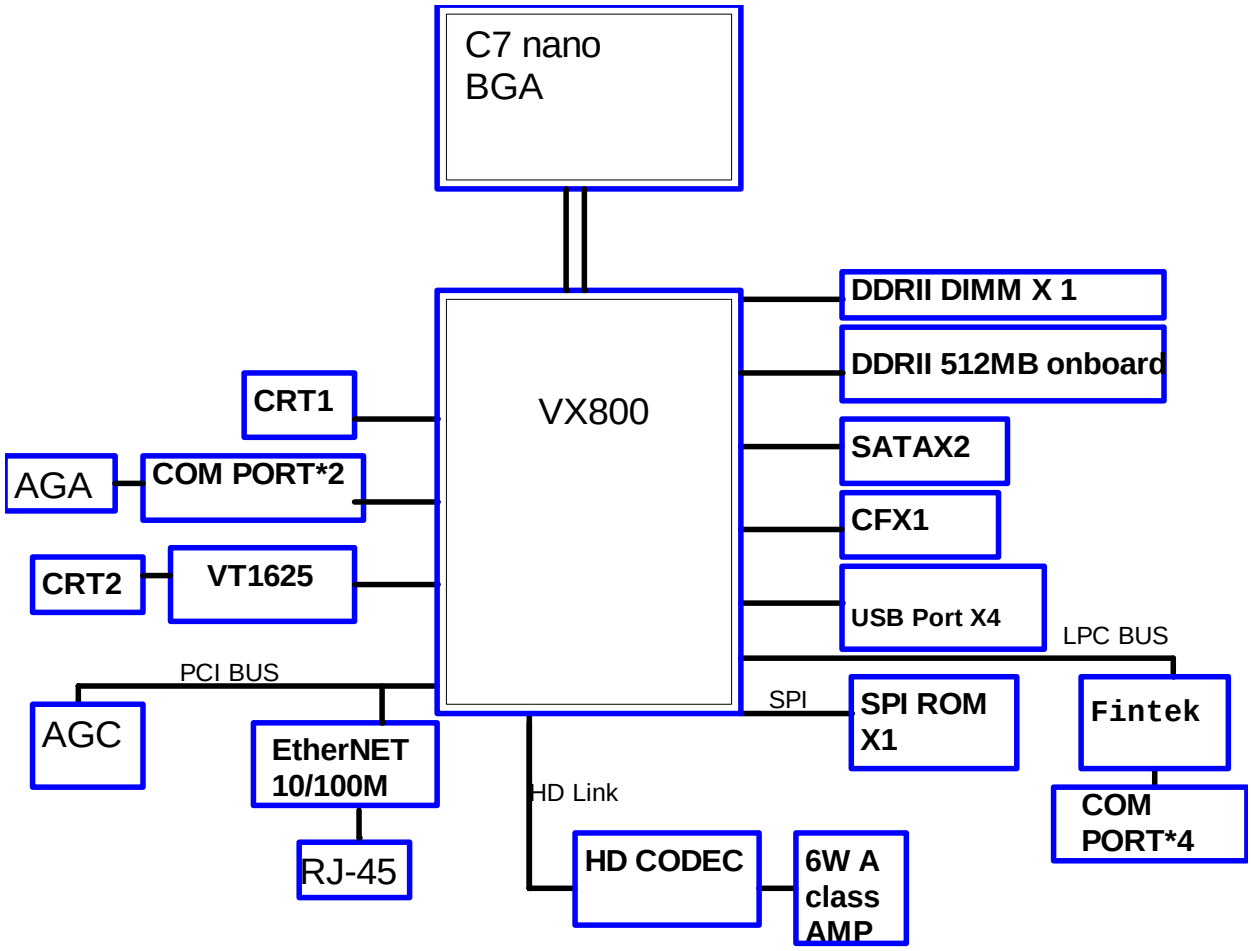
- VIA C7 1.5GHz processor, VX800 chipset.
  - 3D core support DX9
  - VIA PadLock engine: AES, RNG, Security Hash
- Optional on board 512MB DDR2 memory
- VGA DB15 output + optional secondary VGA
- Digital Input: 25 x optical isolated and 5 TTL level input for door switch with intrusion logger
- Digital Output: 25x 500mA , 2 x 1000mA
- 4 x 16-bit Interruptible Timer
- 4 x RS-232 serial ports
- 72-pin golden finger interface
- ProtectU and Optional iButton socket for software security
- Single 256KB battery back-up SRAM with battery low monitor for each battery
- Secondary real time clock
- One 8-bit readable DIP switch
- 6 watts Stereo amplifier

1.2 Package Contents

Check if the following items are included in the package.

- Quick Manual
- ACE-B8700 board
- 1 x Software Utility CD

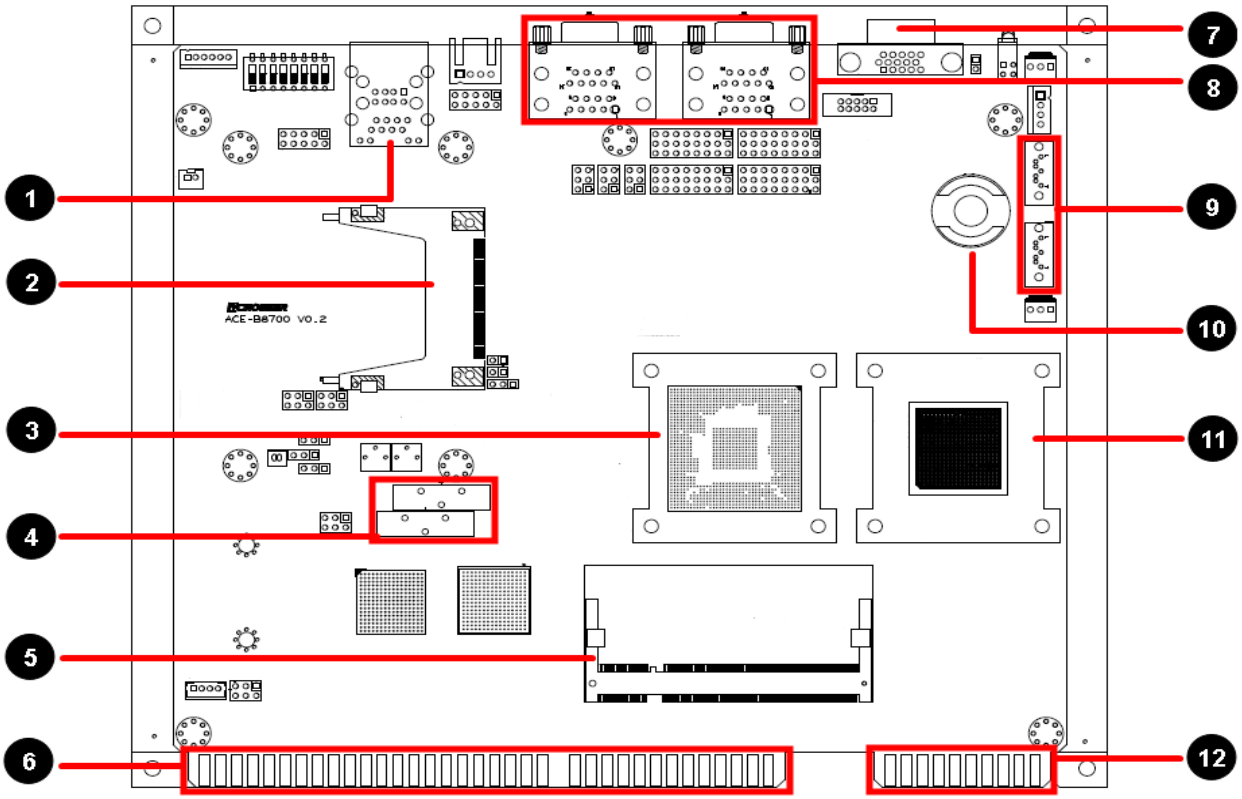
1.3 Block Diagram



2 H/W INFORMATION

This chapter describes the installation of ACE-B8700. At first, it shows the Function diagram and the layout of ACE-B8700. It then describes the unpacking information which you should read carefully, as well as the jumper/switch settings for the ACE-B8700 configuration.

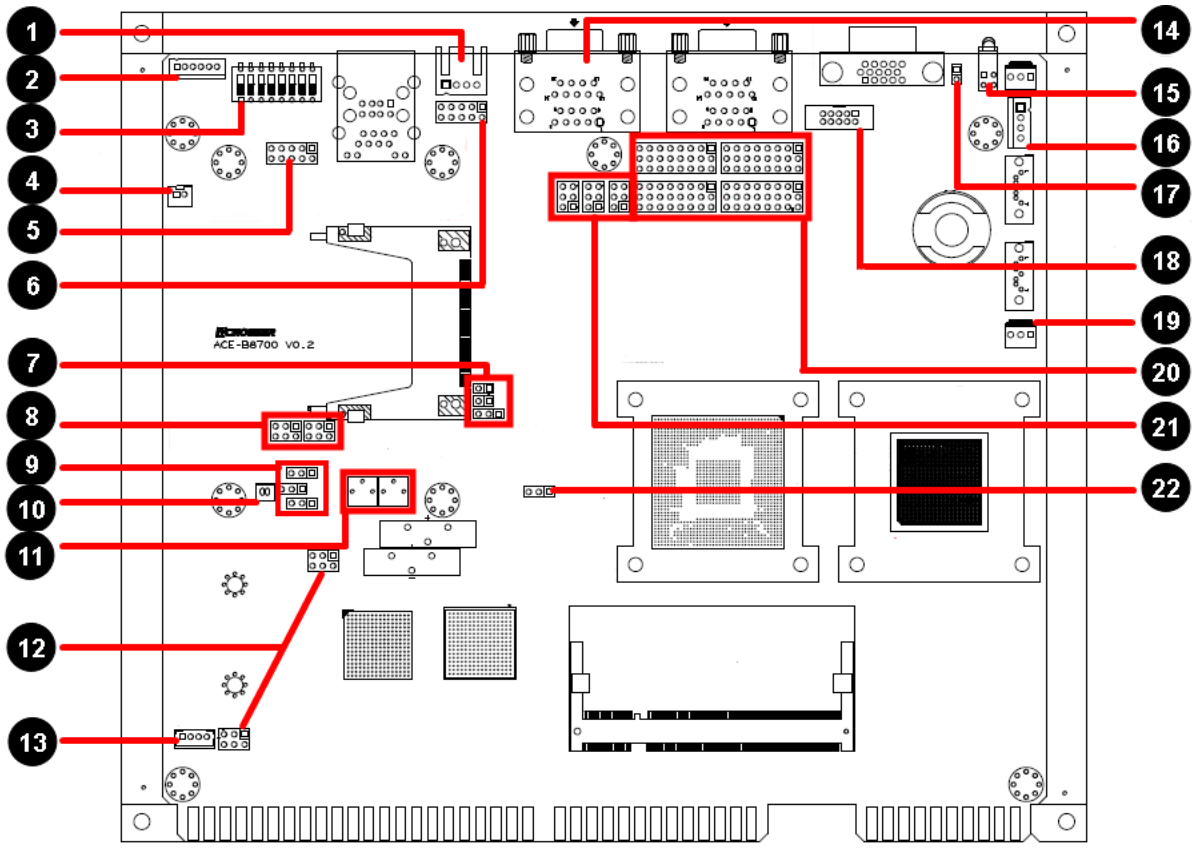
2.1 Locations (Top Side)



1	**USB1** One RJ45 with two layer USB connector	5	**DIMM1** DDR2 SODIMM socket	9	**SATA1 & SATA2** Standard 7-pin SATA connector
2	**CF1** Standard CF Card Slot	6	**72 Pins Golden Fingers** General Gaming interface	10	**U73** iButton holder
3	**U6** Chipset VIA VX800	7	**VGA1** D-Sub 15-pin VGA connector	11	**U2** Processor VIA C7 1.5G
4	**BAT1** CR2032 Size Coin Battery **BAT2** CR2032 Size Coin Battery for AGA/SRAMA	8	**COM1_2 & COM3_4** Dual D-Sub 9-pin RS232 connector	12	**20 Pins Golden Fingers** Work with 72 Pins Golden Fingers

2.2 Connector and Jumper Setting

2.2.1 Locations (Top side)

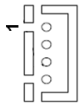


2.2.2 List of Connector and Jumper Setting

1	**CCTALK1** JST connector for ccTalk (Signal share with COM6).	2	**KM1** JST connector for Keyboard and Mouse.	3	**SW1** 8-bit readable DIP switch.
4	**CN4** JST connector for Case Open Intrusion logger.	5	**CN3** Pin header for 2 USB ports.	6	**COM6(optional)** Pin header for RS232 port.
7	**JP11** CF Card master/slave select pin header. **JP13** CF Card Voltage select pin header.	8	**JPC_2** Bill enable, Coin enable and Hopper pre-set pin header.	9	**JBAT3** SRAM A and SRAM B supply voltage select from BAT2 or BAT3 pin header. **JSRAMA & JSRAMB** SRAM A and SRAM B data clear pin header.
10	**BAT3(optional)** Rechargeable Battery for SRAM A and SRAM B.	11	**VR1 & VR2** Adjust audio volume.	12	**JPB_1** Select Audio output with/without amplifier pin header. **JPB_2** Select SPEAKER RIGHT+ connect to 72 Pins Golden Fingers (B4, B5) or (A2, B2).
13	**AUDIO1** JST connector for Audio output.	14	**COM3_4** RS232/ccTalk/RS485 output.	15	**LED1** LED for Power & HDD.
16	**SATAPWR1** JST connector for SATA power.	17	**JP20** Reset pin header.	18	**VGA2(optional)** Secondary VGA.
19	**FAN1** CPU Fan Connector.	20	**JPA_1 & JPA_2** Select COM1 or COM2 is RS232 or TTL. **JPA_3** Select COM3 is RS232 or ccTalk. **JPA_5** Select COM4 is RS232 or RS485.	21	**JPA_4** Select COM3 is RS232 or ccTalk. **JPA_6** Select COM4 is RS232 or RS485. **JPA_7** Select COM6 is RS232 or ccTalk.
22	**JBAT1** CMOS clear pin header.				

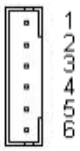
2.3 Connector and Jumper Setting Table

1. CCTALK1



Pin	Signal
1	DATA
2	COM
3	NC
4	12V

2. KM1



Pin	Signal
1	Mouse data
2	Keyboard data
3	GND
4	5V
5	Mouse clock
6	Keyboard clock

3. SW1

Status	Signal
ON	GND
OFF	3.3V

4. CN4

Pin	Signal
1	Case open
2	GND

5. CN3

Pin	Signal	Pin	Signal
1	5V	2	5V
3	-USB0	4	-USB2
5	+USB0	6	+USB2
7	GND	8	GND
9	NC	10	GND

6. COM6

Pin	Signal	Pin	Signal
1	-DCD	2	-DSR
3	SIN	4	-RTS
5	SOUT	6	-CTS
7	-DTR	8	-RI
9	GND	10	NC

7. JP11/JP13

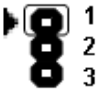
	JP11
Pin	Setting
1-2 Open	Slave
1-2 Close	Master (default)

	JP13
Pin	Setting
1-2 Close	5V
2-3 Close	3.3V (default)

8. JPC_2

Pin	Status	Setting
1-2	Open	Preset is LOW
	Close (default)	Preset is HIGH
3-4	Open	Preset is LOW
	Close (default)	Preset is HIGH
5-6	Open	Preset is LOW
	Close (default)	Preset is HIGH

9. JBAT3/JSRAMA/JSRAMB



	JBAT3	JSRAMA JSRAMB
Pin	Setting	Setting
1-2 close	BAT2 (default)	Normal (default)
2-3 close	BAT3	Clear SRAM

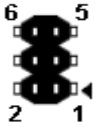
10. BAT3

Pin	Signal
1	GND
2	3.3V

11. VR1/VR2

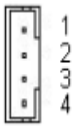
Adjust volume level by turning VR clockwise

12. JPB_1/JPB_2



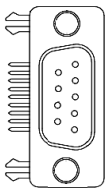
	JPB_1	JPB_2
Pin	Setting	Setting
1-3, 2-4 close	Audio Out with Amplifier (default)	SPEAKER RIGHT+ connect to 72 Pins Golden Fingers(B5, B4) (default)
3-5, 4-6 close	Audio Out without Amplifier	SPEAKER RIGHT+ connect to 72 Pins Golden Fingers(A2, B2)

13. AUDIO1



Pin	Signal
1	SPEAKER RIGHT+
2	GND
3	SPEAKER LEFT+
4	GND

14. COM3_4

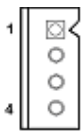


		COM3	COM4
Pin	RS232	ccTalk	RS485
1	-DCD	12V	-
2	SIN	Data	Data+
3	SOUT	-	Data-
4	-DTR	-	-
5	GND	GND	-
6	-DSR	-	-
7	-RTS	-	-
8	-CTS	-	-
9	-RI	-	-

15. LED1

LED	Signal
Green	HDD
Red	Power

16. SATAPWR1

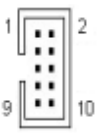


Pin	Signal
1	12V
2	GND
3	3.3V
4	5V

17. JP20

Pin	Signal
1	Reset
2	GND

18. VGA2

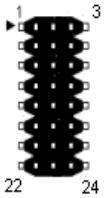


Pin	Signal	Pin	Signal
1	RED	2	GND
3	GREEN	4	GND
5	BLUE	6	GND
7	VSYNC	8	SCL
9	HSYNC	10	SDA

19. FAN1

Pin	Signal
1	GND
2	12V
3	NC

20. JPA_1/JPA_2/JPA_3/JPA_5

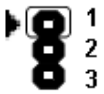


	JPA_1 & JPA_2	JPA_3	JPA_5
Pin	**Setting**	**Setting**	**Setting**
1-2, 4-5, 7-8, 10-11, 13-14, 16-17, 19-20, 22-23 Close	TTL Output	ccTalk output	RS485 output
2-3, 5-6, 8-9, 11-12, 14-15, 17-18, 20-21, 23-24 Close	RS232 output (default)	RS232 output (default)	RS232 output (default)

21. JPA_4/JPA_6/JPA_7

	JPA_4	JPA_6	JPA_7
Pin	**Setting**	**Setting**	**Setting**
1-3, 2-4 Close	RS232 (default)	RS232 (default)	RS232
3-5, 4-6 Close	ccTalk	RS485	ccTalk (default)

22. JBAT1



Pin	Setting
1-2 Close	Normal (default)
2-3 Close	Clear COMS

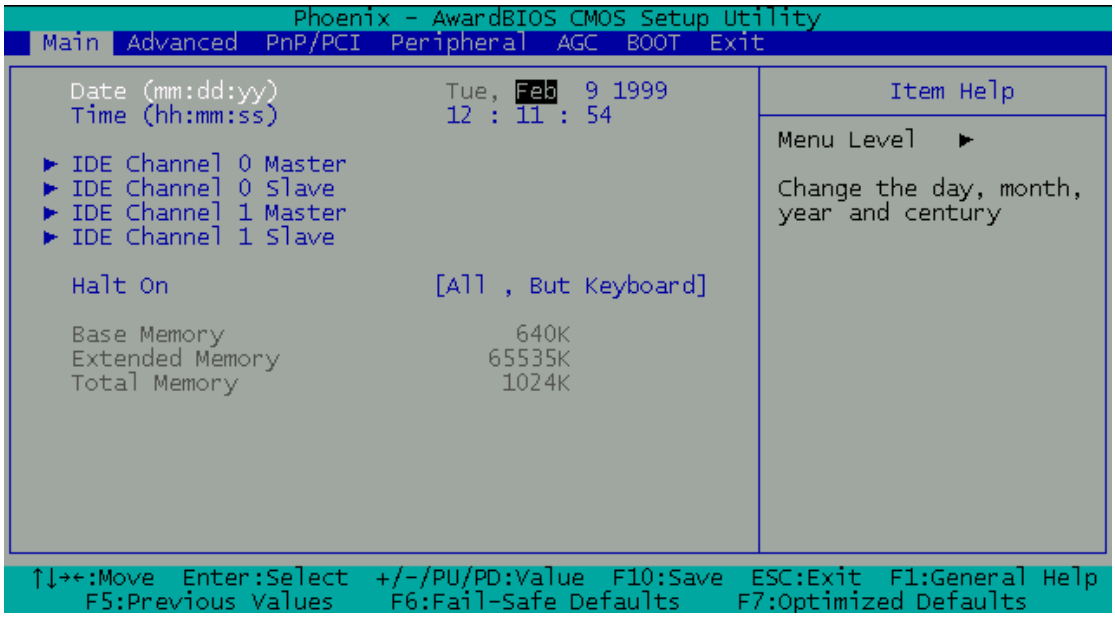
3 BIOS SETTING

This chapter describes the BIOS menu displays and explains how to perform common tasks needed to get the system up and running. It also gives detailed explanation of the elements found in each of the BIOS menus. The following topics are covered:

- Main Setup
- Advanced Chipset Setup
- Peripherals Setup
- PnP/PCI Setup
- AGC Setup
- Boot Setup
- Exit Setup

3.1 Main Setup

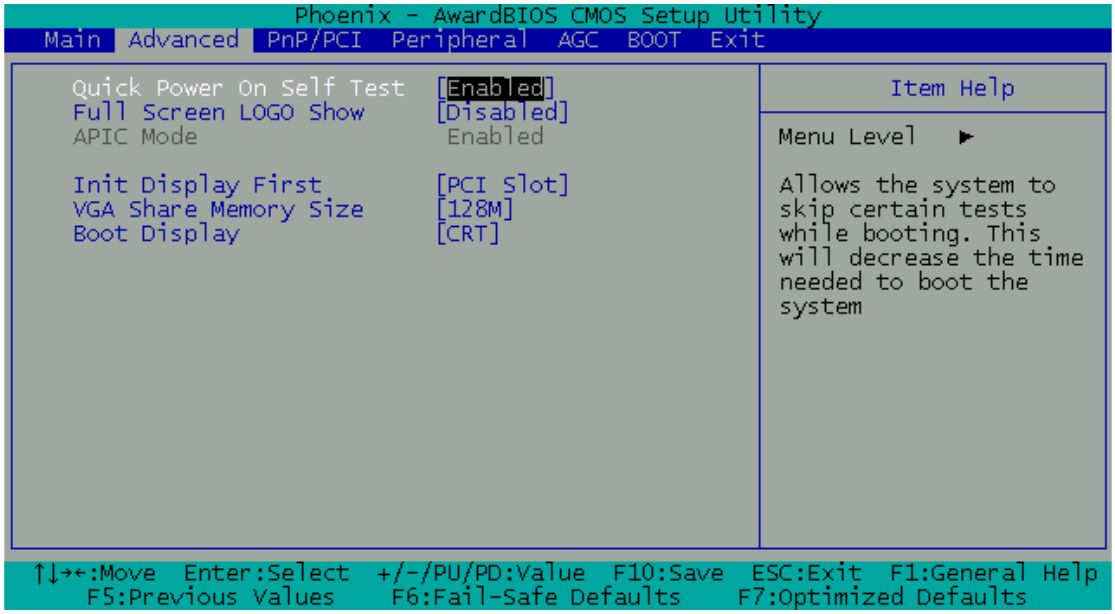
Once you enter the Award BIOS™ CMOS Setup Utility, the Main Menu will appear on the screen. Use the arrow keys to highlight the item and then use the <Pg Up> <Pg Dn> keys to select the value you want in each item.



Note: Listed at the bottom of the menu are the control keys. If you need any help with the item fields, you can press the <F1> key, and it will display the relevant information.

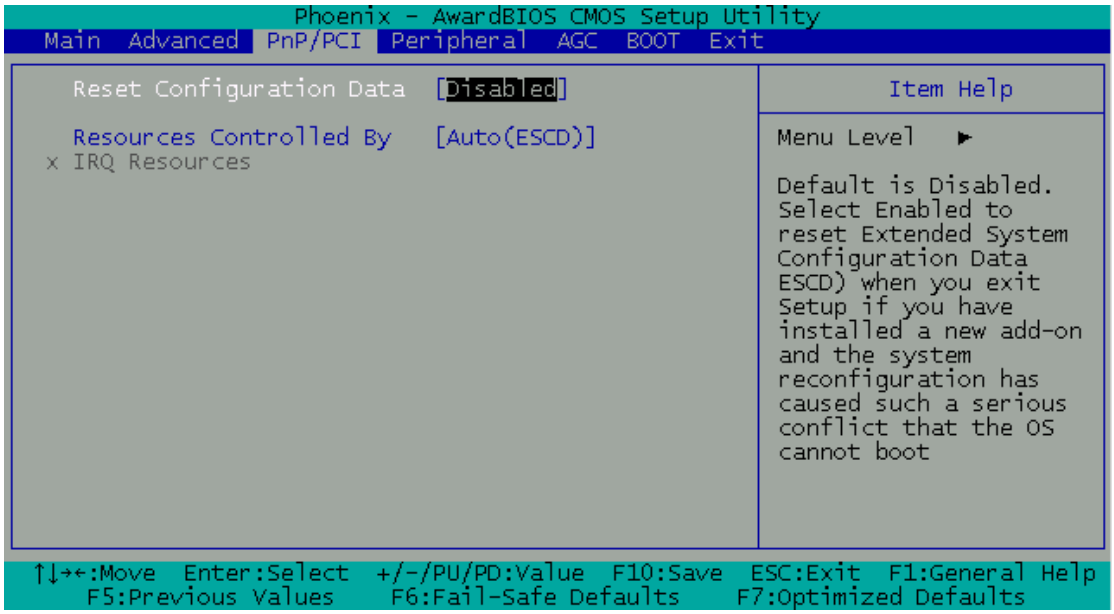
Option	Choice	Description
Date Setup	N/A	Set the system date. Note that the 'Day' automatically changes when you set the date
Time Setup	N/A	Set the system time
IDE Channel 0 Master/Slave	N/A	The onboard PCI IDE connectors provide 1 channel for connecting up to 2 IDE hard disks or other devices. The first is the "Master" and the second is "Slave", BIOS will auto-detect the IDE type.
Halt On	All Errors, No Errors, All but keyboard.	Select the situation in which you want the BIOS to stop the POST process and notify you.

3.2 Advanced Chipset Setup



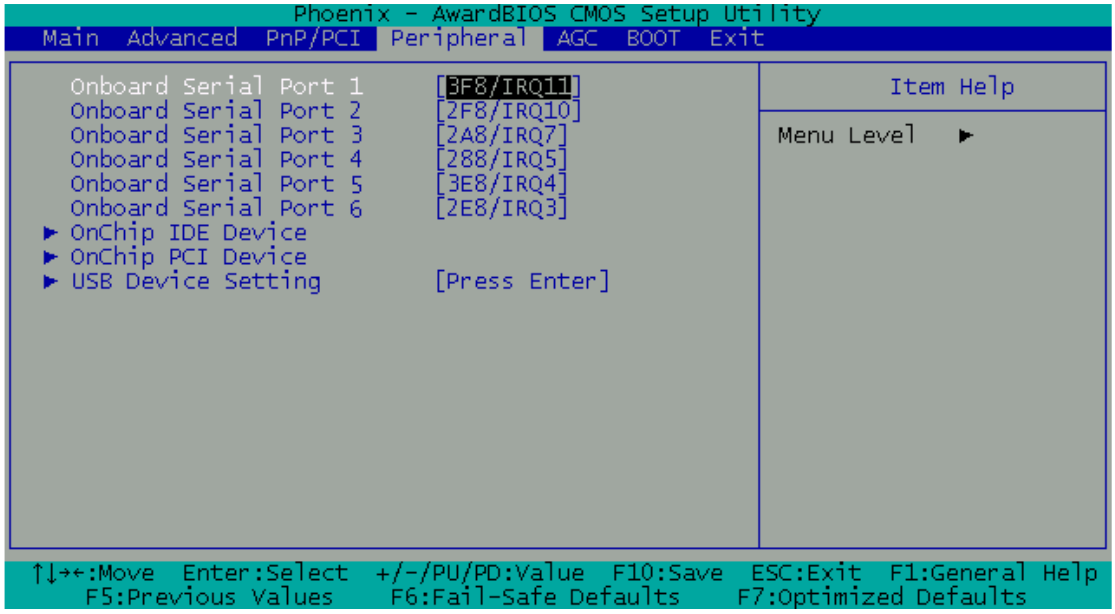
Option	Choice	Description
Quick Power On Self Test	Enabled Disabled	This category speeds up Power On Self Test (POST) after you have powered up the computer. If it is set to Enable, BIOS will shorten or skip some check items during POST.
Full Screen Logo Show	Enabled Disabled	Select *Enabled* to show the OEM full screen logo if you have add-in BIOS.
VGA Share Memory Size	64M 128M 256M	This Item is for setting the Frame Buffer (Share system memory as display memory).
Boot Display	CRT CRT+CRT2	This Item is to set display device

3.3 PnP/PCI setup



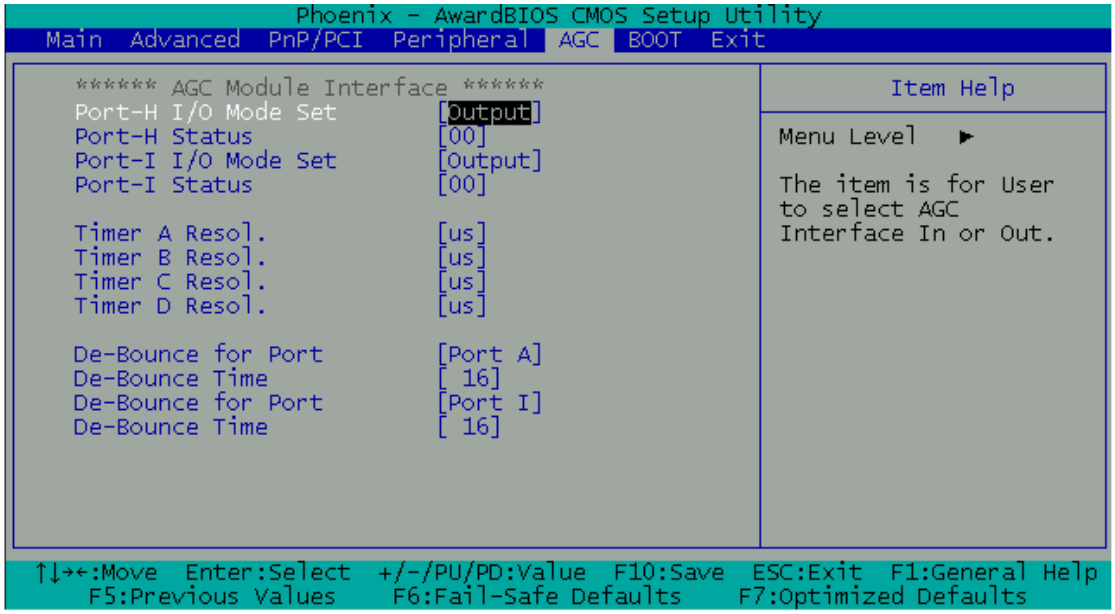
Option	Choice	Description
Reset Configuration Data	Enabled Disabled	Normally, you leave this field Disabled. Select Enabled to reset Extended System Configuration Data (ESCD) when you exit Setup. If you have installed a new add-on and the system reconfiguration has caused such a serious conflict, then the operating system cannot boot.
Resources Controlled By	Auto(ESCD) Manual	The Award Plug and Play BIOS has the capacity to automatically configure all of the boot and Plug and Play compatible devices. However, this capability means absolutely nothing unless you are using a Plug and Play operating system such as Windows 95. If you set this field to “manual,” then you may choose specific resources by going into each of the submenus.
IRQ Resources	N/A	When resources are controlled manually, assign a type to each system interrupt, depending on the type of the device that uses the interrupt

3.4 Peripherals Setup



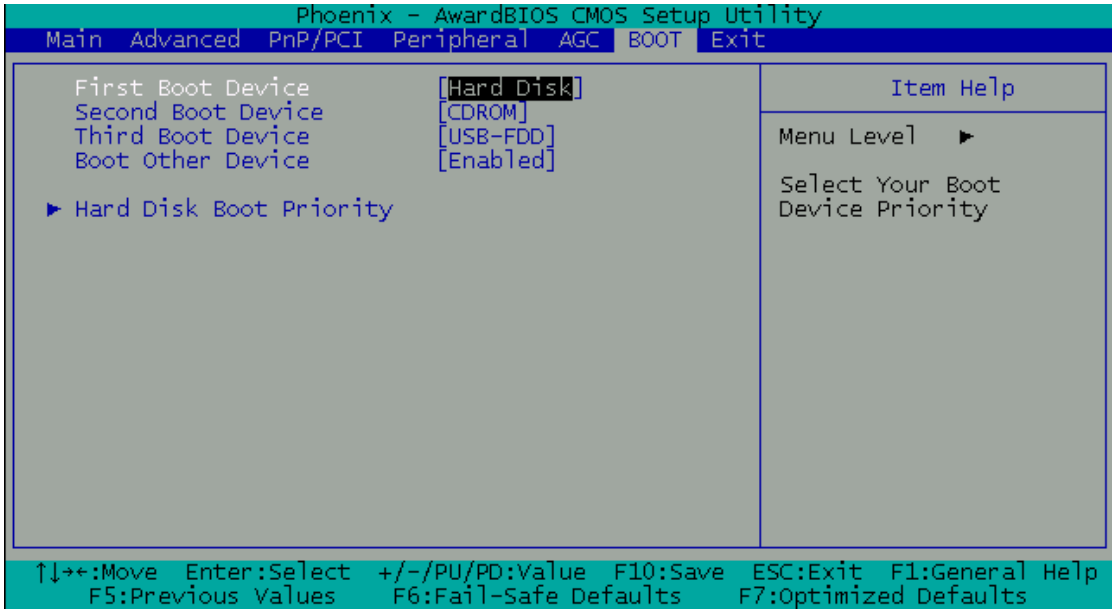
Option	Choice	Description
Onboard Serial Port 1 **Onboard Serial Port 2** **Onboar`d Serial Port 3** **Onboard Serial Port 4** **Onboard Serial Port 5** **Onboard Serial Port 6**	Serial Port 1: 3F8 / IRQ11 Serial Port 2: 2F8 / IRQ10 Serial Port 3: 2A8 / IRQ7 Serial Port 4: 288 / IRQ5 Serial Port 5: 3E8 / IRQ4 Serial Port 6: 2E8 / IRQ3	Select an address and the corresponding interrupt for each serial port.
On chip IDE DEVICE		The integrated peripheral controller contains an IDE interface with support for two IDE channels. Select Enabled to activate each channel separately.
USB Device Setting	Enabled Disabled	Select *Enabled* if your system contains a Universal Serial Bus (USB) 2.0 controller and you have USB peripherals
OnChip PCI Device		This item allows you to decide to enable/disable AC97 Audio

3.5 AGC Setup



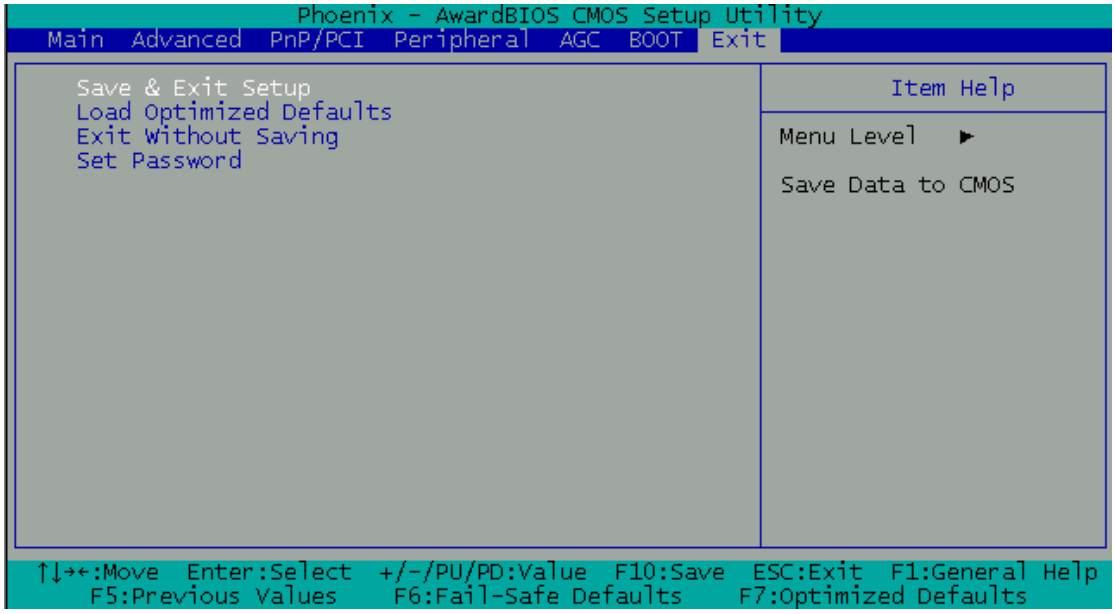
Option	Choice	Description
Port-H I/O Mode Set	Output Input	
Port-H Status	00 to FF	If Port H I/O Mode is “Output” , User can modify it
Port-I I/O Mode Set	Output Input	
Port-I Status	00 to FF	If Port I I/O Mode is “Output” , User can modify it
Timer A/B/C/D Resolution.	us / ms / sec	For timer resolution ‘us’=microsecond ‘ms’=millisecond ‘sec’=second
De-bounce Time for Port	A B C D E F G H	Select one of these Ports to set De-bounce Time
Port A~H de-bounce Time	0-255	Setting de-bounce time for each I/O port. The value 0 means that the de-bounce time is 1 ms. The default setting is 16 (i.e. 17 ms).
De-bounce Time for Port	I J	Select one of these Ports to set De-bounce Time
Port I/J de-bounce Time	0-255	Setting de-bounce time for each I/O port. The value 0 means that the de-bounce time is 1 ms. The default setting is 16 (i.e. 17 ms).

3.6 Boot setup



Option	Choice	Description
First / Second / Third Boot Device/Other Boot Device	Hard Disk CDROM USB-FDD USB-CDROM Disabled	The BIOS attempts to load the operating system from the devices in the sequence selected in these items.
Hard Disk Boot Priority	N/A	These fields set the Boot Priority for each Hard Disk (SATA/IDE HDD and USB Flash)

3.7 Exit Setup



Option	Choice	Description
Save & Exit Setup	Pressing <Enter> on this item for confirmation: Save to CMOS and EXIT (Y/N)? Y	Press “Y” to store the selections made in the menus in CMOS – a special section of memory that stays on after you turn your system off. The next time you boot your computer, the BIOS configures your system according to the Setup selections stored in CMOS. After saving the values the system is restarted again
Load Optimized Defaults	When you press <Enter> on this item you get a confirmation dialog box with a message like this: Load Optimized Defaults (Y/N)? N	Press ‘Y’ to load the default values that are factory-set for optimal-performance system operations.
Exit Without Saving	Pressing <Enter> on this item for confirmation: Quit without saving (Y/N)? Y	This allows you to exit Setup without storing any changes in CMOS. The previous selections remain in effect. This shall exit the Setup utility and restart your computer.
Set Password	Pressing <Enter> on this item for confirmation: ENTER PASSWORD:	When a password has been enabled, you will be prompted to enter your password every time you try to enter Setup. This prevents unauthorized persons from changing any part of your system configuration. Type the password, up to eight characters

		in length, and press <Enter>. The password typed now will clear any previous password from the CMOS memory. You will be asked to confirm the password. Type the password again and press <Enter>. You may also press <Esc> to abort the selection and not enter a password. To disable a password, just press <Enter> when you are prompted to enter the password. A message will confirm that the password will be disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

4 AGC REGISTER DESCRIPTION

This chapter describes the function of the Register inside an AGC chip. To program the application's software, an user must have the know-how of these Registers.

4.1 PCI Configuration Register

PCI CFG Register Offset Address	32 bit Register				PCI Readable	PCI Writable
	31 24	23 16	15 8	7 0		
00h	Device ID		Vendor ID		Yes	No
04h	Status		Command		Yes	No
08h	Class Code			Revision ID	Yes	No
0Ch	BIST	Header Type	Latency Timer	Cache Line Size	Yes	No
10h	PCI Base Address 0 for Memory Mapped Configuration Registers				Yes	Yes
14h	PCI Base Address 1 for I/O Mapped Configuration Registers				Yes	Yes
18h	PCI Base Address 2 (Not Supported)				No	No
1Ch	PCI Base Address 3 (Not Supported)				No	No
20h	PCI Base Address 4 (Not Supported)				No	No
24h	PCI Base Address 5 (Not Supported)				No	No
28h	Cardbus CIS Pointer (Not Supported)				Yes	No
2Ch	Subsystem ID		Subsystem Vendor ID		Yes	No
30h	PCI Base Address for Local Expansion ROM (Not Supported)				Yes	No
34h	Reserved				No	No
38h	Reserved				No	No
3Ch	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Yes	Yes / No

Vendor ID Register (00h : 01h)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
15 : 0	Vendor ID. Identifies manufacturer of the device.	Yes	No	1204h

Device ID Register (02h : 03h)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
31 : 16	Device ID. Identifies particular device.	Yes	No	8700h

Command Register (04h : 05h)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
0	I/O Space. Value of 1 allows device to respond to I/O space accesses.	Yes	No	1
1	Memory Space. Value of 1 allows device to respond to memory space accesses	Yes	No	1
2	Master Enable. Value of 0 disables device from generating bus master accesses. **Not Supported**	Yes	No	0
3	Special Cycle. **Not Supported.**	Yes	No	0
4	Memory Write/Invalidate**. Not Supported.**	Yes	No	0
5	VGA Palette Snoop. **Not Supported.**	Yes	No	0
6	Parity Error Response. **Not Supported.**	Yes	No	0
7	Wait Cycle Control. **Not Supported.**	Yes	No	0
8	SERR# Enable. **Not Supported.**	Yes	No	0
9	Fast Back-to-Back Enable. **Not Supported.**	Yes	No	0
15 : 10	Reserved	Yes	No	0

Status Register (06h : 07h)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
22 : 16	Reserved	Yes	No	0
23	Fast Back-to-Back Capable. **Not Supported.**	Yes	No	0
24	Master Data Parity Error Detected. **Not supported**	Yes	No	0
26 : 25	DEVSEL Timing. Value of 01 is **Slow**.	Yes	No	10
27	Target Abort. 1 if Device has Signal Target Abort.	Yes	Yes	0
28	Received Target Abort. **Not Supported.**	Yes	No	0
29	Received Master Abort. **Not Supported.**	Yes	No	0
30	Signaled System Error. **Not Supported.**	Yes	No	0
31	Detected Parity Error. **Not Supported.**	Yes	No	0

Revision ID Register (08h)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
7 : 0	Revision ID. Identifies particular device.	Yes	No	15h

Class Code Register (09h : 0Bh)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
15 : 8	Specific Register Level Programming Interface (00h). No interface defined.	Yes	No	00h
23 : 16	Subclass Encoding (80h). Other bridge device.	Yes	No	80h
31 : 24	Base Class Encoding. Other bridge Device.	Yes	No	06h

Cache Line Size Register (0Ch)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
7 : 0	System Cache Line Size (in units of 32-bit words). Can be written and read; however, the value has no effect on operation of chip.	Yes	No	0

Latency Timer Register (0Dh)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
15 : 8	PCI Latency Timer. **Not Supported.**	Yes	No	0

Header Type Register (0Eh)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
22 : 16	Configuration Layout Type. Specifies layout of bits 10h through 3Fh in configuration space. Only one encoding 0 is defined. All other encodings are reserved.	Yes	No	0
23	Header Type. Value of 1 indicates multiple functions. Value of 0 indicates a single Function.	Yes	No	0

Built-In Self Test Register (0Fh)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
31 : 24	Built-In Self Test. Value of 0 indicates that device has passed its test. **Not Supported.**	Yes	No	0

Base Address 0 Registers for Memory Accesses to Local Configuration (10h)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
0	Memory Space Indicator. Value of 0 indicates register maps into Memory space. Value of 1 indicates register maps into I/O space.	Yes	No	0
2 : 1	Location of register: 00 = Locate anywhere in 32 bit memory address space 01 = Locate below 1 MB memory address space 10 = Locate anywhere in 64 bit memory address space 11 = Reserved	Yes	No	0
3	Prefetchable. Value of 1 indicates no side effect on reads.	Yes	No	0
6 : 4	Memory Base Address. Memory base address for access to local configuration registers (default 8 Kbytes).	Yes	No	0
31 : 7	Memory Base Address. Memory base address for access to local configuration registers.	Yes	Yes	0

Base Address 1 Register for I/O Accesses to Local Configuration (14h)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
0	Memory Space Indicator. Value of 0 indicates register maps into Memory space. Value of 1 indicates register maps into I/O space.	Yes	No	1
1	Reserved	Yes	No	0
6 : 2	I/O Base Address. Base address for I/O access to local configuration registers **(default 128 bytes).**	Yes	No	0
31 : 7	I/O Base Address. Base address for I/O access to local configuration registers	Yes	Yes	0

Base Address 2 Registers (18h)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
31 : 0	Not Supported	Yes	No	0

Base Address 3 Registers (1Ch)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
31 : 0	Not Supported	Yes	No	0

Base Address 4 Registers (20h)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
31 : 0	Not Supported	Yes	No	0

Base Address 5 Registers (24h)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
31 : 0	Not Supported	Yes	No	0

Cardbus CIS Pointer Registers (28h)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
31 : 0	Card bus Information Structure Pointer for PCMCIA. **Not Supported.**	Yes	No	0

Subsystem Vendor ID Registers (2Ch)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
15 : 0	Subsystem Vendor ID (Unique add-in board Vendor ID)	Yes	Yes	00h

Subsystem ID Registers (2Eh)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
31 : 16	Subsystem ID. (Unique add-in board Device ID)	Yes	Yes	00h

Base Address for Local Expansion ROM Registers (30h)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
31 : 0	Not Supported	Yes	No	0

Interrupt Line Registers (3Ch)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
7 : 0	Interrupt Line Routing Value indicates which system interrupt controller(s) input the interrupt line of device is connected to.	Yes	Yes	0

Interrupt Pin Registers (3Dh)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
15 : 8	Interrupt Pin Register indicates the interrupt pin that the device uses. The following values are decoded: 0 = No Interrupt Pin 1 = INTA# 2 = INTB# 3 = INTC# 4 = INTD# **Note:** supports only one PCI interrupt (INTA#).	Yes	No	1

Min Gnt Registers (3Eh)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
23 : 16	Min Gnt. Specifies needed length of Burst period for the device, assuming a clock rate of 33 MHz. Value is a multiple of 1/4 µs increments. **Not Supported.**	Yes	No	0

Max Lat Registers (3Fh)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
31 : 24	Max Lat. Specifies how often the device must gain access to PCI bus. Value is a multiple of 1/4 µs increments. **Not Supported.**	Yes	No	0

4.2 SRAM Memory Address Map

The following table shows the SRAM Memory Address map (max. 1024 KB) and their offset addresses, relative to the ***"PCI Base Address 0"***. To access SRAM memory, the user must use Byte-Access command.

Memory Offset Address	32 bit Data width				Software Readable	Software Writable
	31 24	23 16	15 8	7 0		
00h	Byte 3	Byte 2	Byte 1	Byte 0	Yes	Yes
04h	Byte 7	Byte 6	Byte 5	Byte 4	Yes	Yes
08h	Byte 11	Byte 10	Byte 9	Byte 8	Yes	Yes
....	**....**	**....**	**....**	**....**	Yes	Yes
....	**....**	**....**	**....**	**....**	Yes	Yes
FFFF4h	Byte 1048567	Byte 1048566	Byte 1048565	Byte 1048564	Yes	Yes
FFFF8h	Byte1048571	Byte 1048570	Byte 1048569	Byte 1048568	Yes	Yes
FFFFCh	Byte 1048575	Byte 1048574	Byte 1048573	Byte1048572	Yes	Yes

4.3 I/O-Interface Address Map

The following table shows the I/O Address map, including descriptions and their offset addresses relative to the ***"PCI Base Address1"***.

I/O Offset Address	32 bit Register				Software Readable	Software Writable
	31 24	23 16	15 8	7 0		
00h	Reserved				No	No
04h	Reserved				No	No
08h	Reserved		Interrupt & Timer Enable Register		Yes	Yes
0Ch	Reserved		I/O & Timer Interrupt Source Registers		Yes	No
10h	Reserved			Port BCD Mode	Yes	Yes
14h	Reserved			Port A Data	Yes	Yes
18h	Reserved			Port B Data	Yes	Yes
1Ch	Reserved			Port C Data	Yes	Yes
20h	Reserved			Port D Data	Yes	Yes
24h	Reserved			Port EFGH Mode	Yes	Yes
28h	Reserved			Port E Data	Yes	Yes
2Ch	Reserved			Port F Data	Yes	Yes
30h	Reserved			Port G Data	Yes	Yes
34h	Reserved			Port H Data	Yes	Yes
38h	Reserved			Port IJ Mode	Yes	Yes
3Ch	Reserved			Port I Data	Yes	Yes
40h	Reserved			Port J Data	Yes	Yes
44h	Reserved				No	No
48h	Reserved				No	No
4Ch	Reserved		TIMER-A Register		Yes	Yes
50h	Reserved		TIMER-B Register		Yes	Yes
54h	Reserved		TIMER-C Register		Yes	Yes
58h	Reserved		TIMER-D Register		Yes	Yes
5Ch	Reserved			Timer Resolution	Yes	Yes
60h	Port D de-bounce	Port C de-bounce	Port B de-bounce	Port A de-bounce	Yes	Yes
64h	Port H de-bounce	Port G de-bounce	Port F de-bounce	Port E de-bounce	Yes	Yes
68h	Reserved	Reserved	Port J de-bounce	Port I de-bounce	Yes	Yes

Interrupt & Timer Enable Register (08h & 09h)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
0	Port A Interrupt Enable bit. **'0'** = No support Interrupt from Port A as Input; **'1'** = Support Interrupt from Port A as Input	Yes	Yes	0
1	Port B Interrupt Enable bit. **'0'** = No support Interrupt from Port B as Input; **'1'** = Support Interrupt from Port B as Input	Yes	Yes	0
2	Port C Interrupt Enable bit. **'0'** = No support Interrupt from Port C as Input; **'1'** = Support Interrupt from Port C as Input	Yes	Yes	0
3	Port D Interrupt Enable bit. **'0'** = No support Interrupt from Port D as Input; **'1'** = Support Interrupt from Port D as Input	Yes	Yes	0
4	Port E Interrupt Enable bit. **'0'** = No support Interrupt from	Yes	Yes	0

	Port E as Input; **'1'** = Support Interrupt from Port E as Input			
5	Port F Interrupt Enable bit. **'0'** = No support Interrupt from Port F as Input; **'1'** = Support Interrupt from Port F as Input	Yes	Yes	0
6	Port G Interrupt Enable bit. **'0'** = No support Interrupt from Port G as Input; **'1'** = Support Interrupt from Port G as Input	Yes	Yes	0
7	Port H Interrupt Enable bit. **'0'** = No support Interrupt from Port H as Input; **'1'** = Support Interrupt from Port H as Input	Yes	Yes	0
8	Port I Interrupt Enable bit. **'0'** = No support Interrupt from Port I as Input; **'1'** = Support Interrupt from Port I as Input	Yes	Yes	0
9	Port J Interrupt Enable bit. **'0'** = No support Interrupt from Port J as Input; **'1'** = Support Interrupt from Port J as Input	Yes	Yes	0
10	Reserved	Yes	Yes	0
11	Reserved	Yes	Yes	0
12	Timer-A Enable bit. **'0'** = Timer-A disable; **'1'** = Timer-A Enable	Yes	Yes	0
13	Timer-B Enable bit. **'0'** = Timer-B disable; **'1'** = Timer-B Enable	Yes	Yes	0
14	Timer-C Enable bit. **'0'** = Timer-C disable; **'1'** = Timer-C Enable	Yes	Yes	0
15	Timer-D Enable bit. **'0'** = Timer-D disable; **'1'** = Timer-D Enable	Yes	Yes	0

Interrupt Source Register (0Ch & 0Dh)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
0	Interrupt Status in Port A. 0 = No Interrupt, 1 = Interrupt active. To clear this bit, must be wrote any data to Port A as Input	Yes	No	0
1	Interrupt Status in Port B. 0 = No Interrupt, 1 = Interrupt active. To clear this bit, must be wrote any data to Port B as Input	Yes	No	0
2	Interrupt Status in Port C. 0 = No Interrupt, 1 = Interrupt active. To clear this bit, must be wrote any data to Port C as Input	Yes	No	0
3	Interrupt Status in Port D. 0 = No Interrupt, 1 = Interrupt active. To clear this bit, must be wrote any data to Port D as Input	Yes	No	0
4	Interrupt Status in Port E. 0 = No Interrupt, 1 = Interrupt active. To clear this bit, must be wrote any data to Port E as Input	Yes	No	0
5	Interrupt Status in Port F. 0 = No Interrupt, 1 = Interrupt active. To clear this bit, must be wrote any data to Port F as Input	Yes	No	0
6	Interrupt Status in Port G. 0 = No Interrupt, 1 = Interrupt active. To clear this bit, must be wrote any data to Port G as Input	Yes	No	0
7	Interrupt Status in Port H. 0 = No Interrupt, 1 = Interrupt active. To clear this bit, must be wrote any data to Port H as Input	Yes	No	0
8	Interrupt Status in Port I. 0 = No Interrupt, 1 = Interrupt active. To clear this bit, must be wrote any data to Port I as Input	Yes	No	0
9	Interrupt Status in Port J. 0 = No Interrupt, 1 = Interrupt active. To clear this bit, must be wrote any data to Port J as Input	Yes	No	0
10	Reserved	Yes	No	0
11	Reserved	Yes	No	0
12	Timer-A Interrupt status. 0 = No Interrupt from Timer-A, 1 = Timer-A Interrupt activ. To clear this bit, must be wrote to Timer-A register	Yes	No	0
13	Timer-A Interrupt status. 0 = No Interrupt from Timer-B, 1 = Timer-B Interrupt activ. To clear this bit, must be wrote to Timer-B register	Yes	No	0
14	Timer-A Interrupt status. 0 = No Interrupt from Timer-C, 1 = Timer-C Interrupt activ. To clear this bit, must be wrote to Timer-C register	Yes	No	0
15	Timer-A Interrupt status. 0 = No Interrupt from Timer-D, 1 = Timer-D Interrupt activ. To clear this bit, must be wrote to Timer-D register	Yes	No	0

Port BCD Mode (10h)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
0	Port A (8 bit). 0 = Input Mode, Output Mode disable	Yes	No	0
1	Port B (8 bit). 0 = Input Mode, 1 = Output Mode	Yes	Yes	0
2	Port C (8 bit). 0 = Input Mode, 1 = Output Mode	Yes	Yes	0
3	Port D (8 bit). 0 = Input Mode, 1 = Output Mode	Yes	Yes	0
7 : 4	Reserved	Yes	No	0

Port A Data (14h)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
0	Bit 1 of Port A	Yes	Only to clear Interrupt	0 / 1
1	Bit 2 of Port A	Yes	Only to clear Interrupt	0 / 1
2	Bit 3 of Port A	Yes	Only to clear Interrupt	0 / 1
3	Bit 4 of Port A	Yes	Only to clear Interrupt	0 / 1
4	Bit 5 of Port A	Yes	Only to clear Interrupt	0 / 1
5	Bit 6 of Port A	Yes	Only to clear Interrupt	0 / 1
6	Bit 7 of Port A	Yes	Only to clear Interrupt	0 / 1
7	Bit 8 of Port A	Yes	Only to clear Interrupt	0 / 1

Port B Data (18h)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
0	Bit 1 of Port B	Yes	Yes (only in Output Mode)	0 / 1
1	Bit 2 of Port B	Yes	Yes (only in Output Mode)	0 / 1
2	Bit 3 of Port B	Yes	Yes (only in Output Mode)	0 / 1
3	Bit 4 of Port B	Yes	Yes (only in Output Mode)	0 / 1
4	Bit 5 of Port B	Yes	Yes (only in Output Mode)	0 / 1
5	Bit 6 of Port B	Yes	Yes (only in Output Mode)	0 / 1
6	Bit 7 of Port B	Yes	Yes (only in Output Mode)	0 / 1
7	Bit 8 of Port B	Yes	Yes (only in Output Mode)	0 / 1

Port C Data (1Ch)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
0	Bit 1 of Port C	Yes	Yes (only in Output Mode)	0 / 1
1	Bit 2 of Port C	Yes	Yes (only in Output Mode)	0 / 1
2	Bit 3 of Port C	Yes	Yes (only in	0 / 1

			Output Mode)	
3	Bit 4 of Port C	Yes	Yes (only in Output Mode)	0 / 1
4	Bit 5 of Port C	Yes	Yes (only in Output Mode)	0 / 1
5	Bit 6 of Port C	Yes	Yes (only in Output Mode)	0 / 1
6	Bit 7 of Port C	Yes	Yes (only in Output Mode)	0 / 1
7	Bit 8 of Port C	Yes	Yes (only in Output Mode)	0 / 1

Port D Data (20h)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
0	Bit 1 of Port D	Yes	Yes (only in Output Mode)	0 / 1
1	Bit 2 of Port D	Yes	Yes (only in Output Mode)	0 / 1
2	Bit 3 of Port D	Yes	Yes (only in Output Mode)	0 / 1
3	Bit 4 of Port D	Yes	Yes (only in Output Mode)	0 / 1
4	Bit 5 of Port D	Yes	Yes (only in Output Mode)	0 / 1
5	Bit 6 of Port D	Yes	Yes (only in Output Mode)	0 / 1
6	Bit 7 of Port D	Yes	Yes (only in Output Mode)	0 / 1
7	Bit 8 of Port D	Yes	Yes (only in Output Mode)	0 / 1

Port EFGH Mode (24h)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
0	Port E (8 bit). 0 = Input Mode, 1 = Output Mode	Yes	Yes	0
1	Port F (8 bit). 0 = Input Mode, 1 = Output Mode	Yes	Yes	0
2	Port G (8 bit). 0 = Input Mode, 1 = Output Mode	Yes	Yes	0
3	Port H (8 bit). 0 = Input Mode, 1 = Output Mode	Yes	Yes	0
7 : 3	Reserved	Yes	No	0

Port E Data (28h)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
0	Bit 1 of Port E	Yes	Yes (only in Output Mode)	0 / 1
1	Bit 2 of Port E	Yes	Yes (only in Output Mode)	0 / 1
2	Bit 3 of Port E	Yes	Yes (only in Output Mode)	0 / 1
3	Bit 4 of Port E	Yes	Yes (only in Output Mode)	0 / 1
4	Bit 5 of Port E	Yes	Yes (only in Output Mode)	0 / 1
5	Bit 6 of Port E	Yes	Yes (only in Output Mode)	0 / 1
6	Bit 7 of Port E	Yes	Yes (only in Output Mode)	0 / 1

7	Bit 8 of Port E	Yes	Yes (only in Output Mode)	0 / 1

Port F Data (2Ch)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
0	Bit 1 of Port F	Yes	Yes (only in Output Mode)	0 / 1
1	Bit 2 of Port F	Yes	Yes (only in Output Mode)	0 / 1
2	Bit 3 of Port F	Yes	Yes (only in Output Mode)	0 / 1
3	Bit 4 of Port F	Yes	Yes (only in Output Mode)	0 / 1
4	Bit 5 of Port F	Yes	Yes (only in Output Mode)	0 / 1
5	Bit 6 of Port F	Yes	Yes (only in Output Mode)	0 / 1
6	Bit 7 of Port F	Yes	Yes (only in Output Mode)	0 / 1
7	Bit 8 of Port F	Yes	Yes (only in Output Mode)	0 / 1

Port G Data (30h)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
0	Bit 1 of Port G	Yes	Yes (only in Output Mode)	0 / 1
1	Bit 2 of Port G	Yes	Yes (only in Output Mode)	0 / 1
2	Bit 3 of Port G	Yes	Yes (only in Output Mode)	0 / 1
3	Bit 4 of Port G	Yes	Yes (only in Output Mode)	0 / 1
4	Bit 5 of Port G	Yes	Yes (only in Output Mode)	0 / 1
5	Bit 6 of Port G	Yes	Yes (only in Output Mode)	0 / 1
6	Bit 7 of Port G	Yes	Yes (only in Output Mode)	0 / 1
7	Bit 8 of Port G	Yes	Yes (only in Output Mode)	0 / 1

Port H Data (34h)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
0	Bit 1 of Port H	Yes	Yes (only in Output Mode)	0 / 1
1	Bit 2 of Port H	Yes	Yes (only in Output Mode)	0 / 1
2	Bit 3 of Port H	Yes	Yes (only in Output Mode)	0 / 1
3	Bit 4 of Port H	Yes	Yes (only in Output Mode)	0 / 1
4	Bit 5 of Port H	Yes	Yes (only in Output Mode)	0 / 1
5	Bit 6 of Port H	Yes	Yes (only in Output Mode)	0 / 1

6	Bit 7 of Port H	Yes	Yes (only in Output Mode)	0 / 1
7	Bit 8 of Port H	Yes	Yes (only in Output Mode)	0 / 1

Port IJ Mode (38h)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
0	Port I (8 bit). 0 = Input Mode, 1 = Output Mode	Yes	Yes	0
1	Port J (8 bit). 0 = Input Mode, 1 = Output Mode	Yes	Yes	0
7 : 2	Reserved	Yes	No	0

Port I Data (3Ch)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
0	Bit 1 of Port I	Yes	Yes (only in Output Mode)	0 / 1
1	Bit 2 of Port I	Yes	Yes (only in Output Mode)	0 / 1
2	Bit 3 of Port I	Yes	Yes (only in Output Mode)	0 / 1
3	Bit 4 of Port I	Yes	Yes (only in Output Mode)	0 / 1
4	Bit 5 of Port I	Yes	Yes (only in Output Mode)	0 / 1
5	Bit 6 of Port I	Yes	Yes (only in Output Mode)	0 / 1
6	Bit 7 of Port I	Yes	Yes (only in Output Mode)	0 / 1
7	Bit 8 of Port I	Yes	Yes (only in Output Mode)	0 / 1

Port J Data (40h)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
0	Bit 1 of Port J	Yes	Yes (only in Output Mode)	0 / 1
1	Bit 2 of Port J	Yes	Yes (only in Output Mode)	0 / 1
2	Bit 3 of Port J	Yes	Yes (only in Output Mode)	0 / 1
3	Bit 4 of Port J	Yes	Yes (only in Output Mode)	0 / 1
4	Bit 5 of Port J	Yes	Yes (only in Output Mode)	0 / 1
5	Bit 6 of Port J	Yes	Yes (only in Output Mode)	0 / 1
6	Bit 7 of Port J	Yes	Yes (only in Output Mode)	0 / 1
7	Bit 8 of Port J	Yes	Yes (only in Output Mode)	0 / 1

Timer-A Register (4Ch & 4Dh)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
0 - 15	16 bit Timer-A up to **65536 sec/ms/us**. If this register is written, the Timer-A will count down and if **"0"** state is reached, it will generate an interrupt.	Yes	Yes, only if Timer-A is enabled	0

Timer-B Register (50h & 51h)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
0 - 15	16 bits Timer-B up to **1 to 65535 mS**. If this register is written, the Timer-B will count down and if **"0"** state is reached, it will generate an interrupt.	Yes	Yes, only if Timer-B is enabled	0

Timer-C Register (54h & 55h)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
0 - 15	16 bits Timer-C up to **1 to 65535 mS**. If this register is written, the Timer-C will count down and if "0" state is reached, it will generate an interrupt.	Yes	Yes, only if Timer-C is enabled	0

Timer-D Register (58h & 59h)

Bit Field	Description	Software Readable	Software Writable	Value after Reset
0 - 15	16 bits Timer-D up to **1 to 65535 mS**. If this register is written, the Timer-D will count down and if "0" state is reached, it will generate an interrupt.	Yes	Yes, only if Timer-D is enabled	0

Timer Resolution Register (5Ch)

Default set of the register value to be 55H (ms resolution) for using timer-A ~timer-D.
Note* The resolutions for second & microsecond are reserved for further use.

De-bounce Time Register (60h ~6Ah)

Setting de-bounce time for each I/O port. De-bounce range from 1~256 ms. The value 00 means the de-bounce time is 1ms. Defaul setting is 10.

5 ELECTRICAL CHARACTERISTICS

5.1 Basic Electrical Characteristics Table

Electrical Characteristics					
Symbol	Parameter / Condition	Value			Unit
		Min.	Typ.	Max.	
Vth I.IH	Isolation input voltage high level threshold	3.6	12	36	V
Vth I.IL	Isolation input voltage low level threshold			0.8	V
Vout O.D	Open drain output voltage			12	V
Isink[1] O.D	Open drain sink current	-	-	500	mA
Isink[2] O.D	Open drain sink current (Tower Lamp)	-	-	1.0	A
+12V	+12V power input	11.4	12	12.6	V
+5V	+5V power input	4.85	5	5.25	V
ccTalk	Communication pin high threshold threshold	3.0	5.0	5.5	V
ccTalk	Communication pin low level Threshold	-0.3		0.8	V
RS232	Maximum Working baud rate			115.2	Kbps
AGA	Maximum Working baud rate		19.2		Kbps
T.P.C	Total power consumption in ACE-B8700 without External device		16		W

5.2 72 Pins Golden Finger

Component Side				Solder Side		
I/O TYPE	**Port/Bit**	**Function**	**Pin**	**Function**	**Port/Bit**	**I/O TYPE**
			1			
A.O		SPEAKER RIGHT+	2	Audio GND		
A.O		SPEAKER LEFT +	3	Audio GND		
I.I	B0	Button 1	4	Audio GND		
I.I	B1	Button 2	5	SPEAKER RIGHT+		A.O
I.I	B2	Button 3	6	Door SW2	A1	I
I.I	B3	Button 4	7	Door SW3	A2	I
I.I	B4	Button 5	8	Door SW4	A3	I
I.I	B5	Button 6	9	Door SW5	A4	I
I.I	B6	Button 7	10	Touch-Cal Key-Lock	D3	I.I
I.I	B7	Button 8	11	Spare Key-Lock	D4	I.I
I.I	C0	Button 9	12	Coin-En	I0	O.D
I.I	C1	Button10	13	Bill-En	I1	O.D
			14			
I.I	D0	Dissolve Key-Lock	15	Button 15	C6	I.I
I.I	C2	Button11	16	Button 16	C7	I.I
I	A0	Door SW1	17			
I.I	E0	Coin-In Signal A	18	Button 12	C3	I.I
I.I	E2	Bill-In	19	Coin-In Signal B	E1	I.I
I.I	D1	OM Key-Lock	20	Setup Key-Lock (Hand Pay)	D2	I.I
I.I	C5	Button 14	21	Button 13	C4	I.I
		GND	22	Hopper Sensor	E3	I.I
O.D	H7	Spare Meter1	23	Lamp13	G4	O.D
O.D	H0	Key-In Meter	24	Hand-Pay Meter1	H5	O.D
O.D	H1	Bill-In Meter	25	Hand-Pay Meter2	H6	O.D
O.D	H2	Coin-In Meter	26	Lamp14	G5	O.D
O.D	H3	Pay-Out Meter	27	Lamp15	G6	O.D
O.D	H4	Key-Out Meter	28	Lamp16	G7	O.D
O.D	F0	Lamp1	29	Lamp7	F6	O.D
O.D	F1	Lamp2	30	Lamp8	F7	O.D
O.D	F2	Lamp3	31	Lamp9	G0	O.D
O.D	F3	Lamp4	32	Lamp10	G1	O.D
O.D	F4	Lamp5	33	Lamp11	G2	O.D
O.D	F5	Tower Lamp6	34	Tower Lamp12	G3	O.D
		GND	35	GND		
		GND	36	GND		

5.3 20 Pins Golden Finger

Component Side				Solder Side		
I/O TYPE	**Port/Bit**	**Function**	**Pin**	**Function**	**Port/Bit**	**I/O TYPE**
		GND	1	GND		
		GND	2	GND		
		+5V	3	+5V		
		+5V	4	+5V		
		+12V	5	+12V		
		+12V	6	+12V		
O.D	I2	Hopper SSR	7			
			8			
		GND	9	GND		
		GND	10	GND		

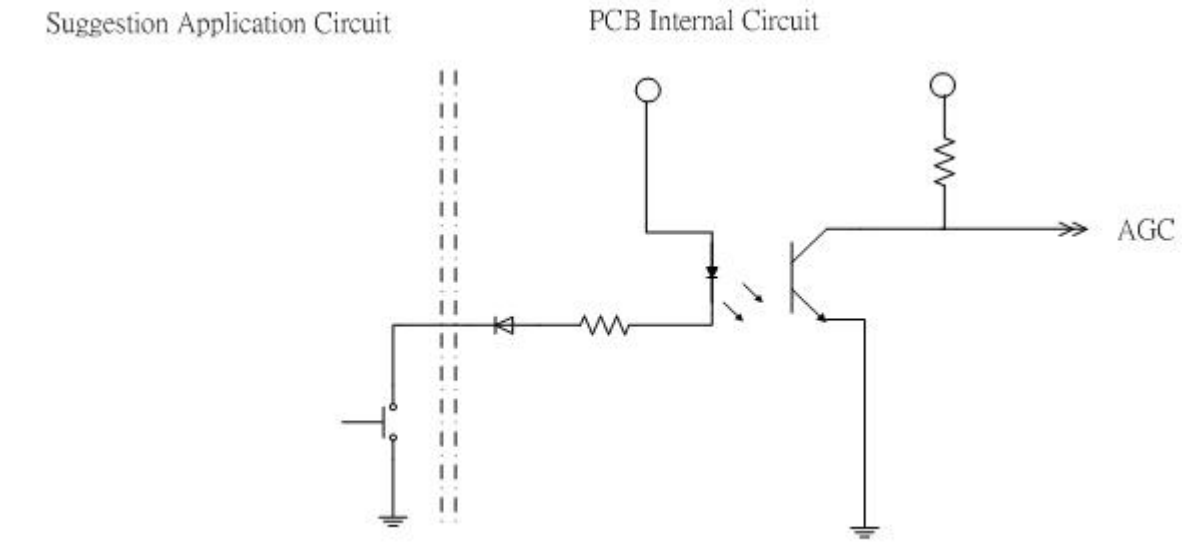
5.4 AGC Port Assignment

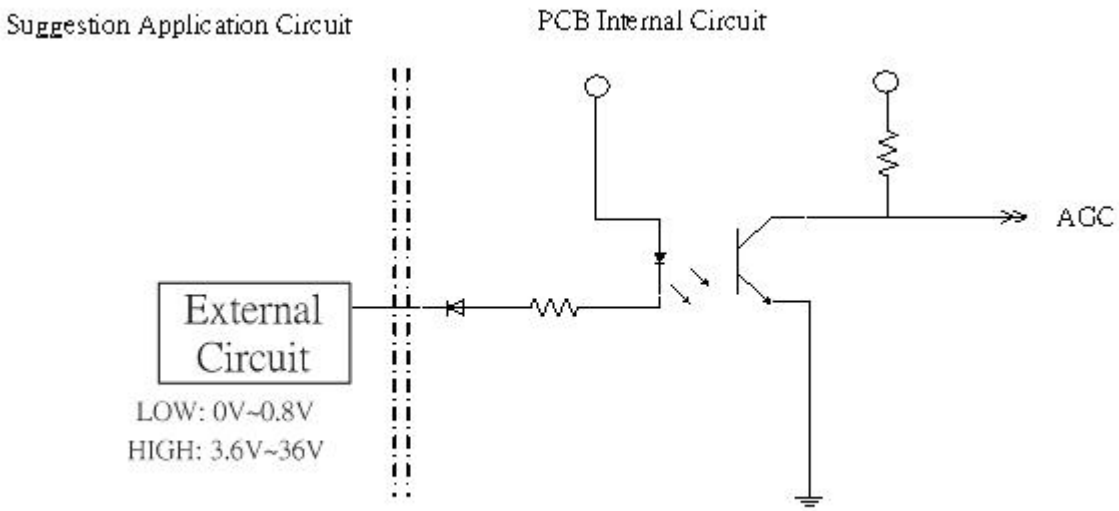
Port/Bit	I/O	72 Pins	Remark
A0	I	Door SW1	AGA intrusion bit 0
A1	I	Door SW2	AGA intrusion bit 1
A2	I	Door SW3	AGA intrusion bit 2
A3	I	Door SW4	AGA intrusion bit 3
A4	I	Door SW5	AGA intrusion bit 4
A5	I		Power on/off AGA intrusion bit 5
A6	I		Chassis Switch AGA intrusion bit 6
A7			
B0	I.I	Button 1	
B1	I.I	Button 2	
B2	I.I	Button 3	
B3	I.I	Button 4	
B4	I.I	Button 5	
B5	I.I	Button 6	
B6	I.I	Button 7	
B7	I.I	Button 8	
C0	I.I	Button 9	
C1	I.I	Button 10	
C2	I.I	Button 11	
C3	I.I	Button 12	
C4	I.I	Button 13	
C5	I.I	Button 14	
C6	I.I	Button 15	
C7	I.I	Button 16	
D0	I.I	Dissolve Key-Lock	
D1	I.I	OM Key-Lock	
D2	I.I	Setup Key-Lock(Hand Pay)	
D3	I.I	Touch-Cal Key-Lock	
D4	I.I	Spare Key-Lock	
D5			
D6			
D7			
E0	I.I	Coin-In Signal A	
E1	I.I	Coin-In Signal B	
E2	I.I	Bill-In	
E3	I.I	Hopper Sensor	
E4			
E5			
E6	I.I	Coin enable feedback	
E7	I.I	Bill enable feedback	
F0	O.D	Lamp1	
F1	O.D	Lamp2	
F2	O.D	Lamp3	
F3	O.D	Lamp4	
F4	O.D	Lamp5	
F5	O.D	Lamp6	
F6	O.D	Lamp7	
F7	O.D	Lamp8	
G0	O.D	Lamp9	
G1	O.D	Lamp10	
G2	O.D	Lamp11	

G3	O.D	Lamp12	
G4	O.D	Lamp13	
G5	O.D	Lamp14	
G6	O.D	Lamp15	
G7	O.D	Lamp16	
H0	O.D	Key-In Meter	
H1	O.D	Bill-In Meter	
H2	O.D	Coin-In Meter	
H3	O.D	Pay-Out Meter	
H4	O.D	Key-Out Meter	
H5	O.D	Hand-Pay Meter1	
H6	O.D	Hand-Pay Meter2	
H7	O.D	Spare Meter1	
I0	O.D	Coin-En	
I1	O.D	Bill-En	
I2	O.D	Hopper SSR	
I3			
I4			
I5			
I6			
I7			
J0	I		DIP Switch Bit 0
J1	I		DIP Switch Bit 1
J2	I		DIP Switch Bit 2
J3	I		DIP Switch Bit 3
J4	I		DIP Switch Bit 4
J5	I		DIP Switch Bit 5
J6	I		DIP Switch Bit 6
J7	I		DIP Switch Bit 7

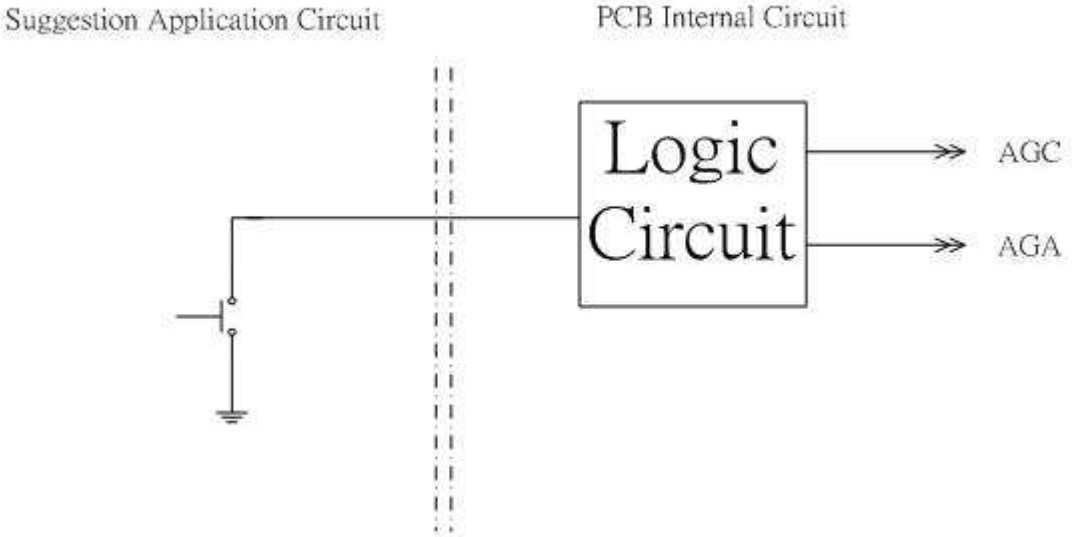
Notes

1. I.I (Isolated-Input) external connection application note.

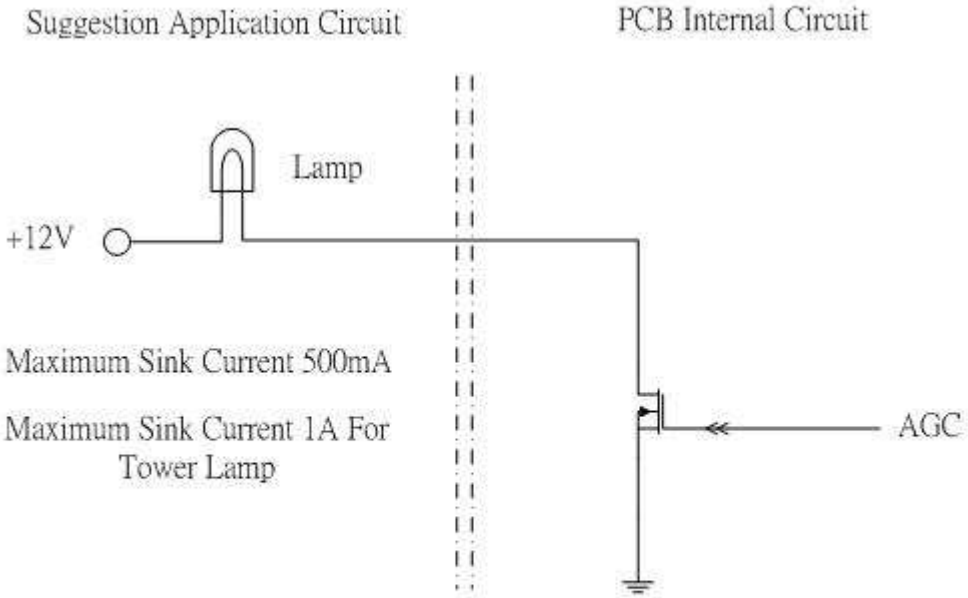




2. I (TTL Input) external connection application note.



3. O.D (Open-Drain) output external connection application note.



4. A.O (Audio Output) is maximum 12V peak for 8Ω speaker.

   Please don not short the R- and L- together.

5. Notice for Rechargeable battery

Please charge the battery 24hrs firstly before using.

- Watch Dog Timer Reset Sample Code (Fintek F81216AD)

```
#include <conio.h>
#include <stdlib.h>
#include <stdio.h>
#include <dos.h>

int main(int argc, char *argv[])
{
    unsigned char Time;
    int Temp;


    if ( argc != 2 )
       {   Show_Help();     return 1;        }

    clrscr();

    Time=atoi(argv[1]);

    // Set Watchdog
    outportb(0x300 , 0x03); //
    outportb(0x301 , Time); //
    outportb(0x301 , Time); //


    cprintf("If you can see this message, Reset system is Fail",Time);

    return 1;
}
```