NCP1271ADAPGEVB

19 V, 3.0 A Universal Input AC-DC Adaptor Using NCP1271 Evaluation Board User's Manual

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EVAL BOARD USER'S MANUAL

Introduction

The NCP1271 is one of the latest fixed−frequency current−mode PWM switching controllers with (1) adjustable Soft−Skip™ standby operation for low−level audible noise, (2) integrated high−voltage startup for saving standby power, (3) timer based overload fault detection, and (4) internal latch protection features. Table 1 summarizes all the features of an NCP1271 based power supply.

This evaluation board user's manual presents an example circuit (Figure 2) using the NCP1271 (65 kHz version) in a flyback topology. The design steps and subsequent measurements are also included. An Excel based design worksheet is available at www.onsemi.com.

The measurements show that the 19 V, 3.0 A circuit delivers above 85% across a universal input (85 to 265 Vac). The no load standby consumption is 83 mW at 230 Vac and the light load operation is greater than 75% efficient.

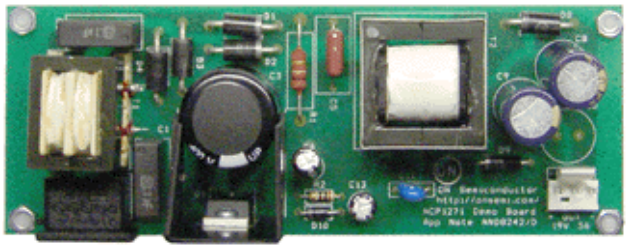

Figure 1. Evaluation Board Photo

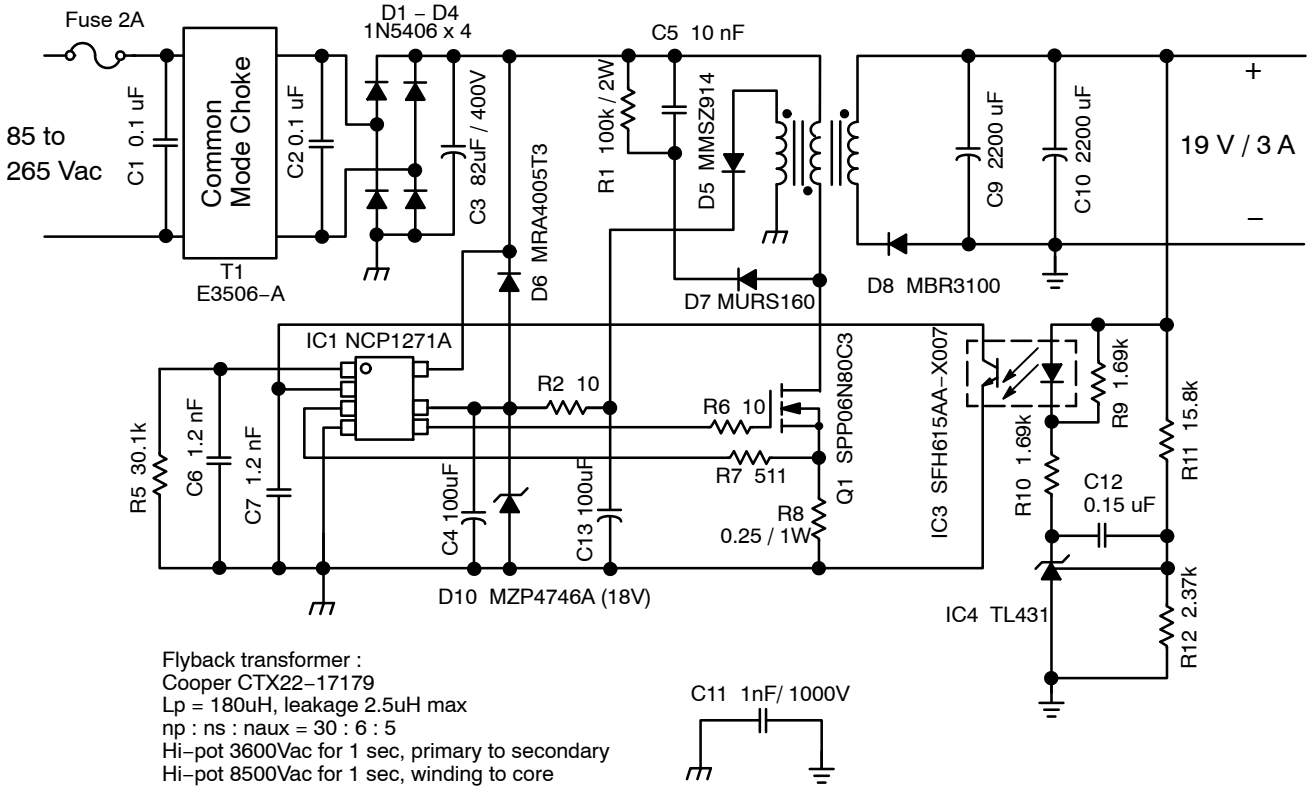

Figure 2. Evaluation Board Schematic

Table 1. FEATURES OF POWER SUPPLY USING NCP1271

	Operation Mode	Features
Topology	CCM/DCM Flyback	• Fixed−frequency current−mode control with inherent primary current limitation. • Frequency jittering to soften the EMI signature. • Built−in soft−start. • Output short−circuit fault detection independent of the auxiliary winding. • Integrated high voltage startup that minimizes standby power loss.
Standby Condition	Soft−Skip Operation	• Adjustable skip level for optimal standby power consumption. • Proprietary Soft−Skip to reduce the risk of low−frequency audible noise. • Soft−Skip operation is automatically disabled if an abrupt transient load is applied from standby operation. This improves the output response to a transient load.
Fault Condition	Double Hiccup Restart	• Double Hiccup operation minimizes the power dissipation in a fault mode and allows the application to auto−recover when the fault is removed.
Latch Protection Activated	Latch Off	• An internal latch makes it easy to add overtemperature protection (OTP) or overvoltage protection (OVP) to any applications. • Latch is reset by unplugging the AC input and allowing V_{CC} to drop below 4 V (typ).

THE EVALUATION BOARD SPECIFICATION

Input	85 to 265 Vac, 50 Hz
Output	19 Vdc, 3.0 A, Isolated
Features	• < 100 mW Input Power at 230 Vac • Excellent Light Load Performance • No Audible Noise • > 85% Full Load Efficiency • Short Circuit Protection Activates at < 100W for Any Input Voltage

A Discontinuous Conduction Mode (DCM) flyback was selected for this application. DCM gives very good stability, small inductor size (lower leakage inductance), and good transient response.

Flyback Calculations

Several resources are available at www.onsemi.com to calculate the necessary component values for a flyback supply. In particular, an Excel based design spreadsheet can be found at:

www.onsemi.com/collateral/NCP1271SHEET.xls

Additionally, most of the other NCP12xx application notes also apply to the NCP1271. For detailed information on designing a flyback power supply, please visit AND8076/D. Other app notes which may also aid in the design include:

AND8069/D	Tips and Tricks to Build Efficient Circuits With the NCP1200
AND8205/D	How to Choose a Switching Controller for Design
AND8023/D	Implementing the NCP1200 in Low−Cost AC/DC Converters
AND8032/D	Conducted EMI Filter Design for the NCP1200
AND8076/D	A 70 W Low Standby Power Supply with the NCP12xx Series

Based on the results from the NCP1271 design spreadsheet, the final values for this adapter's key flyback parameters were calculated to be:

Np:Ns = 5:1
Lp = 180 μH
R_{CS} = 0.3 Ω
Ipeak(full load) = 3.5 A
Switch Rating = 6 A, 800 V
Diode Rating = 3 A, 100 V
Rsnubber = 100 kΩ
Csnubber = 10 nF

Setting the Short Circuit Protection Level

The current sense resistor (R_{CS} or R8), provides two functions. First it senses the primary current for current−mode PWM operation. Secondly, it provides the maximum primary current limitation according to equation 1:

$$I_{p(max)} = \frac{1\ V}{R_{CS}} \qquad \text{(eq. 1)}$$

The short circuit protection activates when the $I_{p(max)}$ current is reached for more than 130 ms (typ). This also corresponds to V_{FB} being greater than or equal to 3 V for 130 ms. Therefore, R_{CS} must be set large enough to ensure that the required peak current can always be delivered, but small enough to meet the short circuit protection requirements. A DCM flyback converter has the following relationship:

$$P_{out} = 1/2 \times L_p \times I_p^2 \times F_{SW} \times \eta \qquad \text{(eq. 2)}$$

Therefore, for an assumed efficiency of 80%, a peak current of 4 A should trigger the short circuit protection circuitry at 80 W. This corresponds to an R_{CS} value of 0.25 Ω. This change in R_{CS} may also require that the snubber and transformer be re−calculated to handle this level of peak current during the short circuit fault time. A few iterations of the Excel based NCP1271 design spreadsheet should produce a good starting point for the application's design.

Over Power Compensation

For this evaluation board, the short circuit protection is activated with an output load of 76 W at 85 Vac and 93 W at 265 Vac. The variation in short circuit power level with input voltage is due to the propagation delay (Tprop) of the NCP1271. This propagation delay has a more pronounced effect on the power delivered at high line than at low line as shown in Figure 3.

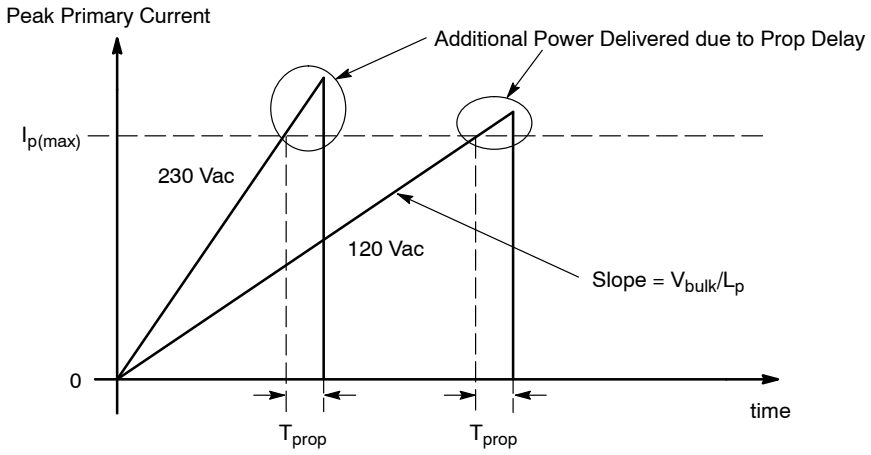

Figure 3. Effect of Propagation Delay on the Maximum Power Delivered at High Line and Low Line

This effect is called “Over Power” because it delivers more power than what is requested by the feedback loop. Specifically, for a DCM flyback system, the total power delivered to the output including the prop delay effect is:

$$P_{out} = \frac{1}{2} \cdot L_p \cdot (I_{p(max)} + V_{bulk}/L_p \cdot T_{prop})^2 \cdot F_{sw} \cdot \eta \quad \text{(eq. 3)}$$

The NCP1271 has been designed with a very low Tprop (50 ns typ). This minimizes the over power effect. However, if reduced variation is required, then over power compensation can be easily implemented by using one of the circuits shown in Figures 4 and 5.

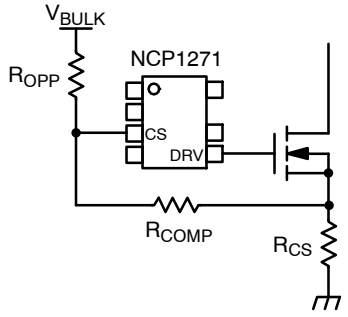

Figure 4. Over Power Compensation by means of a Resistor to the Bulk Voltage

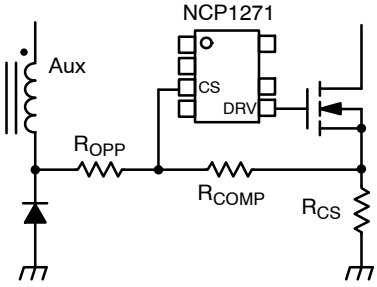

Figure 5. Over Power Compensation by Modifying the Auxiliary Winding Topology

The circuit in Figure 4 simply modifies the CS setpoint proportional to the HV bulk level. This creates an offset which compensates for the propagation delay. However, this does increase the standby power dissipation. Figure 5 gives another option which results in much lower power dissipation. By altering the position of the Aux winding diode, a new point is created whose voltage is proportional to Vin. The power dissipation is now reduced by a factor of $(Np:Naux)^2$. Values for Ropp are best found experimentally to give suitable precision for the activation of the short circuit protection.

Biasing the Controller

The NCP1271 includes a high voltage (HV) startup pin (Pin 8) which charges V_{CC} to its operating level. This pin can be directly connected to the high voltage DC bus. Once the device is powered up, an auxiliary winding powers V_{CC} as shown in Figure 6.

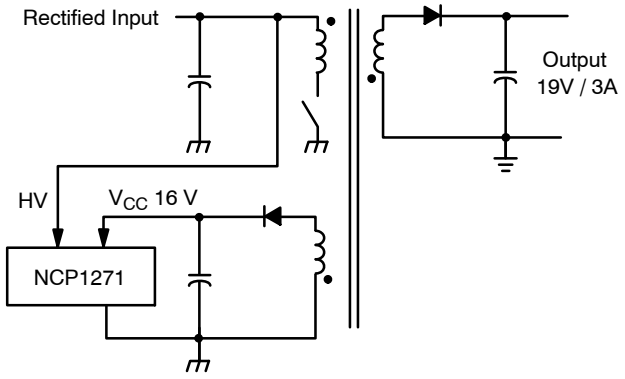

Figure 6. V_{CC} Biasing Scheme

The range of V_{CC} is from 10 V (min) to 20 V (max). Therefore, the auxiliary winding should be designed to give a level of V_{CC} within this range over all output loads. When the circuit is in standby mode, very few pulses are delivered and the auxiliary level decreases. To provide enough voltage range, a nominal V_{CC} level of 16 V was selected for this application. Additionally, an 18 V (±5%) Zener diode was added externally to protect the controller from abnormally high auxiliary levels. The 16 V bias supply is constructed from a 6:5 turns ratio (19 V:16 V) between the main output and the auxiliary winding.

Figure 7 shows the auxiliary supply circuit. A resistor is included to provide the flexibility to redesign the circuit for higher output voltages. Any extra bias voltage greater than 18 V is simply dissipated across the resistor.

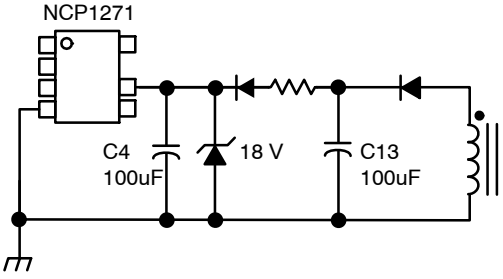

Figure 7. Auxiliary Supply

Soft−Skip Adjustment

When the load current drops, the compensation network responds by reducing the peak current. When the peak current reaches the skip peak current level, the NCP1271 enters skip operation to reduce the power consumption. The peak current level at which skip is entered should be set high for good standby power dissipation. However, it also needs to be set low enough that no audible noise occurs during each bunch of skip pulses. To address this need, the NCP1271 has a proprietary Soft−Skip feature which ramps each bunch of pulses. This dramatically lowers acoustic noise and allows a higher skip level to be set for greater power savings. The NCP1271 also allows the designer to select the optimal level of the peak current during skip through a simple resistor from pin 1 to GND. This skip resistor sets the skip level according to equation 4:

$$V_{skip} = I_{skip} \times R_{skip} \quad \text{(eq. 4)}$$

where I_{skip} = 43 μA (typ)

The peak current when skip mode is activated can be calculated with equation 5:

$$I_{peak(skip)} = \frac{V_{skip}}{3\ V} \times I_{peak(max)} \quad \text{(eq. 5)}$$

For this evaluation board, V_{skip} was set to 1.3 V (R_{skip} = 30.1 kΩ). And $I_{peak(max)}$ is 1 V / 0.25 Ω = 4 A. Therefore, $I_{peak(skip)}$ = 1.7 A.

Minimum On Time Limitation

The NCP1271 includes a current sense (CS) Leading Edge Blanking (LEB) filter. The LEB filter blanks out the first 180 ns (typ) of the CS voltage at the beginning of each drive pulse. This helps to prevent a premature reset of the output due to noise. However, this also results in a minimum on time of the device. The duration is equal to the LEB time (180 ns typical) and the propagation delay of logic (50 ns typical). If the application circuit is configured for 0% skip (by connecting Pin 1 to Ground), then that minimum on time duration may result in an abnormally high output voltage during no load conditions. Therefore, it is recommended to set skip to some small value rather than disable it completely.

Ramp Compensation

The NCP1271 also incorporates a feature called “ramp compensation.” Ramp compensation is a known mean to cure subharmonic oscillations. These oscillations take place at half the switching frequency and occur only during continuous conduction mode (CCM) with a duty−cycle greater than 50%. To prevent these oscillations, one usually injects between 50 and 75% of the inductor down slope into the CS pin. The NCP1271 generates an internal current ramp that is synchronized with the clock. This current ramp is then routed to the CS pin.

Since the flyback design in this app note is well within DCM operation, ramp compensation is not necessary. However, for designs that do run in CCM with the NCP1271, ramp compensation is easy to implement. It only requires one external resistor between Rcs and the CS pin. The value of the ramp resistor to obtain 50% inductor down slope injection can be calculated with the following equation:

$$R_{ramp} = 0.50 \times R_{CS} \times \frac{\left((V_{out} + V_f) \times \frac{N_P}{N_S}\right)}{\left(L_p \times F_{sw} \times \frac{100\ \mu A}{0.80}\right)} \quad \text{(eq. 6)}$$

Maximum Duty Cycle and Ramp Compensation

If the ramp resistor is set too high, the maximum duty cycle will be reduced. But as a long as R_{ramp} is below 10 kΩ, this will not be a problem. A typical graph of the maximum duty cycle verses R_{ramp} is shown in Figure 8. However, it is not recommended to try to reduce the maximum duty cycle by the R_{ramp} value because this relationship is not guaranteed by the production tests of the device.

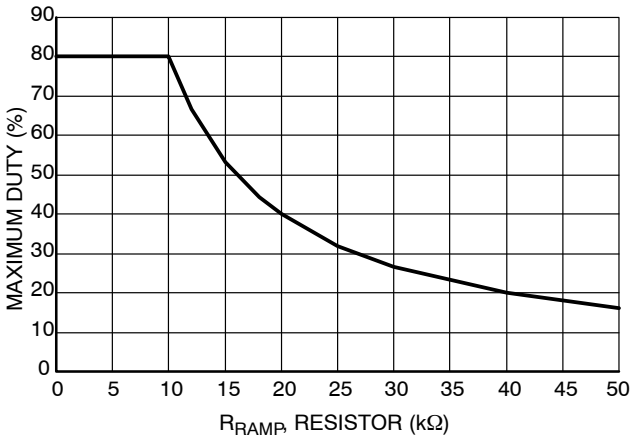

Figure 8. Maximum Duty Cycle Characteristics

Optional Output OVP Latch

The NCP1271 includes a feature where if Pin 1 is brought above 8.0 V (typ), the part will safely latch off the controller. The controller is reset by unplugging the AC input. This allows for easy implementation of overvoltage (OVP) or overtemperature (OTP) protection.

In order to pull the Pin 1 voltage above the latch threshold, a greater than 8.0 V source is needed. That is usually the bias supply voltage V_{CC}. Therefore, to protect Pin 1, a resistor (R_{limit}) is connected to limit the current below the maximum allowed level. In addition, the internal ESD diode will limit the maximum voltage on Pin 1 to about 10 V.

This latch off feature can be configured in a variety of ways. Some of the most popular include using the auxiliary winding to detect an overvoltage and using an NTC resistor to detect an overtemperature condition. A few variations of these circuits are listed in Figures 9 to 12.

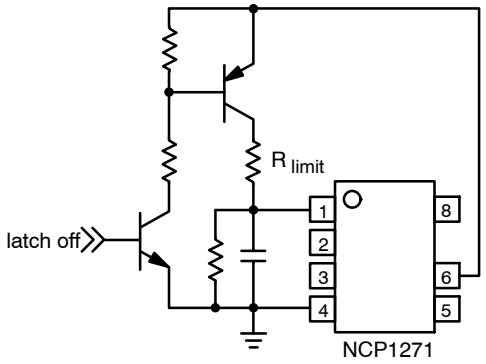

Figure 9. Simple Latchoff Circuit by Bipolar Transistors

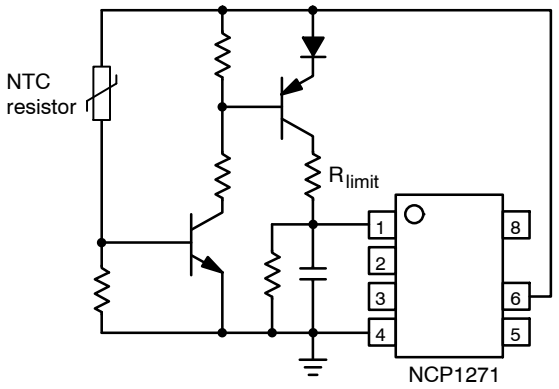

Figure 10. Overtemperature Protection Latch with a NTC Thermistor

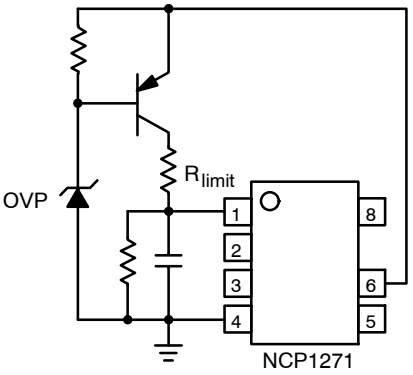

Figure 11. Output Overvoltage Protection Using the Auxiliary Winding

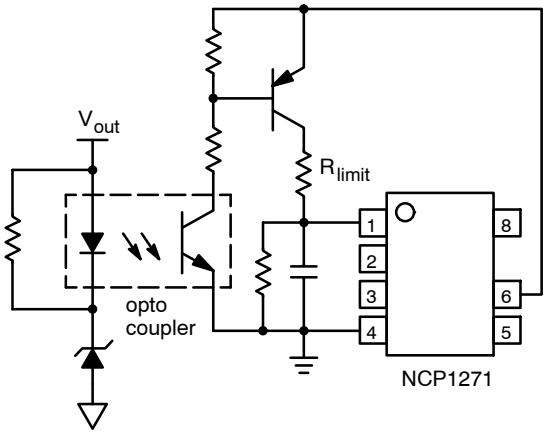

Figure 12. Output Overvoltage Protection Using an Optocoupler

It is important to note that when Pin 1 is open it sets the default skip level to 1.2 V. However, in this mode, pin 1 is internally pulled high to the Vskip−reset level (6.5 V typ). This only leaves about 1.5 V of noise margin before the part latches off. Therefore, if a skip level of 1.2 V is desired, then instead of leaving pin 1 open, it is always recommended to place a 28 kΩ resistor from pin 1 to GND. Then the skip level becomes 1.2 V (28 kΩ x 43 μA = 1.2 V), and the pin 1 voltage is also 1.2 V. This gives much better noise immunity and reduces the chance of falsely triggering the latch due to noise or leakage current from the external latch circuitry. Additionally, a small capacitor should be added to pin 1 to further increase the noise immunity.

HV Pin Protection Circuit

When the main power is interrupted in the application, the high voltage DC bus may potentially go negative in a short transient period. Since this is directly connected to pin 8, it could create a reverse current out of the HV Pin and could potentially damage the device. There are two easy solutions to this problem. The first is demonstrated in Figure 13. The inserted diode turns on when the HV Pin voltage goes below the V_{CC} biasing voltage. This eliminates the chance of negative voltage on the HV pin. A second method is shown in Figure 14. Here, the inserted resistor limits the negative current to a low level and protects the HV pin. Either option works well, but for this evaluation board, a diode between V_{CC} and HV was used.

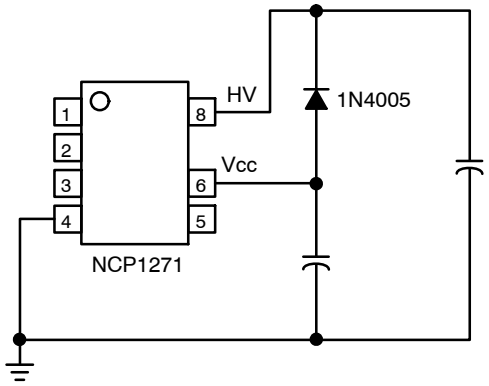

Figure 13. Protection Diode for HV Pin

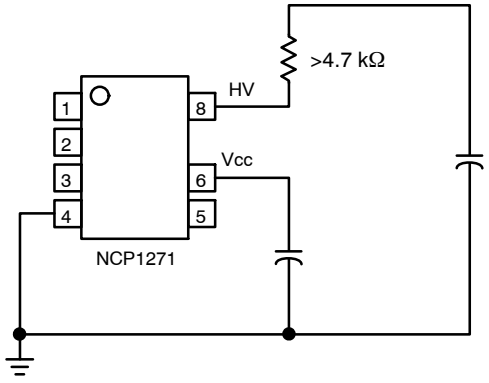

Figure 14. Protection Resistor on HV Pin

Layout Consideration

Figures 9−10 show the layout of the design. It is a single−layer PCB. As with any power converter, some care must be exercised with the design and layout. The following are some important guidelines.

1. Minimize the high−current loop and locate the IC controller outside the high−current loop to prevent malfunctioning of the IC internal logic due to strong magnetic fields from the high current.
2. Locate the decoupling capacitors close to the device to improve noise immunity.
3. Locate the V_{CC} capacitor very close to the device to prevent the circuit from entering a UVLO fault condition because of noise.
4. Locate the output voltage sense resistor close to the output load points.
5. Minimize the current sense trace. It can become easily polluted with noise.
6. Minimize the distance between the feedback opto−coupler and controller because this trace is also easily polluted.
7. Minimize the distance between the MOSFET and controller because the PCB trace is high frequency and high current so it can easily pollute other parts of the circuit.

Additionally, there are three pins in the NCP1271 that may need external decoupling capacitors.

1. Skip/latch pin (Pin 1) – If the voltage on this pin is above 8.0 V, the circuit enters latch−off protection mode. Hence, a decoupling capacitor on this pin is essential to improve noise immunity. Additionally, a resistor should always be placed from this pin to GND to prevent noise from causing the pin 1 level from exceeding the latch−off level.
2. Feedback pin (Pin 2) – A small capacitor may be necessary here for improved stability and noise immunity.
3. V_{CC} pin (Pin 6) – The NCP1271 maintains normal operation when V_{CC} is above $V_{CC(off)}$ (9.1 V typical). If V_{CC} drops below $V_{CC(off)}$, then the circuit enters UVLO protection and restarts after a double hiccup. Therefore, if V_{CC} inadvertently drops below $V_{CC(off)}$ due to switching noise, then the circuit will recognize it as a fault condition. Hence, it is important to locate the V_{CC} capacitor and a ceramic decoupling capacitor as close as possible to the NCP1271.

MEASUREMENTS

Standby Performance

Thanks to the features in the NCP1271, the evaluation board power supply offers excellent no load and light load standby performance. The 230 Vac power consumption of the 57 W circuit is only 83 mW. And the input power at 230 Vac with 500 mW load is only 710 mW. Figure 15 shows the efficiency with output loads from 500 mW to 60 W at 120 Vac and 230 Vac.

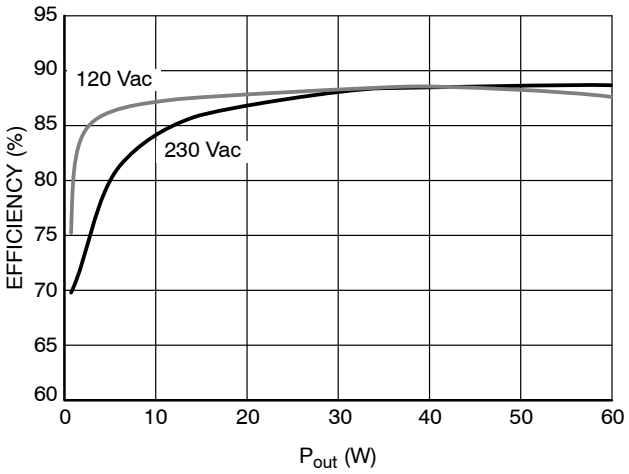

Figure 15. Efficiency of the NCP1271 Evaluation Board at Nominal Line Voltages

Dynamic Study

Figure 16 shows the startup transient waveforms of the circuit when the input is 110 Vac. A 4 ms soft−start is observed in the drain current. The V_{FB} drops below 3.0 V after 32 ms. Since this is shorter than the 130 ms fault validation time, the circuit does not enter fault condition and starts up normally.

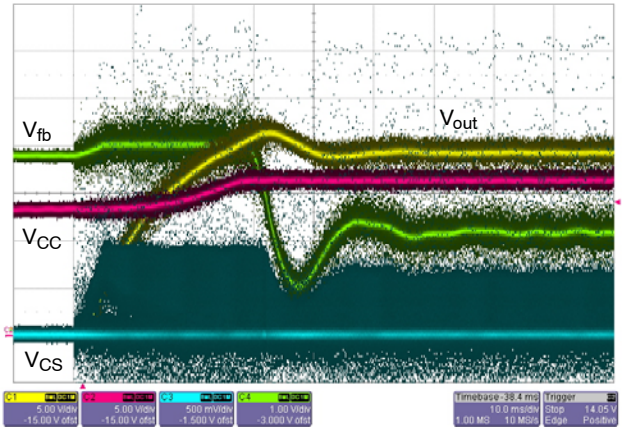

Figure 16. Startup Transient

Figure 17 shows the go−to−standby transition from full load operation. The output voltage (yellow trace) does not consume current and remains at 19 V, but the V_{CC} voltage drops from 16 V to 15 V because the V_{CC} auxiliary winding is not supplying current to the controller. The minimum V_{CC} voltage in the transition can be as low as 12 V. This is why the 16 V biasing voltage was selected to maintain V_{CC} above $V_{CC(off)}$ and prevent a V_{CC} reset.

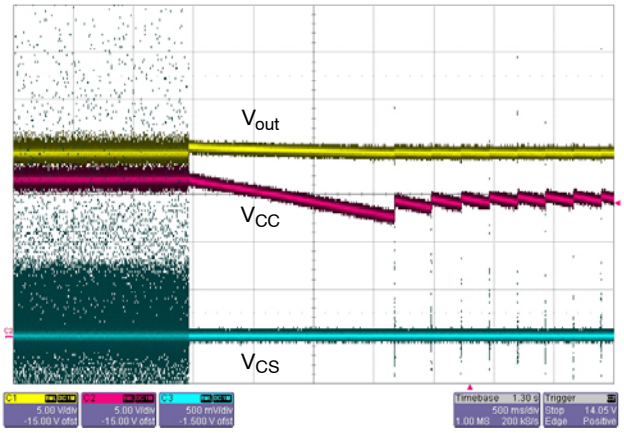

Figure 17. Operating to Standby

Short Circuit Protection Measurements

Figure 18 details the operation of the short circuit protection . The load steps from 60 W to 100 W, causing the peak current to increase to its maximum (1 V) as shown by the blue CS voltage. After approximately 130 ms, the controller shuts the power supply down and enters double hiccup fault operation (Figure 19). This provides very low power dissipation and protects the power components. When the short circuit fault is removed, the application recovers by executing a soft start and bringing the output back to 19 V.

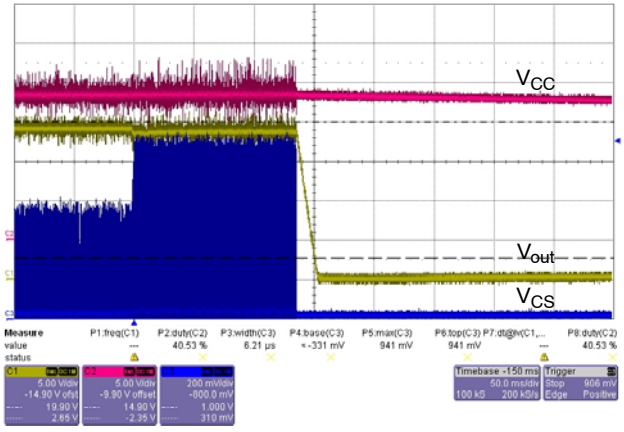

Figure 18. Short Circuit Protection is Activated When the Output Load Increases to about 100 W

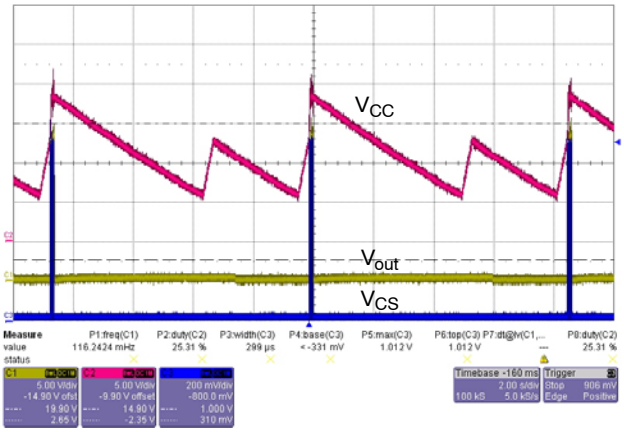

Figure 19. The Controller Enters Double Hiccup Fault Operation during a Continuous Short Circuit Event

Conclusion

A 57 W flyback power supply featuring over voltage and short circuit protection using the NCP1271 was demonstrated to have excellent light load power dissipation and active mode efficiency. The NCP1271's proprietary Soft−Skip™ operation offers low−audible−noise and excellent standby performance. The NCP1271 design worksheet, as well as other design aid resources, are available at www.onsemi.com.

TEST PROCEDURE

Required Equipment

- >100VA 1-to-1 Isolated Transformer at AC line voltage
- AC Power Supply with sinusoidal voltage output, 50 to 60 Hz, 85 to 264 Vac, at least 80 W
- Digital Power Meter with low-power-range power consumption measurement capability
- Oscilloscope or Voltmeter
- NCP1271EVB Evaluation Board
- Electronic Load that can handle at least 6.4 A 19 V 57 W

Test Procedure

1. Connect the equipment as shown in Figure 20.
2. The electronic load is will draw up to 3 A in constant current mode. Make sure that the wires connecting between the electronic load and evaluation board can handle 3 A current.
3. Set the AC Power Supply to 85 Vac. Limit the maximum input current to 2 A.
4. Then, turn on the system and apply an 85 Vac input to the Evaluation Board with no load on the output.
5. Check if the output voltage is close to the nominal output 19 V and stable (no bouncing around). Note that there may be significant voltage drop across the output wire.
6. Increase the load to 3A and check that the output voltage is 19 V.
7. Sweep the input voltage up to 264 Vac with 3A load on the output. Ensure that the output is 19 V and there is no noise.
8. Decrease the output load to 0.5 A and sweep the input voltage from 264 Vac to 85 Vac. Ensure that the output is 19 V and there is no noise.

NOTE: High Voltage is dangerous. Please be extra careful when dealing with high voltage.

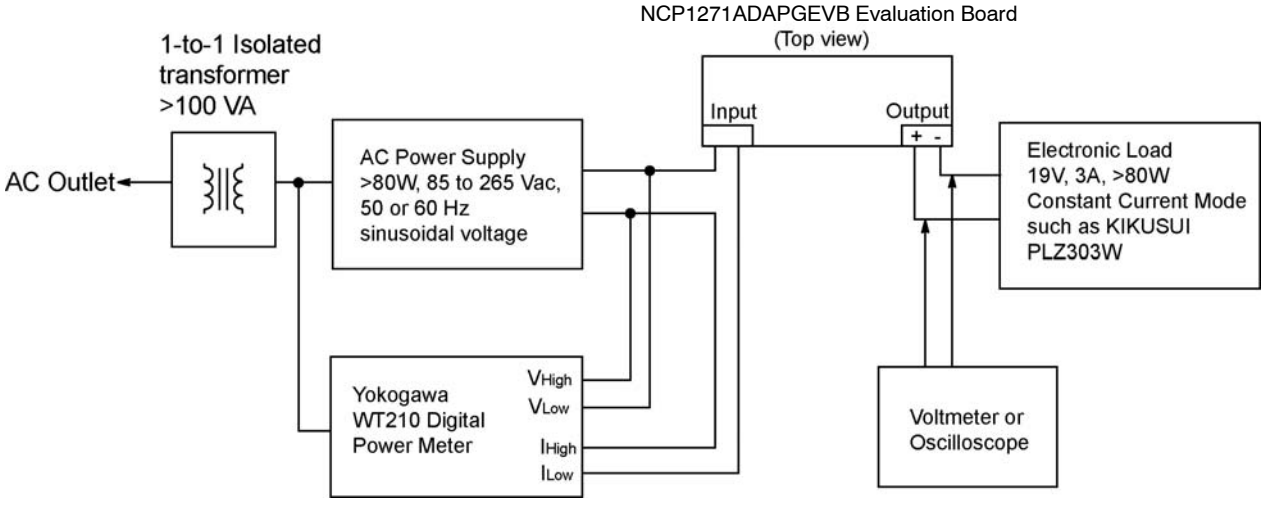

Figure 20. Test Setup

Table 2. BILL OF MATERIAL

Desig-nator	QTY	Description	Value	Toler-ance	Footprint	Manufacturer	Manufacturer Part Number	Substi-tution Allowed	Lead Free
T1	1	Common Mode Line Choke	3 A, 508 μH	N/A	N/A	Coilcraft	E3506-AL	Yes	Yes
T2	1	Custom Transformer 180 μH Primary inductance, turn ratio = 30:6:5, 2.5 μH max leakage	180 μH, 30:6:5	10%	N/A	Cooper/ Coiltronics	CTX22-17179	Yes	Yes
IC1	1	65kHz Flyback PWM Controller, SO-7	N/A	N/A	SO-7	ON Semiconductor	NCP1271D65R2	No	Yes
IC3	1	Opto coupler	CTR 50-600%	N/A	SMD-4	Vishay	SFH615AA-X007	Yes	Yes
IC4	1	Voltage Reference	2.5 V	1%	SO-8	ON Semiconductor	TL431AIDG	No	Yes
D1 - D4	4	Standard Diode	3 A, 600 V	N/A	Axial	ON Semiconductor	1N5406G	No	Yes
D5	1	Switching Diode	100 V	N/A	SOD-123	ON Semiconductor	MMSD914T1G	No	Yes
D6	1	Standard Diode	1 A, 600 V	N/A	SMA	ON Semiconductor	MRA4005T3G	No	Yes
D7	1	Ultrafast Diode	1 A, 600 V	N/A	SMB	ON Semiconductor	MURS160T3G	No	Yes
D8	1	3A 100V Schottky diode, axial 267-05	3 A, 100 V	N/A	Axial	ON Semiconductor	MBR3100G	No	Yes
D10	1	18V Zener Diode	18 V, 14 mA	5%	Axial	ON Semiconductor	MZP4746ARLG	No	Yes
Q1	1	N-Channel Mosfet	6 A, 800 V	N/A	TO-220AB	Infineon	SPP06N80C3	Yes	Yes
R1	1	Leaded Resistor	100 kΩ, 2 W	5%	Axial	Digi-key	P100KW-2BK	Yes	Yes
R2	1	Leaded Resistor	10 Ω, 1/4 W	5%	Axial	Yageo	CFR-25JB-5210R	Yes	Yes
R5	1	Ceramic Chip Resistor	30.1 kΩ, 1/4 W	1%	1206	Vishay	CRCW12063012FE3	Yes	Yes
R6	1	Ceramic Chip Resistor	10 Ω, 1/4 W	1%	1206	Vishay	CRCW120610R0FE3	Yes	Yes
R7	1	Ceramic Chip Resistor	511 Ω, 1/4 W	1%	1206	Vishay	CRCW12065110FE3	Yes	Yes
R8	1	Ceramic Chip Resistor	0.25 Ω, 1 W	1%	2512	Vishay	WSL2512R2500FEA	Yes	Yes
R9, R10	2	Ceramic Chip Resistor	1.69 kΩ, 1/4 W	1%	1206	Vishay	CRCW12061691FE3	Yes	Yes
R11	1	Ceramic Chip Resistor	15.8 kΩ, 1/4 W	1%	1206	Vishay	CRCW12061582FE3	Yes	Yes
R12	1	Ceramic Chip Resistor	2.37 kΩ, 1/4 W	1%	1206	Vishay	CRCW12062371FE3	Yes	Yes
C1-C2	2	Ceramic X2 Capacitor	0.1 μF, 275 V	10%	N/A	Evox Rifa	PHE840MA6100MA04	Yes	Yes
C3	1	Electrolytic Capacitor	82 μF, 400 V	20%	N/A	Panasonic	ECOS2GP820BA, or EETED2G820BA	Yes	Yes
C4, C13	2	Electrolytic Capacitor	100 μF, 25 V	20%	N/A	Panasonic	ECA1EM101	Yes	Yes
C5	1	Polyester Film Capacitor	10 nF, 630 V	10%	N/A	Newark	DME6S1K	Yes	Yes
C6 - C7	2	Ceramic Chip Capacitor	1.2 nF, 25 V	10%	1206	Vishay	VJ1206Y122KXXA	Yes	Yes
C8 - C10	3	Electrolytic Capacitor	2200 μF, 25 V	20%	N/A	Rubycon	025YXG2200M12.5X30	Yes	Yes
C11	1	Ceramic Y2 Capacitor	1 nF, 1 kV	20%	N/A	Evox Rifa	ERO610RJ4100M	Yes	Yes

Table 2. BILL OF MATERIAL

Desig-nator	QTY	Description	Value	Toler-ance	Footprint	Manufacturer	Manufacturer Part Number	Substi-tution Allowed	Lead Free
C12	1	Ceramic Chip Capacitor	0.15 μF, 25 V	10%	1206	Vishay	VJ1206Y154KXXA	Yes	Yes
Fuse	1	Time Delay Fuse	2 A, 250 V	N/A	N/A	Cooper	1025TD2-R	Yes	Yes
Heat−sink	1	Heatsink for TO-220 Package	11.2°C/W	N/A	N/A	Aavid	590302B03600	Yes	N/A
Heat−sink Insulation	1	Mica Insulation for TO-220 Package	N/A	N/A	N/A	Keystone	4672	Yes	N/A
Heat−sink Washer	1	Nylon #4 Shoulder Washer	N/A	N/A	N/A	Keystone	3049	Yes	Yes
AC Connector	1	IEC60320 C8 Connector	2.5 A 250 Vac 770 W	N/A	N/A	Qualtek	770W-X2/10	Yes	Yes
DC Connector	1	3-terminal 3.96 mm pitch male header	N/A	N/A	N/A	Molex	26-60-4030 or 009652038	Yes	Yes
Stand off	4	Standoff M/F Hex 4-40 Nyl 0.750”	N/A	N/A	N/A	Digi-key	4804K	Yes	N/A
Accessories	1	4-40 1/4 inch screw	N/A	N/A	N/A	Newark	30F698	Yes	N/A
Accessories	5	4-40 screw nuts	N/A	N/A	N/A	Newark	31F2106	Yes	N/A

NCP1271 57 W Adaptor Layout

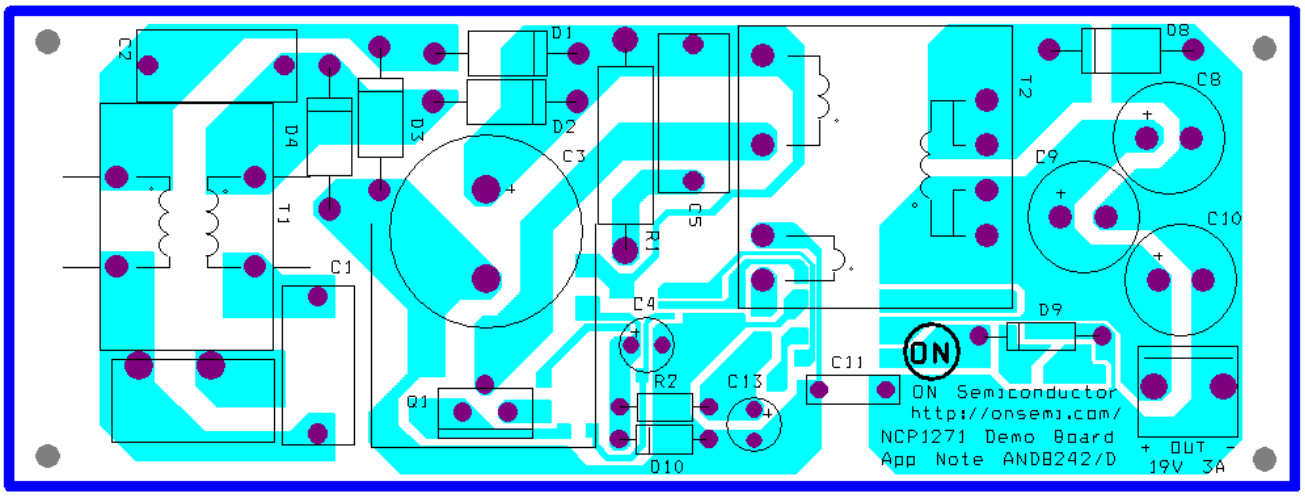

Figure 21. Top View

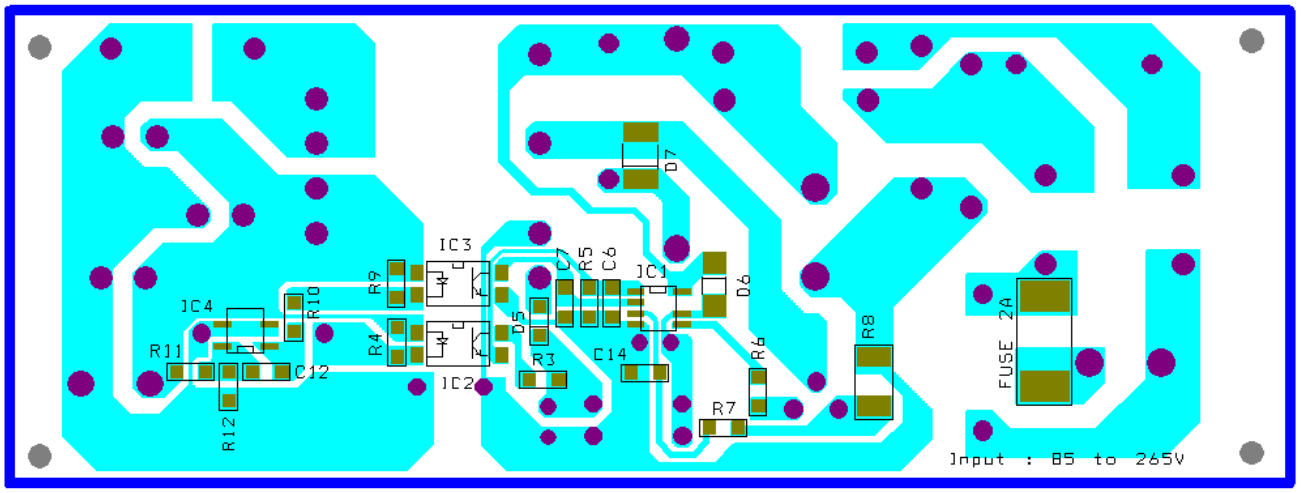

Figure 22. Bottom View

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